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Design and Analysis of a High Speed, Power Efficient 8 Bit ALU Based on SOI / SON MOSFET Technology

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This paper shows an overall performance comparative analysis in terms of Average Power Consumption, Average Delay and Power-Delay Product for an 8 bit Arithmetic Logic Unit (ALU) using bulk MOS, Silicon-on-Insulator (SOI) and Silicon-on-Nothing (SON) technology. The entire design is done in 32nm technology for all the three cases (Bulk, SOI & SON) and then compared. The comparisons have been carried out with the help of the simulation runs on Synopsys HSpice tool, and that clearly indicates, for lower Supply Voltages (V_{dd}), SOI / SON technology provides a significant reduction in Average Power Consumption, Average Delay and Power-Delay Product compared to that of Bulk MOS technology.

Keywords: Arithmetic logic unit, Bulk MOS technology, Silicon-on-insulator (SOI) technology, Silicon-on-nothing (SON) technology.

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1. INTRODUCTION

Scaling beyond 50 nm technology node requires innovative approaches to overcome the barriers due to the fundamental physics that limits the conventional MOSFET. To overcome the limitations, new challenging technologies are coming under research and experiment. Because of scaling theory, bulk silicon device technology faces the power explosion of chips, where the future devices like SOI / SON / CNFET, are developed ensuring low power solution to IC implementation.

The advancement of VLSI technology has led to the growth of Integrated Circuit (IC) devices. With the blooming development of integrated circuits, many computing intensive applications such as multimedia processing, digital communication can now be realized in hardware to either speed up the operation or to reduce the power or energy consumption. Most of the Very Large Scale (VLSI) applications, such as digital signal processing and microprocessors, extensively use arithmetic (e.g., Addition, Subtraction, Multiplication etc.) and logical operations (e.g., NOT, NAND, AND, NOR, OR, XOR and XNOR etc.).

This paper describes the circuit design approaches to design an 8 bit Arithmetic Logic Unit (ALU) using SOI/SON technology. Here, we have considered ALU because it is the mostly used and a fundamental building block of the central processing unit of a digital computer. The ALU, heart of the processor, performs a number of arithmetic and logical operations as stated above. Here we have designed an 8 bit ALU circuit which performs eight arithmetic and four logical operations between two 8 bit variables depending on a particular combination of select inputs (specified by the user).

Figure 1 shows the block diagram of an 8 bit ALU circuit which performs our intended arithmetic and logical operations.

The internal circuit diagram of the 1bit ALU is shown in figure 2 which can perform the desired operations for only 1 bit data inputs. Now we have

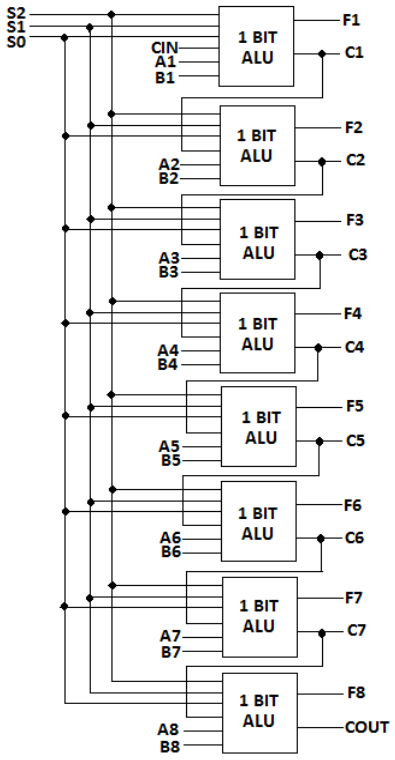

Fig. 1 – Block Diagram of 8 bit ALU

incorporated the block of 1 bit ALU circuit to design our 8 bit ALU which performs the same arithmetic and logical operations for 8 bit data inputs. The eight arithmetic and four logical operations are described in table 1 as follows. The particular combination of select inputs is responsible for a specific ALU operation which must be determined by the user.

Predictive Technology Model (PTM) and BSIM Model have been utilized for simulation of MOSFET and SOI circuits respectively at 32 nm technology [1]-[3]. A modified model of BSIMSOI has been used for SON circuit simulation purpose [4].

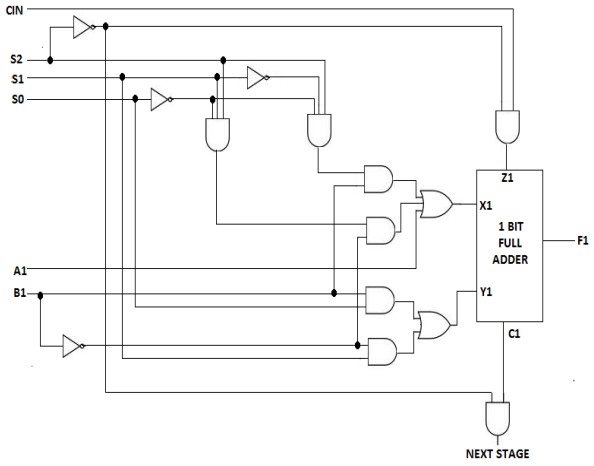

Fig. 2 – ALU circuit for 1 bit operation

Table 1 – Function Table of ALU Operation

S2	S1	S0	CIN	X_i	Y_i	Operation
0	0	0	0	A_i	0	A_iTransfer
0	0	0	1	A_i	0	A_iIncrement
0	0	1	0	A_i	B_i	Addwithoutcarry
0	0	1	1	A_i	B_i	Addwithcarry
0	1	0	0	A_i	B_i‘	Subtractwithoutborro
0	1	0	1	A_i	B_i‘	Subtractwith borrow
0	1	1	0	A_i	1	A_iDecrement
0	1	1	1	A_i	1	A_iTransfer
1	0	0	0	A_i	0	OR
1	0	1	0	A_i	B_i	XOR
1	1	0	0	A_i	B_i‘	AND
1	1	1	0	A_i	1	NOT

2. BULK, SOI AND SON TECHNOLOGIES

Over past few years, the process of realizing digital circuits has changed dramatically. Today‘s most of the electronic circuits are designed using traditional MOS technology which is a very mature technology with the three most important advantages like low manufacturing costs, high performance and good low-power consumption. However it will be increasingly difficult to reduce both chip size and average power consumption of bulk CMOS circuits. But increased demand for ultra-low power, high speed circuits is pushing the device fabrication process to go beyond the submicron technologies which could not be achieved with bulk CMOS process leading to an alternative, Silicon-on-Insulator (SOI) technology [5]. Instead of bulk silicon substrate, Silicon-on-Insulator MOS employs a buried oxide layer between the active device region and the silicon substrate which eliminates most of the parasitic capacitances found in bulk CMOS processes.

SOI MOS devices offer superior electrical characteristics over bulk MOS devices[6] such as reduced junction capacitances, increased channel mobility, suppresses short-channel effect, excellent latch-up immunity and improved sub-threshold characteristics[7]. SOI technologies allow significant reduction of the dynamic power consumption of large digital circuits and moreover SOI substrates offer the ability to integrate the passive elements with improved characteristics in the RF range [8]. These are very attractive options in terms of high speed, low power dissipation, latch-up and soft-error immunities, co-integration of digital and analog / RF circuits [9, 10].The development of SOI technology has been limited so far by the difficulty in controlling the silicon film thickness, adjusting buried oxide layer thickness, shallow source drain series resistances and the fringing fields [11-13]. Although different short channel effects (SCEs) are highly suppressed in SOI structure, SOI structure is not fully immune to different SCEs. Higher threshold voltage roll-off and degraded sub threshold slope are two important issues among different SCEs [14]. To overcome such types of drawbacks in conventional SOI structure, different improved SOI structures are proposed in recent times [15]. Our primary focus is on the fully depleted structure, because of its advantages over the partially depleted model. PD structure suffers from the basic floating body effect which in turn adds to the History effect [16, 17].

Silicon-on-Nothing (SON), an innovative SOI structure, proposed and developed recently, enables fabrication of extremely thin silicon and burieddielectric super SOI devices, which are capable of quasitotal suppression of SCEs and excellent electrical performances [18]. In SON technologies, the buried layer of usual SOI is replaced with air which causes less SCEs and leakage currents. The most significant advantage of fully depleted (FD) SON architecture comparing to FDSOI is the reduced electrostatic coupling of channel source/drain and substrate through buried layer (BL) which allows in turn to reduce the minimal channel length of transistors or to relax the requirements on silicon film thickness [19, 20]. Moreover, since the so-called “nothing”’ (air) layer embedded below the Si active film has lower dielectric permittivity than oxide, the parasitic capacitances between source/drain and substrate are reduced and therefore higher circuit speed can be expected with SON devices. Thick buried layer can be a drawback of SOI structure due to large positive charge accumulated in the thick BL, while in the case of SON structure; no charge will accumulate in the air gap [21]. Figure 3 shows the simple cross sectional structure of FDSOI and FDSON.

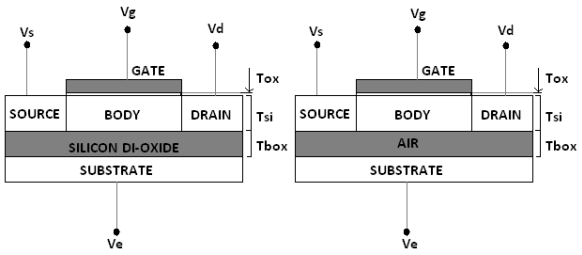

Fig. 3 – Cross sectional structure of a) FD-SOI; b) FD-SON

3. POWER CONSUMPTION AND PROPAGATION DELAY TIMEDEFINITIONS

The total power consumption in CMOS digital circuits can be expressed as the sum of four components [22],

$$P_{total} = \sum_i \alpha . C_{load} . V_{DD}^{\ 2} . f + V_{DD}(I_{short-circuit} + I_{leakage} + I_{static}) \quad (1)$$

Where $I_{short\text{-}circuit}$ denotes the average short circuit current, $I_{leakage}$ denotes the reverse leakage and sub-threshold leakage currents, and I_{static} denotes the DC current component drawn from the power supply. The switching power consumption, which is the first term in equation 1, is the most dominating component in most CMOS logic gates.

Here, α is the switching activity at node i, C_{load} is the load capacitance at node i, V_{dd} is the supply voltage, and f is the clock frequency.

Now, the propagation delay time has two components: τ_{PHL} and τ_{PLH}, which determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively. τ_{PHL} is defined as the time delay betweenthe $V_{50\%}$–transition of the rising input voltage and the $V_{50\%}$–transition of the falling output voltage. Similarly, τ_{PLH} denotes the time delay between the $V_{50\%}$–transition of the falling input-voltage and the $V_{50\%}$–transition of the rising output voltage.

We are concerned about only the average propagation delay τ_P of the CMOS inverter which indicates the averagetime required for the input signal to propagate through the inverter [22].

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} \tag{2}$$

Now, the power-delay product (PDP) is a fundamental parameter which is used for determining the quality and the performance of a CMOS process and gate design. The power- delay product can be physically defined as the average energy required for a gate to switch its output voltage from low to high and from high to low. It is expressed as [22],

$$PDP = 2P_{avg}\tau_P \tag{3}$$

where P_{avg} is the average switching power consumption at maximum operating frequency and τ_P is the average propagation delay. The factor 2 is accounted for two transitions of the output from low to high and from high to low.

4. RESULTSANDDISCUSSIONS

The comparison discussed in section 2 is verified here with circuit simulations. Table 2, 3and 4 show the comparative analysis of different performance parameters in terms of Average Power Consumption, Average Delay and PDP of the arithmetic and logic unit respectively using bulk MOS, SOI and SON technology for the same supply voltage(1V) and same operating frequency. Moreover, figures 5, 6 and 7 depict the graphical representation of the above stated three performance parameters of our 8 bit arithmetic and logic unit depending on the results obtained from the table 2, 3 and 4 as described below.

On the basis of the evaluation and comparison of the performance parameters of 8 bit ALU between 32nm Complementary Metal Oxide Semiconductor (CMOS)

Table 2 – Comparison of Average Power Consumption

Operation	CMOS (Watt)	SOI (Watt)	SON (Watt)
AjTransfer	3.12×10^{-7}	0.66×10^{-7}	0.63×10^{-7}
AjIncrement	4.87×10^{-7}	2.04×10^{-7}	1.93×10^{-7}
Addwithoutcarry	11.88×10^{-7}	5.99×10^{-7}	5.48×10^{-7}
Addwithcarry	4.45×10^{-7}	0.62×10^{-7}	0.59×10^{-7}
Subtractwithoutborrow	4.34×10^{-7}	0.71×10^{-7}	0.69×10^{-7}
Subtractwith borrow	2.26×10^{-7}	2.11×10^{-7}	1.95×10^{-7}
AjDecrement	11.92×10^{-7}	6.01×10^{-7}	5.40×10^{-7}
AjTransfer	4.48×10^{-7}	0.64×10^{-7}	0.62×10^{-7}
OR	4.17×10^{-7}	1.04×10^{-7}	0.96×10^{-7}
XOR	4.79×10^{-7}	0.57×10^{-7}	0.48×10^{-7}
AND	4.42×10^{-7}	2.23×10^{-7}	2.21×10^{-7}
NOT	4.69×10^{-7}	1.16×10^{-7}	1.06×10^{-7}

Table 3 – ComparisonofAverageDelay

Operation	CMOS (sec)	SOI (sec)	SON (sec)
AjTransfer	2.47×10^{-12}	1.60×10^{-12}	1.41×10^{-12}
AjIncrement	3.53×10^{-12}	2.27×10^{-12}	1.66×10^{-12}
Addwithoutcarry	4.09×10^{-12}	2.43×10^{-12}	2.02×10^{-12}
Addwithcarry	2.38×10^{-12}	1.55×10^{-12}	1.43×10^{-12}
Subtractwithoutborrow	2.47×10^{-12}	1.60×10^{-12}	1.41×10^{-12}
Subtractwith borrow	3.54×10^{-12}	2.27×10^{-12}	2.16×10^{-12}
AjDecrement	3.28×10^{-12}	1.79×10^{-12}	1.61×10^{-12}
AjTransfer	2.38×10^{-12}	1.55×10^{-12}	1.28×10^{-12}
OR	2.47×10^{-12}	1.59×10^{-12}	1.41×10^{-12}
XOR	2.47×10^{-12}	1.60×10^{-12}	1.57×10^{-12}
AND	2.47×10^{-12}	1.60×10^{-12}	1.57×10^{-12}
NOT	2.55×10^{-12}	1.88×10^{-12}	1.52×10^{-12}

Table 4 – ComparisonofPower-Delay Product (PDP)

Operation	CMOS (Joule)	SOI (Joule)	SON (Joule
AjTransfer	1.54×10^{-16}	0.21×10^{-16}	0.18×10^{-16}
AjIncrement	3.45×10^{-16}	0.92×10^{-16}	0.64×10^{-16}
Addwithoutcarry	9.72×10^{-16}	2.92×10^{-16}	2.21×10^{-16}
Addwithcarry	2.12×10^{-16}	0.19×10^{-16}	0.17×10^{-16}
Subtractwithoutborro	2.15×10^{-16}	0.26×10^{-16}	0.19×10^{-16}
Subtractwith borrow	1.59×10^{-16}	0.96×10^{-16}	0.84×10^{-16}
AjDecrement	7.83×10^{-16}	2.15×10^{-16}	1.74×10^{-16}
AjTransfer	2.14×10^{-16}	0.19×10^{-16}	0.16×10^{-16}
OR	2.06×10^{-16}	0.33×10^{-16}	0.27×10^{-16}
XOR	2.37×10^{-16}	0.18×10^{-16}	0.15×10^{-16}
AND	2.18×10^{-16}	0.71×10^{-16}	0.69×10^{-16}
NOT	2.39×10^{-16}	0.44×10^{-16}	0.32×10^{-16}

technology, SOI and SON, clear superiority of the future devices can be observed. The above results and analysis clearly indicate that SON is more suitable for circuit design rather than MOSFETs.

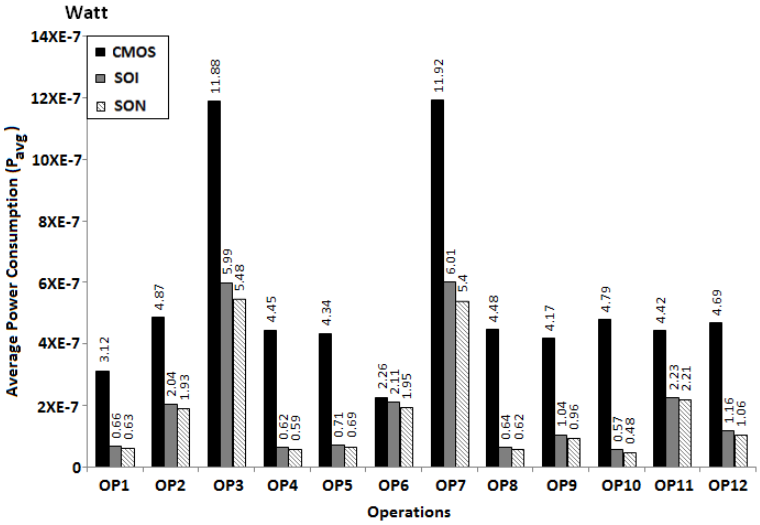

Fig. 5 – Details of average power consumption

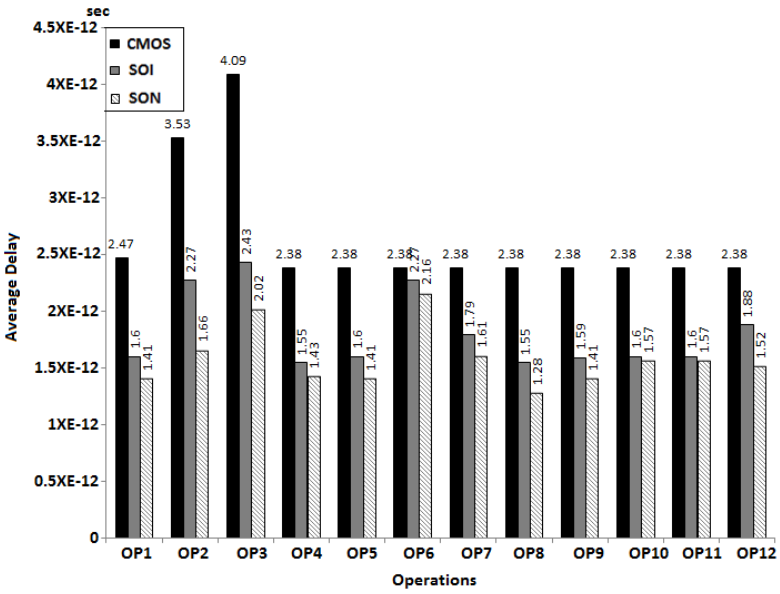

Fig. 6 – Details of average delay

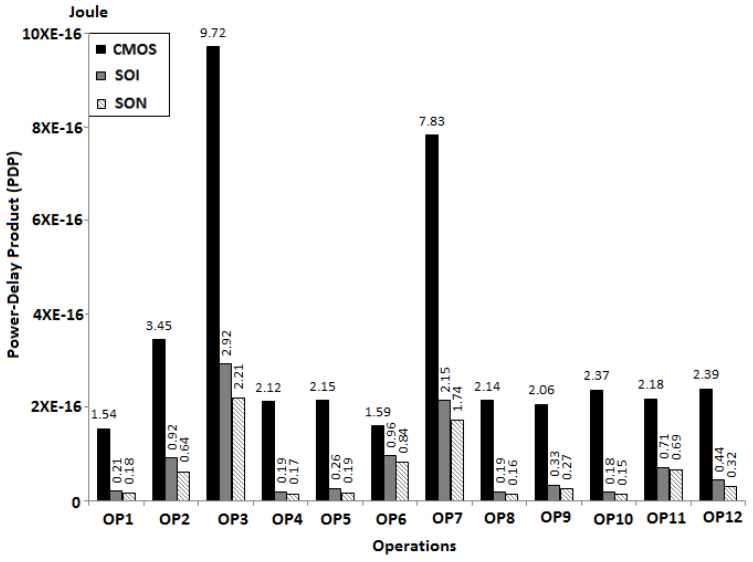

Fig. 7 – Details of power-delay product (PDP)

5. CONCLUSIONS

In this paper, we have implemented the 8 bit ALU using the devices like, CMOS, SOI and SON in 32 nm technology. Through this paper, power consumption and delay for each arithmetic and logical operation is compared for each of the devices and a significant improvement is noticed over MOSFET. Simulation results show an improvement of 63.63 % for SOI and 66.36 % for SON in terms of average power consumption. As far as the average delay is concerned, the results show an efficient improvement of 36.27 % for SOI and 44.01 % for SON circuits compared to MOSFET circuits.

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