Nanofabrication of gallium nitride photonic crystal light-emitting diodes

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ABSTRACT

We describe a comparison of nanofabrication technologies for the fabrication of 2D photonic crystal structures on GaN/InGaN blue LEDs. Such devices exhibit enhanced brightness and the possibility of controlling the angular emission profile of emitted light. This paper describes three nano lithography techniques for patterning photonic crystal structures on the emitting faces of LEDs: direct-write electron beam lithography, hard stamp nanoimprint lithography and soft-stamp nanoimprint lithography with disposable embossing masters. In each case we describe variations on the technique as well as its advantages and disadvantages. Complete process details have been given for all three techniques. In addition, we show how high performance GaN dry etch techniques, coupled with optical process monitoring can transfer resist patterns into underlying GaN material with high fidelity.

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1. Introduction

Light-emitting diode (LED) technology is undergoing extremely rapid developments at this time. Many academic, government and industrial laboratories across the world are working on improving their efficiency and lifetime while at the same time bringing down their cost so that they can replace more conventional light sources in a variety of applications [1,2]. Nitride semiconductors from the GaN family provide the current materials technology for emitters in the blue and green, and achieve external quantum efficiencies up to ∼60% for packaged blue LED lamps [3]. Phosphide semiconductors meanwhile continue to offer the highest performance at red visible wavelengths. LED-based illumination has been taking over in sectors such as traffic lights and automobile lighting and is now set to make bold strides into areas such as car headlights and street lighting. Electronics manufacturers are also particularly interested in utilising LEDs for backlights in LCD televisions and later on for general purpose room lighting applications. The opportunities to develop LEDs with tailored angular emission profiles for more specialised applications, including backlights, projectors and fibre optic communications, are also significant. Harbers et al. give a recent discussion of the potential for LED solutions in the first two application areas [4]. Incorporation of a photonic crystal structure on the emitting face of LEDs is now recognised as perhaps the most important technology for adapting LEDs to various application requirements. The fabrication techniques for photonic crystal (PhC) and photonic quasi-crystal (PhQC) LEDs described in this paper will have their first commercial impact in applications requiring increased brightness and optimised angular emission profiles as prime considerations.

All inorganic LEDs generate light inside a high-index medium, and this factor limits the efficiencies attained by simple planar device architectures. This feature arises due to total internal reflection of a large fraction of light within the high refractive index GaN epitaxial layers. As a result, much of the light remains confined as trapped modes inside these layers. The numerical extraction efficiency is only ∼4% for GaN-based devices coupling directly into air, but can be increased up to ∼10% by encapsulation with a transparent polymer [5]. Several other techniques have been developed to extract even more of the internally trapped radiation. These include random surface roughening [6], use of corrugated or patterned substrates [7,8] and patterning the LED surface with a photonic crystal structure [9–12]. PhC and PhQCs function by coupling modes trapped in high-index material into modes which

can escape. In this context, the possibility of fabricating thin device structures by laser lift-off (LLO) processing of GaN-based epitaxial structures grown on sapphire is very important [13]. This is because such techniques remove sapphire and thus modes trapped in sapphire and also maximise the interaction between trapped modes in GaN and the etched PhC structures. The interaction of guided modes with a PhC/PhQC grating can be maximised when the total GaN thickness is reduced to only a few microns [3]. Furthermore, heat dissipation is also greatly improved over conventional devices, as heat transport through sapphire substrate is replaced by much more efficient heat transfer through metallic back contacts. LLO was recently used in the fabrication of thin GaN-based PhC LEDs with a record extraction efficiency exceeding 70% for non-encapsulated devices [14].

In addition to improvement of extraction efficiencies, PhC and PhQC patterning allows tailored modifications to the polar radiation characteristics of LEDs from the near-Lambertian pattern obtained using planar non-encapsulated devices. Much attention has been focussed on enhancing emission in directions close to the surface normal, as desirable in étendue-limited applications [3,15]. However, it is also possible to design PhC and PhQC patterns which cause preferential light emission at large angles to the surface normal, as desirable for certain forms of display backlights; specifically direct illumination of flat panels [16]. Here highly homogeneous illumination of the applications plane is critical. PhQC patterns departing from traditional crystallographic symmetry offer major advantages over their regular PhC counterparts by virtue of the azimuthal uniformity of emission [3,16,17].

All implementations of PhC and PhQC patterns in visible LEDs require a sub-micron patterning capability, and a brief overview of techniques available is included in Ref. [3]. In this paper, we report on direct-write electron beam lithography (EBL), and two different embodiments of nanoimprint lithography (NIL). NIL techniques have superior potential for mass production, and Watts et al. reviewed currently available fabrication equipment and economic considerations [18]. In all process flows, the PhC/PhQC pattern is first transferred into a mask layer, and must then be transferred into the semiconductor material by a dry etch process, allowing good control over the hole depth and sidewall profile. Currently most PhC and PhQC designs assume vertical sidewalls, and etch processes must therefore offer a high degree of anisotropy to approximate this idealised geometry in the real device. For GaN-based devices, conventional and thin LEDs made by LLO have different constraints on hole depth, as can be understood with reference to the typical *p–i–n* device structure on sapphire shown in Fig. 1. The topmost *p*-type layers of commercial LED wafers above the active region are normally kept to a thickness of ∼150 nm. Therefore in devices with the conventional (so-called *p*-up) geometry, the PhC/PhQC hole etch depth cannot exceed this value without catastrophic shorting of the junction, and/or etch damage to the active region. In contrast, in thin GaN devices made by LLO processing, the depth of holes etched into *n*-type GaN can be significantly greater, as illustrated by published device results [14,19].

This paper presents results from the integrated development and optimisation of patterning and dry etch nanofabrication technologies, with particular reference to GaN-based LEDs. We show results on the processing of as-grown GaN LED wafers on sapphire, corresponding to process flows for conventional *p*-up LEDs. Fig. 1 shows the structure of a typical device. However, the processing techniques developed are applicable to thin GaN devices made by LLO routes, as well as to LEDs fabricated from non-nitride materials. The results to date have been obtained using 2-inch sapphire based wafers. However, the techniques developed are applicable to GaN device structures on larger sapphire wafers [20], and lower-cost large silicon substrates [21]. Both these approaches are being actively pursued to reduce the epitaxy-related cost component of
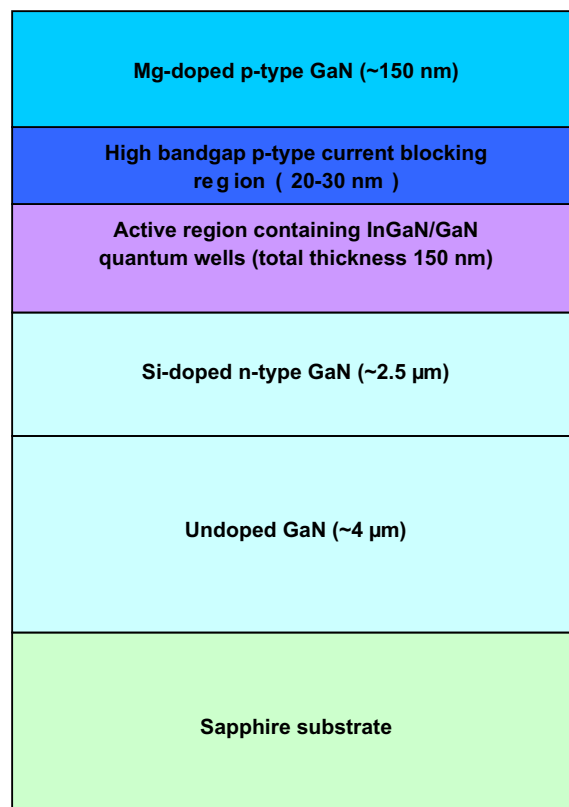

Fig. 1. Structure of a typical epitaxial GaN blue LED wafer material showing the positions and thicknesses of various layers.

GaN LEDs. Our specific motivation concerned the development of PhQC LEDs for direct flat panel backlighting. Results on the performance characteristics of devices made by optimised fabrication routes will be reported elsewhere.

2. PhC nanofabrication with direct-write e-beam lithography

Direct-write e-beam lithography has been used for many years to write nanometre-scale features on semiconductors. Photonic crystal structures consisting of arrays of holes, several hundred nanometres in diameter and spaced a few hundred nanometres apart, can be, and are, easily written by e-beam lithography. This technique, though not suitable for commercial production, is very well suited to R&D operations as no masks or stamps need to be prepared. We have carried out PhC patterning using the direct-write technique with a view to explore the suitability of various resists for defining these structures.

In this work we patterned a 12-fold photonic quasi-crystal design [22] with different hole diameters and pitch on GaN LED epi-layer wafers. It has been proved that by changing the hole diameter and/or pitch the emission profile of photonic crystal LEDs could be modified [23]. Various e-beam resists such as Hydrogen SilsesQuioxane (HSQ) – a silica-based resist, NEB31 – a chemically-amplified resist from Sumitomo, ZEP-520A a non chemically-amplified resist from Nippon Zeon and PolyMethyl MethAcrylate (PMMA) were used to write PhC patterns. HSQ and NEB31 are negative tone resists whereas ZEP-520A and PMMA are positive tone resists. Leica VB6 e-beam tool was used to write patterns on commercial 2" GaN LED epi-layer wafers – sourced form Lumi-innovations. VB6 is a very high resolution machine and can produce e-beam spot sizes down to around 4 nm diameter on a design grid of 1.25 nm.

GaN LED epi-layer wafers were cleaned with acetone, methanol, isopropanol and purified water before spinning on resist. All GaN samples were coated with 200 nm thick resist. It was found that 30 nm of an Aluminium (Al) layer on top of the resist mask gives very high quality patterns − Al layer acts as a discharge layer for e-beam lithography. It was also found that HSQ has a number of advantages over other e-beam resists such as:

1. HSQ acts as a direct hard mask for dry-etching. While using HSQ there is no need to use a separate metal hard mask. We found no significant change in the 200 nm HSQ mask during the etching of up to 300 nm of GaN LED epi-layer wafer. With other e-beam resists, such as ZEP-520A or PMMA, we needed to use a metal hard mask such as a NiCr mask on top of the e-beam resist [24].
2. It is not sensitive to white light. We deposited 30 nm of Al layer on the top of resist to act as a discharge layer for e-beam writing. The Al layer was deposited by using a Plassys e-beam evaporator tool. It was found that NEB31 resist was exposed during a similar deposition of Al layer.
3. HSQ can be easily removed from GaN LED epi-layer wafers using buffered HF.

With HSQ, the best e-beam dose was found to be 700–800 µC/cm^2 at 100 kV e-beam accelerating voltage. This was determined by using a dose estimation matrix. The hole size can be varied by changing the e-beam dose [25]. The criterion chosen for the best e-beam dose was the achievement of exactly the same size hole diameter in the HSQ resist as was provided in simulated designs. Each sample contained an array of 4×4 patterns together with four alignment markers. These alignment markers were used to fabricate n and p contact after dry-etching of the photonic crystal pattern. Each pattern had dimensions of 300×300 µm. Samples also contained blank devices. These blank devices were intended to compare LEDs with and without PhQC pattern. After e-beam writing the samples were developed in Tetra Methyl Ammonium Hydroxide (TMAH) resist developer and inspected under an optical microscope. Patterns in HSQ were transferred to the epi-layer by a chlorine-based dry etch process that is described in Section 5. After dry-etching some samples were cleaved and their plan and cross-sectional views obtained with an SEM. Some representative micrographs appear in Fig. 2 here.

## 3. PhC nanofabrication with rigid stamp nanoimprint lithography

Direct-write e-beam lithography is a serial process and is thus far too slow for use as a viable commercial patterning process. Patterning even a full 2 in. diameter wafer with PhC patterns using this technique will cost upwards of $10 K which is clearly unacceptable. Nanoimprint lithography (NIL) has emerged in recent years as an affordable technique for the mass replication of submicron size structures over large areas. Micro and nano optics are the areas where NIL has been especially popular and thus commercial PhC patterning has been mostly carried out with this technique. Among the advantages of NIL are relatively low cost of capital equipment and high production speed which combine to make NIL patterning very affordable [26]. We have explored the two basic variants of NIL to imprint PhC patterns on GaN LED wafers with a view to understand yield limiting factors.

In this work the following two rigid stamps NIL approaches were used.

1. Heat and pressure NIL
2. Flash imprint NIL

3.1. Heat and pressure (H&P) NIL

A silicon stamp was first fabricated for H&P NIL. A clean 15×15 mm Si substrate with a thickness of 500 µm was spin coated with HSQ. An inverse design of PhQC was transferred to
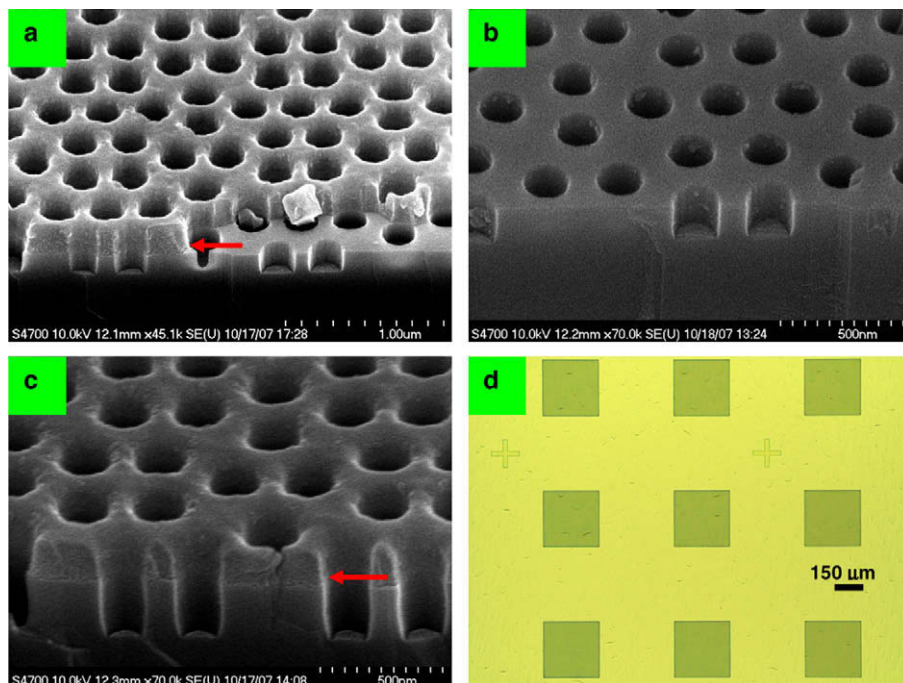
Fig. 2. (a) SEM micrograph of GaN epi-layer wafer. Arrow indicates interface between HSQ and GaN epi-layer wafer. The etching depth is ~150 nm. (b) SEM micrograph of GaN epi-layer wafer after removing HSQ by using buffered HF. (c) SEM micrograph of GaN epi-layer wafer with HSQ. Arrow indicates interface between HSQ and GaN epi-layer wafer. Etching depth is ~300 nm. Note: No significant change has been observed in HSQ after etching 300 nm GaN epi-layer wafer by using ICP tool. (d) Optical micrograph of GaN epi-layer wafer with 300×300 µm patterns with alignment markers.

HSQ by using e-beam lithography. The design was further transferred to the Si substrate by inductively coupled plasma (ICP) dry-etching [27]. The gas used for dry-etching was SF_6/C_4F_8. The dry-etching depth was found to be 260 nm as measured under SEM.

This work used a commercial nanoimprint tool called nanoimprint from Obducat in Sweden. The commercially available NIL polymer mr-I-9020 [28] was spin coated on GaN epi-layer wafer at 2000 RPM. The Si stamp was placed face down on the GaN epi-layer wafer. The entire assembly was then placed in the nano-imprinter. The glass transition temperate (T_g) of mr-I-9020 is above 100 °C. The temperature was raised above the T_g to 120 °C and a pressure of 40 Bar was applied. At high temperatures the viscosity of the polymer is low enough to fill all the cavities in the stamp. After a few minutes the polymer started cross-linking and this caused an increase in viscosity. The polymer solidified and the shape formation of the imprint finished after 15 min. The stamp was detached from the GaN LED epi-layer wafer at a temperature below the T_g of mr-I-9020. During the H&P NIL process,

pressure was used to keep the Si stamp attached with the substrate during the stamp cavity filling process.

After imprinting the GaN LED epi-layer wafer was examined under SEM. Very encouraging results were achieved with H&P NIL, as seen in Fig. 3. It was found that this NIL technique could be used to imprint on smooth as well as on rough surfaces. The disadvantage of H&P NIL technique is that, due to its slow speed, it cannot be used for industrial production and for processes that need alignment of the stamp with the substrate.

3.2. Flash NIL

Flash NIL requires UV exposure for cross-linking the NIL resist. For this reason, a quartz stamp was prepared for flash NIL. In this work a quartz substrate having dimensions of 65×65 mm and thickness of 6 mm was used. NEB31 negative tone e-beam resist was spin coated on quartz substrate. NEB31 mask has an advantage over HSQ in that its etch rate is lower during quartz etching. An Inverse PhQC pattern with pillars of 550 nm diameter was written on
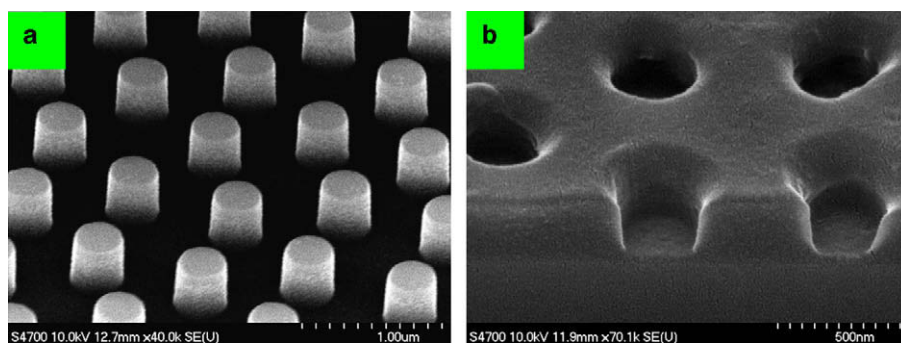

Fig. 3. (a) SEM micrograph of silicon stamp after dry-etching by using ICP tool. HSQ was removed by using buffered HF. (b) SEM micrograph of pattern imprint patterns on GaN epi-layer by using an Obducat nanoimprint imprinter tool.
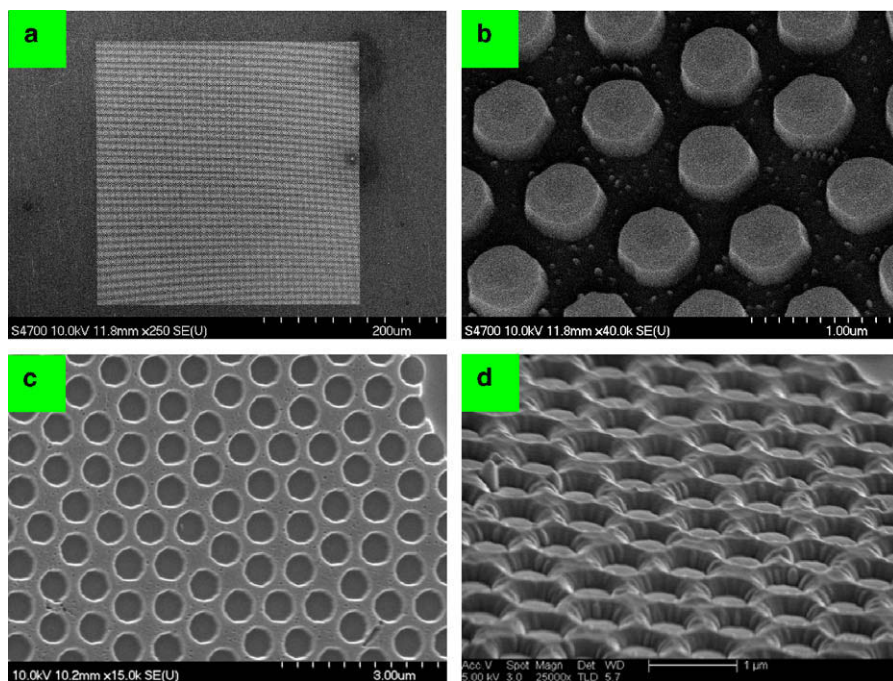

Fig. 4. (a) SEM micrograph of 300×300 µm pattern fabricated on Quartz stamp by using e-beam lithography and dry-etching. (b) SEM micrograph of Quartz stamp at high magnification. (c) SEM micrograph of GaN epi-layer wafer after imprinting by using the flash NIL technique. (d) SEM micrograph of GaN epi-layer wafer after the pattern was transferred into GaN by using the ICP tool.

NEB31 resist. BP80 dry etch machine and CHF_3 gas were used for dry-etching the quartz substrate. After dry-etching the patterns were examined under SEM. Vertical etching profile with depth of 180 nm was found in SEM.

In this work the commercially available flash NIL polymer mr-UVCUR06 [29] was spin coated on GaN epi-layer wafer at 3000 RPM. After spinning the sample was baked at 90 °C for 60 s. Flash NIL was done by using the hard contact mode of an MA6 mask aligner. The sample was exposed to UV for 5 min. After flash NIL, the substrate was cleaved and observed under SEM. It was found that the thickness of the residual layer was 20 nm whereas the NIL feature depth was 180 nm. SEM micrographs are shown in Fig. 4.

4. PhC nanofabrication with flexible stamp nanoimprint lithography

Rigid stamp nanoimprint lithography has its limitations. Frequently encountered problems include release from the master, stitching errors in the step and repeat process, damage to bowed wafers, especially in high-pressure imprint processes and clearing the inevitable residual layer when device fabrication involves pattern transfer into the underlying substrate. An alternative wafer-scale nanoimprint process is to use flexible stamp nanoimprint lithography [30–32]. In principle this nanoimprint technique reduces or even overcomes the limitations of other methods and lends itself to large scale low cost roll-to-roll processing [33]. The technique exploits the concept of a single use disposable master. It also relies upon the development of imprint resists with low surface energy that allow easy release of the disposable master. Imprint resists can be formulated to have sufficient etch selectivity to be compatible with deep relief pattern transfer into gallium nitride substrates.

Master structures can be made using a variety of techniques, such as photolithography in photoresist or direct-write electron

Fig. 5. Schematic of pattern transfer with a disposable master film. A roller is shown pressing the patterned film into a UV-curable polymer layer on a harder substrate. Photo-curing of the imprinted polymer allows clean separation of the master.

beam patterning and then transferred to nickel replicas by standard electroforming techniques. The pattern on the nickel can then be transferred to the surface of a polyethylene terephthalate (PET) film using a roll-to-roll UV replication process. This provides a large supply (100's of metres) of "disposable masters" for nanoimprinting.

The UV cross-linking materials used in the replication process comprises a conventional acrylate system containing a small percentage of fluoroacrylate. The formulation of each resist can be designed so that spin coated films have a reduced surface energy enabling clean release of the master without additional processing steps. The disposable masters are flexible; their stiffness is determined by the combination of the PET backing film and the formulation of the lacquer containing the relief.

The first step in the process is to spin coat the substrate (typically gallium nitride) with a thin film of UV sensitive imprint resist, followed by a short low temperature pre-bake to evaporate excess solvent and to promote adhesion of the polymer film to the wafer. The imprint step involves using a roller to press the disposable master into the resist with only light force, as shown schematically in Fig. 5. Unlike conventional imprinting, the line of contact of the flexible master makes contact pressure virtually irrelevant. In many cases a simple hand roller is fit for purpose. Experiments show that the degree of filling and the thickness of the residual layer are controlled by the thickness of the spin coated layer rather than the pressure.

After imprinting the next step is to cure the resist. This involves a short exposure to UV light and an optional thermal cure to complete the cross-linking of the imprint resist. Finally the disposable master is released by peeling it from the imprinted substrate. It is often found that the disposable master is already partially released after the cure, owing to the low surface energy design of the imprint resists, eliminating the need for force at a critical stage. Fig. 6 shows a pattern that has been transferred to a wafer using this process. The pattern consists of an array of 400 diameter nm holes, shown at the right. The left hand panel in this figure shows the master stamp used in this process. It was directly written onto silicon by electron beam lithography.

Given that disposable masters are produced on a thin PET film, in a roll-to-roll process, they are highly cost effective to produce. A single rigid master structure can be used to produce many 100's or 1000's of metres of disposable master film. As implied by the description, the individual disposable master films are cheap enough to be discarded after each use. This provides a distinct advantage over rigid stamps, which are more expensive to produce, as they are made from more expensive materials (metals, silicones) which also need to be much thicker to provide the required rigidity and robustness.

There are, however, several issues that can limit the applicability of flexible master nanoimprint lithography. Firstly, if the pat-
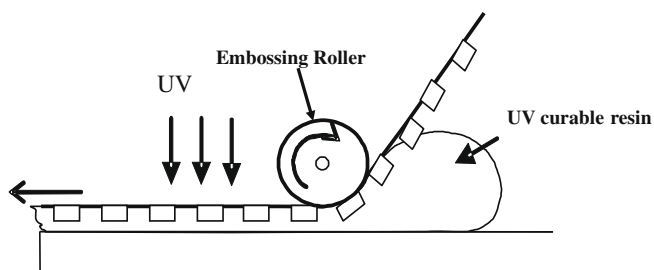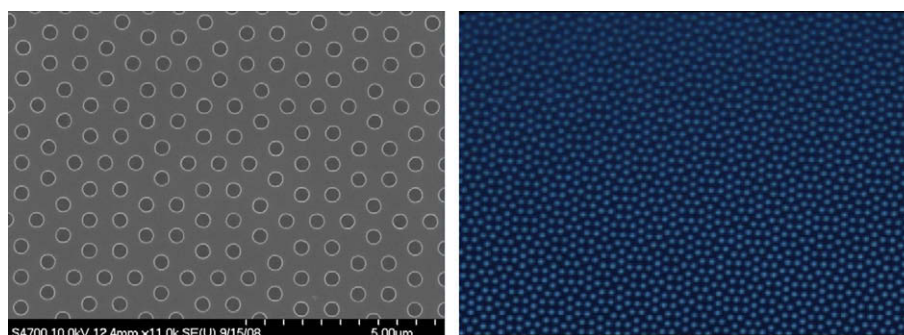
Fig. 6. Left hand image here shows electron beam written master. Right hand image shows patterned imprint resist on wafer after flexible master nanoimprint lithography.

tern is to be successfully transferred to a GaN wafer by means of etching then the "residual layer", or layer of imprint resist in between the pattern and the wafer, needs to be as thin as possible. This implies excellent control over imprint resist spin coating and may impact the choice of materials that can be used in the imprint resist formulation. Secondly, the imprint resist must be formulated to provide the appropriate etch selectivity. The choice of materials available to impart etch resistance may not correspond with the requirements for achieving a thin residual layer. We have successfully explored the use of nano-silica-loaded NIL resist in this work for imparting increased etch resistance to patterned resist. Special resist formulations containing an optimum amount of nano-silica can significantly reduce resist erosion during dry-etching and thus provide a higher etch selectivity relative to GaN. This is distinct from the incorporation of oxetanyl xilsesquioxane (OXSQ) units that contain molecular scale Si–O cage units [33]. In our work we made use of much bigger (∼40 nm diameter) nano-silica particles that resulted in etch rates down to 50 nm/min i.e. about a factor of four lower than the GaN etch rate under the same conditions Thirdly, the flexible master must be manufactured from thin PET to maintain flexibility and the UV replicated coating containing the relief must not limit the flexibility. This implies a thin replicated coating and therefore can restrict the use of deeper surface relief profiles.

5. Dry-etching for pattern transfer

Inductively coupled plasma (ICP) etching is now used in most fabrication of GaN-based LEDs [34]. This process offers high-density plasmas with concentrations of reactive species in the 10^{12} cm^{-3} range, and also gives wide scope for manipulating the physical and chemical contributions to the overall etch process. In standard ICP processing of GaN LED structures grown on insulating sapphire substrates, etching proceeds through the p-type layers and active region to produce mesas. Control of the etch depth and sidewall profile are relatively non-critical in this application. However, in the fabrication of PhC and PhQC LEDs, ICP etching has a second, more demanding role in transferring the photonic microstructure from a mask material into the GaN itself. The examples in this paper all involve pattern transfer into the topmost p-type GaN layers of LED structures grown on c-plane sapphire by metal organic vapour phase epitaxy. In this situation, the GaN is etched on the gallium-polar (0 0 0 1) crystal plane of the wurtzite-phase material. Processing of flip-chip and vertical-current LEDs
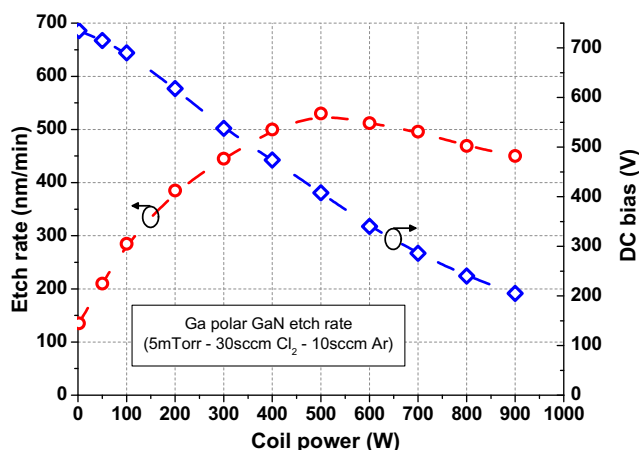
mentioned in the introduction involves dry-etching of GaN on the nitrogen-polar (0 0 0 $\bar{1}$) crystal plane, which may show dissimilar behaviour with respect to both etch rate and roughening [35,36]. The need for separate optimisation of such processes has not been widely recognised in the literature.

The ICP etch tool used in work at Strathclyde University is a Surface Technology Systems LPX system, which is equipped with a laser reflectometer. Chlorine–argon gas mixtures were used, and samples were mounted with grease or wax on silicon carrier wafers. For routine etching of LED mesas, ICP etch processes are operated at etch rates often in the 500–1000 nm/min range. However, considerably slower etch rates are desirable for accurate control of PhC and PhQC hole depths. More specifically, the total process time should be long compared to the stabilisation time of a few seconds expected after the plasma is first struck. Etch rates may be controlled effectively by adjusting the inductively-coupled coil power; with zero coil power the process becomes equivalent to a simple capacitively-coupled reactive ion etch process. Fig. 7 shows the dependence between etch rate on the GaN (0 0 0 1) face and coil power, holding other process parameters constant. These included a platen power of 200 W, a pressure of 5 milliTorr, a chlorine flow of 30 standard cubic centimetres per minute (sccm), and argon flow of 10 sccm, and a chuck set point temperature of 30 °C. The recipe with a coil power of 500 W is representative of one used for mesa etching in standard LED processing. The recipe with a 50 W coil power, corresponding to an etch rate in the plot of 210 nm/min, was chosen for the etching of PhQC structures.

HSQ masks patterned by e-beam lithography, as discussed in Section 2, proved satisfactory for the transfer of PQC patterns into GaN. The etch selectively between HSQ and GaN is similar to the value of 1:6 obtained between conventional SiO$_2$ hard masks and GaN. Etch rates measured from profiling of long step features also transferred accurately to sub-micron HSQ patterns. Fig. 8 shows a representative atomic force microscope (AFM) images of a PhQC test patterns etched to a nominal hole depth of 105 nm. The measured hole depth on this sample, averaged from five locations, was 99 nm. A second sample etched to a target hole depth of 55 nm was also examined by AFM. The measured hole depth, averaged from three locations, was 56 nm.

Fig. 8. Tapping-mode AFM image of 2 × 2 μm area of a PQC test pattern etched into GaN, with a hole diameter of 400 nm, and nominal hole depth of 105 nm. The protrusions on the surface surrounding the holes are believed to originate during epitaxial growth.
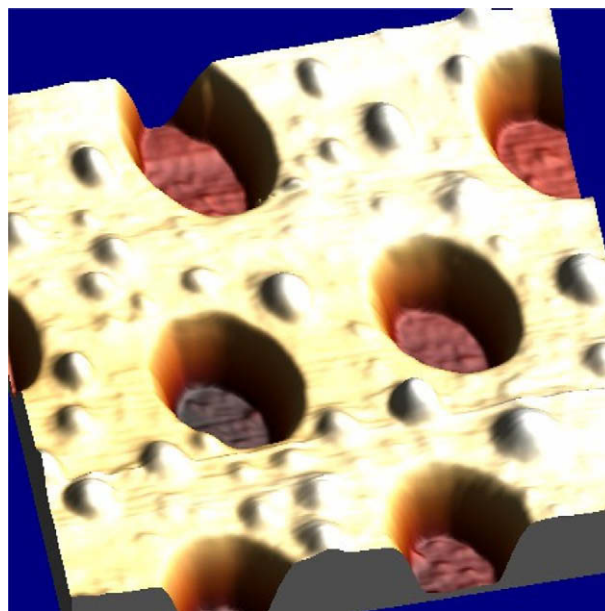

Fig. 7. Etch rate on the GaN (0 0 0 1) crystal face and dc self-bias as a function of ICP coil power. Other process parameters were kept constant, and are detailed in the text.

Fig. 7 also shows the trend in dc self-bias with changing coil power, which is relevant to the sidewall slope obtained in ICP etching. The larger dc biases at lower coil powers enhance the sputter-based physical contribution, and thus favour formation of near-vertical sidewalls, if other factors are favourable. However, the actual sidewall slope obtained is also a function of the HSQ mask profile, cross-sectional SEM views of which are shown in Fig. 2. Experimental determination of the sidewall slope of PhQC holes in GaN of depths of interest for working devices (typically <150 nm) is challenging. However, cross-sectional SEM views of a specially prepared test sample with a hole depth of 800 nm showed that the GaN sidewalls are within 10° of vertical with the preferred etch recipe.

As noted already, the ICP etch tool employed features a laser reflectometer allowing real-time in situ monitoring of the etch process through thin film interference effects. This monitoring technique is now very common in epitaxial growth, but is also widely adopted for endpoint detection in plasma etch systems [37]. The monitoring wavelength in this study was 670 nm, and the beam was focussed onto the sample at normal incidence through a window in the ceiling of the process chamber. The refractive index difference of ~0.6 between GaN and sapphire substrates produces large changes in sample reflectance as the optical thickness of the GaN layer changes. Derivation of GaN etch rates is thus very straightforward, and is analogous to the already widespread use of reflectometry in growth monitoring [38]. Provided the GaN layer thickness is sufficiently large, etch rates under several different etch conditions can be measured in a single process run. This methodology was used to obtain the data plotted in Fig. 7, using a uniform GaN epi-layer of nominal 4 μm thickness. The ternary alloy layers of LED structures, as illustrated in Fig. 1, do not greatly complicate reflectance monitoring per se, since their refractive indices do not differ from that of GaN by more than a very few percent. However, etch rates of aluminium-containing alloys are lower than those of GaN, and thus simple GaN epi-layers are preferred to full LED structures for studies of GaN etch rates.

Reflectance monitoring also allows etch rates of novel mask materials, and the selectivities with respect to GaN etch rates, to be determined in a straightforward fashion. These measurements are particularly important for polymeric nanoimprint resists, where the finite thickness of the residual layer needs to be taken into account for pattern transfer into the underlying GaN. The polymer formulations themselves have high transparency in the visible, and a suitable sample type to study the etch resistance is an unpatterned layer of the polymer on an opaque silicon substrate. Illustrative results are shown in Fig. 9, which is a plot of reflectance versus time during exposure of a 230-nm layer of a cured acrylate-fluoroacrylate resin, as discussed in Section 4, to the etch conditions used for pattern transfer into GaN. Full removal of the polymer is evidenced by the constant reflectance value reached after at etch time of ~25 s. The flat reflectance signal in the first 2 s after the process start corresponds to a 'dead time' caused by plasma stabilisation. The effective etch time of 23 s for the polymer layer thus corresponds to an average etch rate of 600 nm/min, ~3× that of GaN under the same conditions. Even this relatively low etch resistance proved sufficient for transfer of submicron motheye-type patterns [39], produced by the flexible stamp nanoimprint lithography method discussed in Section 4, into GaN layers. However, much lower polymer etch rates down to 50 nm/min have been demonstrated using modified resins employed in the most recent work on PQC-LED fabrication. That work shows that using proprietary blends of acrylate-fluoroacrylate resin the ICP etch rate of the resist can be reduced from 3× that of GaN to less than that of GaN. While resist without nano-silica can be successfully used for the transfer of shallow patterns to GaN, silica-loaded resists can enable the transfer of significantly deeper patterns.

After pattern transfer, LED structures measuring 350 × 350 μm were fabricated using standard photolithography, dry-etching and metallization techniques. An SEM micrograph of our finished PhQC LED device appears in Fig. 10. The n-contact pad, seen to the right, required etching down to the n-type contact layer of the epitaxial

p-contact pad   Patterned emitting surface   n-contact pad
                     (covered in thin spreading metal)   (lower height)
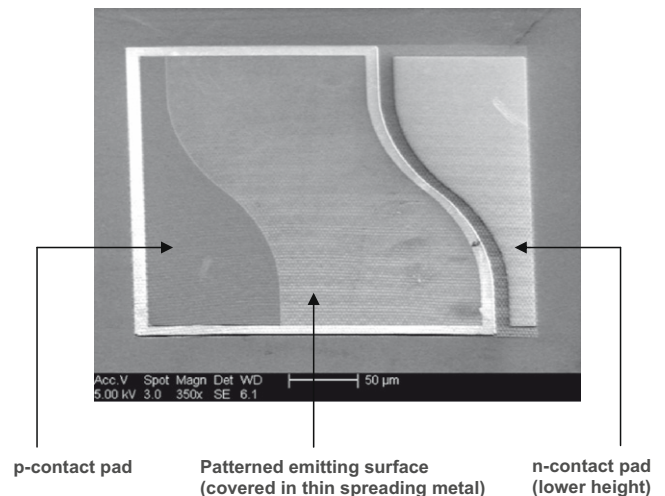
Fig. 10. SEM micrograph of a finished PhQC LED device showing the central area patterned with PhQC structure as well as the *n* and *p* contacts to the right and left, respectively.
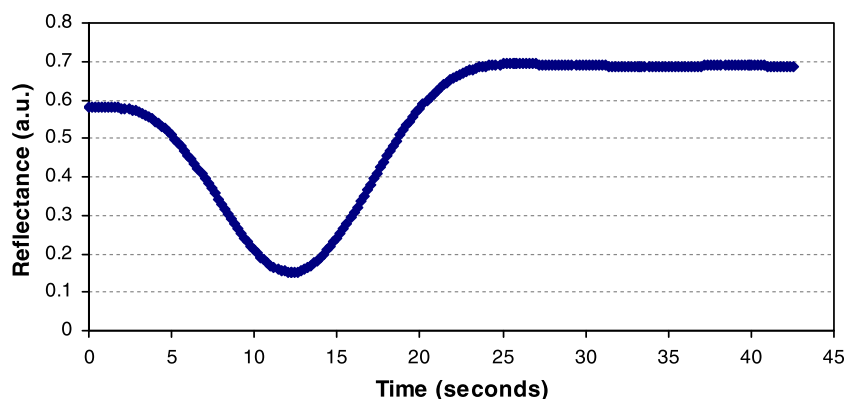

Fig. 9. Plot of reflectance versus time measured during a test of the etch resistance of an acrylate-based nanoimprint resin to the ICP etch recipe used for pattern transfer into GaN.

structure whereas the *p*-contact pad was formed directly on top of the wafer. A thin Ni/Au bilayer spreading metal was deposited on the top face of the LED to distribute current evenly across the entire cross-section of the device. This transparent conductive layer is needed in all large area LEDs because the relatively low electrical conductivity of *p*-type GaN would otherwise lead to current crowding effects resulting in uneven illumination from the emitting face of the LED. In order to further reduce current crowding effects and resulting non-uniform thermal effects in the LED chip we utilised anode and cathode electrode designs developed by Bulashevich and colleagues from simulation of such effects in blue GaN LEDs [40]. The curved contours of this design are clearly seen in Fig. 10. We tested our devices both on wafer and after dicing and bonding onto TO-style headers. Their I–V characteristics are essentially identical to unpatterned reference devices made on the same chips, thus showing that the PhQC patterning process doesn't cause electrical degradation of LEDs. These devices performed very well in our tests, generating strong and uniform emission from the top emitting face. Detailed descriptions of our electrical and optical tests on these devices will be published elsewhere.

6. Summary

We have described nanofabrication technologies for patterning photonic crystal structures on LED wafers. These include direct-write electron beam lithography, hard stamp nanoimprint lithography, soft-stamp nanoimprint lithography for patterning resist and inductively-coupled plasma-based dry-etching for transferring patterns into semiconductor material. Process details have been provided which clearly show that electron beam lithography is desirable for R&D purposes whereas nanoimprint lithography is the only option for large scale device manufacturing. Soft-stamp nanoimprint lithography with disposable masters, in particular, appears to be the lowest cost technique for mass manufacture of PhC LEDs. ICP dry-etching is also demonstrated as ideal for transferring patterns defined in resist to the underlying semiconductor wafer material with high fidelity.

Acknowledgements

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