The University Of Sheffield.

NOVEL DESIGN TECHNIQUES AND CONTROL SCHEMES FOR HIGHER EFFICIENCY SWITCHED-MODE POWER CONVERTERS

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Summary

This thesis details novel control schemes and design techniques with the aim of improving the performance of several switched-mode power converter topologies. These improvements include higher steady-state and transient efficiencies for hard-switching converters and the automatic current limiting provision for LLC resonant converters.

The thesis initially attempts to use linear closed-loop controllers to improve the transient response of synchronous buck converters, enabling them to be designed with a lower open-loop bandwidth so that the system can achieve higher efficiency. Three types of controllers were investigated viz: the PID, the state-feedback and the predictive controller. All three controllers exhibit similar step responses, which are the maximum transient responses achievable by the linear controllers with the given requirements.

The thesis then examines the parallel converter (i.e. a converter with two parallel connected power modules (PMs)) in detail with a view to improve the efficiency and to minimise the current ripple experienced by the output capacitor. Two control schemes and a design technique for the parallel converter are proposed, to simultaneously improve its efficiency and power density. The parallel converter in this research consists of two non-identical rated PMs (termed main PM and auxiliary PM), with the transient response requirement allocated to the auxiliary PM, thereby allowing the main PM to operate at a lower frequency for higher steady-state efficiency.

The first control scheme activates the auxiliary PM only when a pre-determined deviation in load/output voltage is exceeded under a load step. Thus, eliminating the losses contributed by the low efficiency auxiliary PM for small load step changes. The second control scheme shapes the auxiliary PM inductor current to be equal and opposite to the main PM current ripple, which when combined reduce the current ripple as experienced by the output filter capacitor, thereby allowing a lower value (and hence physically smaller) capacitor to be selected for higher power density. In order to improve the converter's steady-state efficiency further, the minimum load condition is

allocated to the auxiliary PM in the new design technique. These allow both the main PM inductance and its switching frequency to be lower for higher efficiency.

In recent years, the LLC has received much attention owing to its favourable operating characteristics including high efficiency and high power density. Usually one chooses to operate at or very close to the load independent point (LIP) since very little control effort is required to regulate the converter's output voltage in response to changes in the load. However under fault conditions where the load tends towards a short circuit, excessive currents can flow and thus control action need to be taken to protect both the converter and the load. The final topic of the thesis hence studies the characteristics of an LLC resonant converter with current-limiting capacitor-diode clamp and develops a new equivalent circuit model to predict the behaviour under overload conditions. A detailed analysis of the converter is presented using the proposed model, from which a design methodology is derived allowing the optimum circuit components to be selected to achieve the required current limiting/protection characteristics.

Publications

Some of the work contained in this thesis has been disseminated at the following international conferences and in learned society journals:

[P1] **C.-W. Tsang**, M.P. Foster and D.A. Stone, 'Parallel buck converter with non-identical power module for improved transient efficiency', Power Control and Intelligent Motion (PCIM) 2013.

[P2] **C.-W. Tsang**, M.P. Foster and D.A. Stone, 'New design approach for higher energy efficiency with parallel converter', IET PEMD conf., 2012, pp 1-6.

[P3] **C.-W. Tsang**, M.P. Foster, D.A. Stone and D. Gladwin, 'Active current ripple cancellation in parallel connected buck converter modules', IET Power Electron., 2013, 6, pp 721-731.

[P4] **C.-W. Tsang**, M.P. Foster, D.A. Stone and D. Gladwin, (In Press) 'Analysis and design of the LLC resonant converter with capacitor-diode clamp current-limiting', IEEE Trans. Power Electron., accepted April 2014.

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Nomenclature

Subscript m, x and i are also used with the list of symbol above to distinguish the parameters for the main PM, auxiliary PM and interleaved converter PMs (e.g. δ_m, δ_x and δ_i are the duty cycles for the main PM, auxiliary PM and interleaved PM respectively).

$\boldsymbol{A}, \boldsymbol{B}, C, \boldsymbol{D}, \boldsymbol{E}, \boldsymbol{K}$	matrices, bold font represents vector
A_c	inductor core area
A_s	resonant tank inductor ratio $(= L_p/L_s)$
A_w	winding cross-sectional area
BW	system bandwidth
B_f	flux density
B_{peak}	peak flux density
B_s	capacitance sharing ratio $(= C_r/C_s)$
$\boldsymbol{B}'$	augmented input vector, bold font represents vector
CCM	continuous conduction mode
CMC	current mode control
C_c, C_s	resonant tank capacitors
C_{gs}, C_{rss}, C_{oss}	parasitic capacitors of MOSFET
C_i	input capacitor
C_o	output capacitor
C_r	equivalent resonant capacitance (with inactive diode-clamp)
DT	dead-time
D_k	predictive controller's control gain
D_{c1}, D_{c2}	diode-clamp diode
D_1, D_2, D_3, D_4	diodes
$\frac{d}{dt}I_m, \frac{d}{dt}I_x, \frac{d}{dt}I_{m+x}$	rate of inductor currents
$\frac{d}{dt}I_{m(+)}$, $\frac{d}{dt}I_{x(+)}$	rate of rise of inductor currents
$\frac{d}{dt}I_{m(-)}, \frac{d}{dt}I_{x(-)}$	rate of fall of inductor currents
$\frac{d}{dt}I_{m(net)}, \frac{d}{dt}I_{x(net)}$	net rate of inductor currents
$\frac{d}{dt}I_{x(net+)}$	net rate of rise of inductor current
$\frac{d}{dt}I_{x(net-)}$	net rate of fall of inductor current

ESR	equivalent series resistance
e	error signal, $e = r - y$
e_{ss}	steady-state error
FHA	fundamental harmonic approximation
$FRDB$	fast response double buck scheme
$FRHE$	fast recovery with high transient efficiency scheme
f_{sm}, f_{sx}, f_{si}	switching frequencies
$f_{s(min)}$	minimum switching frequency
$f_{s(max)}$	maximum switching frequency
f_n	nominalised frequency ($f_n = f_s/f_0$)
f_0	resonant frequency
$HSSE$	high steady-state efficiency design technique
IAE	integral of the absolute magnitude of the error
ISE	integral of the squared of the error
$ITAE$	integral of time multiplied by absolute error
$ITSE$	integral of time multiplied by the squared error
I	identity matrix
I_{co}	current reference
$I_{(dc)}$	dc current
I_i	input current
$I_{m(rms)}$, $I_{x(rms)}$, $I_{i(rms)}$	rms currents
I_{ref}	current reference
I_n	normalised output current $(= I_{o(over)}/I_{o(rate)})$
I_m, I_x	inductor current
I_o	output current
$I_{o(rate)}$	maximum rated output current
$I_{o(over)}$	overloading output current
I_{peak}	peak current
I_r	compensation ramp
I_s	current step
J	cost function
k_{im}	imaginary component used in $M_{g(clmp)}$
k_{re}	real component used in $M_{g(clmp)}$
KVL	Kirchhoff's voltage law
KCL	Kirchhoff's current law
K_c	input voltage compensation gain

K_e	Euler's equation gain
K_g	instrumentation amplifier gain
K_P, K_{Pm}, K_{Px}	proportional gains of PID controller
K_I, K_{Im}, K_{Ix}	integral gains of PID controller
K_D, K_{Dm}, K_{Dx}	derivative gains of PID controller
K_1, K_2, K_i	state feedback controller gains
K_{PWM}	PWM gain
K_{Id}	discrete-time equivalent of integrator gain
K_s	system gain
LIP	load independent point
L, L_m, L_x, L_i	inductors
L_p, L_s	resonant tank inductors
L_{mm}, L_{mx}	magnetising inductors
l	legth of wire
M_g	nomalised gain (with inactive diode-clamp)
$M_{g(max)}$	maximum nomalised gain (with inactive diode-clamp)
$M_{g(min)}$	minimum normalised gain (with inactive diode-clamp)
$M_{g(clmp)}$	nomalised gain (with activated diode-clamp)
m	number of auxiliary PM cycles with respect to main PM cycle
m_n	number of phases
N_k	predictive controller's feedback gain
N_L	inductor number of turns
N_p	transformer primary number of turns
N_s	transformer secondary number of turns
n	transformer turn ratio
n_y	predictive controller's output horizon
n_u	predictive controller's input horizon
PCM	peak current mode
PM	power module
PWM	pulse-width modulation
P_{gm}	gate drive loss
P_{cm}	MOSFET conduction loss
P_{sm}	MOSFET switching loss
P_{cL}	inductor conduction loss
P_{sL}	inductor switching loss
P_{cd}	diode conduction loss
$P(n)$	total loss ratio

$P_c(n)$	conduction loss ratio
$P_s(n)$	switching loss ratio
$P_{gm}(n)$	gate drive loss ratio
$P_{cm}(n)$	MOSFET conduction loss ratio
$P_{sm}(n)$	MOSFET switching loss ratio
$P_{cL}(n)$	inductor conduction loss ratio
$P_{sL}(n)$	inductor switching loss ratio
$P_{cd}(n)$	diode conduction loss ratio
P_{cm}	MOSFET conduction loss
P_r	predictive controller feedforward gain
p	ripple reduction ratio
Q	quality factor $(= \sqrt{L_s/C_r}/R_{eq})$
Q_g	MOSFET gate charge
Q_n	normalised Q-factor $(= Q_{over}/Q_{rate})$
Q_{over}	Q-factor at overloading
Q_r	charge due to current ripple
Q_{rate}	Q-factor at maximum rated load
Q_{rr}	reverse recovery charge
Q_{us}	charge due to load step
R	real component of Z_c
R_C	parasitic capacitor resistance
R_{ds}	MOSFET on-state resistance
R_{eq}	equivalent load resistance
R_g	instrumentation amplifier gain resistor
R_L	parasitic inductor resistance
R_l	load resistance
R_w	winding resistance
r	reference signal
SBC	synchronous buck converter
SCM	sensorless current mode
$SCM - PCM$	sensorless and peak current mode scheme
$SMPC$	switched-mode power converter
SSA	state-space averaging
S_1, S_2	MOSFETs
s	complex frequency $(= j\omega_s)$
T, T_s	switching period
T_D	derivative time constant

T_I	integral time constant
T_f	MOSFET fall time
T_r	MOSFET rise time
T_p	time period
T_{set}	settling time
T_x	auxiliary PM switching period
T_1	transformer
t	time
$t_{m(on)}$, $t_{x(on)}$	on-periods
$t_{m(off)}$, $t_{m(off)}$	off-periods
$t_{m(cf)}$	cut-off period
u	intput signal
VMC	voltage mode control
VR	voltage regulator
V_C	voltage across capacitor C_o
V_c	voltage across capacitor C_c
V_f	diode forward voltage drop
V_{gs}	MOSFET gate-source voltage
V_g	MOSFET gate drive voltage
V_i	input voltage
$V_{i(min)}$	minimum input voltage
$V_{i(max)}$	maximum input voltage
$V_{i(norm)}$	nominal input voltage
V_{L_m}	voltage across inductor L_m
V_n	normalised output voltage $(= V_{o(over)}/V_{o(rate)})$
V_{R_C}, V_{R_L}, $V_{R_{ds}}$	voltage across parasitic components R_c, R_L, R_{ds}.
V_o	output voltage
V_{os}	voltage overshoot
$V_{o(rate)}$	maximum rated output voltages
$V_{o(over)}$	overloading output voltage
V_{ref}	voltage reference
V_{th}	MOSFET threshold voltage
V_{us}	voltage undershoot
v_{co}	control signal
v_{ds}	MOSFET drain-source voltage
v_s	sawtooth signal

X	imaginary component of Z_c
$\boldsymbol{x}$	state vector, bold font represents vector
$\boldsymbol{x}'$	augmented state equation
$\dot{\boldsymbol{x}}$	$(d/dt)\boldsymbol{x}$
$\dot{\boldsymbol{x}}'$	$(d/dt)\boldsymbol{x}'$
$\tilde{\boldsymbol{x}}$	state vector x with disturbance
$\dot{\tilde{\boldsymbol{x}}}$	$(d/dt)\tilde{\boldsymbol{x}}$ with disturbance
y	output signal
$\tilde{y}$	output signal y with distribute
Z_1	resonant tank impedance (with inactive diode-clamp)
Z_2	resonant tank impedance (with activated diode-clamp)
Z_c	equivalent clamping capacitance impedance (with activated diode-clamp)
α	load sharing ratio
$\alpha_c,\ \beta_c,\ k_c$	inductor core loss constants
α_d	damping factor
β	frequency ratio f_{sm}/f_{si}
γ	frequency ratio f_{sx}/f_{si}
δ	diode-clamp non-conduction angle
$\delta_{(+)}$	desired duty cycle for $t_{(on)}$
$\delta_{(-)}$	desired duty cycle for $t_{(off)}$
$\delta_m, \delta_x, \delta_i$	duty cycles
$\tilde{\delta}_m$	duty cycle δ_m with distribute
$\delta_{m(ss)}, \delta_{x(ss)}$	steady-state duty cycles
δ'_m	complemented main PM duty cycle
ζ	damping ratio
θ	angle
λ	weighting function
ρ	wire resistivity
ω_n	system natural frequency
ω_s	angular switching frequency $(= 2\pi f_s)$
Δ	tolerant
ΔV_o	output voltage ripple
ΔI_m	current ripple
$2SFC$	two-switch forward converter

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1. Introduction

1.1. Background

The proliferation of electrical systems in modern society has put an increasing emphasis on power supply (converter) design, owing to the growing requirement to interface a multitude of devices with different specifications to the standard mains utility supply. Some examples of these devices include televisions (TVs) and personal computers (PCs), which, in the year 2012, have worldwide shipments of 238 million and 341 million, respectively [1].

Classically, linear DC power supplies [2]-[4] such as those shown in Fig 1.1 were used for this purpose. In these cases, the AC mains input is first passed through a transformer to provide isolation and to step-down the voltage to the desired level, after which the output is rectified by diodes and smoothed by a capacitor to produce the DC voltage, V_{i}. The final step utilises a linear regulator to maintain the output at the desired output level, V_{o}.

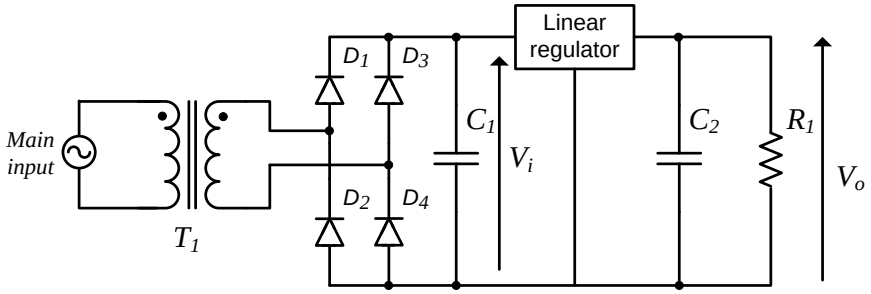


Fig. 1.1 Schematic of a linear DC power supply.

Several issues are generally found with this type of power supply; firstly, the power density is low because the size of the transformer is large due to the low utility supply frequency (50 Hz in the UK). Secondly, the efficiency of the linear regulator is low because it regulates the output power by dissipating any excessive input power as heat. These issues become more problematic

in battery operated portable devices such as mobile phone and tablet computers, where efficient operation leads to longer battery life.

1.2. Switched-mode power converters

The above issues can be overcome by a switched-mode power converter (SMPC) where the AC mains input is first converted into DC by rectifiers and capacitors as shown in Fig. 1.2. The DC voltage, V_i, is then chopped by a DC chopper to produce a high frequency ac signal (e.g. at 300 kHz), after which it is smoothed by a low-pass filter to produce the desired DC output voltage, V_o. Due to the higher switching frequency (compared to the AC main frequency) of the pseudo ac signal, a smaller isolation transformer than is required in mains frequency applications can be used to achieve a higher power density. The efficiency of the SMPC is also higher when compared to the linear regulator, as only the required level of power is transferred to the output by controlling the on-period of the DC chopper. The higher efficiency also allows smaller heat-sinks to be used for higher power density and lower cost. These advantages have led a proliferation of SPMC within the consumer electronics industry. Indeed, the market value of SPMC technologies is expected to reach US$4.3 billion by 2016 [5] and US$9.7 billion by 2020 [6].

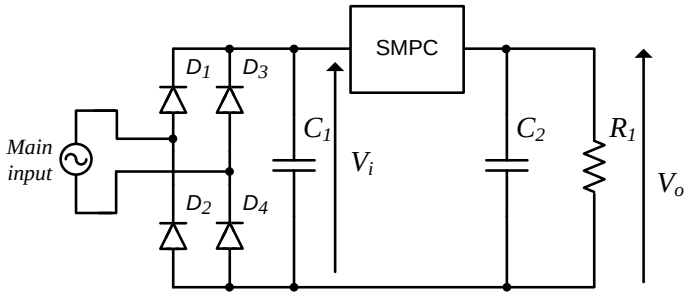
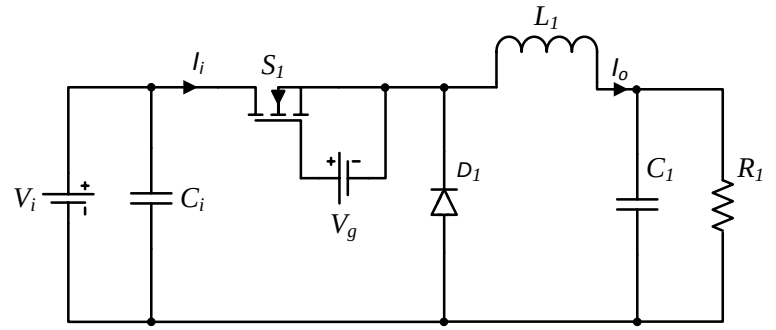


Fig. 1.2 Schematic of main connected power supply with SMPC.

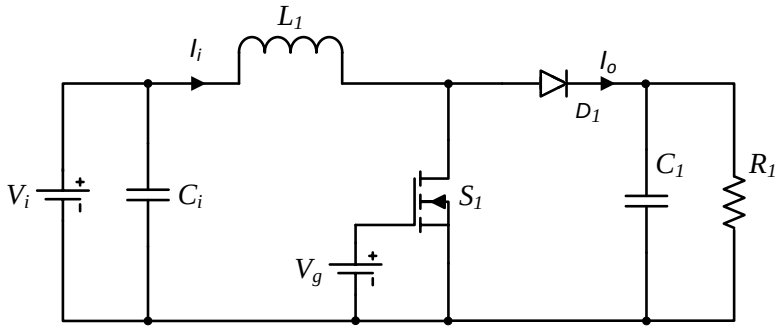
Different types of SMPC have been developed over time. They are classified into three groups for the following discussion: these are the isolated converter, the non-isolated converter and the resonant converter.

1.2.1. Non-isolated converter

To use one of the six non-isolated topologies [7][8] in this section, the conversion ratios must be small (e.g. for a 5 V to 3.3 V step-down converter) with no isolation requirement, as these converters are either pre-regulated with an isolated converter (discussed in section 1.2.2) or are battery powered. The three most basic SMPCs—the buck converter [9], the boost converter [10] and the buck-boost converter [11]—are formed by four main components. These being a power electronic switch (S_1), a diode (D_1), an inductor (L_1) and a capacitor (C_1) as shown in Fig. 1.3. In the buck converter shown in Fig. 1.3 (a), power is transferred to the output from the input during the on-period of the switching device (MOSFET), and is cut-off during the off-period. The output voltage is proportional to the ratio of the on-period to the overall switching period. This ratio is always smaller than unity and so the output voltage is always lower than the input voltage in a practical system (i.e. this is a step-down converter). The inductor stores energy during the on-period which is then released during the off-period to smooth the pulsated (discontinuous) input current, I_i, forming a DC (continuous) output current, I_o, perturbed by a small ripple (n.b. D_1 is commonly replaced by a MOSFET to reduce the converter's loss. The buck converter with this modification is called the synchronous buck converter (SBC), for which more detail will be given in chapter 3). The boost converter in Fig. 1.3 (b) stores energy in the inductor during the on-period which is then released together with power directly from the input during the off-period, producing an output voltage that is always greater than the input voltage (i.e. this is a step-up converter). With the inductor in series with the input source, the input current is continuous while the output current is discontinuous. The operation of the buck-boost converter in Fig. 1.3 (c) is similar to the boost converter, where the inductor stores energy during the on-period and releases it during the off-period. However since the input is not connected to the load during the off-period, the output voltage can both be lower or higher than the input voltage (i.e. this can operate in either step-down or step-up mode) dependent on the amount of energy stored. Both the input and output current of the buck-boost topology are discontinuous and the output voltage is inverted.



(a)



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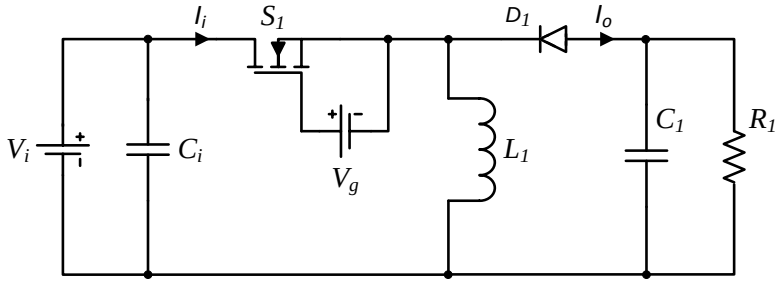
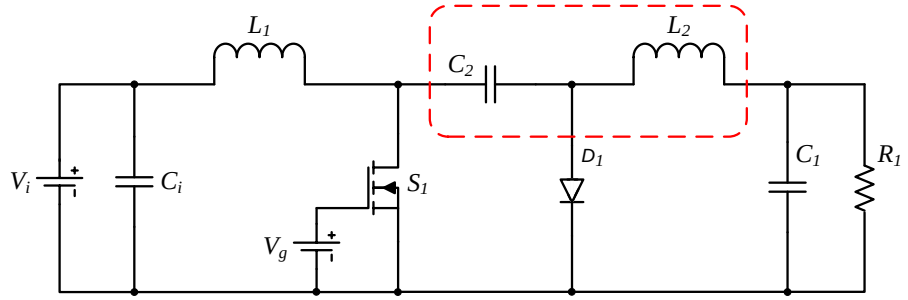


(c)

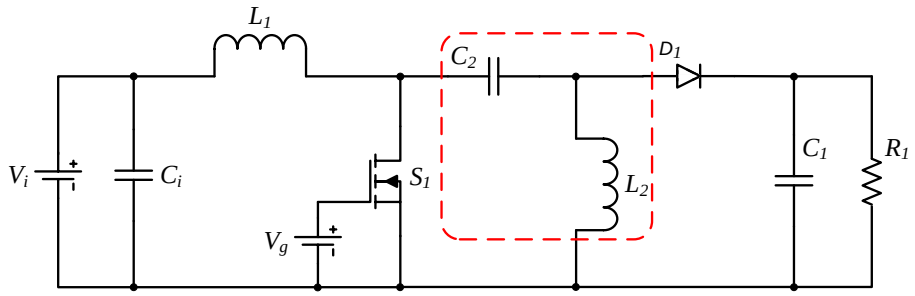
Fig. 1.3 The three most basic SMPC. (a) Buck converter (b) Boost converter (c) Buck-boost converter

By cascading the boost converter with the buck converter and removing any superfluous components, the Cuk converter in Fig 1.4 (a) is obtained [12]. This topology contains two additional components from the above three topologies—these being the inductor, L_2, and

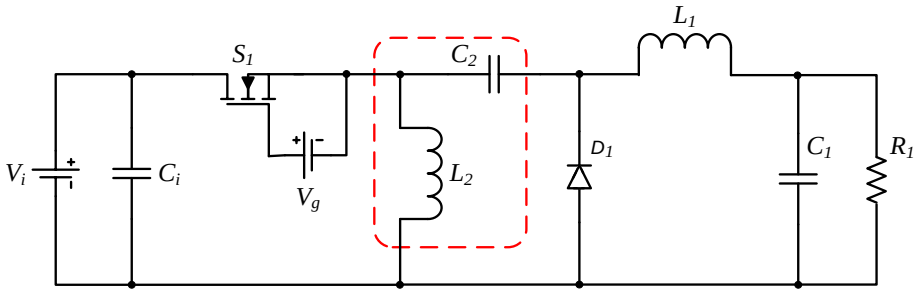
capacitor, C_2—which make this topology more complicated. The capacitor C_2 acts as an energy transfer medium, charging up from the input and L_1 during the off-period and releasing energy to L_2 during the on-period. By controlling the amount of energy stored in C_2, both step-up and step-down conversion can be achieved. The output voltage of this topology is also inverted. The advantage of this topology is that the two inductors are in series with the input and output; both the input and output currents are continuous. As the output polarity in most applications is non-inverted, two further topologies with the same components as in the Cuk converter were developed. These are the SEPIC [13] and ZETA [14] converters shown in Fig. 1.4 (b) and (c) respectively. The operation of these converters is similar to the Cuk converter with the capacitor acting as the transfer medium. The output voltage can both be higher or lower than the input by virtue of controlling the charge to the capacitor. The configurations of the SEPIC and ZETA converters are identical to the boost and buck converters respectively, without the two additional components enclosed by a dashed box in the figures, hence they have the same input and output current characteristics respectively.



(a)



(b)



(c)

Fig. 1.4 Inverting and non-inverting step up/down converters. (a) Cuk converter (a) SEPIC converter (b) Zeta converter.

1.2.2. Isolated power converter

In applications where isolation is required (e.g. to prevent electrical shock) and the output voltage is always significantly lower than the input voltage, a transformer can be added to the buck converter topology to form the four isolated step-down converters [7][8] shown in Fig. 1.5: the forward, push-pull, half-bridge and full-bridge converters (n.b. step-up conversion can be achieved with a greater than unity transformer turns ratio). The forward converter shown in Fig. 1.5 (a) operates in a similar manner to the buck converter where power is only transferred during the on-period. The additional demagnetising winding, L_{dm} and the diode D_{dm} in parallel with the transformer primary, are needed to reset the transformer core by removing stored flux in each cycle. The additional diode D_2 ensures the transformer secondary is cut-off from the output during the off-period of the switching device. This topology is only suitable for applications of up to 100 W [8] due to the high voltage stress seen by the switch.

In the push-pull converters, Fig. 1.5 (b), a demagnetising winding is not required as a flux balance in the transformer primary is achieved with an 'ac' excitation signal through a centre-tapped transformer. Since this converter only uses half of the primary winding at any one time, the utilisation of the transformer is low which makes it only suitable for application with power rating of up to 500 W [8]. In the half-bridge converter in Fig. 1.5 (c), an 'ac' signal in the transformer primary is formed by taking the mid-point input voltage as a reference. With the elimination of the need for two primary windings, transformer utilisation has increased, however as only half of the input voltage is available, the required input current is twice as large for the same output power requirement, which makes it also only suitable for application of up to 500 W [8]. In the full-bridge converter shown in Fig. 1.5 (d), the two capacitors in half-bridge are replaced by two switches. By switching the diagonal legs of the bridge in pairs, the full input voltage, V_{i}, is made available across the transformer primary, making it suitable for use in applications of up to and above 5 kW [8].

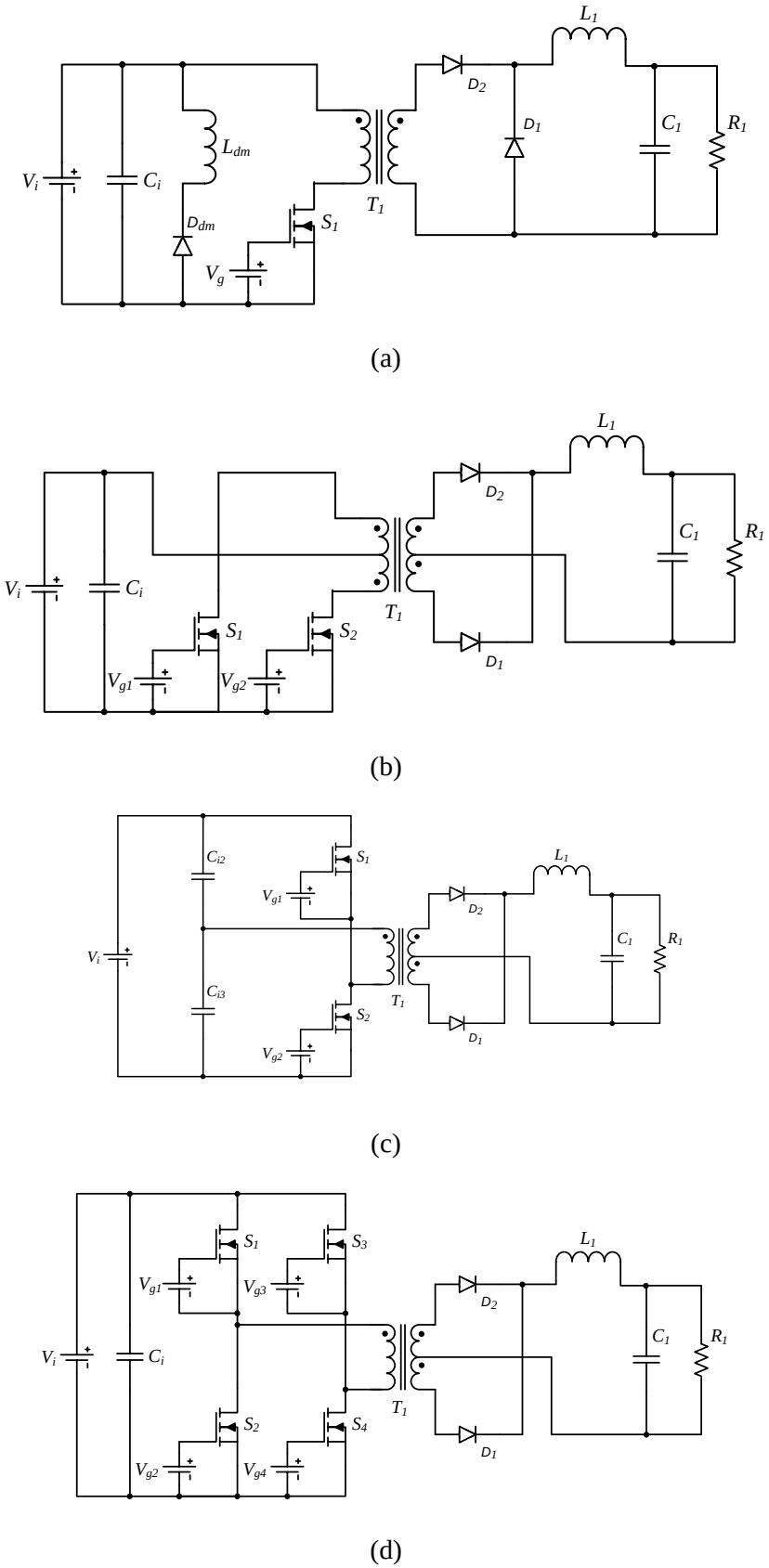


Fig. 1.5 Isolated step down converter. (a) Forward converter (b) Push-pull converter (c) Half-bridge converter (d) Full-bridge converter

In applications where isolation and both step-up and step-down conversions are needed, the flyback converter, shown in Fig. 1.6, can be used. This converter operates as the buck-boost converter; however, its output is non-inverted because the primary and secondary windings are wound in opposite directions. This converter is only suitable for application of up to 100 W [8] as the magnetic core has to store all the load energy during the on-period of the switching device.

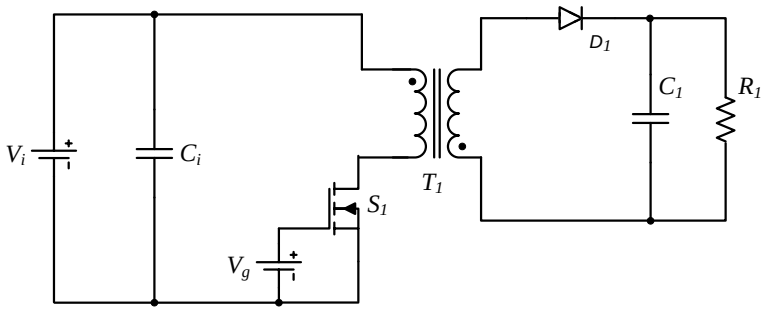
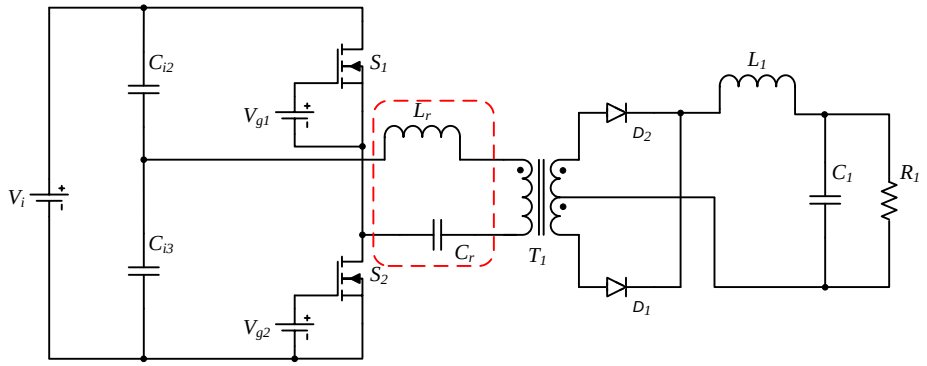


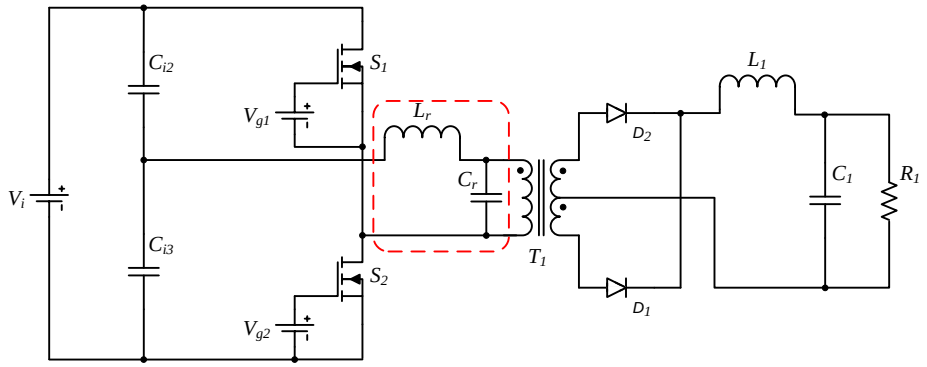
Fig. 1.6 Flyback isolated step up/down converter.

1.2.3. Load resonant converters

Converters mentioned up to this point are classified as hard-switching converters as the current and voltage across the switches (MOSFETs) are non-zero each time a switching event occurs, thereby inducing switching losses, stress and EMI. The load resonant converter overcomes this by ensuring the switching event occurs at either zero current (ZCS) or the zero voltage (ZVS). The resonant converter is formed by adding a resonant tank (with the resonant inductor L_r and capacitor C_r enclosed in Fig. 1.7) to either the half-bridge or full-bridge converters in Fig. 1.5 (c) and (d). The two most basic resonant converters, the series and parallel resonant converters [15], are formed by placing the resonant tank in series or in parallel with the load as shown in Fig. 1.7 (a) and (b) respectively. The regulation of this type of converter is achieved by changing the resonant tank impedance with the switching frequency.



(a)



(b)

Fig. 1.7 Half-bridge resonant converter. (a) Series resonant converter (b) Parallel resonant converter

The characteristics and limitations of all these basic topologies are summarised in Table 1.1.

Topology	Power rating (W)	Voltage conversion	Output voltage polarity	Input current	Output current
Buck	> 1M	Step-down	+	Continuous	Discontinuous
Boost	> 1000	Step-up		Discontinuous	Continuous
Buck-boost	> 100	Step-down/ Step-up	-		Discontinuous
Cuk				Continuous	Continuous
SEPIC			+		Discontinuous
ZETA				Discontinuous	Continuous
Forward	< 100	Step-down			
Push-pull	< 500				
Half-bridge	< 500				
Full-bridge	> 5000				
Flyback	< 100	Step-down/ Step-up			
Series-resonant		Step-down			
Parallel-resonant		Step-down/ Step-up			

Table 1.1 Summary of the topologies characteristics.

The limitations as summarised in Table 1.1 can, however, be overcome with a small modification to the topologies. For example, a higher power rating version of the forward converter (for up to 1 kW), called the 2-switches forward converter [16], is formed by replacing the demagnetising circuit by two diodes as shown in Fig. 1.8.

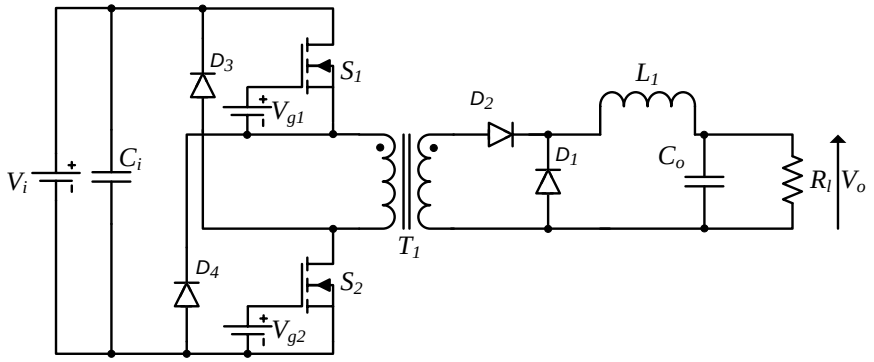


Fig. 1.8 Two-switch forward converter.

1.2.4. Design considerations and challenges

The design of a converter starts by selecting a suitable topology based on the application's specifications, which can be achieved with the help of Table 1.1. Other factors affecting the topology selection include engineer expertise, available literature, design guidelines, compatibility to the existing product portfolio, converter complexity and reliability, to name but a few.

Having selected the topology, the engineer can then focus on the design and selection of the converter's components to meet the steady-state and the transient response requirements of the application. Attention must also be paid tosize, weight, cost and efficiency. For certain applications, the implications of these requirements are contradictory and, therefore, a suitable compromise must be found. For example, a computer voltage regulator (VR) must provide excellent transient response, whilst achieving high efficiency. The fast transient response in buck converters can be achieved by selecting its low-pass filter with a higher bandwidth (corner frequency), this however requires the converter to operate at a higher switching frequency, leading to a reduction in efficiency due to the increase in switching losses in the semiconductor switching device and magnetic components. Even through some of the losses in the semiconductors can be mitigated to a certain extent by employing resonance (as in the resonant converters or the resonant switch converter [17]), these converters require a different set of design and control techniques. Solutions utilising the same set of design and control techniques as the original converter are a more attractive alternative. Some of these solutions include connecting multiple converters in series [18], in parallel [19], or both in series and parallel [20].

With energy efficiency becoming more important in recent years due to rising energy prices and tightening regulations from environmental protection agencies, this thesis primary focuses on identifying control schemes and design techniques to improve the efficiency of the converter. These control schemes and design techniques utilise the same set of design and control techniques as the original converter, similar to the approach in [18]-[20]. Step-down converters (i.e. buck and forward converters) are selected for the investigation as the majority of applications have a step-

down conversion ratio. These new control schemes and design techniques also work with step-up converters. Resonant converters, like the LLC resonant converter, are becoming increasingly popular, due to their low switching losses. One of the issues that prevents this converter from being widely adapted is the low impedance around the operating frequency, allowing excessive current to flow under overload or short circuit conditions. This thesis also develops an equivalent circuit model to predict the overloading issue experienced in the LLC resonant converter which allows the desired clamping capacitor to be selected.

1.3. Thesis outline

The work in this thesis is divided into eight chapters:

Chapter 1 introduces the characteristics and applications of the most commonly used converters. The research focus, thesis outline and contribution are also presented.

Chapter 2 reviews the different modelling techniques and the design and control techniques that have been developed to improve the efficiency of step-down converters. New design and control techniques that could lead to higher converter efficiency and power density are identified. Also included in the review is the overloading issue of LLC resonant converters.

Chapter 3 explores the use of closed-loop controllers to improve the transient performance of synchronous buck converters (SBCs). The full derivation of the converter's equivalent circuit models (in both the state-space and the transfer function forms) and the complete design procedures for the three types of controllers (the PID, the state feedback and the predictive controllers) are presented. The step responses of the converter with the three different types of controllers are compared to identify the best controllers.

Chapter 4 investigates the characteristics of the two control schemes developed to improve the transient performance of the parallel converter, the fast response double buck (FRDB) scheme and sensorless and peak current mode control (SCM-PCM) scheme. By combining the advantages of the two schemes, a new control scheme—the fast recovery with high transient efficiency (FRHE)

scheme—is proposed to improve the converter efficiency during transient operation without unduly increasing the transient response time.

Chapter 5 studies the effects of the different system requirements on the parallel converter's efficiency to assist the development of a new design technique, the high steady-state efficiency (HSSE) technique. In HSSE, the design specifications and requirements that prevent the main power module (PM) from having high steady-state efficiency are conveniently allocated to an auxiliary PM, to allow the main PM be optimised for conduction loss for high steady-state efficiency.

Chapter 6 demonstrates a new active current ripple cancellation (ACRC) scheme, which shapes the auxiliary PM current to reduce the main PM current ripple and hence reduce the current ripple seen by the output capacitor, allowing a lower value output capacitor to be selected. The selection of the auxiliary PM components and duty cycle under different operating conditions are also given.

Chapter 7 presents a design methodology for LLC resonant converters with a capacitor-diode clamp. A new fundamental harmonic approximation (FHA) based equivalent circuit model is obtained through the application of describing function techniques by examining the fundamental behaviour of the capacitor-diode clamp. The current limiting performance of the converter under overload condition is studied and design guidelines are given.

Chapter 8 concludes the thesis and details any further work.

1.4. Contribution

This thesis proposes novel control and design techniques to improve both the steady-state and transient efficiencies of the parallel converter and addresses the overload issue of the LLC resonant converter. In particular, the work presented herein has been disseminated in internationally recognised journals and conferences. The main contribution are summarised below:

- A novel fast recovery with high transient efficiency (FRHE) scheme [P1] is proposed to improve the transient efficiency of the converter with two parallel connected SBCs. By activating the auxiliary PM only when the threshold voltage or settling time are to be exceeded, the transient efficiency of the prototype converter is improved by as much as 4.7% under continuous load step.

- A novel high steady-state efficiency (HSSE) design technique [P2] is proposed to improve the steady-state efficiency of the converter with two parallel connected 2SFCs. By allocating both the transient response requirement and the minimum load condition to the auxiliary PM, the main PM can then be optimised for steady-state operation. The steady-state efficiency of the prototype converter is improved by up to 12%.

- A novel active current ripple cancellation (ACRC) scheme [P3] is proposed to reduce the current ripple as seen by the output capacitor. Through shaping of the current waveform of the auxiliary PM, the current ripple of the prototype converter is reduced by 67% and the efficiency is also improved under most load conditions.

- A new equivalent circuit model for a LLC resonant converter with the capacitor-diode clamp [P4] is developed to predict the overload current. By extracting the fundamental behaviour of the capacitor-diode clamp using a describing function technique, the converter current limiting characteristic under different operating frequency and overload conditions are predicted, allowing the optimum clamping capacitors to be selected.

2. Control schemes and switched-mode power converter topologies for high efficiency

2.1. Introduction

The previous chapter introduced different switched-mode power converter topologies usually employed within industry, and highlighted the focus of the thesis. This chapter provides a thorough review of different types of modelling techniques, control schemes and design and control techniques developed and employed by power supply designer for SMPCs. It also proposes new control schemes and design techniques that allow higher efficiency, higher power density and overload protection to be achieved. From the review of existing literatures, five areas are identified as suitable for further research:

1) Effect on the converter's transient responses with different feedback controllers
2) Control schemes that provide lower losses under transient conditions.
3) Design techniques that improve the efficiency under steady-state conditions.
4) Reduction in current ripple for higher power density
5) Overload characteristics of an LLC converter with capacitor-diode clamp.

This chapter commences by examining the mathematical modelling techniques employed to predict both the steady-state and the transient behaviour of converters before applying some of the techniques to the analysis and design of converters and their feedback controllers.

2.2. Mathematical modelling

In order to study the converter's behaviour, system (converter) mathematical models are essential. As the buck converter is a nonlinear system due to the switching action in each period, equivalent LTI models must be obtained in order to design suitable feedback controllers using linear control systems theory. Dependent on whether the system is to be controlled in either voltage mode (VMC)

or current mode (CMC), differing modelling techniques must be utilised [2]. VMC is a single loop control system where the output voltage is regulated directly through a linear controller. CMC is a dual loop control system where the output voltage is regulated indirectly through the inductor current. The outer voltage loop sets the current reference of the inner-loop through a linear controller to regulate the inductor current. CMC is widely employed as it gives better performance, but due to its complexity and issues with noise, VMC is still popular, and in the case where high performance is desired, state feedback control can be utilised in VMC to give similar overall performance to the CMC approach.

The two most popular VMC modelling techniques are the state-space averaging (SSA) and the PWM switched model. The SSA was developed by Cuk and Middlebrook [21] in the mid 1970's, by first writing the piecewise linear circuits equations into sets of linear state equations, and then taking the time weighted average of these equations, a linear system model can be obtained. Vorperian [22] realised that the only nonlinear elements in the system are the switching elements (diodes, MOSFETs, etc.) and this led to the development of the PWM switched model, where linear system models are obtained by only linearising the switches. Although both methods were proved to model converters equally well, after the subsequent identification of the 'duty-ratio constraint' for SSA [23][24], the PWM switch model still has the following advantages over the SSA:

- The complexity of the linearisation is reduced as only the switches and not the whole circuit is included in the linearisation
- The invariant structure of the switches implies that once it has been linearised, it can be substitute into any converter topology directly.

Other work connected to the PWM switch model includes:

(1) An extension to model converters with switches that are not connected back to back [25]

(2) The introduction of two alternative forms of PWM transformers allowing analysis by inspection [26].

Other modelling techniques include: (1) the MISSCO technique where a minimum separable switching configuration of the circuit is first identified, the low frequency behaviour of the MISSCO is than obtained by taking the average of its impulse response [27]. (2) The invariant structure models, where different converters can be organised in a table as in the canonical circuit model proposed by Cuk [21], where parameters of the converters are modified to fit into the four fixed parts (i.e. e(s), j(s), μ and He(s)), and the average power-stage model [28] where the same buck converter like structure (i.e. voltage source, three resistors, a inductor and a capacitor without the switch and diode) can be derived for any converter topology. (3) The graphical approach where the physical systems are represented graphically as in signal flow graph [29] and its modification, the bond graph [30], these modelling techniques make modelling of complex systems like the cascaded or multi-phase converters easier, and (4) The sampled-data model where the evolution of system states is calculated from the initial condition instead of averaging, as in SSA, to preserve the exact system dynamics [31]-[34]. (5) The Energy Factor (EF) method, proposed by Luo and Ye [35] where a model is obtained by identifying the input energy (PE), energy in the reactive elements (SE), capacitor /inductor stored energy ratio (CIR) and the energy losses (EL), without the use of elementary circuit analysis. (6) System identification which is used in the cases where the internal structure of the circuit is inaccessible or for complex system [36][37].

2.3. Closed-loop controllers

In order to obtain the desired output voltage, the duty cycle of a converter can be calculated and set directly [2]-[4]. This is open-loop control which is sensitive to system variation and changes in operating conditions. To overcome this, the duty cycle can instead be set by a controller which produces an error signal (difference between a reference and the output voltages) where the error signal itself is driven to zero using some form of compensator.

One of the most widely used controllers is the PID controller [38][39], due to its ease of use and its ability to give good performance in the vast majority of applications. This controller contains three terms: 'P' - the proportional gain, 'I' – the integral gain and the derivative gain 'D'. Different combinations of the three terms can be selected according to the system need, the common combinations are the P, I, PI, PD and PID. The PID is the most complex of all, but produces the best performance for systems characterised by dominant second order behaviour where, based on the system model, one can often independently control damping factor, overshoot and settling time within certain bounds. If the system mathematical equation is not available, PID parameter values can often be obtained empirically based on the Ziegler-Nichols tuning methodology. This method can be based on the system step response or the system frequency response where in both cases, the specified parameters (i.e. a_u & L_u and K_u & T_u respectively) are first found and then substituted into their corresponded look up table to obtain appropriate PID parameter values [40]. Other empirical tuning methods have been developed by engineers through experience [3][41]. On-line auto-tuning, where the PID control loop is tuned automatically given the desired characteristics [42][43] are also popular. When the mathematical equations are available, controllers can be designed by utilising a root locus plot as in pole-zero cancellation or using a pole-placement technique as in the robust PID controller [38].

The second most common control technique is state feedback control, similar to the robust PID controller, it is also a pole-placement technique, but unlike PID, the feedback signal is applied through pure gain terms and an additional integrator is usually required to ensure adequate steady-state behaviour. Since it may not be possible to obtain measurements of all states in practical systems, state-observer techniques can be employed to estimate the unknown / inaccessible states. When the practical system model is unavailable, the state-feedback controller can be obtained through the use of a genetic algorithm, where the controller parameters are obtained through the natural selection process [41], and when the model is available, state feedback with an integrator [38] or the LQR control where gains are selected through minimise the user define cost function

[44] may be employed. In predictive controllers, in addition to the system error signal(s), past knowledge and the future response are also stored and predicted to form the control input [45].

Other control techniques, described in the literature, which do not require the linear model include sliding-mode control [46], artificial neural networks [47], and fuzzy logic controllers. These have also been successfully employed to provide a robust system [48].

All of the controllers aim to improve both the steady-state and the transient performance of the converter and this improvement permits converters to be designed with a lower open-loop performance allowing it to operate at lower frequency and, hence, higher efficiency. In this regard Chapter 3 investigates the transient response of the synchronous buck converter with the different types of controller (i.e. the PID controller, the state feedback controller and predictive control) all designed to improve transient performance whilst achieving high-efficiency.

2.4. Transient efficiency of a parallel converter

Numerous control techniques have been developed with the aim of improving part-load efficiency of converters. Some of these techniques include reducing the converter switching frequency and/or skipping some of the switching cycles during light load conditions [49]-[54]. The improvements from these techniques are, however limited, since the converter still has to satisfy all the system requirements across the different load conditions. One way to overcome this limitation is by adding a dedicated circuit to the converter to decouple the conflicting requirements such as the transient performance requirement from the efficiency requirement [55]-[61]. The parallel converter [58]-[61] has received much attention since the loading requirements can partitioned across a number of power modules (PMs) all of which can be designed and controlled using similar techniques, expediting the development process of the overall system.

With identical power modules connected in parallel [58], the converter's bandwidth (i.e. corner frequency) is increased proportional to the number of PMs in parallel without any increase in switching frequency. Unfortunately, paralleling becomes impractical with the ever increasing

transient performance requirement, since either the switching frequency or the numbers of PM utilised have to be high. An alternative scheme is to connect non-identical PMs together [59]. In this scheme, one PM, a 'main PM', can be designed to operate at a low switching frequency for high efficiency under steady-state conditions, while the second PM, an 'auxiliary PM', can be designed to run at a high switching frequency for high BW under transient conditions. Since the auxiliary PM is only enabled during the transient conditions, high bandwidth and efficiency can both be obtained.

Different ways of utilising the auxiliary PM under transient conditions have been suggested. In the fast response double buck converter (FRDB) [60], the auxiliary PM only operates when the output voltage drops below a threshold level. Even though the voltage undershoot requirement is met, the extra bandwidth available from the auxiliary PM is not fully exploited. In the sensorless and peak current mode controlled converter (SCM-PCM) [61], the auxiliary PM operates when a transient condition is detected. It remains in operation until the main PM recovers from the transient condition. The wide bandwidth of the auxiliary PM is fully exploited in this scheme. However, since the efficiency of the auxiliary PM is lower than the main PM, due to the auxiliary power modules' higher switching frequency, the longer operating duration leads to lower overall efficiency under transient conditions in comparison to the FRDB scheme.

Chapter 4 combines the high efficiency characteristic associated with the FRDB and fast transient response characteristic associated with the SCM-PCM to achieve an equitable compromise between the transient response and efficiency.

2.5. Steady-state efficiency of a parallel converter

To improve the converter steady-state efficiency, multiple converters can be connected in series [18], in parallel [19] or a combination of the two [20] to process the power more efficiently. The majority of research in this area has again been focussed on the parallel converter arrangement. In the interleaved converter [59], identical PMs are designed to minimise both switching and conduction losses across the whole load range. High efficiency at heavy load is achieved through a reduction in conduction loss by sharing current between the identical PMs which reduces the $I_o{}^2 R_l$ loss to $m_n(I/m_n)^2 R_l$ (where I_o is the load current, R_l is the load resistance and m_n is the number of PM in parallel). High efficiency at light load is achieved by disabling some of the PMs. With two or more converters connected in parallel, there are a number of possible variations on the design of the converter. In [59], multiple converters, optimised for different load conditions, are operated in parallel to achieve high efficiency across a wide range of load. Alternatively, without increasing the need to parallel as many PMs together as in [19][20][59], a single PM can be designed to run at low frequency for high efficiency, without being constrained by the transient response requirement which is fulfilled by the second PM [62].

Chapter 5 extends the design approach in [62], where, apart from the transient response requirement, the minimum load condition is also allocated to the auxiliary PM, hence allowing the main PM to be designed with a larger inductor current ripple to reduce the conduction loss for higher efficiency. The unfulfilled requirements are met by the auxiliary PM in this case.

2.6. Active current ripple cancellation schemes

An important issue with a larger inductor current ripple as proposed in section 2.5 is the need for a greater output capacitance in order to meet the voltage ripple design requirement, thereby potentially increasing both the cost and size of the overall converter.

Instead of increasing the capacitance, ripple cancellation techniques [63] may be utilised. Over time, numerous techniques have been developed for cancelling the input current ripple [64][65] or

the output current ripple [66][67]. In passive ripple cancellation techniques [64], the current ripple in the filter inductor is reflected to a secondary inductor which is coupled in anti-parallel to the filter inductor. The combination of these two current waveforms produce an output current that is free of current ripple. The setback of this scheme is the size of the required filter and also, since the coupled inductor is fixed at the design stage, the technique is sensitivity to parameter drift.

In active ripple cancellation techniques [65]-[67], current is first sensed using a current transformer or Rogowski coil, it is then amplified to the correct amplitude by a linear amplifier for injection back into the converter. The system complexity is higher in this scheme but they have, however, been shown to have higher ripple attenuation at the low frequency range, and with closed-loop control these methods are robust against parameter drift. The combination of the two, the hybrid filter, which has advantages from both type of filters have also been demonstrated in [68].

An alternate approach to the above active filtering techniques, which requires no current ripple sensing, are demonstrated in [69]-[72]. In these approaches, a switched-mode power converter is designed to operate complementarily to the main converter, producing a current waveform that is exactly the opposite to the main converter current ripple to achieve ripple cancellation [69]-[72]. In [69]-[71], a dedicated converter is added for ripple cancellation, while in [72], the interleaved converter is modified to achieve ripple cancellation without the need for any extra components.

Chapter 6 explores a way of achieving ripple cancellation in the parallel converter with non-identical power modules without any extra components beyond the PMs, by reusing the auxiliary power module of the converter to inject a complimentary current into the output capacitor in addition to improving overall system transient response as described earlier.

2.7. LLC resonant converter with capacitor-diode clamp

As electronic systems are miniaturised, power supply designers are placed under increasing pressure to reduce the size of their designs, imposing strict requirements on the chosen power supply topology, components, efficiency and cooling requirements. Size reduction in hard-switching converters (e.g. buck converters) can be achieved by increasing the switching frequency, which reduces the size of passive components. The drawback of this approach is the increase in switching losses, ultimately compromising converter efficiency.

Resonant converters such as series resonant, parallel resonant and multi-resonant converters [73][74] overcome this drawback by soft-switching, where the switching devices are switched under zero voltage (ZVS) or zero current (ZCS) conditions. One variation of the multi-resonant converter, the LLC resonant converter [75]-[80], has become popular due to its narrow range of operating frequency for wide input voltage and load ranges when operated around the converter's (series) resonant frequency, also referred as the load independent point (LIP). The narrow frequency range is the result of the resonant tank components, L_s and C_r becoming a virtual short-circuit (zero impedance) at the resonant frequency. The operating frequency is adjusted mainly to compensate for the change in the input voltage. It is not overly necessary to adjust the frequency to compensate for changes in the load. Unfortunately, due to the low impedance around the LIP, excessive current can flow to the load during transient and overload conditions, and so a current protection mechanism must be included.

For LLC resonant converters, current-limiting can be achieved by i) reducing the MOSFET conduction times, ii) increasing the switching frequency [81][82], iii) operating at a sub-harmonic of the switching frequency [83], or iv) by changing the resonant frequency characteristics of the converter by switching in (or out) the resonant tank components [81][82][84]-[87]. Although methods i) to iii) provide adequate protection, a current sensor is needed to detect the overload condition and some action by the controller is required to adjust the MOSFET timings. Method iv), in contrast, does not necessarily require any direct action to be taken by the controller assuming

an appropriate circuit can be developed. By way of example, in [81][82] and [86] the resonant capacitor of a LLC resonant converter was divided into two capacitors with anti-parallel diodes and connected to the converter's input voltage rail, thereby clamping the voltage across the two capacitors, hence reducing the output current in an overload condition. The advantage of this scheme is that the current limiting occurs as soon as the over-current condition appears and is performed autonomously without the need for any feedback mechanism. Although a practical circuit was presented, very little information regarding the behaviour of a converter was included. A variation to the capacitor-diode clamp was presented in [87], where, instead of splitting the capacitor and fixing the clamping voltage to the input rail, the capacitor voltage is clamped to the output voltage through a transformer allowing the clamping voltage to be more readily specified and hence allowing the desired current-limiting performance to be obtained. Although a detailed analysis was presented, this scheme requires a controller for the current-limiting, similar to that in methods i) to iii).

In chapter 7, the resonant capacitor of a LLC converter is split into clamped and non-clamped portions to allow the desired current limiting performance to be obtained. An equivalent circuit model, which is based on fundamental harmonic analysis similar to that presented in [88], is derived for the converter to predict the current characteristic under overloading.

2.8. Summary

This chapter has carried out an up-to-date review on the different control schemes and design techniques developed by other researchers and also identified how they may be improved. The review started by identifying the different ways in which buck converters can be designed and controlled. The converter's linear model can be found using different techniques, but the most commonly used are the state-space averaging technique and PWM switched model. Numerous linear closed-loop controllers are also available to shape the converter's steady-state and transient responses. The two most commonly used controllers are the PID controller and state feedback controller, while predictive control provides the most potential for improved transient response.

For higher efficiency, a dedicated circuit can be added to the original converter to share the system requirements. The most popular is by connecting another power converter in parallel, which allows similar control and design techniques to be used. To improve the transient efficiency of the parallel converter configuration, two schemes, the FRDB and SCM-PCM schemes, have been developed. It was found that one scheme focus on the efficiency while the other on the transient response, a new approach which combined the advantage of the two schemes can be obtained. For higher steady-state efficiency, converters that are optimised for different load conditions can be put in parallel and be enabled according to the load conditions. Alternatively, the transient response requirement can be allocated to the auxiliary PM to allow the main PM to be designed for higher efficiency. A new design technique which looks at the allocation of the different system requirements to the different power modules can be developed to enhance the steady-state efficiency. In order to reduce the current ripple, hence the size of the capacitor, current ripple cancellation scheme can be used. Numerous types of passive and active current ripple cancellation techniques have been developed to reduce the input and/or output current ripples. None of which are currently based on the parallel converter with non-identical power modules, a new active current ripple cancellation is needed to be developed for the parallel converter.

The LLC resonant converter has the advantage of high power density, higher efficiency and low EMI in comparison to the hard-switching converter. It has however got load related issues where large currents can flow under overload conditions. A capacitor-diode clamp was shown to be able to limit this current automatically, but no mathematical modelling or design guidelines have been developed so far. A new mathematical model and design guideline are therefore provided here.

3. Closed-loop controllers for buck converters

3.1. Introduction

The previous chapter reviewed the different types of controller available for buck converters and discussed the extra transient response performance that can be obtained from the selection of one type of controller over the other. This chapter investigates the transient performance of the buck converter with three different types of controller, to identify the one that provides the best transient performance. From the analysis of the converter's operation, equivalent circuit models in both state-space and transfer function forms are obtained. With these models, a PID controller, a state feedback controller and a predictive controller are designed for a 5 W (i.e. V_o = 5 V, I_o = 1 A) converter. The step responses of the converter with each of the three controllers are compared in both simulation and experiment.

3.2. Circuit operation and component selection

A standard synchronous buck converter (SBC) is shown in Fig. 3.1, containing two sub-circuits:

(i) a dc chopper which is formed by the MOSFETs, S_1 and S_2, allowing power to be periodically transferred to the filter in (ii)

(ii) a low-pass filter that is formed by the inductor L_m and capacitor C_o which attenuates the higher harmonic components to produce a DC output voltage (V_o).

Capacitor C_i is the DC-link reservoir capacitor and R_l is the load resistance.

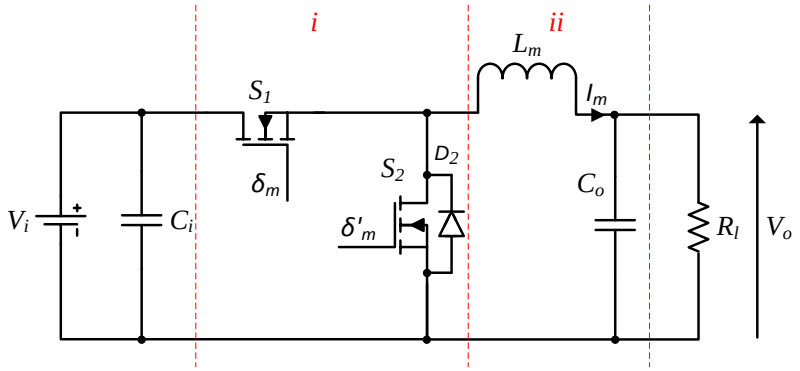


Fig. 3.1 Circuit diagram of the synchronous buck converter.

The two MOSFETs are switched in a complementary manner such that S_1 is driven by a rectangular waveform with a duty cycle, δ_{m}, which is defined as the ratio between the on-period $\left(t_{m(\mathrm{on})}\right)$ and switching period (T_{s}) as in (3.1), and S_2 is driven by the complemented duty cycle $\delta'_{\mathrm{m}}(=1-\delta_{\mathrm{m}})$:

$$\delta_{\mathrm{m}} = \frac{t_{m(\mathrm{on})}}{T_{\mathrm{s}}} \tag{3.1}$$

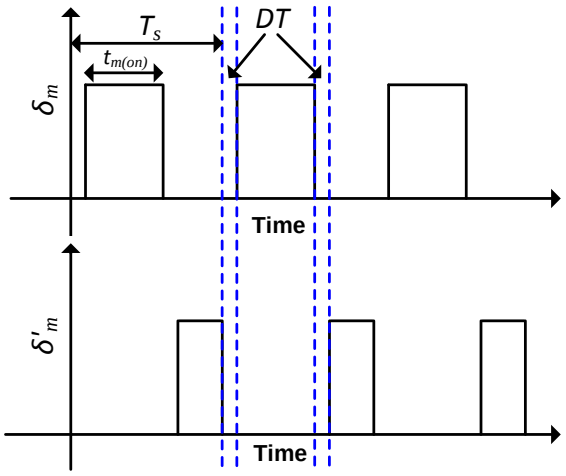


Fig. 3.2 MOSFETs drive signals with dead-times.

In order to prevent shoot-through which could damage the MOSFETs, a small dead-time (DT) interval is introduced to ensure both MOSFETs are switched off prior to a turn-on event as shown

in Fig. 3.2. The diode D_2, which may be the MOSFET body-diode, provides a freewheeling path during the dead-time as shown in Fig. 3.3.

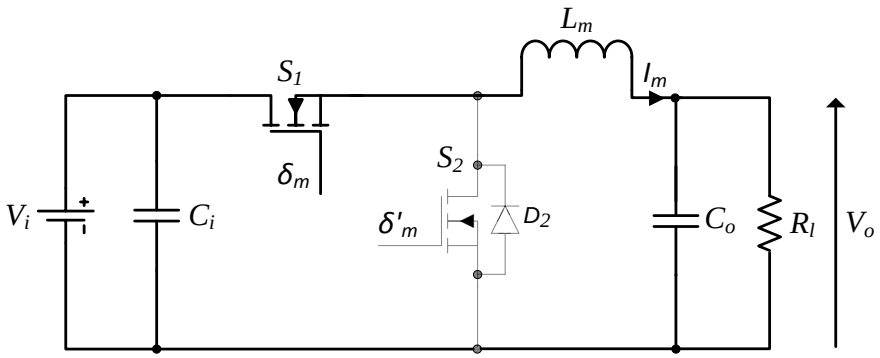


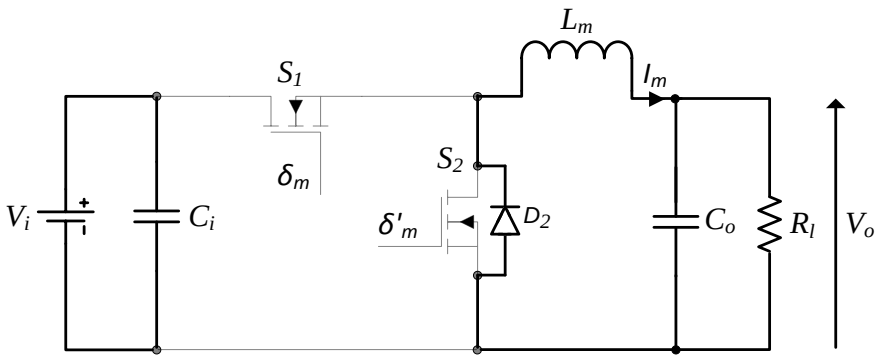
Fig. 3.3 Circuit diagram of SBC under the dead-time period.

With the bi-directional synchronous rectifier S_2, which allows the inductor current to flow in both directions (see Fig. 3.5), the synchronous buck converter always operates in the continuous conduction mode (CCM). In CCM, there are two distinct periods within each switching period, T_s, the on- and off-period. During the on-period, S_1 is switched on and S_2 is switched off as shown in Fig. 3.4 (a), the inductor current rises at the rate $(d/dt)I_{\mathrm{m}(+)}$ given in (3.2). During the off-period $(t_{m(\mathrm{off})})$, S_1 is switched off and S_2 is switched on as shown in Fig. 3.4 (b), the inductor current falls at the rate $(d/dt)I_{\mathrm{m}(-)}$ given in (3.3) (n.b parasitic resistances are neglected for all components). The net rate of change of the inductor current over one switching period, $(d/dt)I_{\mathrm{m(net)}}$, is the difference between the current increase during the on-period and decrease during the off-period over one switching period as formulated in (3.4), which can be simplified with the substitution of $t_{m(\mathrm{on})} = \delta_\mathrm{m} T_\mathrm{s}$ and $t_{m(\mathrm{off})} = (1-\delta_\mathrm{m})T_\mathrm{s}$.

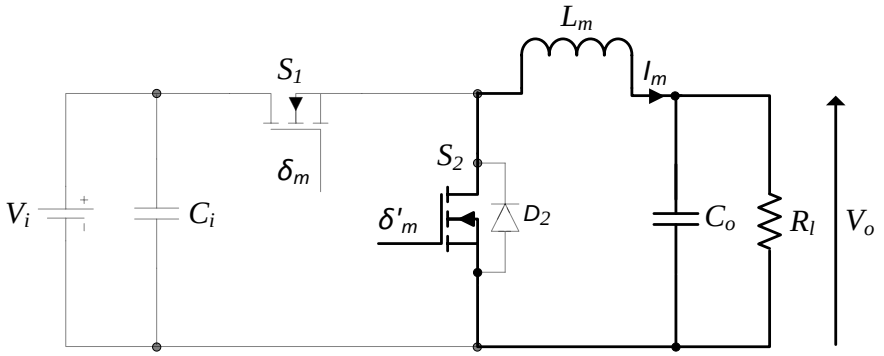
$$\frac{d}{dt} I_{\mathrm{m}(+)} = \frac{V_\mathrm{i} - V_\mathrm{o}}{L_\mathrm{m}} \tag{3.2}$$

$$\frac{d}{dt} I_{\mathrm{m}(-)} = \frac{-V_\mathrm{o}}{L_\mathrm{m}} \tag{3.3}$$

$$\frac{d}{dt}I_{\mathrm{m(net)}} = \frac{\frac{V_{\mathrm{i}}-V_{\mathrm{o}}}{L_{\mathrm{m}}}t_{m(\mathrm{on})}+\frac{-V_{\mathrm{o}}}{L_{\mathrm{m}}}t_{m(\mathrm{off})}}{T_s} = \frac{V_{\mathrm{i}}\delta_{\mathrm{m}}-V_{\mathrm{o}}}{L_{\mathrm{m}}} \tag{3.4}$$



(a)



(b)

Fig. 3.4 Circuit diagrams showing the two subintervals. (a) on-period (b) off-period.

The converter reaches steady state if the net rate of change of inductor current over one switching period is zero (volt-second balance) as shown in Fig. 3.5. By equating (3.4) to zero and solving for V_{o}, (3.5) is obtained which shows that for a given input voltage, there is a duty cycle for each output voltage where the converter reaches steady state $(\delta_{\mathrm{m(ss)}})$.

$$V_{\mathrm{o}} = \delta_{\mathrm{m}}V_{\mathrm{i}} \tag{3.5}$$

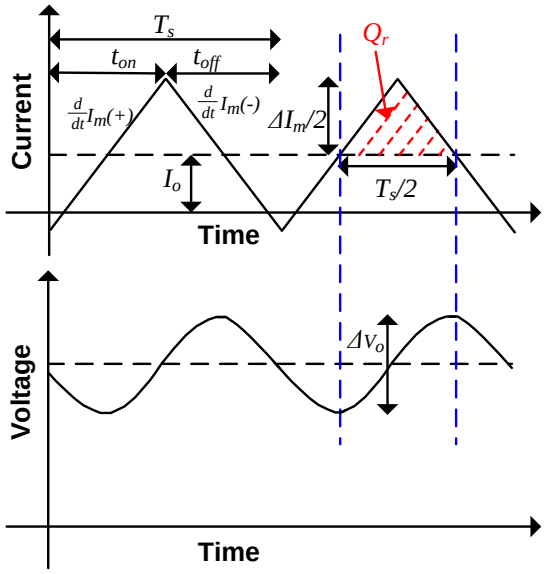


Fig. 3.5 Steady state inductor current and output voltage waveforms.

The inductor peak-to-peak current ripple (ΔI_{m}) in steady state can be found from the total change in inductor current during either the on- or off-period. Equation (3.6) shows ΔI_{m} calculated from the on-period, into which V_{o} is substituted from (3.5).

$$\Delta I_{\mathrm{m}} = \frac{V_{\mathrm{i}}-V_{\mathrm{o}}}{L_{\mathrm{m}}}\delta_{\mathrm{m(ss)}}T_{\mathrm{s}} = \frac{V_{\mathrm{i}}(1-\delta_{\mathrm{m(ss)}})}{L_{\mathrm{m}}}\delta_{\mathrm{m(ss)}}T_{\mathrm{s}} \tag{3.6}$$

By rearranging (3.6) in term of L_{m}, the minimum inductance that satisfies the current ripple requirement can be found by:

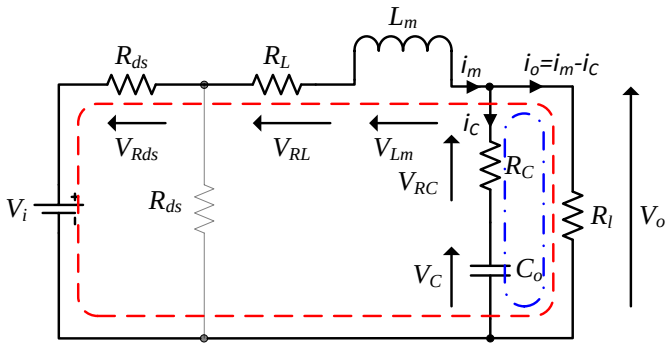
$$L_{\mathrm{m}} \geq \frac{V_{\mathrm{i}}-V_{\mathrm{o}}}{\Delta I_{\mathrm{m}}}\delta_{\mathrm{m(ss)}}T_{\mathrm{s}} \tag{3.7}$$

Due to the current ripple, ΔI_{m}, a net current that is the difference between the inductor current and the load current flows into C_{o}. The integral of this current is the charge (Q_{r}) responsible for the voltage ripple (ΔV_{o}). From the shaded area in the current waveform in Fig. 3.5, the minimum capacitance that must be selected in order to satisfy the output voltage ripple requirement can be found by (3.8):

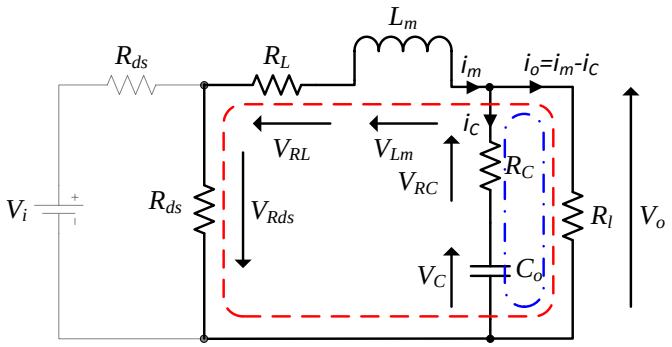
$$C_{\mathrm{o}} \geq \frac{1}{2}\frac{T_{\mathrm{s}}}{2}\frac{\Delta I_{\mathrm{m}}}{2}\frac{1}{\Delta V_{\mathrm{o}}} \geq \frac{\Delta I_{\mathrm{m}} T_{\mathrm{s}}}{8\Delta V_{\mathrm{o}}} \tag{3.8}$$

3.3. Equivalent circuit model

In order to obtain an accurate equivalent circuit model, parasitic resistances of the main components are now included. The MOSFETs on-state is replaced by the on-state resistance (R_{ds}) and the parasitic resistances of the inductor and capacitance are represented by R_{L} and R_{C} respectively. The equivalent circuits of the converter during the on- and off-period are given in Fig. 3.6 (a) and (b) respectively.



(a)



(b)

Fig. 3.6 Equivalent circuit model under different subintervals. (a) on-period (b) off-period.

From Fig. 3.6 (a) or (b), the output voltage for the on- and off-period are identical and can be found by Ohm's law. With Kirchhoff's current law (KCL), the following equation is obtained:

$$v_{\mathrm{o}} = R_{\mathrm{l}} i_{\mathrm{o}} = R_{\mathrm{l}} \left(i_{\mathrm{m}} - C_{\mathrm{o}} \frac{d}{dt} v_{\mathrm{C}} \right) \tag{3.9}$$

where v_{C} is the voltage across the output capacitor.

Applying Kirchhoff's voltage law (KVL) around the inner loop in dash-dotted line and the outer loop in dashed line in Fig. 3.6 (a) yield two first order differential equations in (3.10) and (3.11) for the on-period:

$$v_{\mathrm{c}} = -v_{\mathrm{R_C}} + v_{\mathrm{o}} = -R_{\mathrm{C}} C_{\mathrm{o}} \frac{d}{dt} v_{\mathrm{C}} + R_{\mathrm{l}} \left(i_{\mathrm{m}} - C_{\mathrm{o}} \frac{d}{dt} v_{\mathrm{C}} \right) \tag{3.10}$$

$$v_{\mathrm{i}} = v_{\mathrm{R_{ds}}} + v_{\mathrm{R_L}} + v_{\mathrm{L_m}} + v_{\mathrm{o}} = i_{\mathrm{m}} (R_{\mathrm{ds}} + R_{\mathrm{L}}) + L_{\mathrm{m}} \frac{d}{dt} i_{\mathrm{m}} + R_{\mathrm{l}} \left(i_{\mathrm{m}} - C_{\mathrm{o}} \frac{d}{dt} v_{\mathrm{C}} \right) \tag{3.11}$$

where $v_{\mathrm{R_C}}$, $v_{\mathrm{R_{ds}}}$, $v_{\mathrm{R_L}}$ are the voltages across R_{C}, R_{ds}, R_{L} respectively and $v_{\mathrm{L_m}}$ is the voltage across L_{m}.

By applying a similar procedure to the off-period equivalent circuit model in Fig. 3.6 (b), two first order equations for the off-period can also be found. Since the inner loop in Fig. 3.6 (b) is identical to that in Fig. 3.6 (a), the first equation is identical to (3.10). The second equation is:

$$0 = i_{\mathrm{m}} (R_{\mathrm{ds}} + R_{\mathrm{L}}) + L_{\mathrm{m}} \frac{d}{dt} i_{\mathrm{m}} + R_{\mathrm{l}} \left(i_{\mathrm{m}} - C_{\mathrm{o}} \frac{d}{dt} v_{\mathrm{C}} \right) \tag{3.12}$$

Using the above equations, the equivalent circuit model in state-space form is obtained with the following three steps:

Step 1: System state and output equations

In state-space modelling, the system (converter) is modelled by a state equation and an output equation which are formed by organising a set of first order differential equations in term of state variables. The state variables are variables that sufficiently describe the system future behaviour given the present state of the system and the excitation signal. With the two energy-storage elements in the converter, two state variables are required which are selected to be the inductor current, i_{m}, and capacitor voltage, v_{c}, (n.b. the state variables are non-unique, voltage across the inductor, $v_{\mathrm{L_m}}$, and many other variables may also be selected [38]).

With the choice of the state variables as i_{m} and v_{c}, the state equation for the on-period is obtained in (3.13) by rearranging (3.10) and (3.11) in terms of the state vector $\boldsymbol{x} = [i_{\mathrm{m}} \quad v_{\mathrm{c}}]^T$ and the input signal $u = V_{\mathrm{i}}$. Similarly, with (3.10) and (3.12), the state equation for the off-period is found in (3.14):

$$\dot{\boldsymbol{x}} = \boldsymbol{A}_1\boldsymbol{x} + \boldsymbol{B}_1 u = \begin{bmatrix} -\frac{(R_{\mathrm{l}}(R_{\mathrm{ds}}+R_{\mathrm{L}}+R_{\mathrm{C}})+R_{\mathrm{C}}(R_{\mathrm{ds}}+R_{\mathrm{L}}))}{\mathrm{L_m}(R_{\mathrm{l}}+R_{\mathrm{C}})} & -\frac{R_{\mathrm{l}}}{L_{\mathrm{m}}(R_{\mathrm{l}}+R_{\mathrm{C}})} \\ \frac{R_{\mathrm{l}}}{C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{C}})} & -\frac{1}{C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{C}})} \end{bmatrix}\boldsymbol{x} + \begin{bmatrix} \frac{1}{L_{\mathrm{m}}} \\ 0 \end{bmatrix} u \tag{3.13}$$

$$\dot{\boldsymbol{x}} = \boldsymbol{A}_2\boldsymbol{x} + \boldsymbol{B}_2 u = \begin{bmatrix} -\frac{(R_{\mathrm{l}}(R_{\mathrm{ds}}+R_{\mathrm{L}}+R_{\mathrm{c}})+R_{\mathrm{C}}(R_{\mathrm{ds}}+R_{\mathrm{L}}))}{L_{\mathrm{m}}(R_{\mathrm{l}}+R_{\mathrm{C}})} & -\frac{R_{\mathrm{l}}}{L_{\mathrm{m}}(R_{\mathrm{l}}+R_{\mathrm{C}})} \\ \frac{R_{\mathrm{l}}}{C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{c}})} & -\frac{1}{C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{C}})} \end{bmatrix}\boldsymbol{x} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} u \tag{3.14}$$

By isolating (3.9) also in term of the state variables and with the output signal $y = V_o$, the output equation for the on- and off-period is obtained as followed:

$$y = \boldsymbol{C}_1\boldsymbol{x} = \boldsymbol{C}_2\boldsymbol{x} = \begin{bmatrix} \frac{R_{\mathrm{l}}R_{\mathrm{C}}}{R_{\mathrm{l}}+R_{\mathrm{C}}} & \frac{R_{\mathrm{l}}}{R_{\mathrm{l}}+R_{\mathrm{C}}} \end{bmatrix}\boldsymbol{x} \tag{3.15}$$

The compact state and output equations are given in (3.14) and (3.15) respectively:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}_i\boldsymbol{x} + \boldsymbol{B}_i u \tag{3.16}$$

$$y = \boldsymbol{C}_i\boldsymbol{x} + D_i u \tag{3.17}$$

where the subscript i is 1 for the on-period and 2 for the off-period. $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$ and $\boldsymbol{x}$ in bold represent vectors. $\boldsymbol{x}$ is the state vector, u is the input signal and D is the direct feed-forward term which is not applicable in this system and is therefore set to zero.

Step 2: State-space averaging

Equations (3.13)-(3.15) form a system piecewise-linear set of equations that require a switching function to model the DC chopper (inverter) to allow the trajectories of the state-variables to be obtained. For control purposes such a detailed model of the switching process is not usually necessary and one often employs an averaging technique to simplify the analysis. In order to obtain the average behaviour of the converter over one period, the state and output equations are combined using a state-space averaging technique [38]. Each of the two state and output equations for the on- and off-period are weighted over their corresponding duration as follows:

$$\dot{\boldsymbol{x}} = \big(\boldsymbol{A}_1\delta_{\mathrm{m}} + \boldsymbol{A}_2(1-\delta_{\mathrm{m}})\big)\boldsymbol{x} + \big(\boldsymbol{B}_1\delta_{\mathrm{m}} + \boldsymbol{B}_2(1-\delta_{\mathrm{m}})\big)u \tag{3.18}$$

$$y = \big(\boldsymbol{C}_1\delta_{\mathrm{m}} + \boldsymbol{C}_2(1-\delta_{\mathrm{m}})\big)\boldsymbol{x} \tag{3.19}$$

From (3.13) and (3.14), $\boldsymbol{A}_1$ is identical to $\boldsymbol{A}_2$, the average behaviour of the state matrix ($\boldsymbol{A}$) in (3.18) is simplified to $\boldsymbol{A}_2$. Similarly, $\boldsymbol{C}_1$ is identical to $\boldsymbol{C}_2$, the average behaviour of the output matrix ($\boldsymbol{C}$) is simplified to $\boldsymbol{C}_2$. The average behaviour of the input matrix ($\boldsymbol{B}$) is found as follows:

$$\boldsymbol{B} = \begin{bmatrix} \frac{1}{L_{\mathrm{m}}} \\ 0 \end{bmatrix}\delta_{\mathrm{m}} + \begin{bmatrix} 0 \\ 0 \end{bmatrix}(1-\delta_{\mathrm{m}}) = \boldsymbol{B}_1\delta_{\mathrm{m}} \tag{3.20}$$

Substituting the average matrices into (3.13) and (3.14), the state-space averaged state and output equations are found:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}x + \boldsymbol{B}u = \begin{bmatrix} -\frac{(R_\mathrm{l}(R_\mathrm{ds}+R_\mathrm{L}+R_\mathrm{C})+R_\mathrm{c}(R_\mathrm{ds}+R_\mathrm{L}))}{L_\mathrm{m}(R_\mathrm{l}+R_\mathrm{C})} & -\frac{R_\mathrm{l}}{L_\mathrm{m}(R_\mathrm{l}+R_\mathrm{C})} \\ \frac{R_\mathrm{l}}{C_\mathrm{o}(R_\mathrm{l}+R_\mathrm{C})} & -\frac{1}{C_\mathrm{o}(R_\mathrm{l}+R_\mathrm{C})} \end{bmatrix} \boldsymbol{x} + \begin{bmatrix} \frac{1}{L_\mathrm{m}} \\ 0 \end{bmatrix} \delta_\mathrm{m} u \tag{3.21}$$

$$y = \boldsymbol{C}\boldsymbol{x} = \begin{bmatrix} \frac{R_\mathrm{l}R_\mathrm{C}}{R_\mathrm{l}+R_\mathrm{C}} & \frac{R_\mathrm{l}}{R_\mathrm{l}+R_\mathrm{C}} \end{bmatrix} \boldsymbol{x} \tag{3.22}$$

Step 3: Small-signal model

The state-space averaged model found in step 2 describes the system's steady state (DC) behaviour. However, for the controller design, the relationship between a small change in system output and a small change in duty cycle, or the transient behaviour (AC) is needed. This is obtained by introducing perturbation terms to the state vector $\boldsymbol{x}$, the output signal y and the duty cycle δ_m as in (3.23). The original $\boldsymbol{x}$, y and δ_m are rewritten in upper case $\boldsymbol{X}$, Y and Δ_m respectively and the terms with tilde are the perturbations.

$$\begin{aligned} \boldsymbol{x} &= \boldsymbol{X} + \tilde{\boldsymbol{x}} \\ y &= Y + \tilde{y} \\ \delta_\mathrm{m} &= \Delta_\mathrm{m} + \tilde{\delta}_\mathrm{m} \end{aligned} \tag{3.23}$$

By substituting the new variables in (3.23) into (3.21) and (3.22), the following equations are obtained:

$$\dot{\tilde{\boldsymbol{x}}} = \boldsymbol{A}(\boldsymbol{X} + \tilde{\boldsymbol{x}}) + \boldsymbol{B}_1 V_i \left(\Delta_\mathrm{m} + \tilde{\delta}_\mathrm{m}\right) \tag{3.24}$$

$$Y + \tilde{y} = \boldsymbol{C}(\boldsymbol{X} + \tilde{\boldsymbol{x}}) \tag{3.25}$$

As only the effects of perturbations are of concern, the terms belonging to the DC state and output equations (i.e. $\boldsymbol{AX} + \boldsymbol{B}\Delta_{\mathrm{m}}$ and $Y = \boldsymbol{CX}$) are set to zero. After substituting $\tilde{y} = \tilde{v}_{\mathrm{o}}$ the system's small-signal model in state-space form is found as follows:

$$\dot{\tilde{\boldsymbol{x}}} = \boldsymbol{A}\tilde{\boldsymbol{x}} + \boldsymbol{B}_1 V_{\mathrm{i}}\tilde{\delta}_{\mathrm{m}} = \begin{bmatrix} -\frac{(R_{\mathrm{l}}(R_{\mathrm{ds}}+R_{\mathrm{L}}+R_{\mathrm{C}})+R_{\mathrm{C}}(R_{\mathrm{ds}}+R_{\mathrm{L}}))}{L_{\mathrm{m}}(R_{\mathrm{l}}+R_{\mathrm{C}})} & -\frac{R_{\mathrm{l}}}{L_{\mathrm{m}}(R_{\mathrm{l}}+R_{\mathrm{C}})} \\ \frac{R_{\mathrm{l}}}{C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{C}})} & -\frac{1}{C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{C}})} \end{bmatrix}\tilde{\boldsymbol{x}} + \begin{bmatrix} \frac{1}{L_{\mathrm{m}}} \\ 0 \end{bmatrix} V_{\mathrm{i}}\tilde{\delta}_{\mathrm{m}} \tag{3.26}$$

$$\tilde{v}_{\mathrm{o}} = \boldsymbol{C}\tilde{\boldsymbol{x}} = \begin{bmatrix} \frac{R_{\mathrm{l}}R_{\mathrm{C}}}{R_{\mathrm{l}}+R_{\mathrm{C}}} & \frac{R_{\mathrm{l}}}{R_{\mathrm{l}}+R_{\mathrm{c}}} \end{bmatrix}\tilde{\boldsymbol{x}} \tag{3.27}$$

The state and output equations in (3.26) and (3.27) can be represented in the block diagram in Fig. 3.7 (n.b. in Fig. 3.7 $u = \tilde{\delta}_{\mathrm{m}}$ and $y = \tilde{v}_{\mathrm{o}}$):

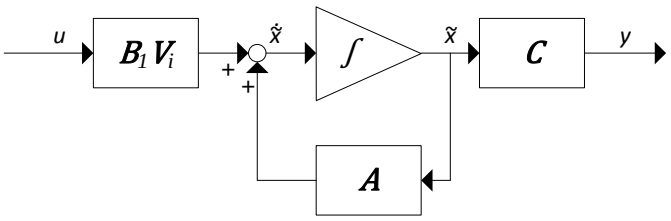


Fig. 3.7 Block diagram of system in state-space form.

The transfer function form of the small-signal model can be obtained by applying a Laplace transform to (3.26) which is solved in term of $\tilde{x}(s)$ and to (3.27) as follows:

$$\tilde{x}(s) = [s\boldsymbol{I} - \boldsymbol{A}]^{-1}\boldsymbol{B}_1 V_{\mathrm{i}}\tilde{\delta}_{\mathrm{m}}(s) \tag{3.28}$$

$$\tilde{v}_{\mathrm{o}}(s) = \boldsymbol{C}\tilde{x}(s) \tag{3.29}$$

where $\boldsymbol{I}$ is the identity matrix and s is the complex frequency.

Substituting (3.28) into (3.29) yields:

$$\tilde{v}_{\mathrm{o}}(s) = \boldsymbol{C}[s\boldsymbol{I} - \boldsymbol{A}]^{-1}\boldsymbol{B}_1 V_{\mathrm{i}}\tilde{\delta}_{\mathrm{m}}(s) \tag{3.30}$$

With the duty cycle as the control variable, the control-to-output transfer function is given by (3.31):

$$\frac{\tilde{v}_{\mathrm{o}}}{\tilde{\delta}_{\mathrm{m}}}(s) = \boldsymbol{C}[s\boldsymbol{I} - \boldsymbol{A}]^{-1}\boldsymbol{B}_1 V_{\mathrm{i}} \tag{3.31}$$

Substituting $\boldsymbol{A}$, $\boldsymbol{B}_1$ and $\boldsymbol{C}$ into (3.31), the system's small-signal control-to-output transfer function is found in as follows:

$$\frac{\tilde{v}_{\mathrm{o}}}{\tilde{\delta}_{\mathrm{m}}}(s) = \begin{bmatrix} \frac{R_{\mathrm{l}}R_{\mathrm{C}}}{R_{\mathrm{l}}+R_{\mathrm{C}}} & \frac{R_{\mathrm{l}}}{R_{\mathrm{l}}+R_{\mathrm{C}}} \end{bmatrix} \begin{bmatrix} s + \frac{(R_{\mathrm{l}}(R_{\mathrm{ds}}+R_{\mathrm{L}}+R_{\mathrm{C}})+R_{\mathrm{C}}(R_{\mathrm{ds}}+R_{\mathrm{L}}))}{L_{\mathrm{m}}(R_{\mathrm{l}}+R_{\mathrm{C}})} & -\frac{R_{\mathrm{l}}}{L_{\mathrm{m}}(R_{\mathrm{l}}+R_{\mathrm{C}})} \\ \frac{R_{\mathrm{l}}}{C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{C}})} & s + \frac{1}{C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{C}})} \end{bmatrix}^{-1} \begin{bmatrix} \frac{V_{\mathrm{i}}}{L_{\mathrm{m}}} \\ 0 \end{bmatrix}$$

$$= \frac{V_{\mathrm{i}}\left(C_{\mathrm{o}}R_{\mathrm{l}}R_{\mathrm{C}}s + \frac{\left(R_{\mathrm{l}}{}^2+R_{\mathrm{l}}R_{\mathrm{C}}\right)}{(R_{\mathrm{l}}+R_{\mathrm{C}})}\right)}{\left(L_{\mathrm{m}}C_{\mathrm{o}}(R_{\mathrm{l}}+R_{\mathrm{C}})\right)s^2 + \left(L_{\mathrm{m}} + C_{\mathrm{o}}(R_{\mathrm{L}}(R_{\mathrm{l}}+R_{\mathrm{C}}) + R_{\mathrm{ds}}(R_{\mathrm{l}}+R_{\mathrm{C}}) + R_{\mathrm{l}}R_{\mathrm{C}})\right)s + \frac{\left(R_{\mathrm{l}}^2+R_{\mathrm{L}}(R_{\mathrm{l}}+R_{\mathrm{C}})+R_{\mathrm{ds}}(R_{\mathrm{l}}+R_{\mathrm{C}})+R_{\mathrm{l}}R_{\mathrm{c}}\right)}{(R_{\mathrm{l}}+R_{\mathrm{C}})}} \tag{3.32}$$

The transfer function of the system in (3.32), is represented by a single block $G(s)$ as shown in the block diagram in Fig. 3.8 (n.b. $U(s) = \tilde{\delta}_{\mathrm{m}}(s)$ and $Y(s) = \tilde{v}_{\mathrm{o}}(s)$):

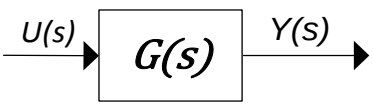


Fig. 3.8 Block diagram of system in transfer function form.

3.4. Controller design

It was shown in section 3.2 that the desired output voltage in an ideal SBC can be obtained with the duty cycle calculated by (3.5). This is open-loop control which is sensitive to system variation and change in operating conditions (i.e. the duty cycle must be adjusted to account for all voltage drops across the components parasitic resistances and also the change in input voltage). This sensitivity can be mitigated with closed-loop control where a feedback loop is formed around the system as shown in Fig. 3.9. For example [38][39] shows that a system with a simple proportional gain (K_{P}) controller with a gain of 100 reduces the steady-state error from 10% in open-loop to 0.1%, given the same 10% disturbance.

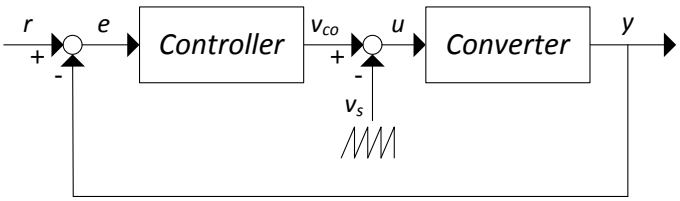


Fig. 3.9 Block diagram of closed-loop system.

In a closed-loop system, the control signal (v_{co}) is produced by the controller according to the error signal (e) which is the difference between the set-point or desired point (r) and the actual system response y. The control signal is transformed into the converter's control signal (actually the MOSFET gate signals $u = \delta_{\mathrm{m}}$) by a pulse-width modulator (PWM) where v_{co} is usually compared with a saw-tooth signal, v_{s}, producing a high signal wherever $v_{\mathrm{s}} < v_{\mathrm{co}}$, otherwise a low signal as shown in Fig. 3.10. This conversion maps the range of control signal $\left(v_{\mathrm{co(max)}} - v_{\mathrm{co(min)}}\right)$ to the range of duty cycle $\left(\delta_{\mathrm{m(max)}} - \delta_{\mathrm{m(min)}}\right)$ which can be described by a constant gain (K_{PWM}) in (3.33):

$$K_{\mathrm{PWM}} = \frac{\delta_{\mathrm{m(max)}} - \delta_{\mathrm{m(min)}}}{v_{\mathrm{co(max)}} - v_{\mathrm{co(min)}}} \tag{3.33}$$

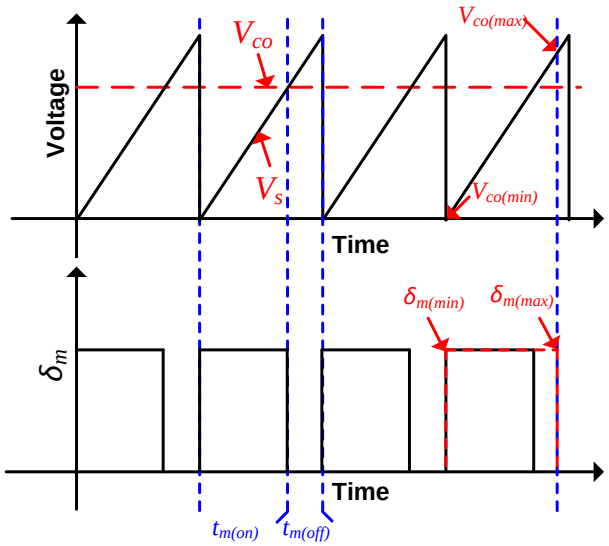


Fig. 3.10 Operation of PWM, $u = 1$ if $v_s < v_{co}$ otherwise $u = 0$.

3.4.1. Performance indices

Depending on the types of controller and how they are designed, the system steady state and transient responses will be different. In order identify the controller that produces the optimum response, a quantitative measure of each response is required. From the transient response in Fig. 3.11, the amplitude and duration of the transient oscillation determines the total area above and below the set-point as shaded in the figure. Optimum control may minimise this area. The area can be measured by integrating all the error which is obtained by subtracting the system response from the set-point. This error is positive when the response is below the set-point and is negative otherwise. The negative sign can simply be removed by inversion as is done in the performance index integral of the absolute magnitude of the error (IAE) or by squaring the error as used in the integral of the square of the error (ISE) index. With most converters demanding zero steady-state error, the time at which the error occurs can also be included to penalise more heavily slowly decaying transient errors. The two performance indices that take time into consideration are the integral of time multiplied by absolute error (ITAE) as in (3.34) and integral of time multiplied by the squared error (ITSE) [38].

$$ITAE = \int_0^{T_{\text{set}}} t|e(t)|\,dt \tag{3.34}$$

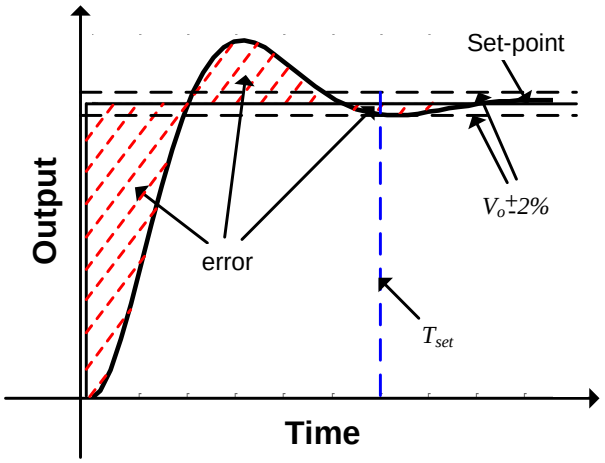


Fig. 3.11 Example of a system step response.

Using the ITAE performance index, researchers have performed simulation on system with different orders and coefficients [38]. The result is sets of coefficients which when used produce a step response that is ITAE optimised. The set of coefficients for a third-order system, which will be used in the following sections for controllers design, is listed in (3.35):

$$s^3 + 1.75\omega_{\text{n}}s^2 + 2.15{\omega_{\text{n}}}^2 s + {\omega_{\text{n}}}^3 \tag{3.35}$$

The natural frequency (ω_{n}) is found by (3.36) given the desired settling time (T_{set}) and damping ratio ζ. T_{set} is the time the system takes to settle within a certain percentage ($\pm 2\%$ in Fig. 3.11) of the set-point and ζ controls how quickly the oscillations decay.

$$\omega_{\text{n}} = \frac{4}{\zeta T_{\text{set}}} \tag{3.36}$$

3.4.2. Robust PID control

As was mentioned, a proportional controller reduces the steady-state error to a small value. In order to eliminate the steady-state error and also to shape the transient response, an integral gain (K_{I}) and derivative gain (K_{D}) are added to form what is commonly known as a PID controller as shown in the block diagram of Fig. 3.12 (n.b. K_{PWM} is assumed to be one which allows the block diagram to be drawn without the PWM signal for clarity). The proportional term produces a control action that is proportional to the error, $E(s)$. The integral term accumulates error over time, which has the effect of amplifying the error by time, allowing small residual steady-state error to be detected and eliminated. The derivative term operates on the rate of change of error, predicting the system behaviour to improve the system response. The transfer function of the PID controller, $G_c(s)$, is given by (3.37):

$$G_{\mathrm{c}}(s) = \frac{K_{\mathrm{D}}s^2 + K_{\mathrm{P}}s + K_{\mathrm{I}}}{s} \tag{3.37}$$

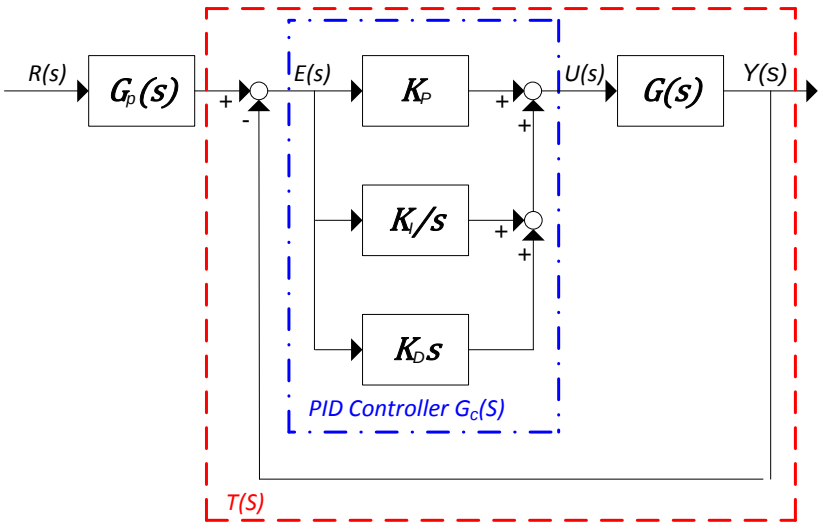


Fig. 3.12 Block diagram of system with robust PID controller.

For ease of manipulation, the system transfer function in (3.32) is substituted by the generalised notation as in (3.38). With (3.37) and (3.38), the compensated system transfer function $\left(T(s)\right)$ is found to be a third-order function as in (3.39):

$$G(s) = \frac{K_S}{s^2+2\zeta\omega_n s+{\omega_n}^2} \tag{3.38}$$

$$T(s) = \frac{GG_{\mathrm{c}}(s)}{1+GG_{\mathrm{c}}(s)} = \frac{K_{\mathrm{s}}\left(K_{\mathrm{D}}s^2+K_{\mathrm{P}}s+K_{\mathrm{I}}\right)}{s^3+(2\zeta\omega_{\mathrm{n}}+K_1K_{\mathrm{D}})s^2+({\omega_{\mathrm{n}}}^2+K_1K_{\mathrm{P}})s+K_1K_{\mathrm{I}}} \tag{3.39}$$

With a robust PID controller, the transient response is ITAE optimised. The coefficients of the compensated system characteristic equation (i.e. denominator) should follow that given in (3.35), leading to the following compensated system transfer function:

$$T_{\mathrm{ITAE}}(s) = \frac{{\omega_{\mathrm{n}}}^3}{s^3+1.75\omega_{\mathrm{n}}s^2+2.15{\omega_{\mathrm{n}}}^2s+{\omega_{\mathrm{n}}}^3} \tag{3.40}$$

The denominator of (3.40) can be obtained by selecting the three PID parameters, K_{P}, K_{I} and K_{D} through matching the coefficients in (3.39) to those in (3.40) as in (3.41):

$$\begin{aligned} 2\zeta\omega_{\mathrm{n}} + K_{\mathrm{s}}K_{\mathrm{D}} &= 1.75\omega_{\mathrm{n}} \\ {\omega_{\mathrm{n}}}^2 + K_{\mathrm{s}}K_{\mathrm{P}} &= 2.15{\omega_{\mathrm{n}}}^2 \\ K_{\mathrm{s}}K_{\mathrm{I}} &= {\omega_{\mathrm{n}}}^3 \end{aligned} \tag{3.41}$$

The numerator of (3.40) can be obtained by cancelling the zeros introduced by the controller with a pre-filter, $G_{\mathrm{p}}(s)$, with the following transfer function:

$$G_{\mathrm{p}}(s)\frac{{\omega_{\mathrm{n}}}^3}{K_{\mathrm{s}}(K_{\mathrm{D}}s^2+K_{\mathrm{P}}s+K_{\mathrm{I}})} \tag{3.42}$$

3.4.3. State feedback control

Instead of operating on the error with an accumulator and a differentiator as in PID controllers, the state variables are fed back feedback with two constant gains k_1 and k_2 in a full-state feedback controller. The practical controller implementation is simpler in state feedback control but it requires all the state variables to be measured unless a state observer [38] is used, which is outside the scope of this thesis. In order to achieve line and load regulation, a feedback loop with an integrator is also included. Using the state-space averaged model from section 3.3, the combined system featuring the state feedback gains ($\boldsymbol{K}$ matrix) with integral gain (K_i) is shown in Fig. 3.13. in this diagram, $\boldsymbol{K}$ is the vector of the two constant gains $[k_1 \quad k_2]$ and K_i is the integrator gain.

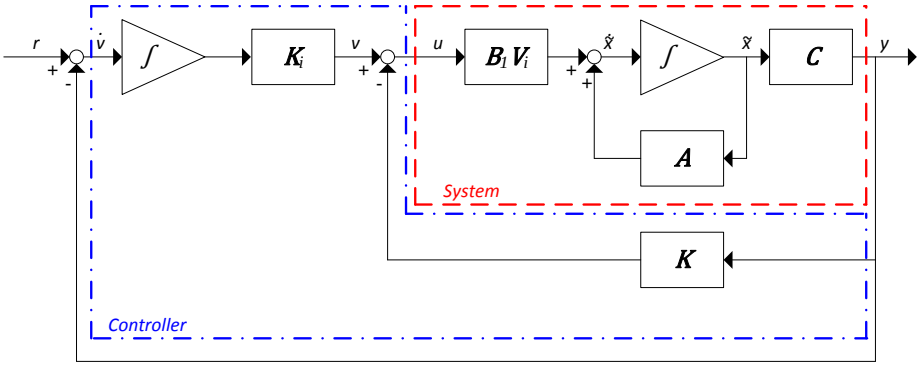


Fig. 3.13 Block diagram of system with state feedback with integral control.

Following the signal flow paths in Fig. 3.13, three first-order differential equations can be derived. Two are from the system which was found in (3.26) and one from the integrator given in (3.43). Defining a new state vector $\boldsymbol{x}' = [\tilde{x} \quad v]^T$, the augmented state equation of the three equations is formed in (3.44):

$$\dot{\boldsymbol{v}} = -C\tilde{\boldsymbol{x}} + r \tag{3.43}$$

$$\dot{\boldsymbol{x}}' = \boldsymbol{A}'\boldsymbol{x}' + \boldsymbol{B}'u + \boldsymbol{E}r = \begin{bmatrix} \boldsymbol{A} & 0 \\ -\boldsymbol{C} & 0 \end{bmatrix}\boldsymbol{x}' + \begin{bmatrix} \boldsymbol{B} \\ 0 \end{bmatrix}u + \begin{bmatrix} 0 \\ I \end{bmatrix}r \tag{3.44}$$

Following again the signal flow path in Fig. 3.13, u is found as in (3.45). After substituting into (3.44), the compensated system equation is found as in (3.46):

$$u = -\boldsymbol{K}'\boldsymbol{x}' = [\boldsymbol{K} \quad -K_{\mathrm{i}}]\boldsymbol{x}' \tag{3.45}$$

$$\dot{\boldsymbol{x}}' = \boldsymbol{A}'\boldsymbol{x}' - \boldsymbol{B}'\boldsymbol{K}'\boldsymbol{x}' + \boldsymbol{E}r = \left(\boldsymbol{A}' - \boldsymbol{B}'\boldsymbol{K}'\right)\boldsymbol{x}' + \boldsymbol{E}r \tag{3.46}$$

By expanding (3.46), the following state equation is obtained:

$$\begin{aligned}\dot{\boldsymbol{x}}' = \boldsymbol{A}''\boldsymbol{x}' + \boldsymbol{E}r &= \left(\begin{bmatrix} A_{11} & A_{12} & 0 \\ A_{21} & A_{22} & 0 \\ -C_{11} & -C_{12} & 0 \end{bmatrix} - \begin{bmatrix} B_{11} \\ 0 \\ 0 \end{bmatrix}[k_1 \quad k_2 \quad -K_{\mathrm{i}}]\right)\boldsymbol{x}' + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} r \\ &= \begin{bmatrix} A_{11} - B_{11}k_1 & A_{12} - B_{11}k_2 & B_{11}K_{\mathrm{i}} \\ A_{21} & A_{22} & 0 \\ -C_{11} & -C_{12} & 0 \end{bmatrix}\boldsymbol{x}' + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} r\end{aligned} \tag{3.47}$$

The compensated system characteristic can be found from the determinant of (3.47) as follows:

$$det\left(s\boldsymbol{I} - \boldsymbol{A}''\right) = \begin{bmatrix} s - (A_{11} - B_{11}k_1) & -A_{12} + B_{11}k_2 & -B_{11}K_{\mathrm{i}} \\ -A_{21} & s - A_{22} & 0 \\ C_{11} & C_{12} & s \end{bmatrix}$$

$$\begin{aligned} = s^3 &+ (-A_{22} - A_{11} + B_{11}k_1)s^2 \\ &+ (A_{11}A_{22} - A_{22}B_{11}k_1 + A_{12}A_{21} - A_{21}B_{11}k_2 + B_{11}C_{11}K_{\mathrm{i}})s \\ &- (A_{21}C_{12} + A_{22}C_{11})B_{11}k_{\mathrm{i}} \end{aligned} \tag{3.48}$$

Just as in robust PID control, the coefficients of the compensated system characteristic equation are given in (3.35). The three gains of the state feedback control with integral control, k_1, k_2 and K_{i}, are found by matching the coefficients in (3.48) to that in (3.35) as in (3.49):

$$-A_{22} - A_{11} + B_{11}k_1 = 1.75\omega_n$$

$$A_{11}A_{22} - A_{22}B_{11}k_1 - A_{12}A_{21} + A_{21}B_{11}k_2 + B_{11}C_{11}K_i = 2.15{\omega_n}^2 \quad (3.49)$$

$$(-A_{21}C_{12} - A_{22}C_{11})B_{11}K_i = {\omega_n}^3$$

3.4.4. Predictive control

In predictive control, the control law can be derived with the system expressed in either state-space and transfer function form. The transfer function form is chosen here for the reason of personal preference. The configuration of the system with the predictive controller is shown in Fig. 3.14. The control law contains three gains, the feedback gain N_k, the feedforward gain P_r and control gain D_k. The block $z/(z-1)$ is the discrete-time equivalent of an integrator.

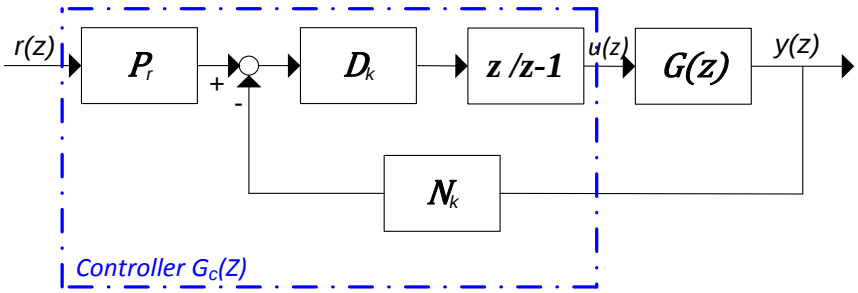


Fig. 3.14 Block diagram of system with predictive controller.

The three tuning factors of a predictive controller are as followed:

- n_y, the output horizon which determines how many steps ahead the system response is predicted, and should be greater than the system settling time, T_{set}, which can be found by (3.50)

$$n_y = \frac{T_{set}}{T_s} \quad (3.50)$$

- n_{u}, the input horizon which determines how many steps of control move is predicted, three should be enough for most system.
- λ, the weighting function of the control input, the larger its value, the smaller the input change is allowed, reducing the settling time.

In order to form the prediction equation, the system transfer function with integrator is rearranged in incremental form as follows:

$$\begin{aligned}&(1 + A_1 z^{-1} + A_2 z^{-2} + \cdots + A_{\mathrm{n}+1} z^{-n-1}) y_{\mathrm{k}} \\ &= (b_1 z^{-1} + b_2 z^{-2} + \cdots + b_{\mathrm{n}+1} z^{-n}) \Delta u_{\mathrm{k}}\end{aligned} \tag{3.51}$$

The difference equations for the next sample and the ones that follow the so-called k-step ahead predictor, are formulated in (3.52), which can be organised into matrices as in (3.53):

$$\begin{aligned}y_{\mathrm{k}+1} + A_1 y_{\mathrm{k}} + \cdots + A_{\mathrm{n}+1} y_{\mathrm{k}-\mathrm{n}} &= b_1 \Delta u_{\mathrm{k}} + b_2 \Delta u_{\mathrm{k}-1} + \cdots + b_{\mathrm{n}} \Delta u_{\mathrm{k}-\mathrm{n}+1} \\ y_{\mathrm{k}+2} + A_1 y_{\mathrm{k}+1} + \cdots + A_{\mathrm{n}+1} y_{\mathrm{k}-\mathrm{n}+1} &= b_1 \Delta u_{\mathrm{k}+1} + b_2 \Delta u_{\mathrm{k}} + \cdots + b_{\mathrm{n}} \Delta u_{\mathrm{k}-\mathrm{n}+2} \\ &\vdots \\ y_{\mathrm{k}+\mathrm{n_y}} + \cdots + A_{\mathrm{n}+1} y_{\mathrm{k}+\mathrm{n_y}+1-\mathrm{n}} &= b_1 \Delta u_{\mathrm{k}+\mathrm{n_y}-1} + \cdots + b_{\mathrm{n}} \Delta u_{\mathrm{k}+\mathrm{n_y}-\mathrm{n}}\end{aligned} \tag{3.52}$$

$$\begin{aligned}&\begin{bmatrix} 1 & 0 & .. & 0 \\ A_1 & 1 & .. & 0 \\ A_2 & A_1 & .. & 0 \\ : & : & : & : \end{bmatrix} \begin{bmatrix} y_{\mathrm{k}+1} \\ y_{\mathrm{k}+2} \\ : \\ y_{\mathrm{k}+\mathrm{n_y}} \end{bmatrix} + \begin{bmatrix} A_1 & A_2 & .. & A_{\mathrm{n}+1} \\ A_2 & A_3 & .. & 0 \\ A_3 & A_4 & .. & 0 \\ : & : & : & : \end{bmatrix} \begin{bmatrix} y_{\mathrm{k}} \\ y_{\mathrm{k}-1} \\ : \\ y_{\mathrm{k}-\mathrm{n}} \end{bmatrix} \\ &= \begin{bmatrix} b_1 & 0 & .. & 0 \\ b_2 & b_1 & .. & 0 \\ b_3 & b_2 & .. & 0 \\ : & : & : & : \end{bmatrix} \begin{bmatrix} \Delta u_{\mathrm{k}} \\ \Delta u_{\mathrm{k}+1} \\ : \\ \Delta u_{\mathrm{k}+\mathrm{n_y}-1} \end{bmatrix} + \begin{bmatrix} b_2 & b_3 & .. & b_{\mathrm{n}} \\ b_3 & b_4 & .. & 0 \\ b_4 & b_5 & .. & 0 \\ : & : & : & : \end{bmatrix} \begin{bmatrix} \Delta u_{\mathrm{k}-1} \\ \Delta u_{\mathrm{k}-2} \\ : \\ \Delta u_{\mathrm{k}-\mathrm{n}+1} \end{bmatrix}\end{aligned} \tag{3.53}$$

With the use of Toeplitz/Hankel notation [45] (arrow pointing right representing the future value and arrow pointing left representing the current and past values), the output prediction in (3.53) can be simplified to (3.54):

$$C_{\mathrm{A}} y_{\rightarrow \mathrm{k}} + H_{\mathrm{A}} y_{\leftarrow \mathrm{k}} = C_{\mathrm{zb}} \Delta u_{\rightarrow \mathrm{k}-1} + H_{\mathrm{zb}} \Delta u_{\leftarrow \mathrm{k}-1} \tag{3.54}$$

By rearranging (3.54) in term of $y_{\rightarrow \mathrm{k}}$ and substituting $H = C_{\mathrm{A}}^{-1} C_{\mathrm{zb}}$, $P = C_{\mathrm{A}}^{-1} H_{\mathrm{zb}}$ and $Q = -C_{\mathrm{A}}^{-1} H_{\mathrm{A}}$, the following equation is obtained:

$$\begin{aligned} y_{\rightarrow \mathrm{k}} &= C_{\mathrm{A}}^{-1} [C_{\mathrm{zb}} \Delta u_{\rightarrow \mathrm{k}-1} + H_{\mathrm{zb}} \Delta u_{\leftarrow \mathrm{k}-1} - H_{\mathrm{A}} y_{\leftarrow \mathrm{k}}] \\ &= H \Delta u_{\rightarrow \mathrm{k}-1} + P \Delta u_{\leftarrow \mathrm{k}-1} + Q y_{\leftarrow \mathrm{k}} \end{aligned} \tag{3.55}$$

The control law is obtained by minimising the error and control input as in the cost function (J) in (3.56). Where $||.||_2$ is the 2- norm which minimise area of a plane.

$$J = \|r_{\rightarrow} - y_{\rightarrow}\|_2^2 + \lambda \|\Delta u_{\rightarrow}\|_2^2 \tag{3.56}$$

By minimising the future change in control move $\Delta u_{\rightarrow}$ and locating the minimum by setting the rate of change to zero (i.e. $dJ/d\Delta u_{\rightarrow} = 0$). The control law in (3.57) is obtained.

$$\begin{aligned} \Delta u_{\mathrm{k}} &= (H^T H + \lambda I)^{-1} H^T (r_{\rightarrow} - Q y_{\leftarrow} - P \Delta u_{\leftarrow}) \\ &= P_{\mathrm{r}} r_{\rightarrow} - N_{\mathrm{k}} y_{\leftarrow} - D_{\mathrm{k}} \Delta u_{\leftarrow} \end{aligned} \tag{3.57}$$

where $P_{\mathrm{r}} = (H^T H + \lambda I)^{-1} H^T$, $N_{\mathrm{k}} = (H^T H + \lambda I)^{-1} H^T P$ and $D_{\mathrm{K}} = (H^T H + \lambda I)^{-1} H^T Q$.

For a second-order system, the incremental form of the control law in (3.57) is as follows:

$$u(k) = r(k) + u(k-1) + y(k) + y(k-1) + y(k-2) \tag{3.58}$$

3.4.5. Digital implementation

Due to the number of controllers designed in this work, it is more convenient to implement them using a microcontroller. The robust PID controller, the PID control law in (3.38) can be written in time constant form in (3.59), which can then be converted to the discrete-time domain by Euler's method [89] as in (3.60):

$$\frac{\frac{K_D}{K_I}s^2+\frac{K_P}{K_I}s+1}{s} = \frac{T_I T_D s^2+T_I s+1}{s} \tag{3.59}$$

$$x(k) = x[k-1] + K_e\left[\left(1+\frac{T_s}{T_I}+\frac{T_D}{T_s}\right)e[k] - \left(1+2\frac{T_D}{T_s}\right)e[k-1] + \frac{T_D}{T_s}e[k-2]\right] \tag{3.60}$$

where T_I is the integral time constant and T_D is the derivative time constant.

For the state feedback controller, the discrete-time equivalent of the integrator gain (K_{Id}) is obtained by (3.61):

$$K_{Id} = K_I T_s \tag{3.61}$$

3.5. Design examples and experimental results

In order to compare the transient response of the converter with the three controllers, a converter was designed with the following specification: input voltage V_i = 12 V, output voltage V_o = 5 V, output current I_o = 1 A, switching frequency f_s = 20 kHz, output voltage ripple $\Delta V_o < 1\%$, steady-state error $e_{ss} = 0$, settling time T_{set} = 1 ms and percentage overshoot < 1%.

Using Ohm's law, for the given I_o, the load resistance, R_l, is found to be 5 Ω. For the given V_o, the duty cycle is calculated by (3.5) to be 41.7%. With this δ_m and T_s = 50 µs, the filter inductor L_m and capacitor C_o are calculated by (3.7) and (3.8) to be 365 µH and 50 µF respectively. The component's parasitic resistances, R_C and R_L are measured with a milliohm meter to be

36 mΩ, 34 mΩ respectively and MOSFET R_{ds} is given in manufacturer's datasheet to be 540 mΩ. Substituting all the parameters into the (3.26) and (3.27), and (3.32), the system state and output equations are found in (3.62) and (3.63) respectively, and the transfer function is found in (3.64):

$$\dot{\tilde{\boldsymbol{x}}} = \begin{bmatrix} -1648 & -2682 \\ 19840 & -4337 \end{bmatrix} \tilde{\boldsymbol{x}} + \begin{bmatrix} 2701 \\ 0 \end{bmatrix} \tilde{\delta}_{m} \tag{3.62}$$

$$\tilde{y} = [0.036 \quad 0.992]\tilde{\boldsymbol{x}} \tag{3.63}$$

$$G(s) = \frac{8.153x10^{-6}s+4.529}{8.531x10^{-8}s^2+5.106x10^{-4}s+5.149} \tag{3.64}$$

3.5.1. Robust PID controller

For the design of the robust PID controller, (3.64) is nominalised against s^2, the high frequency zero from the capacitor ESR is also removed to yield:

$$G(s) = \frac{5.5x10^7}{s^2+5985s+6x10^7} \tag{3.65}$$

By combining (3.65) with the transfer function of the PID controller in (3.37), the control-to-output transfer function is found:

$$T(s) = \frac{5.5x10^7(K_D s^2+K_P s+K_I)}{s^3+(5985+5.5x10^7K_D)s^2+(6x10^7+5.5x10^7K_P)s+5.5x10^7K_I} \tag{3.66}$$

With T_{set} and ζ selected to be 1 ms and is 0.71 respectively, ω_n is calculated by (3.36) to be 5676. After substituting into the third-order equation in (3.35), the desired control-to-output transfer function is:

$$T_{ITAE}(s) = \frac{1.811x10^{11}}{s^3+9901s^2+6.88x10^7s+1.811x10^{11}} \tag{3.67}$$

Equating the coefficients of (3.66) with those in (3.67) as in (3.68), the three parameters of the PID controller are found: $K_{\mathrm{P}} = 0.16$, $K_{\mathrm{I}} = 3293$ and $K_{\mathrm{D}} = 7.12 \text{ x } 10^{-5}$.

$$5985 + 5.5 \text{ x } 10^{7} K_{\mathrm{D}} = 9901$$

$$6 \text{ x } 10^{7} + 5.5 \text{ x } 10^{7} K_{\mathrm{P}} = 6.88 \text{ x } 10^{7} \tag{3.68}$$

$$5.5 \text{ x } 10^{7} K_{\mathrm{I}} = 1.811 \text{ x } 10^{11}$$

A converter with this controller is simulated in Matlab/Simulink as in the block diagram in Fig. 3.15. Included in the block diagram are the converter transfer function, the PID controller, the PWM gain which is detailed in (3.33), the ADC gain which maps the range of measured voltage into the range of the saw-tooth signal, the dead-time of 1% of duty cycle and the saturation block which prevents duty cycle from exceeding 100%.

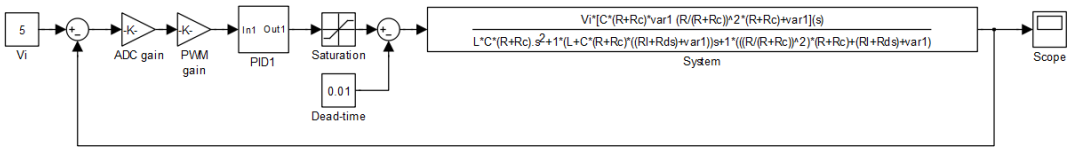


Fig. 3.15 Simulink model of system with the robust PID controller.

The system step responses with and without the pre-filter are shown in solid and dashed lines in Fig. 3.16 respectively, the effect of the pre-filter is small so will not be implemented practically.

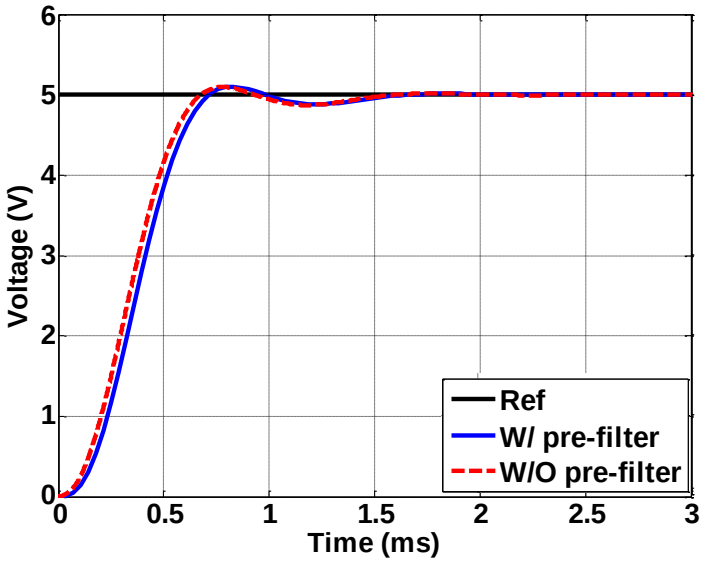


Fig. 3.16 Simulated system step responses with PID controller.

3.5.2. State feedback controller

Following the design procedure in section 3.4.3, by substituting the variable in (3.62) and (3.63) into (3.48), the following characteristic equation is obtained:

$$\begin{aligned} & s^3 + (4337 + 1648 + 2676k_1)s^2 \\ & \quad + (7.1x10^6 + 1.16x10^7k_2 - 5.3x10^7 - 5.3x10^7k_2 - 95.6k_\mathrm{i})s \\ & \quad + (19844 + 156)2676k_\mathrm{i} \end{aligned} \tag{3.69}$$

With the same ω_n found in previous section to be 5676, the desired characteristic equation is:

$$s^3 + 9901s^2 + 6.88x10^7s + 1.811x10^{11} \tag{3.70}$$

Matching the coefficients of (3.69) to those in (3.70) results in (3.71), the three gains are found: $k_1 = 1.46,\ k_2 = -0.167$ and $K_\mathrm{i} = 3411$.

$$4337 + 1648 + 2676k_1 = 9901 \tag{3.71}$$

$$7.1x10^6 + 1.16x10^7k_1 - 5.3x10^7 - 5.3x10^7k_2 - 95.6k_\mathrm{i} = 6.88x10^7$$

$$(19844 + 156)2676k_\mathrm{i} = 1.811x10^{11}$$

A converter with this state feedback controller is simulated in Simulink with the block diagram in Fig. 3.17. As with PID controller, the ADC, the PWM, dead-time and saturation block are also include:

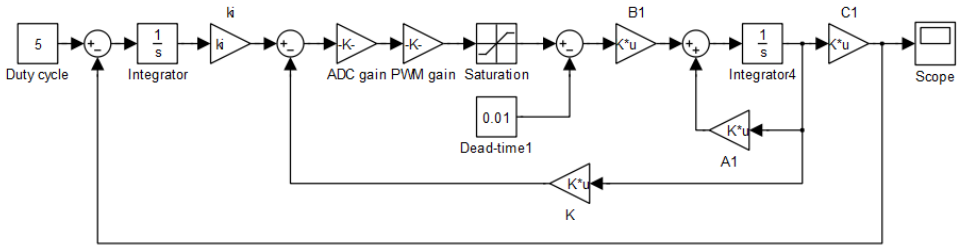


Fig. 3.17 Simulink model of system with the state feedback control with integral control.

The system step response with the state feedback controller is shown by the dotted line in Fig. 3.18. The response is only marginally better than that with the robust PID controller, which is expected as both controllers are designed base on the same ITAE optimised coefficients.

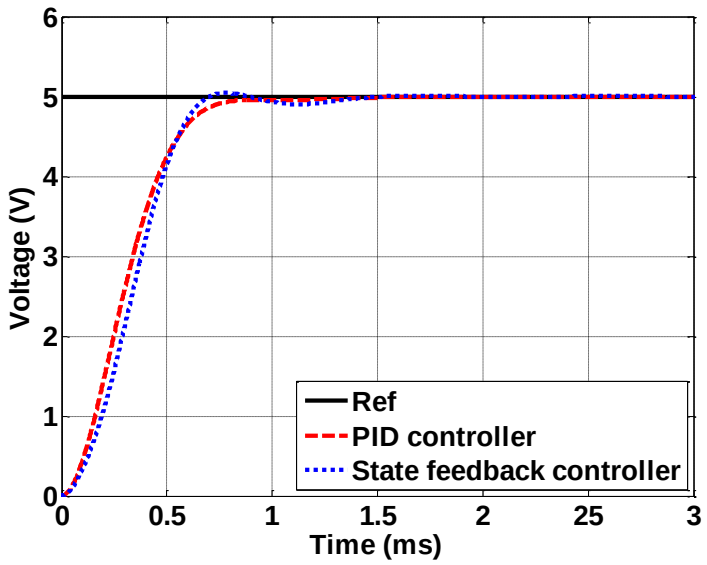


Fig. 3.18 Simulated system step response with state feedback controller.

3.5.3. Predictive controller

The predictive controller is designed based on the procedure in section 3.4.4. The controller is simulated in Simulink with the block diagram in Fig. 3.19:

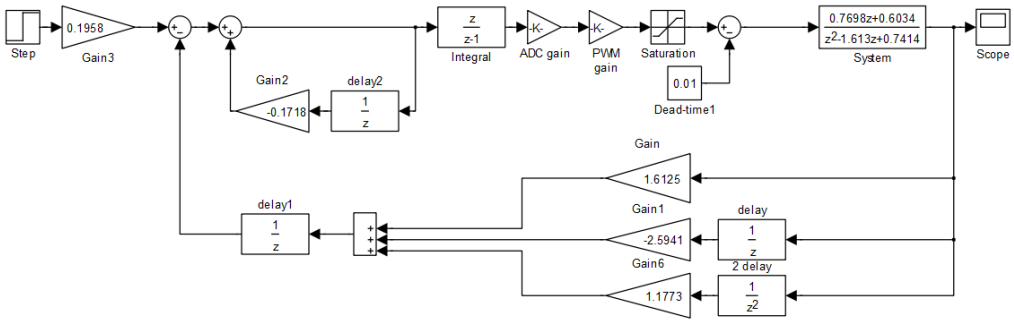


Fig. 3.19 Simulink model of system with predictive controller.

Using (3.50), n_y must be greater than or equal to 20. n_y = 30 is selected in this design. n_u and λ are initially set to 1 and 0 respectively. The control law $(C1)$ is found with (3.57) and (3.58) and is shown in Table 3.1. The step response with $C1$ is shown by the dashed line in Fig. 3.20 which has an overshoot larger than the overshoot requirement. To reduce the overshoot, λ is increased to 60 which lead to control law $(C2)$ with the step response shown by the dotted line in Fig. 3.20. The overshoot is now within the requirement. To fine tune the controller, the control law $(C3)$ with N_u increased to 2 and λ reduced to 55 is formed. $C3$ leads to a response with lower overshoot and slightly better settling time as shown in dash-dotted line in Fig. 3.20.

	$r(k)$	$u(k-1)$	$y(k)$	$y(k-1)$	$y(k-2)$
C1	1.0957	−0.9700	−9.0365	14.5571	−6.6163
C2	0.2180	−0.1930	−1.7832	2.8967	−1.3166
C3	0.1958	−0.1718	−1.6125	2.5941	−1.1773

Table 3.1 Predictive control laws with different tuning factors.

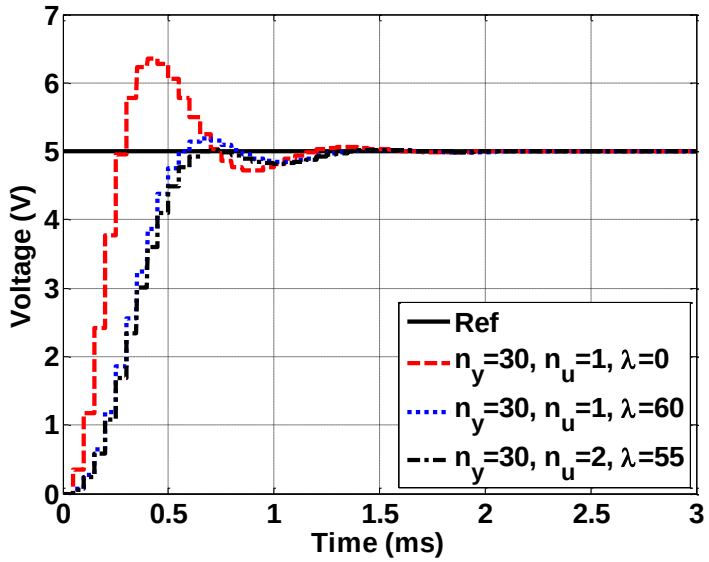


Fig. 3.20 Simulated system responses with predictive controllers.

The simulated step responses of the three controllers, the robust PID, the state feedback controller with integrator and the predictive controller are plotted together in dashed line, dotted line and dash-dotted line respectively in Fig. 3.21. The response with the predictive controller is almost identical to that with the other two controllers, this is because both the PID controller and state feedback controller are ITAE optimised, therefore, the transient response cannot be improved for the same system requirements.

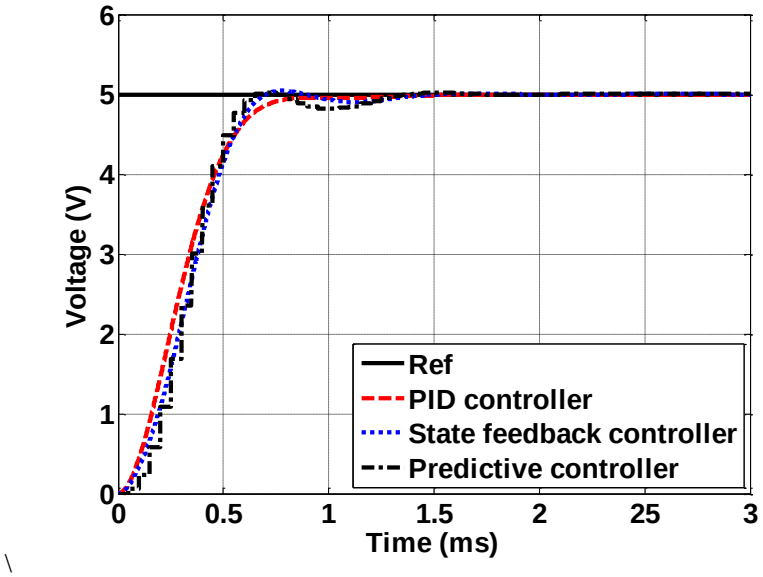
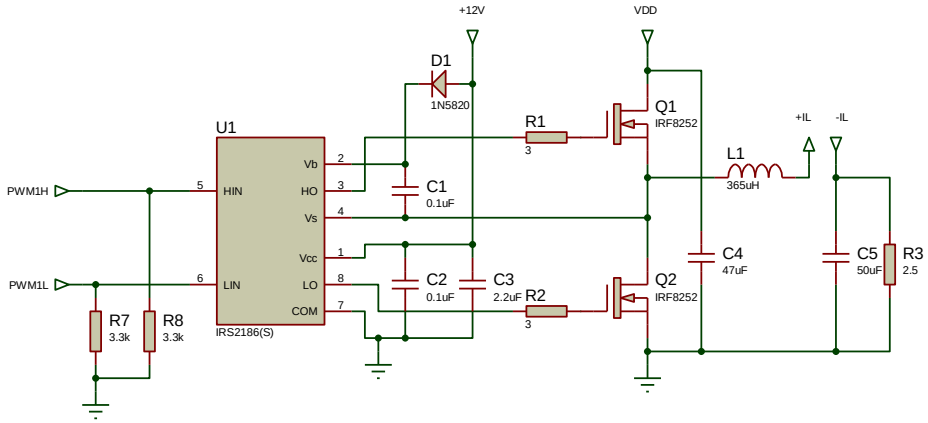


Fig. 3.21 Simulated system step responses with the three controllers.

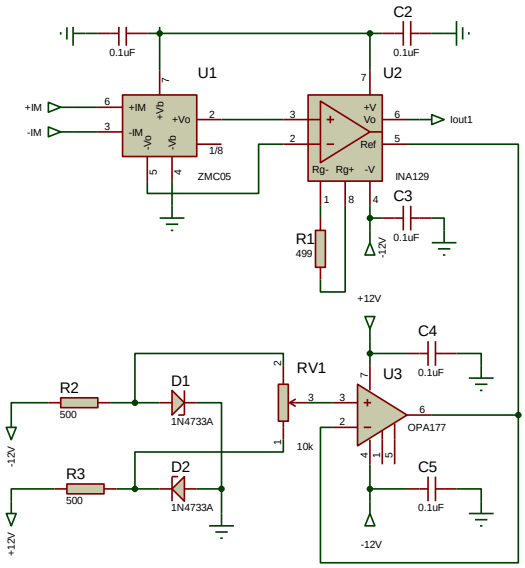
3.5.4. Converter prototype

A prototype SBC was built to validate the simulations presented in the previous sections. It was split into two main functional parts: the converter and microcontroller. The schematic of the converter is shown in Fig. 3.22 (a) containing the two MOSFETs, Q_1 and Q_2, which are selected to be IRF510, the low-pass filter capacitor C_5 and inductor L_1 which is custom built on an RM10 core with 50 turns, and the gate driver IRS2186 which is based on the bootstrap principle [90] where a floating high side drive is obtained with the bootstrap capacitor C_1 as shown in Fig. 3.22 (a). The current sensing circuit in Fig. 3.22 (b) is placed between inductor and capacitor to provide current feedback for the state feedback controller. The current sensing circuit contains the current sensor ZMC05 which measures the magnetic field generated by the current passing through the $+I_{\mathrm{M}}$ and $-I_{\mathrm{M}}$ pins and produces an sense voltage between the $+V_{\mathrm{b}}$ and $-V_{\mathrm{b}}$ which is amplified by an instrumentation amplifier INA129 with its gain set by R_{G} by (3.72) [91]. An op-amp is also included to remove any offset in the instrumentation amplifier.

$$K_g = 1 + \frac{49.4x10^3}{R_g} \tag{3.72}$$



(a)



(b)

Fig. 3.22 Schematic of the prototype converter. (a) synchronous buck converter and (b) current sensing circuit.

The microcontroller dsPIC33FJ16GS502 [92] from Microchip, which has high performance PWMs and ADCs, was selected for the prototype. The configuration of the microcontroller is shown in Fig. 3.23. It is programmed by their low cost programmer PICKIT2 [93] through the

ICSP connection. Pin 28 set the voltage range of the ADC and low-pass filters are included for each channel to reduce the measurement noise.

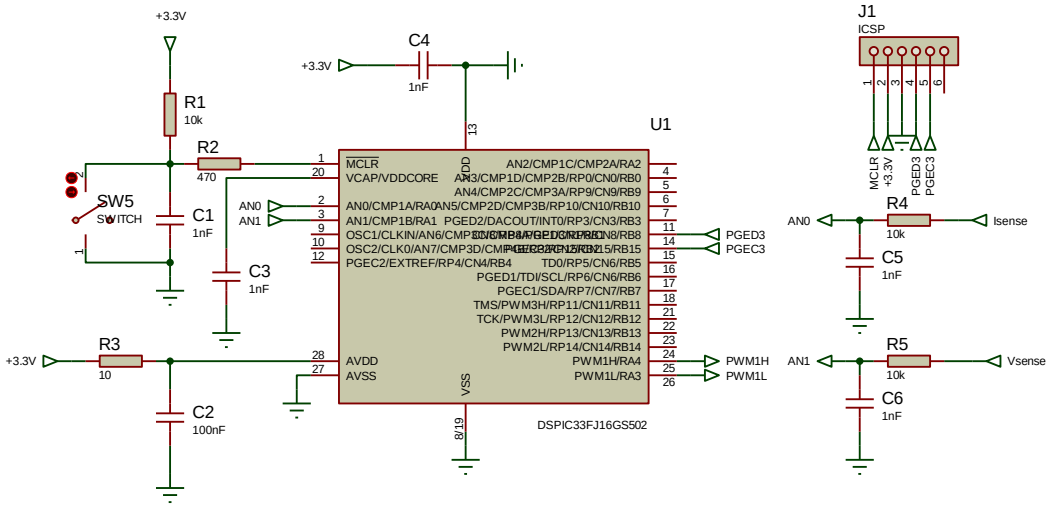


Fig. 3.23 Schematic of the microcontroller in the prototype converter.

The complete circuit is shown in Fig. 3.24:

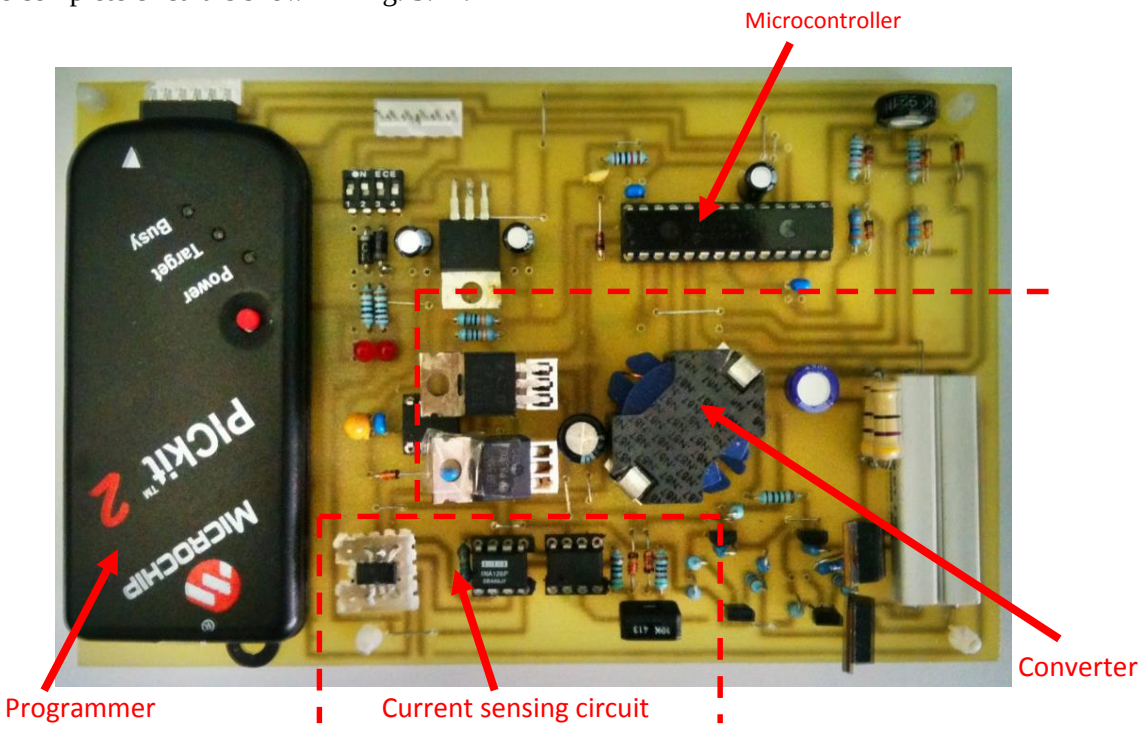


Fig. 3.24 Image of the prototype converter.

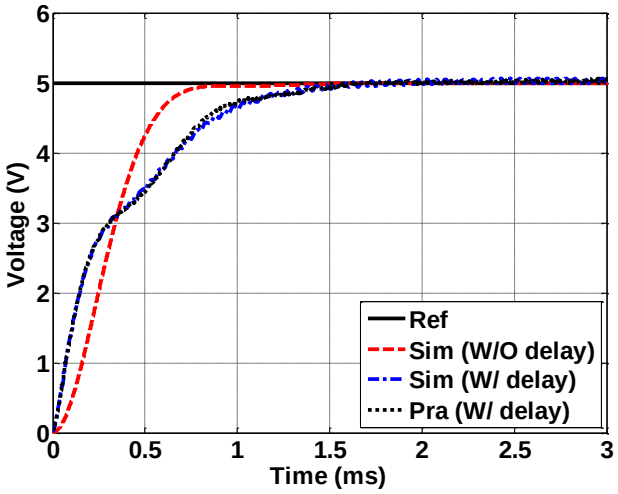
For the practical implementation, the discrete-time control law of the robust PID controller is obtained by (3.60) in (3.73) and of the state feedback controller with (3.61) in (3.74). The predictive controller is already in the incremental form in (3.75):

$$u(k) = u(k-1) + 0.16[10.9e(k) - 18.8e(k-1) + 8.9e(k-2)] \quad (3.73)$$

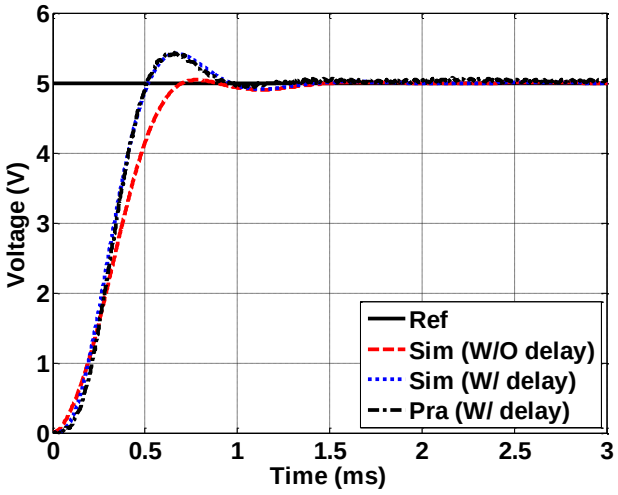
$$u(k) = 1.46x_1(k) - 0.17x_2(k) + 0.17r(k) \quad (3.74)$$

$$u(k) = 0.20r(k) - 0.17u(k-1) - 1.61y(k) + 2.59y(k-1) - 1.18y(k-2) \quad (3.75)$$

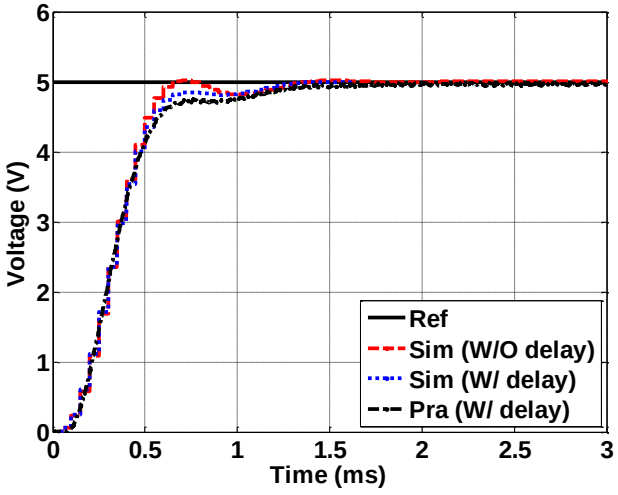
With the switching frequency of the PWM at 20 kHz, the control bandwidth is also limited to 20 kHz (i.e. the duty cycle can only be changed once every cycle). With the different length of time needed for the microcontroller to calculate the above control laws under different operating conditions, the control input is applied at the next cycle, introducing a constant time-delay of 50 μs. With this time delay, the system responses with the three controllers are re-simulated. The system responses with the PID controller, the state feedback controller and the predictive controller without the time delay are shown in dash line in Fig. 3.25 (a), (b) and (c) respectively. Also shown in the figures are the simulated and practical responses with the time delay in the dotted line and dash-dotted line respectively. The practical responses of the system with time delay are in excellent agreement with the simulation.



(a)



(b)



(c)

Fig. 3.25 Simulated and practical system responses. (a) PID controller (b) State feedback controller (c) Predictive controller

The practical result of the three controllers are plotted in Fig. 3.26, showing that different types of controller respond to the time delay differently, with the predictive controller being affected the least.

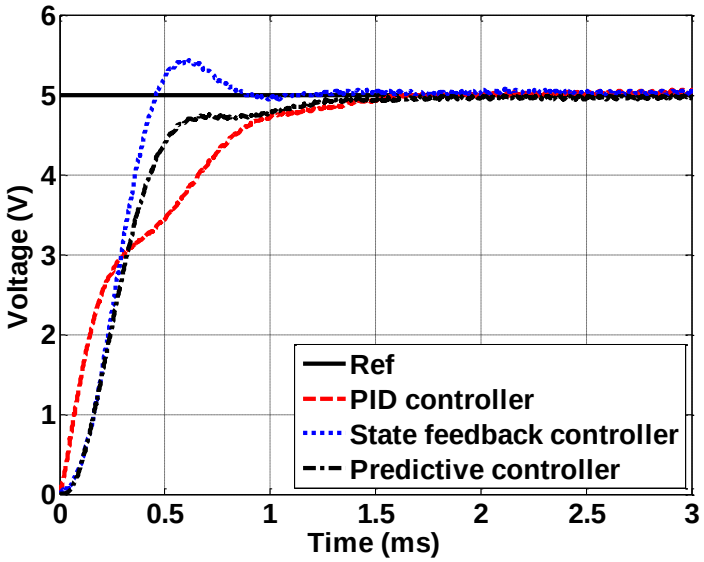


Fig. 3.26 Practical system responses with different controller with time delay.

3.6. Summary

From the steady state operation of synchronous buck converters, the equations defining the required filter inductance and capacitance, and the sets of first-order differential equations for state-space modelling are obtained. From the differential equations, the state-space form of the equivalent circuit model is arrived at through a state-space averaging technique. This equivalent circuit model is converted to the transfer function through the use of a Laplace transform. The closed-loop system configuration is briefly discussed before the details of the robust PID controller, the state feedback controller with integrator and the predictive controller are given. A 5 W converter is designed to allow the step responses with the three controllers to be compared. Before the inclusion of the time delay, simulation results show that the step responses of the converter with the three controllers are almost identical; no major transient performance advantage is gained. When the time delay is included in the simulation, the step responses are

shown being affected differently depending on the type of controller, with the converter with the predictive controller being the least affected. A prototype converter is built and implemented with the three controllers. The measurements from the prototype show excellent agreement with the simulation with and without the time delay.

4. Improvements in transient response with parallel converters

4.1. Introduction

Chapter 3 has shown that the improvement in transient response performance of a synchronous buck converter withdifferent types of linear controller is limited. This chapter investigates the transient performance of a parallel converter (i.e. converter with two parallel connected power modules). A detailed analysis of two control schemes, the fast response double buck (FRDB) [60] and sensorless and peak current mode control (SCM-PCM) [61], presented in the literature is undertaken, from which a new control scheme which combines the high efficiency characteristic of the FRDB and fast transient performance characteristic of the SCM-PCM is proposed. A 25 W (V_o = 5 V, I_o = 5 A) parallel converter is designed and controlled by the proposed scheme. Its transient performance and efficiency are compared with a similar converter implemented with the FRDB and the SCM-PCM schemes to show the advantages of the proposed scheme.

4.2. Circuit configuration and components selection

The parallel converter discussed in this chapter is formed by two parallel connected power modules (PMs), each of which is based on the synchronous buck converter detailed in section 3.2. One power module is called the main PM, while the other called the auxiliary PM as shown in Fig. 4.1. The subscript m and x are used to represent the parameters for the main and auxiliary PM respectively. For example, δ_m is the duty cycle of the main PM while δ_x is the duty cycle of the auxiliary PM.

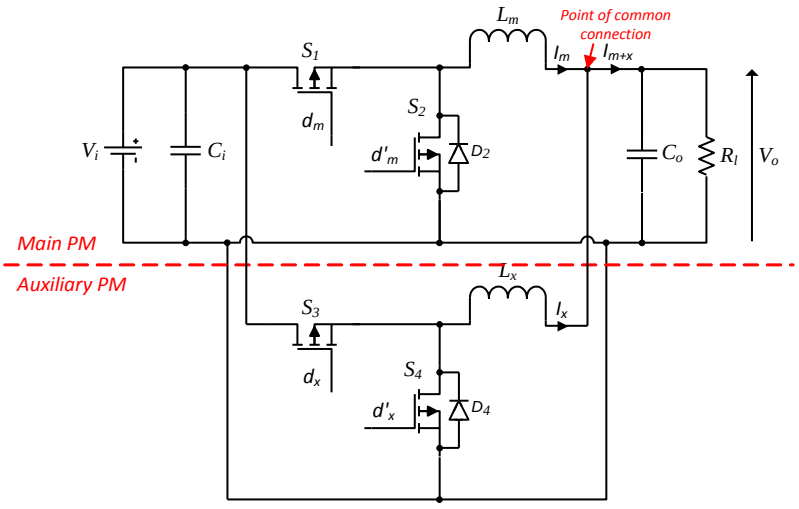


Fig. 4.1 Parallel converter with two parallel connected SBC.

With the two PMs connected in parallel as in Fig. 4.1 (i.e. sharing the same input and output connections), the total rate of change of inductor current $\left((d/dt)I_{m+x}\right)$ at any given instant is simply the sum of the rates of change of the main and auxiliary PMs inductor currents at that instant as in (4.1):

$$\frac{d}{dt}I_{\mathrm{m+x}} = \frac{d}{dt}I_{\mathrm{m}} + \frac{d}{dt}I_{\mathrm{x}} \tag{4.1}$$

Under the maximum load step (increases) or drop (reduction), the duty cycles of both PMs are set to the maximum or minimum respectively to minimise the transient recovery time. Under these conditions, the inductors of the two PMs can be represented by the equivalent inductance, L, which is found by the parallel law as followed:

$$L = \frac{1}{\frac{1}{L_{\mathrm{m}}} + \frac{1}{L_{\mathrm{x}}}} \tag{4.2}$$

Due to the limited rate of change of inductor current, an excess or deficit in charge is provided to the output during the load changes which must be absorbed or released by the output capacitor. Depending on the magnitude of the load step or drop, the capacitance calculated by (3.8) for the

steady state output voltage ripple requirement is often too low to satisfy the voltage overshoot (V_{os}) and undershoot (V_{us}) requirements for the supply. For clarity, the remaining chapter focuses on the load step (increases) case, similar procedures can however be applied for the load drop (reduction).

The typical current and voltage waveforms of a converter subjected to a load step change are shown in Fig. 4.2. At time, t_1, a load current step of magnitude I_s is introduced, the inductor current is temporarily below the new load current level due to the limited rate of change of inductor current, until t_2. The integral of this current is the charge (Q_{us}) responsible for the voltage drop in the capacitor. The total voltage drop, V_{us}, during this period can be found by the charge equation as follows:

$$V_{\mathrm{s}} = \frac{Q_{\mathrm{us}}}{C_{\mathrm{o}}} = \frac{I_s T_p}{2C_{\mathrm{o}}} \tag{4.3}$$

where T_{p} is the time taken for I_{o} to reach the new load current.

With the load current step during the period, $t_1 < t < t_2$, described by (4.4), an expression for the minimum capacitance is obtained by rearranging (4.4) in term of T_{p} and substituting into (4.3), then rearranging in term of C_{o} as in (4.5) [94] (n.b. for load drop, $V_{\mathrm{i}} - V_{\mathrm{o}}$ in (4.5) is replaced by V_{o}):

$$I_s = \frac{(V_{\mathrm{i}} - V_{\mathrm{o}})T_{\mathrm{p}}}{L} \tag{4.4}$$

$$C_{\mathrm{o}} \geq \frac{L{I_{\mathrm{s}}}^2}{2V_{\mathrm{us}}(V_{\mathrm{i}} - V_{\mathrm{o}})} \tag{4.5}$$

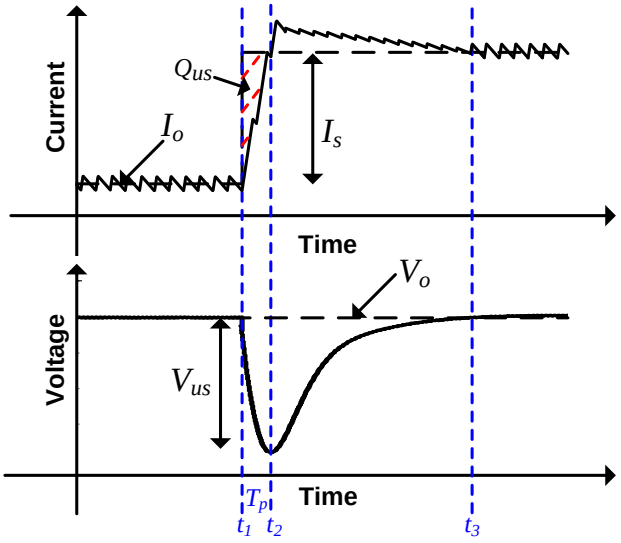


Fig. 4.2 Current and voltage waveforms of converter subjected to load step.

4.3. Control schemes for transient condition

Before giving any detail of the operations of the different control schemes for the parallel converter during the transient condition, the two main control structures employed with the SBC are summarised. The voltage-mode control (VMC) employed in section 3.4 is a single-loop control system where a control signal, v_{co}, is produced by the controller based on the difference between the output voltage feedback and reference signals. The control signal is compared with the saw-tooth signal, v_s, which produces a high signal whenever $v_{co} < v_s$, otherwise a low signal. In current-mode control (CMC), the voltage-loop is used to provide a reference signal, I_{co}, for an inner current-loop which is subsequently used to generate the duty cycle, δ_m, for the MOSFETs without the need of the saw-tooth as in the VMC. A compensation ramp, I_r, as shown in Fig. 4.3 is however needed to prevent sub-harmonic oscillations. A summary of VMC and CMC is provided in [95].

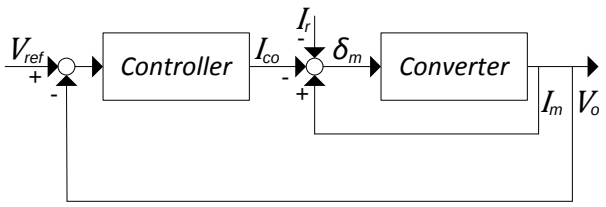


Fig. 4.3 Block diagram of closed-loop current mode control.

The duty-cycle waveform, δ_m, itself can be generated in a number of different ways. In the peak current mode control (PCM) [61], the drive signal remains high until the inductor current signal, I_m, becomes equal to I_{co} minus the compensation ramp signal, after which it is turned off for a fix duration before the next cycle begins as shown in Fig. 4.4.

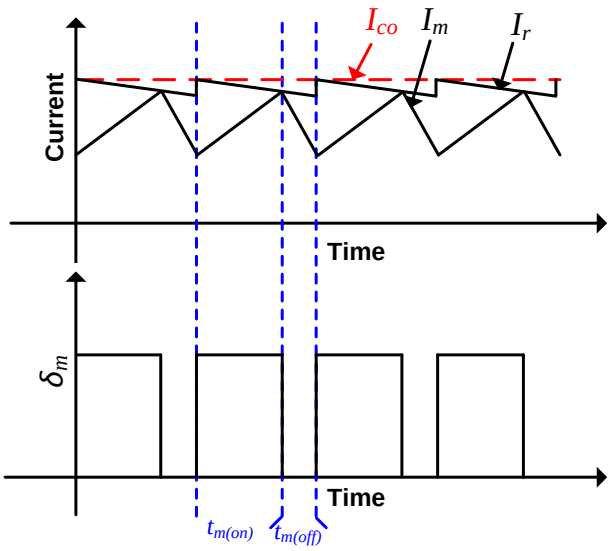


Fig. 4.4 Current mode control current and PWM waveforms.

To reduce the need for an extra current sensor, and the sensitivity of measurement noise as the magnitude current signal is small, the current signal in sensorless current mode (SCM) control [96] is reconstructed by integrating the voltage across the inductor. The blocks dedicated for the current reconstruction, also called the observer, are enclosed in the block diagram of the system with SCM control in Fig. 4.5. The E/D forwards or blocks V_i during the on- and off-period

respectively, to emulate the voltage across the inductor, which is $V_{\mathrm{i}} - V_{\mathrm{o}}$ during the on-period and $-V_{\mathrm{o}}$ during the off-period (n.b. neglecting parasitic resistances).

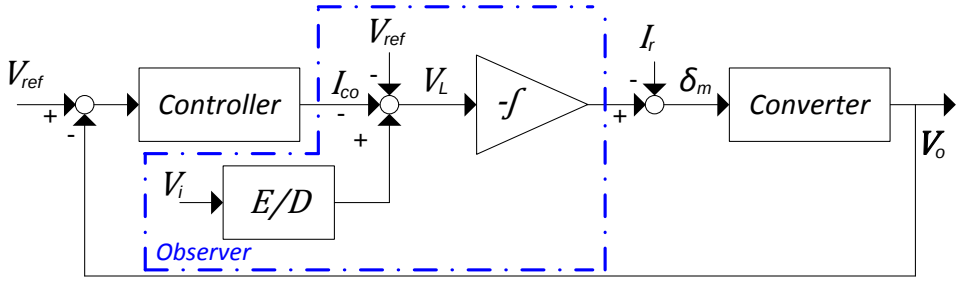


Fig. 4.5 Block diagram of a converter with the SCM control.

Although CMC has been shown to provide superior performance in certain applications it requires an extra feedback loop and can impact on noise and stability. Therefore, for consistency, VMC is employed for the majority of the work presented here with the exception of section 4.3.2 where CMC is employed to implement the SCM-PCM control scheme.

4.3.1. FRDB scheme

In the first control scheme being studied in the chapter, the fast response double buck (FRDB) scheme [60], the main PM remains in operation at all time with its duty cycle, δ_{m}, sets by a linear controller, while the auxiliary PM is only in operation when the output voltage exceeds the threshold voltage, V_{us}, as detected by the threshold logic. The auxiliary PM duty cycle, δ_{x}, is set by a non-linear controller (hysteretic control) [97] which generates a high or low drive signal whenever the output voltage exceeds the hysteresis band ($\pm\Delta$) as shown in Fig. 4.6. The threshold logic produces two signals, the signal 'E/D' enables or disables the auxiliary PM while the signal 'Sat' saturates the main PM linear controller. The block diagram of the converter with the FRDB scheme is shown in Fig. 4.7.

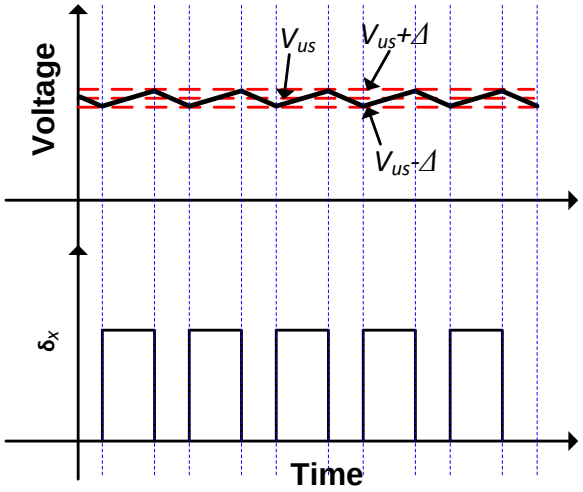


Fig. 4.6 Auxiliary PM with nonlinear hysteretic control.

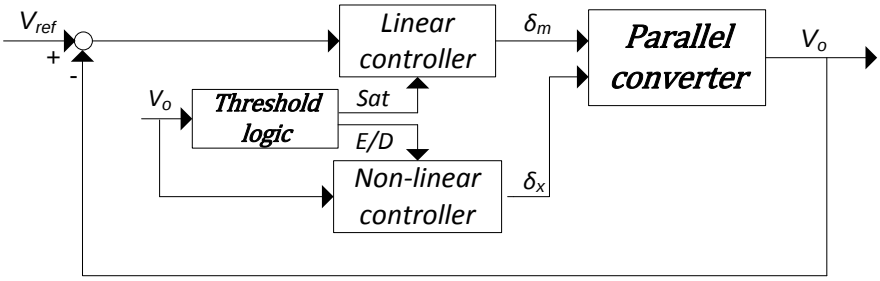


Fig. 4.7 Block diagram of the converter with FRDB.

Under steady-state operation, the output voltage is within the undershoot threshold level, $V_{\rm us}$, and so the auxiliary PM is disabled. $V_{\rm o}$ is regulated by the main PM as in the standard SBC in previous chapter. A load step applied at time t_1 in Fig. 4.8, causes the output voltage to drop. With a large enough load step, the voltage drop exceeds the threshold voltage at time t_2, the threshold logic carry out the following two actions: 1) saturate the main PM duty cycle (i.e. $\delta_{\rm m} = 1$) to allow its current to recover at the maximum rate, and 2) enable the auxiliary PM to provide any extra charge needed to keep the voltage within the $V_{\rm us} \pm \Delta$. At time t_3, the main PM current has reached a level where it alone can maintains the output voltage within the threshold level, the main PM control input is unsaturated and the auxiliary PM is disabled. The transient response ends as soon as the output voltage reaches the set-point at time t_4, with a similar response to the standard SBC, the auxiliary PM has no effect on the settling time. The duration over which the main PM is saturated

and the auxiliary PM enabled are shown in Fig. 4.8. The main PM is designed as in the standard SBC, while the auxiliary PM is designed to have high rate of change of inductor current (i.e. low inductance) in order to keep the V_o within $V_{us} \pm \Delta$.

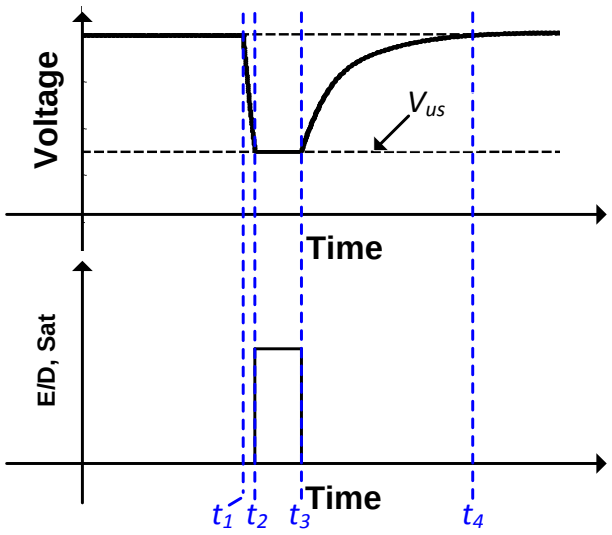


Fig. 4.8 Voltage waveform and auxiliary PM timing diagram with FRDB.

4.3.2. SCM-PCM scheme

In the second control scheme being studied in this chapter, the sensorless and peak current mode (SCM-PCM) scheme [61], both PMs remain in operation at all times. The main PM duty cycle is set by the PCM but without the outer voltage loop. The current loop reference, I_{co}, is set equal to the load current I_m. The auxiliary PM duty cycle is set by the SCM scheme. The block diagram of the converter with SCM-PCM scheme is shown in Fig. 4.9.

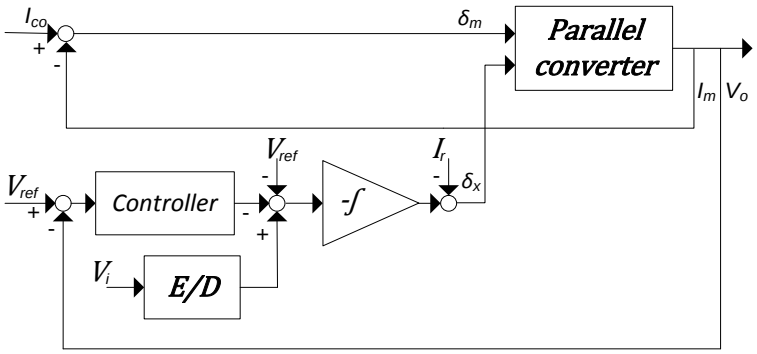


Fig. 4.9 Block diagram of the converter with SCM-PCM.

Under steady-state condition, I_{m} matches the load demand, the auxiliary PM sees no voltage error, injecting an average current of zero. When the load demand is suddenly increased, time t_1 in Fig. 4.10, the output voltage drops due to the deficit in charge as I_{m} is rising to the new load demand. The auxiliary PM sees the voltage drop and starts providing the extra charge required to bring the output voltage back to its steady-sate value. At time t_2, while the main PM current is still recovering to the new demand, the extra charge from the auxiliary PM has brought the output voltage back to the steady-state level. The transient response as perceived at the output ends here. After time t_2, the main PM current continuous to rise to the new level, the charge required by the auxiliary PM to keep the output voltage at the set-point is reduced. At time t_3, I_{m} has settled to the new load demand and I_{x} has returned to the average of zero and this is the instant where the converter's actual response to the transient event is complete. The main and auxiliary PMs are designed such that their equivalent inductor, L, and capacitor together prevent the threshold voltage to be exceeded under the maximum rated load step.

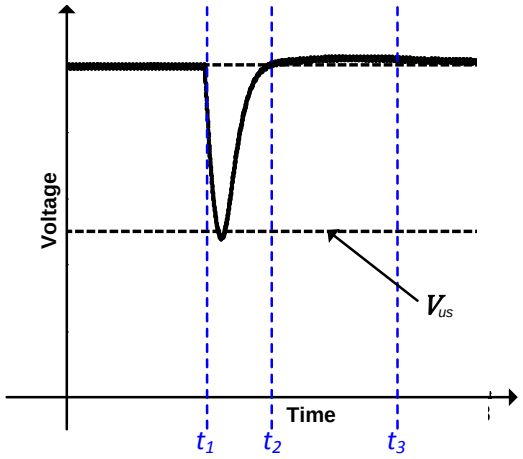


Fig. 4.10 Voltage waveform with SCM-PCM.

4.3.3. Proposed FRHE scheme

In the FRDB scheme, the auxiliary PM only operates when the main PM is unable to sustain the output voltage within the undershoot voltage threshold level and so the extra bandwidth available in the auxiliary PM is not exploited. In the SCM-PCM scheme, the auxiliary PM remains in operation at all time and so the wide bandwidth of the auxiliary PM is fully exploited. However, since the efficiency of the auxiliary PM is lower than the main PM due to its higher operating frequency (more detail will be given in chapter 5 and 6), the continual operation of the auxiliary PM leads to lower system efficiency in transient conditions in comparison to the FRDB scheme. A new scheme, the fast recovery with high transient efficiency (FRHE) scheme, which combining the advantages of the FRDB and SCM-PCM schemes, is proposed in this section to achieve the compromise between the transient performance and efficiency.

In the proposed (FRHE) scheme, the main PM remains in operation at all time to regulate the output voltage. In order to prevent current diversion through the auxiliary PM (during the transient condition), the V_o is regulated indirectly through I_m with its reference, I_{ref}, obtained through Ohm's law (i.e. $I_{ref} = V_{ref}/R_l$ where R_l is given in this work). The operation of the auxiliary PM is similar to the FRDB scheme, which is enabled to prevent the threshold voltage from being exceeded. However, instead of having the threshold logic which demands the auxiliary PM

inductance to be low, it is replaced by the load detection block which enables the auxiliary PM when a specific load change is exceeded. In order to shape both the transient and steady-state responses as in the SCM-PCM scheme, two PID controllers, PID_{m} and PID_{x}, are required. The block diagram of the converter with the proposed scheme is shown in Fig. 4.11.

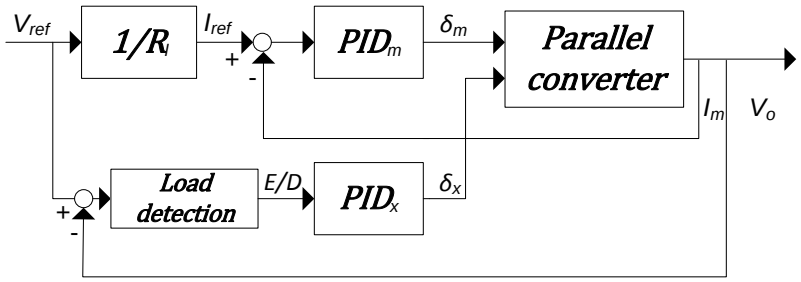


Fig. 4.11 Block diagram of the converter with the proposed control scheme.

Under steady-state conditions or with a small load steps, the load detection block disables the auxiliary PM, the output voltage is regulated by the main PM alone as in the FRDB scheme. With a large enough load step, the main PM alone is unable to prevent the threshold voltage from being exceeded and so, the load detection block enables the auxiliary PM to provide the extra current required to bring the output to the set-point with the minimum time as in the SCM-PCM scheme. The transient response under the maximum load step is identical to that in the SCM-PCM, that is, the transient response starts at time t_1, and perceived to end by the output at time t_2 while the actual converter's response to the transient event ends at time t_3 as shown in Fig. 4.12. The interval for which the auxiliary PM is active is defined as T_{p} in Fig. 4.12. In the case where the auxiliary is enabled only once the threshold voltage is exceeded, the on-duration is reduced only slightly to T_{p1}. The main and auxiliary PMs are designed as in the SCM-PCM scheme, where their equivalent inductance and capacitor are selected to prevent the threshold voltage from being exceeded under the maximum load step.

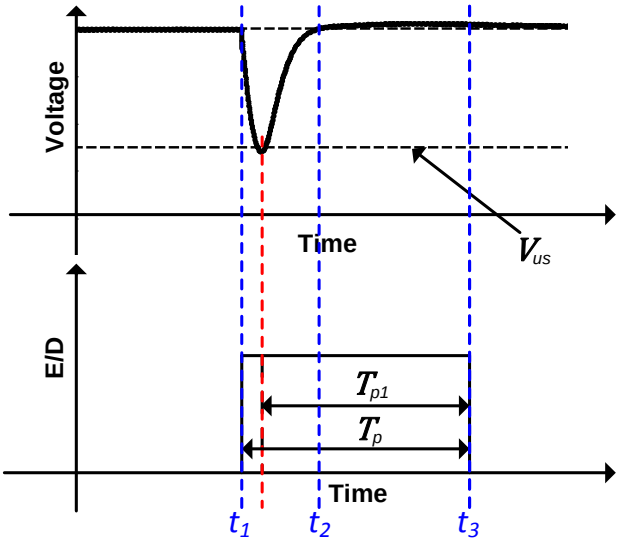


Fig. 4.12 Voltage waveform and auxiliary PM timing diagram with the proposed scheme.

4.4. Controller design

In section 3.4.2, each of the PID controllers investigated contained the proportional gain K_P, the integral gain K_I and the derivative gain K_D, which were found using the set of ITAE optimised coefficients. This is not possible for the multi-input single-output converters described in this chapter due to the interaction between the two inputs. The controller parameters are instead found using the genetic algorithm (GA) [98], which searches for an optimum solution through a process akin to evolution, allowing an optimal solution to be identified irrespective of the interaction of the system's inputs. Genetic algorithms are inspired by natural selection processes and use the evaluation of a cost function across a population. The population evolves over many generations and converges to optimum solutions for the problem. GA typically uses the following three main operators:

- Selection: retain the best solutions for the next generation, which are to be improved by the following two operators.

- Crossover: two solutions are combined together to extract the best parts in each of the two solutions.

- Mutation: part of a solution is changed randomly, in the hope that the change provides a new and better solution.

Apart from these three operators, the number of solutions in each generation and number of generations can also affect the identified solution.

The GA controller parameter tuning starts by generating the first generation of random candidate solutions (each candidate contains the parameters of the two PID controllers) within the search spaces (i.e. range of K_P, K_I, and K_D). Each of these solutions is then applied to the converter. Thereafter, performance is measured in order to identify the promising solutions for further refinement through the crossover and mutation in the next generation. This refinement process is continued until the performance of the solution shows no meaningful improvement with each generation. The whole GA tuning process is summarised in the flow chart in Fig. 4.13.

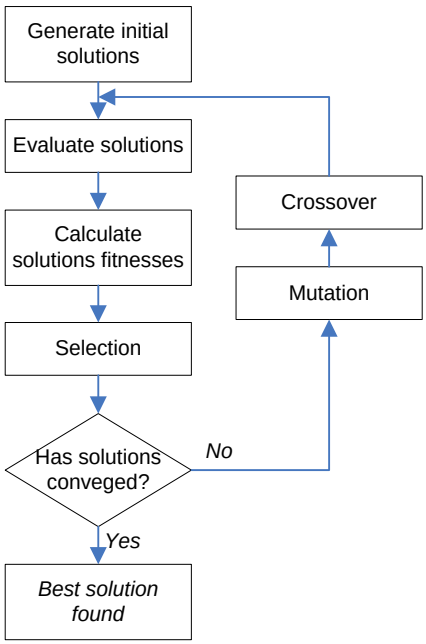


Fig. 4.13 Flow chart of the GA tuning process.

In order for the GA to know which sets of solutions (PIDs) produce a good performance, a quantitative measure of each response, as described in section 3.4.1, is required. For this measure,

the converter is subjected to repeat load step and drop, the transient responses from each of these changes in load conditions cause the measurable errors in the two PMs which are measured by the ITAE performance index (see section 3.4.1). The combined errors (ITAE score) of the two PMs accumulated over numbers of the load changes to allow the best controllers, with the minimum errors, to be identified.

4.5. Design example and experimental results

To demonstrate the difference in transient response and efficiency of the converter with the proposed control scheme over the FRDB and SCM-PCM schemes, a 25 W (V_o = 5 V, I_o = 5 A) parallel connected SBCs has been designed and built. The maximum current step I_s is 4 A, the current ripple ΔI_m is 0.5 A and the maximum undershoot V_{us} is 0.25 V.

Following the design procedure outlined in [61], the switching frequency of the main PM, f_{sm}, that produces the highest efficiency is 40 kHz. In this work, the switching frequency of the auxiliary PM, f_{sx}, is selected to be five times that of the main PM at 200 kHz. With these switching frequencies, the filter inductors of the main and auxiliary PMs are calculated by (3.7) to be $L_m \geq$ 146 µH and $L_x \geq$ 29 µH respectively. With the equivalent inductance of the two PMs calculated by (4.2) to be 24 µH, the filter capacitor C_o is calculated by (4.5) to be 620 µF. The two practical inductors and capacitor used are: L_m =172 µH, L_x = 31µH and C_o = 660 µF.

A converter with the component values defined as above and with the closed-loop configuration in Fig. 4.11 is simulated in a Matlab/Simulink with the 'SimPowerSystems' toolbox as shown in Fig. 4.14. The derivative gain of the main PM, K_{Dm}, is set to zero in order to reduce the need of computation power and susceptibility to noise. This is justified as this power module does not required tight control.

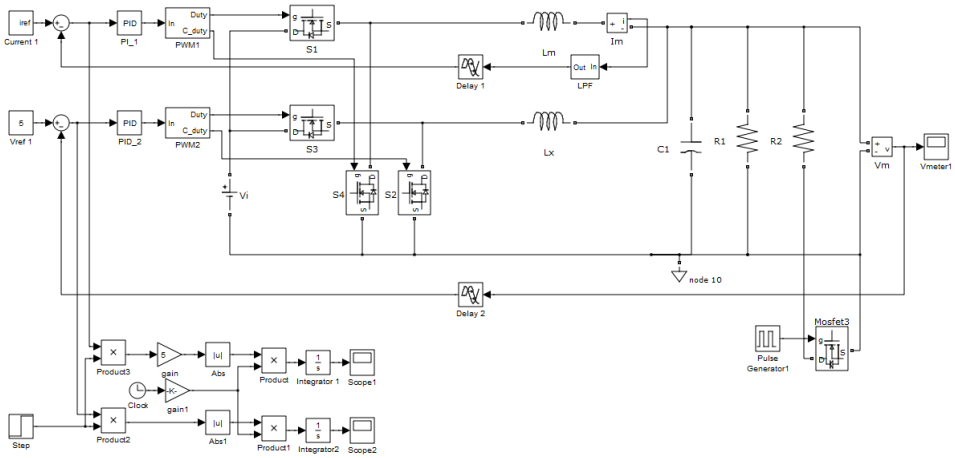


Fig. 4.14 Simulink model of the converter with the proposed control schemes.

The GA tuning in Fig. 4.13 is implemented by the 'Genetic Algorithm toolbox for use with Matlab' [99], with one hundred population (solutions) and a maximum of 20 generations. The parameters of the PID controllers are found with the following values:

$$PID_{\mathrm{m}}: \qquad K_{\mathrm{Pm}}(s) = 0.1, K_{\mathrm{Im}}(s) = 78, K_{\mathrm{Dm}}(s) = 0 \tag{4.6}$$

$$PID_{\mathrm{x}}: \qquad K_{\mathrm{Px}}(s) = 0.2, K_{\mathrm{Ix}}(s) = 312, K_{\mathrm{Dx}}(s) = 5x10^{-5} \tag{4.7}$$

4.5.1. Settling time and on-duration characteristics

With the PID controllers defined as above and under the maximum load step of 4 A, the settling time (to within ±2% of the set-point value) of the converter with the auxiliary PM disabled (i.e. standard SBC and FRDB) is 510 μs as shown in dotted-line in Fig. 4.15. The settling time of the converter with the auxiliary PM enabled (i.e. the proposed FRHE scheme and the SCM-PCM) is reduced to 230 μs as shown in dashed-line in the same figure. This represents a reduction of more than a factor of two.

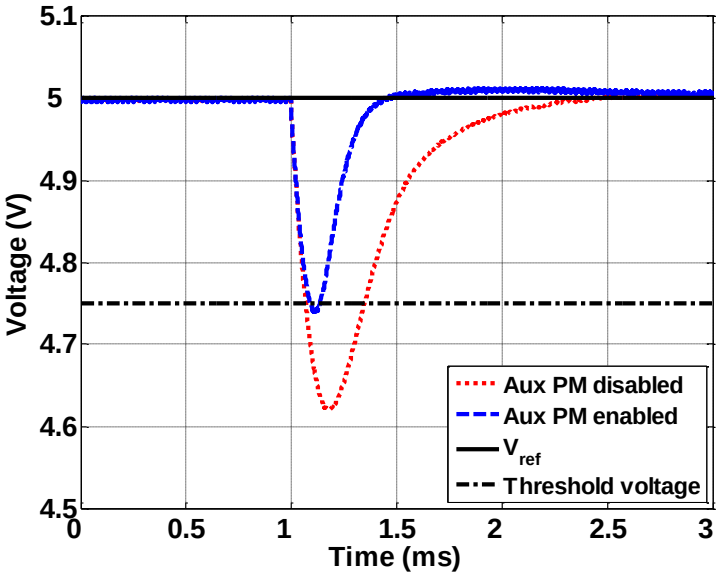


Fig. 4.15 Simulated transient responses with auxiliary PM enabled and disabled.

As the magnitude of the load step reduces, the settling time under all schemes reduces as shown in Fig. 4.16. With the auxiliary PM disabled, the settling times of the standard SBC (and FRDB) is shown in the crossed-line in Fig. 4.16 (n.b. for I_s < 1.8 A, the voltage undershoot stays within the ±2% set-point and is recorded as zero). With the auxiliary PM enabled, the settling time of the proposed scheme (and SCM-PCM) is shown in the triangle-line in the same figure. In order to guarantee the settling time that can be achieved by the converter (i.e. 230 μs) under the maximum load step, the auxiliary PM must be enabled for load step > 2.4 A. The voltage undershoot at this load step (i.e. 2.4 A) is 4.85 V, within the threshold voltage of 4.75 V.

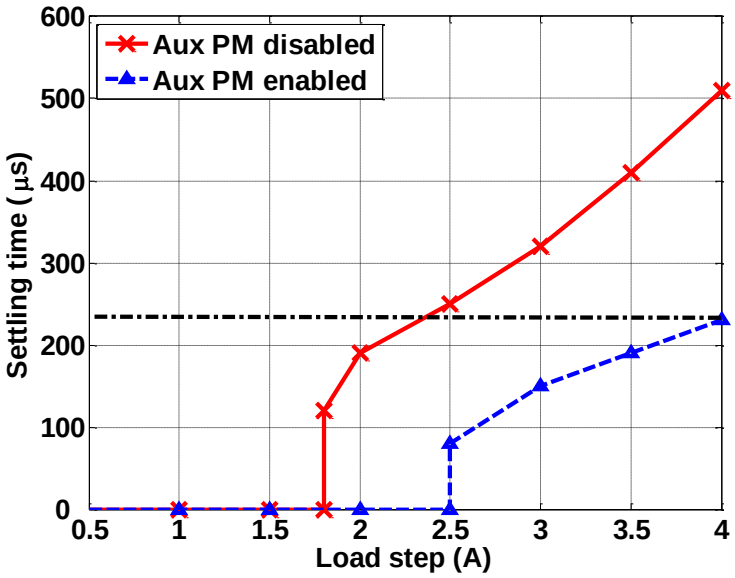


Fig. 4.16 Converter settling times with the auxiliary PM enabled and disabled.

The on-duration of the auxiliary PM under the different load step change and control schemes are shown in Fig. 4.17. The auxiliary PM is always off in the standard buck converter and is always on in the SCM-PCM scheme for 1.5 ms. In the proposed scheme, in order to guarantee the settling time of ≤ 230 µs the auxiliary PM is enabled when I_s > 2.4 A, otherwise disabled. The efficiency of the converter with the different on-duration with the schemes will be detailed shortly.

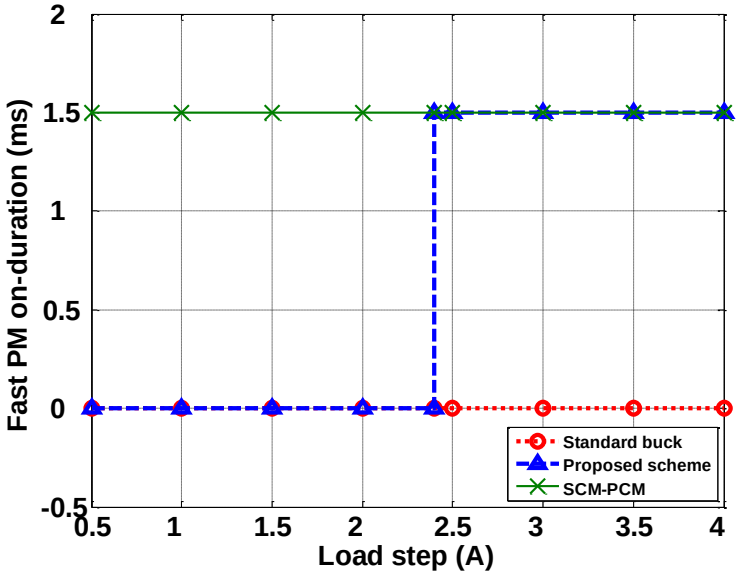


Fig. 4.17 On-duration of the auxiliary PM with the different control schemes.

4.5.2. Converter prototype

A prototype converter is built in Fig. 4.18 to validate the improvements in settling time and, moreover, to determine the improvements in efficiency with the proposed scheme. Both inductors are custom made, with the L_m built on RM14 core with 18 turns and L_x built on RM10 core with 8 turns. An International Rectifier IRS2186 provides the high and low-side gate drives, the current sensing circuit with the shunt current monitor AD8512 from Analog Devices and the control board with the microcontroller dsPIC33FJ16GS502 from Microchip and ICD3 [100] programmer as shown in Fig. 4.19 are built on external circuit boards.

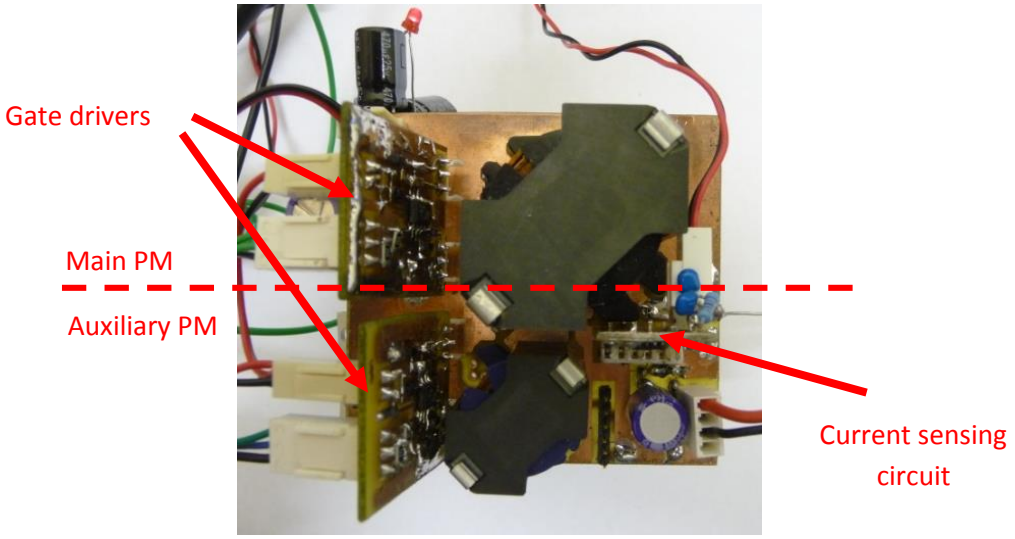


Fig. 4.18 Image of the prototype converter.

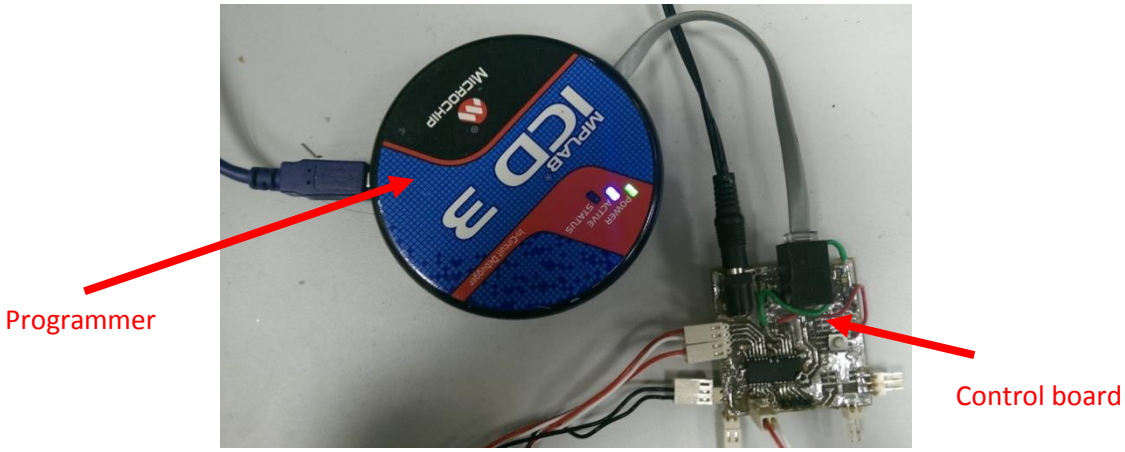


Fig. 4.19 Image of the control board and programmer.

The parameters of the two PID controllers in (4.6) and (4.7) are converted to the discrete-time PID control laws by Euler's method in (3.60) to (4.8) and (4.9) respectively. These two control laws are implemented in the microcontroller.

$$PID_{\mathrm{md}}: \qquad u[k] = u[k-1] + 0.1\big[e[k] - e[k-1]\big] \tag{4.8}$$

$$PID_{\mathrm{xd}}: \qquad u[k] = u[k-1] + 0.2\big[51e[k] - 101e[k-1] + 50e[k-2]\big] \tag{4.9}$$

The transient responses of the standard SBC and converter with the proposed control scheme subjected to the maximum load steps are shown in Fig. 4.20. The responses matches that predicted in the simulation, confirming the two fold improvement in settling time over the FRDB under the maximum load step.

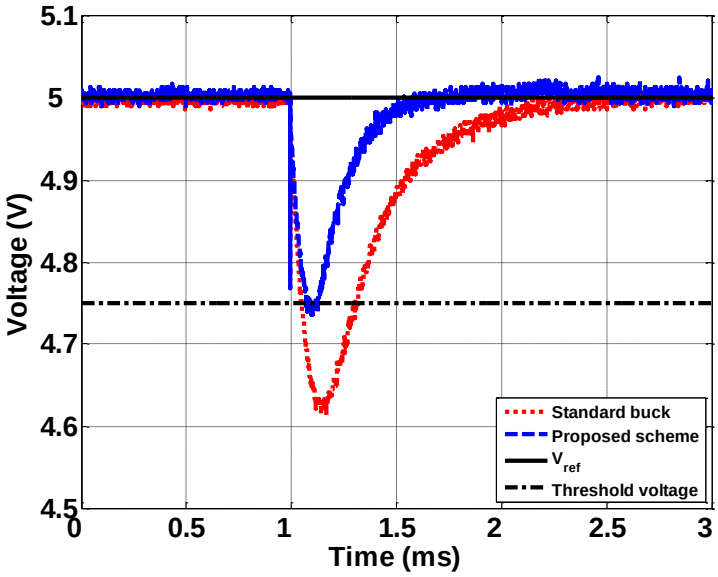


Fig. 4.20 Practical transient responses under different schemes.

In order to measure the efficiency improvement with the proposed scheme, the converter is subject to repeat load step and drop of 4 A in a 1.5 ms interval. Fig. 4.21 shows the efficiency of the converter measured by a bespoke calorimeter detailed in Appendix C. The crossed-line shows the efficiency is improved by up to 4.7% with I_s = 0.5 A over the SCM-PCM (triangle-line).

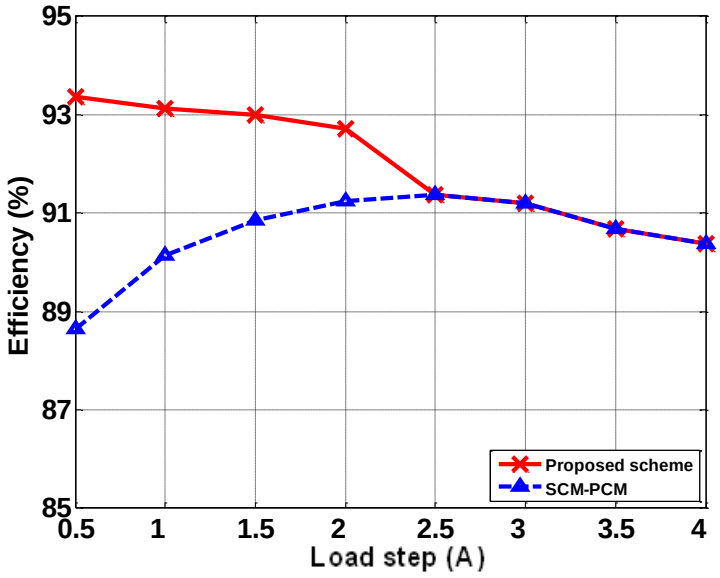


Fig. 4.21 Practical converter efficiency under different schemes.

4.6. Summary

The minimum inductance and capacitance required to satisfy the undershoot requirement are identified through the converter operation under load step change. From a detailed analysis of the FRDB and SCM-PCM schemes which were developed to improve the converter's transient performance, a new scheme (FRHE) which combines the high efficiency characteristic of the FRDB and the good transient response of the SCM-PCM is proposed. This proposed scheme enables the auxiliary PM when a load step is large enough to cause the voltage undershoot or settling time to be exceeded. Two PID controllers with parameters obtained by a GA are utilised in the proposed scheme to shape both the steady-state and transient responses. A 25 W, two PMs, parallel connected converter was designed and built in order to show the settling time and efficiency improvement of the proposed scheme. Simulation shows that under the full load step, the settling time with the proposed scheme is a factor of two shorter then that with the standard SBC and FRDB scheme. This is validated in the prototype, showing a good agreement between the two set of results. The efficiency with the proposed scheme is measured in the prototype, for $I_s < 2.4$ A is improved by up to 4.7% in comparison with the SCM-PCM. This scheme is particular suitable for application where its load are constantly changing (e.g. VR).

5. Improvements in steady-state efficiency with parallel connected converters

5.1. Introduction

The previous chapter has shown that both shorter settling time and higher efficiency can be achieved by enabling the auxiliary power module (PM) during a load step transient event that would otherwise have led to the output voltage contravening the undershoot voltage design specification requirement. In this chapter the improvements in steady-state operating efficiency facilitated by the parallel converter is examined and a new design procedure, the high steady-state efficiency (HSSE) design technique, is proposed for a converter featuring two parallel connected PMs. From a detailed investigation of the operation of a two-switch forward converter, and by analysing the division of work between the two PMs, the HSSE design technique is derived to allow higher steady-state efficiency to be achieved with the parallel converter. Following a component loss analysis, two 360 W (V_o = 24 V, I_o = 15 A) converters are designed and built to demonstrate the efficiency improvement using the proposed HSSE technique over that of an interleaved converter. Detailed simulation and experimental studies highlight the advantages of the proposed method.

5.2. Two-switch forward converter (2SFC)

Before describing the parallel converter with the proposed design technique, the circuit configuration and operating characteristics of the two-switch forward converter (2SFC) will first be reviewed. The primary reason of selecting the 2SFC over the SBC is that this converter contains an extra transformer that provides a greater degree of freedom over the choice of the circuit parameters during the design phase.

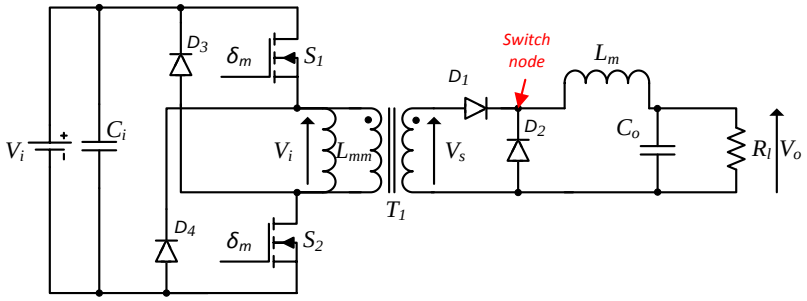


Fig. 5.1 Circuit diagram of two-switch forward converter (2SFC).

The circuit diagram of a 2SFC is shown in Fig. 5.1, containing three main sections:

(i) a DC chopper formed by two MOSFETs, S_1 and S_2, that are used to control power flow from the input to the output and two freewheeling diodes, D_1 and D_2, that allow the pseudo AC waveform to be formed at the switch-node

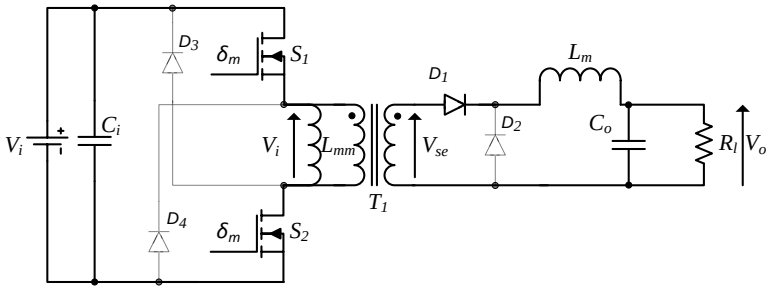
(ii) a transformer, T_1, that provides galvanic isolation and also allows the input voltage to be scaled according to the output voltage requirement, and the two demagnetising diodes, D_3 and D_4, allow the transformer core flux to be reset during the MOSFETs' off-period

(iii) a LC low-pass filter, L_m and C_o, that attenuates the higher harmonic components present in the switch-node voltage to produce a DC output.

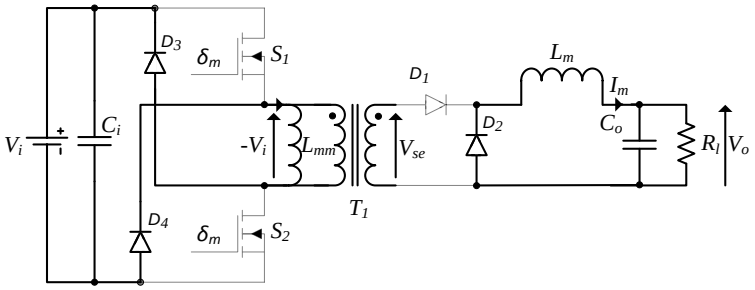
5.2.1. Circuit operation

The 2SFC can operate in both the continuous conduction mode (CCM) or discontinuous conduction mode (DCM) as characterised by current flow through the filter inductor L_m. In the case of CCM, two distinct periods (the on and off-periods) are observed within a single cycle whereas for DCM, an extra period (the cut-off period (t_cf)) is also observed. During the on-period the two MOSFETs are switched on, thus a voltage, V_se, equal to nV_i is induced in the transformer secondary winding. This voltage forward biases diode D_1 and reverse biases diode D_2 as shown in Fig. 5.2 (a), allowing power to be transferred to the load as well as charging the inductor, L_m, with energy. The magnetising inductance, L_mm, is also charged by V_i in this period.

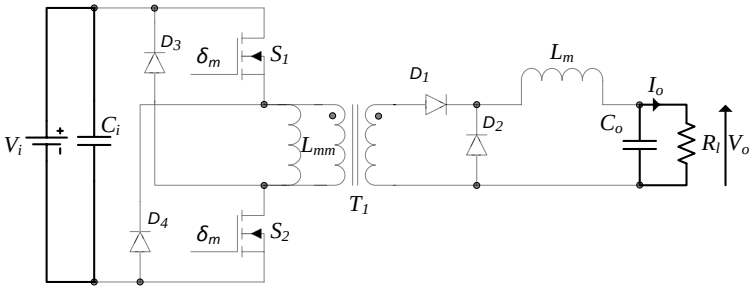
During the off-period, the two MOSFETs are switched off, the diode D_1 is reverse biased while the diode D_2 is freewheeling. The energy stored in the inductor L_{m} is transferred to the output capacitor and the load as shown in Fig. 5.2 (b). The energy stored in the magnetising inductor is also released, and to maintain its current flow, the freewheeling diodes D_3 and D_4, are forced into conduction, allowing the magnetising current to be circulated back to the source. With the magnetising inductance clamped to $-V_{\mathrm{i}}$, discharging at the opposite rate to that during charging in the on-period, the duty cycle must be lower than 50% to ensure the transformer core flux is reset after each cycle.



(a)



(b)



(c)

Fig. 5.2 Circuit diagrams of a parallel converter with two parallel connected 2SFC. (a) on-period (b) off-period (c) cut-off period

If the inductor current falls to zero (i.e. the filter inductor releases all its energy) before the next cycle, the converter enters DCM operation as indicated by the cut-off period, t_{cf}, where the filter inductor current is zero since D_2 is reversed bias and thus energy is supplied to the load by filter capacitor alone, Fig. 5.3. The load is fully supported by the output capacitor as shown in Fig. 5.2 (c).

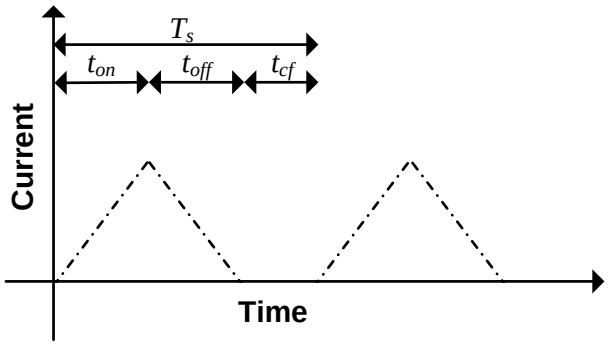


Fig. 5.3 Inductor current waveform in DCM.

The two power modules of the parallel connected converter discussed in this chapter are formed by combining two 2SFCs as shown in Fig. 5.4. As in the previous chapter, one power module is again called the main PM while the other called the auxiliary PM. The utilisation of each PM is determined by the load condition which will be detailed in section 5.3.1.

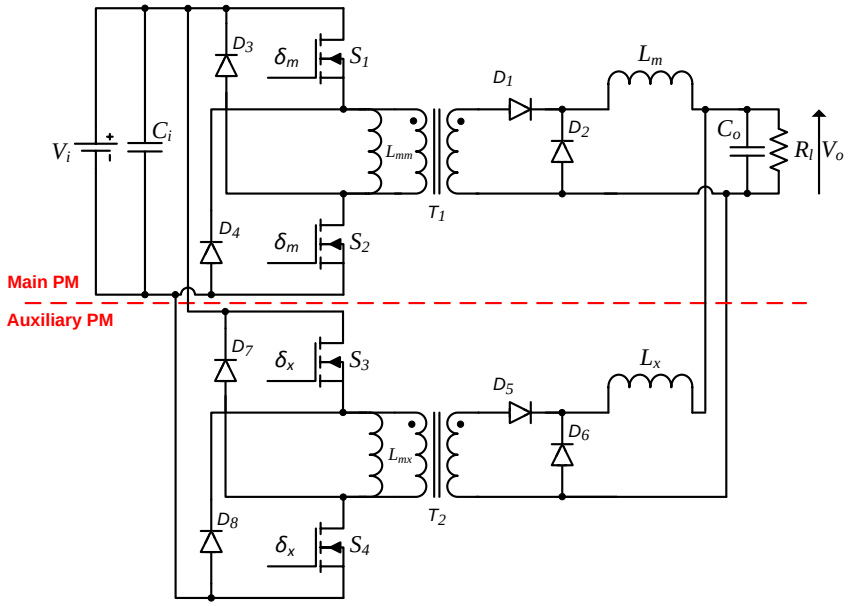


Fig. 5.4 Parallel connected two-switch forward converters.

5.3. Design techniques for parallel converter

For a converter with a single PM (i.e. a standard 2SFC), the only design variable in (3.7) and (3.8) that is not constrained by the system requirements is the switching frequency. Since both the switching frequency, f_{sm}, and the bandwidth (BW) [2] in (5.1) are inversely proportional to L (n.b. L is the equivalent inductor of the two PMs as calculated by 4.2) and C_{o}, f_{sm} must be high in order to achieve a high BW. As the switching losses of the inductor, the transformer and the MOSFETs increase proportionally to the switching frequency (see (5.3), (5.4) and (5.6)), high efficiency is not easily achievable in the standard converter with a high BW requirement.

$$BW = \frac{1}{2\pi\sqrt{LC_{\mathrm{o}}}} \tag{5.1}$$

- ***Parallel converter with non-identical power module***

The parallel converter described in the previous chapter [62] shares the system requirements between the two non-identical PMs (i.e. allocating the BW or transient requirement to the auxiliary PM) which allows the main PM to operate at a much lower switching frequency f_{sm} and so be optimised for conduction losses to achieve higher efficiency.

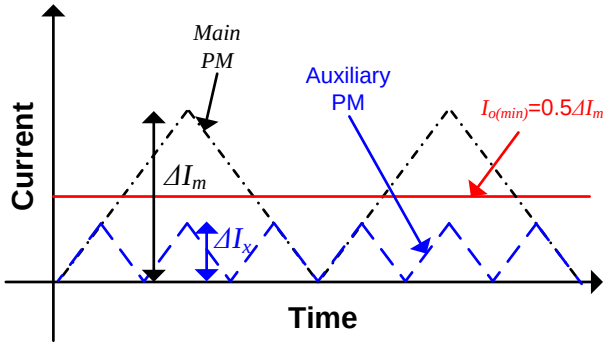
- ***Parallel converter with identical power module***

A more popular design approach is adopted in the interleaved converter [58], where the system requirements are shared equally between identical PMs. Under heavy load condition, all PMs (or phases) are activated to share the load current, to reduce the dominated conduction losses from ${I_{\mathrm{o}}}^2 R_{\mathrm{l}}$ to $m_{\mathrm{n}}(I_{\mathrm{o}}/m_{\mathrm{n}})^2 R_{\mathrm{l}}$ where m_{n} is the number of phases (PM) connected in parallel. Under light load condition, all PMs except one can be disabled as in the phase shedding technique [19], to reduce the dominated switching losses by m_{n}.

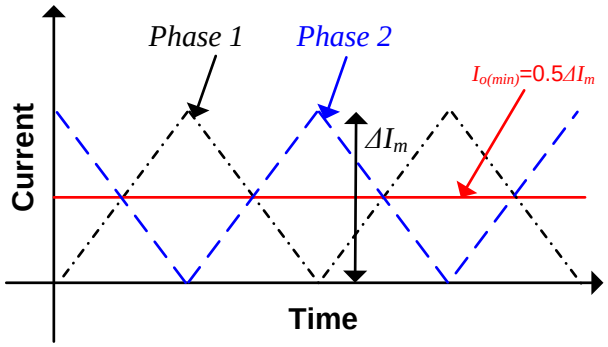
5.3.1. Proposed (HSSE) design technique

In the parallel converter with either non-identical or identical PMs, the current ripple must be less than twice the minimum load current $(I_{o(min)})$ (5.2) in order to stay in the CCM as shown in Fig. 5.5 (a) and (b) respectively [58][62]. With the current ripple described by (3.6) and a given main PM inductance, L_m, a minimum switching frequency must be selected which constrains the maximum achievable efficiency (n.b. L_m of the interleaved converter is constrained by the BW / transient requirement).

$$I_{o(min)} \geq \frac{1}{2}\Delta I_m \tag{5.2}$$



(a)



(b)

Fig. 5.5 Current waveforms of the parallel converter. (a) non-identical PM (b) identical PM

To overcome the above constraint, a new design technique, the high steady-state efficiency (HSSE) design technique, is proposed for a parallel converter with two non-identical PMs. Using the HSSE design technique, both the BW requirement and the minimum load conditions are allocated to the auxiliary PM, allowing a larger main PM current ripple ΔI_{m} (with respect to the $I_{\mathrm{o(min)}}$) and a lower main PM switching frequency f_{sm} to be selected as shown in Fig. 5.6.

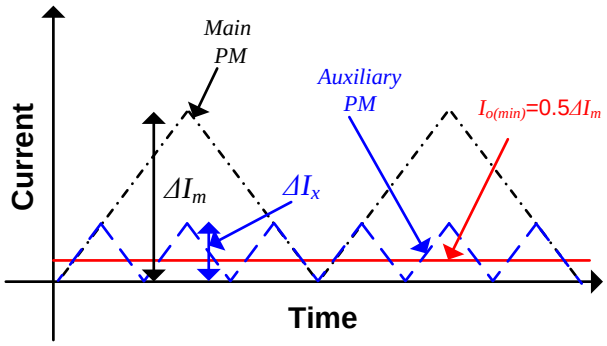


Fig. 5.6 Current waveforms of converter with the proposed design technique.

Larger ΔI_{m} allows a lower value filter inductor L_{m} to be used for the same switching frequency f_{sm}, reducing the conduction loss of the main PM inductor (lower value inductor → less turns (5.11)). Furthermore the switching losses in the auxiliary PM reduce since a lower switching frequency f_{sx} can be employed as a direct results of the extra BW gained by the main PM from the use of a lower value inductor L_{m}. With the main PM optimised for conduction losses, where the majority of the load current can be processed efficiently, the auxiliary PM only needs to process a small portion of load current, permitting this PM to be optimised for switching losses. Instead of sharing the load current equally as is done in the interleaved converter, the main PM is designed to handle up to 90% of the load current and is in operation for load currents above 10%, while the auxiliary PM is designed to handle up to 10% load current and is in operation when load current is below 10% or above 90% (n.b. the auxiliary PM must also be able to temporary support a large current during transient condition).

5.4. Loss analysis

All the components present within a converter incur losses during operation [101]. In general there are two types of losses that are related to the repetitive switching nature of the circuit (switching losses) and conduction losses which are related to current flow and voltage drops.

- ***Switching losses***

For the magnetic components (i.e. transformer and inductor), there are two types of switching related losses: i) the hysteresis loss and ii) eddy current loss (which is usually considered negligible for ferrite cores). The hysteresis loss is a result of not being able to recover the energy required to magnetise the core within each cycle. Hysteresis loss, P_{sL}, increases with flux density (B_{f}) and switching frequency, f_{s}, as described by (5.3). The constants k_c, α_c and β_c are material specific values and are usually provided by the manufacturer. For example, the core material 3F3 has the constants as follows: k_{c} = 1.5$x10^{-6}$ α_{c} =1.3 and β_{c} = 2.5.

$$P_{\mathrm{sL}} = k_{\mathrm{c}} f_{\mathrm{s}}^{\alpha_{\mathrm{c}}} B^{\beta_{\mathrm{c}}} \tag{5.3}$$

For the MOSFETs, the switching related losses consisted of two main parts, the gate drive loss (P_{gm}) and switching losses (P_{sm}) due to the overlapping of the drain-source voltage and current, V_{ds} and I_{d}, that occurs during a switching event (turn-on or turn-off). The loss P_{gm} is caused by the three parasitic capacitors, C_{gs}, C_{rss} and C_{oss}, across the three terminals of the MOSFET as shown in Fig. 5.7, which need to be charged or discharged to change the voltages at these terminals. The power required to switch on a MOSFET can be found by (5.4). To switch off a MOSFET, a low impedance path is provided to drain this charge away.

$$P_{\mathrm{gm}} = Q_{\mathrm{g}} V_{\mathrm{g}} f_{\mathrm{s}} \tag{5.4}$$

where Q_{g} is the total gate charge, V_{g} is the gate drive voltage.

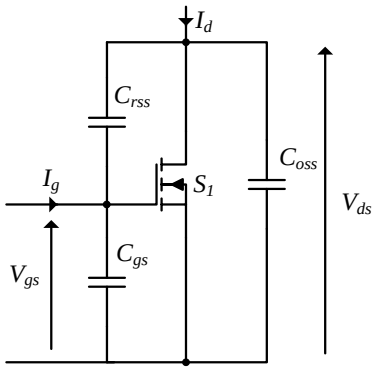


Fig. 5.7 Circuit diagram of MOSFET with the three parasitic capacitors.

The overlapping nature of V_{ds} and I_{d} during a MOSFET switching event [90] is the result of finite time taken to charge or discharge the three parasitic capacitors. The switching waveform of a MOSFET over one complete switching cycle period is shown in Fig. 5.8. When the gate signal is applied to switch on the MOSFET at t_1, the capacitor C_{gs} is charged and C_{rss} is discharged by the gate current, I_{g}, causing the gate voltage (V_{gs}) to rise. Both V_{ds} and I_{d} remain unchanged until V_{gs} reaches the MOSFET threshold voltage (V_{th}) at t_2, at which point the MOSFET begins to conduct with I_{d} starts rising proportionally to the gate voltage while V_{ds} remains unchanged, this overlapping leads to the first term in the loss equation (5.5). This period (t_{r1}) end as soon as I_{d} reaches the load current level at t_3, at which point V_{ds} start to fall. The I_{d} remains unchanged, leading to the second overlapping described by the second term of (5.5). Due to the need to discharge C_{rss} during this period (t_{r2}), the gate voltage remains constant until t_4 when $V_{\mathrm{ds}}{\sim}0V$. After t_4, the gate voltage continuous to rise to the gate drive voltage to guarantee the MOSFET to stay on and also to reduce the on-state resistance. Without detailing the switch-off procedure as for the switch-on, the same equation in (5.5) with t_{r1} and t_{r2} replaced by t_{f2} and t_{f1} can be obtained for the switch-off:

$$P_{\mathrm{s(on)}} = \frac{t_{\mathrm{r1}}}{T_s} V_{\mathrm{i}} \frac{I_{(\mathrm{rms})}}{2} + \frac{t_{r2}}{T_s} \frac{V_{\mathrm{i}}}{2} I_{(\mathrm{rms})} \tag{5.5}$$

where $I_{(\mathrm{rms})}$ is the rms current through the MOSFET.

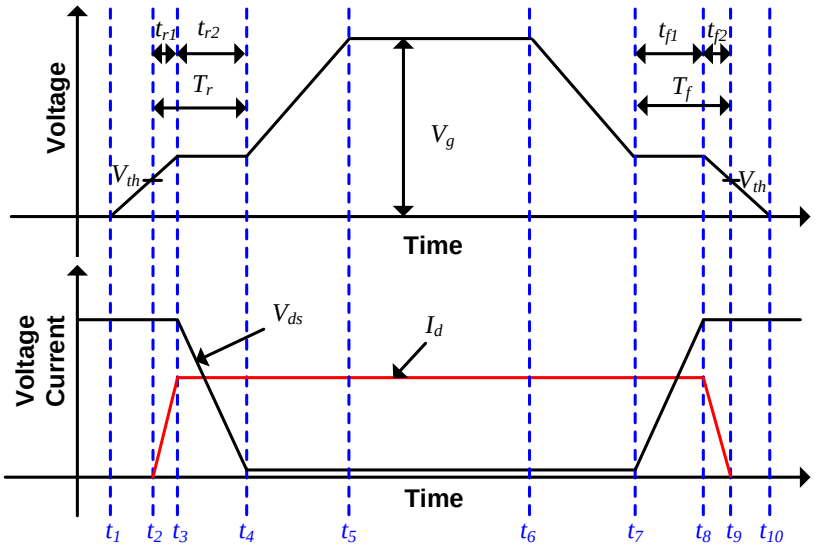


Fig. 5.8 MOSFET switching waveforms

By combining the two overlapping periods of the switch on (i.e. t_{r1} and t_{r2}) to T_{r} and the two periods of the switch off (i.e. t_{f1} and t_{f2}) to T_{f} for notation simplification, and substituting the switching period for the switching frequency in (5.5), the MOSFETs switching loss is simplified to (5.6):

$$P_{\mathrm{sm}} = \frac{(T_{\mathrm{r}}+T_{\mathrm{f}})V_{\mathrm{i}}I_{(\mathrm{rms})}f_{\mathrm{s}}}{2} \tag{5.6}$$

The switching loss of a diode (P_{sd}) is the result of finite time required to alter from a blocking state to the on-state, vice versa, which can be found from (5.7). This loss becomes negligible if a Schottky diode is used.

$$P_{\mathrm{sd}} = Q_{\mathrm{rr}}V_{\mathrm{i}}f_{\mathrm{s}} \tag{5.7}$$

where Q_{rr} is the reverse recovery charge.

- ***Conduction losses***

The conduction losses (P_c) in the parasitic resistances of each of the components can be found by Ohm's law as in (5.8):

$$P_{\mathrm{c}} = {I_{(\mathrm{rms})}}^2 R_i \tag{5.8}$$

where $I_{(\mathrm{rms})} = \sqrt{{I_{(dc)}}^2 + \frac{{\Delta I_m}^2}{12}}$ for a triangular waveform [101] and the subscript i in R_i representing the resistance of the different components.

The parasitic resistances of the transformer and inductor are the winding resistances which are proportional to the length, l, and the resistivity of the wire, ρ, and is inversely proportional to the cross-sectional area, A_w, as in (5.9):

$$R_{\mathrm{w}} = \frac{\rho l}{A_w} \tag{5.9}$$

With A_w selected to satisfy a specific current density, the number of turns should be low to minimise the resistance. For the transformer, the minimum number of primary turns, N_{p}, that must be selected in order to prevent the transformer core from saturation is given in (5.10):

$$N_{\mathrm{p}} = \frac{V_{\mathrm{i}}}{B_{\mathrm{peak}} A_{\mathrm{c}} \omega} \tag{5.10}$$

where A_{c} is the core area, B_{peak} is the peak flux density and $\omega = 2\pi f_{\mathrm{s}}$.

For the inductor, the minimum number of inductor turns (N_L) required to create the desired inductance is given in (5.11):

$$N_{\mathrm{L}} = \frac{L_{\mathrm{m}} I_{\mathrm{peak}}}{B A_{\mathrm{c}}} \tag{5.11}$$

where I_{peak} is the peak current.

To ensure low conduction losses, the number of turns should be kept to a minimum. However, for low switching losses, the number of turns should be high as both N_{p} and N_{L} are inversely proportional to the flux density. So, there is a compromise associated with the number of turns and the core and winding losses.

The conduction loss of the capacitor is assumed negligible. The conduction loss of the diodes can be calculated by (5.12):

$$P = V_f I_{avg} \tag{5.12}$$

With the components' losses equations given above, the effect of the different components' design and selection can be tested out and compared, allowing the ones that produce the least losses to be identified as potentially suitable for high efficiency designs. This loss analysis forms a critical part of the proposed HSSE design scheme.

5.5. Design examples and experimental results

To demonstrate the difference in efficiency of a parallel converter designed with the proposed design technique over the interleaved converter, two 360 W parallel converters were designed and built. The interleaved converter is used as benchmark with the switching frequency (f_{si}) of each PM selected to be 200 kHz. The other system requirements are as follows: input and output voltages, V_{i} = 400 V and V_{o} = 24 V, minimum load current $I_{\mathrm{o(min)}}$ = 0.5 A and V_{os} < 1 V under the maximum load drop.

5.5.1. Interleaved converter design

For the interleaved converter with f_{si} = 200 kHz, the LC filter parameters are calculated as follows: the inductances of each individual PM, L_{i}, is calculated by (3.7) to be 68 µH, this gives the equivalent inductance, L, of the two PMs to be 34 µH as calculated by (4.2), the output capacitance and the BW are calculated by (4.5) and (5.1) to be 159 µF and 2.16 kHz respectively. The number of turns on the filter inductor with RM12 core is calculated by (5.11) to be 13. In

order to find the transformer primary number of turns that leads to the lowest losses, the total transformer switching and conduction losses for the four different flux densities, B_{peak}, between 25 mT and 200 mT are calculated by (5.3) and (5.8)-(5.10) respectively. The results are listed in Table 5.1, showing that the transformer has the lowest losses when B_{peak} = 50 mT. The number of turns on the primary winding of the transformer wound using an ETD34 core is calculated by (5.10) to be 66.

B_{peak} (mT)	25	50	100	200
Losses (W)	0.74	0.55	2.48	10.71

Table 5.1 Interleaved PM transformer losses under different $\boldsymbol{B_{\text{peak}}}$.

5.5.2. Converter designed by the proposed HSSE technique

For a parallel converter designed using the proposed HSSE technique, the main PM is designed to minimising its losses while satisfying most of the system specifications. After finalising the main PM design, the auxiliary PM may be designed to meet the unfulfilled requirements. The design process is detailed as followed:

- ***Main power module design***

Since the switching frequency of the main PM is selectable, the number of turns for transformer primary winding is determined by two variables, the f_{sm} and B_{peak}. The switching and conduction losses of the transformer under different f_{sm} and B_{peak} are calculated by (5.3) and (5.8)-(5.10) respectively. The sum of the two losses under the different conditions are plotted in Fig. 5.9, which shows that for B_{peak} below 50 mT, the transformer losses are inversely proportional to the f_{sm}; however, when the B_{peak} goes above 100 mT, the switching losses outweighs the conduction losses, the transformer losses is proportional to f_{sm}.

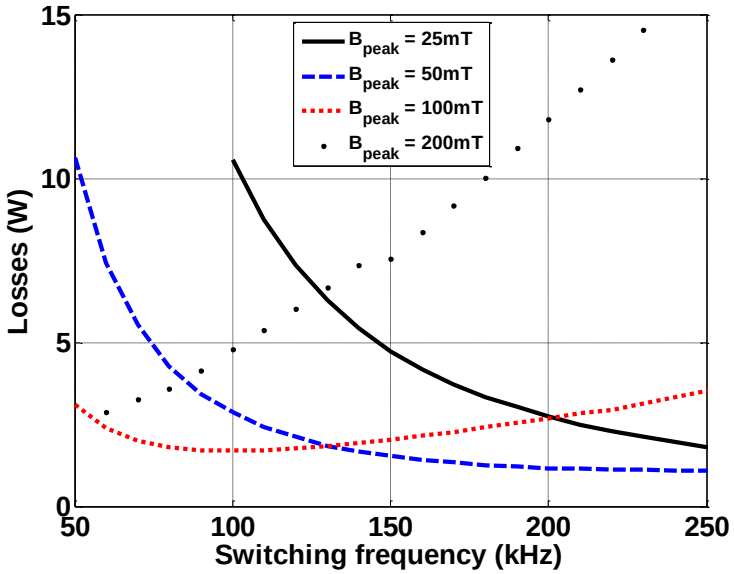


Fig. 5.9 Main PM transformer losses under different B_{peak}.

The current ripple of the main PM filter inductor is also selectable and so the number of turns is determined by the two variables, ΔI_{m} and f_{sm}. The influence of f_{sm} and ΔI_{m} on the inductor losses are shown in Fig. 5.10. For ΔI_{m} at 4 A, the increase in core loss outweighs the reduction in conduction loss, the inductor losses increase proportionally to f_{sm}. For ΔI_{m} values at and below 3 A, the inductor losses reduce gradually with increasing in f_{sm}, but whenever a smaller core is selected, which is possible with the lower inductance value due to the increase in f_{sm}, a jump in the losses are observed as more turns are required for the same inductance value with a smaller core, which in-turn increases the conduction losses.

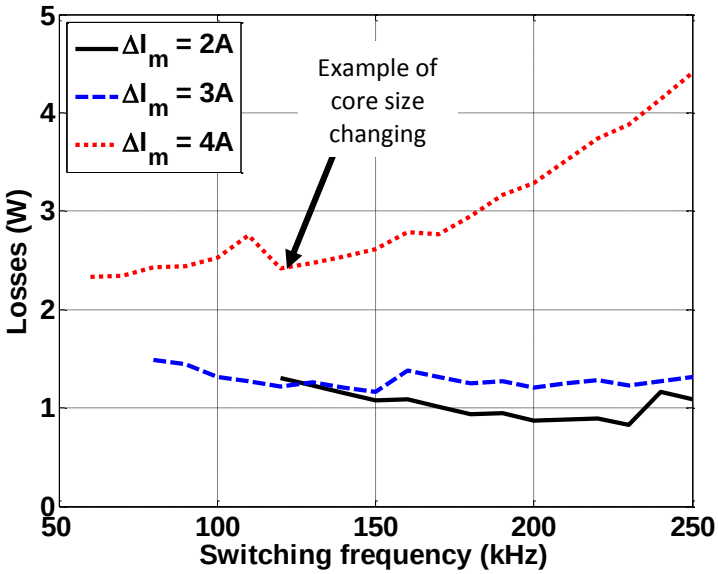


Fig. 5.10 Main PM inductor losses under different ΔI_{m}.

In order to finalise the selection of flux density B_{peak} for the transformer and current ripple ΔI_{m} for the inductor, a good value of switching frequency f_{sm} must be selected. A spreadsheet was built to calculate the different component losses under different f_{sm} as detailed in section 5.4. The losses due to the MOSFETs, the transformer, the inductor, and the total of the three losses are plotted in Fig. 5.11. It was found that the minimum losses occur at f_{sm} of 80 kHz, but since increasing f_{sm} to 100 kHz only increases the losses by 2 % but the BW is increased by almost 30 %, 100 kHz is selected.

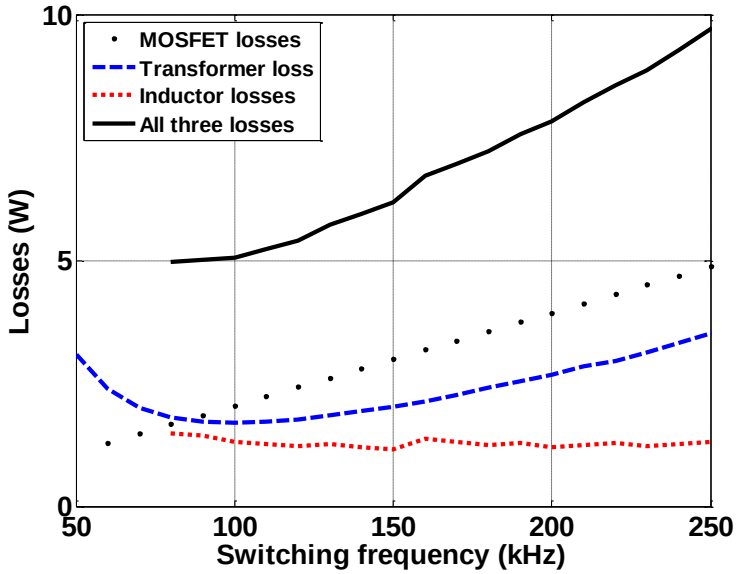


Fig. 5.11 Main PM components losses.

With f_{sm} = 100 kHz, Fig. 5.9 shows that the transformer has the least losses when B_{peak} = 100 mT. With a value for B_{peak} selected the main PM transformer primary number of turns with ETD34 core are calculated by (5.10) to be 66. From Fig. 5.10, ΔI_{m} of 3 A is selected for the inductor as the inductance with ΔI_{m} of 2 A is too large to be built with the selected RM core series. The number of turns calculated by (5.11) is 12, with RM14 core. The inductance is calculated by (3.7) to be 45 µH. With only the main PM in operation for $10\% < I_{\mathrm{o}} < 90\%$, the output capacitance must be selected based on ΔI_{m} to guarantee the voltage ripple requirement is satisfied under these load conditions which is calculated by (4.5) to be 211 µF. The BW is calculated by (5.1) to be 1.63 kHz.

- ***Auxiliary power module design***

The auxiliary PM is designed to meet the unfulfilled requirements. These are that the converter can operates at $I_{o(\mathrm{min})}$ of 0.5 A and provide the remaining BW of 0.53 kHz. The auxiliary PM switching frequency must therefore be at least 220 kHz to fulfil both of these requirements. The auxiliary PM filter inductance at this f_{sx} is 62 µH as calculated from (3.7) and the number of turns with RM8 core as calculated by (5.11) is determined to be 8. The total transformer losses with the

four B_{peak} are calculated by (5.3), (5.8)-(5.10) and are listed in Table 5.2. B_{peak} of 25 mT should be selected for the minimum losses. The transformer primary number of turns with this B_{peak} is calculated by (5.10) to be 153, with an ETD 29 core.

B_{peak} (mT)	25	50	100	200
Losses (W)	0.1	0.33	2.05	9.24

Table 5.2 Auxiliary PM transformer losses under different B_{peak}.

The parameters of the transformers and inductors of the interleaved converter and the converter with designed with the HSSE technique are summarised in Table 5.3.

	Standard design method	**Proposed HSSE design method**	
	Interleaved PM	**Main PM**	**Auxiliary PM**
Switching frequency (kHz)	200	100	220
Filter capacitor (µF)	159	211	
Filter inductor (µH)	68	45	62
Inductor number of turns, N_L, & core type	13, RM12	12, RM14	8, RM8
Transformer number of turns, N_P & core type	66, ETD34	66, ETD34	153, ETD29

Table 5.3 Summary of parameter for the interleaved and the proposed converters.

5.5.3. Prototype converters

Prototypes of the two converters are built with the similar double layered PCB. The converter with the proposed HSSE design technique is shown in Fig. 5.12. The inductors, transformers and isolated gate drivers are distributed on the top layer while the MOSFETs and diodes are in the bottom layer attached with a heat sink. MOSFET IPP60R160C6 is selected for the converter due to its low R_{ds}, t_{r}, t_{f} and Q_{g}. The duty cycles of the two PMs are controlled by the same Microchip PIC-based control board described in Chapter 4 (Fig. 4.18).

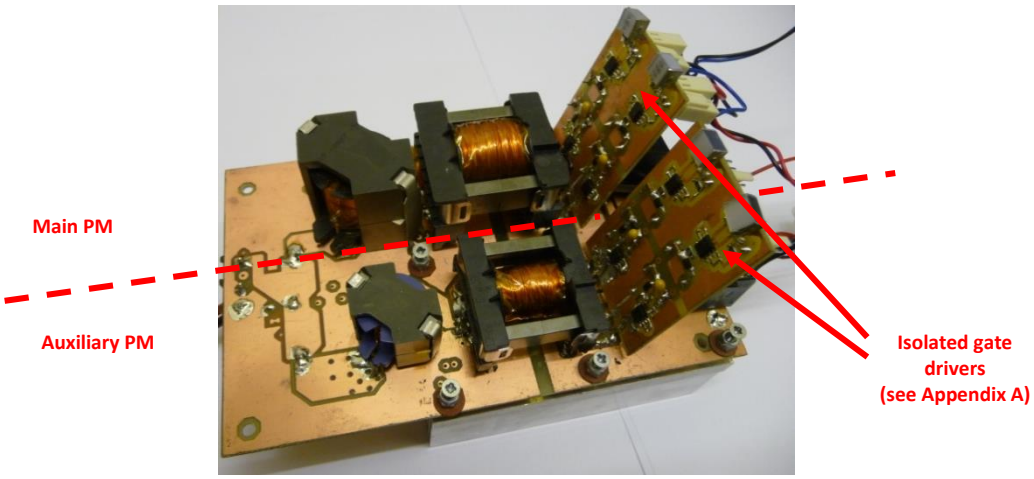


Fig. 5.12 Prototype of the 2SFC (proposed HSSE design technique).

The predicted efficiencies of the interleaved converter under different load conditions are shown in dashed line in Fig. 5.13. The efficiency of the converter with the proposed design technique contains three parts: 1) in dashed line for load conditions between the minimum load to 10% load where only the auxiliary PM is utilised; 2) dotted line for load conditions above 10% to 90% where only the main PM is utilised; 3) solid line for load conditions above 90% to full load where both PMs are utilised. Results show that the efficiency of the converter with the proposed design technique is improved under all load conditions. For load conditions below 10%, the improvement ranges between 6% to 12%, for load conditions between 10% to 90% the improvement ranges between 2% to 12% and for load condition above 90%, due to the lower efficiency of the auxiliary PM, the improvement ranges between 1.5% to 2%.

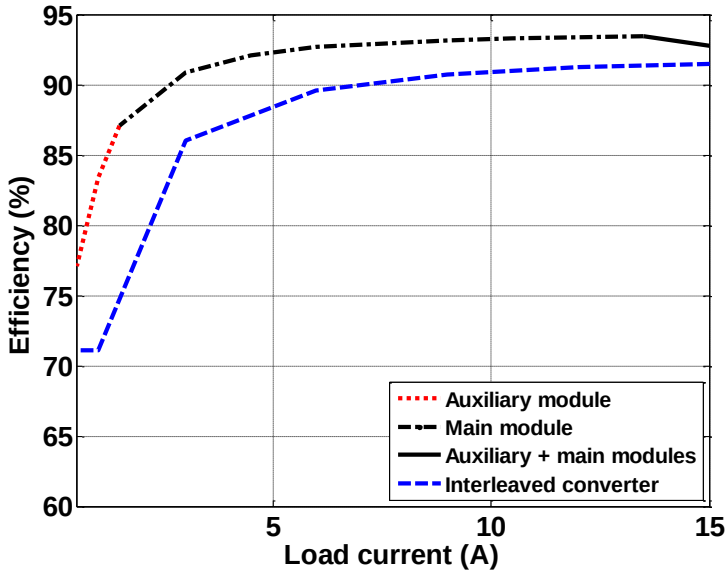


Fig. 5.13 The calculated efficiency curves for the two converters.

The experimental results of the two converters measured using a bespoke calorimeter (see Appendix C) and are plotted similarly in Fig. 5.14. The trend in experimental results matched well with the calculated result; however, there is a mismatch between efficiency values. The mismatch under light load condition is as much as 11% for the converter with the proposed design technique and 9% for the interleaved converter, but is reduced to 2% and 1% respectively at the maximum load condition. This is taken as measurement error, as the loss measurement is more difficult at light load, when the losses are correspondingly lower than at higher load. The efficiency improvement of the converter with the proposed design technique at minimum load, 10% load and full load conditions are predicted to be 6%, 12% and 1.5% respectively. The measured efficiency improvements are 4%, 7% and 1% respectively.

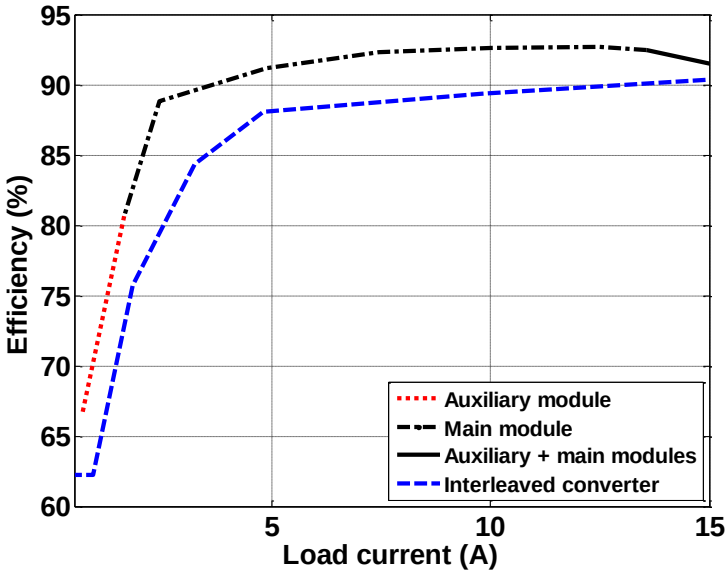


Fig. 5.14 Measured efficiency curves of the two converters.

5.6. Summary

This chapter has proposed a new design technique termed HSSE, to improve the steady-state efficiency of a parallel converter with two non-identical PMs. From the analysis of the existing design techniques, it was found that the efficiency is constrained by the minimum current ripple needed to keeps the converter operating in the CCM under the minimum load condition. The new design technique overcomes this constraint by allocating both the bandwidth and minimum load requirements to the auxiliary PM, allowing a larger ΔI_{m} and a lower f_{sm} to be selected for higher efficiency. For the purpose of showing the efficiency improvement with the proposed design technique, an interleaved converter and a converter with the proposed design technique are designd and built. The calculated results show the efficiency improvement is in the range of 1.5-12% dependent on the load conditions. The trends of experimental results match that of the theoretical one. Efficiencies from the prototypes are however lower at all load conditions. At light load, the efficiency are mismatched by 11%, while at maximum load, the efficiency mismatch are only 2%. This mismatch does not alter the trend in the efficiency improvement from the proposed design technique which ranged 1% to 7% across the load range, and is attributable to the difficulties in measuring low values of losses.

6. Active current ripple cancellation using a high frequency auxiliary converter

6.1. Introduction

The previous chapter has shown that the steady-state efficiency of the parallel converter can be improved by allocating the transient response requirement and minimum load condition to the auxiliary PM. One disadvantage of this technique is that the required filter capacitance is high due to the larger current ripple produced by the main PM. This chapter presents a novel active current ripple cancellation scheme that allows the filter capacitor value to be reduced. From the operation of the two PMs under steady-state condition, guidelines for selecting the inductor for each PM and the duty cycle profiles required to shape the inductor currents are obtained. Through the component losses analysis, two 20 W (V_o = 3.3 V, I_o = 6 A) converters are designed and built to demonstrate the effectiveness of the active current ripple cancellation schemes. The efficiencies of the two converters are compared through simulation and experimentation.

6.2. Active current ripple cancellation

The HSSE design technique proposed in the previous chapter required the main PM to be designed with a large current ripple to achieve high efficiency, which demands a large output capacitor to satisfy the output voltage ripple requirement. To reduce the size of the capacitor, the large current ripple seen by the output capacitor, due to the large ΔI_m, is reduced by the auxiliary PM through a novel ripple cancellation technique which is detailed in the next section. The parallel converter utilised in this chapter is given in Fig. 4.1. To avoid current circulation between the two PMs, the synchronous rectifier (i.e. MOSFET S_1) of the auxiliary module is not utilised for the work in this chapter.

6.2.1. Theory of operation

Current ripple cancellation by switched-mode power converters have been demonstrated [69]-[72]. The parallel converter in these schemes contains two identical PMs, with the main PM operating complementarily to the auxiliary PM, producing two current ripple waveforms as shown in solid and dash-dotted lines in Fig. 6.1. The combination of the two current ripples lead to a resultant current with almost no current ripple as shown in the dotted line Fig. 6.1.

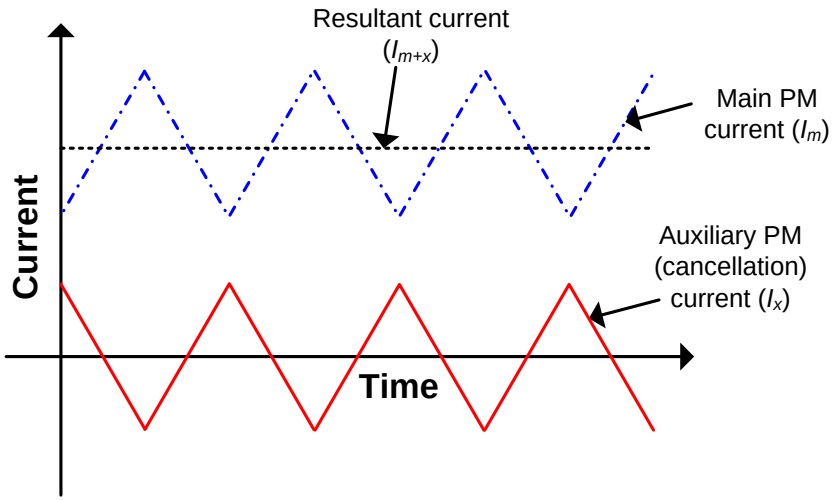


Fig. 6.1 Active current ripple cancellation with identical PMs.

The scheme proposed here differs from the above schemes by employing two non-identical PMs, reusing the auxiliary PM, the primary purpose of which was to improve the converter's transient response. Fig. 6.2 shows the main concept of the proposed ripple cancellation technique, where the cancellation current (I_x), which is equal and opposite to the main PM current (I_m), is generated by the auxiliary PM and is summed with the main PM current (at the point of common connection in Fig. 4.1), to produce the resultant current (I_{m+x}). Since the auxiliary PM is a unidirectional buck converter and is operating at a higher switching frequency than the main PM, I_x is always positive. The resultant current seen by the capacitor therefore has the current ripple of the auxiliary PM and an amplitude of $I_m + I_x$.

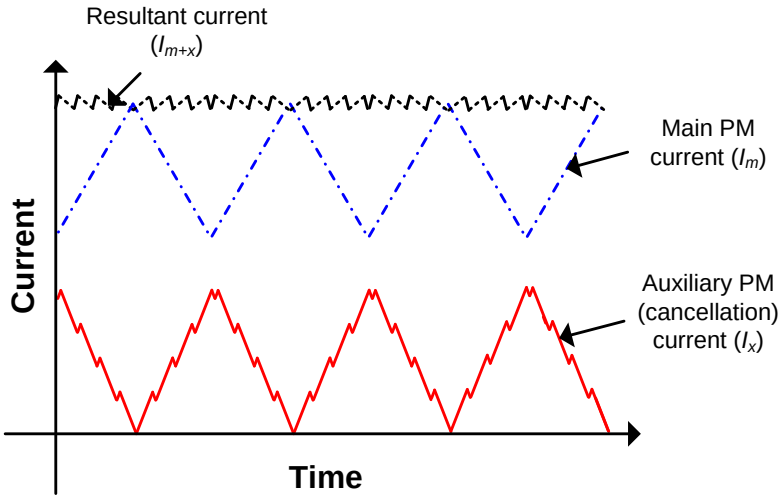


Fig. 6.2 Main PM, auxiliary PM and resultant current waveforms.

6.2.2. Inductor current ripple and rate of change

The four parameters that determine the effectiveness of the ripple cancellation scheme are the rate of change of inductor current $\left((d/dt)I\right)$, the net rate of change of inductor current $\left((d/dt)I_{(\mathrm{net})}\right)$, the duty cycles (δ) and the inductor current ripple (ΔI) (n.b. the analysis in the following sections assumes all component losses are negligible). The five equations found in chapter 3 for the main PM are recapped as followed:

$$\frac{d}{dt}I_{\mathrm{m}(+)} = \frac{V_{\mathrm{i}}-V_{\mathrm{o}}}{L_{\mathrm{m}}} \tag{3.2}$$

$$\frac{d}{dt}I_{\mathrm{m}(-)} = \frac{-V_{\mathrm{o}}}{L_{\mathrm{m}}} \tag{3.3}$$

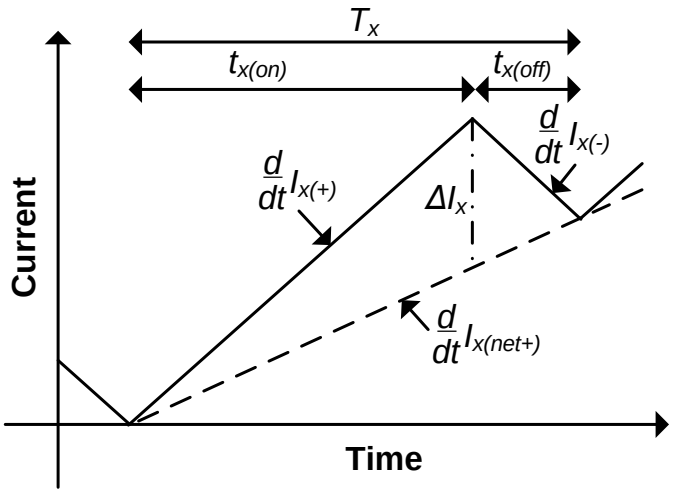
$$\frac{d}{dt}I_{\mathrm{m(net)}} = \frac{\frac{V_{\mathrm{i}}-V_{\mathrm{o}}}{L_{\mathrm{m}}}t_{\mathrm{m(on)}}+\frac{-V_{\mathrm{o}}}{L_{\mathrm{m}}}t_{\mathrm{m(off)}}}{T_s} = \frac{V_{\mathrm{i}}\delta_{\mathrm{m}}-V_{\mathrm{o}}}{L_{\mathrm{m}}} \tag{3.4}$$

$$V_{\mathrm{o}} = \delta_{\mathrm{m}}V_{\mathrm{i}} \tag{3.5}$$

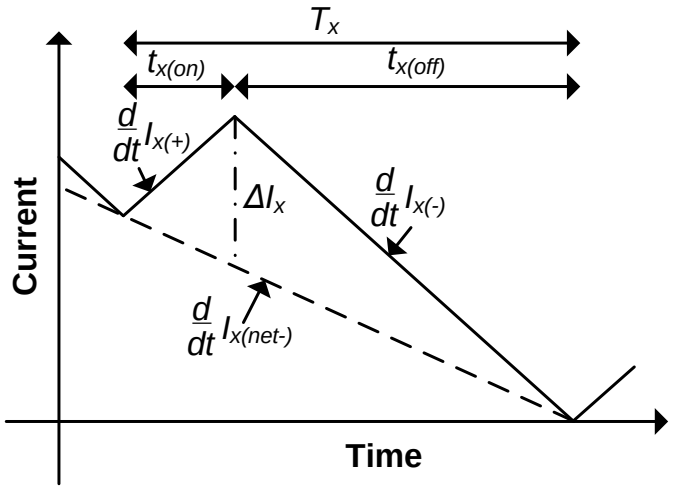
$$\Delta I_{\mathrm{m}} = \frac{V_{\mathrm{i}}-V_{\mathrm{o}}}{L_{\mathrm{m}}}\delta_{\mathrm{m(ss)}}T_{\mathrm{s}} = \frac{V_{\mathrm{i}}\left(1-\delta_{\mathrm{m(ss)}}\right)}{L_{\mathrm{m}}}\delta_{\mathrm{m(ss)}}T_{\mathrm{s}} \tag{3.6}$$

For the main PM operating in steady state, the duty cycle, $\delta_{\mathrm{m(ss)}}$ is described by (3.5), the rate of current rise, $(d/dt)I_{\mathrm{m(+)}}$, and rate of current fall, $(d/dt)I_{\mathrm{m(-)}}$, and current ripple, ΔI_{m}, can be found using (3.2), (3.3) and (3.6) respectively.

For the auxiliary PM, the duty cycle is set to cancel the current ripple of the main PM detailed in section 6.3.1, the net rate of change of inductor current $\left((d/dt)I_{\mathrm{x(net)}}\right)$ over one switching period is non-zero and is calculated by (3.4) (n.b. the subscript of m in (3.4) is replaced by x). Defining $\delta_{\mathrm{x(ss)}}$ to be the auxiliary PM duty cycle for no net rate of change of inductor current, for $\delta_{\mathrm{x}} > \delta_{\mathrm{x(ss)}}$, a net increase in rate of change of current, $(d/dt)I_{\mathrm{x(net+)}}$, is observed as shown in Fig. 6.3 (a), for $\delta_{\mathrm{x}} < \delta_{\mathrm{x(ss)}}$ a net decrease in rate of change of current occurs, as shown by $(d/dt)I_{\mathrm{x(net-)}}$ in Fig. 6.3 (b).



(a)



(b)

Fig. 6.3 Current waveforms of the auxiliary PM under one auxiliary PM cycle. (a) $\delta_x = 0.75$ (b) $\delta_x = 0.25$

The current ripple of the auxiliary PM can be found with the aid of Fig. 6.3. For $\delta_x > \delta_{x(ss)}$, Fig. 6.3 (a) shows that ΔI_x is generated by the difference in the rate of current rise $(d/dt)I_{x(+)}$ and the net rate of current rise $(d/dt)I_{x(net+)}$ over the on-period as in (6.1) and for $\delta_x < \delta_{x(ss)}$, Fig. 6.3 (b) shows that ΔI_x is similarly generated by the difference in the rate of current fall $(d/dt)I_{x(-)}$ and the net rate of current fall $(d/dt)I_{x(net-)}$ over the off-period and is also described by (6.1). An

interesting result is that (6.1) is the same as the second expression in (3.6), while the ΔI_{m} is affected by the output voltage through $\delta_{\mathrm{m(ss)}}$, the ΔI_{x} is affected by the desired net rate of change of the auxiliary PM inductor current through δ_{x}.

$$\Delta I_{\mathrm{x}} = \left(\frac{V_{\mathrm{i}}-V_{\mathrm{o}}}{L_{\mathrm{x}}} - \frac{V_{\mathrm{i}}\delta_{\mathrm{x}}-V_{\mathrm{o}}}{L_{\mathrm{x}}}\right)\delta_{\mathrm{x}}T_{\mathrm{x}}$$
$$= \frac{V_{\mathrm{i}}(1-\delta_{\mathrm{x}})}{L_{\mathrm{x}}}\delta_{\mathrm{x}}T_{\mathrm{x}} \qquad (6.1)$$

From (3.4), it can be shown that the net rate of change of the auxiliary PM inductor current, $(d/dt)I_{\mathrm{x(net)}}$, increases linearly from the minimum of 0 at $\delta_{\mathrm{x}} = \delta_{\mathrm{x(ss)}}$ to the maximum net rate of rise or fall of the inductor current at δ_{x} of 1 and 0 respectively (see Fig. 6.6 (a)) and from (6.1), the current ripple, ΔI_x is reduced symmetrically from the maximum at $\delta_{\mathrm{x}} = \delta_{\mathrm{x(ss)}}$ to the minimum of 0 at δ_{x} of 1 and 0 (see Fig. 6.6 (b)).

6.2.3. Generation of the cancellation current

The inductor current waveforms of the two PMs over one main PM cycle is shown in Fig. 6.4 (from an expansion of Fig. 6.3). Fig. 6.4 shows that in order to achieve exact current ripple cancellation, the net rate of the auxiliary PM inductor current fall (3.4) (n.b. the second expression in (3.4) with subscript of m in those equations replaced by x) must match the rate of main PM inductor current rise (3.2) during the main PM on-period as in (6.2). Similarly, the net rate of auxiliary PM inductor current rise (3.4) must match the rate of the main PM inductor current fall in (3.3) during the main PM off-periods as in (6.3).

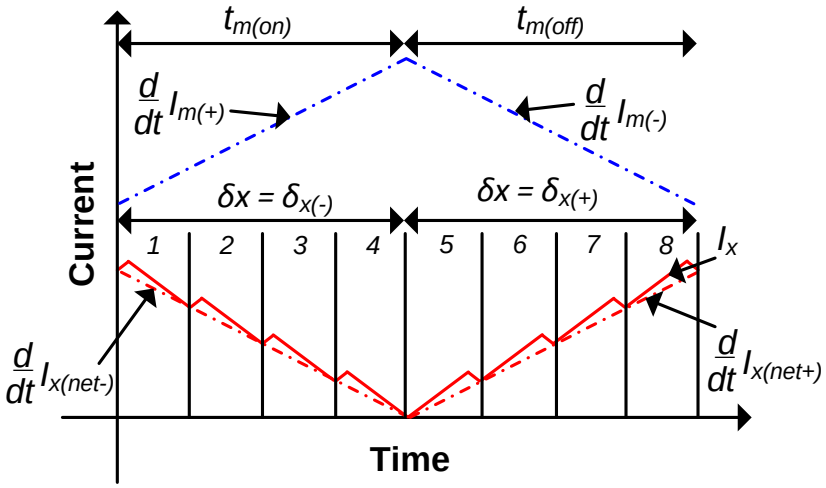


Fig. 6.4 Current waveforms of the main and auxiliary PMs over one main PM cycle.

$$-\frac{V_{\mathrm{i}}\delta_{\mathrm{x}}-V_{\mathrm{o}}}{L_{\mathrm{x}}}=\frac{V_{\mathrm{i}}-V_{\mathrm{o}}}{L_{\mathrm{m}}} \tag{6.2}$$

$$\frac{V_{\mathrm{i}}\delta_{\mathrm{x}}-V_{\mathrm{o}}}{L_{\mathrm{x}}}=-\frac{-V_{\mathrm{o}}}{L_{\mathrm{m}}} \tag{6.3}$$

From (3.2) and (3.3), or the right hand side of (6.2) and (6.3), it can be seen that $(d/dt)I_{\mathrm{m}(+)}$ depends on both the V_{i} and V_{o}, while the $(d/dt)I_{\mathrm{m}(-)}$ depends only on the V_{o}, the two main PM rates of inductor current are asymmetric except at $V_{\mathrm{o}} = 0.5\,V_{\mathrm{i}}$. For $V_{\mathrm{o}} > 0.5V_i$, $\frac{d}{dt}I_{\mathrm{m}(-)}$ is higher and for $V_{\mathrm{o}} < 0.5V_{\mathrm{i}}$, $(d/dt)I_{\mathrm{m}(+)}$ is higher.

With m auxiliary PM cycles (see section 6.3.2) contained within each main PM cycle (eight in the case of Fig. 6.4), and the adjustable net rate of change of the auxiliary PM inductor current through δ_{x}, the cancellation current (I_{x}) during the main PM on- and off-period can be generated by the auxiliary PM by setting δ_{x} for each auxiliary PM cycle, provided that L_{x} can produce the higher of the two net rates as detailed in the next section. The δ_{x} that produces the desired $(d/dt)I_{\mathrm{x(net-)}}$ is termed $\delta_{\mathrm{x}(-)}$, and the δ_{x} that produces the desired $(d/dt)I_{\mathrm{x(net+)}}$ is termed $\delta_{\mathrm{x}(+)}$.

6.3. Design consideration

This section develops several relationships that allow suitable auxiliary PM inductor to be selected.

6.3.1. Auxiliary PM inductor and duty cycle selection

By rearranging (6.2) and (6.3) in terms of the ratio between the two inductors, L_m/L_x, and the substitution of V_o by (3.5), the relationship between the main and auxiliary duty cycles (δ_m and δ_x) and the inductor ratio L_m/L_x for the main PM on- and off-period are obtained in (6.4) and (6.5) respectively.

$$\left.\frac{L_m}{L_x}\right|_{t_{sm(on)}} = -\frac{1-\delta_m}{\delta_x-\delta_m} \tag{6.4}$$

$$\left.\frac{L_m}{L_x}\right|_{t_{sm(off)}} = \frac{\delta_m}{\delta_x-\delta_m} \tag{6.5}$$

Since $(d/dt)I_{m(+)}$ is higher for $V_o < 0.5V_i$ ($\delta_m < 0.5$), the L_x (for a given L_m) is selected based on (6.4) which is plotted in region 1 (Fig. 6.5). Similarly, since $(d/dt)I_{m(-)}$ is higher for $V_o > 0.5V_i$ ($\delta_m > 0.5$) , L_x is selected based on (6.5) and is plotted in region 2 (Fig. 6.5).

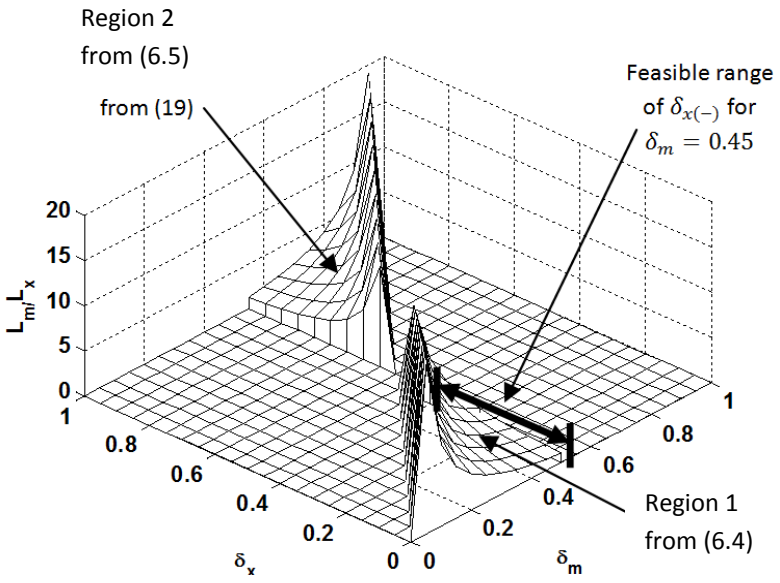
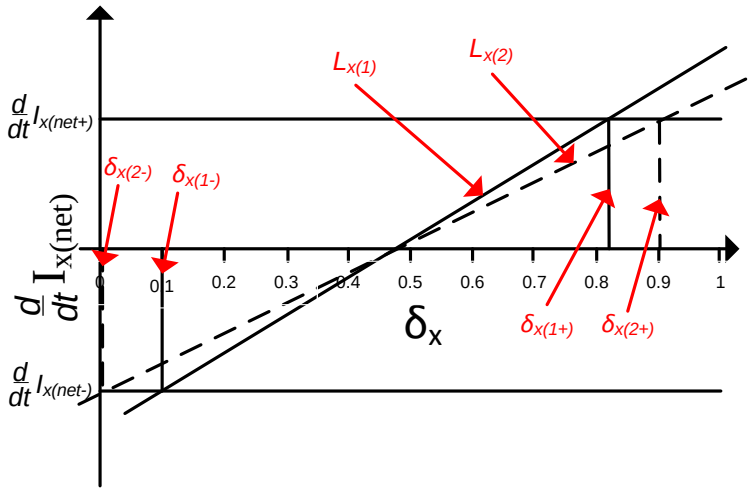


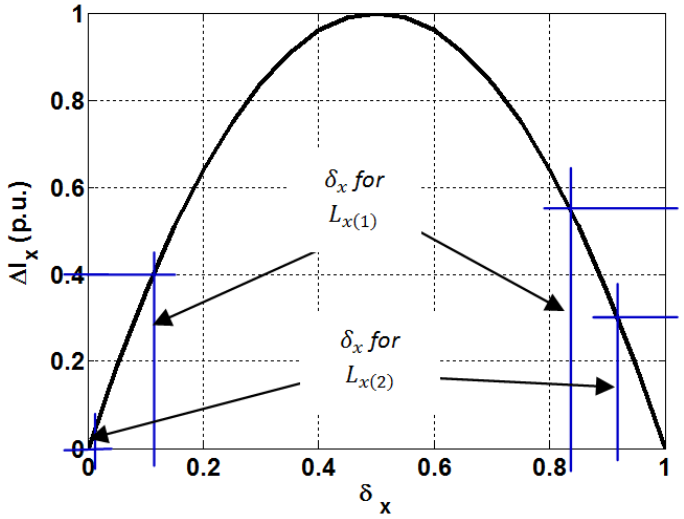
Fig. 6.5 Ratio of the two inductors against δ_m and δ_x.

Fig. 6.5 shows that dependent on δ_{m}, there is a range of δ_{x}, and hence L_{x}, that can be selected to allow the desired net rate of change of the auxiliary PM inductor current to be produced (e.g. for $\delta_{\mathrm{m}} = 0.45$, any $\delta_{\mathrm{x}} < 0.45$ can be selected, as labelled in the feasible range in Fig. 6.5).

Fig. 6.6 (a) shows the net rate of change of auxiliary PM inductor current as a function of δ_{x} for two different inductors, $L_{\mathrm{x}(1)}$ and $L_{\mathrm{x}(2)}$ $\left(L_{\mathrm{x}(1)} < L_{\mathrm{x}(2)}\right)$, and also the two $(d/dt)I_{\mathrm{x(net)}}$ during the main PM on- and off-period for a given L_{m} and $\delta_{\mathrm{m(ss)}}$ in the horizontal lines (n.b. $\delta_{\mathrm{m(ss)}} = \delta_{\mathrm{x(ss)}} = 0.48$ in this example, which is also the auxiliary PM duty cycle where $(d/dt)I_{\mathrm{x(net)}} = 0$). The interception points are the duty cycles ($\delta_{\mathrm{x}(1-)}$ and $\delta_{\mathrm{x}(1+)}$ for $L_{\mathrm{x}(1)}$, and $\delta_{\mathrm{x}(2-)}$ and $\delta_{\mathrm{x}(2+)}$ for $L_{\mathrm{x}(2)}$) where the auxiliary PM produces the two desired net rate of change of inductor currents $(d/dt)I_{\mathrm{x(net-)}}$ and $(d/dt)I_{\mathrm{x(net+)}}$. The values of $\delta_{\mathrm{x}(-)}$ (i.e. $\delta_{\mathrm{x}(1-)}$ and $\delta_{\mathrm{x}(2-)}$) and $\delta_{\mathrm{x}(+)}$ (i.e. $\delta_{\mathrm{x}(1+)}$ and $\delta_{\mathrm{x}(2+)}$) together with the different L_{x} values determine the ΔI_{x} as illustrated in Fig. 6.6 (b), where $L_{\mathrm{x}(1)}$ has the larger current ripple of 0.59 p.u. during the main PM off-period $\left(\delta_{\mathrm{x}(+)} = 0.82\right)$, while $L_{\mathrm{x}(2)}$ has the larger current ripple of 0.32 p.u. during $t_{\mathrm{sm(off)}}$ $\left(\delta_{\mathrm{x}(+)} = 0.90\right)$.



(a)

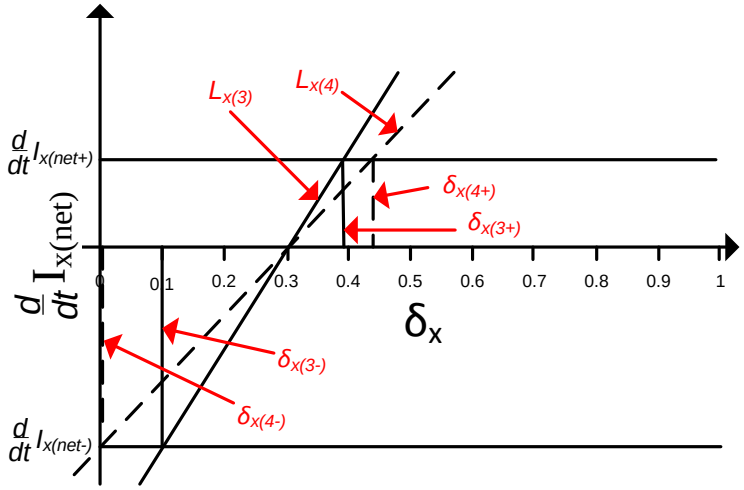


(b)

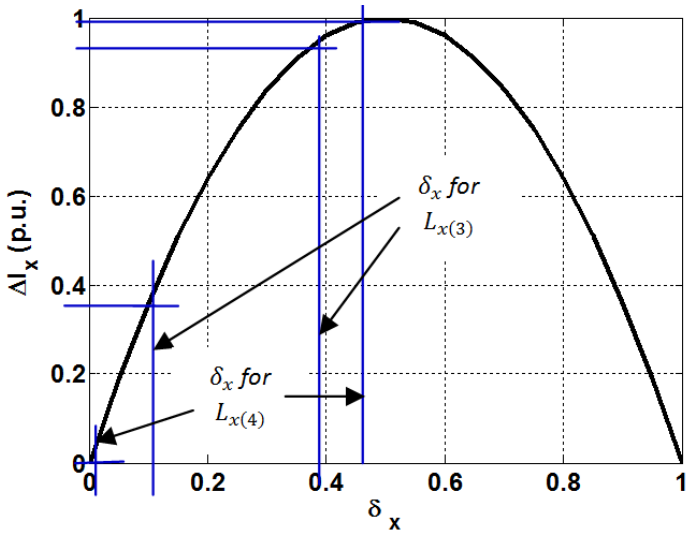
Fig. 6.6 Effect on δ_x and ΔI_x with different L_x at $\delta_{x(ss)} = 0.48$. (a) δ_x (b) ΔI_x

Since ΔI_x determines the minimum switching frequency of the auxiliary PM (f_{sx}) (from (6.1)), the higher inductance of $L_{x(2)}$ with smaller ΔI_x allows the auxiliary PM to operate at lower f_{sx} and usually with higher efficiency. Furthermore, by selecting $\delta_{x(-)} = 0$ as with $L_{x(2)}$, the auxiliary PM can be disabled completely during the main PM on-period if required to further enhance the efficiency. It should be noted that a higher auxiliary inductor value does not always lead to smaller ΔI_x as illustrated in Fig. 6.7 (a), where $\delta_{x(ss)}$ is now set to 0.3. The higher inductance $L_{x(4)}$ has the

maximum current ripple of 0.99 p.u. in comparison to $L_{x(3)}$ which has a current of only 0.95 p.u. as shown in Fig. 6.7 (b).



(a)



(b)

Fig. 6.7 Effect on δ_x and ΔI_x with different L_x at $\delta_{x(ss)} = 0.3$. (a) δ_x (b) ΔI_x

6.3.2. Ripple reduction ratio

It was shown in section 6.3.1 that L_x is always chosen to be less than L_m (except for the case when $L_x = L_m$ where $\delta_m = 0.5$) and given that $\Delta I_m > \Delta I_x$, f_{sx} must be greater than f_{sm} (as seen in section 6.2.3 $f_{sx} = m f_{sm}$). Therefore δ_m and the ripple reduction ratio p (difference in current ripples between the two PMs) determine the minimum f_{sx}. Using (6.4) and (6.5) with f_{sm} selected to be 30 kHz, the minimum frequency ratio f_{sx}/f_{sm} for $1 \leq p \leq 3$ are shown in Fig. 6.8. Since a high frequency ratio m leads to high f_{sx} and, hence, low auxiliary PM efficiency. Thus, there is a maximum value for the ripple reduction ratio that must not be exceeded beyond which the benefit afforded by the reduction in conduction losses due to the smaller main PM inductor (resulting from the large ΔI_m) will be negated by the increase in switching losses from the operation of the auxiliary PM for ripple cancellation.

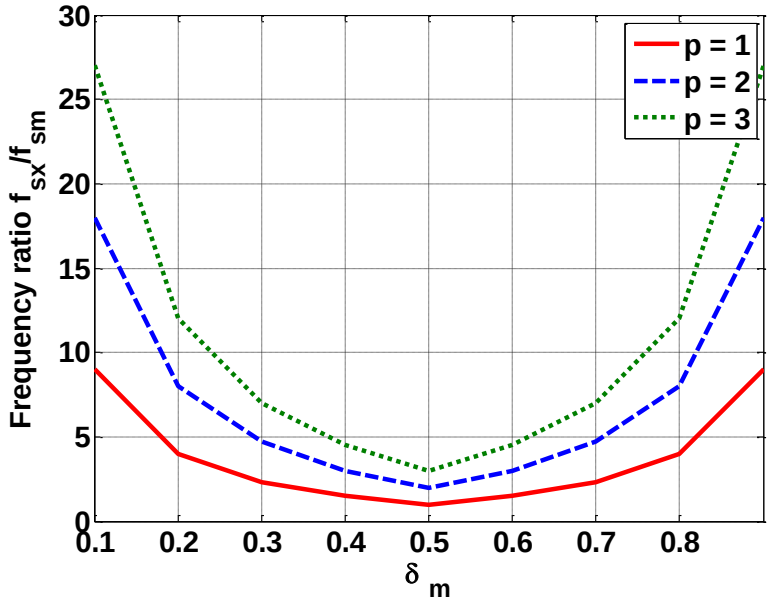


Fig. 6.8 Frequency ratios of the two PMs under different δ_m and p.

6.3.3. Efficiency comparison

The interleaved converter has become popular due to its lower conduction losses due to the load current sharing between the PMs and also its current ripple attenuation ability which allows lower switching frequency to be used, resulting in lower switching losses. In a two PM interleaved

converter, the effectiveness of the ripple attenuation, whilst ideal with a duty cycle of 0.5 on both converters, diminishes as the duty cycle approaches the minimum or maximum value allowable. The efficiency improvement from the proposed converter scheme becomes more apparent under these extreme duty cycle conditions.

- ***Component loss ratio***

In order to investigate the difference in the component losses between the two converters, the loss ratio for each of the components in the converters, with the proposed scheme, is divided by the losses in the interleaved converter to normalise the measurements to that of the interleaved converter. With the RMS current of the main and auxiliary PMs and interleaved converter PMs defined as $I_{\mathrm{m(rms)}}$, $I_{\mathrm{x(rms)}}$ and $I_{\mathrm{i(rms)}}$ respectively (the three currents are detailed in Appendix B), and the switching frequencies of the main and auxiliary PMs β and γ times that of the interleaved converter respectively. The MOSFET switching loss ratio $P_{\mathrm{sm}}(n)$ is obtained (5.6) as follows:

$$P_{\mathrm{sm}}(n) = \frac{\frac{(t_{\mathrm{r}}+t_{\mathrm{f}})V_{\mathrm{i}}I_{\mathrm{m(rms)}}\beta f_{\mathrm{si}}}{2} + \frac{(t_{\mathrm{r}}+t_{\mathrm{f}})V_{\mathrm{i}}I_{\mathrm{x(rms)}}\gamma f_{\mathrm{si}}}{2}}{2\frac{(t_{\mathrm{r}}+t_{\mathrm{f}})V_{\mathrm{i}}I_{\mathrm{i(rms)}}f_{\mathrm{si}}}{2}} = \frac{I_{\mathrm{m(rms)}}\beta + I_{\mathrm{x(rms)}}\gamma}{2I_{\mathrm{i(rms)}}} \tag{6.6}$$

Similarly, the MOSFET gate drive and conduction losses, inductor switching and conduction losses and diode conduction losses ratios using (5.4) and (5.8), (5.3) and (5.8) and (5.12) are found as in (6.7) to (6.11) respectively:

$$P_{\mathrm{gm}}(n) = \frac{2\beta+\gamma}{4} \tag{6.7}$$

$$P_{\mathrm{cm}}(n) = \frac{I_{\mathrm{m(rms)}}{}^2 R_{\mathrm{ds}} + I_{\mathrm{x(rms)}}{}^2 R_{\mathrm{ds}}\delta_{\mathrm{x}} + V_{\mathrm{f}} I_{\mathrm{x(rms)}}(1-\delta_{\mathrm{x}})}{2I_{\mathrm{i(rms)}}{}^2 R_{\mathrm{ds}}} \tag{6.8}$$

$$P_{\mathrm{sL}}(n) = \frac{(\beta+\gamma)^{\alpha_{\mathrm{c}}}}{2} \tag{6.9}$$

$$P_{\mathrm{cL}}(n) = \frac{I_{\mathrm{m(rms)}}{}^2 + I_{\mathrm{x(rms)}}{}^2}{2I_{\mathrm{i(rms)}}{}^2} \tag{6.10}$$

$$P_{\mathrm{cd}}(n) = \frac{\beta}{2} \tag{6.11}$$

To identify the difference in losses between the two converters, the total conduction loss ratio $P_{\mathrm{c}}(n)$ is formulated by multiplying the components' conduction loss ratios in (6.8), (6.10) and (6.11) with loss corresponding to the components to give (6.12) For example, the difference in the diode conduction loss between the two converters can be found by $(P_{\mathrm{cd}}(n)P_{\mathrm{cd}})/(P_{\mathrm{cd}} + P_{\mathrm{cm}} + P_{\mathrm{cL}})$, where $P_{\mathrm{cd}}(n)$ is the diode conduction loss ratio, P_{cd} is the diode conduction loss and $(P_{\mathrm{cd}} + P_{\mathrm{cm}} + P_{\mathrm{cL}})$ is the total conduction losses of the interleaved converter. Similarly, the total switching loss ratio can be found with (6.6), (6.7) and (6.9) to give (6.13). For proposed parallel converter to achieve higher efficiency than the interleave converter, the sum of $P_{\mathrm{c}}(n)$ and $P_{\mathrm{s}}(n)$ calculated from (6.12) and (6.13) must be less than 1.

$$P_{\mathrm{c}}(n) = \frac{P_{\mathrm{cd}}(n)P_{\mathrm{cd}} + P_{\mathrm{cm}}(n)P_{\mathrm{cm}} + P_{\mathrm{cL}}(n)P_{\mathrm{cL}}}{P_{\mathrm{cd}} + P_{\mathrm{cm}} + P_{\mathrm{cL}}} \tag{6.12}$$

$$P_{s}(n) = \frac{P_{\mathrm{gm}}(n)P_{\mathrm{gm}} + P_{\mathrm{sm}}(n)P_{\mathrm{sm}} + P_{\mathrm{sL}}(n)P_{\mathrm{sL}}}{P_{\mathrm{gm}} + P_{\mathrm{sm}} + P_{\mathrm{sL}}} \tag{6.13}$$

6.3.4. Practical consideration

In a practical system, both the input voltage and load vary. The input voltage affects the rate of rise of the main and auxiliary PM inductor currents (3.2) and (3.4). With a fixed output voltage, (3.5) shows that as the input voltage changes, the duty cycle changes inversely to provide regulation. The change in δ_{m}, $\delta_{\mathrm{x}(-)}$ and $\delta_{\mathrm{x}(+)}$ due to the change in input voltage $(V_{\mathrm{i}}/V_{\mathrm{i(nom)}})$ can thus be compensated by a gain that is the inverse of the change, or $k_c = V_{\mathrm{i(nom)}}/V_{\mathrm{i}}$. For example, assuming the main PM duty cycle $\delta_{\mathrm{m(nom)}}$ calculated for the nominal input voltage, $V_{\mathrm{i(nom)}}$, of 12 V is 0.4, if the input voltage is increased to 13.2 V, the new duty cycle is $\delta_{\mathrm{m}} = k_{\mathrm{c}}\delta_{\mathrm{m(nom)}} = 0.9x0.4 = 0.36$. The change in load condition affects the voltage drop across the parasitic resistances of components, leading to the change in δ_{m}, $\delta_{\mathrm{x}(-)}$ and $\delta_{\mathrm{x}(+)}$ which can be similarly compensated.

6.4. Design example and experimental results

To demonstrate the benefits of the proposed ripple cancellation technique, a parallel converter is designed using the methods just mentioned and compared to an interleaved converter. Both converters have the following specifications: output power rating of 20 W (V_o = 3.3 V, I_o = 6 A), V_i = 12 V (±10%), ΔI_m = 1 A, I_s = 5.5 A, ΔV_o = 33 mV and V_{os} = 165 mV.

With this specification and (6.12) and (6.13), the total loss ratio $P(n) = P_c(n) + P_s(n)$ of the two converters with the load sharing ratio, $0 \le \alpha \le 1$ $\left(6 \ge \frac{\Delta I_m}{2} \ge 0\ A, \text{see Appendix B}\right)$, main PM to interleaved converter switching frequency ratio ($\beta = f_{sm}/f_{si}$) over the range $0.05 \le \beta \le 1$ (f_{sm} = 30 kHz and $600 \ge f_{si} \ge 30$ kHz) and ($\gamma = f_{sx}/f_{si} = 2.57$) are plotted in Fig. 6.9. The figure shows there is a region where the proposed converter can achieve higher efficiency than the interleaved converter ($P(n) < 1$) (e.g. with β = 0.2, α must be greater than 0.75 ($\Delta I_m < 3$ A)).

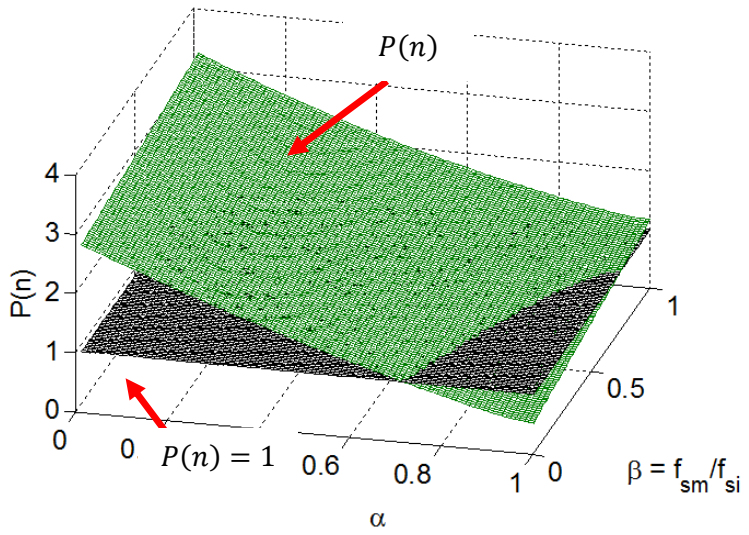
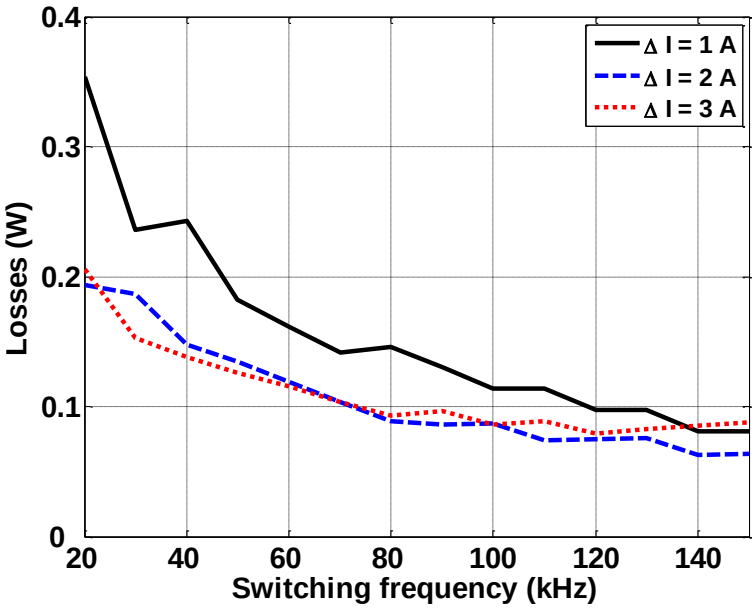


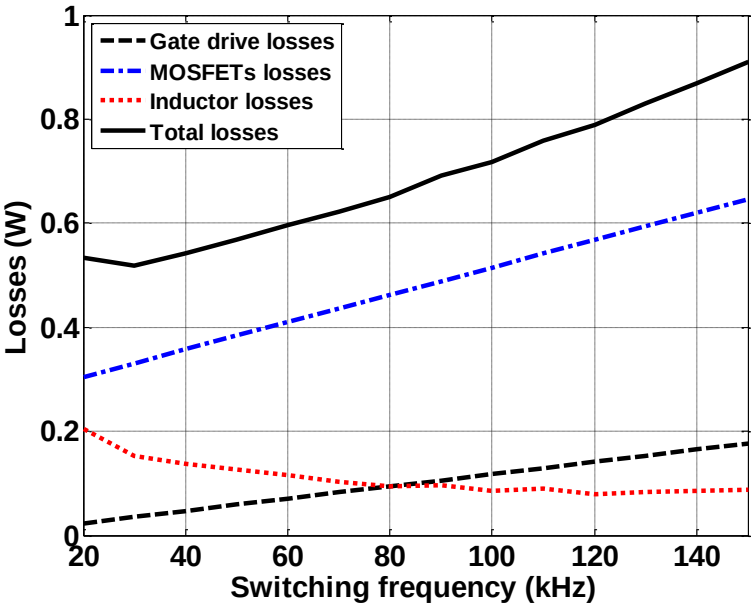
Fig. 6.9 Loss ratio between the propose converter and interleaved converter.

6.4.1. Switching frequencies and component value selection

Having proved that the proposed converter can achieve better performance, one now has to select the main PM switching frequency f_{sm} and ripple current ΔI_m ($\leq$ 3 A) to achieve the highest efficiency. The main PM inductor losses with f_{sm} between 20 kHz to 150 kHz and ΔI_m between 1 A and 3 A when operating under full load condition are calculated from (5.3) and (B1) and are plotted in Fig. 6.10 (a). Results show that the inductor losses reduce gradually with an increase in f_{sm} and also with larger ΔI_m. One would usually expect the inductor losses to be a continuous function of frequency for a single core size, however, the curves presented in Fig. 6.10 (a) were generated using different core sizes as determined by the core area loss product inequality, hence the discontinuities observed as the core size changes. For f_{sm} < 70 kHz, ΔI_m of 3 A produces the lowest losses. Combining the inductor losses at $\Delta I_m = 3\ A$ with the gate drive losses in (5.4) and MOSFET losses (i.e. MOSFET switching loss in (5.6), MOSFET conduction loss and diode conduction loss [101]), Fig. 6.10 (b) shows that the lowest losses are produced at f_{sm} = 30 kHz and so this is selected for the main PM. For f_{sm} = 30 kHz, the inductance L_m is calculated by (3.7) to be 27 μH.



(a)



(b)

Fig. 6.10 Main PM calculated losses. (a) Inductor losses (b) Total losses

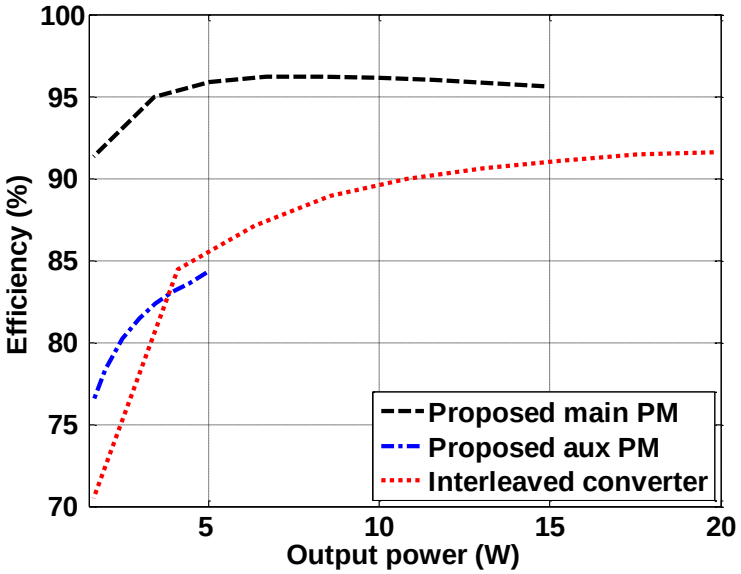
For the auxiliary PM, the inductor L_x is selected so that the current ripple seen by the output capacitor is reduced from 3 A to 1 A. Considering the maximum input voltage $V_{i(max)}$, also inductor tolerance of 10%, the minimum L_x is found by (6.4) to be 8 µH. The minimum f_{sx} that satisfies the

ΔI_x and is m ($m \in \mathbb{Z}^+$) times higher than f_{sm} is calculated by (6.1) to be 360 kHz. The output capacitor that satisfies the overshoot requirement V_{os} is calculated by (4.5) to be 347 µF, 330 µF was therefore selected practically.

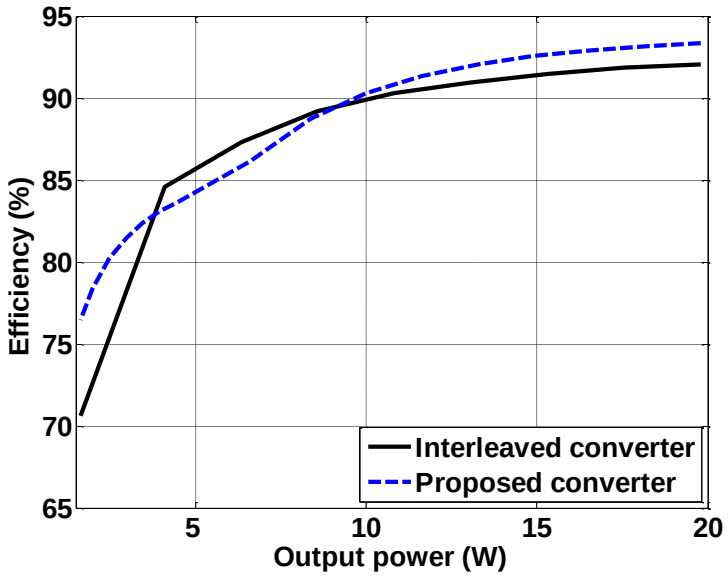
For the interleaved converters, with the ripple attenuation of 37% at interleaved PM duty cycle δ_i = 0.275 [94], the current in each of the interleaved PM, ΔI_i, must be less than 1.6 A in order to produce the net current ripple less than 1 A. With the same capacitance and from (5.1) and (3.7), the minimum interleaved PM switching frequency, f_{si}, that produces the same BW as the proposed converter is 140 kHz. The interleaved PM inductance L_i is calculated from (3.7) to be 12 µH.

The predicted efficiencies of the individual PMs are shown in Fig 6.11 (a) as a function of output power. In order to satisfy the current ripple requirement while achieving high efficiency, both PMs of the proposed converter are active for output powers above 6.5 W. With the auxiliary PM performing the ripple cancellation and processing an average power of 5 W. The main PM processes any remaining power. When the output power is below 6.5 W, only the auxiliary PM is enabled and the converter is operating without ripple cancellation. For the interleaved converter, both PMs are in operation at all times to maintain the current ripple requirement. The phase dropping technique is not implemented [58], as this would increase the output ripple.

The efficiencies of the proposed converter and interleaved converter operating under the conditions described above are shown in Fig 6.11 (b). The results show that the efficiency gain due to the large ΔI_m and loss due to the ripple cancellation produce an efficiency that is higher than that of the interleaved converter under light and heavy load conditions by as much as 6%. The efficiency under mid-range load is about 1.5% lower than that of the interleaved converter.



(a)



(b)

Fig. 6.11 Calculated efficiencies. (a) Efficiencies of the different PMs (b) Efficiencies of the proposed converter and interleaved converter

6.4.2. Prototype converter

The prototype proposed parallel converter is shown in Fig 6.12. A dsPIC33FJGS502 microcontroller is used to generate the two synchronous PWM signal at frequencies of 30 kHz and 360 kHz for the main and auxiliary PMs respectively. It is also used to keep track of the auxiliary PM cycle and set the duty cycles for both PMs. The IRL8113 MOSFET was selected for the two converters due to its low on-state resistance and gate capacitance, and diode DSB20I15PA was also chosen for the auxiliary PM.

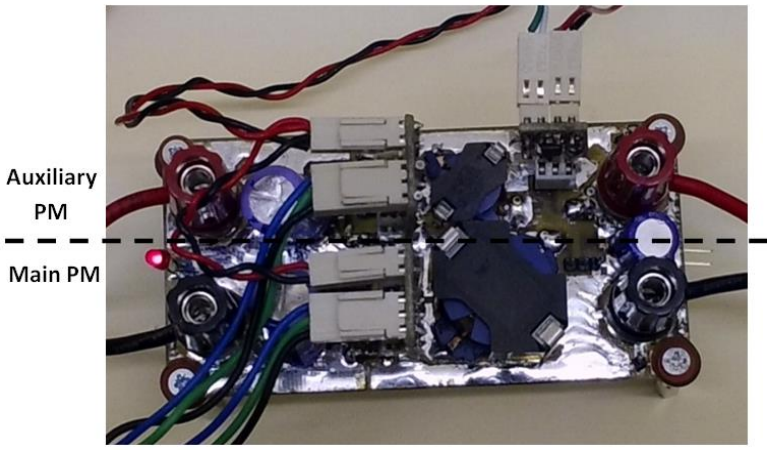
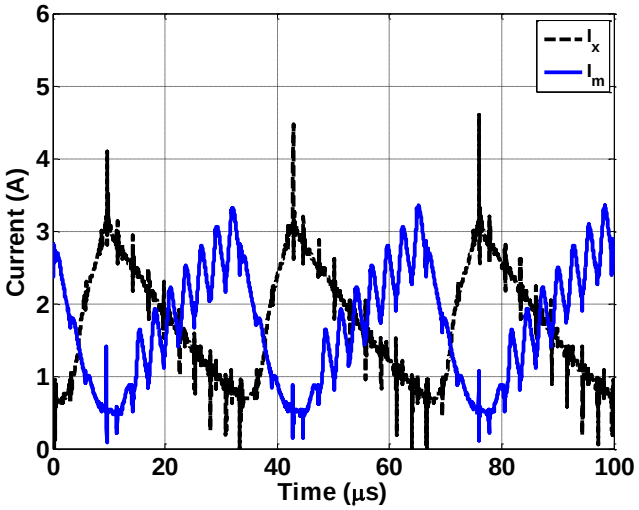


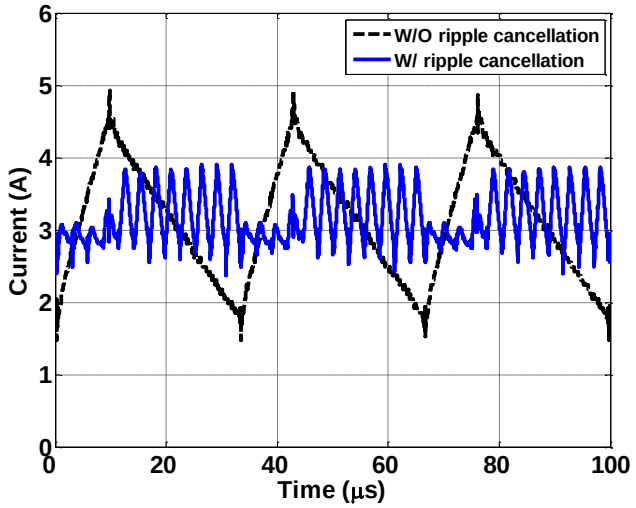
Fig. 6.12 Prototype of the converter with the proposed scheme.

The converter was initially tested at half load with an input voltage of 12 V. The δ_{m} was calculated from (3.5) to be 27.5%. Due to the unaccounted components losses in the PMs, δ_{m} was adjusted to 28.4% for the correct output voltage. With the practical inductances L_{m} and L_{x} of 28 µH and 8 µH respectively, from (6.4), the $\delta_{\mathrm{x}(-)}$ that produced the desired $(d/dt)I_{\mathrm{x(net-)}}$ is calculated to be 7.9% and from (6.5), the $\delta_{\mathrm{x}(+)}$ that produces the desired $(d/dt)I_{\mathrm{x(net+)}}$ is calculated to be 36.5%. Due to the extra current from the auxiliary PM (i.e.$(1-\alpha)I_{\mathrm{o}}$, see Appendix A), the δ_{m} is reduced to 28%, or with a gain of 0.986. As the losses affect the $\delta_{\mathrm{x}(-)}$ and $\delta_{\mathrm{x}(+)}$ similarly, they are recalculated with the gain to be 7.8% and 36.0% respectively. The practical values of $\delta_{\mathrm{x}(-)}$ and $\delta_{\mathrm{x}(+)}$ used are 5% and 35.8% respectively.

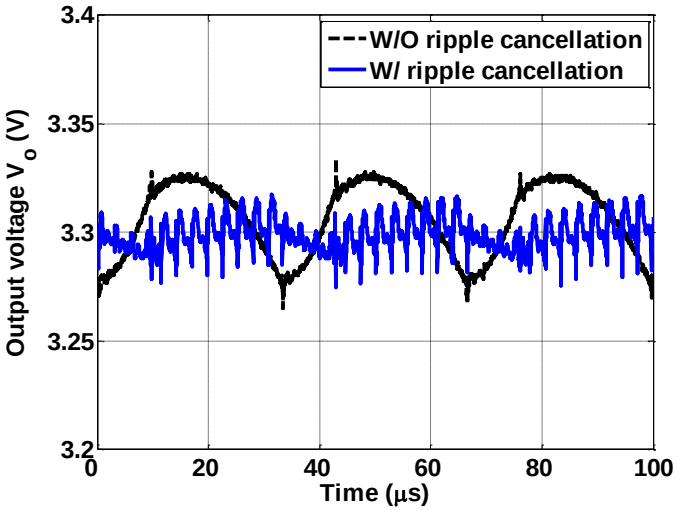
The current waveforms of the two PMs of the converter with the proposed scheme are shown in Fig. 6.13 (a). The output currents and voltages with the above duty cycles, operating with and without ripple cancellation, are shown in Fig. 6.13 (b) and (c) respectively. After the ripple cancellation, the peak to peak current ripple of 3 A is reduced to 1 A as shown in Fig. 6.13 (b) and the output voltage ripple is reduced from 50 mV to 30 mV as shown in Fig 6.13 (c).



(a)



(b)



(c)

Fig. 6.13 Prototype output current and voltage waveforms with and without ripple cancellation. (a) Main and auxiliary PMs current waveforms (b) Output current waveforms (c) Output voltage waveforms

The system was then further tested with the input voltage changed from 12 V to 13.2 V and the load condition increased from the half load condition to full load condition. When the input is increased to 13.2 V, the δ_{m} is increased to 24.9%, or with a gain k_{c} of 0.890. The $\delta_{\mathrm{x}(-)}$ and $\delta_{\mathrm{x}(+)}$ are recalculated with the gain to be 4.5% and 31.9% respectively. The practical values used for the $\delta_{\mathrm{x}(-)}$ and $\delta_{\mathrm{x}(+)}$ are 3.4% and 32.4% respectively. When doubling the load current, to compensate for the extra voltage drop across components, the δ_{m} is increased to 28.6%, or with a gain of 1.021, the $\delta_{\mathrm{x}(-)}$ and $\delta_{\mathrm{x}(+)}$ are recalculated to be 5.1% and 36.6% respectively, the practical value for the $\delta_{\mathrm{x}(-)}$ and $\delta_{\mathrm{x}(+)}$ are 5.3% and 36.2% respectively. The duty cycles for the two PMs at different input voltages and load conditions are summarised in Table 6.1.

	W/O ripple cancellation		W/ ripple cancellation					
	V_i = 12 V, I_o = 3 A		V_i = 12 V, I_o = 3 A		V_i = 13.2 V, I_o = 3 A		V_i = 12 V, I_o = 6 A	
	Calculated	Practical	Calculated	Practical	Calculated	Practical	Calculated	Practical
δ_m	0.275	0.284	0.275	0.280	0.249	0.249	0.286	0.286
δ_{x-}	0.000	0.000	0.078	0.050	0.045	0.034	0.051	0.053
δ_{x+}	0.000	0.000	0.360	0.358	0.319	0.324	0.366	0.362

Table 6.1 Summaries of the duty cycles at different input voltages and load currents.

The efficiency with V_{i} = 12 V across the different load conditions was measured using a bespoke calorimeter (see Appendix C) and is shown in Fig 6.14. The measured efficiencies of the two converters are about 3% lower than the calculated due to the unaccounted losses. The efficiency of the proposed converter operating under light and heavy load conditions is more efficient then the interleaved converter confirming the findings of the analysis presented earlier, with the improvement as high as 5% dependent on the load. At the mid-range load the efficiency of the proposed system is only 0.5% lower than the interleaved converter.

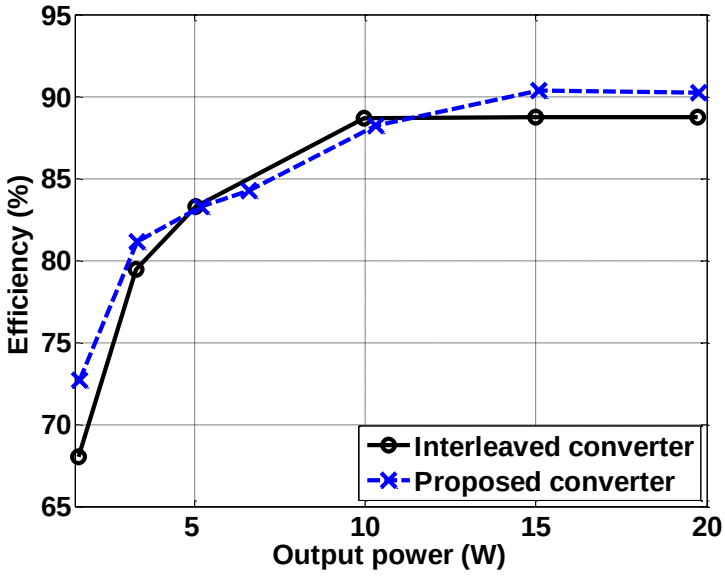


Fig. 6.14 Measured efficiency of the proposed and interleaved converters.

6.5. Summary

This chapter has demonstrated a design and control technique for achieving higher efficiency in a parallel converter and shown how they can be designed to reduce the current ripple seen by the filter capacitor. The analysis has shown that by allowing the current ripple cancellation to be handled by the auxiliary PM operating at a higher frequency, both switching and conduction losses in the main PM can be reduced. Using a 20 W converter as an example, predictions show efficiency improvements over the interleaved converter of up to 6% are achievable under light and heavy load conditions and efficiency in the mid-range is only slightly lower. Experimental measurements taken on a prototype converter confirm this trend with the mid-range load efficiencies only dropping by 0.5%. This chapter also shows that non-identical PMs can be used for ripple cancellation, provided that the selected auxiliary PM inductor can produce a higher net rate of change of inductor current than the rates of the current ripple. Using the equations in section 6.2 and 6.3, the current ripple seen by the filter capacitor is successfully reduce from 3 A to 1 A under different input voltages and load conditions. The proposed converter design technique also works for other power rating and the ripple cancellation technique can reduce the current ripple to a smaller amplitude.

7. LLC resonant converter with capacitor-diode clamp

7.1. Introduction

The previous four chapters have described the control schemes and design techniques through which the efficiencies of the hard-switching converter can be improved, this chapter addresses the overloading issue of the high efficiency LLC resonant converter. A new fundamental harmonic approximation (FHA) based equivalent circuit model for LLC resonant converters with capacitor-diode clamp is obtained through the application of describing function techniques, and by examining the fundamental behaviour of the capacitor-diode clamp. Using the new circuit model, a new design methodology for achieving the best current limiting characteristics is proposed. A prototype 90 W ($\boldsymbol{V_o}$ = 36V, $\boldsymbol{I_o}$ = 2.5 A) LLC converter is designed using the proposed methodology and comparisons of the voltage gain and the voltage-current characteristics under different overload conditions and operating frequencies are presented to show the performance of the proposed model.

7.2. Circuit operation

The circuit diagram of a half-bridge LLC resonant converter is shown in Fig. 7.1. It consists of three main functional parts:

(i) a DC chopper formed by two complementary switched MOSFETs S_1 and S_2, converting the DC input voltage, V_{i}, into a square waveform of frequency f_{s} (n.b. D_{s1} and D_{s2} are the body diodes of the MOSFETs which are critical for ZVS),

(ii) a resonant tank formed by resonant inductors and capacitor L_{p}, L_{s}, C_{r} allowing the fundamental component of the square waveform to pass through,

(iii) a transformer, bridge rectifier and output filter formed by diodes $D_1 - D_4$ and capacitor C_{o}, converting the AC waveform produced in (ii) into the isolated DC output.

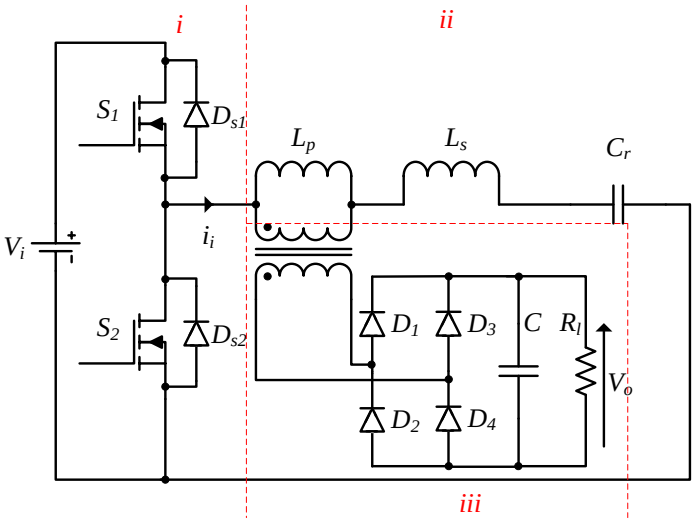


Fig. 7.1 Half-bridge LLC resonant converter.

The typical gain characteristics of a LLC resonant converter under different load conditions (i.e. Q) are shown in Fig. 7.2. Figure shows that at the load independent point (LIP), the nominalised gain curves remain at unity irrespective to the load conditions. This is a major issue where destructive current can flow through the converter.

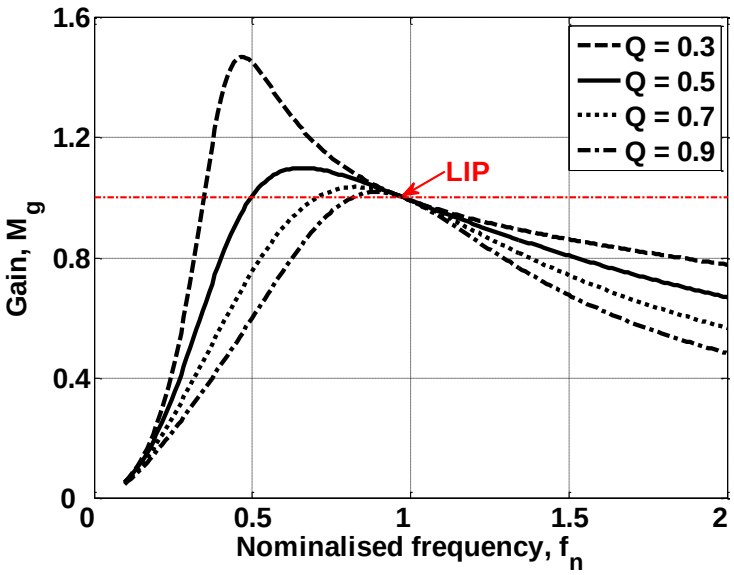


Fig. 7.2 Gain characteristics of LLC converter under different conditions.

A previous approach [82] has split the resonant capacitor into two which are then clamped by clamping diodes. The approach proposed in this chapter splits the resonant capacitor into the

clamped portion (as in [82]) and a non-clamped portion, to allow the desired clamping characteristic to be obtained. A half-bridge LLC resonant converter with the proposed capacitor-diode clamp is shown in Fig. 7.3, the resonant capacitor is split into $2C_c$ and C_s, and containing one extra functional part (iv):

(iv) diodes D_{c1} and D_{c2} which clamp the voltage, V_c, to the input voltage rail under high-current operation.

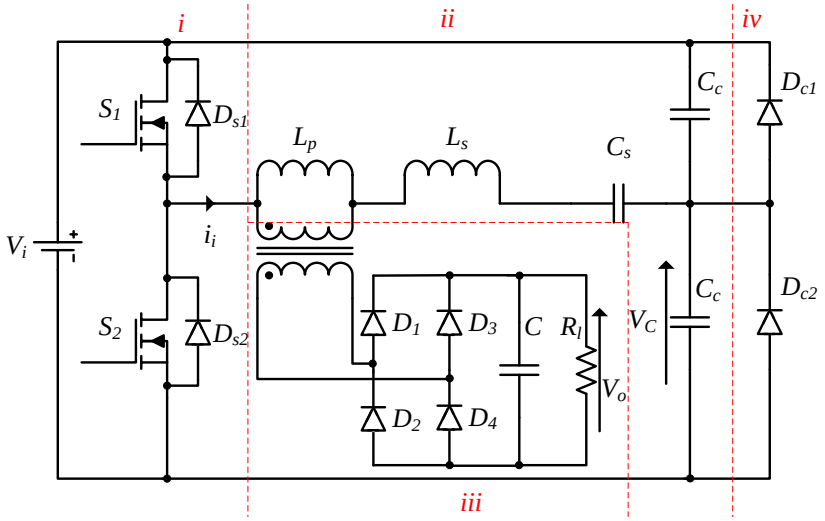


Fig. 7.3 Half-bridge LLC resonant converter with capacitor-diode clamp.

Under normal operation (i.e. below what is termed the current limit), the capacitor common point voltage V_c operates within the two clamping voltage levels, 0 and V_i, as shown in Fig. 7.4 (a). Since the clamping diodes D_{c1} and D_{c2} do not conduct during the switching period and the circuit can be simplified to Fig. 7.5 (a), thus the two capacitors, C_c, are effectively connected in parallel such that $2C_c$ is connected in series with C_s which together form the resonant capacitor C_r found in the standard LLC resonant converter. With these capacitors, C_s can be found by (7.1):

$$C_s = (2C_cC_r)/(2C_c - C_r) \tag{7.1}$$

The range of C_s, and hence C_c, is controlled by the capacitance sharing ratio B_s as given in (7.2). The capacitance sharing ratio can take on values in the range $0 \leq B_s \leq 1$, with $B_s = 1$ being the

extreme where no capacitance is clamped by the diodes D_{c1} and D_{c2} and $B_s = 0$ being where the whole resonant capacitor is clamped. The effect of the capacitor ratio B_s to the current limiting performance will be detailed in section 7.4.

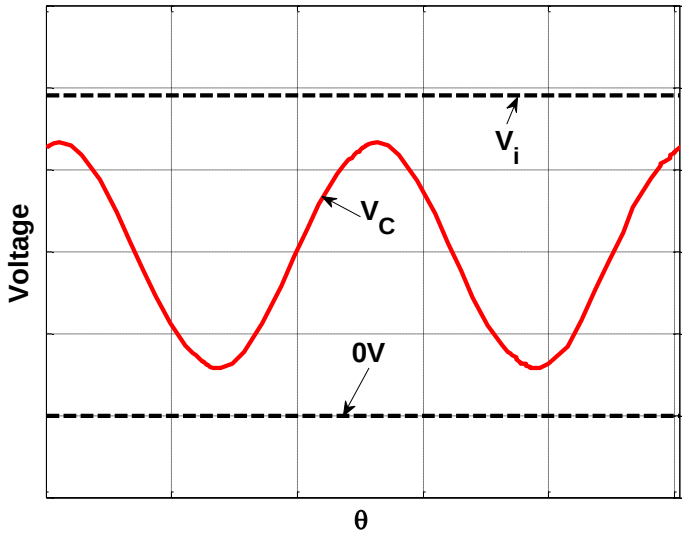
$$B_s = \frac{C_r}{C_s} \tag{7.2}$$

Under overload condition (i.e. the pre-designed load current is exceeded), the diode-clamp becomes active since V_c exceeds the input voltage rail, causing D_{c1} and D_{c2} to conduct momentarily, this has the effect of reducing the circuit's resonant frequency. Under this condition there is an apparent increase in the switching frequency to resonant frequency ratio that has the effect of reducing the current flow in the circuit. The conduction state for each clamping diode can be determined as follows:

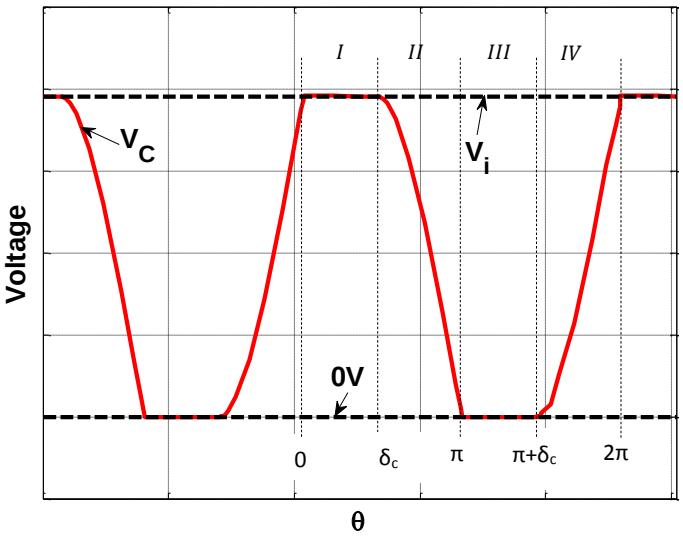
1) D_{c1} conducts when $V_c > V_i$, clamping V_c to V_i

2) D_{c2} conducts when $V_c < 0\ V$, clamping V_c to $0\ V$

In either case the clamping diode ceases conduction when the resonant circuit input current $I_i = 0$ A. When the diode clamp is inactive V_c takes on a cosinsoidal shape, assuming the resonant circuit current is sinusoidal. The quasi cosine-square waveform of V_c under current-limited operating conditions is shown in Fig. 7.4 (b), with the diode clamp conduction states 1) and 2) described above found in intervals II and IV respectively and diode clamp non-conduction states in intervals I and III. The sub-circuits for the converter with D_{c1} and D_{c2} conducting are shown in Fig. 7.5 (b) and (c) respectively.

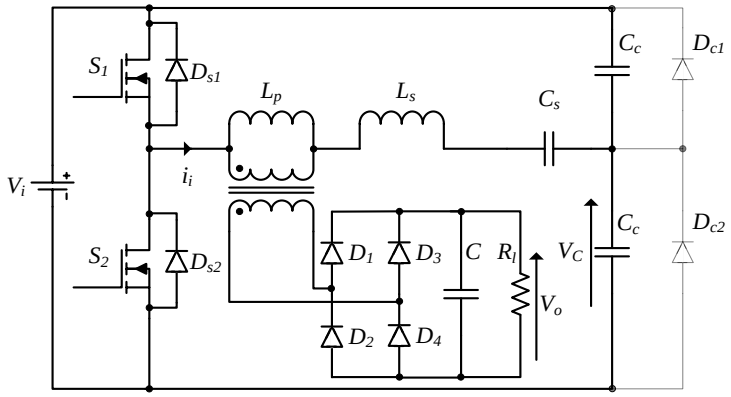


(a)

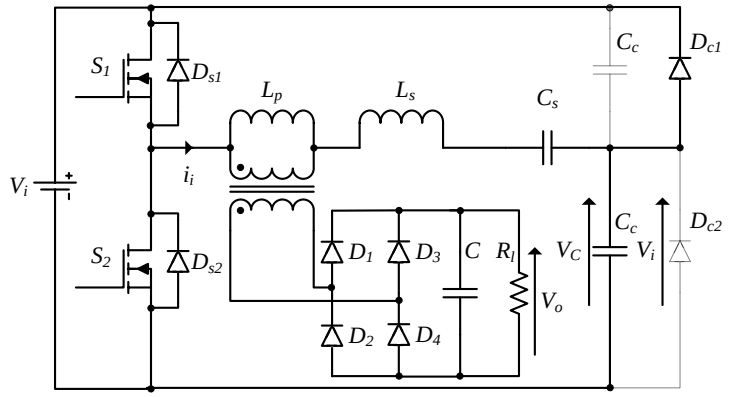


(b)

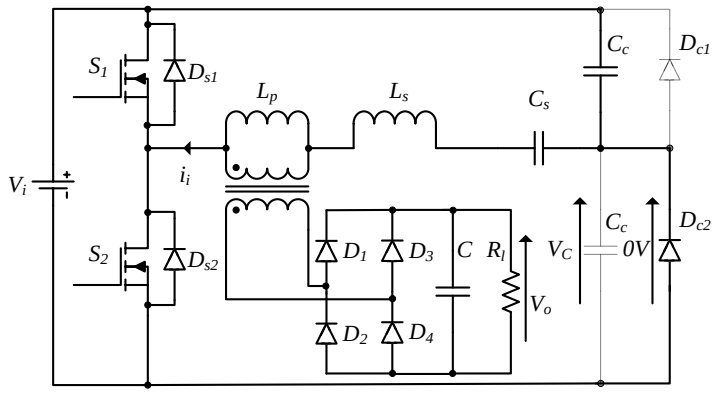
Fig. 7.4 Resonant capacitor voltage waveforms. (a) normal operation and (b) overloading operation



(a)



(b)



(c)

Fig. 7.5 Equivalent circuit under different diode-clamp conduction states. (a) diode clamp inactive (b) conduction state 1 $\delta_c < \theta \leq \pi$ (c) conduction state 2) $\pi + \delta_c < \theta \leq 2\pi$

7.3. Equivalent circuit model

When the diode-clamp is inactive, the static behaviour of the converter can be predicted using a variety of methods, including fundamental harmonic approximation (FHA) [102], describing function [103] and state-plane techniques [104] depending on the required modelling accuracy. Although the methods presented in [103] and [104] can predict the static behaviours more accurately across a wide range of switching frequencies, they can be difficult to use when multiple operating modes are encountered and therefore the equivalent circuit models derived here are based on FHA which has been shown to provide reasonable prediction accuracy when the converter is operating in the vicinity of the load independent point [105].

With FHA one assumes the resonant current can be approximated to a sinusoidal current since the resonant circuit operates similar to a band-pass filter responding only to the fundamental component of the input voltage and attenuating the higher frequency components. With this assumption, the input current i_{i} can be defined as in (7.3), with a peak value of I_{i} when the converter is operating at a frequency f_{s}. To simplify the analysis that follows, angles are used to remove the time dependences such that $2\pi f_{\mathrm{s}} t = \theta$:

$$i_{\mathrm{i}} = I_{\mathrm{i}} sin(\omega_{\mathrm{s}} t) = I_{\mathrm{i}} sin(2\pi f_{\mathrm{s}} t) = I_{\mathrm{i}} sin(\theta) \tag{7.3}$$

7.3.1. Diode-clamp inactive

Employing FHA techniques similar to those applied in [73] and [102], the magnitude of the input current (I_{i}) and output voltage (V_{o}) can be calculated using (7.4) and (7.5) respectively (n.b. in the following analysis, the non-ideality of diodes and of components parasitic resistances are neglected).

$$I_{\mathrm{i}} = \frac{2V_{\mathrm{i}}}{\pi Z_1} \tag{7.4}$$

$$V_{\mathrm{o}} = \frac{\pi I_{\mathrm{i}}(R_{\mathrm{eq}}||sL_p)}{4n} \tag{7.5}$$

where $Z_1 = R_{\mathrm{eq}}||sL_{\mathrm{p}} + sL_{\mathrm{s}} + \frac{1}{sC_{\mathrm{s}}} + \frac{1}{2sC_c}$, is the input impedance of the resonant circuit and the load, $s = j\omega_{\mathrm{s}}$, is the complex frequency and $R_{\mathrm{eq}} = \frac{8n^2R_{\mathrm{l}}}{\pi^2}$ is the equivalent resistance presented by the rectifier, output filter and load reflected through a transformer with a primary turns (N_{p}) to secondary turns (N_{s}) ratio $n = N_{\mathrm{p}}/N_{\mathrm{s}}$.

In order to study the converter's general behaviour, irrespective of the resonant tank components selection, the nominalised gain M_{g} is obtained by substituting (7.4) into (7.5), and rearranging in terms of $(2nV_{\mathrm{o}})/V_{\mathrm{i}}$. Applying normalising terms for inductor ratio $A_{\mathrm{s}} = L_{\mathrm{p}}/L_{\mathrm{s}}$, loaded quality factor $Q = \sqrt{L_{\mathrm{s}}/C_{\mathrm{r}}}/R_{\mathrm{eq}}$ and normalised switching frequency (against the series resonant frequency) $f_{\mathrm{n}} = f_{\mathrm{s}}/f_0$ leads to (7.6), allowing the output voltage to be predicted.

$$M_{\mathrm{g}} = \frac{2nV_{\mathrm{o}}}{V_{\mathrm{i}}} = \frac{A_{\mathrm{s}}{f_n}^2}{A_{\mathrm{s}}{f_n}^2+{f_n}^2-1+j({f_n}^3QA_{\mathrm{s}}-f_{\mathrm{n}}QA_{\mathrm{s}})} \tag{7.6}$$

where f_0 is converter resonant frequency.

Further analysis of the equivalent circuit Fig. 7.5 (a) allows one to obtain the peak voltage and current stresses on the components. For example, since the capacitors C_{c} excited by the sinusoidal input current, the capacitor common point voltage as shown in Fig. 7.4 (a), at any given instant can be found using (7.7). The time dependence is removed by substituting $\omega_{\mathrm{s}}t$ for θ (with $\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$ being the angular switching frequency and t is time), the capacitor branch voltage v_{c} as a function of θ is given by (7.8):

$$v_{\mathrm{c}}(t) = \frac{1}{2C_{\mathrm{c}}}\int I_{\mathrm{i}}sin(\omega_{\mathrm{s}}t)\,dt\ = -\frac{I_{\mathrm{i}}}{2\omega_{\mathrm{s}}C_{\mathrm{c}}}cos(\omega_{\mathrm{s}}t) + V_{\mathrm{n}} \tag{7.7}$$

$$v_{\mathrm{c}}(\theta) = -\frac{I_{\mathrm{i}}}{2\omega_{\mathrm{s}}C_{\mathrm{c}}}cos(\theta) + V_{\mathrm{n}} \tag{7.8}$$

where V_{n} is the initial condition for a given conduction state starting at $\theta = n$.

Due to the DC blocking property of capacitors, the DC component of the DC chopper (the half-bridge inverter) is superimposed onto v_c as in (7.9).

$$v_c(\theta) = -\frac{I_i}{2\omega_s C_c} cos(\theta) + \frac{V_i}{2} \tag{7.9}$$

7.3.2. Diode-clamp active

In this section, a describing function is developed to represent the effects of the diode-clamp/capacitor combination by an equivalent impedance Z_c. This impedance is then combined with a FHA analysis similar to that described in the previous section providing a complete model of the converter when the diode-clamp is active (i.e. when operating under overload conditions). Further analysis of the equivalent circuits in Fig. 7.5 (b) and (c), the derivation of Z_c is given in the three steps as follows:

Step 1: a piecewise equation describing the capacitor voltage v_c (Fig. 4 (b)) representing the circuit conduction states is obtained assuming a sinusoidal resonant current

Since there are two intervals during a single cycle when the diode-clamp is inactive, two separate values for the initial condition V_n in (7.8) are needed. In the first interval I $(0 < \theta \leq \delta_c)$, the capacitor voltage, v_c, is zero at $\theta = 0$, by substituting the known quantities in (7.8), the initial condition, V_0, is found in (7.10):

$$0 = -\frac{I_i}{2\omega_s C_c} cos(0) + V_0$$
$$V_0 = \frac{I_i}{2\omega_s C_c} \tag{7.10}$$

For interval, III $(\pi < \theta \leq \pi + \delta_c)$, v_c has been charged to V_i and now begins discharging towards 0 V. By applying similar arguments as before, the initial condition for this interval is also found in (7.11),

$$V_{\mathrm{i}} = -\frac{I_{\mathrm{i}}}{2\omega_{\mathrm{s}}C_{\mathrm{c}}}cos(\pi) + V_{\pi}$$
$$V_{\pi} = V_{\mathrm{i}} - \frac{I_{\mathrm{i}}}{2\omega_{\mathrm{s}}C_{\mathrm{c}}} \tag{7.11}$$

Combining the initial conditions found in (7.10) and (7.11) with (7.8) and accounting for the two clamping levels, the piecewise description of the capacitor voltage is given in (7.12):

$$v_{\mathrm{C}}(\theta) = \begin{cases} \frac{I_{\mathrm{i}}}{2\omega_{\mathrm{s}}C_{\mathrm{c}}}(1 - cos(\theta)) & 0 < \theta \leq \delta_{\mathrm{c}} \\ V_{\mathrm{i}} & \delta_{\mathrm{c}} < \theta \leq \pi \\ V_i - \frac{I_{\mathrm{i}}}{2\omega_{\mathrm{s}}C_{\mathrm{c}}}(1 + cos(\theta)) & \pi < \theta \leq \pi + \delta_{\mathrm{c}} \\ 0 & \pi + \delta_{\mathrm{c}} < \theta \leq 2\pi \end{cases} \tag{7.12}$$

The diode-clamp non-conduction angle, δ_{c}, is found by evaluating the change in capacitor voltage over the diode-clamp non-conduction period. At the end of the first interval, the capacitor voltage has charged from 0 to V_{i}, therefore, substituting $v_{\mathrm{C}}(\delta_{\mathrm{c}}) = V_{\mathrm{i}}$ into (7.12) and rearranging provides,

$$\delta_{\mathrm{c}} = cos^{-1}\left(1 - \frac{2\omega_{\mathrm{s}}C_{\mathrm{c}}V_{\mathrm{i}}}{I_{\mathrm{i}}}\right) \tag{7.13}$$

Step 2: the fundamental component of v_{c} is determined via Fourier analysis

A describing function for v_c is now developed based on the piecewise equation that has just been developed. The Fourier series representation of a repetitive waveform is defined in (7.14) where $f(t)$ is the original time domain signal $v_{\mathrm{c}}(t)$, a_0 is the DC component, a_n & b_n are harmonic components of the waveform and T is the period of one cycle:

$$f(t) = a_0 + \sum_{n-1}^{\infty}\left(a_{\mathrm{n}}cos(n\omega_{\mathrm{s}}t) + b_{\mathrm{n}}sin(n\omega_{\mathrm{s}}t)\right)$$
$$a_0 = \frac{1}{2\pi}\int_{-T/2}^{T/2} f(t)dt \tag{7.14}$$
$$a_{\mathrm{n}} = \frac{1}{\pi}\int_{-T/2}^{T/2} f(t)cos(n\omega_s t)dt$$

$$b_{\mathrm{n}} = \frac{1}{\pi}\int_{-T/2}^{T/2} f(t)sin(n\omega_s t)dt$$

For AC equivalent circuit analysis, the DC component, a_0, is ignored and since the converter's behaviour is dominated by the fundamental component, the Fourier series can be simplified to a describing function as shown below:

$$f(\theta) = a_1 cos(\theta) + b_1 sin(\theta)$$

$$a_1 = \frac{1}{\pi}\int_0^{2\pi} f(\theta)cos(\theta)d\theta \tag{7.15}$$

$$b_1 = \frac{1}{\pi}\int_0^{2\pi} f(\theta)sin(\theta)d\theta$$

By substituting (7.12) into (7.15) the fundamental component of v_{c} is:

$$v_{\mathrm{C}}(\theta) = \left[\frac{2}{\pi}V_{\mathrm{i}}\cos(\delta_{\mathrm{c}}) + \frac{I_{\mathrm{i}}}{2\pi\omega_{\mathrm{s}}C_{\mathrm{c}}}\left(1 + \cos(\delta_{\mathrm{c}})\left(\cos(\delta_{\mathrm{c}}) - 2\right)\right)\right]\sin(\theta)$$
$$+\left[-\frac{2}{\pi}V_{\mathrm{i}}\sin(\delta_{\mathrm{c}}) - \frac{I_{\mathrm{i}}}{2\pi\omega_{\mathrm{s}}C_{\mathrm{c}}}\left(\delta_{\mathrm{c}} + \sin(\delta_{\mathrm{c}})(\cos(\delta_{\mathrm{c}}) - 2)\right)\right]\cos(\theta) \tag{7.16}$$

Step 3: an equivalent impedance for diode-clamp/capacitor combination is found by dividing the expression obtained in step 2 by the sinusoidal input current $i_{\mathrm{i}} = I_{\mathrm{i}}sin(\theta)$

The equivalent impedance of the diode-capacitor combination is obtained by applying the transform $cos(\theta) = jsin(\theta)$ and then dividing by resonant current as follows:

$$Z_{\mathrm{C}} = \left[\frac{2V_{\mathrm{i}}}{\pi I_{\mathrm{i}}}\cos(\delta_{\mathrm{c}}) + \frac{1}{2\pi\omega_{\mathrm{s}}C_{\mathrm{c}}}\left(1 + \cos(\delta_{\mathrm{c}})\left(\cos(\delta_{\mathrm{c}}) - 2\right)\right)\right]$$
$$+j\left[-\frac{2V_{\mathrm{i}}}{\pi I_{\mathrm{i}}}\sin(\delta_{\mathrm{c}}) - \frac{1}{2\pi\omega_{\mathrm{s}}C_{\mathrm{c}}}\left(\delta_{\mathrm{c}} + \sin(\delta_{\mathrm{c}})(\cos(\delta_{\mathrm{c}}) - 2)\right)\right] \tag{7.17}$$

By substituting Z_c into the FHA model provides (7.18) where the effect of the diode-clamp is accounted for allowing the magnitude of the resonant tank current under clamping (i.e. overload) to be found. The output voltage can be found by substituting (7.18) into (7.5).

$$I_i = \frac{2V_i}{\pi Z_2} \tag{7.18}$$

where $Z_2 = R_{eq}||sL_p + sL_s + \frac{1}{sC_s} + Z_c$, which s and R_{eq} are as defined in previous section.

7.3.3. Diode-clamp conduction point

Since (7.18) cannot be solved analytically owing to the dependence on I_i for determining both δ_c and Z_c, an iterative procedure similar to that employed in [88] is used: the value for the resonant tank current is first estimated using (7.4) by assuming the diode-clamp is inactive. Once a value for I_i has been obtained, the non-conduction angle, δ_c, and capacitor-diode clamp equivalent impedance, Z_c, are found by (7.13) and (7.17), after which a refined value for I_i is found by (7.18). The refinement of δ_c, Z_c and I_i are achieved through an iterative loop, flowchart shown in Fig. 7.6, where a new value for the current $I_i[k+1]$ is reapplied to (7.13) and (7.17) until they converge. To ensure satisfactory convergence, a damping factor α_d should be used to determine the new resonant tank current value, $I_i[k+1]$, in a similar manner to the technique commonly employed with Newton's method [106].

$$I_i[k+1] = I_i[k] + \alpha_d(I_{DC}[k+1] - I_i[k]) \tag{7.19}$$

where $I_i[k+1]$ and $I_i[k]$ is the new value and old value of resonant tank current respectively, $I_{DC}[k+1]$ is the present refined resonant tank current predicted by (7.18) and α_d is the damping factor with a value between 0 and 1.

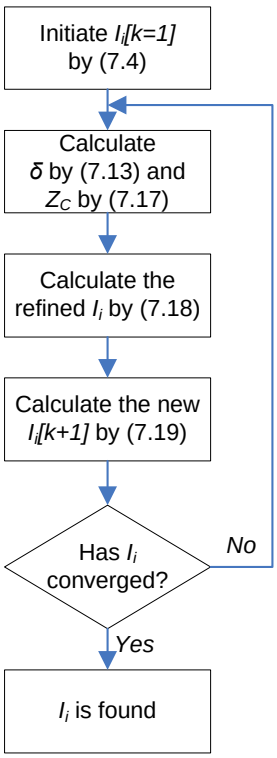


Fig. 7.6 Flowchart describing the interactive procedure for finding the load current during overloading conditions (i.e. $V_c > V_i$).

7.3.4. Nominalised gain with active diode-clamp

Similar to the inactive diode-clamp case (i.e. normal non-current limited operation), the converter gain with an active diode-clamp, $M_{g(clmp)}$, is obtained by substituting (7.18) into (7.5) and rearrange in terms of $(2nV_o)/V_i$ as in (7.20), after which substituting $s = j\omega$, using $Z_c = R + jX$ (where R and X are the real and imaginary part of Z_c in (7.17) respectively), and introducing the $j\omega C_r$ term into both the numerator and denominator as in (7.21):

$$M_{g(clmp)} = \frac{V_o}{V_i}2n = \frac{R_{eq}||sL_p}{R_{eq}||sL_p+sL_s+\frac{1}{sC_s}+Z_c} \tag{7.20}$$

$$M_{g(clmp)} = \frac{j^2\omega^2 L_p C_r}{j^2\omega^2 L_p C_r+\frac{j^3\omega^3 L_s L_p C_r}{R_{eq}}+j^2\omega^2 L_s C_r+\frac{j\omega L_p C_r}{C_s R_{eq}}+\frac{C_r}{C_s}+\frac{j^2\omega^2 R L_p C_r}{R_{eq}}+Rj\omega C_r+\frac{j^3\omega^2 C_r X L_p}{R_{eq}}+j^2 X\omega C_r} \tag{7.21}$$

The final step involves substituting the following normalising factors $L_p = A_s L_s$, $L_s C_r = 1/{\omega_0}^2$, $L_s/R_{eq} = Q/\omega_0$, $f_n = \omega/\omega_0$ and $B_s = C_r/C_s$, to obtain:

$$M_{g(clmp)} = \frac{{f_n}^2 A_s}{{f_n}^2 A_s + {f_n}^2 - B_s + k_{re} + j({f_n}^3 A_s Q - f_n A_s Q B_s + k_{im})} \tag{7.22}$$

where $k_{re} = \omega C_r(f_n A_s Q R + X)$ and $k_{im} = \omega C_r(-R + f_n A_s Q X)$, are terms accounting for the change in the effective impedance of the C_c caused by the diode-clamp when it is active and it is assumed that the values for R and X have converged.

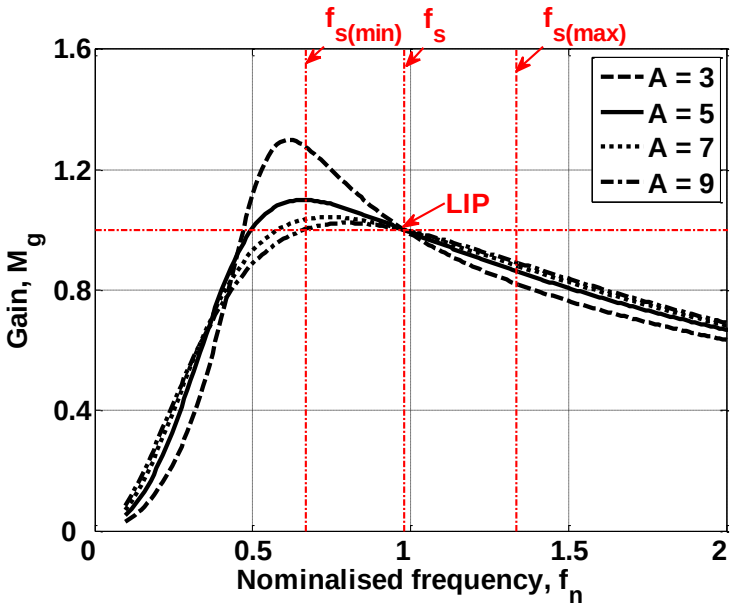
Without the diode-clamp (i.e. normal operation), $R = 0$, and B_s can either be zero (i.e. $C_c = 0.5C_r$) or one (i.e. $C_s = C_r$,). When $B_s = 0$, $X = -\frac{1}{2\omega C_c}$, $k_{re} = -1$ and $k_{im} = -f_n A_s Q$, and when $B_s = 1$, $X = 0$ $k_{re} = 0$ and $k_{im} = 0$. In both cases, (7.22) can be simplified to (7.6).

7.4. Analysis of converter operating characteristic

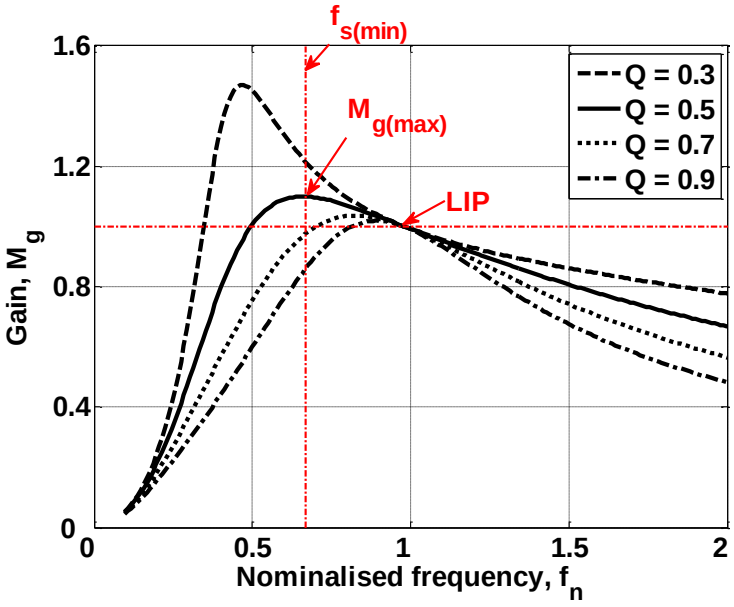
Before giving detailed discussion on the characteristic of the capacitor-diode clamp, the converter operating under normal non-overload conditions is briefly described.

Assuming the capacitor-diode clamp has been designed such that it only becomes active when the load current exceeds the maximum rated load current, the converter can be treated as standard LLC resonant converter up to the maximum load condition. When the standard LLC converter is operated at the series resonant frequency, f_0, its voltage gain, M_g, is fixed and is unaffected by changes in the load (i.e. operation at the LIP). Thus, one popular method for designing LLC converters [102][107] is to select the transformer turn ratio, *n*, such that the voltage gain at the series resonant frequency under the nominal operating condition is unity, $M_g(f_0) = 1$. The resonant tank components are then selected through the normalised variables A_s and Q using (7.6) to accommodate the M_g requirement for changes in the input voltage over a given frequency range. In practice small changes in frequency are also required to compensate for inevitable voltage drops caused by changes in the load.

With the nominal input voltage, $V_{\mathrm{i(nom)}}$, at the LIP, the converter gain from (7.6) with inductor ratio $3 \leq A_{\mathrm{s}} \leq 9$ and load $0.3 \leq Q \leq 0.9$ are plotted in Fig. 7.7 (a) and (b) respectively. Fig. 7.5 (a) shows that smaller A_{s} values lead to higher gain while Fig. 7.7 (b) shows that smaller Q values lead to higher gain. If A_{s} is selected to be 5, the maximum Q that satisfies the gain requirement, $M_{\mathrm{g(max)}}$, can be identified with Fig. 7.7 (b). The $f_{\mathrm{s(min)}}$ and $f_{\mathrm{s(max)}}$ in Fig. 7.7 are the minimum and maximum frequencies the converter used for the line and load regulations.



(a)



(b)

Fig. 7.7 Converter gain characteristics. (a) $Q = 0.5$, $3 \leq A_{\mathrm{s}} \leq 9$ (b) $0.3 \leq Q \leq 0.9$, $A_{\mathrm{s}} = 5$

Since $Q = \sqrt{L_s/C_r}/R_{eq}$, changing Q is equivalent to changing in load resistance R_{eq}, or load condition, the gain curves under overload conditions can be studied through the nominalised Q-factor, Q_n, as calculated by (7.23). For example, assuming A_s is selected to be 5 and the Q-factor under the rated load condition, Q_{rate}, is 0.3, gain curve with Q = 0.9 equals to Q_n = 3, representing three times overloading.

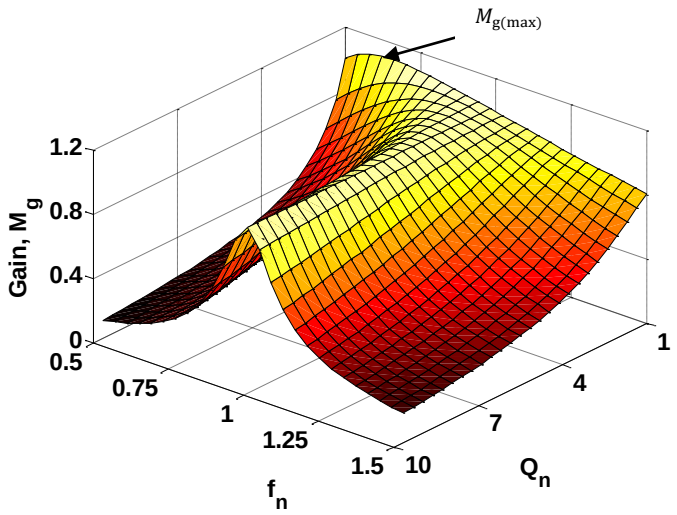
$$Q_n = \frac{Q}{Q_{rate}} \tag{7.23}$$

7.4.1. Capacitor diode-clamp characteristics

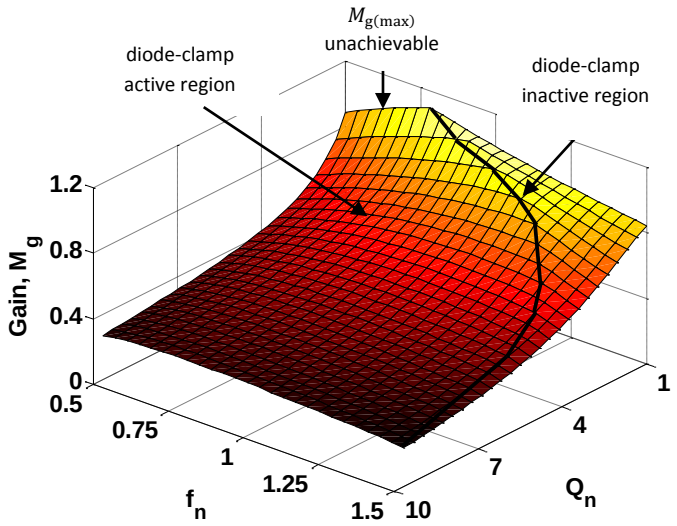
This section compares voltage gain under normal and overload conditions when operating in the vicinity of LIP.

In the case where the diode-clamp is inactive, with $A_s = 5$ and $Q_{rate} = 0.5$, the converter voltage gain characteristic for $1 \leq Q_n \leq 10$ and $0.5 \leq f_n \leq 1.5$ is calculated using (7.6) and is plotted in Fig. 7.8 (a). As expected there is little change in the gain around the LIP ($f_n = 1$) for increasing Q_n.

Assuming all of the resonant capacitor (calculated for the above A_s and Q_{rate}) is now split into the two clamping capacitors $C_c(= 1/(2C_r))$ and is clamped by D_{c1} and D_{c2} to the input voltage under overload, the voltage gain $M_{g(clmp)}$ under the same f_n and Q_n range is calculated by (7.22) and is plotted in Fig. 7.8 (b). For each operating points, k_{re} and k_{im} are calculated by the procedure highlighted in Fig. 7.6. The results show that in the diode-clamp inactive region (to the right of the diode-clamp active-inactive boundary solid black line), the gain is unaffected, whereas in the diode-clamp active region the gain around the LIP ($f_n = 1$) is dramatically reduced for increasing Q_n and thereby reducing the current that would otherwise flow under overloading conditions. Fig. 7.8 (b) also shows the peak gain at $f_n = 0.6$ is reduced below the required $M_{g(max)}$, and so load regulation at the rated load ($Q_n = 1$) may no longer be achievable with low input voltages.



(a)



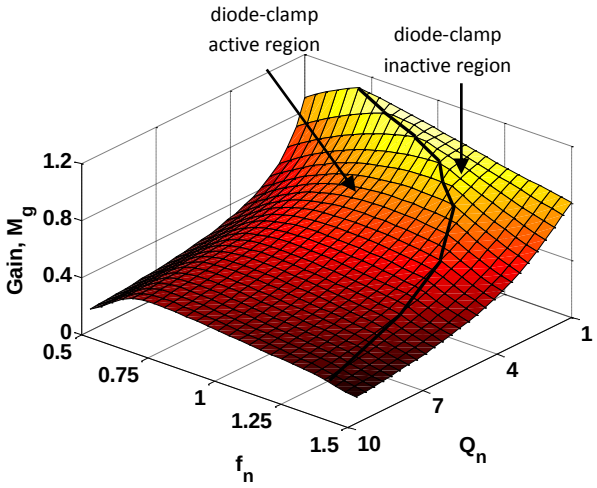
(b)

Fig. 7.8 Converter gain characteristics with A_s = 5 and Q_{rate} = 0.5. (a) B_s = 1 and (b) B_s = 0

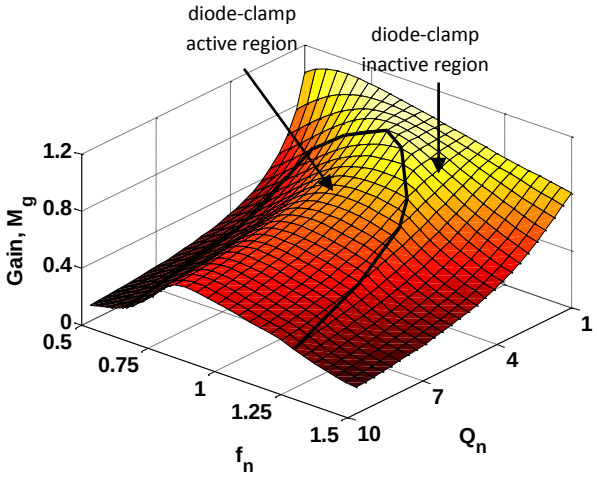
Therefore, to retain regulation (that is to achieve the required $M_{g(max)}$) for the rated load condition, the diode-clamp active region must be reduced. This can be achieved by increasing C_c, by choosing a larger value for B_s, which reduces the voltage V_c for the same load current and, thus, a larger current is required to activate the diode-clamp.

Using (7.22) the voltage gain characteristic with B_s of 0.25, 0.5 and 0.75 are plotted in Fig. 7.9 (a), (b) and (c) respectively. The figures show that as B_s increases, the diode-clamp active region reduces. For $B_s \geq 0.5$, the $M_{g(max)}$ is retained for this particular example, allowing normal

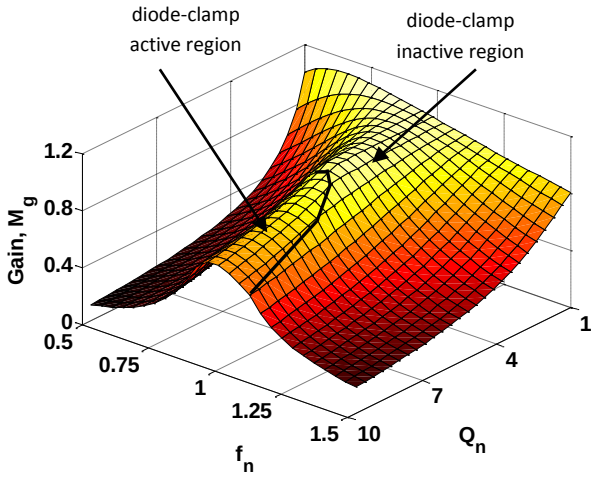
regulation at the full rated load condition. The penalty with the higher B_s is the diode-clamp becomes less effective at reducing the voltage gain, hence overload current.



(a)



(b)



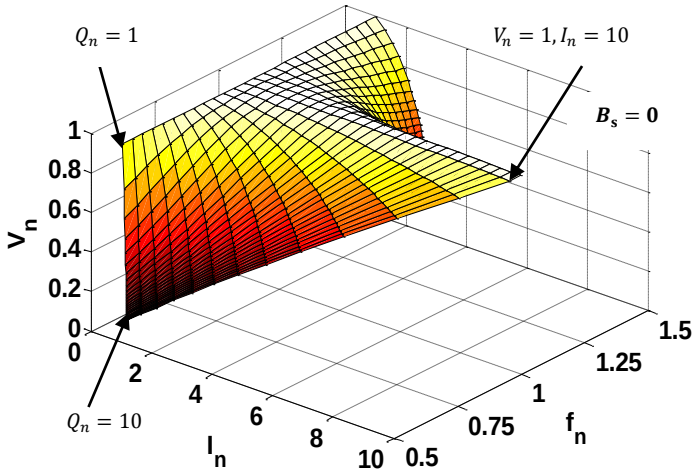
(c)

Fig. 7.9 Converter gain characteristics with A_s = 5 and Q_{rate} = 0.5. (a) B_s = 0.25 (b) B_s = 0.5 (c) B_s = 0.75

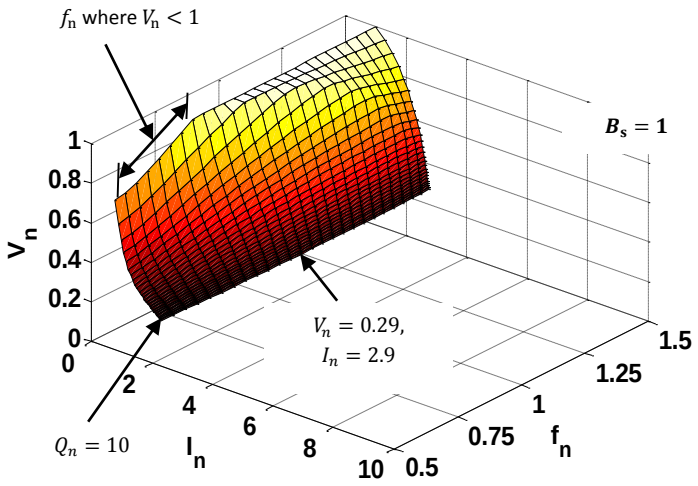
The design task involves the selection of the lowest B_s that retains the $M_{g(max)}$ operating point while providing the current-limiting action when operating with overload conditions ($Q_n > 1$).

7.4.2. Converter Voltage-Current (VI) characteristics

To illustrate how the reduction in voltage gain by the action of diode-clamp leads to the reduction in overload current, the converter voltage gain M_g under different Q_n and f_n, for the different B_s, are first normalised against the unclamped rated full load gain (i.e. $B_s = 1$, $Q_n = 1$) at the corresponding frequency f_n, after which the converter normalised output voltage V_n and normalised current I_n for $1 \leq Q_n \leq 10$ are calculated and plotted in Fig. 7.10 (a)-(e).

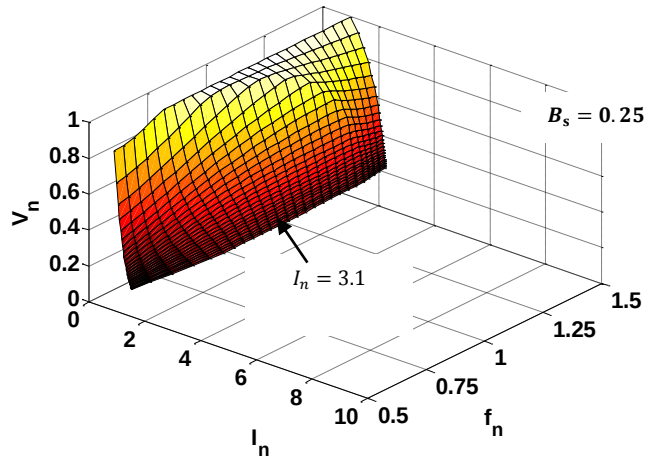


(a)

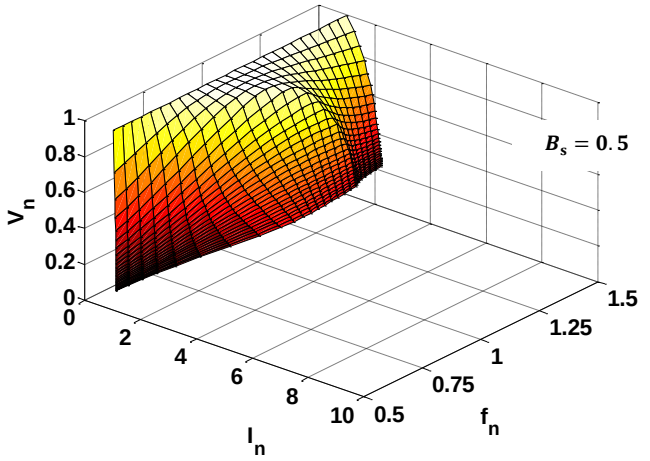


(b)

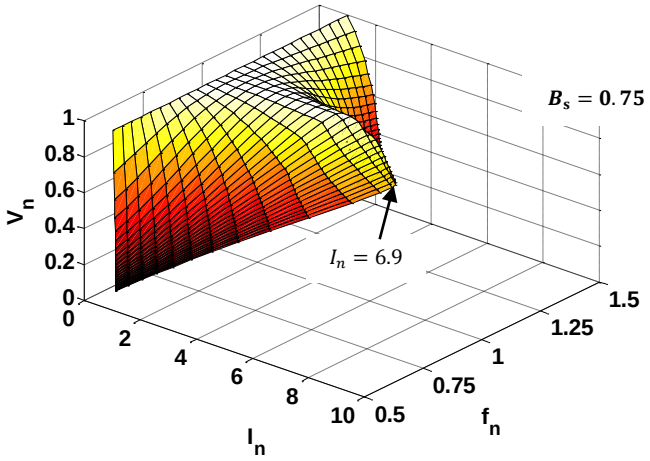
Fig. 7.10 Converter VI characteristics. (a) $B_s = 1$ (b) $B_s = 0$



(c)



(d)



(e)

Fig. 7.10 Converter VI characteristics. (a) B_s = 1 (b) B_s = 0 (c) B_s = 0.25 (d) B_s = 0.5 (e) B_s = 0.75

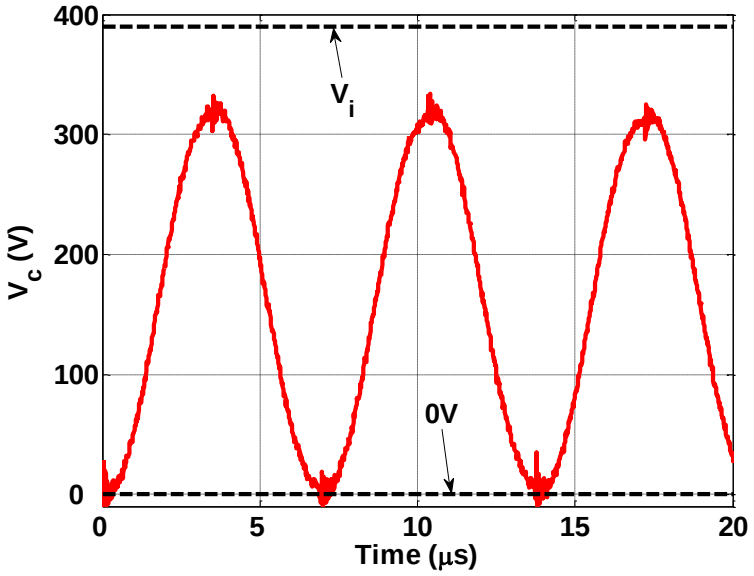
Fig. 7.10 (a) shows operation with no clamping action (B_s = 1), the voltage V_n at the LIP for different values of Q_n is unaffected and is equal to unity as expected. Thus, ten times overloading ($Q_n = 10$) leads to ten times increase in the current I_n when operating at $f_n = 1$. Fig. 7.8 (b) shows that with the resonant capacitance fully clamped (B_s = 0), the reduction in $M_{g(clmp)}$ by the diode-clamp in Fig. 7.8 (b) leads to the reduction of V_n to 0.29, and I_n to 2.9 (at the LIP with $Q_n = 10$). The figure also shows there is a range of f_n where the $V_n < 1$. This means regulation is not achievable for low input voltages as discussed in section 7.4.1. The $V_n I_n$ characteristic for B_s = 0.25, 0.5 and 0.75 are plotted in Fig. 7.10 (c), (d) and (e) respectively. Fig. 7.10 (d) and (e) show that for $B_s \geq 0.5$, regulation is achieved at all f_n. Comparing Fig. 7.10 (c) to (e), the I_n at the LIP with $Q_n = 10$ is increased from 3.1 to 6.9, showing the reduction in the effectiveness diode-clamp to reduce the current as B_s increases. Fig. 7.10 shows that with a suitably chosen value for B_s the overload current can be limited without the need for any external control action.

7.5. Design example

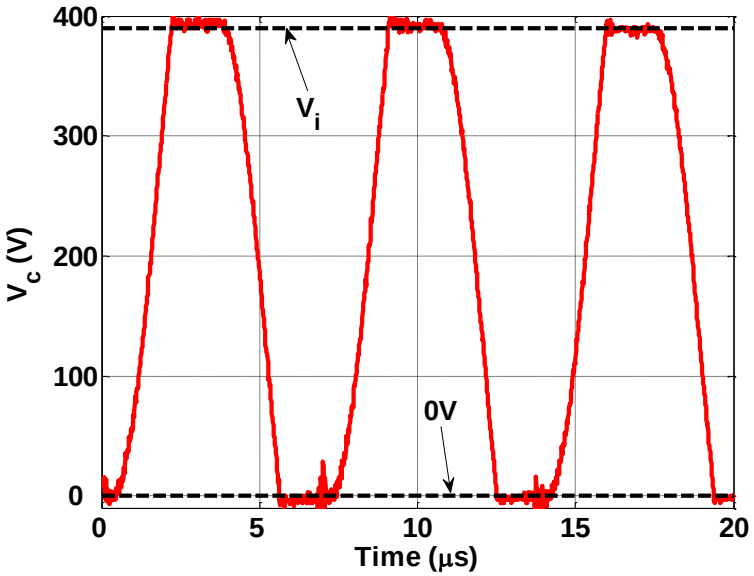
To validate the accuracy of the proposed equivalent circuit model and analysis presented in the previous sections, a LLC resonant converter with power rating of 90 W (V_o =36 V, I_o = 2.5 A), $V_i = 390V \pm 4\%$ and f_0 =147 kHz is designed and constructed.

Following the design procedure in [102] and with the converter operating at the LIP under the nominal input voltage of 390 V, the transformer turn ratio n is selected to be 5.5, the minimum gain for the minimum input voltage is calculated to be 1.09. With the inductor ratio, A_s, selected to be 5 (a good compromise to achieve a narrow operating frequency range a low circulating currents), the maximum quality factor that satisfies the required gain is Q = 0.52. This leads to the selection of the following resonant tank components: L_s = 236 µH, L_p = 1.2 mH and C_r = 5 nF with the minimum and maximum operating frequencies of 100 kHz and 152 kHz respectively. The C_c that provides the optimum current limiting performance is found empirically using the model to be 3.6 nF. The C_s is calculated to be 17 nF and the B_s is 0.3 from (7.2).

With the resonant tank components above, the capacitor common point voltage v_c under full load and ten times overloading at the nominal input voltage of 390V are plotted in Fig. 7.11 (a) and (b) respectively. Fig. 7.11 (a) shows that under the full load condition, the peak-to-peak value of v_c is below the input voltage and therefore the diode-clamp is inactive. It should be noted that the v_c waveform shown Fig. 7.11 (a) has a different DC offset to the ideal case presented in Fig. 7.4 (a), the reason for this is the additional DC path created by the oscilloscope probe causing an imbalance in the capacitor branch- its peak-to-peak value is unaffected. The voltage waveform across capacitor C_c at ten times overloading is clamped between the 0 and V_i as shown in Fig. 7.9 (b). From Fig. 7.11 (b), the conduction angle δ_c is found to be 91°, in comparison to the value of $\delta_c = 95°$ found by the procedure in section 3.3, an error of just 4%.



(a)



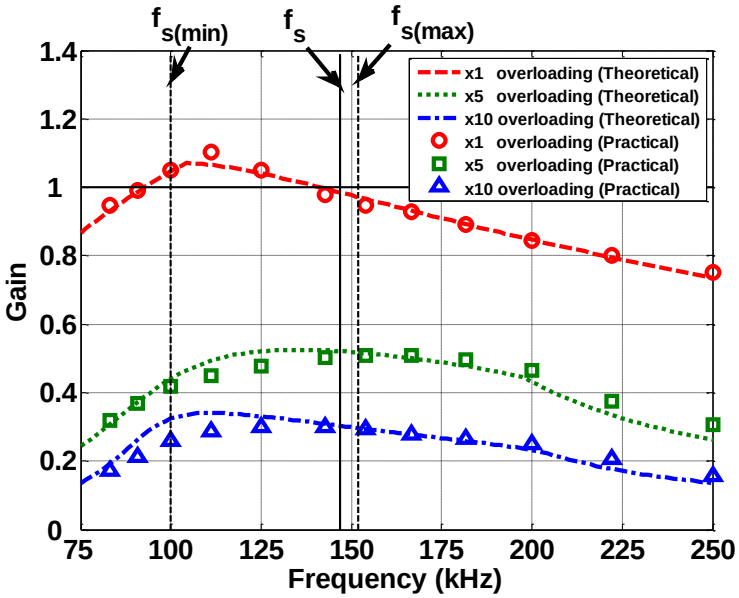
(b)

Fig. 7.11 Measured resonant capacitor voltage waveform v_c. (a) normal operation and (b) overloading operation

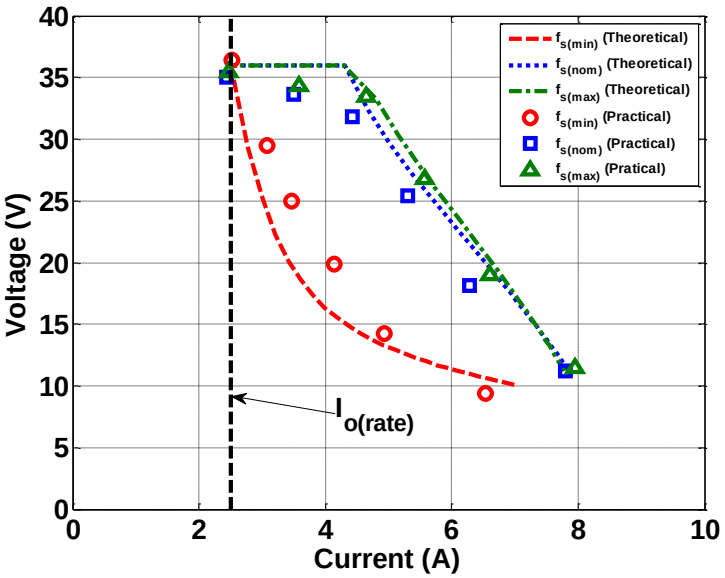
The voltage gains of the prototype converter under the full rated load and five and ten times overload conditions are predicted using the model using (22) and shown in dash-line, dot-line and dash-dot-line respectively in Fig. 7.12 (a). The practical gains under the same load conditions are

plotted in circle, square and triangle in Fig. 7.12 (a) respectively, showing a good match to the theoretical result.

The converter's *VI* characteristic, from full rated load to ten times overload conditions, under the $f_{s(min)}$, f_s and $f_{s(max)}$ are plotted in dash-line, dot-line and dash-dot-line respectively in Fig. 7.12 (b) (n.b. V_i is select according to f_s $\left(V_{i(max)} \geq V_i \geq V_{i(min)} \mapsto f_{s(min)} \leq f_n \leq f_{s(max)}\right)$ to maintain the desired output voltage at the maximum rate load under different f_s). At ten times overload, the current is limited by the diode-clamp to 8 A for the three input voltages. The measured practical VI characteristics under the three input voltages from the prototype converter are plotted as circle, square and triangle markers in respectively Fig. 7.12 (b). The trends agree well with the model predictions.



(a)



(b)

Fig. 7.12 Comparison of the theoretical and practical results. (a) voltage gain characteristics (b) VI characteristics

7.6. Summary

An FHA equivalent circuit model describing the behaviour of the LLC resonant converter with the capacitor-diode clamp has been derived using describing function techniques, where the equivalent impedance of the diode/capacitor, Z_c, is first obtained using a three step process, after which it is combined with the FHA to allow the resonant current to be found. An iterative procedure for determining the conduction point of the diode-clamp has also been detailed. A resonant capacitance sharing ratio B_s has been introduced to allow the best current-limiting performance to be investigated. The presented analysis has shown that in order to achieve the best current limiting characteristic in overload condition, the clamped portion of the resonant capacitors C_c must be selected such that the current-clamp starts operating as soon as the maximum load current under the minimum input voltage, is exceeded. A 90 W converter and its diode-clamp was designed with A_s = 5, Q_{rate} = 0.52 and B_s = 0.3. Using the proposed equivalent circuit model, converter static gain characteristics and the VI characteristics between the rated load and ten times overloading are predicted using the new nominalised gain equation $M_{g(clmp)}$. When compared with the experimental measurements taken from the prototype, the overall trend of the practical results follow that of the prediction, at ten times overloading, output current was successfully reduced from 25 A to 8 A.

8. Conclusion and future work

8.1. Conclusion

The work described in this thesis has demonstrated significant improvements in the efficiency of buck converters based on the application of a parallel converter strategy.

After verifying the modelling and control processes in chapter 3, chapter 4 developed a new control scheme for parallel converters, the fast recovery with high transient efficiency (FRHE) scheme [P1], which combines the fast transient response characteristic of the fast response double buck (FRDB) scheme and the high efficiency characteristic of the sensorless and peak current mode (SCM-PCM) scheme, to achieve higher efficiency in transient condition. From a 25 W prototype converter implemented with the FRHE, the efficiency in transient condition was improved by as much as 5% when compared to conventional control schemes – a 40% reduction in dissipated thermal energy.

Chapter 5 demonstrated a novel design technique for parallel converters, the high steady-state efficiency (HSSE) design technique [P2]. In this new design technique, both the transient performance requirement and minimum load condition are allocated to the auxiliary power modules to allow the dominant conduction losses in steady-state condition to be reduced. From a 360 W prototype converter designed with the HSSE, the efficiency in steady-state condition under all load conditions was improved. At 10% load condition, the efficiency is significantly improved by 7% in comparison to the interleaved converter, extending the 85 plus percent efficiency to lighter load conditions.

Chapter 6 presented a new current ripple reduction technique, the active current ripple cancellation (ACRC) [P3] for parallel converters, to reduce the current ripple while maintaining high efficiency. In this technique, the current waveform of the auxiliary PM was engineered to be the exact opposite to the main PM current ripple which, when combined, reduced the current ripple to the desired level. For a 20 W prototype converter, the current ripple as seen by the output

capacitor is reduced by 67%, allowing smaller filter capacitor to be used. The efficiency under the light and heavy load conditions is also improved by as much as 6% in comparison to the interleaved converter, but is 1.5% lower under the mid-range load condition.

Despite the high efficiency of LLC resonant converters, the overloading issue prevents this topology to be more widely adapted. Chapter 7 addresses this issue by utilising a capacitor diode-clamp and develops a new fundamental harmonic approximation (FHA) based equivalent circuit model for LLC resonant converters with capacitor-diode clamp [P4] through the application of describing function techniques. Using the equivalent circuit model, the effects of the converter with the different capacitor clamp are illustrated, allowing the best current limiting property to be identified. From a 90 W converter, the load currents under different overloading conditions are predicted, the measured results validated the accuracy of the model. With the capacitor diode-clamp, the converter overloading current with ten times overloading is successfully reduced from 25 A to 8 A. The ability to limit overload current in this way reduces stresses on components during overload and hence allows the use of smaller, and hence more cost effective active devices.

8.2. Future work

1) The approach of this thesis is to develop multiple control schemes and design techniques to improve converter performance. This has been achieved with the proposal of the FRHE scheme in Chapter 4, the HSSE design technique in Chapter 5 and ACRC scheme in Chapter 6. All these schemes and techniques have so far been tested on the different converters as a stand-alone solution to improve the different aspect of converter performance. Further research would implement all the proposed schemes and technique together in a single converter, allowing high steady-state and transient efficiencies and high power density to be achieved simultaneously. In this thesis, the parasitic resistance of components are also assumed negligible; the inclusion of the parasitic resistance will improve the prediction accuracy.

2) The ACRC scheme in Chapter 6 has demonstrated how to calculate the duty cycles for both the main and auxiliary PMs to produce the correct output voltage and to achieve ripple cancellation. These duty cycles, however, have to be recalculated to compensate for the change in input voltage, load conditions, or the drift in component values due to change in temperature and ageing. In order to achieve the line and load regulation autonomously, closed-loop control is required. Average current mode control [108] as shown in the block diagram in Fig. 8.1 could be used. Instead of just using the outer voltage loop to set the inner current loop reference, I_{ref} is also added to set the minimum main PM current to prevent current diversion.

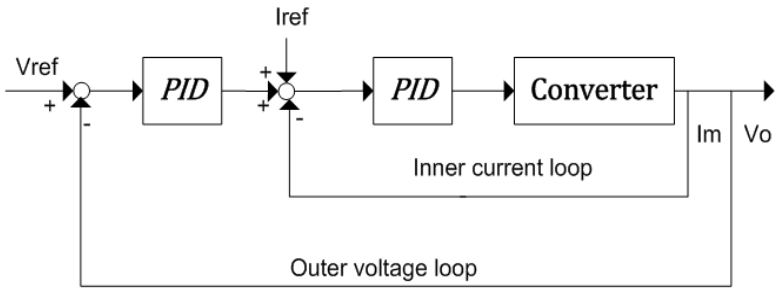


Fig. 8.1 Block diagram of the converter with average current mode control.

3) The capacitor-diode clamp in Chapter 7 was able to reduce the overloading current automatically, without any external control action. This reduction is, however, not sharp enough for some applications, resulting in the need to adjust the switching frequency to reduce the converter's gain. Further research will need to identify ways to improve the sharpness of the current limiting diode-clamp. One possibility is to include a second capacitor-diode clamp [87] as enclosed in dashed box in Fig. 8.2 to clamp the unclamped capacitor, C_{s}, to the output voltage. This idea could be taken forward in a future investigation resulting from the thesis.

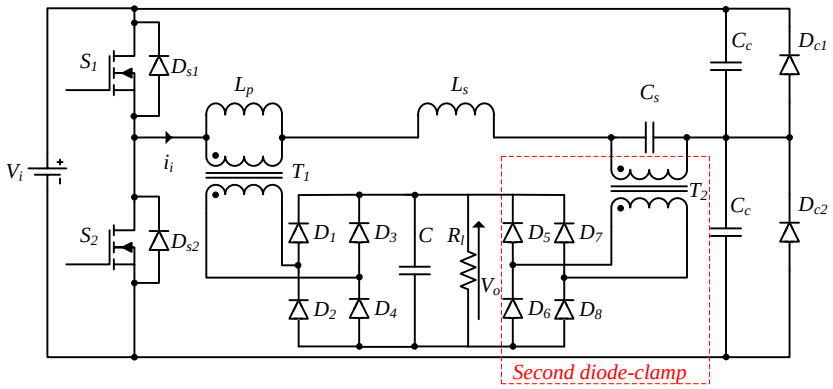


Fig. 8.2 Circuit diagram of the proposed dual capacitor-diode clamp.

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Appendix A - Isolated MOSFET gate driver

In order to isolate the control board (4.19) which controls the duty cycles of the converter in Chapter 5 from the non-isolated high voltage MOSFETs, isolated gate drivers are required. The circuit diagram of a two stages transformer coupled isolated gate driver is shown in Fig. A1. In the first stage, the PWM signal from the microcontroller is first amplified and decoupled by a gate driver, after which its DC component is removed by the capacitor C_{g1} and diode D_1 to allow the signal to pass through the pulse transformer, T_{P1}, without saturation. The isolated pseudo AC signal is then restored with the DC component by the capacitor C_{g2} and diode D_2. The C_{g1} and C_{g2} are select based on the allowable voltage ripple and the amount of charge passing through the capacitors in each cycle [90]:

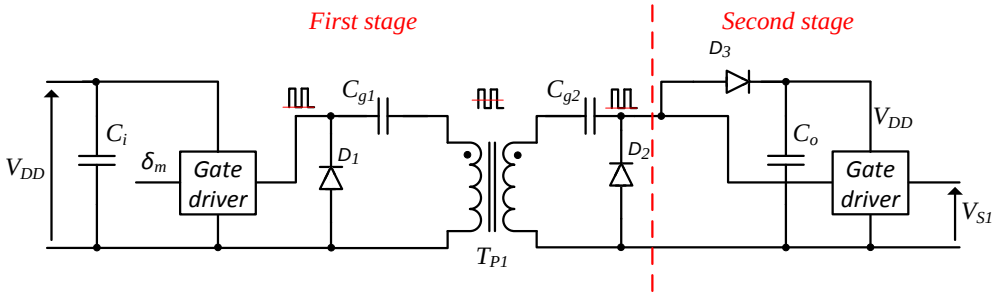


Fig. A1 Circuit diagram of the two stages transformer coupled isolated gate driver.

With the maximum current through off-the-shelve pulse transformer at 200 mA, this low drive current lengthens the MOSFET switching duration, increasing the switching losses, to overcome this, a second stage is added as shown in Fig. A1. The power to the second stage is stored in C_o which is accumulated over the on-duration. With gate driver UCC27324 from Texas Instruments, the drive current can then be increased to 4 A.

Appendix B - rms current

For the main PM, with the auxiliary PM not performing ripple cancellation and the interleaved converter, their rms currents can be found by (B1) [101].

$$I_{(\mathrm{rms})} = \sqrt{I_{(\mathrm{dc})}{}^2 + \frac{\Delta I_{\mathrm{m}}{}^2}{12}} \tag{B1}$$

During the ripple cancellation mode, apart from the current ripple due to the on- and off-period of the auxiliary PM, there is also a low frequency current ripple which is exact opposite to the current ripple of the main PM. In order to include this extra current ripple, the $I_{(\mathrm{dc})}$ term in (B1) is reformulated as followed:

With Fig. B1 and by geometry, the $I_{\mathrm{x(dc)}}$ during the main PM on- and off- period is found as in (B2):

$$I_{\mathrm{x(dc)}}(t) = \begin{cases} -\frac{\Delta I_{\mathrm{m}}}{\delta T} t + \Delta I_{\mathrm{m}} & 0 < t \leq \delta T \\ \frac{\Delta I_{\mathrm{m}}}{(1-\delta)T} t - \frac{\Delta I_{\mathrm{m}} \delta}{(1-\delta)} & \delta T < t \leq T \end{cases} \tag{B2}$$

By performing integration on (B2) and with $\frac{\Delta I_{\mathrm{m}}}{2} = (1-\alpha) I_{\mathrm{o}}$, (B3) is obtained as followed:

$$I_{\mathrm{x(rms)}} = \sqrt{1.33(1-\alpha)^2 I_o{}^2 + \frac{\Delta I_{\mathrm{x}}{}^2}{12}} \tag{B3}$$

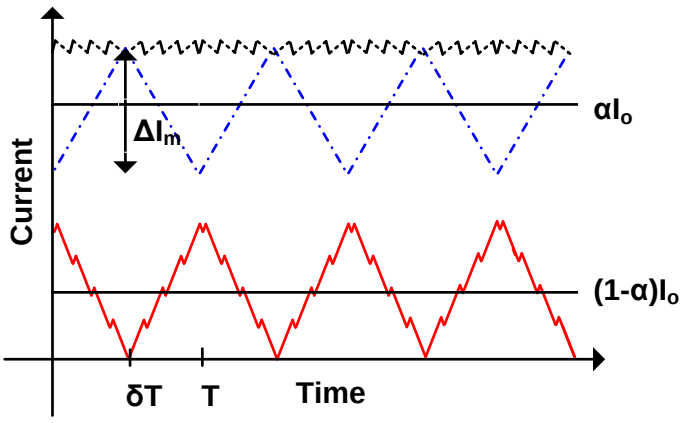


Fig. B1 Current waveform of auxiliary PM in ripple cancellation mode.

Appendix C - Calorimeter for efficiency measurement

Due to the switching nature and high efficiency of SMPCs, measuring the difference between the input and output powers through their corresponded voltages and currents can lead to a high margin of error. Instead, the calorimetric method measures the losses through the heat generated by the converter to allow higher measurement accuracy to be achieved.

The calorimetry used in this thesis is the indirect calorimetric method detailed in [109]. In this method, a well insulated box is built and the internal temperature rise is calibrated against the known power losses generated by a power resistor, to produce a calibration curve as in Fig. C3 (a) and (b). To measure the power losses of the converter, the power resistor is replaced by the converter and set to operate at the desired operating condition. The temperature rise generated by the converter is measured and compared against a calibration curve to determine the losses at the tested operating condition.

Two bespoke calorimeter were built for this thesis:

- a large one with the internal diameters of 250 mm x 250 mm x 250 mm with a layer of 22 mm thick expanded polystyrene sheets. This is used for the high power converter in Chapter 5.
- a small one with the internal diameters of 150 mm x 150 mm x 150 mm with three layers of 10 mm thick expanded polystyrene sheets as shown in Fig. C1.

Holes were added for wires; the hole were then sealed with PVA glue. One possible source of error is heat conducted out of the box through the connection wires, but the wiring was kept constant between tests to try to include this in the calibration curves.

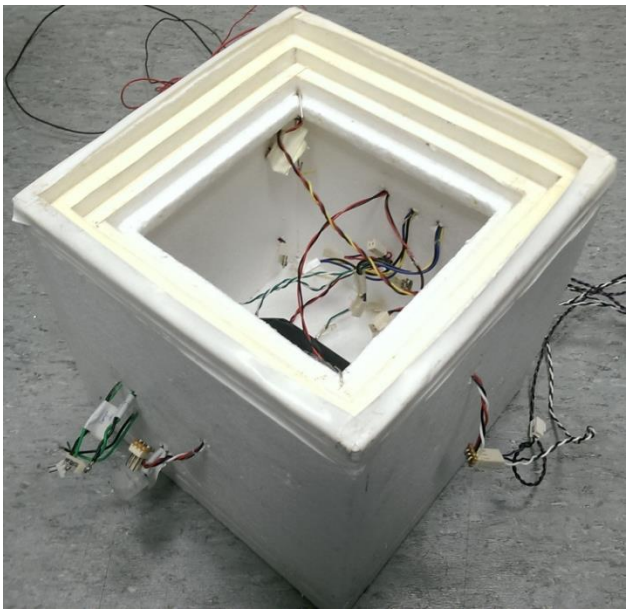
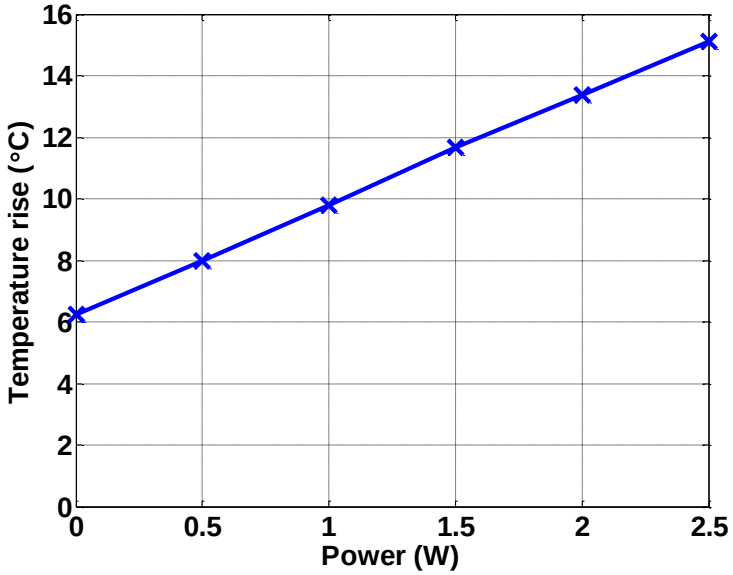


Fig. C1 Bespoke calorimeter.

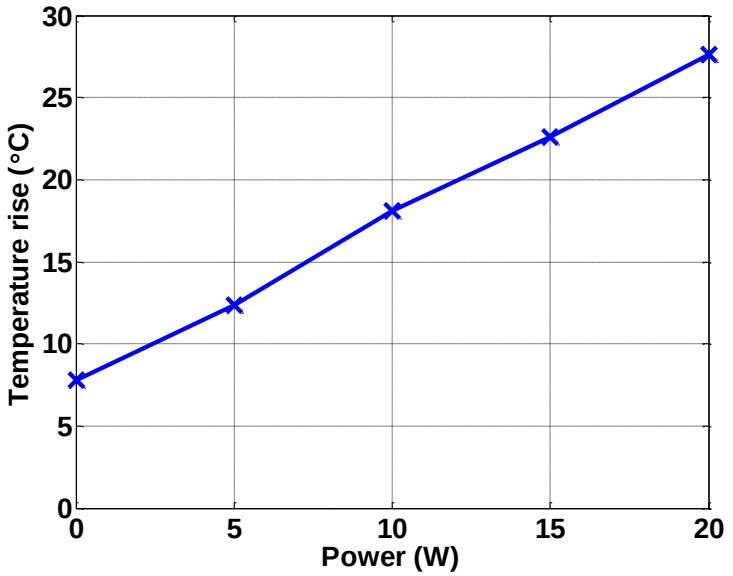
The average internal temperature is measured with four platinum temperature sensors, Pt100 [110] located on the four side-walls, and is measured by date acquisition device (DAQ) RedLab 1208FS [111]. By setting the voltage range of the DAQ to $\pm$1V and operating in the differential mode with its 12-bit resolution, the measured voltage resolution is 0.48 mV, this translate to a temperature resolution of 0.1°C. The external temperature is regulated by an environmental chamber at 25°C. To help to spread the temperature inside the box, a 90 mm fan is also included as shown in Fig. C2. The power loss due to the fan is included in the calibration curve as offset as shown in Fig. C3.

Fig. C2 Calorimeter with fan for heat spread.

The calibrating curve for this setup is shown in Fig. C3.



(a)



(b)

Fig. C3 Calibration curves. (a) small box (b) large box.