Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2012, Article ID 242459, 8 pages
doi:10.1155/2012/242459

Research Article

Robustness Comparison of Emerging Devices for Portable Applications

S. D. Pable,[1] Mohd. Ajmal Kafeel,[2] A. K. Kureshi,[3] and Mohd. Hasan[2]

[1] *Department of Electronics and Telecommunication Engineering, P.D.V.V.P College of Engineering, Ahmednagar 414 111, India*
[2] *Department of Electronics Engineering, AMU, Aligarh, India*
[3] *Vishwabharati Acadmey's COE, Sarola Baddi, Ahmednagar, India*

Correspondence should be addressed to S. D. Pable, sachinp_79@yahoo.co.in

Received 4 October 2011; Accepted 15 November 2011

Academic Editor: Christian Brosseau

Copyright © 2012 S. D. Pable et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Extensive development in portable devices imposes pressing need for designing VLSI circuits with ultralow power (ULP) consumption. Subthreshold operating region is found to be an attractive solution for achieving ultralow power. However, it limits the circuit speed due to use of parasitic leakage current as drive current. Maintaining power dissipation at ultralow level with enhanced speed will further broaden the application area of subthreshold circuits even towards the field programmable gate arrays and real-time portable domain. Operating the Si-MOSFET in subthreshold regions degrades the circuit performance in terms of speed and also increases the well-designed circuit parameter spreading due to process, voltage, and temperature variations. This may cause the subthreshold circuit failure at very low supply voltage. It is essential to examine the robustness of most emerging devices against PVT variations. Therefore, this paper investigates and compares the performance of most promising upcoming devices like CNFET and DG FinFET in subthreshold regions. Effect of PVT variation on performance of CNFET and DG FinFET has been explored and it is found that CNFET is more robust than DG-FinFET under subthreshold conditions against PVT variations.

1. Introduction

ULP applications like pacemakers, hearing aids, body-based sensor networks, wireless sensor networks, and many other biomedical systems are bounded by ULP budget rather than the higher performance. Supply voltage (V_{DD}) scaling is a well-established technique for reducing the power consumption significantly since energy has squared dependency on V_{DD}. Under extreme voltage scaling, the V_{DD} is reduced to the threshold voltage (V_{th}) of the MOSFET. Under this condition, the power consumption is significantly reduced up to milli Watt range but the speed of such circuits degrades substantially. This region of operation of a Si-MOSFET is popularly known as a subthreshold region. Under subthreshold conditions, the parasitic off-state leakage current of a MOSFET is utilized as the switching current for designing ULP circuits. It is possible to reduce the power consumption further under deep subthreshold but the delay penalty rises exponentially.

Subthreshold circuits also exhibit improvement in transconductance due to exponential I-V characteristics, smaller gate capacitance, and near-ideal voltage transfer characteristics (VTC). Previous research on subthreshold operation of Si-MOSFET shows that subthreshold circuits are more appropriate for ULP and moderate throughput applications [1–4]. Recently, while designing low-power circuits, importance is given to operate the device at minimum energy delay point (EDP) instead of minimum energy point (MEP). It is observed from Figure 1 that minimum EDP of an inverter with a fan out of four loading occurs in the subthreshold region with 32 nm Si-MOSFET [5]. For combinational circuits penalty in delay is significant. Therefore, the key challenges for the subthreshold circuit designer are (a) to improve the speed and (b) to reduce device variability.

Due to reduced speed and variability issues in Si-MOSFET, it is important to investigate the potential of upcoming devices for enhancing the performance of

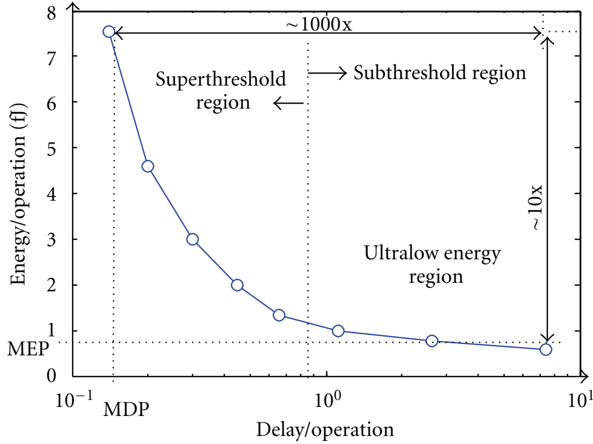


Figure 1: Energy delay tradeoff for inverter under test at 32 nm technology node.

subthreshold circuits for real-time applications where performance cannot be ignored. Device parameter variations under subthreshold conditions are significant and may cause the circuit failure. FinFET and CNFET transistors are evolving rapidly, and it is expected that these devices will replace the existing bulk CMOS technology in the future [6]. To the best of our knowledge, no prior publication has modeled the delay, switching energy, and variability of FinFET and CNFET devices under subthreshold conditions at ULP levels on the same platform.

The organization of this paper is as follows. Section 2 introduces the device design metric parameters considered for comparison purpose. Section 3 explores the DG FinFET structure. Section 4 explores the optimisation of number of tubes per device and inter-CNT pitch for optimum value of delay and energy. Section 5 extensively compares the subthreshold performance and the effect of PVT variation on CNFET- and FinFET-based inverter. Section 6 concludes this paper.

2. Device Design Metric under Subthreshold Conditions

CNFET and DG-FinFET are the most promising emerging nanodevices. However, for extending their application area even for ULP, there is a need to explore the reliability of these devices in the presence of PVT variations for future ULP circuits.

The subthreshold operating region uses small parasitic off-state leakage current as a switching current to realize ULP circuits. For Si-MOSFET device, this small leakage current can be expressed as follows [1]:

$$I_{\text{sub}} = I_0 e^{(V_{\text{GS}} - V_{\text{th}} + \eta V_{\text{DS}})/nV_T}\left(1 - e^{-V_{\text{DS}}/V_T}\right), \quad (1)$$

where "V_{th}" is the transistor threshold voltage, "n" is the subthreshold slope factor ($n = 1 + C_d/C_{\text{ox}}$), "$V_T$" is the thermal voltage, and "η" is the DIBL coefficient.

The ON-OFF current ratio ($I_{\text{on}}/I_{\text{off}}$) is an important device performance metric that mainly decides the power dissipation of the device. I_{on} is the subthreshold leakage current at $V_{\text{DD}} = V_{\text{GS}} = V_{\text{DS}}$, and I_{off} is the leakage current at $V_{\text{GS}} = 0\,\text{V}$ and $V_{\text{DS}} = V_{\text{DD}}$. For better performance, higher subthreshold ON-OFF current ratio is preferred. The subthreshold slope (S) is another important device design metric that determines the relationship between subthreshold leakage current and gate voltage. From the definition of inverse subthreshold slope, it can be expressed as follows [7]:

$$S = \left(\frac{d\left(\log_{10} I_{\text{sub}}\right)}{dV_{\text{GS}}}\right)^{-1}. \quad (2)$$

The gate delay and switching energy in terms of "S" and load capacitance (C_L) is given by [8]

$$T_{\text{delay}} \propto \frac{C_L S}{I_{\text{off}}}, \quad (3)$$

$$E_{\text{dyn}} \propto C_L S^2. \quad (4)$$

It is clear from (3) and (4) that the time delay and switching energy are proportional to "S" and the load capacitance. It is essential to optimize device parameters for better value of "S" for lower delay and switching energy. Due to the performance challenges inherently present in Si-MOSFET under subthreshold conditions it is necessary either to optimize the Si-MOSFET device parameters or to explore FinFET or CNFET for ULP applications. Our previous work on subthreshold FPGA has successfully optimized the Si-MOSFET for better performance under subthreshold conditions [9]. Device and circuit performance parameters to be considered for designing better subthreshold circuits are subthreshold leakage current, $I_{\text{ON}}/I_{\text{OFF}}$, "$S$", C_g, gate delay, total power consumption, dynamic energy, and static noise margin. The next sections describe the FinFET device structure followed by optimization of CNFET device parameters for fair performance comparison (equal V_{th} and width) with that of FinFET.

3. Structure of DG FinFET Device

A FinFET transistor is a vertical double-gate emerging device with a potential to replace bulk devices at nanometer technology node [10–12]. The structure of the subcircuit model of a FinFET device used for simulation is as illustrated in Figure 2. A FinFET is modeled as a pair of FD SOI device with source and drain connected together as shown in Figure 2(c). The DG FinFET can either have a three-terminal (3T) configuration, where both the gates are shorted, or a four-terminal (4T) configuration, having fixed back-gate bias and the front gate acting as the control electrode. In this work, three-terminal symmetric FinFET is considered because it has better drive current as compared to other configurations [10]. Device parameters used for FinFET simulation are as listed in Table 1.

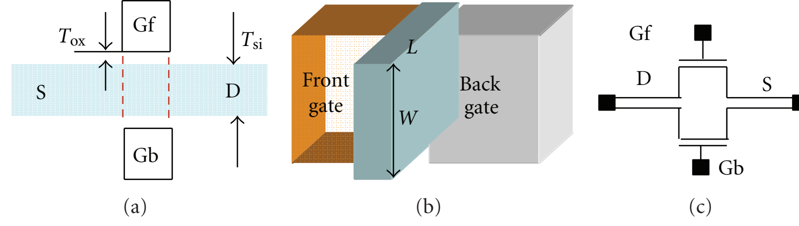


Figure 2: The structure of the subcircuit model of a FinFET device: (a) top view of front and back gates; (b) three-dimensional view; (c) subcircuit symbol of DG FinFET [10].

Table 1: 32 nm DG FinFET device default parameters values.

Parameter	nFinFET	pFinFET
L_g (nm)	32	32
T_{si} (nm)	8.6	8.6
T_{ox} (nm)	1.4	1.4
N_{ch} (cm^{-3})	2×10^{16}	2×10^{16}
V_{th} (V)	0.29	−0.25
H_{fin} (nm)	13	13
T_{fin} (nm)	8.6	8.6
Gate material	Metal	Metal
Doping profile	Uniform	Uniform

4. Optimisation of CNFET under Subthreshold Conditions

CNFET provides many potential advantages like improved channel transport and high carrier velocity of CNT, which results in significant improvement in speed over Si-MOSFET [13–15]. Single wall carbon nanotube can be visualized as a sheet of graphite that is rolled up and joined together as shown in Figure 3(a). A typical layout of a MOSFET-like CNFET device is illustrated in Figure 3(b). As shown in Figure 3, the CNTs are placed on the bulk substrate (k_2) and a high (k_1) dielectric separates the CNTs from metal gate electrode by an insulator thickness "T_{OX}," with dielectric constant of 16. "W_{gate}" is the width of metal gate, channel length (L_g) = 32 nm, and source drain under-lapped L_{SS} = L_{DD} = 32 nm. The power dissipation and speed of CNFET devices are mainly governed by the number of tubes in the channel (n), tube diameter, and inter-CNT pitch. Hence, there is a need to explore the best possible values of "n" and "pitch" for better device and circuit performance in ULP regions for a given tube diameter. Various CNFET models have been developed for future deep nanometer technology [13, 14]. The impact of scattering on BTBT is not taken into account in CNFET compact model developed in [14], and this effect can be of importance. Therefore, the experimentally validated Stanford University CNFET model is used for simulating the CNFET device [13]. The chirality vector (19, 0) is chosen for the CNT, which corresponds to 1.5 nm tube diameter and V_{th} of 0.29 V for CNFET.

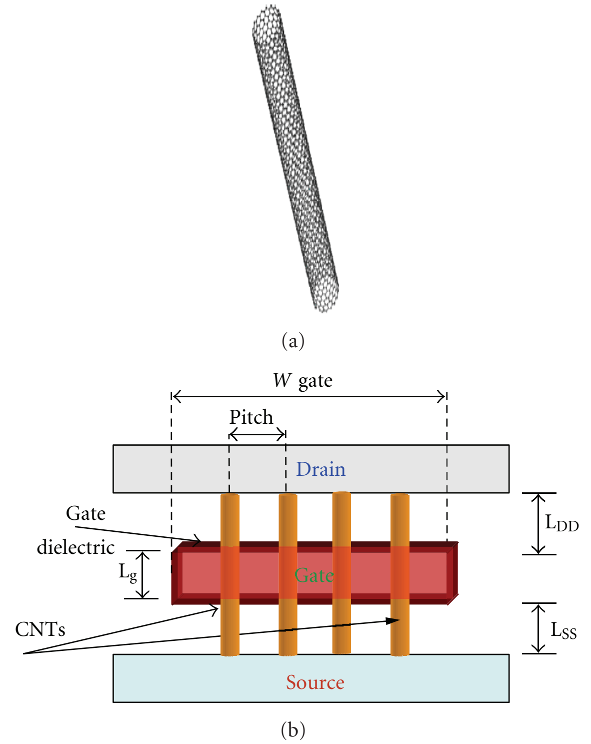


Figure 3: (a) CNT structure. (b) Schematic of CNFET device.

To design better reconfigurable ULP circuits, it is necessary to explore the performance and impact of CNFET technology parameter variations on circuit characteristics. The drive current, and hence the speed of CNFET, is a function of number of tubes per device (n), device transconductance, $g_{CNFET} V_{DD}$, V_{th}, and voltage drop across the doped source region (V_{SS}). The V_{th} is determined by the CNT diameter and is constant for a given diameter.

The CNFET delay and switching energy are given by [16]

$$T_{CNFET,n} \propto \frac{C_{CNFET,n} V_{DD}}{I_{CNFET,n}}, \quad (5)$$

$$\text{Energy}_{CNFET,n} \propto C_{CNFET} V_{DD}^{2}, \quad (6)$$

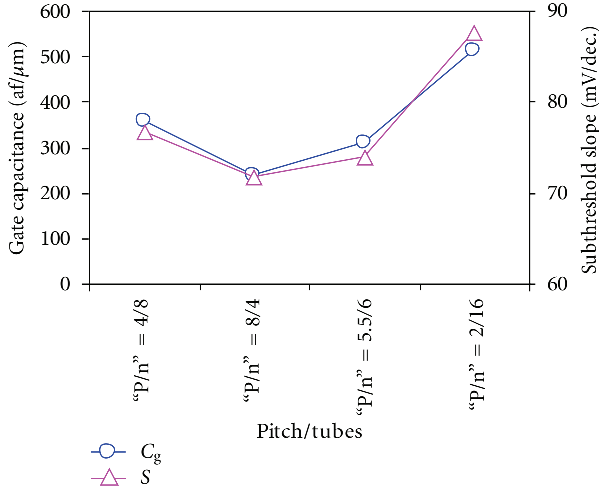


FIGURE 4: "C_g" and "S" as a function of pitch and number of tubes.

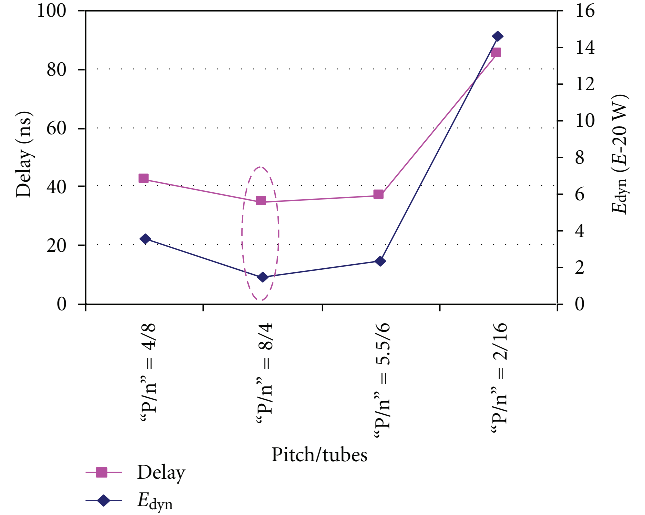


FIGURE 5: Delay and dynamic energy as a function of pitch and number of tubes.

C_{CNFET} is the gate capacitance of CNFET. The total gate capacitance of CNFET with the number of tubes "n" is given by [16]

$$C_{\text{CNFET},n} = n \cdot C_{g\text{-CNT1}} L_{g,\text{CNT}} + C_{g\text{-parasitic}} W_{g,\text{CNT}}, \tag{7}$$

where "$W_{g,\text{CNT}}$" is the width of CNFET, "$L_{g,\text{CNT}}$" is the gate length, and "$C_{g\text{-parasitic}}$" includes fringing capacitance.

It is important to optimize the number of tubes and inter-CNT pitch ("P") for optimum performance of a CNFET device. To achieve optimum values of "n" and "P," "S" and the gate capacitance ("C_g") are plotted for different values of "P" and "n" ratio (P/n) as shown in Figure 4. The CNFET pitch "P" and the number of tubes "n" are varied by keeping 32 nm device width constant. It is evident from Figure 4 that by using "P" = 8 nm and "n" = 4, minimum values of "C_g" and "S" with moderate drive current are obtained. The impact of "P" and "n" on delay and dynamic energy of a five-stage inverter chain is also investigated. The delay, dynamic energy, and power dissipation are measured for the third inverter in a chain for more realistic comparison [16] and are shown in Figures 5 and 6, respectively. It is evident from (4), (5) and Figures 5 and 6 that the device having minimum "C_g" and "S" shows minimum delay, power dissipation, and dynamic energy. Therefore, for further performance analysis of the CNFET device and circuits, "P" = 8 nm and "n" = 8 are considered.

5. Performance Comparison of Emerging Devices under Subthreshold Conditions

It is well established that subthreshold circuits are more prone to PVT variations [1–4]. To better understand the effect of PVT variations, the analysis of FinFET and CNFET begins with a focus on device level characteristics first and then the circuit level performance characteristics are explored. Switching threshold (V_M) and signal to noise margin (SNM) are obtained from the VTC curves. VTC comparison of CNFET- and FinFET-based inverter is shown

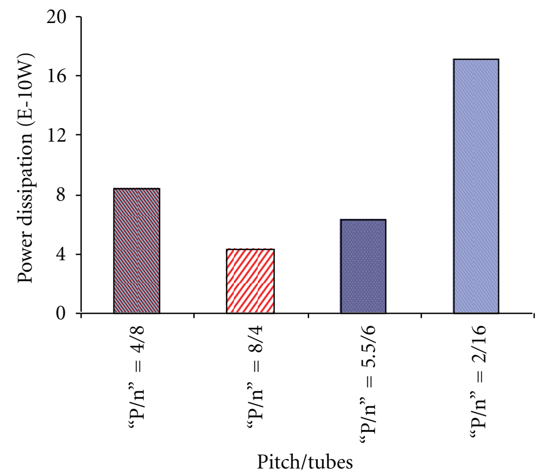


FIGURE 6: Power dissipation as a function of pitch and number of tubes.

in Figure 7 for the same width and V_{th} with input voltage being scaled down. It is observed that CNFET-based circuits have steeper VTC with switching threshold voltage of 0.1 V ($V_{\text{DD}}/2$) and that of FinFET is 0.093 V. This is due to ballistic transport of carriers in CNFET.

From (3) and (4), "C_g" and "S" play an important role in determining the speed and switching energy. Hence, it is important to investigate the impact of width and V_{DD} scaling on "S" and "C_g." Figure 8 shows the comparison of "C_g" and "S" for CNFET and FinFET for different widths at 0.2 V_{DD}. The width of CNFET device is varied by changing the value of "n" [16] and keeping inter-CNT pitch constant. The parasitic capacitance is proportional to device width in FinFET [17]. Hence, the parasitic capacitance starts dominating the intrinsic gate capacitance with increasing width, thereby increasing "C_g" significantly. In case of CNFET, the "C_g" increases due to the increase in both "n" and width of CNFET

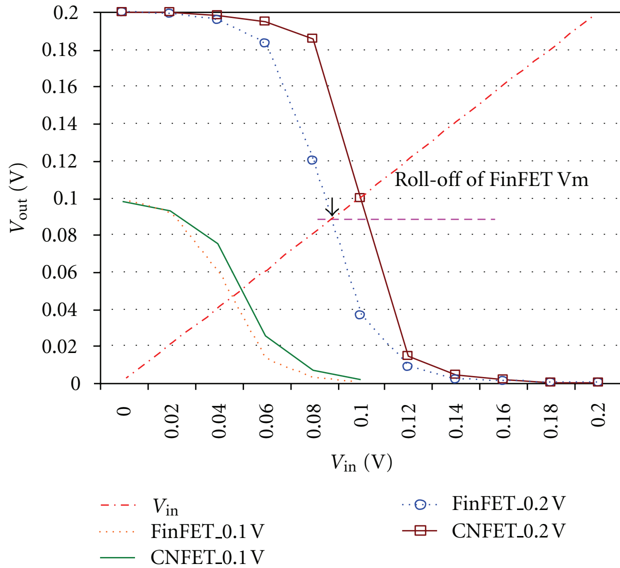


Figure 7: VTC comparison of CNFET and FinFET.

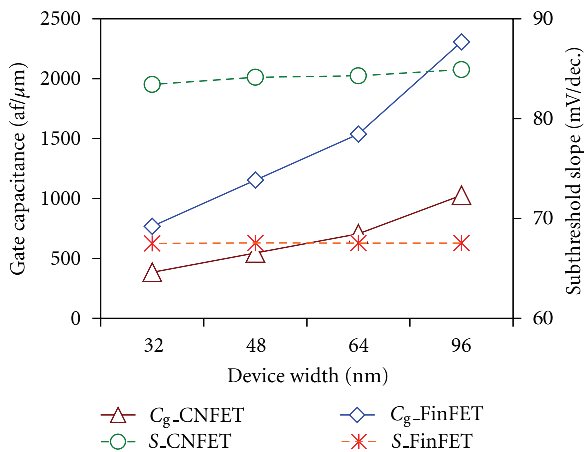


Figure 8: C_g and S comparison of 32 nm CNFET and FinFET.

as from (7). It is clear from Figure 8 that the minimum size of FinFET has almost 3.25X higher "C_g" than CNFET, which is a major cause of higher power and dynamic energy consumption in case of FinFET as compared to CNFET. It is also observed from Figure 8 that by increasing the device width, "S" of both devices increases slightly. It is evident from Figure 8 that FinFET shows better "S" than CNFET due to its dual gate geometry structure. Though gate leakage power (GPL) is small in subthreshold regions as compared to superthreshold regions, it is also essential to estimate the same for energy constrained applications. Figure 9 shows "GLP" and "S" as a function of V_{DD}. It has been observed that "GLP" of CNFET is almost 5.85X lower than that of FinFET at V_{DD} = 0.2 V. This is due to the absence of dangling bonds and hence suppressed carrier scattering in case of CNFET.

To compare robustness, it is necessary to study the impact of T_{OX}, L_g, V_{DD}, and temperature (T) variation on CNFET and FinFET. Table 2 compares the effect of ±10%

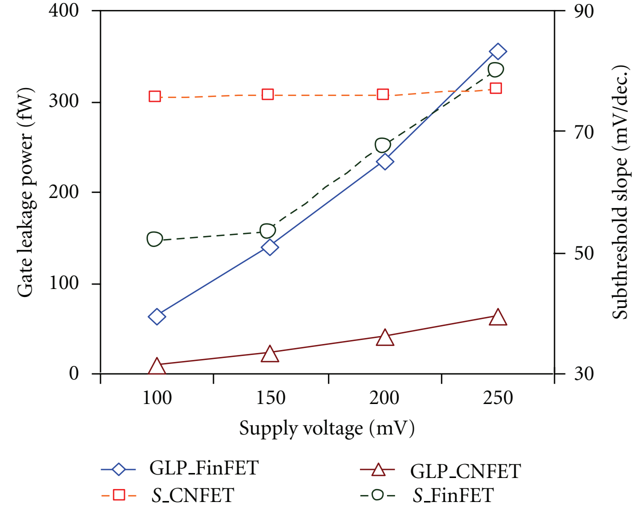


Figure 9: GLP comparison of 32 nm CNFET and FinFET.

PVT variation [17] on different device parameters. It is evident from Table 2 that the drive current in CNFET is a weak function of "L_g" and "T_{OX}" variations due to ballistic transport of carriers [18].

The effective drive capacitance in CNFET is mainly dominated by fringing capacitance, and, therefore, it is less sensitive to geometry parameters such as "L_g" and "T_{OX}" [18] compared with FinFET. However, it is a strong function of V_{DD} compared with case of FinFET due to ballistic transport of carriers. Figures 10 and 11 show the impact of ±15% "T_{OX}" and "L_g" variations on "S" and gate capacitance, respectively. It is evident from Figure 10 that as "T_{OX}" scales down, "S" of CNFET and FinFET improves. This is because when "T_{OX}" reduces, the gate obtains better control over the channel. It is clear from Figure 11 that the "C_g" of FinFET is almost independent of "L_g" variation. This is due to the fact that the dominating gate overlap and fringing capacitances, which are major contributors to "C_g," are "L_g" independent. Hence, the delay dependency on "L_g" is mainly due to the ON current. However, from (7) and Figure 11, it is observed that the "C_g" of CNFET increases with the increase in "L_g".

It is also important to explore the effect of PVT variations on circuit performance parameters such as delay and switching energy. The FO4 inverter chain is used as a test bench. Delay and switching energy is measured across the third inverter [16]. Appropriate device size is chosen for equal rise and fall time. CNFET and FinFET show 11.9% and 28% variation in delay and 8.5% and 19.1% variation in switching energy, respectively, for ±10% variation in "T_{OX}" as depicted in Figures 12 and 13, respectively. Reducing "T_{OX}" in CNFET decreases the "S" by 2.57% and increases the ON current by 10%. However, the "C_g" also increases by 5%. Hence, "T_{OX}" variation has little impact on delay and switching energy of CNFET. In case of FinFET, "T_{OX}" of both front gate and back gate is varied. As the T_{OX} is reduced, the parasitic capacitances start dominating the intrinsic gate capacitance and hence increase the overall "C_g." The I_{off} current increases by 16.91% for 20% reduction in T_{OX}, which

Table 2: Effect of PVT variation on device performance parameter.

Parameter variation	32 nm CNFET				32 nm FinFET			
	%variation in device parameters							
	I_{on}	I_{off}	I_{on}/I_{off}	P_{av}	I_{on}	I_{off}	I_{on}/I_{off}	P_{av}
±10% variation in T_{OX}	10	0.1	15.79	8.32	15.17	16.91	15.08	17.2
±10% variation in L_g	12.18	11.77	4.62	11.84	40.56	47.87	11.74	40.8
±10% variation in V_{DD}	66.31	0.6	66.1	74.26	65.69	19.26	57.53	72.03
±10% variation in T	9.89	10.31	7.02	15.21	14.28	15.09	16.4	8.76

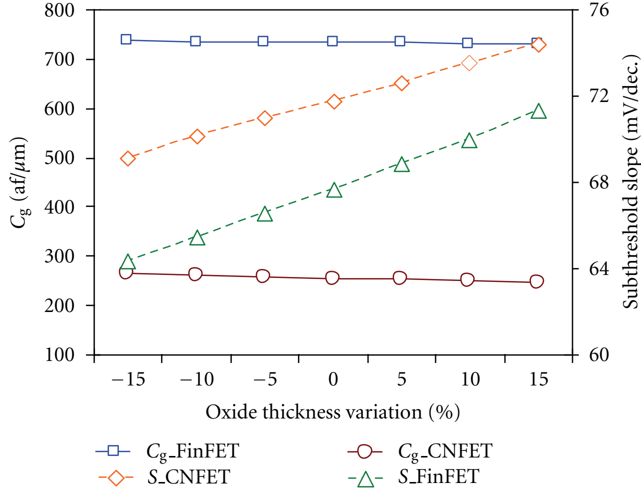


Figure 10: Effect of T_{OX} variation on "C_g" and "S" of 32 nm CNFET and 32 nm FinFET.

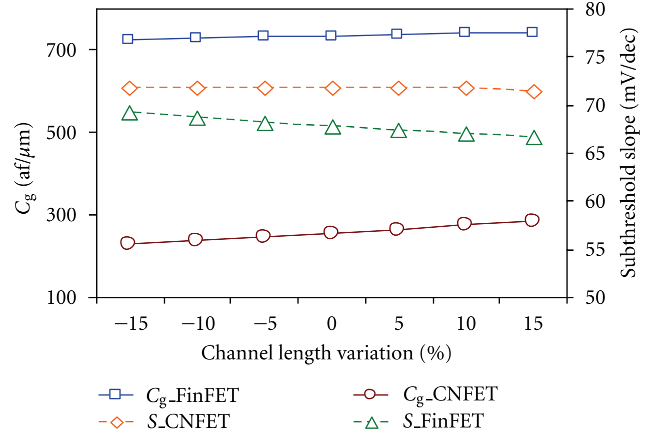


Figure 11: Effect of L_g variation on "C_g" and "S" of 32 nm CNFET and 32 nm FinFET.

results in increase in circuit delay in case of subthreshold circuits [17].

Subthreshold leakage current is also sensitive to "L_g" of the device. Assuming proportional lithographic scaling, the length of the source and drain region is considered to be equal to the "L_g" [16]. The drive current of CNFET decreases by 12% as gate length reduces by 20%. It is also observed that in CNFET, there is negligible change in I_{on}/I_{off} as compared to FinFET for "L_g" variation. Total "C_g" is proportional to gate length and increases by 13% by increasing the "L_g" by ±10% as shown in Figure 11. Hence, "L_g" variation in CNFET has little impact on delay as shown in Figure 14. "S" almost remains constant by varying the "L_g," and from Figure 15 it is also observed that switching energy is less affected by "L_g" variation.

In DG FinFET, the reduction in "L_g" increases the subthreshold current by 40.56% for ±10% "L_g" variation. This is due to pronounced short channel effect [18], which improves the circuit performance in terms of delay as depicted in Figure 14. For FinFET, as "L_g" decreases, the "S" increases by 2.33% as shown in Figure 13, and I_{on}/I_{off} ratio decreases significantly due to increase in I_{off} current (47.87% for ±10%). This results in the consumption of more switching energy as shown in Figure 15. From the above analysis, it is observed that CNFET-based circuit

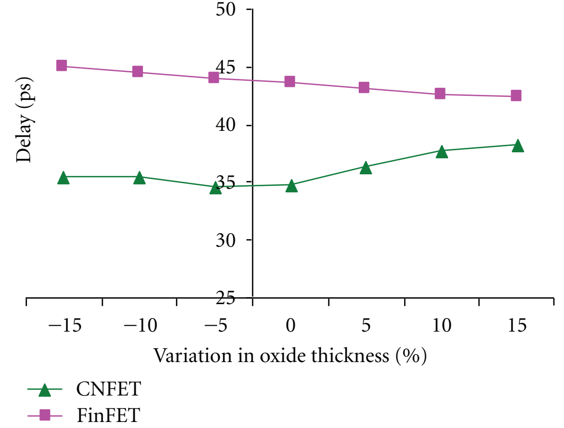


Figure 12: Effect of T_{OX} variation on delay of 32 nm CNFET- and FinFET-based inverter.

performance metrics experience less variation due to "L_g" because of ballistic transport of carriers. CNFET is also found to be more robust against T_{OX} variation. This is due to the fact that the effective drive capacitance in CNFET device is mainly dominated by the fringing capacitance. Hence, the CNFET device is found to be more robust against geometry-based parameter variations over FinFET device.

TABLE 3: Effect of PVT variation on SNM of CNFET and FinFET at $V_{DD} = 0.2$ V.

Parameter variation		32 nm CNFET			32 nm FinFET		
		NM_H (mV)	NM_L (mV)	V_M (mV)	NM_H (mV)	NM_L (mV)	V_M (mV)
	0%	67.6	69.443	100.05	64.24	51.73	93.81
T_{OX}	+10%	68.46	68.38	100.5	66.73	49.53	93.16
	−10%	68.1	67.73	100.36	70.21	45.38	94.8
L_g	+10%	67.4	66.83	100.26	63.98	49.8	93.16
	−10%	68.67	69.86	99.39	62.08	41.48	97.75
V_{DD}	+10%	77.91	79.78	110.04	79.47	65.944	97.75
	−10%	57.84	57.81	90.13	59.56	37.67	81.71
V_{th}	+10%	68.47	67.48	99.39	62.08	41.8	97.75
	−10%	68.93	67.85	99.7	69.84	59.05	89.71
T	25°C	67.6	69.443	100.05	64.24	51.73	93.81
	50°C	65.38	65.48	99.72	65.29	33.75	77.83
	85°C	61.98	62.18	99.72	70.92	28.48	72.16

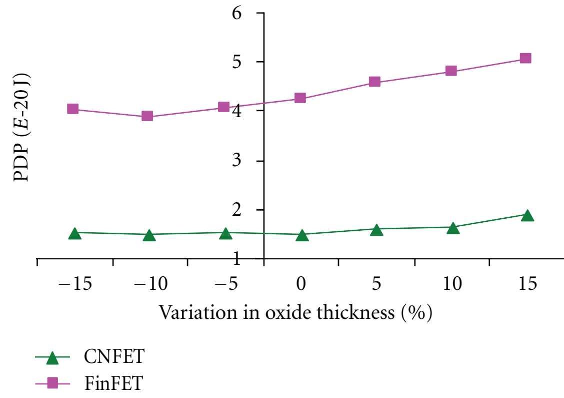


FIGURE 13: Effect of T_{OX} variation on PDP of 32 nm CNFET- and FinFET-based inverter.

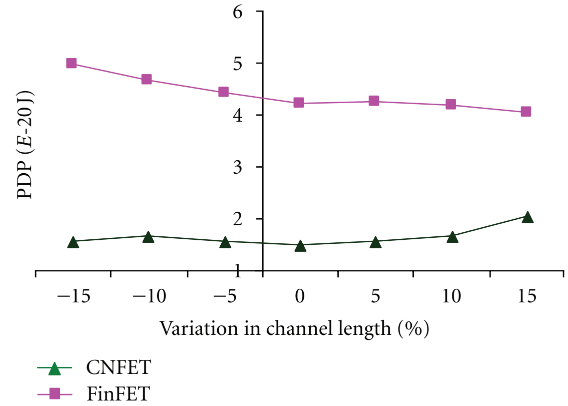


FIGURE 15: Effect of L_g variation on PDP of CNFET and DG FinFET inverter.

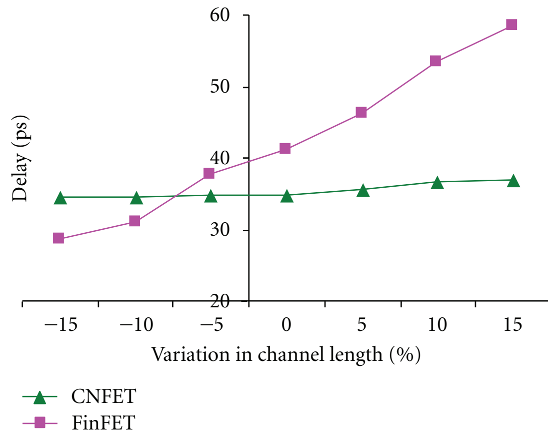


FIGURE 14: Effect of L_g variation on delay of 32 nm CNFET and FinFET inverter.

To evaluate the robustness of subthreshold circuits, SNM is important. SNM is defined as the point where $dV_{out}/dV_{in} = -1$ [17]. To explore the impact of PVT parameter variation, we have assumed ±10% variation in "T_{OX}," L_g, V_{th}, V_{DD} and temperature [17]. Table 3 shows the detailed SNM comparison of CNFET and FinFET inverter. It is evident from Table 3 that CNFET shows less impact against "T_{OX}," L_g, and V_{th} variations on SNM than DG FinFET. This is due to device geometry, ballistic transport of carriers, and V_{th} independency on temperature, respectively. For DG FinFET, as temperature increases, "S" increases and I_{on}/I_{off} reduces significantly. Hence, upon increasing temperature, SNM and switching threshold voltage are significantly affected. However, in CNFET, SNM variation is less due to temperature variation because of high thermal stability property of CNFET. Due to the above-mentioned properties of CNFET, "S" of CNFET is not affected significantly unlike FinFET due to PVT variation. However, SNM of both devices are greatly affected by V_{DD} variations. It can be observed from Table 3 that CNFET shows better SNM and, hence, switching threshold voltage over DG FinFET. Hence, CNFET is more robust than DG FinFET in terms of noise margin and gain.

6. Conclusions

Performance challenges inherently associated with Si-MOSFET under subthreshold conditions led to the need of investigating alternative devices for better system performance. This paper successfully explored the performance and robustness against PVT variations of CNFET and DG FinFET devices. Analysis of subthreshold slope and gate capacitance of CNFET device shows that performance of CNFET circuits can be greatly improved by number of tubes and pitch for minimum subthreshold slope and gate capacitance. PVT variability analysis of CNFET and DG FinFET devices is carried out successfully. CNFET drive current and performance parameters are less sensitive to channel length, oxide thickness, and temperature variation over FinFET. Sensitivity of CNFET devices is slightly higher than that of FinFET for V_{DD} variation.

Acknowledgment

This work is funded by grants received from Department of Science and Technology (DST), Government of India under their FIST programme.

References

[1] H. Soeleman, K. Roy, and B. C. Paul, "Robust subthreshold logic for ultra-low power operation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, no. 1, pp. 90–98, 2001.

[2] S. K. Gupta, A. Raychowdhury, and K. Roy, "Digital computation in subthreshold region for ultralow-power operation: a device-circuit-architecture codesign perspective," *Proceedings of the IEEE*, vol. 98, no. 2, pp. 160–190, 2010.

[3] A. Wang, B. H. Calhoun, and A. P. Chandrakasan, *Sub-Threshold Design for Ultra Low-Power Systems*, Springer, New York, NY, USA, 1st edition, 2006.

[4] B. H. Calhoun, J. F. Ryan, S. Khanna, M. Putic, and J. Lach, "Flexible circuits and architectures for ultralow power," *Proceedings of the IEEE*, vol. 98, no. 2, pp. 167–282, 2010.

[5] http://www.eas.asu.edu/ptm/.

[6] M. Dragoman and D. Dragoman, *Nano Electronics-Principles and Devices*, Artech House, Boston, London, 2nd edition, 2010.

[7] J. J. Kim and K. Roy, "Double gate-MOSFET subthreshold circuit for ultralow power applications," *IEEE Transactions on Electron Devices*, vol. 51, no. 9, pp. 1468–1473, 2004.

[8] H. Soeleman, M. Seok, D. Sylvester, and D. Blaauw, "Nanometer device scaling in subthreshold logic and SRAM," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 175–185, 2008.

[9] S. D. Pable and M. Hasan, "High speed interconnect through device optimization for subthreshold FPGA," *Microelectronics Journal*, vol. 42, no. 3, pp. 545–552, 2011.

[10] W. Zhao and Y. Cao, "Predictive technology model for nano-CMOS design exploration," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 3, no. 1, pp. 1–17, 2007.

[11] H. T. Stephen, P. Xuan, J. Bokor, and H. Chenming, "Comparison of short-channel effect and offstate leakage in symmetric vs. asymmetric double gate MOSFET," in *Proceedings of the IEEE International SOI Conference Proceedings*, pp. 30–31.

[12] R. Vaddi, S. Dasgupta, and R. P. Agarwal, "Robustness comparison of DG FinFETs with symmetric, asymmetric, tied and independent gate options with circuit co-design for ultra low power subthreshold logic," *Microelectronics Journal*, vol. 41, no. 4, pp. 195–211, 2010.

[13] J. Deng and A. Wang, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—part I: model of the intrinsic channel region," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3186–3194, 2007.

[14] S. Frégonèse, C. Maneux, and T. Zimmer, "Implementation of tunneling phenomena in a CNTFET compact model," *IEEE Transactions on Electron Devices*, vol. 56, no. 10, pp. 2224–2231, 2009.

[15] H. S. P. Wong, J. Deng, A. Hazeghi, T. Krishnamohan, and G. C. Wan, "Carbon nanotube transistor circuits-models and tools for design and performance optimization," in *Proceedings of the International Conference on Computer-Aided Design (ICCAD '06)*, pp. 651–654, November 2006.

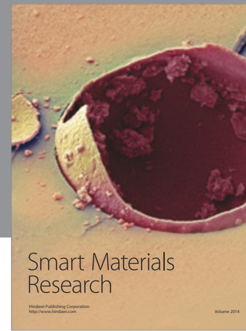
[16] N. Patil, J. Deng, S. Mitra, and P. H. S. Wong, "Circuit-level performance benchmarking and scalability analysis of carbon nanotube transistor circuits," *IEEE Transactions on Nanotechnology*, vol. 8, no. 1, pp. 37–45, 2009.

[17] R. Vaddi, S. Dasgupta, and R. P. Agarwal, "Device and circuit co-design robustness studies in the subthreshold logic for ultralow-power applications for 32 nm CMOS," *IEEE Transactions on Electron Devices*, vol. 7, no. 3, pp. 654–664, 2010.

[18] B. C. Paul, S. Fujita, M. Okajima, and T. Lee, "Impact of geometry-dependent parasitic capacitances on the performance of CNFET circuits," *IEEE Electron Device Letters*, vol. 27, no. 5, pp. 380–382, 2006.

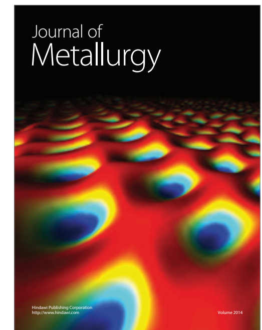
Journal of
Nanotechnology

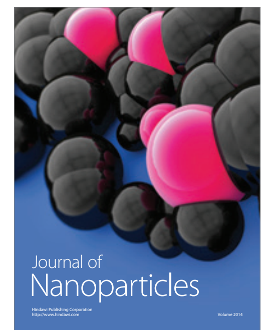
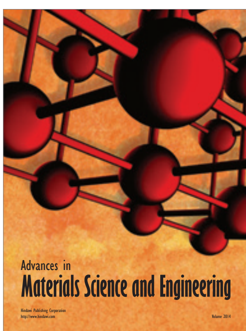
International Journal of
Corrosion

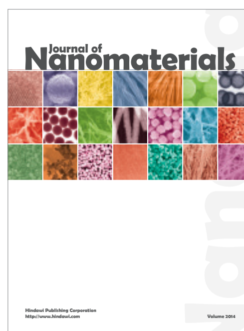
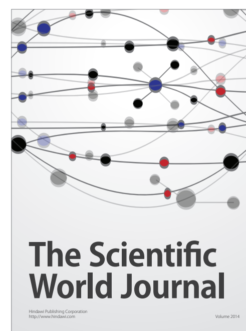
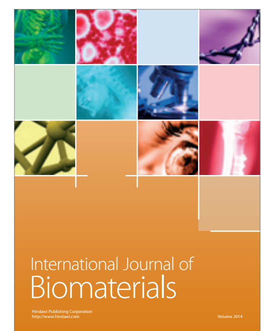
International Journal of
Polymer Science

Smart Materials
Research

Journal of
Composites

BioMed
Research International

Hindawi
Submit your manuscripts at
http://www.hindawi.com

Journal of
Metallurgy

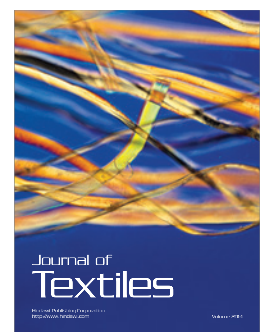
Journal of
Materials

Journal of
Nanoparticles

Advances in
Materials Science and Engineering

Scientifica

Journal of
Nanomaterials

The Scientific
World Journal

International Journal of
Biomaterials

Journal of
Nanoscience

Journal of
Coatings

Journal of
Crystallography

Journal of
Ceramics

Journal of
Textiles