



E-Band Transformer-Based Differential 4-Way Power-Combining Amplifier

Thian, M. (2014). E-Band Transformer-Based Differential 4-Way Power-Combining Amplifier. *Microwave and Optical Technology Letters*, 56(8), 1764-1770. DOI: 10.1002/mop.28433

Published in:
Microwave and Optical Technology Letters

Document Version:
Peer reviewed version

Queen's University Belfast - Research Portal:
[Link to publication record in Queen's University Belfast Research Portal](#)

Publisher rights
Copyright 2014 Wiley Periodicals, Inc.

This is the accepted version of the following article: Thian, M 2014, 'E-Band Transformer-Based Differential 4-Way Power-Combining Amplifier' *Microwave and Optical Technology Letters*, vol 56, no. 8, pp. 1764-1770., 10.1002/mop.28433, which has been published in final form at <http://onlinelibrary.wiley.com/doi/10.1002/mop.28433/abstract;jsessionid=1C9C2C750CE46C9679428CE5737A299B.f03t03>

General rights
Copyright for the publications made accessible via the Queen's University Belfast Research Portal is retained by the author(s) and / or other copyright owners and it is a condition of accessing these publications that users recognise and abide by the legal requirements associated with these rights.

Take down policy
The Research Portal is Queen's institutional repository that provides access to Queen's research output. Every effort has been made to ensure that content in the Research Portal does not infringe any person's rights, or applicable UK laws. If you discover content in the Research Portal that you believe breaches copyright or violates any law, please contact openaccess@qub.ac.uk.

E-Band Transformer-Based Differential 4-Way Power-Combining Amplifier

Mury Thian

The Queen's University of Belfast

Queen's Road, Queen's Island, Belfast BT3 9DT, U.K.

P: +44 (0)28 9097 1845, F: +44 (0)28 9097 1702, E: m.thian@qub.ac.uk

Abstract: This paper presents the design and implementation of a differential 4-way power-combining amplifier operating at E-band. The proposed 4-way power combiner (4WPC) facilitates short interconnects to the PA cells, thereby resulting in reduced loss. Simple *C-L-C* and *L-C* networks are deployed in order to compensate inductive loading due to the routing lines that would otherwise introduce mismatch and subsequently increase overall loss. Realized in SiGe technology, the PA prototype delivered 13.2 dBm output-referred 1-dB compression point and 14.3 dBm saturated output power when operated from a single 3.3 V DC supply at 75 GHz.

Keywords: Balun, cascode, common-mode rejection, differential circuits, E-band, HBT, MMIC, mm-wave, power amplifiers, power combiners, SiGe, transformers.

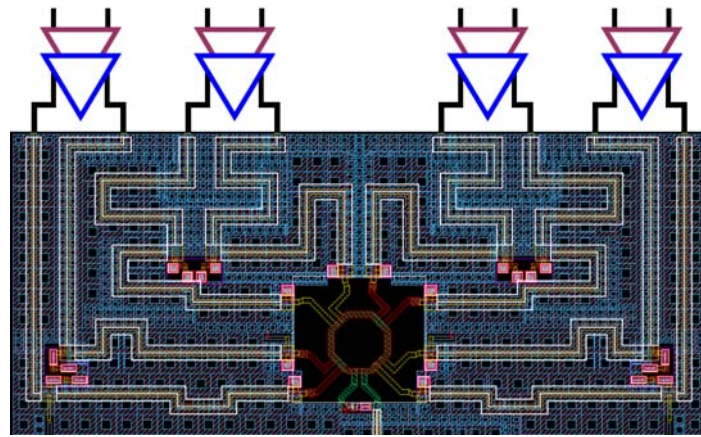
1. Introduction

Advances in silicon-based transistor scaling to few tens of nanometer have resulted in device transit frequencies (f_T) of several hundred GHz, and hence have enabled the development of transceiver ICs operating in mm-wave regime where large bandwidths required for high data-rate wireless links have been allocated. This high f_T , however, comes at the expense of lower

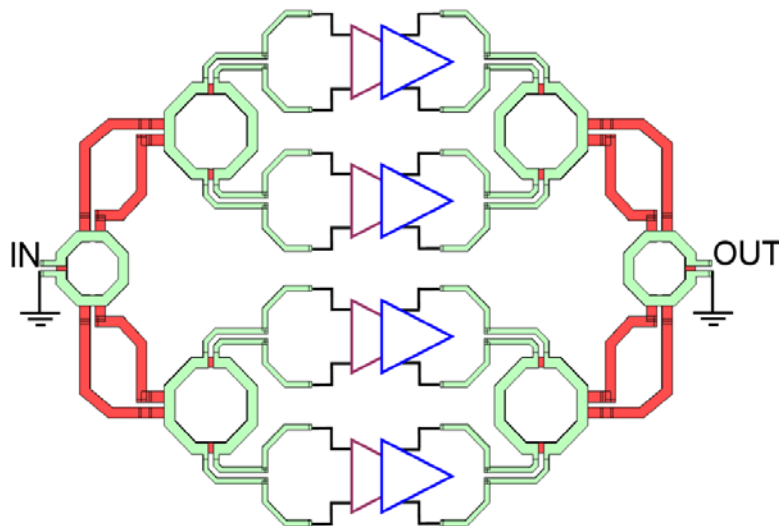
breakdown voltage, thus constraining the power-output capability of the transistor. This is of particular concern for medium-to-long range wireless data transmission due to substantial propagation path loss at mm-wavelengths. For illustration, the free-space propagation path loss at 80 GHz (E-Band) over a 10 m distance is 90.5 dB and for every tenfold increase in distance, the loss is further increased by 20 dB. This situation is exacerbated by additional loss due to rain, fog and atmospheric particles such as oxygen and water vapor. Deployment of effective power amplifiers (PAs) with high output power capability is therefore necessary to overcome these high path losses [1]-[3].

Passive power combining can be utilized, provided its insertion loss is less than the PA added power. Techniques to efficiently combine power from two or more PA cells on-chip have been reported in [4]-[8]. In [4], an eight-way power combiner (8WPC) was designed using microstrip lines with 1.1 dB/mm loss at 60 GHz. This combiner provided zero-degree phase translation and is only suitable for integration with single-ended PA topology. On the other hand, the two-way power combiners (2WPC) described in [5]-[7] are suitable for differential topology which itself offers a number of advantages over the single-ended type. These advantages include excellent noise immunity due to inherently high common-mode rejection ratio, significantly low even-order harmonic signal levels, and insensitivity to parasitic inductance between common emitter/source connection and ground. These types of combiners are synthesized based upon non-radiating evanescent-wave transformer concept, and therefore can provide impedance transformation and balanced-to-unbalanced conversion roles simultaneously, removing the need for additional matching elements and balun. Importantly, when compared to the classic Wilkinson combiner, they offer compact geometry and low insertion loss.

A more ambitious four-way power combiner (4WPC), also suitable for differential circuits, was recently introduced in [8]. It exhibited low insertion loss, just 1.25 dB, and features an extremely compact geometry since its output coil was vertically sandwiched between two input coils. The implementation strategy for this combiner, however, requires rather long (i.e. 540 μm) and thus lossy routing lines to connect the output of the PA cells and the input of the power combiner in order to ensure that the signals are combined constructively, Fig. 1(a).



(a)



(b)

Fig. 1. Differential 4-way power-combining amplifier architectures: (a) as in [8] and (b) proposed PCA.

In this paper we present holistic design and implementation of a new 4WPC variant depicted in Fig. 1(b) that significantly reduces the length of the routing lines and complexity required in [8]. The arrangement also includes a simple yet effective compensation technique that alleviates the detrimental effects of the parasitic inductive loading introduced by the interconnects. Common-mode rejection (CMR) characteristics of two elementary geometries of 2WPC, namely single- and double-loop, which are used to construct the 4WPC will be thoroughly investigated in order to identify which geometry provides better balance-to-unbalance conversion role, hence dispensing the need for additional baluns at both input and output ports.

The proposed power-combining amplifier (PCA) in Fig. 1(b) was specifically designed for E-band applications, for instance, wireless backhaul communications (81-86 GHz). Given the free-space path loss at 80 GHz is 90.5 dB over a 10-m distance and assuming the gain of transmit and receive antennas is 4 dBi each and the receiver sensitivity is -70 dBm, the output power of the PA is therefore aimed to be at least $90.5 - 70 - 4 - 4 = 12.5$ dBm.

The power splitter, driver cells, PA cells, and power combiner were designed and realized using the Infineon B7HF200 SiGe process [9]. High-speed (HS) rather than ultra-high-speed (UHS) NPN transistors are selected since they offer higher BV_{CEO} and BV_{CBO} values, 1.7 V and 6.5 V, respectively. The peak $f_T = 170$ GHz and the peak $f_{max} = 250$ GHz occur at a collector current density of $5 \text{ mA}/\mu\text{m}^2$. Four copper metal layers (M1–M4) are available for the implementation of passive components as well as DC and RF interconnects. The $2.8 \mu\text{m}$ thick topmost metal, M4, has DC current handling capability of $10 \text{ mA}/\mu\text{m}$. The bottom metal, M1, is typically used to provide a uniformly distributed DC voltage grid. Dielectric compounds sandwiched between two metal layers are composed of silicon dioxide (SiO_2) and silicon nitrate (Si_3N_4). The smallest available pad measures $68 \times 68 \mu\text{m}^2$ and it has an equivalent parasitic

capacitance, C_{PAD} , of about 25 fF. Metal-insulator-metal (MIM) capacitors as well as TaN and polysilicon resistors are also provided within the B7HF200 process.

2. Two-Way Power Combiner (2WPC)

Two elementary geometries for the 2WPC, namely single- and double-loop, are illustrated in Fig. 2. While the single-loop offers physically compact geometry, the double-loop can facilitate a shorter interconnect to the PAs, and therefore minimize the routing-line loss. The

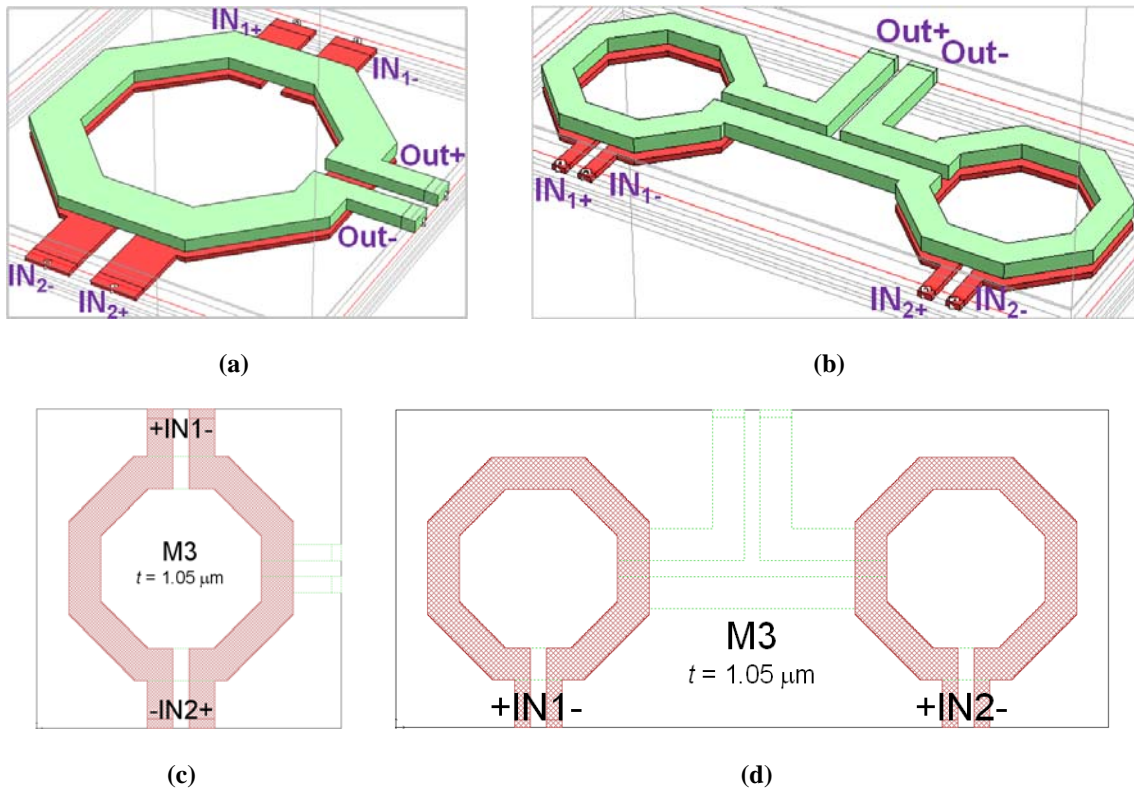


Fig. 2. Differential 2-way power combiner: (a) single-loop, (b) double-loop, (c) input coil of the single-loop, and (d) input coil of the double-loop.

inner diameter and trace width of the coils are set to 50 μm and 10 μm , respectively, in order to maximize self-resonance frequency (SRF) as well as to minimize metal losses. The centres of the two input coils in Fig. 2(d) are 135 μm apart. The self-inductance (L_{coil}) and fringing capacitance (C_{fringing}) of the input and output coils can be approximately estimated using (1) described in [10] and (2) in [11], respectively, where l , w and t denote the length, trace width and thickness of the associated metal conductors, and d is the vertical distance between the input and output coils.

$$L_{\text{coil}} = \frac{0.42\mu_0\ell}{\pi} \left\{ \ln\left(\frac{2\ell}{0.2235(w+t)}\right) + \frac{0.2235(w+t)}{\ell} - 1 \right\} \quad (1)$$

$$C_{\text{fringing}} = \frac{2\pi\epsilon_0\epsilon_r\ell}{\ln\left\{1 + \frac{2d}{t} + \sqrt{\frac{2d}{t}\left(\frac{2d}{t} + 2\right)}\right\}} \quad (2)$$

In order for the combiner to constructively combine two differential signals coming from two identical differential PA cells, it is required that the impedances seen at each input port of the combiner be identical. Any impedance mismatch will be translated into amplitude and phase imbalances and this would result in one PA cell being driven into early breakdown, and as a consequence, limit overall output power.

In PA design, differential topology is preferred to the single-ended type for the reasons mentioned in Section 1. On the other hand the filters and antennas that follow the PA typically have single-ended input ports. This dictates the need for a power combiner that can also function as a balun.

Tight magnetic coupling between the combiner's input and output coils intended for efficient power transfer and low loss unfortunately comes with unwanted large parasitic capacitance as a result of the overlapped area between the input and output coils. The overlapped area in the double-loop is twice as large as in the single-loop, and as a consequence, more

unevenly distributed parasitic capacitance is expected. Presented in Figs. 3(a) and (b) are the simulated real and imaginary parts of the differential input impedances of the single- and double-loop when the output ports, $Out+$ and $Out-$, are terminated in a differential fashion. For both geometries, the differential impedances seen at input ports 1 and 2 are identical, $Z_{diff_{IN1}} = Z_{diff_{IN2}}$. Consider now the case when the output ports are terminated in single-ended fashion, i.e., $Out-$ is grounded. It is shown in Figs. 3(c) and (d) that for the single-loop $Z_{diff_{IN1}} = Z_{diff_{IN2}}$,

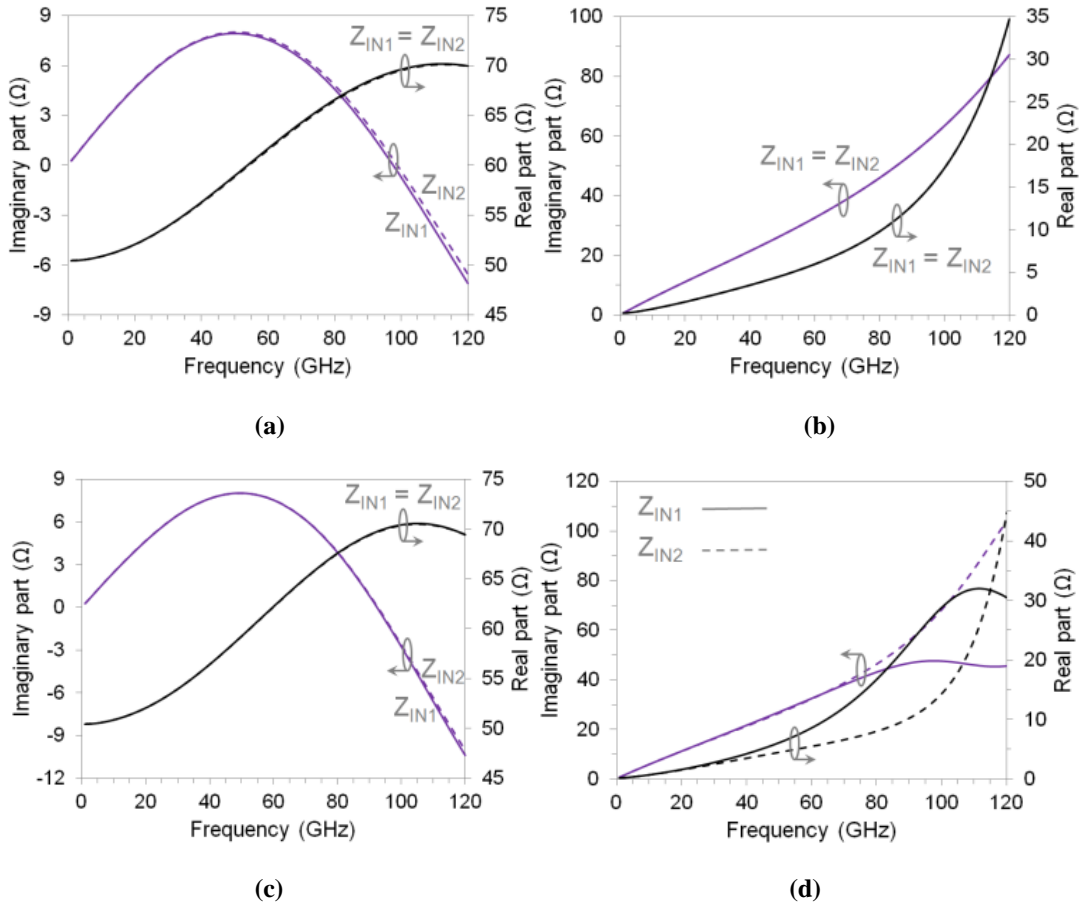


Fig. 3. Simulated input impedances: (a) and (b) single-loop and double-loop 2WPCs when the output ports are terminated in a differential fashion, respectively, (c) and (d) single-loop and double-loop 2WPCs when the output ports are terminated in a single-ended fashion, respectively.

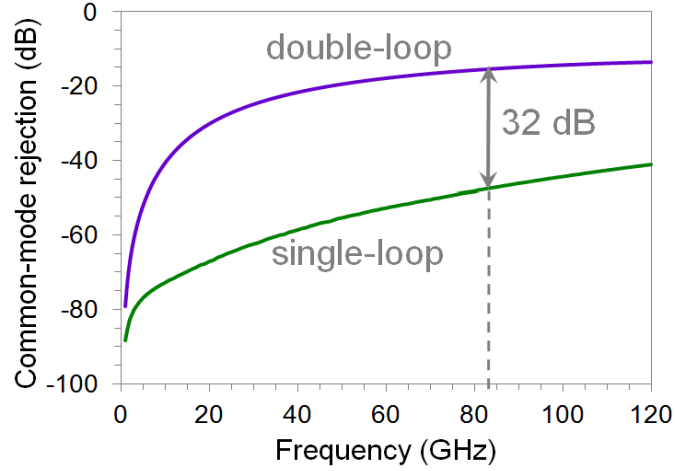


Fig. 4. Common-mode rejection characteristics of the single- and double-loop 2WPCs.

whereas for the double-loop $Z_{diff_{IN1}} \neq Z_{diff_{IN2}}$. The CMR characteristics of the single- and double-loop 2WPCs are presented in Fig. 4. Across the frequency band of interest, the single-loop exhibits over 30 dB better CMR than the double-loop. This implies that when compared to the double-loop, the single-loop exhibits better amplitude and phase balance characteristics, and therefore it can be simultaneously utilized as a balun.

3. Four-Way Power Combiner (4WPC)

The structure of differential 4WPC proposed in this paper is depicted in Fig. 5. It is comprised of three single-loop 2WPCs (rather than double-loop, for the reasons explained earlier): two input combiners with inner diameter 70 μm and one output combiner with inner diameter 50 μm . Shunt capacitances are employed at the input and output of each combiner in order to establish a resonant inductive coupling, and are realized using MIM capacitors whose values are optimized for minimum insertion loss and maximum return loss. In particular, the

design strategy takes advantage of the parasitic capacitance of the output pad, 25 fF, in order to absorb the required shunt capacitance at the output port of the combiner.

Routing lines that are used to provide electrical connections between the two input combiners and the output combiner (M3, Fig. 5) and between the input combiners and the PA cells (M4, Fig. 5) would introduce parasitic inductances and hence a mismatch. Higher loss would incur not only because of the electrical series resistance (ESR) of these lines but also as a direct consequence of the mismatch. To overcome this issue Π -type (C - L - C) and L-type (L - C) networks are proposed. The value of L is fixed based upon the length of the routing line required in the layout. The value of C is then computed and optimized in such a manner that the mismatch introduced by the network is minimized.

The 4WPC structure in Fig. 5 is optimised and simulated using a Method-of-Moment EM solver Sonnet®. At 83.5 GHz (i.e. midpoint of 81-86 GHz), the combiner exhibits 2.3 dB IL (~60% efficiency) implying that the power added resulted from employing the combiner is 3.7 dB. The structure in Fig. 5 is used to implement both power splitter and combiner deployed in the PCA in Fig. 1(b).

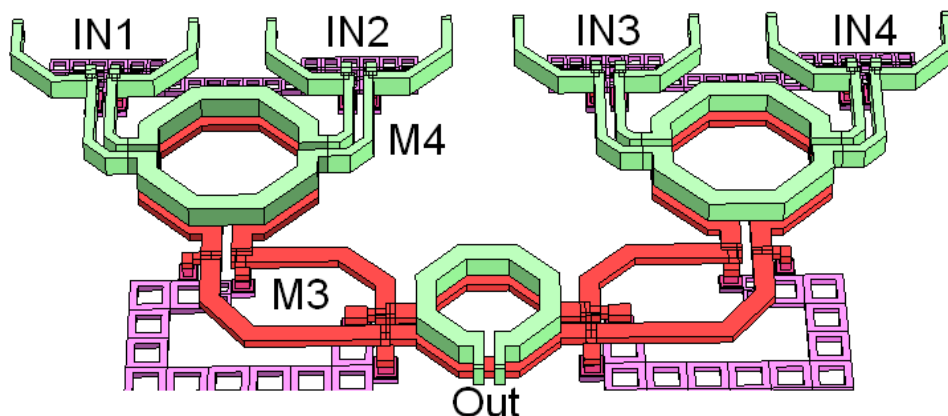
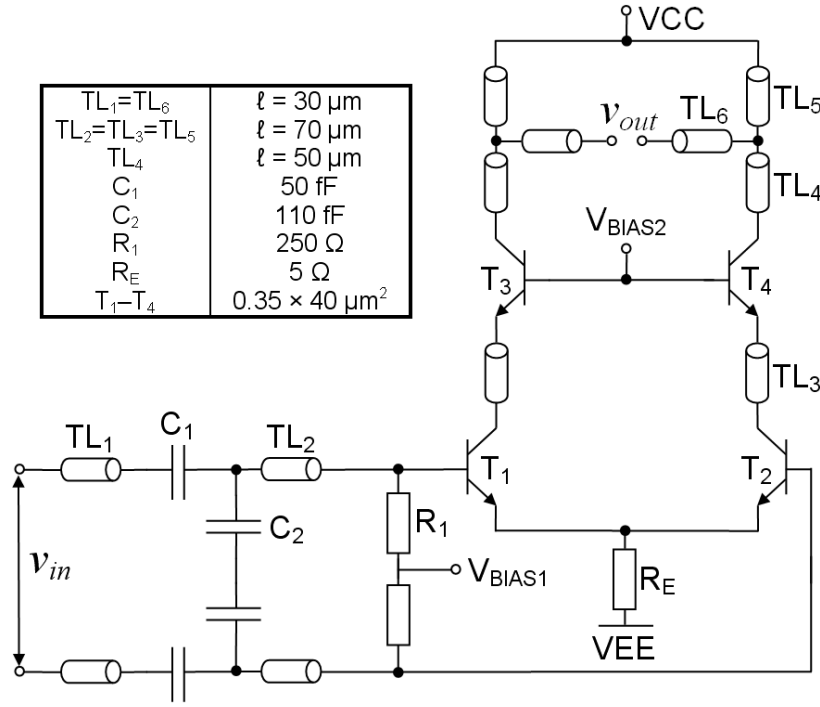


Fig. 5. Differential 4WPC including inter-stage matching circuits.

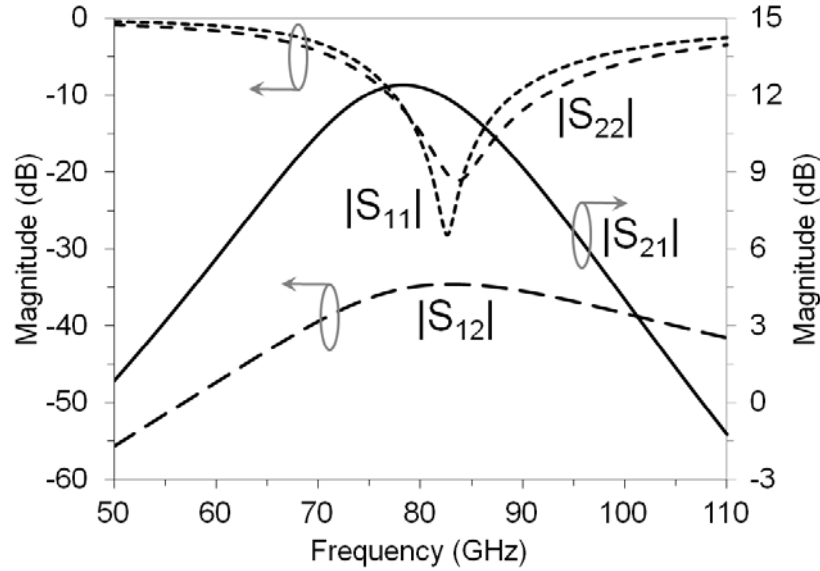
4. Power Amplifier and Driver Cells

The circuit schematic for the driver and PA cells is depicted in Fig. 6(a). The classical differential cascode topology, i.e., a common-emitter T_1 - T_2 followed by a common-base T_3 - T_4 is adopted so as to maximize gain and isolation between input and output ports. Input matching elements (TL_1 - TL_2 , C_1 - C_2) and output matching elements (TL_4 - TL_6) are incorporated in the circuit and their values presented in Fig. 6(a) are optimized at the E-band's center frequency 83.5 GHz. The series capacitance C_1 decouples any DC signals from the input port. On the other hand, no DC blocking capacitance is needed at the output port since the voltage drop across it is essentially zero, and as a result, no DC current will flow through it. The electrical length of TL_3 is optimized for bandwidth improvement. The characteristic impedance of TL_1 - TL_6 is 50Ω . The differential output port is matched to 50Ω rather than the typical 100Ω impedance, so as to enable the amplifier to achieve a given output power level but with reduced voltage swing across CE junction, aimed at preventing avalanche breakdown to occur.

A dedicated biasing circuit comprised of NPN and PNP current mirrors as well as diode-connected transistors, not shown in Fig. 6(a), is employed so as the amplifier can be conveniently operated from a single DC supply voltage, V_{CC} . The tail current is set to 70 mA in the PA cell and 30 mA in the driver cell. In order to ensure that the PA cell operates at peak f_T , the transistors T_1 - T_4 are biased at $5 \text{ mA}/\mu\text{m}^2$ collector current density, resulting in a tail current of $(0.35-0.17) \times (40-0.17) \times 5 \times 2 \approx 70 \text{ mA}$. Resistance R_E is used as a feedback means to stabilize any fluctuations in collector current due to, for instance, temperature changes and components aging.



(a)



(b)

Fig. 6. (a) Simplified schematic of the PA/driver cell and (b) simulated S -parameters of the PA cell.

Shown in Fig. 6(b) are the simulated S -parameter results of the PA cell. The input and output return losses, $|S_{11}|$ and $|S_{22}|$, are better than 10 dB from 77.5 GHz to 89 GHz. The small-

signal gain $|S_{21}|$ of at least 10 dB is obtained across 68.9 - 88.1 GHz frequency range and it reaches a peak 12.4 dB at 78-79 GHz. The simulated S -parameters of the driver cell are similar to those of the PA cell with the exception that the peak gain is 0.4 dB lower.

5. Measurement Results

For experimental verification, two chips prototypes have been designed and fabricated. The first chip shown in Fig. 7(a) consists of two identical 4WPC structures (Fig. 5) connected in a back-to-back configuration, one acting as a power splitter and the other as a power combiner. It occupies $1.028 \times 0.718 \text{ mm}^2$ die area including pads and dummy metals that are specifically introduced to meet the global metal density requirements of the foundry process. The second chip depicted in Fig. 7(b) contains the complete power-combining amplifier illustrated in Fig. 1(b). It measures $1.05 \times 0.51 \text{ mm}^2$ active die area excluding pads and dummy metals.

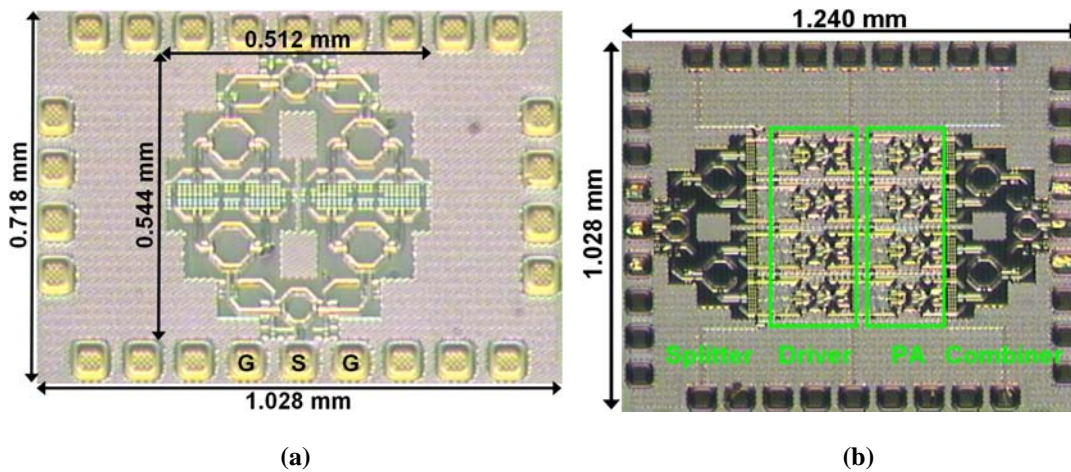


Fig. 7. Chip microphotographs: (a) the 4WPC structure connected in a back-to-back configuration and (b) complete PCA as in Fig. 1(b).

For on-chip small-signal measurements, an Agilent 110 GHz general-purpose network analyzer (PNA) and GSG Cascade probes with 100 μm pitch are used. On the other hand, an HP8350B source with 83558A 75-110 GHz extender and an Agilent E4407B spectrum analyzer with 11974W 75-110 GHz extender are used for large-signal measurements.

The simulated and measured S -parameter results of the chip in Fig. 7(a) are compared in Fig. 8. For convenience, a zoomed-in graph of measured $|S_{21}|$ is plotted on the top and right axis. A broadband characteristic is observed in the simulation with half-circuit's IL of better than 3 dB obtained from 79.7 GHz to 93 GHz. The minimum IL 2.2 dB is achieved at around 87 GHz. At the center frequency 83.5 GHz, the simulated IL is 2.5 dB compared to 2.3 dB in Section 3. Simulated input and output return losses are higher than 9 dB from 78 GHz to 91 GHz. On the other hand, measured IL of about 3.5 dB is obtained from 78 GHz to 84 GHz. Measured I/O return loss is higher than 10 dB from 73.5 GHz to 90 GHz, demonstrating broadband matching

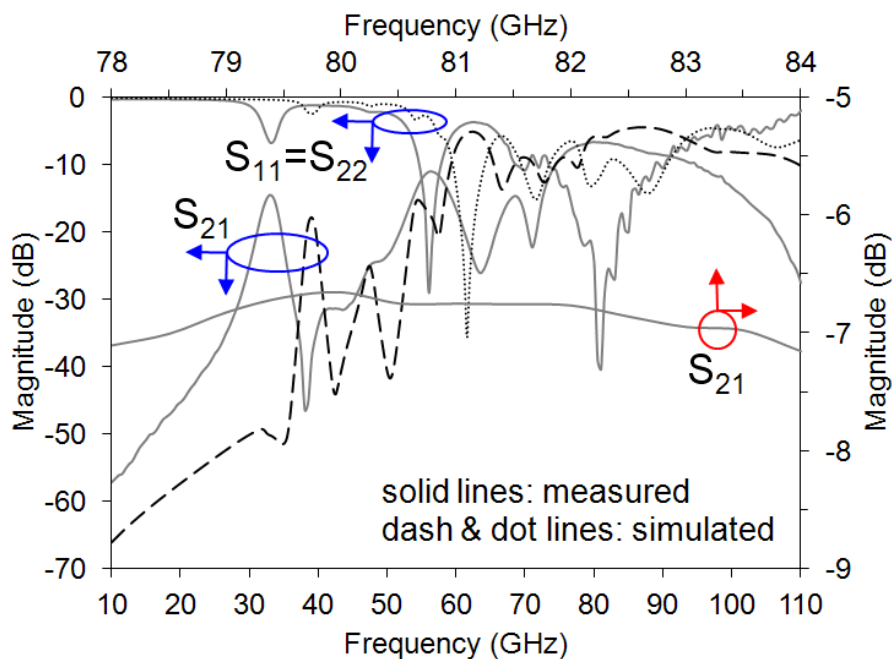


Fig. 8. Measured and simulated S -parameters of the chip in Fig. 7(a).

capability. Frequency shift and higher IL observed in the measurements are likely due to inadequate modeling of substrate capacitive coupling whose effects are detrimental at mm-wave frequencies.

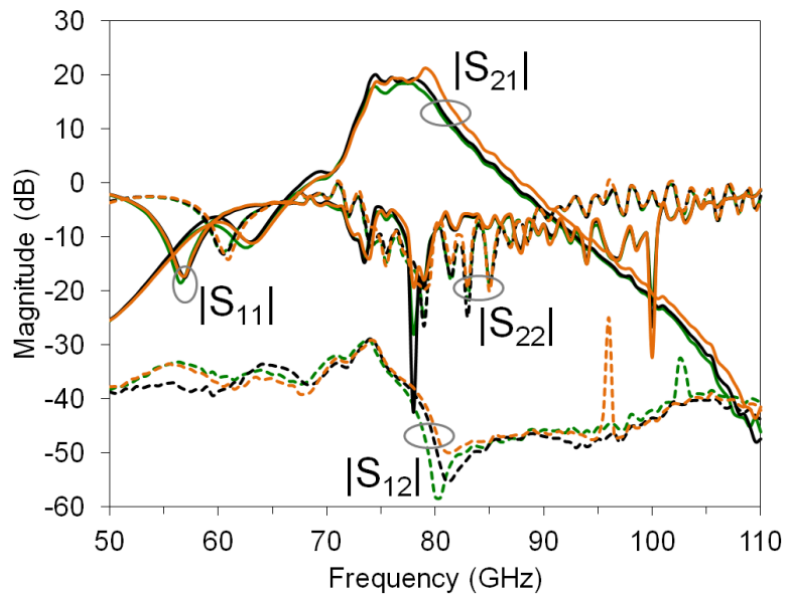


Fig. 9. Measured S -parameters of the PCA for three chip die.

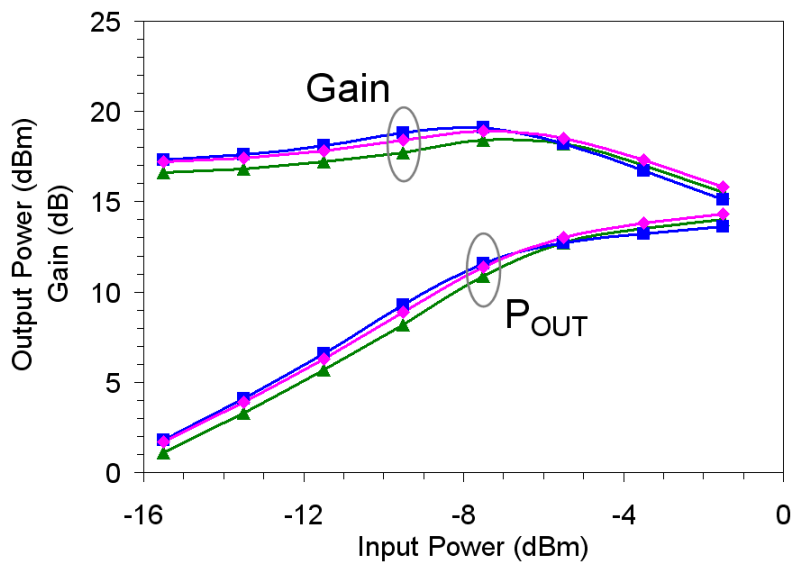


Fig. 10. Measured output power and gain versus input power at 75 GHz and $V_{CC} = 3.3$ V for three chip die.

Fig. 9 presents measured S-parameters of the PCA chip in Fig. 7(b). In order to investigate process variation, three chip die were measured. Measured $|S_{21}|$ of at least 17 dB is obtained from 74.5 GHz to 80.5 GHz with a peak of 21 dB occurred at 79 GHz. Plotted in Fig. 10 are the measured output power and gain versus input power at 75 GHz when the amplifier is operated from $V_{CC}=3.3V$. Measured output-referred 1-dB compression point, OP_{-1dB} , is 13.2 dBm and saturated output power, P_{SAT} , is 14.3 dBm. Further, the frequency response of the amplifier is given in Fig. 11 for $V_{CC} = 3 V$ and 3.3 V. Across 75-81 GHz, for $V_{CC} = 3.3 V$, P_{SAT} is higher than 10.4 dBm and gain is higher than 14.4 dB.

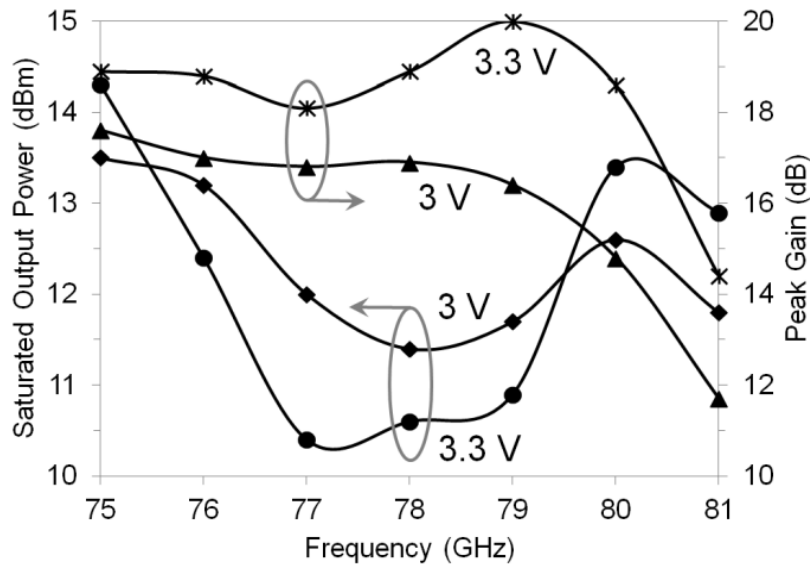


Fig. 11. Measured saturated output power and peak gain versus frequency for two V_{CC} values.

6. Conclusion

A differential 4-way power combiner with low loss and high CMR characteristics that allows full integration with the PA cells on the same chip has been successfully designed and implemented in SiGe technology. Measured insertion loss of the combiner is 3.5 dB from 78

GHz to 84 GHz and return loss is better than 10 dB from 73.5 GHz to 90 GHz. A PCA prototype, comprised of a power splitter, two-stage cascode PA array and a power combiner, has also been built and it delivered 13.2 dBm OP_{-1dB} and 14.3 dBm P_{SAT} when operated from a single 3.3 V DC supply at 75 GHz.

7. Acknowledgments

This work was supported by FP7 Marie Curie IAPP under GigaRadio project. The author wishes to thank Dr Marc Tiebout and Dr Franz Dielacher (Infineon Technologies, Austria) for fruitful technical discussions and Dr Neil Buchanan (the Queen's University of Belfast) for the measurement assistance.

8. References

- [1] U.R. Pfeiffer, S.K. Reynolds, and B.A. Floyd, A 77 GHz SiGe power amplifier for potential applications in automotive radar systems, IEEE Radio Frequency Integrated Circuits (RFIC), Fort Worth, Texas, Jun. 2004, pp. 91-94.
- [2] J. Lin, K. To, D. Hammock, B. Knappenberger, M. Majerus, and W. Huang, Power amplifier for 77-GHz automotive radar in 90-nm LP CMOS technology, IEEE Microw. Wireless Compon. Lett. 20 (2010), 292-294.
- [3] V. Giannello, E. Ragonese, and G. Palmisano, A transformer-coupling current-reuse SiGe HBT power amplifier for 77-GHz automotive radar, IEEE Trans. Microw. Theory Tech. 60 (2012), 1676-1683.

- [4] B. Martineau, V. Knopik, A. Siligaris, F. Ganesello, and D. Belot, A 53-to-68GHz 18 dBm power amplifier with an 8-way combiner in standard 65 nm CMOS, IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2010, pp. 428-429.
- [5] Y. Zhao, J.R. Long, and M. Spirito, Compact transformer power combiners for millimeter-wave wireless applications, IEEE Radio Frequency Integrated Circuits (RFIC), Anaheim, CA, May 2010, pp. 223-226.
- [6] S. Aloui, Y. Luque, N. Demirel, B. Leite, R. Plana, D. Belot, and E. Kerherve, Optimized power combining technique to design a 20 dB gain, 13.5 dBm OCP1 60 GHz power amplifier using 65 nm CMOS technology, IEEE Radio Frequency Integrated Circuits (RFIC), Montreal, Canada, Jun. 2012, pp. 53-56.
- [7] Q. J. Gu, Z. Xu, and M.-C.F. Chang, Two-way current-combining W-band power amplifier in 65-nm CMOS, IEEE Trans. Microw. Theory Tech. 60 (2012), 1365-1374.
- [8] M. Thian, M. Tiebout, N.B. Buchanan, V.F. Fusco, and F. Dielacher, A 76-84 GHz SiGe power amplifier array employing low-loss four-way differential combining transformer, IEEE Trans. Microw. Theory Tech. 61 (2013), 931-938.
- [9] J. Böck, H. Schäfer, K. Aufinger, R. Stengl, S. Boguth, R. Schreiter, M. Rest, H. Knapp, M. Wurzer, W. Perndl, T. Böttner, and T.F. Meister, SiGe bipolar technology for automotive radar applications, IEEE Bipolar/BiCMOS Circuits Technology Meeting (BCTM), Montreal, QC, Canada, Sep. 2004, pp. 84-87.
- [10] F.W. Grover, Inductance Calculations, Princeton, New Jersey: Van Nostrand, 1946.
- [11] Y. Eo and W. Eisenstadt, High-speed VLSI interconnect modeling based on S-parameter measurements, IEEE Trans. Compon., Hybrids, Manuf. Technol. 16 (1993), 555-562.