

**ELECTRON PROPERTIES IN
DIRECTED SELF-ASSEMBLY GE/SIC/SI QUANTUM DOTS**

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University of Pittsburgh, 2014

Artificially ordered semiconductor quantum dot (QD) patterns may be used to implement functionalities such as spintronic bandgap systems, quantum simulation and quantum computing, by manipulating the interaction between confined carriers via direct exchange coupling. In this dissertation, magnetotransport measurements have been conducted to investigate the electronic orbital and spin states of directed self-assembly single- and few-Ge/SiC/Si QD devices, fabricated by a directed self-assembly QD growth technique developed by our group. Diamagnetic and Zeeman energy shifts of electrons confined around the QD have been observed from the magnetotransport experiments. A triple-barrier resonant tunneling model has been proposed to describe the electron and spin transport. The strength of the Coulomb interaction between electrons confined at neighboring QDs has been observed dependent on the dot separation, and represents an important parameter for fabricating QD-based molecules and artificial arrays, which may be implemented as building blocks for future quantum simulation and quantum computing architectures.

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PREFACE

This Ph.D. thesis contains the result of research undertaken at the Department of Physics and Astronomy of the University of Pittsburgh. This research was realized within the project: Spintronic Bandgap Materials, funded by the U.S. Department of Energy (DOE). Certainly, I would have never reached the point of finishing my dissertation without the help and support of others.

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1 QUANTUM SIMULATION WITH QUANTUM DOTS

1.1 INTRODUCTION OF QUANTNUM DOT

Quantum dot (QD) is defined as a three-dimensionally confined semiconductor quantum well (QW). Such QDs, coined as “artificial atoms”, typically consist of a few hundred to a few million atoms and behave in many ways like single atoms [1]. QDs exhibit quantum effects associated with their atomic counterparts, e.g. few electrons are held together by the nuclear potential. It is also expected that zero-dimensional confinement can yield the characteristic structure of a series of isolated current or optical spectrum peaks that can be studied by electronic transport [2, 3] and photo excitation [4] through a discrete spectrum of states.

QD architectures have been proposed as an excellent platform on which control over electron/spin interactions at Hamiltonian level can be effectively implemented. Thus QD architectures can serve as an essential approach to realize apparatus such as spintronic devices [5-9], quantum information and computing [10], and quantum simulation [11-15]. QDs have also been widely used in electronic devices [16-22], photonic devices [23-26], light-emitting devices [27-33], cellular automata [34], and solar cells [35-37].

In this chapter, the theory and experiments of quantum simulation (QS) and quantum computing (QC) will be introduced to demonstrate the advantages of QD-based architectures as one of the motivations, followed by a brief review of fabrication techniques, characterization methods and electronic structures of semiconductor QDs.

1.2 QUANTUM SIMULATION BASED ON QD SYSTEMS

Quantum simulation can be defined as the intentional mapping of quantum dynamics of one physical system onto another quantum system, one that is typically more controllable. Richard Feynman first proposed this idea for efficient simulation of quantum systems [11]. In quantum mechanics, it is common that physical problems turn out to be extremely difficult to simulate on a classical computer because they need to enumerate quantum states one at a time and also because of the exponential proliferation of quantum states required to characterize a large system. Examples of such problems are plenty, such as study of quantum phase transitions [38], computing molecular energy levels [39], etc. Quantum simulation, however, employs a controlled quantum-mechanical device to mimic and investigate other quantum systems. The controlled quantum-mechanical devices used to mimic other quantum systems in quantum simulation are defined as quantum simulators.

Two types of quantum simulators have been proposed for physical realization: analog quantum simulator (AQS) and digital quantum simulator (DQS) [14] as schematically illustrated in Fig. 1.1. A device that maps the evolution of a quantum system and its dynamics, as discussed above, is referred to as an AQS. AQSs have been successfully constructed using a variety of quantum architectures. Atoms in ultracold quantum gases confined by optical lattice have been used to mimic condensed matter systems [40-43]. Circuit excitations in superconducting circuits [44] and single photon systems are promising platforms for simulating quantum phenomena of small-sized quantum systems. Trapped atomic ions held in radiofrequency traps enable the construction of a wide range of Hamiltonians so that various quantum simulations can be implemented [45]. With a DQS, the state of the system to be simulated is encoded in a register of quantum information carriers. The dynamics is approximated with elementary quantum gates,

and implemented in a circuit. In a DQS, the propagator describing the dynamical evolution is constructed from a sequence of quantum gates. The main steps of a DQS consist of preparing the input state, evolving it over a time t and carrying out measurements on the evolved state to extract the physical information of interest. The time evolution of the simulator is designed to match the time evolution of the model system to be simulated. DQS is very flexible as it can, in principle, be reprogrammed to efficiently simulate arbitrary quantum systems whose dynamics are determined by local interactions [12] and is therefore referred to as a universal quantum simulator (UQS) [12]. The idea of UQS is further developed and described as a universal quantum computer [46]. Also, methods to efficiently correct for and quantitatively bound experimental error have been studied to implement large-scale digital simulations [47]. The digital approach has been experimentally explored with various physical systems. For example, a DQS has been implemented with Nuclear magnetic resonance (NMR) systems to study two- and three-body interactions [15]. Trapped ion systems have been used to simulate the full time dynamics of a range of spin systems [48] and to simulate spin-spin interactions [49].

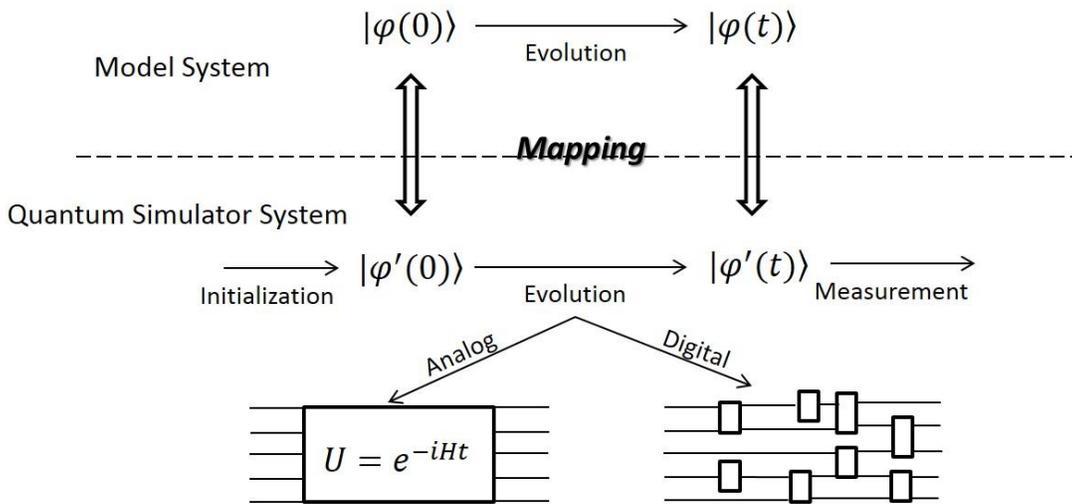


Figure 1.1 Principles of quantum simulation. A quantum simulation starts with mapping the initial state $|\varphi(0)\rangle$ of a model system to $|\varphi'(0)\rangle$ in a quantum simulator system. The time evolution of the simulator is designed to match the evolution of the model system in either analog or digital approach. In the end the evolved state is measured to extract the physical information of the model system. (Figure is adapted from [49])

Quantum simulation based on germanium/silicon-carbide/silicon quantum dot (Ge/SiC/Si QD) system motivates the research described in this dissertation. One attractive feature of using semiconductor systems is that very low relevant temperatures may be reached. The temperature of the semiconductor system can be controlled using a dilution refrigerator. Therefore energy regimes which are interested to the simulation are accessible [50]. Another feature is that due to the long-ranged Coulomb interaction between electrons confined around QDs, the interdot interaction can be tuned by controlling the QD separation. The spin exchange interaction can also be well modulated by applying external magnetic and electric fields [51]. Thirdly, the enhanced spin lifetime in Si and extended transport length originating from weak spin-orbit coupling and lattice inversion symmetry exceeds the time required for quantum gate operation and the spin transport coherence length, respectively [52]. Compared with other systems such as cold atoms, trapped ions and NMR systems, silicon-based architectures are more easily scaled and integrated with existing Si technology.

AQS is anticipated to be useful for helping to provide insight into the physics of quantum material systems. A QD array architecture has been proposed as an AQS to simulate the system of a Cu-O plane in copper-oxide superconductors [53]. An AQS can also be constructed for a Fermi-Hubbard model using a coupled semiconductor QD array confined in a semiconductor two-dimensional-electron-gas (2DEG) system [50]. For a given average electron number in the

QDs, the low-energy physics can be described by an effective one- or two-band Hubbard model [50].

This AQS can be generalized to different lattice geometries by adjusting the gate design and applied gate voltage. Manipulating the long-ranged Coulomb interaction between QDs allows the simulation of two-dimensional Hubbard model that describes strongly-correlated phenomena such as metal-insulator transitions [54] and magnetism [55].

Artificially arranged Ge/SiC/Si QDs can be considered as a promising architecture for AQS if one can manipulate the electronic states confined by the QDs and if the inter-QD (interdot) interaction can be modulated. Pryor, et. al. proposed a method to manipulate the confined electronic states and the interdot interactions in an artificially ordered Ge/Si QD system by varying QD spacing or by applying electrical fields [51]. This method provides a clue to implementing Ge/SiC/Si QDs as an AQS due to the similar type-II band edge alignment of Ge/SiC/Si and Ge/Si QD (Details discussed in section 1.2.3). Compared with AQS that performs dedicated tasks to solve specific Hamiltonians, making a QD-based UQS or quantum computer that performs operations at the qubit level is a far more difficult task.

Quantum computation (QC) architectures have been proposed based on QD system with various QD spatial configurations. D. Loss and D. DiVincenzo first proposed that quantum computing can be implemented by spin states of coupled single-electron QDs [56]. An efficient universal quantum computation (UQC) architecture that uses pairs of spin-1/2 particles to form logical qubits, and Heisenberg exchange to produce all gate operations was presented [57]. In this architecture, a decoherence-free (DF) subspace is constructed and the physical qubits, i.e. the spin-1/2 pairs, evolve in this DF-subspace. Therefore a DF-UQC is possible within this architecture. Heisenberg interaction between neighboring QDs alone has been theoretically

studied to implement UQC. Compared with the earlier proposed QC architecture in Ref. [56], the complexity of one-qubit operations in this architecture can be effectively reduced to accelerate the QC progress [58], even though three physical qubits (QDs) are required to encode one logic qubit as schematically demonstrated in Fig. 1.2. One-way quantum computation is an alternative QC architecture that can be implemented by QDs [59]. The architecture consists of single qubit measurements on a prepared cluster state. A cluster state is a particular type of highly entangled state, which can be generated in lattices with Ising type of interactions [60]. Quantum logic circuit is created by the single qubit measurements that destroy the entanglement of the cluster state at the same time. Cluster states have been created by atom qubits in optical lattices by Mandel, etc., [61]. However these cluster states are not suitable for QC because the atom qubits are too close in the optical lattices (~ 410 nm in Ref. [61]) to measure single atoms. In QD systems, this challenge can be solved as inter-QD interaction can be long-range ($\sim \mu\text{m}$) and the electron/spin states of QDs can be measured individually [62-64].

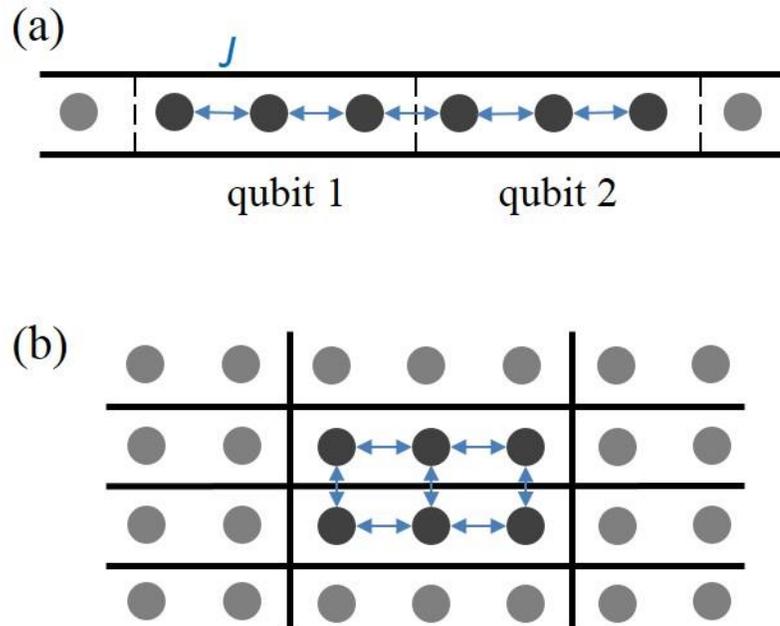


Figure 1.2 Possible layouts of QD architectures for Heisenberg interaction QC [58] for (a) One-dimensional layout, and (b) Two-dimensional layout. Three QDs are required to encode one logical qubit and the Heisenberg interaction J is represented by blue arrows.

The architectures described above use one, two or three QDs to encode one logical qubit and up to about ten QDs to produce one two-qubit operation [57, 58]. Each architecture requires specific QD spatial arrangements [65]. Besides challenges in positioning QDs with high precision, one needs to find an approach to externally manipulate quantum states, to preserve the quantum coherence of these states for some time and to transport the states at a macroscopic distance before the quantum information is dissipated. To accomplish these tasks, this dissertation focuses on growing directed self-assembled Ge/SiC/Si QDs and QDMs with various spatial configurations, integrating QD/QDM structures into vertical transport electronic devices (refer as QD/QDM devices); conducting magnetotransport measurements on the QD/QDM devices; investigating electron states confined around the QDs and exploring interdot electron interactions with respect to QD spatial configurations.

1.3 QUANTUM DOT FABRICATON

QDs were first discovered in 1980s in semiconductor microcrystals grown in a dielectric matrix [66]. Since then, several methods have been developed for QD fabrication.

One widely used fabrication method is the self-assembly of QD islands by molecular beam epitaxy (MBE) in Stranski–Krastanov (S-K) growth mode [67]. Self-assembly QDs spontaneously nucleate when a material is grown on a substrate to which it is not lattice matched. The strain from the lattice mismatch produces coherently strained islands on top of a two-dimensional initial layer of atoms, usually referred to as a wetting layer. For epitaxial thin film growth, there are two other possible growth modes: Volmer-Weber (V-W) mode and Frank-van der Merwe (F-vdM) mode as shown in Fig. 1.3. The VW growth occurs where interactions among adatoms are stronger than those of the adatom with the surface. Therefore the interface energy alone is sufficient for island formation in three dimensions (3D) [68]. During FM growth, adatoms prefer to attach to surface sites, leading to atomically smooth two-dimensional (2D) layers. The 2D layer-by-layer growth indicates a complete formation of films before growth of subsequent layers [68]. S-K growth is a process represented by both 2D wetting layer growth and 3D island formation. Transition from the layer-by-layer to island growth occurs at a critical layer thickness. The critical thickness has been found highly dependent on the surface energies and lattice parameters of the grown film and substrate [69].

Taking growth of Ge QDs on Si substrate in S-K mode as an example, Ge initially wets the Si surface and grows 2D layers due to the low surface energy of Ge. A 4.2% lattice mismatch between Ge and Si ($a_{Ge} = 5.65 \text{ \AA}$, $a_{Si} = 5.43 \text{ \AA}$) causes a linear increase in film elastic energy during the layer growth. As the layer grows, the elastic energy increases and drives a layer-to-

island transition at a critical thickness near three monolayers (ML) [67]. Initially, islands forming on the wetting layer are coherent or defect free. These nanoscale coherent islands are the self-assembling QDs. A substantial fraction of the mismatch induced strain is relieved by elastic deformation of the substrate. As the QDs grow, the QDs' shape changes in order to minimize their free energy [70-72]. Continued growth causes the coherent islands to dislocate which dramatically reduces the QD chemical potential [67, 73]. Critical thickness and critical size at which the dislocation is introduced into the initially coherent Ge QDs have been calculated by Cabrera, etc. [74].

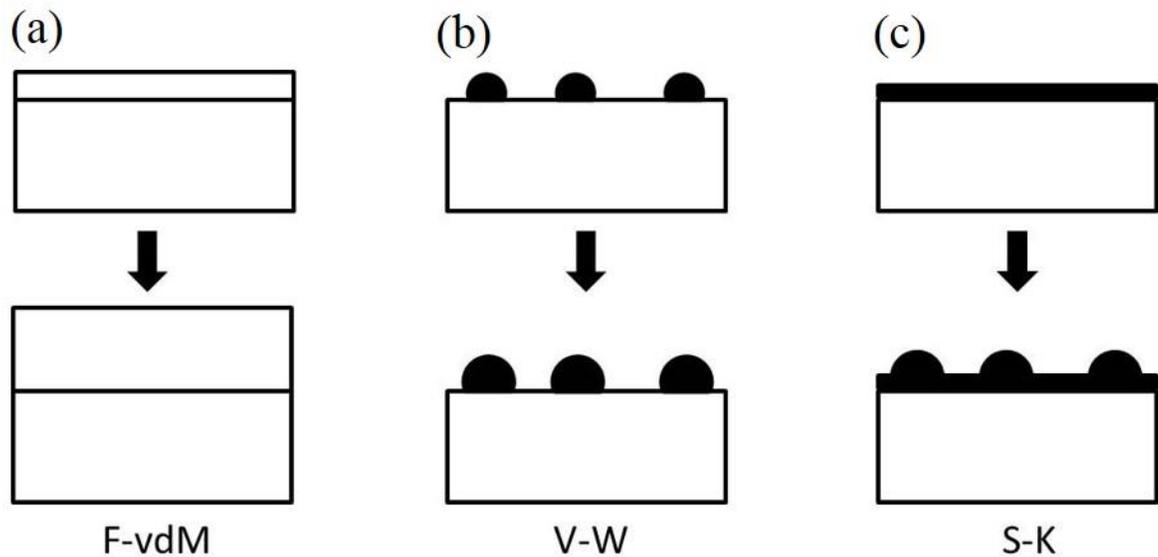


Figure 1.3 Three possible epitaxial growth modes. (a) Frank-van der Merwe (F-vdM) mode, (b) Volmer-Weber (V-W) mode, (c) Stranski-Krastinov (S-K) mode. Where interface energy alone is sufficient to cause island formation, VW growth will occur; S-K growth is uniquely confined to systems where the island strain energy is lowered by misfit dislocations underneath the islands.

Starting from a single layer inhomogeneous QDs, by subsequent multilayer MBE growth, vertically stacked QD structures can be obtained on top of the initial layer of QDs separated by

spacer layers. An example is a structure that consists of successive layers of pure Ge or of SiGe alloys separated by Si barrier layers [75-78]. The QDs in the upper layers grow on the top of the buried ones, giving rise to a vertical correlation between islands along the growth direction. This vertical self-organization has been observed both for InAs/GaAs [79, 80] and Ge/Si [75, 78] QD systems. The origin of the vertical correlation is attributed to inhomogeneous strain fields induced by the buried islands [73]. Electron properties has been investigated for vertical QD molecules both theoretically [81] and experimentally [76]. Vertically correlated QDs can form vertical QDMs. Electronic/magnetic properties and interdot interactions of a vertical QDM can be tuned by applying external electric/magnetic fields and by adjusting the thickness of the spacing layer respectively [81]. In vertically correlated QDs, the depth of the potential well confining carriers increases due to accumulation of strain energy from different dot layers [78]. Therefore carriers are localized more strongly in multilayer QD structures than in single layer QDs. An enhanced efficiency of photo- and electroluminescence [82], photo detectors [83] and solar cells [84] has been reported due to strongly localized electron states in multilayer Ge/Si QD structures. Despite of all these advantages, scaling the self-assembly approaches to larger two-dimensional crystals with nanoscale QDs has not yet been worked out.

The main limitations of self-assembly growth method are the cost of fabrication, difficulties in optimizing growth parameters such as deposition rate and substrate temperatures, the lack of control over positioning individual QDs, and the challenge in obtaining uniform QD size distribution. The non-uniformity of QD size distribution is caused by the Ostwald ripening process, in which larger islands grow at the cost of smaller islands. Surface energy minimization is the driving force of Ostwald ripening effect [73].

Another method that has been frequently used to fabricate QD is creating quantum confinement in a semiconductor heterostructure by lithographic patterning of surface gates, i.e., depositing metal electrodes on heterostructure surface. Individual QDs can be created from two-dimensional electron or hole gases in QWs or semiconductor heterostructures. This type of QD is called lateral QD. Sample surface is first coated with a thin layer of resist. A lateral pattern is then defined in the resist by lithography techniques. This pattern can then be transferred to electron or hole gas by etching, or by depositing metal electrodes that allow application of external voltages between the electron or hole gas and the electrodes.

Experimentally, electrode patterning has been facilitated by nano-imprinting or lithography techniques such as electron beam lithography (EBL), focused beam implantation (FIB), focused laser beam (FLB), etc. 2DEG heterostructures form in the system of GaAs/AlGaAs [85-87], InAs/GaAs [88], GaSb/GaAs [89, 90], Ge/Si [77], etc. Lateral QDs are mainly of interest for experiments and applications involving electron or hole transport. Flexibility of lithography techniques enables fabrication of complex QD devices such as: double-QD with quantum point contact for charge sensing [87, 91], QD-based single electron transistor [92-96], etc. Similarly, a carbon nanotube quantum dot (CNT QD) can be fabricated when electrons are confined to a small region within a carbon nanotube by applying voltage to gate electrodes, thereby causing electrons to accumulate in the vicinity of the electrode. Metallic leads are then laid over the nanotube in order to connect the CNT QD to an electrical circuit [97-99] for electron transport characterization.

The advantage of lithography fabrication method is that QD and electrical circuit can be geometrically defined for various device purpose. While its disadvantage is that, QD size is normally larger than 100 nm in diameter due to insufficient resolution of lithography techniques

and QDs cannot be scaled up to create macroscopic QD superlattice because of slow speed of the process.

To engineer size, shape and position of QDs in fabrication process, a so-called twofold cleaved-edge overgrowth (CEO) method has been developed. The twofold CEO method is an MBE growth technique that uses regrowth of QDs on cleaved edge of a multilayer sample. This method has proven to be a powerful technique for fabricating highly uniform QDs at the intersection of QWs [100-103]. With atomic control of size and position of CEO QDs, coupled QDMs were fabricated at the intersection of GaAs/AlGaAs QWs by Wegscheider, etc. [103] Schedelbeck, etc. reported a control of inter-QD coupling strength in a CEO QDM by adjusting spatial distance between QDs [101]. Although the uniformity and position control of CEO QDs is greatly enhanced compared with that of self-assembled QDs, fabricating CEO QDs/QDMs is challenged by complex MBE growth procedures and limited by material properties.

Other examples of QD fabrication methods are chemical vapor deposition (CVD) and colloidal synthesizing. CVD technique was first reported for fabricating a layer of isolated Si QDs by Nakajima, etc. [104]. In their work, a conventional low-pressure chemical vapor deposition (LPCVD) was used for an extremely short deposition time in the early stage of Si film growth. Si QDs with 5 ~ 20 nm in diameter and 2 ~ 10 nm in height were obtained resulting from a deposition time of 60 seconds. Colloidal semiconductor QDs are synthesized from precursor compounds dissolved in solutions [105, 106]. The synthesis of colloidal QDs is based on three components: precursors, organic surfactants, and solvents. When a reaction medium is heated to a sufficiently high temperature, the precursors chemically transform into molecules that may bind chemically to other molecules. Once these molecules reach a high enough level, the QD

growth starts with a nucleation process [107]. Colloidal QDs are normally 20 ~ 200 Å in diameter, depending on the materials. Many different semiconductor QDs can be produced by colloidal methods. Typical QDs are made of binary alloys such as CdSe [108], CdS [109], InAs [110], and InP [111]. For example, InAs QDs can be prepared via colloidal chemical synthesis using the reaction of InCl_3 and $\text{As}[\text{Si}(\text{CH}_3)_3]_3$. The synthesized InAs QD size ranges from 25 to 60 Å in diameter with size distributions of $\pm 10\% \sim 15\%$ [110]. Large batches of QDs can be synthesized via colloidal synthesis. Therefore colloidal synthetic methods are widely used for commercial applications such as solar cells [36, 106] and light-emitting diodes (LED) [112-114]. However, the lack of position control of individual QDs hinders their application in single- or few-QD electronic/spintronic devices.

Conclusion

Although size- and position-control by lithography patterning method is superb, this approach is slow, and unlikely to meet the demand of fabricating macroscopic arrays of QDs for practical applications. On the other hand lithographic approaches are limited by insufficient resolution to produce the nanometer scale QDs we are interested in. Self-assembly in nature leads to pattern formation at characteristic length scales. It also presents an approach to fabricate densely packed arrays of nanometer scale devices. The general idea is to use a template to direct the assembly during subsequent deposition. The template is typically fabricated by lithography followed by etching to produce artificially patterned substrates. However this approach is labor intensive, particularly if the detailed structure of individual cells within the pattern is to be controlled.

Alternatively, a hybrid approach, directed self-assembly, can be used. An initial lithographically determined pattern sets conditions for the physical driving forces to control evolution during a subsequent sample growth step. In this process, a template is fabricated to guide the assembly of large numbers of structures quickly. To make this practical, it is crucial to understand the underlying physical mechanisms involved. Researches carried out in this dissertation have been toward gaining such an understanding, by probing QD pattern characteristics during directed self-assembly growth [115-118]. With the knowledge of the underlying mechanism and optimized parameters that control the QD growth, directed self-assembly enables deterministic seeding of sub-10 nm QDs in nanometer precision in electronic devices.

1.4 QD STRUCTURAL CHARACTERIZATION

Electronic and optical properties of QDs can be fine-tuned by QD size, shape and composition. These structural parameters determine electron/hole transport, optical spectral position and purity of photoluminescence. The ability to position QDs sufficiently close is also a necessity to develop interdot coupling energies comparable to $k_B T$. To fabricate high quality QD devices with useful and understandable properties, it is of utmost importance to characterize QD structural and position parameters.

Primary methods for structural characterization can be categorized as follows:

1. direct imaging methods such as scanning tunneling microscopy (STM), atomic force microscopy (AFM) [119] and transmission electron microscopy (TEM) [120-126]

2. diffraction methods such as reflective high-energy electron diffraction (RHEED) [127-129] and its ellipsometric equivalent reflectance anisotropic spectroscopy (RAS) [130-133] and X-ray diffraction [134-138].

STM has the advantage of being able to image directly the morphology of a surface on an atomic level and to manipulate surface atoms. For example, an STM-tip-induced QD in a GaAs surface layer has been created by applying voltage bias between the metallic STM tip and GaAs surface [139]. A hole or an electron accumulation layer can be formed under the tip. AFM has in principle atomic resolution. Typically a lateral resolution of a few nanometers and a much higher z resolution of 0.1 nm can be achieved [140, 141]. As demonstrated in Fig. 1.4, the lateral resolution mainly depends on the size and the shape of the AFM tip.

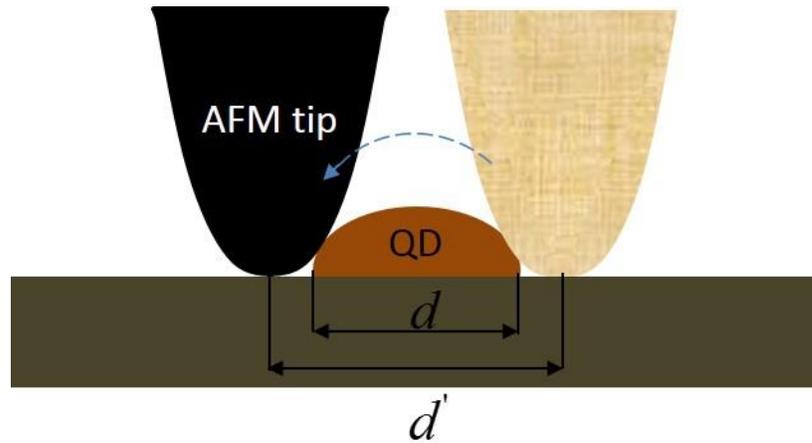


Figure 1.4 AFM characterization of a single QD. The measured diameter d' is larger than actual diameter of the QD d .

STM and AFM measurements of uncovered QDs are challenging to perform in situ or at growth temperatures. However the morphology actually investigated can be different from that after growth, e.g. in this dissertation research, the size and facet angle of Ge/SiC QDs can change

during Si capping layer deposition [116]. This problem can be avoided by using TEM technologies such as high-resolution electron microscopy (HREM) [117] or electron energy loss spectroscopy (EELS) [142], which provide frozen-in morphology information on QDs. The disadvantage is that these techniques are very time consuming can affect the shape of QDs by strain fields [143].

RHEED is a highly surface sensitive technique that can be used to monitor QD growth in MBE systems. RHEED pattern changes from streaky to spotty upon transformation of an initially 2D ordered surface into a QD nanostructure [144]. RAS allows to monitor the asymmetry of the dielectric properties of a sample surface. It has been applied to monitor metal organic chemical vapor deposition (MOCVD) growth of self-assembly QDs by Steimetz, etc. [130] X-ray diffraction techniques are useful for structural investigation after growth. X-ray diffraction characterization of single QD layers [134] and stacks [145] have been reported for InAs/GaAs and Ge/Si QD systems respectively. The diffraction signal due to QDs is weak since the size of QD (10 ~ 100 nm) is much larger than the probing X-ray wavelength (~0.1 nm). Thus, it is important to use high-brightness X-ray sources and implement experimental set-ups to yield a large dynamic range.

A combination of AFM, SEM and TEM characterization techniques has been employed in our research to track the size (volume) and position of precursor SiC nanodots, to monitor Ge/SiC QD growth with different MBE growing conditions. Atomic resolution structural characteristics of Si capped Ge/SiC/Si QDs are also studied by TEM [117].

1.5 CHARACTERIZATION OF QD ELECTRONIC PROPERTIES

1.5.1 Electronic states in QD

The energy of an electron or hole confined in a QD is strongly quantized, i.e., the energy spectrum is discrete. In typical semiconductor QD structures with dimensions in the range of 10 ~ 100 nm, the distance between neighboring energy levels is on the order of a few meV [146]. The quantization of energy is directly reflected in the dependence of the density of the states (DOS) on energy. The DOS for a three-dimensional bulk system has the form

$$\frac{dN}{dE} \propto \frac{d(E^{3/2})}{dE} \propto E^{1/2}. \quad (1.1)$$

For a two-dimensional system such as QW, the DOS is a step function,

$$\frac{dN}{dE} \propto \frac{d(\sum_{\varepsilon_i < E} (E - \varepsilon_i))}{dE} = \sum_{\varepsilon_i < E} 1. \quad (1.2)$$

For a one-dimensional system, e.g. a quantum wire, the DOS has a peculiarity,

$$\frac{dN}{dE} \propto \frac{d(\sum_{\varepsilon_i < E} (E - \varepsilon_i)^{1/2})}{dE} \propto \sum_{\varepsilon_i < E} (E - \varepsilon_i)^{-1/2}. \quad (1.3)$$

For a zero-dimensional system like QD, the DOS has δ -peaks,

$$\frac{dN}{dE} \propto \frac{d(\sum_{\varepsilon_i < E} \Theta(E - \varepsilon_i))}{dE} = \sum_{\varepsilon_i} \delta(E - \varepsilon_i). \quad (1.4)$$

Here ε_i are discrete energy levels, Θ is the Heaviside step function, and δ is the Dirac function.

The quantization of energy is shown in Fig. 1.5 in the dependence of the DOS in systems with different dimensionalities.

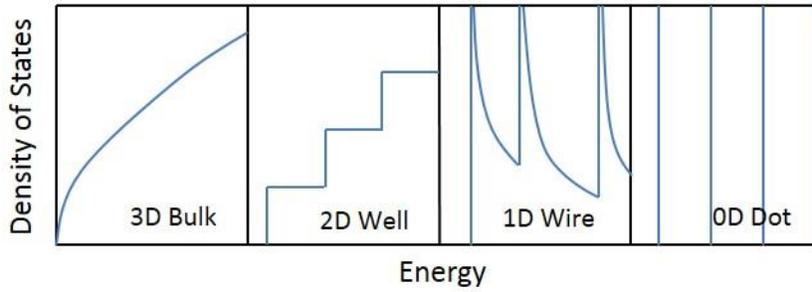


Figure 1.5 Density of States versus energy at different dimensions. From left to right: 3D bulk material, 2D QW, 1D quantum wire and 0D QD.

At cryogenic temperatures (below the Debye temperature) the energy of phonons is too low to excite electrons/holes and the strong quantization of energy determines the electronic properties of semiconductor QDs. Although in any material, electrical and optical properties vary with reduced size, in semiconductors, this size-related transition occurs for a given temperature at a relatively large size compared to metals and insulators. In metals, the relevant energy spacing is small because the Fermi level lies in the center of conduction band (CB). Therefore at the temperature above a few kelvin, the electrical and optical properties resemble those of a continuum, even at small size as tens or hundreds of atoms [147]. In semiconductors, however, Fermi level lies between CB and valance band (VB), such that the edges of the bands dominate the low-energy electrical and optical behavior. Therefore, the electrical transport for semiconductor QDs depends strongly on size, mainly because of the large variation in energy required to add or remove charges on a QD.

QDs are mainly created by producing a lateral confinement restricting the motion of the charge carriers, which are initially confined in a very narrow QW by the potential $V_{QW}(z)$. Thus the QDs have the shape of flat disks, with transverse dimensions considerably larger than their

thickness, and the confined charge carriers can be considered as two-dimensional. Depending on QD fabrication methods, the lateral potential can be approximated by various potential models. A parabolic profile of the confining potential

$$V(r) = V_0 + kr^2, \quad (1.5)$$

has been applied in numeric simulation of electron-states in a GaAs QD by Kumar etc. [148] Their calculation shows that the separation between energy levels is almost independent of the number of electrons confined in QDs, and the evolution of energy levels in magnetic field is similar to that of levels of a parabolic well. These results have been observed in several experiments [148-150]. Therefore, the application of such an approximation in model calculation has been justified.

The symmetry of a 2D, disk-shaped QD leads to a shell structure [1]. In atoms, a 3D spherically symmetric potential yields degeneracies known as shells, 1s, 2s, 2p, 3s, 3p, etc. Each shell can hold a specific number of electrons. The electronic configuration is particularly stable when these shells are completely filled with electrons, occurring at 'magic' atomic numbers 2, 10, 18, 36.... In QDs, a lower degree of symmetry in 2D results in a shell structure with different sequence of magic numbers, 2, 6, 12, 20,...[1]. By measuring electron transport through QDs, a periodic table of artificial 2D elements can be obtained [151].

The borderline between the physics of bulk condensed matter and few-body quantum systems is crossed with the quantized electron transport. Experimentally, a quantum regime can be achieved by studying electronic transport and photoluminescence (PL) spectra of QD devices. The transport between QD and carrier reservoirs occurs via tunneling barriers [16, 152-156]. If the tunneling barriers are thick enough, the transport is dominated by resonant tunneling. If the QD is fully decoupled from its environment, it confines a well-defined number N of electrons.

For weak coupling, the total electrostatic energy of the QD can be estimated by $N(N-1)e^2/(2C)$ [157], where C is the capacitance of the QD. Thus adding a single electron requires energy Ne^2/C , which is discretely spaced by the charging energy e^2/C . If this charging energy exceeds the thermal energy $k_B T$, electrons cannot tunnel on and off the QD by thermal excitations alone, and transport is blocked. This phenomena is usually referred to as Coulomb blockade. Coulomb blockade and Coulomb ‘staircase’ are first observed by Kuzmin [158, 159] and by Fulton [160] for granular systems and thin-film tunnel junctions, respectively. Both of their work show a transport signature as equidistantly spaced clear peaks, separated by regions of zero conductance as schematically shown in Fig. 1.6. Coulomb blockade has been intensively investigated both theoretically [161] and experimentally in various QD systems [161-169]. Most of these experiments focused on single or double electrostatically defined lateral QDs within in a 2DEG in a GaAs/AlGaAs [162] or Si/Si-Ge [167, 168] heterostructure. The results of Coulomb blockade spectroscopy enables us to construct the addition spectrum of these lateral QD device. On the contrary, there are not as many Coulomb blockade investigations in self-assembly QD system because of the difficulties in isolating individual self-assembly QDs and integrating them into single- or few-QD electronic devices.

The rest of this section describes commonly used electrical and photoluminescence (PL) methods for electronic structure investigation in QD systems. In the end, the localization of the charge carriers confined by QDs are briefly discussed.

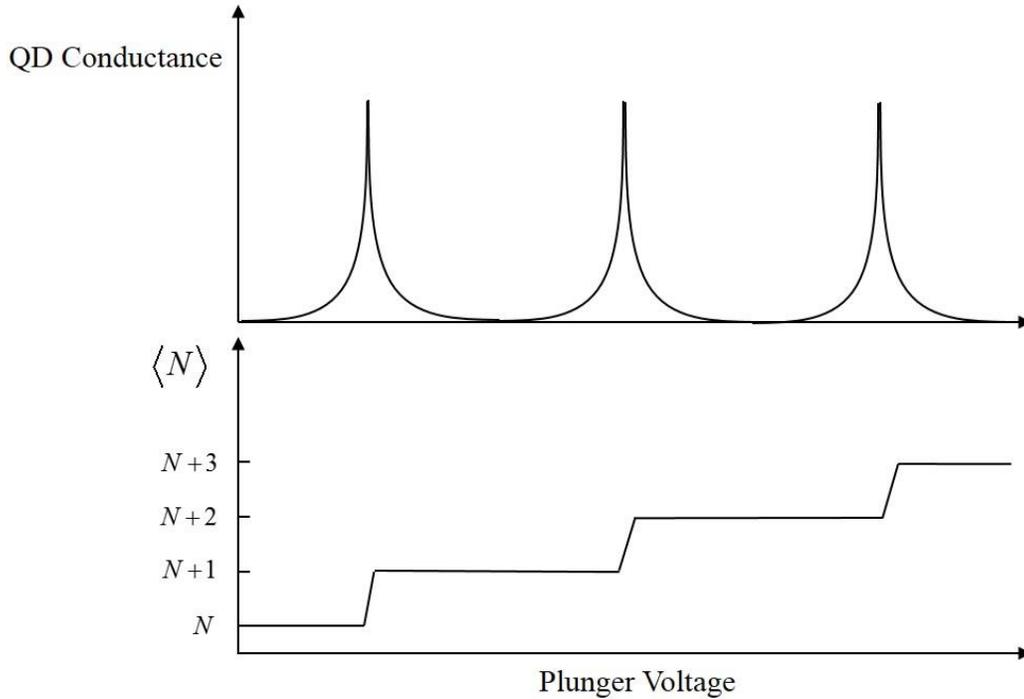


Figure 1.6 Coulomb blockade oscillation. The upper is the QD conductance spectra as a function of the QD plunger gate voltage. The lower one is the corresponding electron occupancy number in the QD. The QD conductance spectra shows features as equidistantly spaced clear peaks, separated by regions of zero conductance. The electron occupancy number increases by one at each conductance peaks.

1.5.2 Electrical characterization methods

Electrical characterization methods are introduced as following:

- CV Spectroscopy

Charging QDs with electrons or holes can be probed with capacitance voltage (CV) spectroscopy. By tuning Fermi level E_F through the states of a QD via a bias voltage, the differential capacitance of the QD can be probed with an additional small alternating (ac) signal.

Assuming that a QD is charged with one electron in the s -like ground state, a second electron (with opposite spin) can fill the ground state and experiences an additional charging energy $E_{21} = E_2 - E_1$ of the order e^2/C . Therefore the Fermi level has to increase in order to fill another electron into the QD. This is the Coulomb blockade phenomenon, as introduced earlier in this section. Coulomb blockade is normally observed at temperatures for which $E_{21} \gg k_B T$. Subsequent bound-state electrons must occupy excited states, due to the Pauli exclusion principle. The energy difference $E_{32} = E_3 - E_2$ consists of the energy difference between the single-particle ground and excited states, plus the addition energy. Magnetic fields further lead to a splitting of the p -like excited state. A clear separation of lowest two peaks has been reported for CV characteristics due to magnetic field induced splitting in Fricke's work [170].

A model taking inter- and intra-QD Coulomb interactions into account using a Monte Carlo simulation of CV experiments has been studied for single-electron charging in InAs self-assembled QDs [62]. The Coulomb interaction provides two capacitance peaks which correspond to sequential loading of two electrons into a single QD. The distance between the peaks and the width of the peaks contain information about interactions inside one dot and between the dots. The inter-QD interaction is important for the quantitative interpretation of the experimental data in Ref. [62]. This inter-QD Coulomb interaction model also provides a clue to explain the magnetotransport data in our research.

- Vertical Tunneling

When a QD is sandwiched between two barriers, electrons can tunnel through the QD only at a bias voltage for which an occupied emitter state is resonant with a QD energy level. This

phenomena is referred to as resonant tunneling. Resonant tunneling devices containing GaAs QDs have been investigated by Reed, etc. [152, 171]

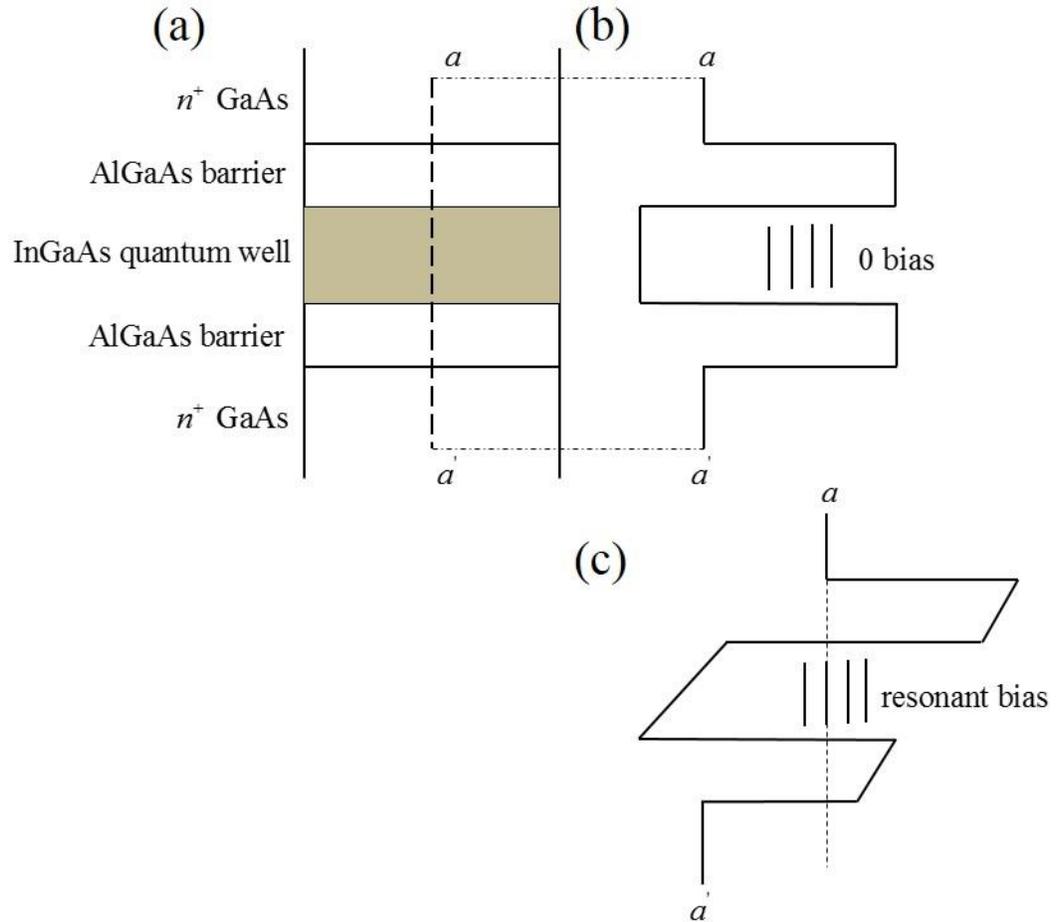


Figure 1.7 Vertical (a-a') potentials of a column QD under zero and resonant bias. (a) A column containing InGaAs QD. (b) The potential of the QD under zero bias along (a-a') axis. (c) The potential of the QD under resonant bias along the same axis as in (b).

The band line-up of the GaAs QDs studied in Ref. [171] is schematically drawn in Fig. 1.7. In samples containing QD within tunneling barriers, electron transport features due to tunneling through QD states have been observed. In forward bias, when electrons flow from the substrate of the device to the top contact, a number of current peaks appear in current-voltage (IV) curve.

These peaks represent sharp increase of conductivity induced by the resonant tunneling transport through the QD. At around 50 K, the resonant tunneling features are almost completely smeared out due to the increased thermal energy.

Vertical resonant tunneling IV characteristic measurement has been employed to investigate electron or hole states for various QD systems [152-156, 172-174]. For example, Yakimov, etc. reported conductance oscillations as a function of bias voltage of isolated epitaxial Ge/Si QDs. The conductance was associated with hole tunneling into the QDs and the oscillations were attributed to the interplay of single-electron charging effects and resonant tunneling through individual energy levels [175]. Resonant tunneling at 300 K with a peak current to valley ratio as high as 10 has been measured for a single self-assembled Si/SiO₂ QD [154]. Resonant tunneling is also characterization exploited to explore the electronic properties of our directed self-assembled Ge/SiC/Si QDs.

- Lateral Transport

The presence of QDs in a layer or channel largely modifies its transport characteristics. For example, a sheet of InAs QDs close to (384 nm) a 2DEG at an AlGaAs/GaAs heterointerface can decrease the mobility of electrons in the channel drastically [176]. The decrease of mobility is attributed to the scattering potential introduced by the QDs.

The lateral transport enables the investigation of not only electronic states of single QDs but also the inter-QD interactions. The lateral transport through a double QD (DQD) has been investigated by Fujisawa, etc. [177]. The number of QDs contributing to the transport has been defined by lithographically patterned split gate structures with depletion zone such that only one or a few QDs is located in the transport channel. The QDs in the DQD are coupling to each other

through an electrostatically tunable tunnel barrier. The lateral transport current spectrum has been associated with the gate voltages defining the DQD and the tunneling barriers between the QDs.

The lateral transport dc current through QD usually consists of elastic resonant tunneling current peaks and inelastic current at the off-resonant conditions. The inelastic current is attributed to electron-phonon coupling. In this process, the electron can tunnel from a higher-energy state in one QD to a lower-energy state in other QDs or to electron reservoir by spontaneously emitting an acoustic phonon [177, 178].

1.5.3 Photoluminescence measurements

Another basic experiment technique for investigating discrete energy levels of QDs is photoluminescence (PL) measurements as schematically presented in Fig. 1.8. An incident laser beam γ_{in} excites the electrons from the VB to the CB and creates electron-hole pairs. These pairs can be excited directly into the discrete levels in the QD, above the discrete level, or to the bulk semiconductor continuum with higher excitation energy. Part of the generated excitons relax nonradiatively to the ground state (Fig 1.6, left) or to weakly excited states in QDs. The electron-hole pairs confined in the QDs recombine, accompanied by emitting photons, which are registered ($e + h \rightarrow \gamma_{out}$).

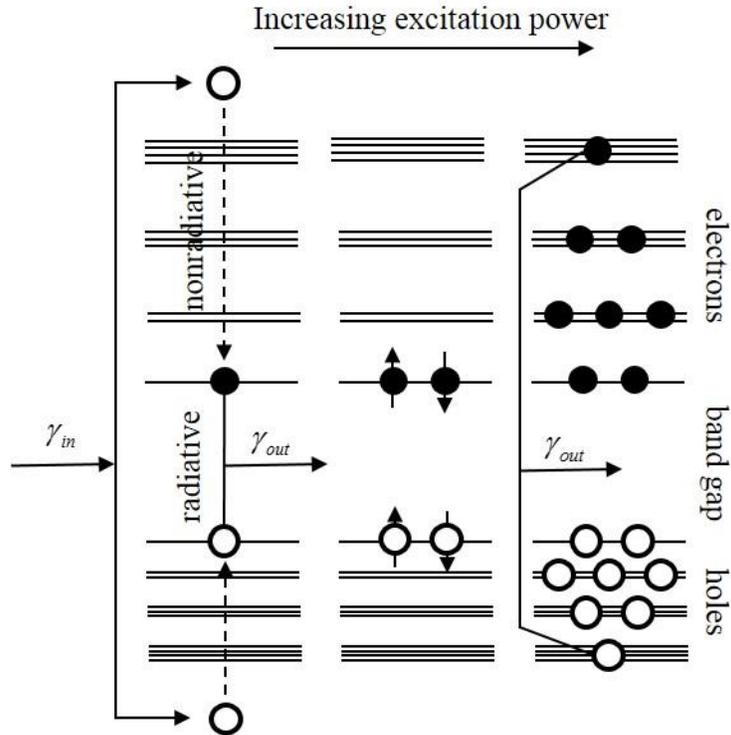


Figure 1.8 The photoluminescence experiment: measurement of the intensity of outgoing beam γ_{out} as a function of its wavelength at the constant wavelength of the incoming beam γ_{in} (PL spectrum), or on the wavelength γ_{in} at the constant wavelength γ_{out} (PLE spectrum) (Figure adapted from [179]).

There are two main types of PL experiments implemented for measuring the spectrum of light emission and absorption by the QD system, respectively.

In the first case (PL), the wavelength of the incident light is small, creating electron-hole pairs high above the discrete energy levels of the QDs. The measured dependence of the radiation intensity on the outgoing beam energy, provides information on the energy levels of the QDs.

In the second case (photoluminescence excitation, PLE), the energy of the incoming photon is varied as shown in Fig 1.6. Only those outgoing photons that have their energy equal to a fix constant are registered. The measured spectrum in this case is the dependence of the emitted

radiation intensity on the incoming photon energies. The spectrum is related to the number of electron-hole pairs excited at a given incoming photon energy. On the other hand, the probability of creating an electron-hole pair by absorbing an incident photon is proportional to a joint density of states of the electron-hole pair. Therefore, in the case of a QD, a peak in the PLE spectrum corresponds to a discrete energy level of the QD.

The spectral lines emitted by a single QD are very narrow because of QD's δ -function DOS. The size dependence of shift and splitting of the energy states can be directly visualized by the optical spectral. Carrier dynamics, i.e. capture, relaxation and recombination, can also be experimentally accessed using time-resolved spectroscopy. Therefore local luminescence probe techniques are particularly useful for the investigation of single QDs. [180, 181]. On the other hand, due to the small intensity of radiation that is emitted by a single QD, the measurements are usually taken from a large system of QDs. The inhomogeneity of the individual QD sizes leads to an additional broadening of peaks.

PL measurements have been widely used to characterize various QD systems as referenced in [180-190]. One example is the PL measurement of a single quantum dot molecule (QDM) in the presence of a electric field. The coupling between excited states of two QDs can be tuned by the field, leading to charge transfer from one dot to the other, which can be characterized in the measured PL spectrum [184]. Another example is the PL measurement on a vertically stacked multilayer InAs/GaAs QD structure. The PL study of this structure shows that an increase of the thickness of the spacing layers between adjacent QD layers leads to a decrease of the lateral dimensions of QDs, accompanied by an increase of the energy separation between the ground and first excited states.

1.5.4 Carrier Localization

Considering carrier location, there are two types of band-edge alignment, type I and type II, with semiconductor quantum dots. In type-I QDs, the band gap of the narrow-gap material lies entirely within the gap of the wide gap semiconductor, and both electrons and holes are confined inside the same region. A typical example of the type-I band-edge lineup is InAs QDs in a GaAs matrix as shown in Fig. 1.9(a).

For type-II QDs, the localization inside the dot occurs only for one of the charge carriers, electron (e) or hole (h), whereas the dot forms a potential barrier for the other particle. Take Ge/Si(001) QDs formed by strain epitaxy as an example, holes are strongly confined in the Ge region, and the electrons are free in the Si conduction band as shown in Fig. 1.9(b). The tensile strain in the Si in the vicinity of the Ge QD reduces the band gap compared to that for bulk Si. Therefore the lowest conduction band edge just above and below the Ge island is formed by Δ_2 valleys, yielding triangle potential well around 0.16 eV, for electrons in Si near the Si/Ge boundary. Thus three-dimensional localization of electrons can be expected in the strained silicon near the Ge dots (Fig. 1.9(c) and (d)) [51, 77, 78, 191, 192]. Type-II QDs such as GaSb/GaAs [89, 90] and Ge/Si systems [77] attract intensive research interest because the effective exchange interaction between spins can be greatly increased due to the weak confinement [51].

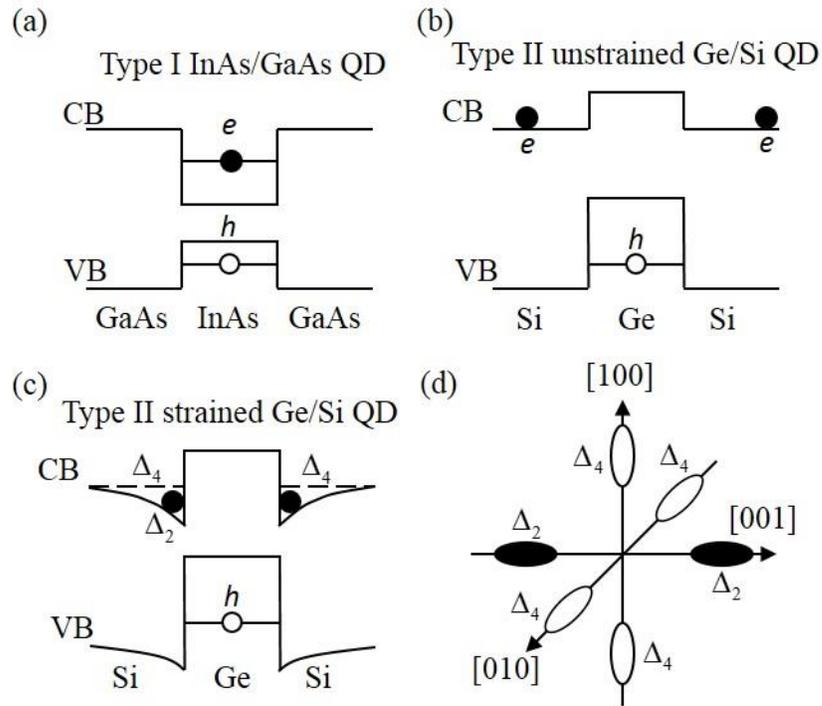


Figure 1.9 Band alignment in type-I and type-II QDs. (a) Schematic overview of the band alignment in type-I InAs/GaAs QD and (b) type-II Ge/Si QD. (c) Band structure in Ge/Si(001) QD's modified by tensile strain. The conduction band (CB) in Si just above and below the Ge dot splits into Δ_4 and Δ_2 valleys. (d) Fermi surface in the Si conduction band. (Adapted from Ref. [77].)

2 DIRECTED SELF-ASSEMBLED GE/SiC/SI QUANTUM DOT

2.1 INTRODUCTION

The directed self-assembly Ge/SiC/Si QDs are fabricated with templated growth technique. Templated growth technique offers a substantial control over the QD size (volume), size distribution and QD location with sub-10 nanometer accuracy [115]. The Ge/SiC/Si QDs are silicon based semiconductor system, so it is promising to be integrated with current semiconductor technologies. EBL patterning and MBE growth are two key techniques employed in the fabrication process: EBL is capable of patterning configuration of nanostructures at nanometer precision and the MBE growth creates sub-10 nm scale dislocation-free Ge/SiC/Si QDs. Two important configuration parameters related to the directed self-assembly QDs and device characterization are the dot size (diameter) ϕ and interdot spacing d .

Random arrangements of Ge islands with $\phi \sim 20\text{--}100$ nm and separations $d \sim 50$ nm have been achieved on Si(100) via the Stranski–Krastanov instability [67, 193], by which Ge islands form over a two-dimensional wetting layer that exceeds a critical thickness. Extremely small carbon-induced Ge (CGe) QDs can be formed by epitaxial growth of a submonolayer amount of C (~ 0.1 ML), followed by 2~4 MLs Ge [194, 195]. The Ge islands are also randomly distributed at the carbon precursor center, with a high density ($\sim 10^{11}/\text{cm}^2$) and relatively narrow size distribution. To control the placement of individual islands, several groups have developed template growth techniques using lithographic patterning methods. One such example is formation of Ge QDs in SiO₂/Si(001) windows prepared either by partial thermal desorption of an ultra-thin oxide layer or by standard electron beam lithography with wet chemical etching [84, 196]. G. Jin, etc., controlled the arrangement of the self-organized Ge dots on the pre-grown Si

mesas by selective epitaxial growth: well-ordered one dimensional Ge dot arrays were formed on the $\langle 110 \rangle$ -oriented ridges of the Si stripe mesas [197]. The formation of these dot arrays was attributed to the balance between the strain energy of the dots and the repulsive interactions of the neighboring dots through the substrate. A brief review of other template growth techniques can be found in Section 1.2.

Due to resolution limitation from the lithography techniques, the smallest island size that has been achieved by these methods is around 40 nm, and the smallest separation observed is about 80 nm [196, 198]. However quantum computation and quantum simulation requires a fine control over QD size and spatial arrangement on the sub-35 nm length scale [51]. To achieve this goal, templated growth technique has been developed in our laboratory, taking advantages of the patterning flexibility by electron beam lithography and the sub-10 nm quantum dot growth ability by molecular beam epitaxy (MBE).

The fabrication process and growth condition optimization are described in section 2.2. In section 2.3, the atomic structure of carbon dot precursor and Ge/SiC QD is characterized by AFM, SEM and TEM. The electronic structure of the Si capped Ge/SiC QD (Ge/SiC/Si QD) are discussed in section 2.4.

2.2 TEMPLATED GROWTH TECHNIQUE AND GROWTH CONDITION OPTIMIZATION

The directed self-assembled Ge/SiC/Si QDs in our research are fabricated by the templated Ge growth technique, first developed by O. Guise, etc., in 2005 [115]. In this process, carbonaceous precursor templated are created on Si substrates by electron-beam induced deposition (EBID) using high resolution electron beam lithography (EBL). Then the template is etched by ozone, followed by annealing in ultra-high vacuum, yielding small (~ 4 nm) SiC nucleation sites for subsequent deposition of Ge. The Ge is deposited by molecular beam epitaxy (MBE) in S-K mode to produce strain relaxed self-assembly Ge quantum dots on the substrate. The Ge accumulates at the SiC nucleation sites due to the localized strain. AFM images Ge islands with mean diameter $d \approx 8$ nm and 2 nm absolute position precision. However the fluctuations of the Ge island volumes are large as the result of competition for Ge by nearest neighbors, i.e., Ostwald ripening (see section 1.3). To become useful for fabricating quantum devices, it will be important to gain an ultimate level of control with Ge nanostructures, which requires understanding how the kinetic history of the Ge/SiC can be tailored to reduce island size fluctuations, and how their structure relates to electronic and optical properties.

The fabrication process used in this research has been modified by capping Ge/SiC QDs with 50 nm intrinsic silicon so that electrons can be confined in the silicon in the vicinity of the apex and the base of the QDs.

The fabrication process scheme in Fig. 2.1 shows growth process for two-dimensional Ge/SiC QD arrays with 50 nm Si capping layer. After each step, AFM images the topography of the resulting nanostructures, as shown underneath each schematic image in Fig. 2.1. Quantitative analysis of the resulting topography of 2D QD arrays after each step provides QD structural

characteristics such as QD volume, volume distribution and QD positioning accuracy. These characteristics, in turn, are good indications for adjusting process parameters of each step to optimized working ranges.

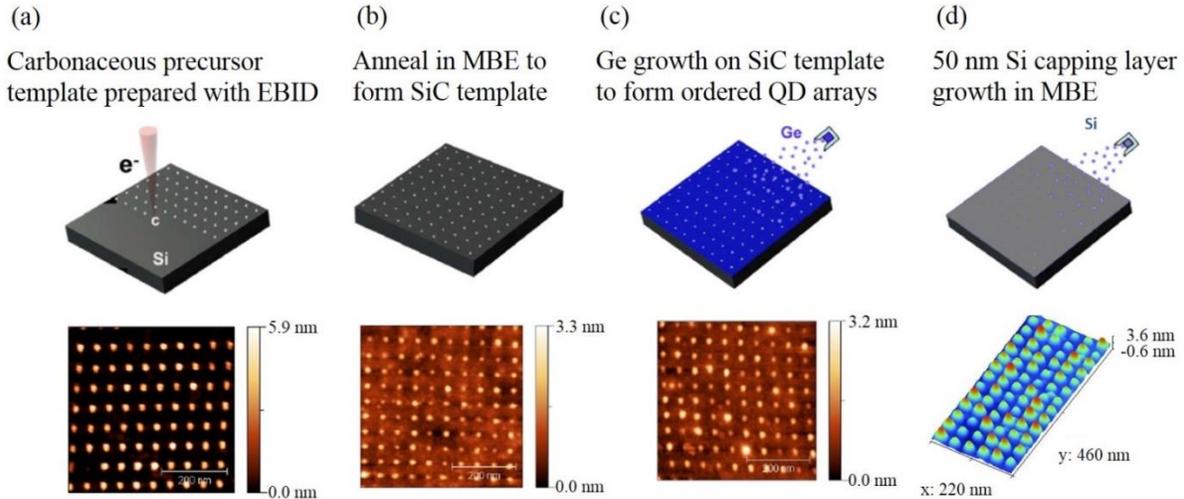


Figure 2.1 Templatd growth of Ge/SiC/Si QD arrays. The top images are processing schemes and the bottom images are AFM topography after each step. (a) Prepare carbonaceous precursor template with EBID. (b) Anneal in MBE to form SiC template. (c) Deposit Ge on SiC template to form QD arrays in MBE. (d) Cap the QD arrays with 50 nm Si layer in MBE.

The details of the processing including growth parameters optimization are described in the following sections.

2.2.1 Precursor template preparation

Precursor template substrates have been prepared with silicon wafers with a miscut of 0.1° cleaned via a modified IMEC/Shiraki process. The cleaning procedure starts with removing native oxides followed by passivation. SiO_2 layer is stripped in a 2% dilute hydrofluoric acid (HF) solution immediately, leaving a hydrogen-atom-terminated flat surface immune to re-oxidation for several hours before the wafer is loaded into the Raith e-LiNE EBL system ($P_{\text{base}} \sim 10^{-7} \text{T}$). The electron beam (ebeam) column is operated with an accelerating voltage of 20 keV and an emission current of ~ 21 pA for precursor deposition. Focused electron beam irradiation of ambient hydrocarbon adsorbates on the Si(001) surface yields nanoscale islands of carbonaceous material, presumably amorphous hydrogenated carbon. These carbonaceous nanostructures are referred to as aC:H from literature [115, 199]. Square arrays of $N \times N$ aC:H nanodots are patterned, with interdot spacing of 100, 50, and 35 nm in this research.

The size of aC:H nanodots positively correlates with the size of final Ge/SiC/Si QDs. Hence it is of utmost importance to investigate the dependence of the size and size distribution of these nanodots on different interdot spacings and various EBL deposition conditions. The full width at half maximum (FWHM) of the diameter of aC:H nanodots as a function of electron charge deposited at single nanodot sites, defined as ebeam dose (a_e), has been studied as shown in Fig. 2.2. The power law fitting of the experiment data provides a power of 0.3. The volume of the deposited aC:H, $V_{\text{aC:H}}$, is assumed to be proportional to the ebeam dose a_e by:

$$V_{\text{aC:H}} \propto a_e. \quad (2.1)$$

Therefore the dependence of the FWHM with the ebeam dose by the power of 0.3 falls around the expectation of 0.33. The deviation may come from z direction deposition anisotropy.

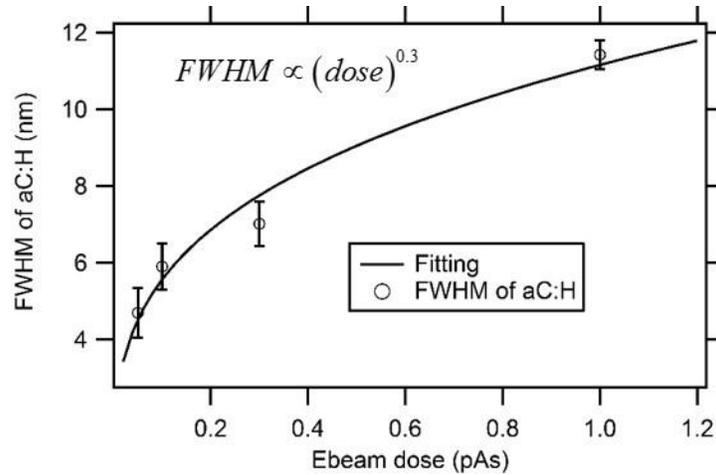


Figure 2.2 FWHM of aC:H nanodots versus ebeam dose. The power law fitting provides a power of 0.3.

Ebeam dose is controlled in EBL by ebeam current and exposure time. An exposure dwell time in the range of 45-50 ms has been used in this research to obtain smallest possible QDs. With ebeam emission current around 21 pA, the ebeam dose on a single nanodot is estimated around 1 pA · s, corresponding to ~10 nm FWHM of aC:H nanodots.

Next, templated aC:H nanodots are exposed to UV-ozone to eliminate excess hydrocarbon contamination between the patterned sites. However this exposure also etches the patterned nanodots. Hence UV-ozone exposure time needs to be critically controlled to prevent the complete removal of nanodots.

The precursor template wafer then is loaded into an ultra-high vacuum (UHV) chamber ($P_{\text{base}} = 1 \times 10^{-10}$ Torr) of molecular beam epitaxy (MBE) and is radiatively heated during 9 hour temperature ramp to 500°C. The wafer dwells at 500°C for at least an hour prior to oxide desorption at 780°C to provide further outgassing. aC:H nanodots are fully converted to SiC during oxide desorption at 780°C [117]. Figure 2.3 shows a square array of SiC nanodots with 35 nm pitch, as well as an arbitrary SiC pattern with minimum spacing of 28 nm.

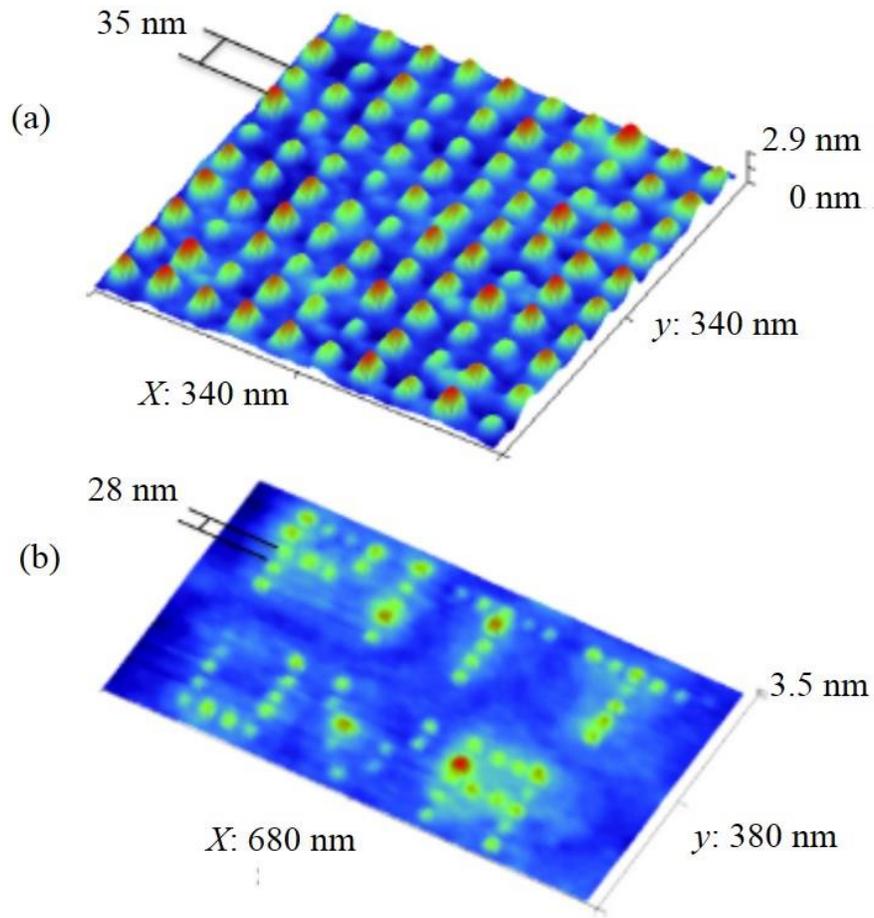


Figure 2.3 AFM image of EBID aC:H nanodots. (a) Square array of SiC nanodots with 35 nm pitch. (b) Arbitrary SiC pattern with minimum spacing of 28 nm.

During the heating of an aC:H template in UHV, the 500°C dwell strongly affects final feature size. AFM topography of the features (either aC:H or converted SiC) is taken for quantitative analysis with Ge either deposited and then selectively removed, or not deposited at all. Figure 2.4(a) shows that the overall heating and conversion to SiC results in up to 86% reduction in feature volume from the original aC:H nanodots. As shown in Fig. 2.4, the longer dwells lead to reduced feature size (Fig. 2.4(a)) and a much broader size distribution (Fig. 2.4(b,c)). The loss of the volume is attributed to the evaporation of residual hydrogen from the

aC:H nanodots at 500°C, leaving behind carbon. The complete dehydrogenation of aC:H has been reported between 450-550°C in Ref. [200]. The broadening of the size distribution either implies the evaporative loss process is locally non-uniform, or that coarsening is occurring simultaneously with evaporation, likely mediated by a non-volatile surface diffusing species, e.g. carbon atoms. The evolution of the size distribution from Gaussian as-EBID to log-normal after processing is consistent with Ostwald ripening [201].

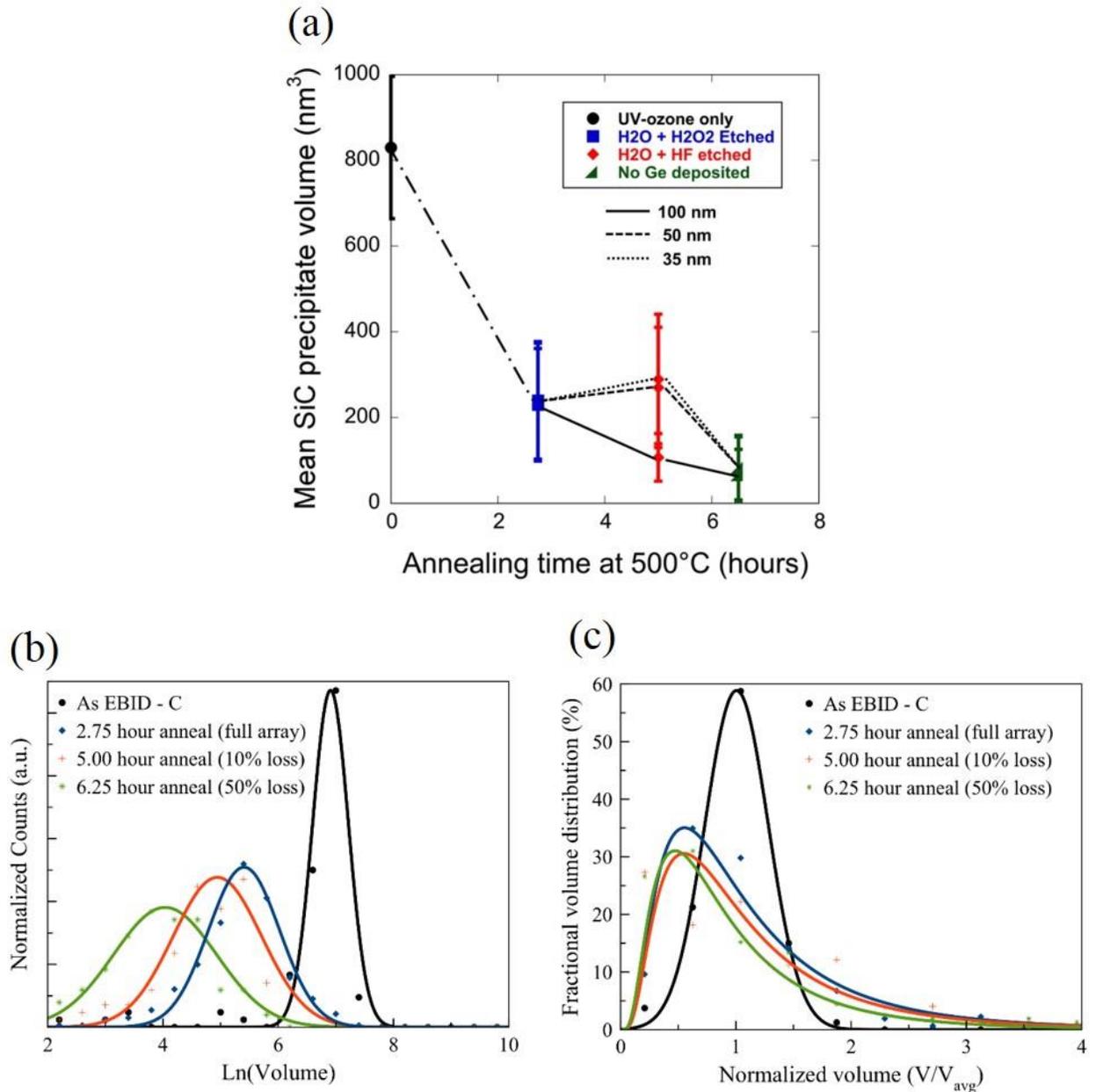


Figure 2.4 Final feature size affected by 500°C dwell. (a) Average SiC nanodot volume vs. dwell times at 500°C. In all cases, Ge has either been deposited and then selectively removed, or not deposited at all. 35nm, 50nm, and 100nm template spacings are delineated by connecting lines. (b) Corresponding distributions of nanodot volumes for the 100 nm pattern spacing for each 500°C dwell time, where $\text{Ln}(\text{Volume})$ is used to more clearly show the evolution of the mean size. (c) The distributions are plotted on a linear volume scale normalized to the mean volume of each distribution.

2.2.2 Ge MBE growth

Upon cooling to the growth temperature, a 1.3 ML of Ge is deposited via magnetron sputtering in 3 mTorr of getter-purified Ar at a rate of 0.1 Å/s, with a subsequent annealing at 700°C. Ge deposited in different growth conditions are characterized to compare the deposition temperature effects on thermal stabilities of overall structures. Figure 2.5 shows the AFM images of a small portion of Ge/SiC arrays after Ge growth at 600°C (Fig. 2.5 (a-c)), and after Ge growth at 400°C followed by a 700°C anneal (Fig. 2.5 (d-f)).

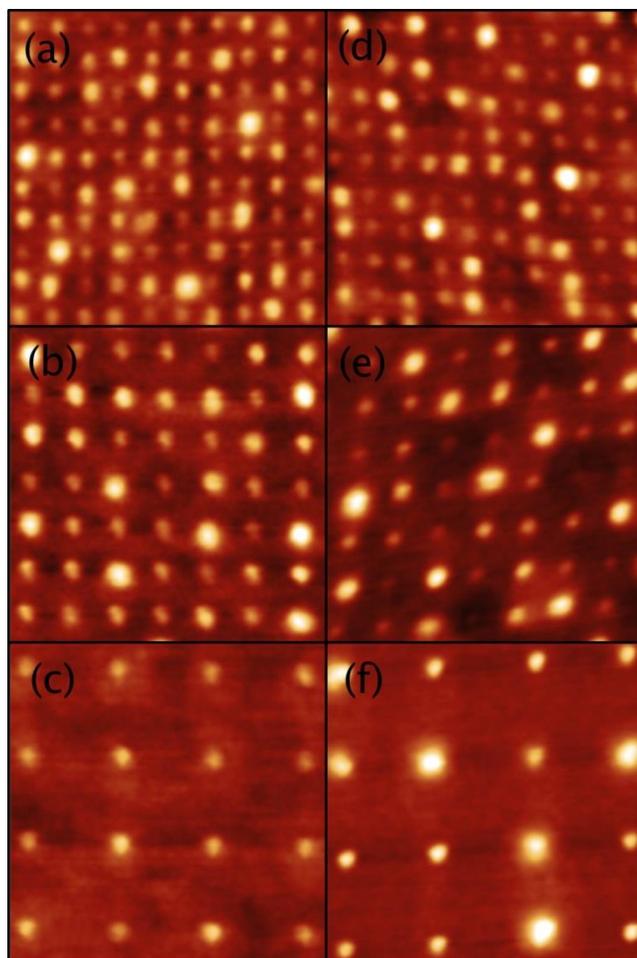


Figure 2.5 AFM of Ge/SiC QDs grown at different Ge deposition temperatures. 35nm, 50nm, and 100nm feature arrays after (a-c) 600°C and (d-f) 400°C followed by 700°C Ge depositions. Each tile is a 350nm x 350nm section from larger arrays. (Note: Small deviations in orthogonality are due to drift during AFM scanning.)

In depositions without post-annealing, the presence of Ge had no effect on the size and distribution of the templated arrays. Ge completely avoids SiC sites during elevated temperature growth ($T \sim 600^\circ\text{C}$) due to the unfavorable Ge-C bond. Hence, Ge strongly prefers to attach to the lower energy surface bonding sites on the nearby Si substrate [117]. Alternatively, the effects of post-deposition annealing on the size uniformity are also shown in Fig. 2.6. Growth of 1.3 ML of Ge at 600°C results in a volume distribution that is nearly identical to that of the underlying SiC

template (obtained by selective etching). This observation holds for all three interdot spacings. On the other hand, growth of Ge at 400°C, followed by a 700°C, 30 min anneal, clearly leads to coarsening. The total volume of the distribution is larger than that of the distribution for conformal Ge on the SiC template, implying additional mass was accumulated. Furthermore, the degree of coarsening increases with the interdot spacing. At 100 nm, a clearly bimodal distribution is produced. The bimodality is less pronounced at 50 nm spacing, and only a shoulder is observed at 35 nm.

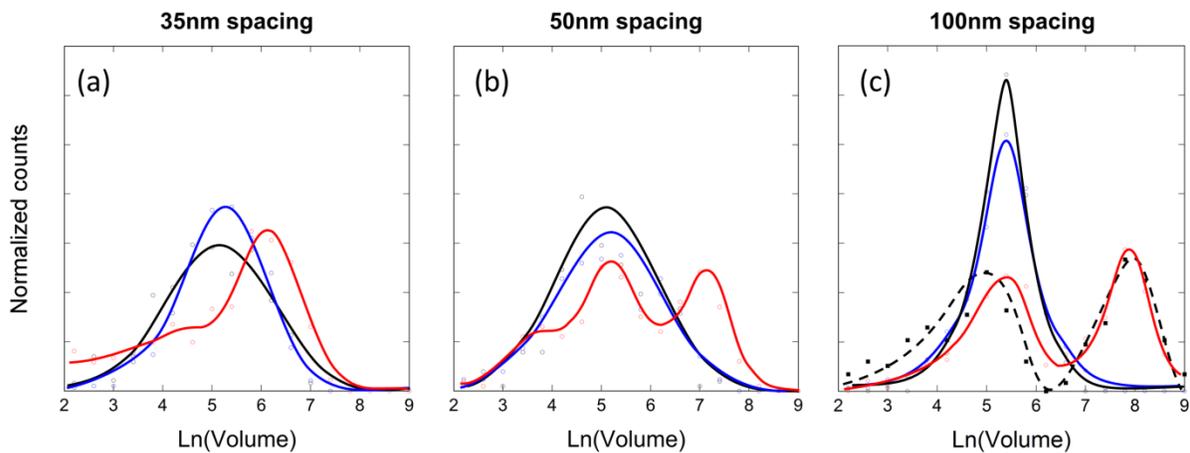


Figure 2.6 Volume distributions of Ge/SiC composite nanodots (2.75 hr dwell at 500°C) for two different growth strategies: (blue) Ge deposited at 600°C and (red) Ge deposited at 400°C then annealed at 700°C. (a) 35nm spacing, (b) 50nm spacing, and (c) 100nm spacing. For comparison, the bare SiC arrays after selective Ge etching are also shown (black). In the case of 100nm spacing, the annealed specimen was also etched (dashed-black).

To further investigate the degree of coarsening, the volume of each island relative to the average volume of its nearest neighbors is plotted in Fig. 2.7. In general, larger islands tend to have smaller neighbors, consistent with the mechanism of Ostwald ripening [201].

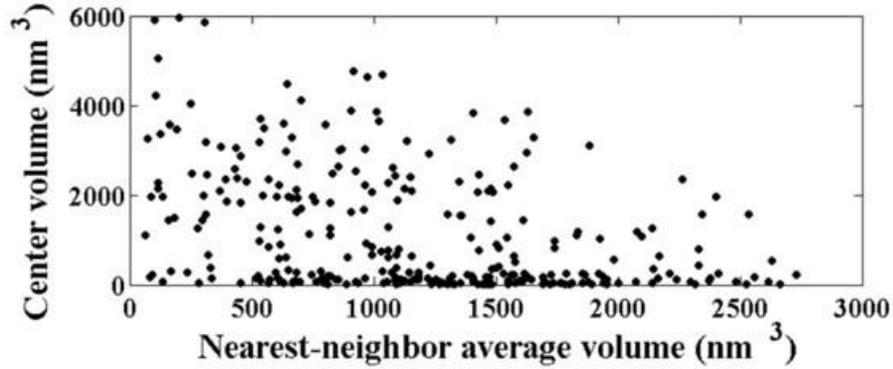


Figure 2.7 Degree of coarsening for Ge/SiC nanodots. A scatter plot showing the average nearest-neighbor volume surrounding each Ge/SiC island.

Figure 2.8(a) shows a 35nm array with Ge deposition at 600°C along with a fast Fourier transform (FFT) of the full array. By extracting the FWHM of the first order $\langle 01 \rangle$ peak, the average spatial variation is determined to be ± 1.6 nm. This positional accuracy of these QDs is adequate for device needs. From a cumulative probability plot of QD diameters for the same 35nm array in Fig. 2.8(b), 51% of islands have FWHM ≤ 10 nm and 95% are ≤ 15 nm.

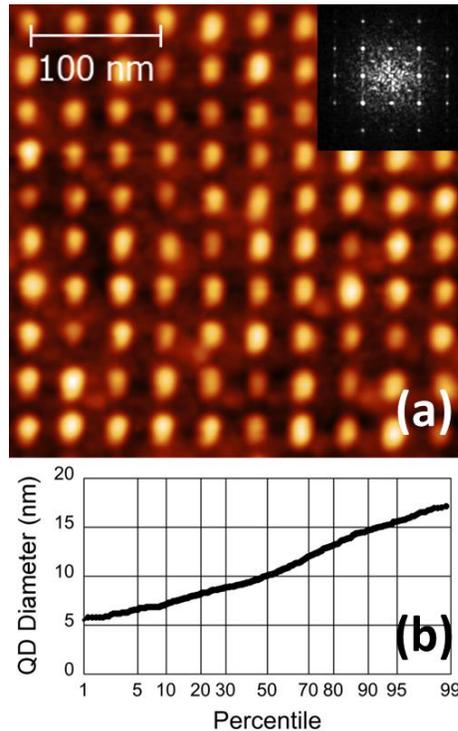


Figure 2.8 Statistical analysis of Ge/SiC size. (a) AFM image of a 10x10 array section of composite Ge/SiC QDs with 35nm spacing. The inset displays a FFT of the full array; the FWHM of the <10> peak determines a positional error of ± 1.6 nm. (b) Cumulative probability plot of the QD diameters for the same 35nm spacing array. 51% of islands have $\varnothing \leq 10$ nm, while 95% have $\varnothing \leq 15$ nm.

In the end of the process, Ge/SiC nanodots are encapsulated with 50 nm Si grown at 250-300°C. The low capping temperature was chosen to ensure conformal Si growth, maintaining single crystalline epitaxy [116].

2.2.3 Structure characterization by TEM

Transmission electron microscopy (TEM) is performed at 300 kV, examining in the <110> zone axis [117]. Figure 2.9(a) shows high resolution, cross-section TEM (HR-XTEM) micrographs of two Si capped Ge/SiC/Si(001) QDs. These QDs are prepared by the above-described process with deposition of 1-3 ML Ge at 600°C without subsequent annealing. The nanodots in Fig. 2.9 have basal diameters of 7 nm and 15 nm, respectively, and heights of 1.5–2 nm. It is observed from Fig. 2.9 that these SiC nanodots are completely surrounded by Si in the cross-section. In Fig. 2.9 (c), ‘V’ shaped dislocation features are clearly observed. The dislocation is caused by the strain from the SiC and Si lattice mismatch.

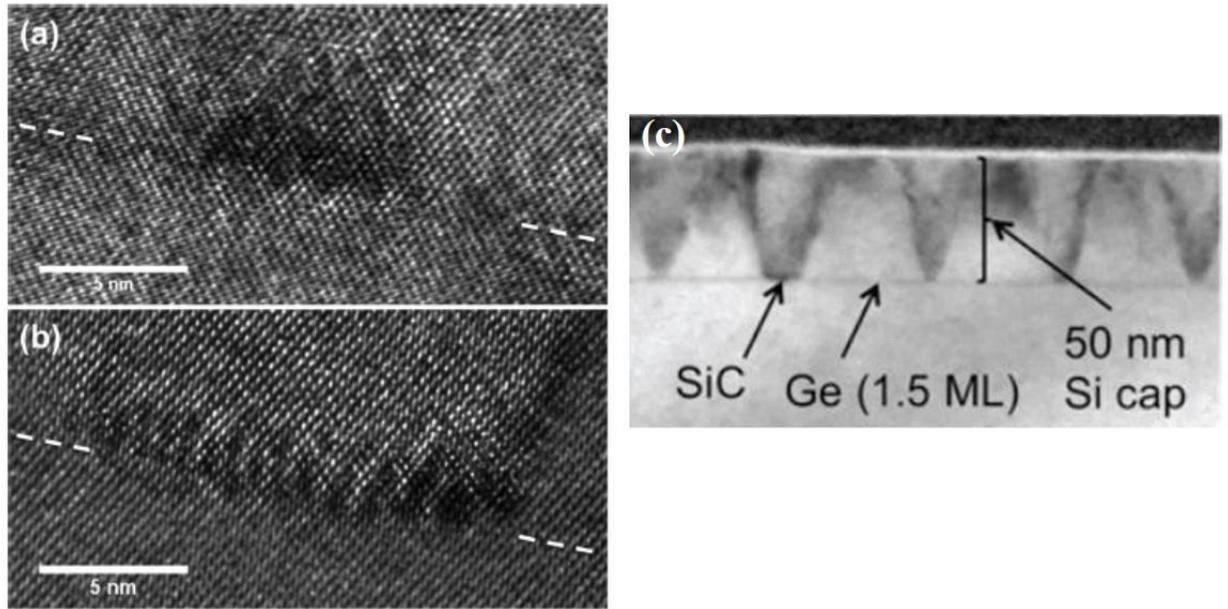


Figure 2.9 XTEM image of Ge/SiC/Si QDs. (a) and (b) Cross-sectional TEM (XTEM) of two carbide nanodots, along a $\langle 110 \rangle$ zone axis. The original Si substrate surface is delineated with dashed. (c) XTEM of one array of Ge/SiC QDs embedded in Si. Strain induced dislocations are visible in the Si capping layer.

Spatial distribution of an embedded SiC nanodot and Ge film is imaged by high-angle annular dark field (HAADF). As shown in Fig. 2.10(a), the SiC nanodot is the dark region, while the white band is the Ge layer. The Ge layer does not preferentially accumulate at the SiC site, nor does it even appear to coexist with the Si capping layer. Figure 2.10(b) also displays a high resolution scanning transmission electron microscopy (STEM) image of the same SiC nanodot. Notably, the Ge film is fully epitaxial and wets the Si substrate completely to the SiC/Si interface. From Fig. 2.9 and 2.10, it is clear that, while fully epitaxial and strain-relaxed 3C-SiC nanodots form, there is no excess Ge accumulation to form a morphological QD, nor even conformal wetting of the carbide template sites. Low temperature Si, however, does epitaxially overgrow the carbides. Apparently, the large chemical and lattice mismatch between Ge and SiC, combined with lower-energy Si (001) surface sites, results in complete Ge avoidance of the

carbide under conditions of high adatom mobility. Despite the avoidance of Ge directly over the SiC nanodot, the overall epitaxial nature of the resulting structures appears promising for the creation of artificial nanoscale molecules with engineered electronic and spintronic properties.

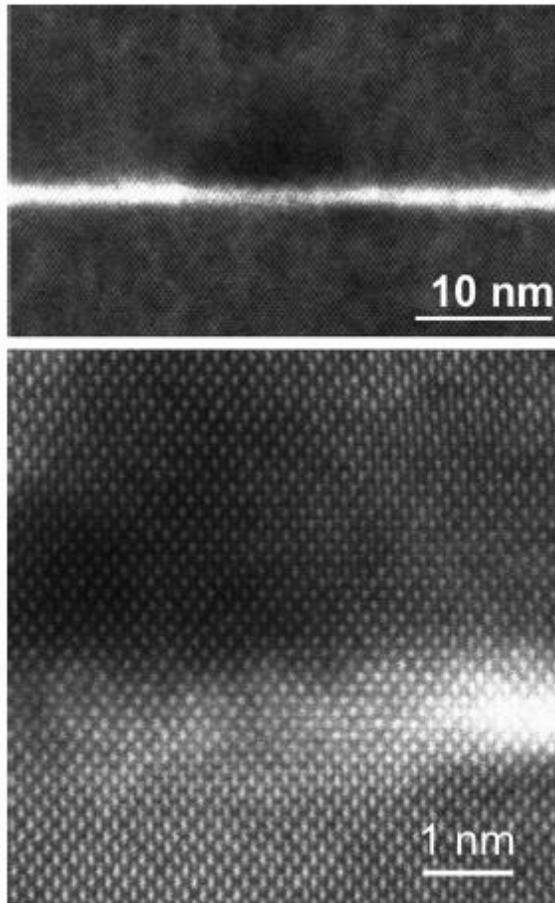


Figure 2.10 HAADF-STEM of Ge/SiC/Si QDs (a) HAADF-STEM image of an embedded SiC nanodot (dark region). Z-contrast clearly shows the deposited Ge film at the substrate-cap interface. No Ge has overgrown the SiC nanodot. (b) High-resolution HAADF-STEM showing the edge of a SiC nanodot and its intersection with the Ge wetting layer.

2.2.4 Fabrication of Ge/SiC/Si QDs and QDMs

The directed self-assembly growth enables deterministic seeding of QDs with arbitrary spatial configurations into QD devices. Therefore it is a promising technique for implementing various types of QD-based architectures as proposed in section 1.2. Figure 2.11 shows a representative AFM image of Si-capped QDM structures (Ge/SiC/Si QDM), with six different spatial configurations referenced to a square face of the die, with the square face size of 45 ± 2 nm, giving an interdot spacing of 22 nm. The configurations of these QDM structures are of research interest because they cover a majority of the proposed QD architectures for quantum simulation and quantum computing in section 1.2. The electronic and spintronic properties of Ge/SiC/Si QD will be studied in the following sections with vertical transport QDM devices fabricated with these QD/QDM structures.

In the fabrication process for these QDMs, an aC:H nanodots precursor pattern is prepared with 1.0 pA·s dose ebeam exposed on an SOI substrate. Being UV-ozone treated for 3 minutes, SiC nanodots form and SiO₂ is desorbed at 850°C in UHV for 30 minutes. Then 1.4 mono-layer Ge is deposited by MBE at 600°C without post-annealing. In the end, the structures are capped with 50 nm Si by MBE at 300°C. The dot spacing d arranges in 11, 22, 45 and 90 nm so that interdot interaction can be investigated as a function of the dot spacing.

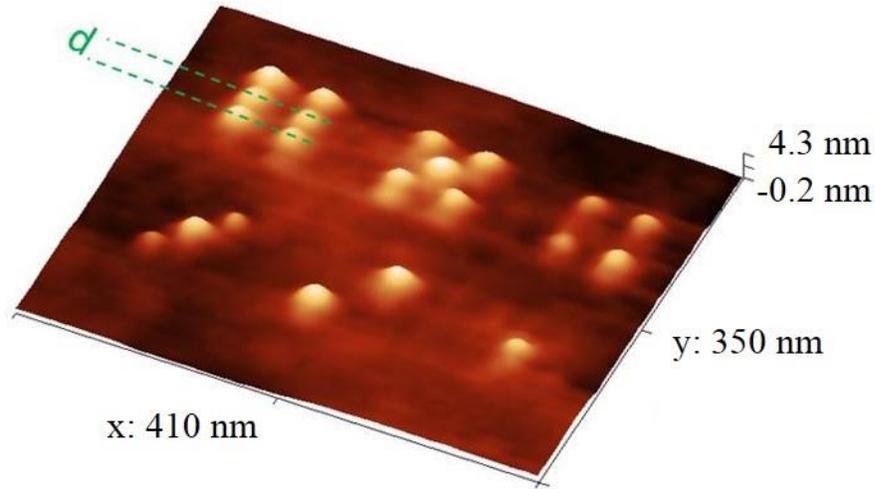


Figure 2.11 AFM image of Ge/SiC/Si QDMs. AFM image of the Si capped (50nm) Ge/SiC QDM structure, with the definition of dice spacing d .

2.3 ELECTRONIC STRUCTURE OF GE/SiC/Si QD

Determination of energy spectrum, kinetics of transitions between electronic levels and interactions of elementary excitations, forms a base of current fundamental studies of QDs.

2.3.1 Electronic states of Ge/SiC/Si QD

Indirect band gap QDs fabricated with IV materials such as Ge, Si, SiC Ge/Si, etc., have been intensively investigated by optical and electrical means [77, 78, 146, 191, 202, 203]. These researches are essential for better understanding experiment results and for the prediction of new ones. As described in section 1.5.4, Ge/Si(001) QDs exhibit a type-II band lineup. A large (~ 0.7 eV) valence band (VB) offset in this heterojunction leads to effective localization of holes in the Ge regions, whereas these Ge regions form potential barriers for electrons. When the hole is

captured by the Ge QD, its Coulomb potential results in the binding of an electron in the vicinity of the QD.

Electronic states have been simulated for $\text{Ge}_{1-x}\text{Si}_x$ /Si heterojunctions [204] and Ge nanoclusters coherently embedded in Si host [70, 203, 205-207]. The simulation results show that the inhomogeneous tensile strain in the Si surrounding Ge nanostructure causes a splitting of the six-fold-degenerate Δ valleys (Δ_6) into the four-fold-degenerate in-plane Δ_4 valleys and the two-fold-degenerate Δ_2 valleys along the [001] growth direction (Fig. 1.9(c)(d)). The Δ_4 and Δ_2 levels shift in the opposite directions with the Δ_2 band moving by twice the amount of the Δ_4 band [76, 77]. Therefore the tensile strain in the surrounding Si reduces the band gap compared to that for bulk Si. A lowering of Si band gap by 0.16 eV induced by the strain on top of Ge islands has been observed experimentally using locally resolved STM by Meyer etc. [208]. The lowest conduction band edge just above and below the Ge island is formed by the Δ_2 valleys yielding triangle potential wells for electrons in the Si near the Si/Ge interface. Therefore one can expect three-dimensional localization of electrons in the strained silicon near the Ge/Si QD (Fig. 1.9(c)).

Regarding the Ge/SiC/Si QD structure fabricate in this work, Petz's calculation suggested that, right at the SiC/Si interface, there is a stress about 1% [118], less than the 4% estimated for the Ge/Si interface in Pryor's model [51]. Hence, the band bending at the SiC/Si interfaces along the growth direction [001] (vertical direction) may create similar but shallower potential wells comparing with Pryor's model. A vertical ([110]) trap assisted tunneling and thermal emission mechanism has been proposed to explain the current-voltage characteristics of SiC/Si heterojunctions [209]. The electron tunnels from the valence band of Si to the trap at SiC/Si interface followed by thermal emission into the conduction band of the SiC. Besides the vertical

confinement, in the Ge/SiC/Si QD devices, electrons are also confined laterally in the Si surrounding the SiC nanodot where the bandgap is lowered, forming an electron-trapping annulus.

2.3.2 Electron transport through QD

The electronic states confined by a QD can be probed by electron transport characterization when a small tunneling is allowed between the QD and nearby emitter and collector leads. When the tunnel coupling is weak, the number of confined electrons in the QD fluctuates weakly, so the number of electrons N is a well-defined number in this case, implying a definite confined charge, $N \times e$, where e is the elementary charge. The quantization of charge permits the use of a ‘capacitance charging model’ in which a single electron is captured by the QD’s self-capacitance C , with charging energy e^2/C . This simple model has been successful in describing transport phenomena such as single-electron transport and Coulomb blockade effects as already discussed in section 1.5. Electron transport through the QD is allowed only at the transition points where N and $(N+1)$ states are both energetically accessible. Otherwise, N is a constant and the transport current is strongly suppressed.

If the tunnel coupling to the leads increases, the number of electrons on the QD becomes less well defined. When the fluctuations in N become much greater than unity, the quantization of charge is completely lost. The transport in this case is usually described by a non-interacting theory. It is more complicated in the intermediate regime where the tunnel coupling is relatively strong but the discreteness of charge still plays an important role. In this case, the transport description incorporates higher order tunneling processes through virtual, intermediate states (Fig. 2.12(b)). When spin is neglected, these processes are known as co-tunneling since they

involve the simultaneous tunneling of two or more electrons [210]. In contrast to first-order tunneling, higher order processes in which the virtual intermediate state costs an additional energy $\Delta\mu(N)$ are allowed for short time scales. Cotunneling process allows the investigation of high-order transport processes and many-body phenomena, such as the Kondo effect, commonly regarded as the result of a coherent superposition of higher-order cotunneling events.

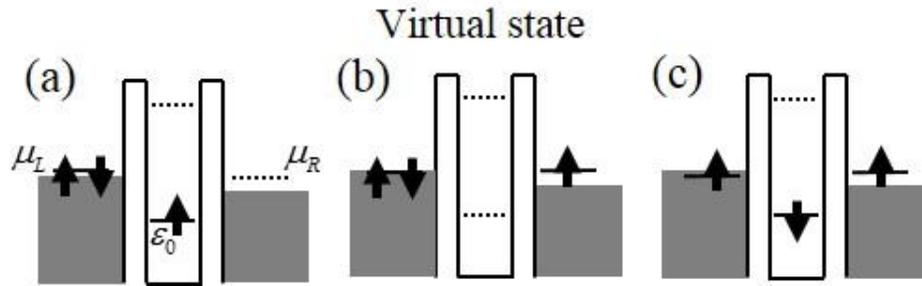


Figure 2.12 Co-tunneling process via a virtual tunnel event.

Kondo phenomena in QDs has been intensively studied both theoretically [211-213] and experimentally [86, 94]. Particularly, the Kondo phenomena involving the virtual tunneling events that effectively flip the spin on a QD via intermediate states have received considerable attention. In a QD, Kondo resonance gives rise to enhanced conductance through the QD when DOS is pinned at electrochemical potentials of the left and right leads sandwiching the QD, $\mu_L = \mu_R$ (Fig. 2.13, left). In the non-equilibrium case, when a bias voltage V is applied between source and drain electrodes, $eV = \mu_L - \mu_R$, the Kondo peak in the DOS splits into two peaks, each pinned to one chemical potential (source and drain) (Fig. 2.13, right). This splitting leads to two specific features in the transport: Firstly, at zero magnetic field, the differential conductance dI/dV versus V mimics the Kondo resonance in the DOS, so a peak in dI/dV is expected around zero voltage. Secondly, a magnetic field lifts spin degeneracy, resulting in two peaks in

the differential conductance at $eV = \pm g\mu_B B$ [214, 215], where g is the Landé factor and μ_B is the Bohr magneton.

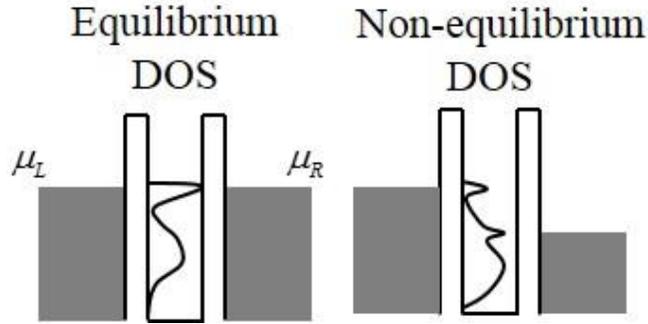


Figure 2.13 Kondo phenomena in QDs. When a bias voltage V is applied between the source (μ_L) and drain (μ_R) electrodes, the Kondo peak in the DOS splits into two peaks, each pinned to one chemical potential.

Electrical manipulation of an electronic two-state system in Ge QDs embedded in Si has been proposed by Pryor, etc. [51]. The manipulation is based on the fact that the electronic ground state localized at the apex of the QD is nearly degenerate with the state localized at the base of the QD. Therefore a small electric field can shift the electronic ground state from apex-localized to base-localized state, which permits sensitive tuning of the electronic, optical, and magnetic properties of the QD. For instance, the exchange coupling between two Ge QDs can be tuned from $500 \mu\text{eV}$ to 0 by shifting the electronic ground states between the apex and base of each QD with a change of voltage of only $\sim 0.1 \text{ mV}$. The strength of the interdot exchange coupling also depends on the dot spacing: A larger dot spacing leads to a weaker interdot exchange coupling. Combining similar geometric and electrical modulation method, exchange interaction is expected to be highly tunable for the directed self-assembly Ge/SiC/Si QD devices in this research.

3 DEVICE FABRICATION

3.1 OVERVIEW

The devices investigated in this research are prepared with QDs/QDMs fabricated by the process described in section 2.2.4. Integrating QDs into devices has been mainly operated in the Nanoscale Fabrication and Characterization Facility (NFCF) cleanroom at University of Pittsburgh and electrodes sputtering has been done in the cleanroom at the Carnegie Mellon Nanofabrication Facility.

The following is the detailed fabrication process and recipes. Precursor carbonaceous nanostructure template is prepared in NFCF as described in section 2.2.1. Chris Petz processes template annealing, subsequent Ge growth and Si capping with MBE. Electrode areas are ebeam lithographed and etched by reactive ion etching system (RIE), followed by aluminum (Al) and gold (Au) sputtering to form Al/Si Schottky barrier contact [216] for subsequent vertical transport measurements. Beginning with a slightly *n*-doped SOI wafer, the outline of the fabrication process is as follows:

1. Cleave a small chip ($\sim 5 \text{ mm} \times 10 \text{ mm}$) from an SOI wafer and clean with modified IMEC/Shiraki cleaning procedure (see section 2.2).
2. Prepare carbonaceous nanodots template on the SOI wafer by EBID.
3. UV-Ozone process, annealing of the template at UHV to form SiC nanodots.
4. Deposit Ge over the SiC nanodot template, then cap the structure with Si by MBE.

5. Pattern, etch and deposit top gates as collectors and back gates as emitters to define vertical transport QD devices on a sub-10 μm scale (EBL, sputtering and ebeam evaporator).
6. Pattern and deposit large size (200 μm) electrode bond pads. These pads are designed to connect the emitter and collector gates to electrode contacts on a chip carrier (EBL, ebeam evaporator).
7. Glue the device chip onto a chip carrier (silver paint) and bond the electrode contacts on the chip carrier to the device electrode bond pads of interest by silver epoxy.

Figure 3.1 shows an integrated QD/QDM device ready for vertical transport characterization. The close-up image on the right shows a ‘crossbar’ electrode lay out. Each cross section site embeds one QD/QDM, sandwiched by one top gate (connected by vertical electrode leads in Fig 3.1) as a collector and one back gate as an emitter (connected by horizontal electrode leads). The details of the electrode structures are discussed in section 3.4. Recipes in the outline listed above are described in section 3.2, 3.3 and 3.4.

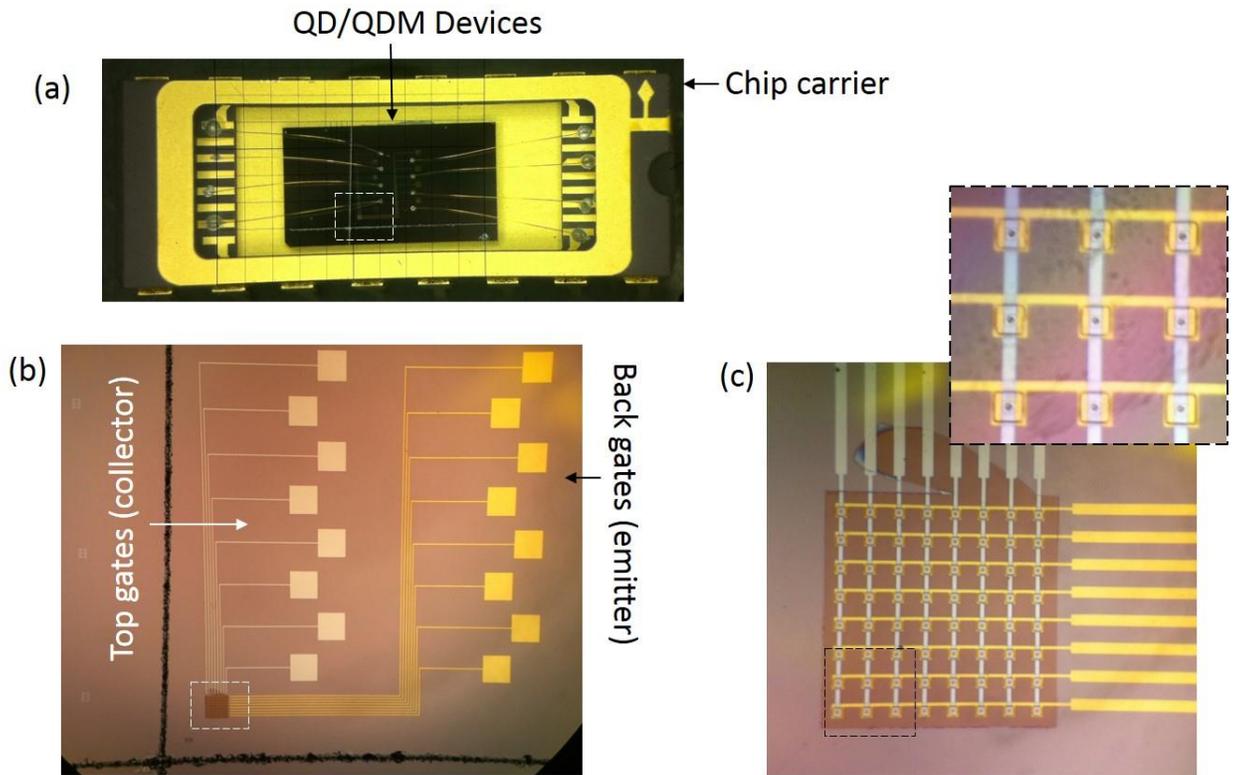


Figure 3.1 An Integrated QD/QDM device. (a) The electrodes of the QD devices are wire-bonded to the chip carrier contacts. (b) and (c) The optical microscope image and its close-up of the QD/QDM devices showing a ‘crossbar’ electrode lay out. Each cross section site embeds one QD/QDM, sandwiched by the top gate (connected by vertical electrode leads) as a collector and back gates (connected by horizontal electrode leads) as an emitter.

3.2 PRECURSOR TEMPLATE FABRICATION

A Raith eLiNE-Plus EBL machine has been used to fabricate aC:H precursor templates. EBL recipe has been developed and optimized to obtain high operation reliability and high resolution. The EBL recipe that has been used is as following.

- 1) Clean an SOI chip with modified IMEC/Shiraki process (section 2.2), and passivate the SOI chip by stripping with diluted (2%) hydrofluoric acid to remove surface oxidation layer and to form hydrogen-terminated surface to prevent immediate re-oxidation.
- 2) Blow N₂ gas to dry the SOI chip.
- 3) Load the passivated chip into EBL high vacuum chamber immediately (less than 10 min) before the surface gets oxidized.
- 4) Expose device areas with predesigned nanodot patterns at ebeam column settings as following: Aperture size = 7.5 μm; Column voltage (electron acceleration voltage) = 20 kV; Ebeam current ~ 21 pA, ebeam working distance ~ 1 mm. At these column settings, the dot with dose 1.0 pA•s corresponds to ebeam dot dwell time ~ 47.6 ms.
- 5) Take SEM images of reference nanodots far away from the device areas after the EBID. The reference nanodots are exposed at the same ebeam column settings but locating about 200 μm away from the device nanodot pattern area. Therefore the SEM imaging provides topographic characterization of all deposited nanodots, while not affecting the device nanodots by electron-scanning. Figure 3.2 shows the SEM image of a reference aC:H nanodot pattern from the sample processing of a device that is used for electronic characterization in this dissertation.

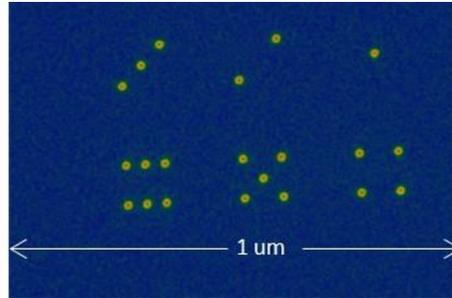


Figure 3.2 SEM image of aC:H nanodot patterns. SEM image of a reference aC:H nanodot pattern from sample processing of the device that is used for electronic characterization in this dissertation.

Exposure parameters have been tested for optimization purpose as discussed in section 2.2.1. Ebeam column aperture size is the smallest allowed by this model to narrow down the diameter of the ebeam. Ebeam focus and focus plan is well adjusted to ensure high resolution ebeam deposition and imaging. A small working distance (the distance from the column to the wafer surface) around 1 mm have been used for best resolution.

3.3 MBE GRWOTH OF GE AND SI CAPPING

The MBE deposition of Ge and Si capping is done by Chris from Jerry Floro's group at University of Virginia. Growth conditions are listed as below:

- 1) Expose the templated nanodots for 3 min to UV-ozone to eliminate excess hydrocarbon contamination between the patterned sites.
- 2) Insert the template into MBE's UHV chamber ($P_{\text{base}}=1 \times 10^{-10}$ Torr) and radiatively heat it up during 9 hour temperature ramp to 500 °C for at least an hour to provide further outgassing. Then desorb the oxide at 850 °C.

- 3) Deposit 1.4 ML Ge at 600 °C.
- 4) Deposit 50 nm Si capping layer at 300 °C.

3.4 ELECTRODE PATTERNING AND DEPOSITION

QDs and QDMs are sandwiched by top gates (collectors)/back gates (emitters) and bonded to a chip carrier for vertical transports characterization. On one device chip, 64 QD patterns are fabricated occupying 8×8 squares grid sites with $20 \mu\text{m} \times 20 \mu\text{m}$ spacing between each grids. Eight top gate leads and eight back gate leads cover 64 QD patterns with crossbar electrode design (Fig. 3.1). This multiplexing electrode design enables convenient testing of multiple devices per chip and per cryostat cool-down. The multiplexing design also benefits investigation of systematic variations in different QDM structures by reducing non-uniformity from chip to chip.

Starting from the Si capped Ge/SiC QD/QDM as shown in Fig. 2.11, the Si surrounding each QD/QDM pattern is etched 400 nm into the SOI device layer for back gates deposition. Al/Au is deposited on Si to form electric contacts. Top gates cover each QD/QDM region by $1 \mu\text{m} \times 1 \mu\text{m}$ squares. The top gates and back gates overlap regions are insulated by depositing SiO_2 layer (~ 30 nm). The QD number contained in these devices varies from 0 to 6 with dot spacing $d = 11, 22, 45, 90$ nm, referred to as “ $n\text{QD}-d$ ”. The schematic image of a vertical transport QD device is shown in Fig. 3.3. The detailed processes and recipes are listed as following.

- Spin Microchem 950 PMMA C4 photoresist at 600 rpm for 10 sec, 4000 rpm for 45 sec, and 600 rpm for 10 sec. A 450 nm thick layer of PMMA is spin coated.
- Hotplate bake, 180 °C for 1 min 30 sec.
- Load into a Raith e-LiNE EBL system and expose pre-designed patterns with electron beam column settings: Aperture size = 10 μm , ebeam voltage = 20 kV, Current measured = 36 pA, ebeam exposure area dose is set at 200 $\mu\text{As}/\text{cm}^2$, and the writing field is 50 μm x 50 μm .
- Develop with MIBK:IPA (1:3) solution for 2 min and rinse with deionized water for 3 min. Then blow dry the chip with N_2 and hot plate baking at 110 °C
- For liftoff steps after metal deposition, soak the chip in acetone for overnight.

The etching is done by the Trion Phantom III LT RIE system. The recipes for SiO_2 and Si etching are both listed:

For SiO_2 etching: Chamber pressure = 15 mTorr, Power = 300W, CHF_3 flow rate = 23sccm, O_2 flow rate = 0, the calibrated etching speed is $\sim 500 \text{ \AA}/\text{min}$.

For Si etching: Chamber pressure = 30 mTorr, Power = 100W, SF_6 flow rate = 10 sccm, O_2 flow rate = 0, the calibrated etching speed is $\sim 4000 \text{ \AA}/\text{min}$.

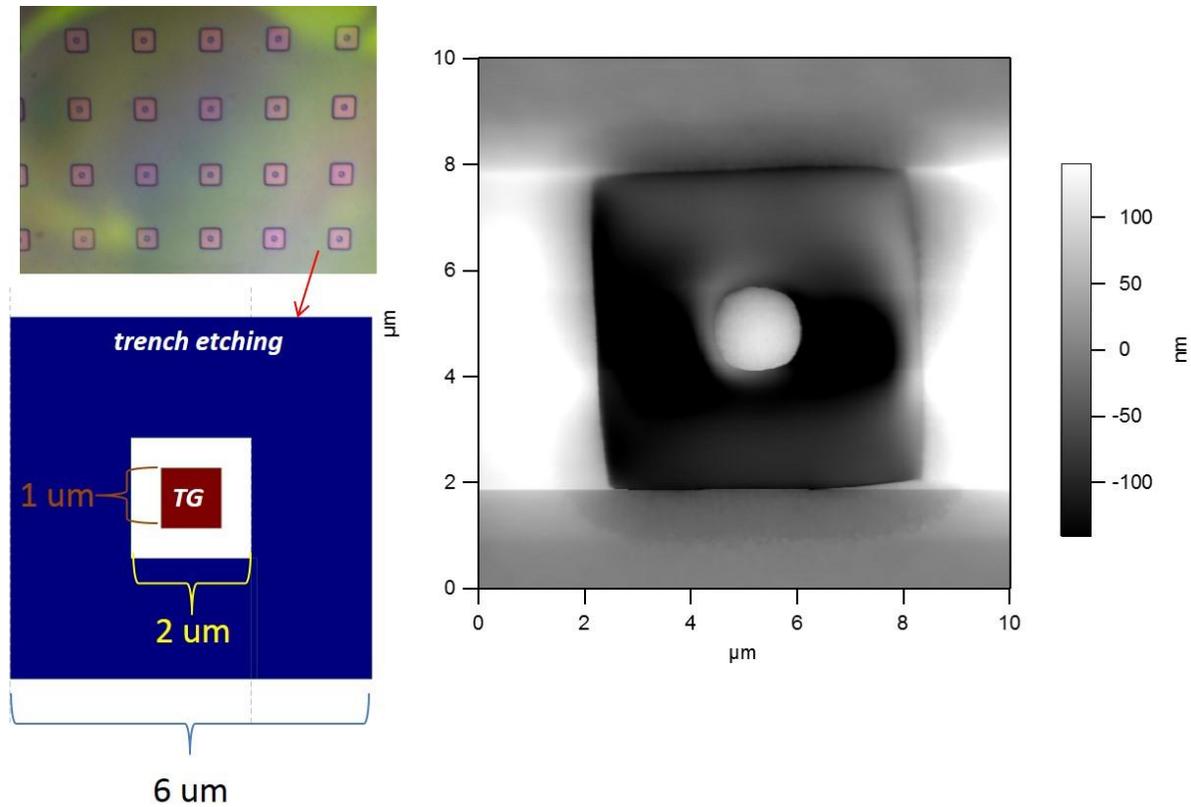


Figure 3.4 EBL patterning and etching of trench structures. Left upper: optical microscopic image of the EBL patterned trench structures before etching. Left lower: the scale of the trench structure. Right: the AFM topography of the etched trench. The center of the trench locates a QD/QDM pattern.

- 3) Deposit Al (6 nm)/Au (50 nm) back gate leads and electrode contact pads by EBL and ebeam evaporator covering part of the trenches, as shown by the green area in Fig. 3.5. The EBL recipe is listed in step 2, and the ebeam evaporator uses ebeam voltage 6 kV for both Al and Au deposition.
- 4) Deposit 50 nm SiO₂ insulating layer over the QD pattern areas to electrically insulate the back gates from the subsequent deposition of top gates. The recipe is the same as in step 1.

- 5) Etch the SiO₂ right on top of the QD/QDM patterns into the Si capping layer on top of the dots, using the recipes listed in step 2.
- 6) Deposit Al (20 nm)/Au (30 nm) top gate leads and electrode contact pads by EBL and ebeam evaporator with the same recipe as in step 3.
- 7) Glue the QD device chip to a 16 pin chip carrier by silver paint. Bond the top gate and back gate contact pads to the chip carrier's electrode contacts by silver epoxy.

Figure 3.5 shows the electrode and etched area layers with different colors representing each process. The top gate is not shown in this image for a better clarification of the back gate and trench structures.

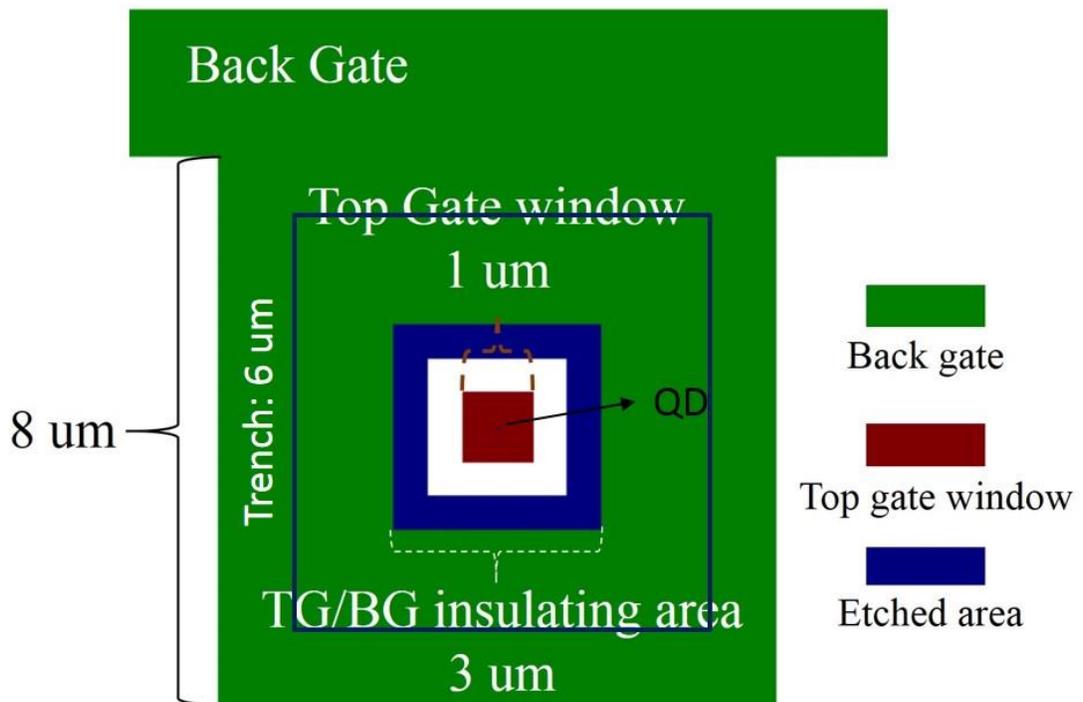


Figure 3.5 The top-view of device electrode structures. The schematic top view of different processing layers without showing the top gate to reveal the structures under the top gate.

4 MAGNETOTRANSPORT THROUGH GE/SiC/SI QD/QDM

4.1 INTRODUCTION

Self-assembly Ge/SiC/Si QD/QDM devices fabricated in chapter 3 are investigated by vertical electron transport measurements, at cryogenic temperatures, to characterize the electrons confined by QDs. Applying magnetic fields induces energy shifts related with the electron's spin degrees of freedom. The interdot interactions of QDMs are expected tunable by applying electric fields and by varying QD spatial configurations. In the following sections, vertical transport measurement set-up is described in section 4.2. Transport current intensity spectrum is shown in section 4.3. A resonant tunneling model is described in details in section 4.4 to explain the transport data. Section 4.5, 4.6 and 4.7 discuss the energy spectrum of QDs, kinetics of the transitions between electronic levels, spintronic dynamics of transport carriers and the interdot interaction.

4.2 MEASUREMENT SET-UP

Magnetotransport is conducted by applying dc voltage from collector gates (top gates) to emitter gates (back gates), measuring the transport current through each device with magnetic field sweeping up to 6 Tesla (see Fig. 4.1 for measurement scheme). The transport is measured at cryogenic temperatures so that thermal excitation energy $k_B T$ does not exceed carrier's energy spacing ΔE . The device is loaded in a dilution refrigerator (Oxford DR200 system) and the DR is cooled down to 70 mK. To observe temperature effects on the transport, magnetotransport at 5 K is also conducted by a Physical Property Measurement System (Quantum Design, PPMS).

Emitter leads and collector leads are selected to characterize individual devices located at the conjunctions of these leads. Most of the transport current is contributed from the electron transport through QDs/QDMs at the conjunction because the resistance between the selected gates over the sandwiched pattern is much lower than that between other devices.

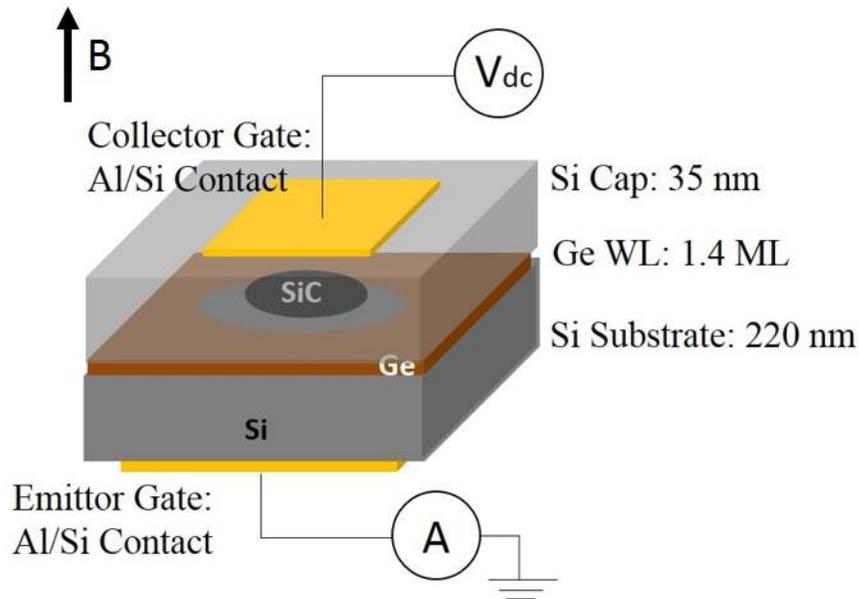


Figure 4.1 Vertical transport measurement scheme for one Ge/SiC/Si QD device.

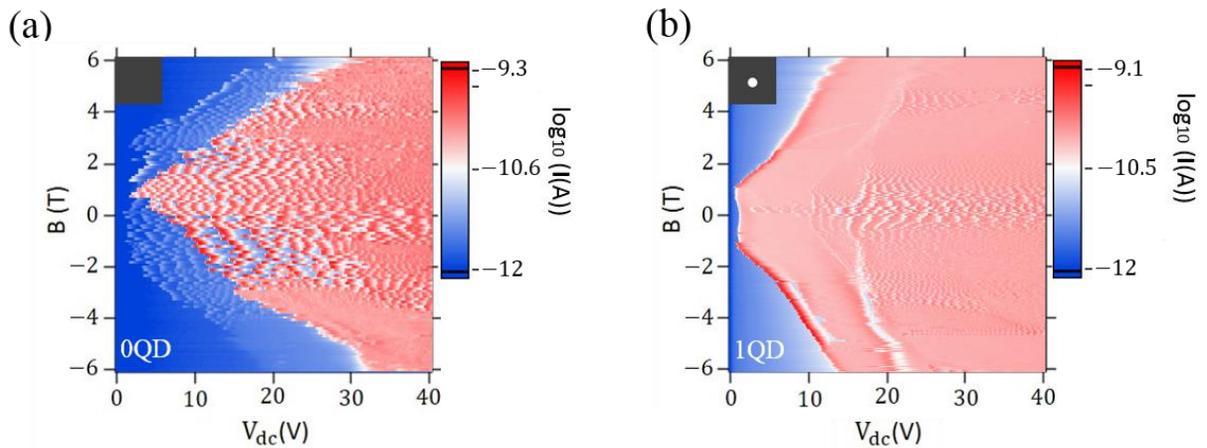
A typical current-voltage (IV) measurement set-up is shown in Fig. 4.1. A dc voltage is applied to the collector gate of the device from a dc analog output (DAC) of a lock-in amplifier, amplified by a voltage amplifier ($\times 14$). The transport current from the emitter gate is amplified by a current amplifier (Femto Current Amplifier). The amplified signal is fed into an analog-to-digital input (ADC) of the lock-in amplifier. A $10\text{ M}\Omega$ resistor is placed in series with the device to limit the transport current.

In the PPMS measurement, the two-terminal measurement scheme is slightly modified: the capacitance and conductance of the device are measured by applying a small amplitude ac voltage (from a lock-in amplifier) superimposed on dc bias voltages. The dc voltage biases the

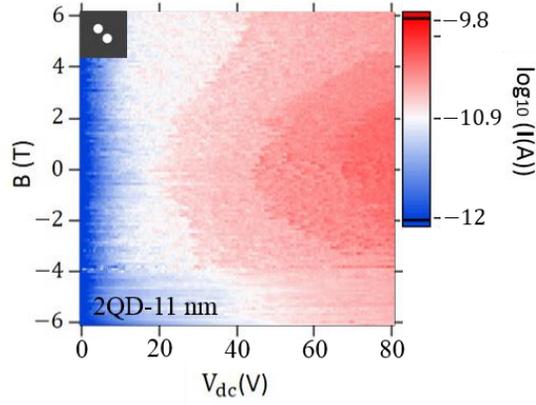
energy levels in QDs. The resistance and capacitance of QD devices at varying energy levels are extracted from the lock-in measurement of the ac signal. To investigate spin effect on transport, magnetic fields are applied along the QD growth direction (z direction) in both measurements.

4.3 TRANSPORT DATA

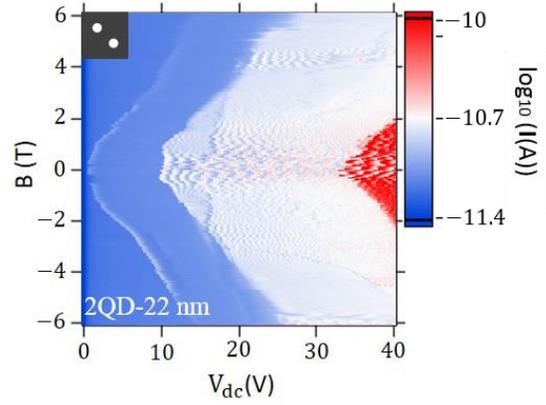
Vertical magnetotransport measurement focuses on the magnetotransport through QDs/QDMs at low temperatures. Magnetotransport data (current intensity (z -axis) graph) with DR temperature at 70 mK is presented in Fig. 4.2. QD spatial configurations are schematically drawn on the upper left corner of each graph, with interdot spacing d noted on the lower left corner. These configurations have been systematically named as “ n QD- d ”. In each current intensity graph, dc bias voltage (fast scan axis, V_{dc}) is the x -axis and magnetic field (slow scan axis, B) is the y -axis. The current intensities are plotted in log scale. Details of transport pattern are discussed associated with corresponding dot spatial configurations in the following sections.



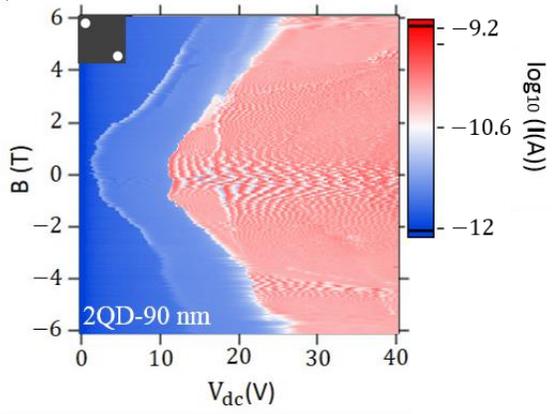
(c)



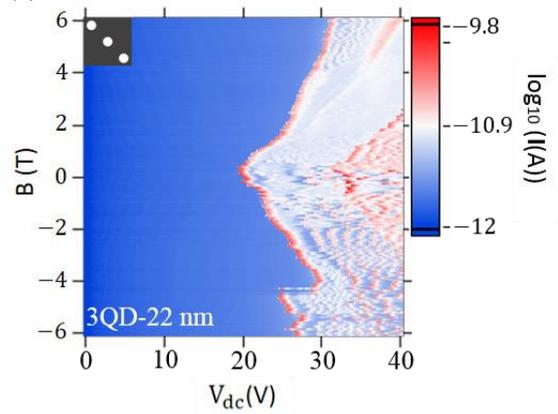
(d)



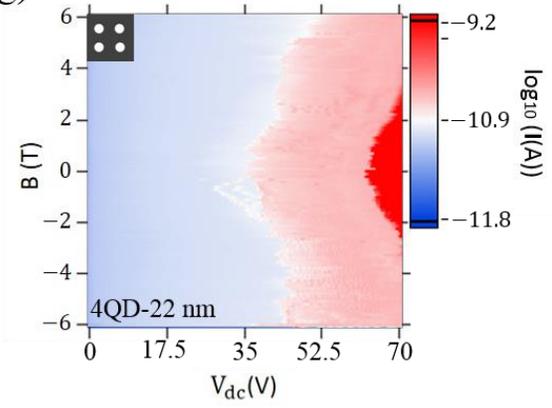
(e)



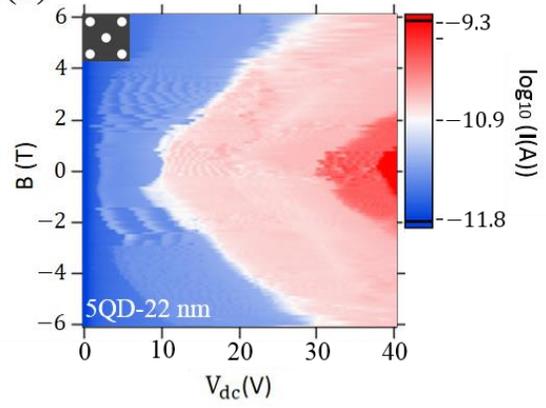
(f)



(g)



(h)



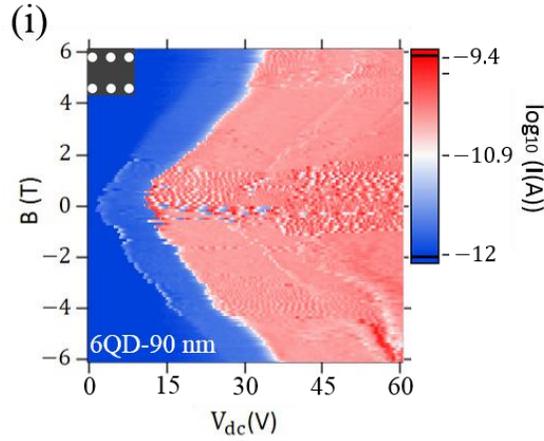


Figure 4.2 Current intensity graphs of IV measurements with sweeping magnetic field for (a) Reference device containing zero QD (0QD device). (b) 1QD device. (c) 2QD-11 nm device. (d) 2QD-22 nm device. (e) 2QD-90 nm device. (f) 3QD-22 nm device. (g) 4QD-22 nm device. (h) 5QD-22 nm device. (i) 6QD-90 nm device.

Figure 4.3 shows capacitance and conductance measured at 5 K by PPMS. The capacitance and conductance intensities are shown for three typical devices: reference device (0QD), 1QD and 6QD-90 nm device, as a function of magnetic field (fast scan axis, x) and dc bias voltage (slow scan axis, y).

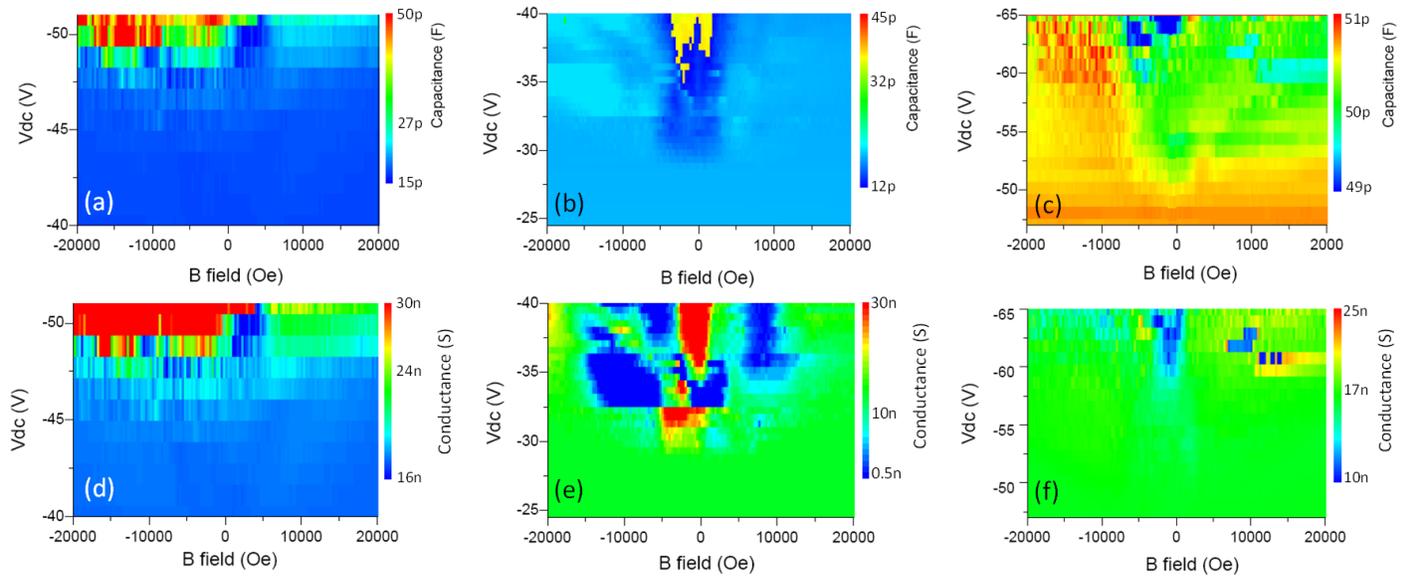


Figure 4.3 CV measurements of QD/QDM devices. Capacitance and conductance of three QDM devices as a function of magnetic field and top gate bias at 5 K. (a,d) 0-QD, (b,e) 1-QD, (c,f) 6-QD. Sharp features near $B = 0$ are observed at low magnetic fields that are not seen in the control structure (0-QD)

Although V-shape conductance peaks centered at zero magnetic field are still observable for devices containing QD/QDM (Fig. 4.3 (e, f)), the transport features in Fig. 4.2 are partially smeared out when the measurement is conducted at 5 K. This temperature effect indicates that the trapping energy at the Si/SiC interfaces are shallow as discussed in section 2.3.1.

The data/image analysis and physical interpretations in the following sections mainly focus on the current intensity spectrum at 70 mK (Fig. 4.2).

4.4 RESONANT TUNNELING

Charge transport in directed self-assembly Ge/SiC/Si QD/QDM device is associated with electrons tunneling from a lightly n -doped Si substrate (the Si device layer of SOI wafer is lightly n -doped with phosphorous), through QDs/QDMs, to the intrinsic Si capping layer. The transition of the relative concentration of Al from 1.0 to 0.0 normally occurs at a length about 20 nm at the Al/Si interface [216], comparable to the capping layer thickness. Hence, the diffused Al atoms from Al/Si contacts also provide electrons as donors like the doping phosphorous atoms. Au is deposited immediately after Al evaporation and the sample is kept in high vacuum in the ebeam evaporator chamber. Therefore the rectifying Schottky-barrier formed at the Al/Si interface is considered as a ‘fresh’ contact with barrier height around 0.45 eV [216]. Two spatially-localized interface trap states are proposed to localize in the Si surrounding the apex

and the base of the SiC islands due to the intrinsic structure/bonding of the SiC/Si interface. The apex-localized-state (ALS) and the base-localized-state (BLS) in this dissertation refer to the two nearly-degenerate states confined at the apex and the base of the Ge/SiC/Si QD, similarly as described in Ref. [51]. The orbital ground state of the QD is presumed to localize at the apex of the QD, with the first excited state located at the base. The SiC island forms a potential barrier between the ALS and the BLS. The entire QD device can be described as a triple-barrier resonant tunneling (TBRT) structure, as shown in Fig. 4.4. The electron chemical potential of the device is tuned by the applied dc voltage between the emitter and collector gates.

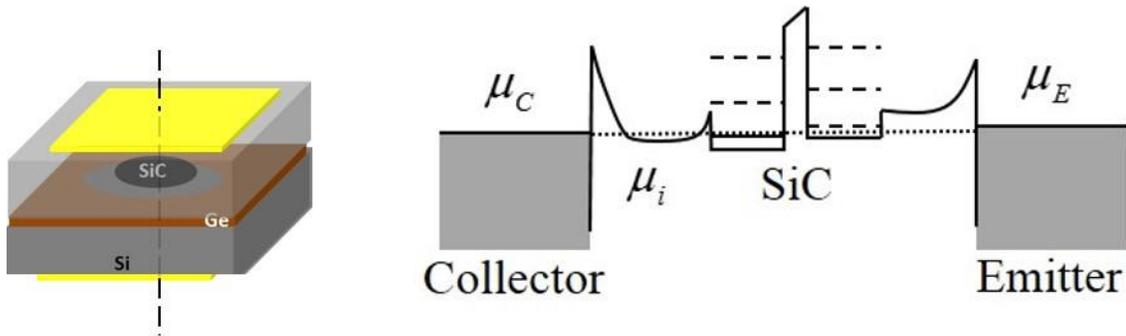


Figure 4.4 The conduction band (CB) diagram of a Ge/SiC/Si QD device at zero bias. On the right is the schematic CB diagram describing the TBRT transport model along the dashed line through the center of the QD (left). The figures are not up to scale.

As shown in Fig. 4.4, the emitter and the collector electrochemical potentials, μ_E and μ_C , affect the QD level occupancy, assumed to be filled with N electrons, with Schottky tunnel barriers at both emitter and collector. Kinetics of transitions between the electronic levels in the QD can be described by a constant interaction model [146, 217]. The constant interaction model assumes that the Coulomb interaction between the electrons on a QD and the electrons in the surroundings is parameterized by a single constant capacitance, the self-capacitance C . It is also

assumes that the discrete energy levels in the QD are not affected by electron-electron interactions, i.e. the number of the electrons on the QD. Figure 4.5 shows a schematic equivalent electric circuit representing QDs capacitively coupled to emitter and collector gates with tunnel barriers, i.e. C_{kE} , R_E and C_{kC} , R_C , respectively.

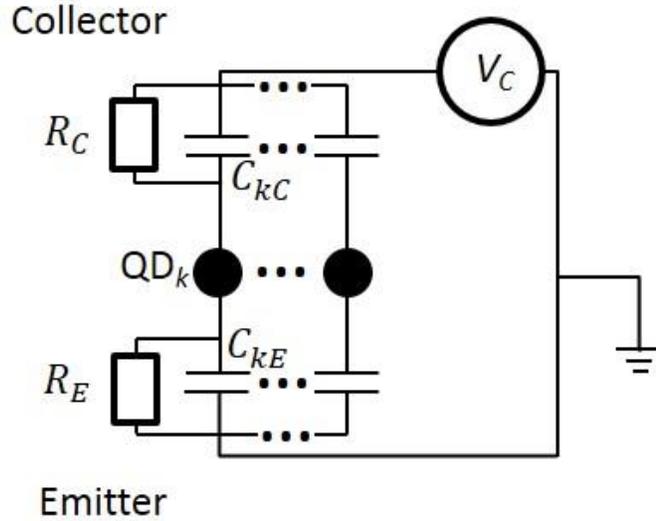


Figure 4.5 An equivalent electric circuit for the constant interaction model. A schematic equivalent electric circuit representing QDs capacitively coupled to the emitter and collector gates with tunnel barriers. R_C , C_{kC} (R_E , C_{kE}) is the tunnel coupling between QD_k and the collector (emitter) gate.

Based on the constant interaction model, the electrochemical potential for the N^{th} electron, i.e., the energy required to add electron N to the k^{th} QD, $\mu_k(N)$, can be written as [146]:

$$\mu_k(N) = \varepsilon_N + \frac{e^2}{C_k} \left(N - \frac{1}{2} \right) + e[\alpha_{kE}V_E + \alpha_{kC}V_C]. \quad (4.1)$$

Here ε_N is the energy level of the N th electron in the confinement potential; V_k , V_E , V_C are electrostatic potentials on the k^{th} QD, the device emitter gate and collector gate respectively;

$\alpha_{kE(C)} = C_{kE(C)} / C_k$ is the lever arm of the emitter (collector), used to relate the gate voltage to the potential on the QD; and C_k, C_E, C_C are the self-capacitance of the k^{th} QD and the mutual capacitance between k^{th} QD and the emitter (collector).

Particularly, in the case of the TBRT structure in this dissertation, it is also reasonable to assume that the thermal energy is low compared to the single-particle spacing, and the tunnel barriers (Al/Si Schottky barrier~ 0.45 eV) are high enough to ensure that the electrons are sufficiently localized to the QD. With these assumptions, electron transport from the emitter gate to the collector gate is blocked at zero or small dc bias.

Experimentally electron tunneling through QDs can be characterized from IV measurements. Figure 4.6 shows a typical IV characteristics at zero magnetic field for a reference device that does not contain any dots (0QD). Sharp current oscillations are observed (Fig. 4.6(a)), superimposed on a nearly zero current background. The threshold for the onset of these oscillations increases approximately linearly with the strength of the applied magnetic field (Fig. 4.6(b)). These oscillations are attributed to resonant tunneling of electrons from the emitter gate, through the Ge wetting layer, to the collector gate. This pattern of current oscillations appears for all of the n QD devices ($n=0, \dots, 6$).

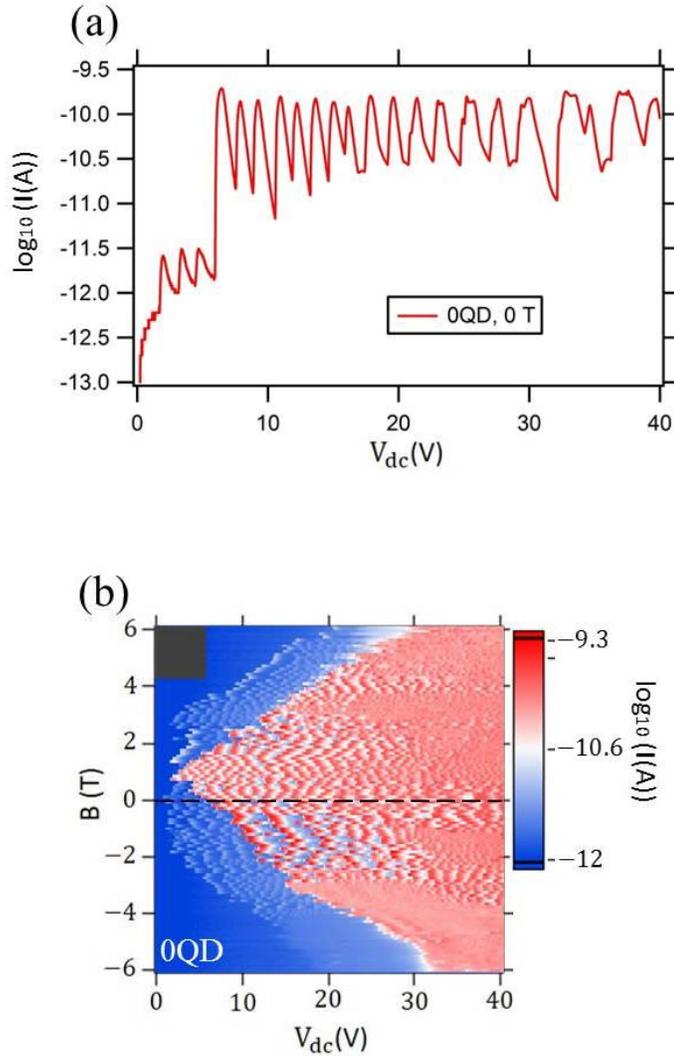
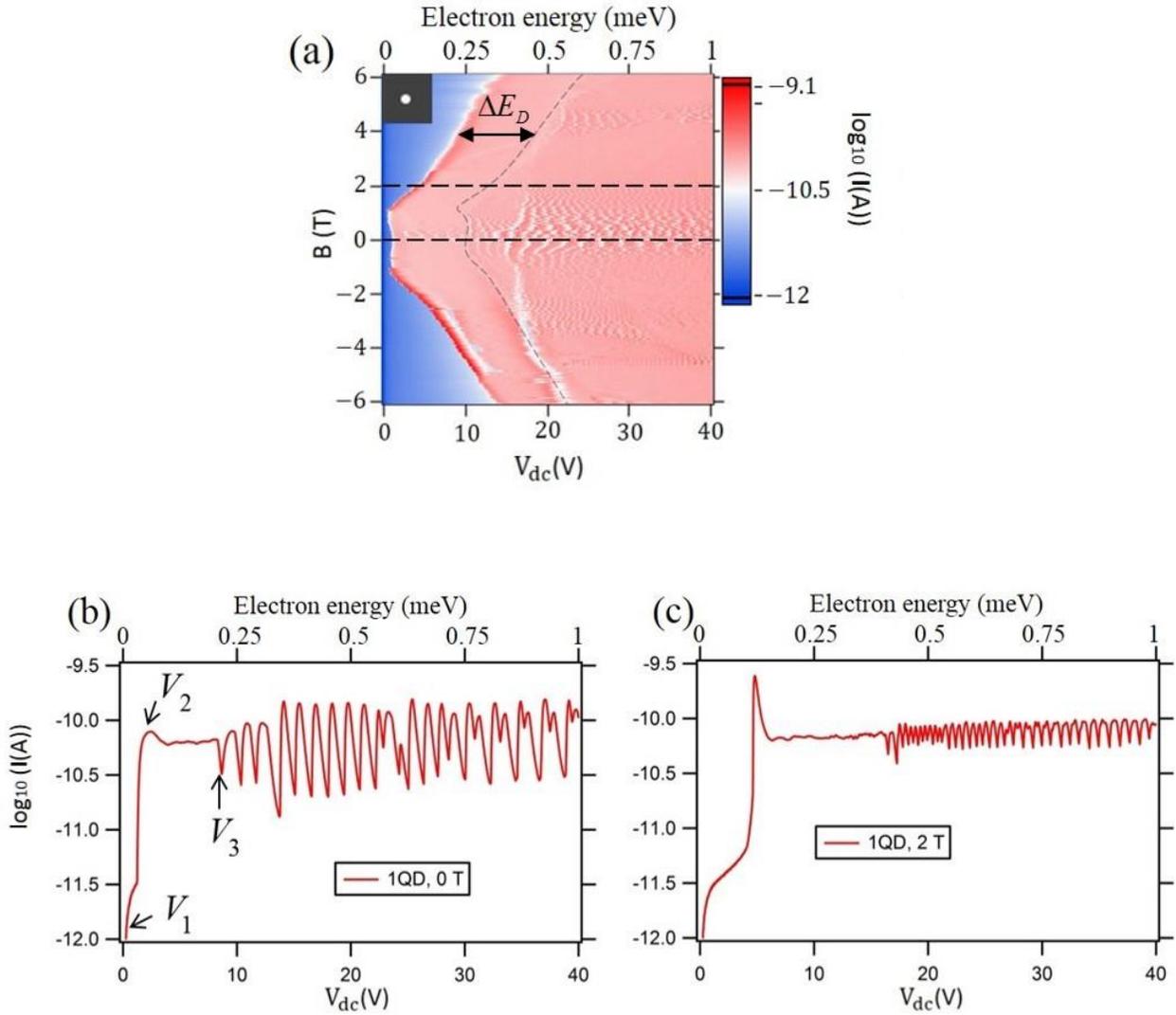


Figure 4.6 Magnetotransport of a reference device at 70 mK. (a) The oscillation of the current is attributed to the electron tunneling through the Ge wetting layer. (b) The current intensity (z -axis) vs. the dc bias voltage (x -axis) and the magnetic field (y -axis). The line cut shows the IV characteristic at zero magnetic field in (a)

Figure 4.7 shows magnetotransport measurements of a 1QD device. In the absence of an applied magnetic field (Fig. 4.7(b)), the current is low up to a threshold of 1.5 V (“ V_1 ”), showing a resonance at $V_{dc}=2$ V (“ V_2 ”), followed by the onset of sharp oscillations at $V_{dc}=8$ V (“ V_3 ”). Application of a magnetic field exceeding 1 Tesla causes the onset peak to become much more

pronounced (Fig. 4.7(c)). The oscillation period undergoes distinct changes at two values of V_{dc} that have visible signatures separated by the primary resonant tunneling peaks and the dashed eye-guide in Fig. 4.7(a). Each change is one of a family of thresholds that for low magnetic fields appears to vary quadratically with B and then increases linearly at higher magnetic fields.



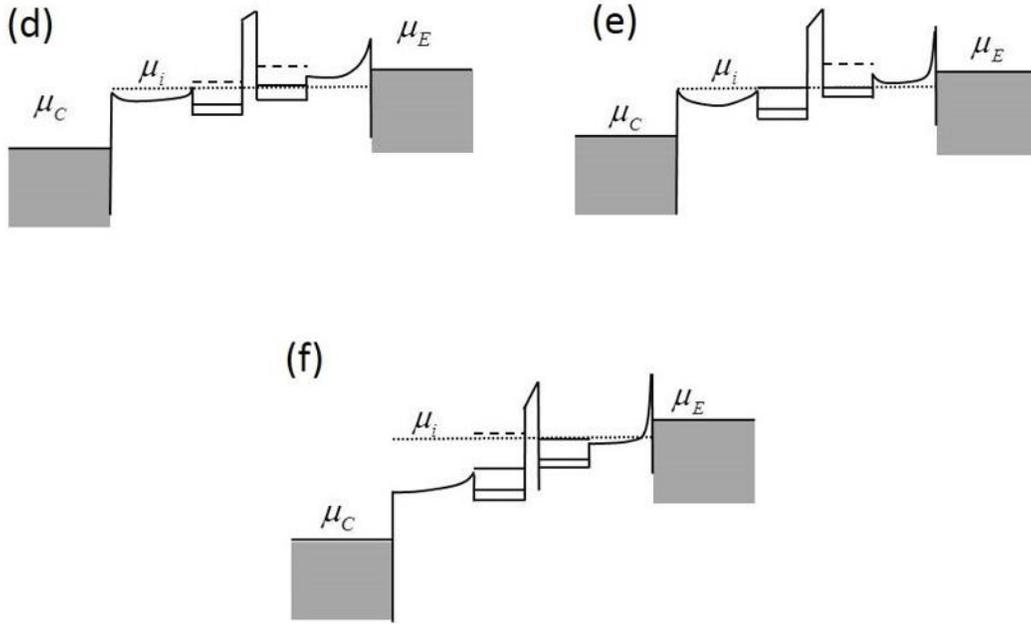


Figure 4.7 Magnetotransport of a 1QD device at 70 mK. (a) The current intensity (z -axis) vs. the dc bias voltage (x -axis) and the magnetic field (y -axis). The dash-line is an eye guide of the secondary tunneling peaks, and ΔE_D represents the charging energy of a second electron to the BLS. (b) and (c) show the line cuts representing the IV curves at 0 T and 2 T respectively. (d), (e) and (f) The schematic CB diagram with the arrowed bias voltages as indicated by V_1 , V_2 and V_3 in (b) respectively. The drawing is not up to scale. (d) One charge accumulates to the base quantum confinement as the voltage increases. The primary resonant tunneling occurs when the lowest bound states are both accessible for the ALS and BLS. (f) A second electron is charged to the ALS as the voltage keeps increasing.

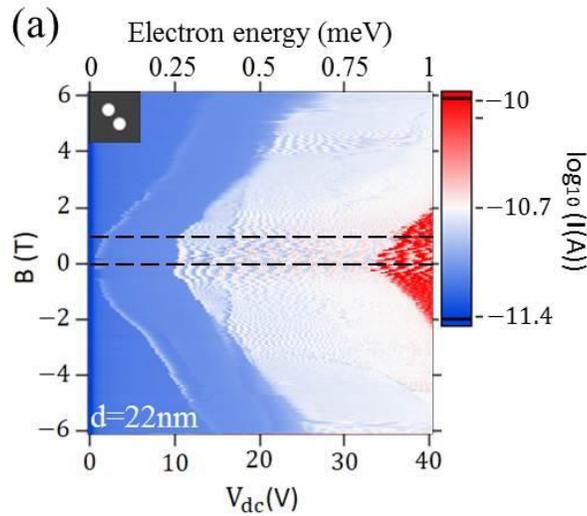
To help understand the magnetotransport characteristics, the electron potential at different bias voltages is sketched (not to scale) in Fig. 4.7(d-f) for three gate bias conditions: V_1 , V_2 , and V_3 defined in Fig. 4.7(b). When the positive dc bias increases, electrons from the emitter gate are transported to the collector gate. The current is comprised of two components: elastic peaks due to resonant transmission between aligned energy states, and an inelastic background

signal which also exhibits peaks when the energy associated with processes matched the energy difference between final and initial states [218].

When an occupied ALS state becomes resonant with the top *i*-Si conduction band, it can tunnel with a high probability, leading to the peak V_2 . After the electron leaves, a sequence of tunneling processes can take place to repopulate the state, either directly from the emitter or by sequential tunneling BLS→ALS followed by repopulation of the BLS state from the emitter. Because there is no direct tunneling from one side of the Ge layer to the other, there is no interference to the tunneling through the QDs/QDMs. As V_{dc} is increased further, an abrupt transition takes place (“ V_3 ”) in which direct tunneling (without intermediate relaxation within the QD) takes place. A “replica” feature is clearly visible for this threshold in which electrons can now tunnel to the collector either from the BLS state (in addition to the ALS state). The energy difference between the primary resonant tunneling peak (V_2) and the nearest secondary tunneling peak (V_3) can be used to characterize the energy difference between the two lowest accessible energy levels for ALS and BLS.

For the QDMs (Fig. 4.8), there are two distinct ALS ground states that can be occupied. The behavior of two QD molecules is shown: 2QD-22 nm (Fig. 4.8(a-c)) and 2QD-90 nm (Fig. 4.8(d-f)), respectively. The first threshold corresponds to the occupation of the lowest ALS of the two dots. The most significant difference with the single QD case is that aside from the resonance there is no appreciable increase in the net current (apart from a slowly increasing background). Only at the second threshold (~10 V) does the current increase significantly. With the calibration of the lever-arm ratio, the energy difference is given by $\Delta U_{A-B} = e\alpha_k \Delta V_k$, where

the index k is used to refer to a specific device. These charging energies for various devices are calculated and listed in Table 4.1. As shown in transport current intensity graphs in Fig. 4.6, 4.7 and 4.8, the current oscillations arise when the biased dc voltage increases for all devices. However the current steps caused by the TBRT are only observed for the dot-devices. The current oscillations indicate the existence of two-dimensionally confined electronic states at the interface between the Ge wetting layer and the Si capping/substrate layer caused by their conduction band offset. The current oscillations features are superimposed on the single- and double-QD device transport current intensity graphs, which are associated with spatially extended states localized near the Ge wetting layer.



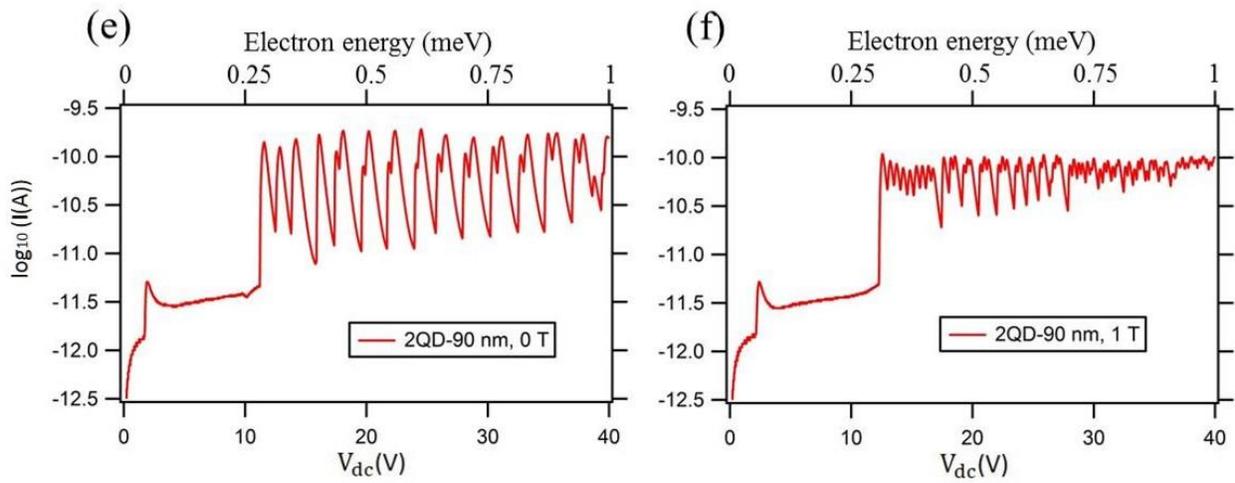
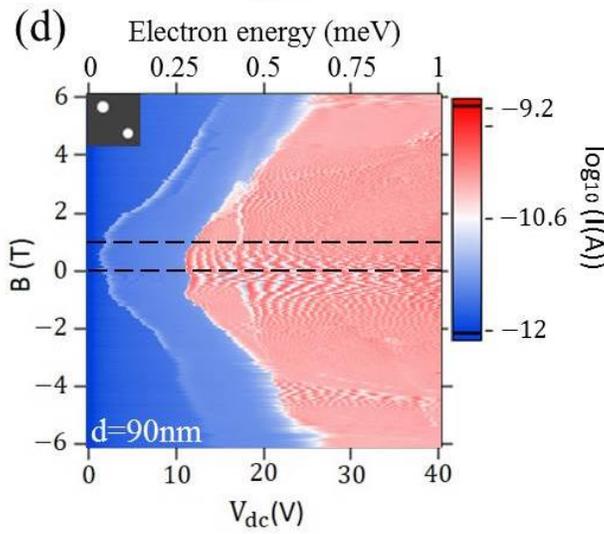
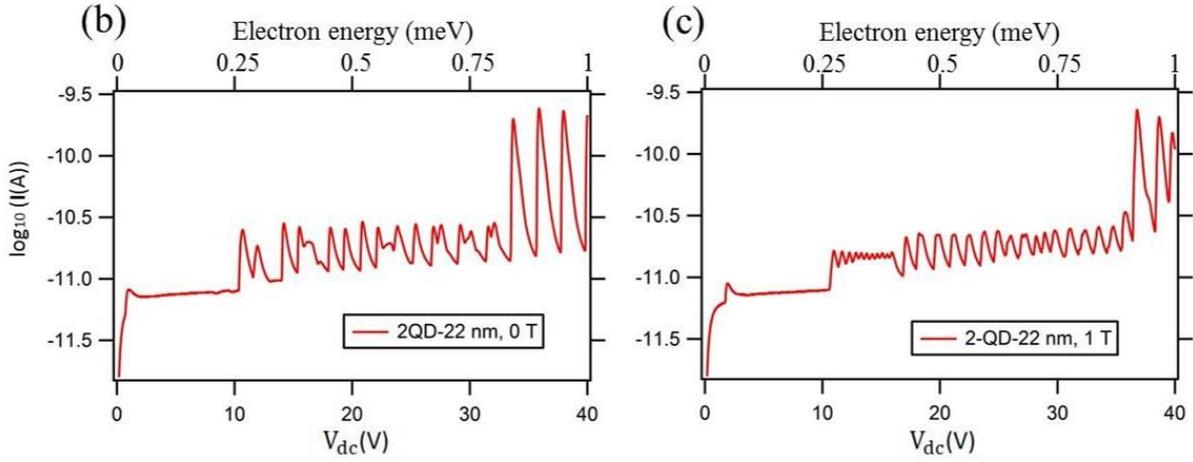


Figure 4.8 Magnetotransport of two 2QD devices at 70 mK. The current intensity (z -axis) vs. the dc bias voltage (x -axis) and the magnetic field (y -axis) for (a) the 2QD-22 nm device and (d) the 2QD-90 nm device. The line cuts at 0 T and 1 T are shown in (b, e) and (c, f) respectively for both of the devices. The current oscillations are attributed to electron tunneling through the Ge wetting layer in the devices.

4.5 MAGNETOTRANSPORT

Applying magnetic fields parallel to the QD growth direction leads to a shift of energy levels in both of the apex and the base region. Magnetotransport measurements provide a useful spectroscopic probe of orbital and spin states in tunneling processes. At low magnetic fields, a diamagnetic (quadratic with field) energy shift is observed [81, 219], while at higher magnetic fields the dominant contribution is linear, due to Zeeman spin splitting [149, 220]. This kind of crossover from diamagnetic to Zeeman has been theoretically predicted and reported experimentally as well on ensemble photoluminescence measurements [149, 219, 221]. Here, the diamagnetic energy shift and its transition to the Zeeman energy shift is directly measured by transport in a single QD device.

In the effective-mass theory, the Hamiltonian for a single electron in a uniform magnetic field \mathbf{B} is

$$H_{eff} = [\mathbf{p} + e\mathbf{A}(\mathbf{r})] \cdot \frac{1}{2m_e^*(\mathbf{r})} [\mathbf{p} + e\mathbf{A}(\mathbf{r})] - eV_e(\mathbf{r}) + \frac{g\mu_B}{\hbar} \mathbf{S} \cdot \mathbf{B} \quad (4.2)$$

where $\mathbf{B} = \nabla \times \mathbf{A}$, is the magnetic field. $\mu_B = e\hbar / 2m_e$, is the Bohr magneton. V_e is electron potential. $m_e^*(\mathbf{r})$ is the position-dependent effective mass of the electron. g is Landé factor and

\mathbf{S} is electron spin. Considering the magnetic field as a perturbation, the Hamiltonian can be written as:

$$H_{eff} = H_0 + H_I + H_{II}, \quad (4.3)$$

where

$$H_0 = H_{00} + \frac{g\mu_B}{\hbar} \mathbf{S} \cdot \mathbf{B}, \quad (4.4)$$

$$H_I = \frac{e}{2} \left[\mathbf{p} \cdot \frac{1}{m_e^*} \mathbf{A} + \mathbf{A} \cdot \frac{1}{m_e^*} \mathbf{p} \right], \quad (4.5)$$

$$H_{II} = \frac{e^2}{2m_e^*} \mathbf{A}^2, \quad (4.6)$$

in which

$$H_{00} = \mathbf{p} \cdot \frac{1}{m_e^*} \mathbf{p} - eV_e(\mathbf{r}), \quad (4.7)$$

is the Hamiltonian with $\mathbf{B} = 0$. The eigenfunctions of H_{00} is denoted as $|i\rangle \equiv \psi_i(\mathbf{r})$, corresponding to eigenvalues, E_0^i . The 1st order energy shift in \mathbf{B} (the Zeeman energy shift), E_Z , is the sum of electron spin energy and the first-order perturbation due to H_I

$$E_Z = g\mu_B \mathbf{B} \cdot (\mathbf{L} + \mathbf{S}), \quad (4.8)$$

where \mathbf{L} is the angular momentum and \mathbf{S} is the electron spin.

For the QDs fabricated in this research, the confinement potential $V_e(\mathbf{r})$ and the effective electron mass $m_e^*(r)$ have an axial symmetry that lies parallel to the magnetic field \mathbf{B} . In this case, $\mathbf{B} \cdot \mathbf{L}$ is a constant of the motion and the gauge can be chosen as $\mathbf{A} = -\frac{1}{2} \mathbf{r} \times \mathbf{B}$, with origin on the symmetry axis. Thus, $H_I = e/(2m_e^*) \mathbf{B} \cdot \mathbf{L}$. The ground state $|0\rangle$ has magnetic quantum number $m_l = 0$. Therefore, $\mathbf{B} \cdot \mathbf{L}|0\rangle \equiv 0$ and $\langle i|H_I|0\rangle = 0$. This indicates the second-order

Zeeman term vanishes, and the diamagnetism term equals to the ground state expectation value with the direction of \mathbf{B} along the QD growth direction (z -direction) [221]

$$E_D = \frac{e^2}{2m_e^*} \mathbf{A}^2 = \frac{e^2 x^2 + y^2}{8m_e^*} B^2 = \frac{e^2 a_{dx}^2}{4m_e^*} B^2 = \gamma B^2. \quad (4.9)$$

In a Ge/SiC/Si QD system, the confined electrons locate in the weakly strained Si annulus region surrounding the SiC nanodot (section 2.3.1). Therefore it is reasonable to assume $m_e^* = 0.19m_0$,

the transverse effective mass of the electron in Si (m_0 is the rest electron mass);

$a_{dx} = \sqrt{\frac{1}{2} \langle x^2 + y^2 \rangle}$ is defined as the diamagnetic length for the ground state, which equals the

expectation value of the ground-state radius; and $\gamma = e^2 a_{dx}^2 / 4m_e^*$ is commonly defined as the diamagnetic coefficient [81, 222, 223].

The second-order perturbation theory is valid only if the magnetic length $l_B = (\hbar / Be)^{1/2}$ exceeds the diamagnetic length a_{dx} [221]. As a result, the diamagnetic shifts transits to the linear Zeeman shifts at a critical magnetic field B_C . For 1QD device as shown in Fig. 4.7, the first-order and second-order energy shift transition occurs at a critical field $B_C \approx 2.5$ T. Therefore the upper-bound of a_{dx} is estimated around 16 nm which is a reasonable upper-bound value for QD structures of around 10 nm in radius.

The Zeeman energy shift in the low field region is given by $dE_Z = \frac{1}{2} g \mu_B dB$, which is associated with the applied dc bias voltage by $dE_Z = e \alpha_{iC} dV_C$. Thus, the lever-arm ratio can be calculated from the slope of the primary resonant tunneling voltage versus the magnetic field:

$$\alpha_{iC} = \frac{g\mu_B}{2e} \left(\frac{dV_C(B)}{dB} \right)^{-1}, \quad (4.10)$$

where g is Lande g -factor of the electrons confined in silicon around the SiC QDs. It is assumed that $g \approx 2$, close to the g -factor value for free electrons in bulk silicon [224] since the electrons are confined in the epitaxially overgrown silicon capping layer and substrate. A linear fit of Zeeman energy shift gives the lever-arm ratio for the single-QD device: $\alpha_{iC} = 2.6 \times 10^{-5}$.

In the diamagnetic energy shift region, a parabolic fit of the resonant tunneling voltage versus the B field gives the diamagnetic coefficient: $\gamma = \frac{1}{2} \frac{d^2 E_D(B)}{dB^2}$. The energy shift is related

to the collector voltage by $dE_D = e\alpha_{iC} dV_C$. Thus the diamagnetic coefficient can be written as

$\gamma = \frac{e\alpha_{iC}}{2} \frac{d^2 V_C}{dB^2}$. Together with $\gamma = e^2 a_{dx}^2 / 4m_e^*$, the expectation of the ground-state radius for the

1QD device in Fig. 4.7 is calculated to be around 12 nm. The transition from the diamagnetic energy shift region at low field to Zeeman energy shift at high field region has been observed for devices containing single and double QDs (Fig. 4.7(a), Fig. 4.8(a) and (d)). In addition, this transition does not show up for the reference devices, indicating the diamagnetic energy shift occurs through the states confined around the QD. The lever-arm ratio and the ground-state expectation radius of the confined electrons are listed in Table 4.1. The lever-arm ratio values for all of the three configurations are close, indicating the electrodes deposition is uniform for all the devices on the device chip. Also, the ground-state expectation values are close, demonstrating that the electronic structures of the quantum dots are not affected much by the dot configuration.

The replica of the primary tunneling peaks (see the eye guide in Fig. 4.7(a)) indicates the adding of a second electron to the BLS. Thus, the charging energy can be calculated from the

voltage difference between the primary and secondary tunneling peaks. The voltage peak difference remains nearly constant at different magnetic fields. This fact implies that the energy levels in the apex and the base are shifted by nearly the same amount by magnetic field. The adding energy is denoted by ΔE_D in Fig. 4.7(a). The summary of the lever-arm ratio, the ground-state expectation radius, and the adding energy of a second electron different QD patterns are listed in Table 4.1.

Dot configuration	1-dot	2-dot	2-dot
Spacing (nm)	/	22	90
Lever-arm ratio	2.6×10^{-5}	2.6×10^{-5}	2.4×10^{-5}
a_{dx} (nm)	12	11	11
Adding Energy (μeV)	250	250	200

Table 4.1 Magnetotransport characterization of QD/QDM devices. The lever-arm ratio, the expectation value of the ground state radius and the adding energy for the QD/QDM are listed for 1QD, 2QD-22 nm and 2QD-90 nm devices.

From the analysis results shown in Table 4.1, the lever-arm ratio values for all of the three configurations are close, indicating that the electrodes deposition is uniform to all the devices on the device chip. In addition, the expectation values of the ground state radius approximately equal, implying that the electronic structures of individual QDs are not obviously

affected by dot configurations. Therefore the conclusion can be made that the fabrication process is uniform from device to device.

4.6 INTERDOT INTERACTIONS

4.6.1 Coulomb interaction

The occupation of an electron at the first QD increases the energy level of the lowest bound state at the second QD. Thus a higher adding energy is required for another electron to tunnel to the second dot. When the bias increases, the electron overcomes the Coulomb repulsion energy from the electron hosted in the base. Thus the transition from the shallow to the primary resonant tunneling peak offers the magnitude of the interdot Coulomb interaction.

By comparing the two dot charging energy of the 22 nm (250 μeV) and 90 nm (200 μeV) spacing configuration, adding the second electron to the base requires higher energy for the 22 nm device. This difference is attributed to the Coulomb repulsion energy difference from the existing first electron in the base: The two confined electrons are localized at the Si surrounding the base of the SiC nanodots and the electron wave function expectation values for both of the configuration are around 16 nm. Thus, the strength of the interdot Coulomb repulsion energy decreases with the distance between two dots, as expected. Also, the interaction strength is comparable to the Zeeman spin splitting energy ($\sim 100 \mu\text{eV}$ at 1 Tesla), providing a possibility to fabricate spintronic bandgap materials. More complex QDMs with more than two dots have

been successfully grown, however considerably more elaborate analysis is required to fully understand the single particle features observed.

A simplified simulation model for the interdot Coulomb interaction can be built as following. The two confined electrons are localized at the base annulus region surrounding the SiC nanodots and the electron wave function expectation values for both of the configuration are around 12 nm. Thus, the strength of the interdot Coulomb repulsion energy depends only on the distance between two dots. The Coulomb interaction between dot A and dot B with dot spacing r is given by:

$$U_{AB}(r) = e^2 \int d\mathbf{r}_A \int d\mathbf{r}_B \frac{|\psi_A(\mathbf{r}_A)|^2 |\psi_B(\mathbf{r}_B)|^2}{|\mathbf{r}_A - \mathbf{r}_B|} \dots \quad (4.11)$$

The closer dot configuration gives larger Coulomb interaction. From table 4.1, it can be concluded that: $U_{AB}(22\text{nm}) - U_{AB}(90\text{nm}) \approx 50 \mu\text{eV}$.

The dependence of the Coulomb interaction on dot spacing provides the possibility of fabricating QD arrays in which the interdot Coulomb interaction can be tuned geometrically. These arrays are capable of implementing the AQS architectures to simulate the 2D Hubbard model as proposed in section 1.2.

4.6.2 Exchange interaction

The exchange interaction alters the expectation value of the energy levels in a QD when the wave functions of two or more electrons overlap. Generally, the electron-electron interaction can be described by an exchange Hamiltonian [225, 226]:

$$H_{ex} = \sum_{i,j} J_{ij} \overline{S_i} \overline{S_j}, \quad (4.12)$$

where \vec{S}_i is the spin operator for electron i , and J_{ij} is the exchange coupling constant between spin i and j . The exchange coupling is given by the exchange integral:

$$J_{ij} = e^2 \int d\mathbf{r}_1 \int d\mathbf{r}_2 \frac{\psi_i^*(\mathbf{r}_1)\psi_j(\mathbf{r}_1)\psi_j^*(\mathbf{r}_2)\psi_i(\mathbf{r}_2)}{|\mathbf{r}_1 - \mathbf{r}_2|}, \quad (4.13)$$

in which $\psi_i(\mathbf{r}_1)$ represents the wavefunction of electron i

In double-QD molecular case, the Hamiltonian is written specifically for dot A and B with dot spacing r as:

$$H_{ex}(r)_{AB} = J_{AB}(r)\vec{S}_A\vec{S}_B, \quad (4.13)$$

where

$$J_{AB}(r) = e^2 \int d\mathbf{r}_A \int d\mathbf{r}_B \frac{\psi_A^*(\mathbf{r}_A)\psi_j(\mathbf{r}_B)\psi_j^*(\mathbf{r}_B)\psi_i(\mathbf{r}_A)}{|\mathbf{r}_A - \mathbf{r}_B|}, \quad (4.13)$$

The average ground state wave function expectation is given in section 4.5, however, without the detailed information of the wave function profile, exchange coupling constant is not accessible. Therefore in this research, the exchange interaction has not be explored.

5 SUMMARY AND CONCLUSION

In this research, directed self-assembly sub-10 nm Ge/SiC/Si QDs have been fabricated with an optimized templated growth technique. The size distribution analysis of nanodot arrays by AFM and SEM shows a high degree of uniformity (51% of Ge/SiC QDs have FWHM ≤ 10 nm and 95% are ≤ 15 nm). In addition, the seeding of individual QDs within 2 nm position precision has been achieved. TEM characterization of the fabricated QDs shows that SiC nanodots form at pre-patterned sites. The Ge wetting layer at the interface of Si capping and substrate layer is repelled from the SiC nanodots, forming an annular lowered band gap region in the Si surrounding the SiC dots. Electrons are weakly confined in this annulus. The fabrication process developed in this dissertation study provides a deterministic and scalable method to implement an extensive class of QD-based architectures.

QD and QDM devices are fabricated by integrating various QD patterns into vertical transport structures. These devices are characterized with low-temperature magnetotransport by sweeping a dc bias applied to the collector gate and measuring the current from the emitter gate in varying magnetic fields.

Based on the analysis on the transport data, the QD/QDM device is identified as a triple-barrier resonant-tunneling (TBRT) structure: electrons resonantly tunnel from the emitter gate via the confinement states at the base and the apex of the QD, to the top gate. In magnetic fields, both the diamagnetic and Zeeman energy shifts are observed, allowing the QD orbital radius to be characterized. The ground-state radius expectation value of the single-QD device is close to that of the double-QD devices, indicating high uniformity of the QD device structures. The dependence of the interdot Coulomb interaction on the dot spacing has also been explored for double-QD systems.

The knowledge obtained from the magnetotransport is necessary to manipulate the electron charge and spin states confined by Ge/SiC/Si QDs. With the demonstrated ability to control the spatial positioning of electronically active QDs in nanometer scale, an enabling technology for new device paradigms has been provided for future application such as quantum computation and quantum simulation.

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