Electronic transport in silicon nanocrystals and nanochains

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Si nanocrystals and nanochains, prepared by material synthesis, provide a means to define nanoscale devices using growth rather than lithographic techniques. Electronic transport in thin films of Si nanocrystals is influenced strongly by single-electron charging and quantum-confinement effects, and by the grain boundary regions between nanocrystals. This paper reviews electronic transport mechanisms in Si nanocrystal materials. These include thermionic emission of electrons across grain boundaries, space charge limited current, hopping transport, and single-electron charging effects. The fabrication of single-electron devices in Si nanocrystal thin films and nanochains is considered, particularly with regards to their operation at room-temperature.

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1. Introduction:

In recent years, there has been great interest in Si nanocrystals prepared by various growth techniques [1-14]. The nanometre-size of these crystals leads to novel electronic and optical properties, associated with single-electron charging and quantum-confinement effects, with the nature of the nanocrystal surface, and with the interface or 'grain boundary' (GB) regions in thin films of nanocrystals. These properties may be exploited for the fabrication of light emitting devices in silicon (For a review, see Ref. [14]), nanoscale electronic devices such as single-electron transistors (SETs), quantum-dot transistors, and single-electron memory [7, 9, 15], and in electron emission devices [16]. Grown Si nanocrystals provide a means to define precisely whole, or parts of, a nanoscale device using 'bottom-up' material synthesis techniques rather than high-resolution lithography. Furthermore, it is possible to control precisely the nanocrystal growth process, leading to nanocrystals with similar size and separation [4, 13, 17]. This raises the possibility of the fabrication of large numbers of nanocrystal devices, with well-defined electrical and optical characteristics.

Si nanocrystals form one particular type within a wide range of semiconductor nanocrystal systems. A system where nanocrystals are embedded within a matrix material may be regarded as a nanocomposite material. Various semiconductor-based nanocomposites have been prepared, e.g. Si, Ge, CdSe, PbSe, or ZnO nanocrystals dispersed in various matrixes, e.g. SiO_2, Si_3N_4, or polymer-based insulating matrixes [17–23]. Nanocomposite materials where Si nanocrystals lie within a SiO_2 matrix are fully-compatible with large-scale integrated (LSI) circuit fabrication processes, and are of particular interest for highly-scaled and multi-functional integrated circuit applications.

We now briefly consider nanoscale devices for LSI circuit applications. The scaling of LSI devices to nanometre sizes has led to large increases in the speed, storage capacity, and functionality of LSI circuits. However, increases in the speed and number of transistors in LSI circuits results in sharp rises in the total power consumption of the chip, and complex circuit-level solutions are necessary to manage this [24]. Ultimately, this trend may limit further increases in the number of transistors on the chip. A reduction in the number of electrons necessary to define the information 'bits' in LSI circuits would lead automatically to smaller operating currents and reduced power consumption. However, this is difficult to achieve in conventional MOS devices, due to problems in sensing small amounts of charge, fluctuations in the value of the charge, and leakage of the stored charge.

Single-electron devices use the 'Coulomb blockade' effect to control charge on nanoscale conducting dots or 'islands', isolated by tunnel barriers, with one-electron precision [25-28]. These devices are inherently low-power, highly-scalable and immune from statistical '$\sqrt{n}$' fluctuations in the charge [9, 25]. However, the practical application of single-electron devices requires room-temperature operation and the fabrication of islands ~10 nm or less in size [9]. A recent, detailed, review of single-electron devices in silicon, including devices operating at room temperature, is provided by Takahashi *et al* [29]. Single-electron devices also tend to be very sensitive to the size and shape of the islands and tunnel barriers. Therefore, in order to maintain reproducibility in the electrical characteristics of different devices in the LSI circuit, it is necessary to control the device morphology at the nanoscale over large areas of the circuit. Si nanocrystal and nanocomposite materials provide a means to do this using well-controlled growth techniques rather than complex high-resolution lithography.

This article reviews the electronic transport characteristics of Si nanocrystals materials, and the fabrication of single-electron and quantum-dot transistors in these materials. We consider first the preparation of Si nanocrystal materials by various techniques. We then discuss electronic transport in continuous nanocrystalline Si (nc-Si) films, i.e. polycrystalline Si films where the grains are only ~10 nm in size. This is followed by a discussion of conduction mechanisms in thin, deposited films of discrete Si nanocrystals, with an emphasis on space charge limited current (SCLC) and hopping transport mechanisms. Single-electron and quantum-dot devices in Si nanocrystal materials are considered next. Finally, we discuss one-dimensional (1-D) 'nanochains' of discrete Si nanocrystals, where the electrical characteristics are dominated by room temperature single-electron charging effects.

2. Material preparation:

A variety of growth techniques have been used to prepare Si nanocrystal thin films, driven in particular by the possibility of Si light emission devices. These techniques include the ion implantation of Si into SiO_2 films [30-39], deposition of thin films of Si nanocrystals by sputtering [1, 40, 41], plasma enhanced chemical vapour deposition (PECVD) or low pressure chemical vapour deposition (LPCVD) techniques [6, 8-1, 42-44], and aerosol deposition of Si nanocrystals [2, 3, 45]. Optimisation of these various processes can allow control over the size and shape of the nanocrystals. Other techniques include the controlled growth of nanocrystals in the gas phase using a VHF pulsed plasma, followed by deposition on to a suitable substrate [4, 5]. This leads to good control over the nanocrystal size and separation. Si nanocrystal films may also be prepared by the crystallisation or phase separation of amorphous Si layers within a superlattice formed by thin layers of amorphous Si and SiO_2 [12, 13]. The superlattice may be grown by PECVD or MBE techniques [46-49],

magnetron sputtering [47, 50], or evaporation of SiO_x powder [13, 51, 52]. These processes can lead to nanocrystals with controlled size, separation and position [13]. A review of Si nanocrystal growth techniques may be found in Ref. [14]. In the following, we discuss briefly Si nanocrystal materials used in the fabrication of nanoscale electronic devices such as SETs, and in investigations of the electronic transport mechanism in nanocrystals.

We consider first nc-Si films prepared by PECVD, using the work of Kamiya *et al* [10, 11] as an example. Kamiya *et al* have prepared nc-Si films using 100 MHz PECVD at 300 °C, from a $SiF_4/H_2/SiH_4$ gas mixture. The SiF_4/H_2 mixture helped to create a high-crystallinity film even at the beginning of the growth process by suppressing thin amorphous Si 'incubation' layers usually formed in the initial stages. A $SiF_4/H_2/SiH_4$ gas flow rate of 30/40/0.25 sccm and a growth temperature of 300°C was used to obtain films ~10 nm thick, where the grains were < 10 nm in size and the crystalline volume fraction was >60 %. For device applications, the films were heavily doped *n*-type with phosphorous during growth, using PH_3. For films thickness from ~10 nm to ~1 μm, the crystalline volume fraction varied from ~60% to close to 100%. Figure 1(a) shows a transmission electron micrograph of a 30 nm thick film, where the grain size is 4 nm – 8 nm [22]. The grains are isolated from each other by amorphous Si grain boundaries (GBs). We shall see in Sec. 5 that such a film is well-suited for the fabrication of room-temperature SETs [53].

In the limit of very small film thickness of the order of a few nanometres, a continuous nc-Si film becomes discontinuous, forming a layer of discrete Si nanocrystals. Yano *et al* [6, 9] have prepared such a film by thermally crystallising an ultra-thin amorphous Si layer at 750°C. The amorphous Si layer (3.4 nm average thickness) was deposited at 520°C using LPCVD. After crystallisation, the films consisted of Si nanocrystals similar in size to the film

thickness, isolated by gaps in the film. These films have been used by Yano *et al* as the basis of LSI few-electron memory circuits [9].

In comparison with CVD processes, more advanced VHF pulsed-plasma techniques may be used to control the size and shape of the nanocrystals [4, 5, 54]. Spherical Si nanocrystals may be grown in a VHF plasma cell from SiH_4, by coalescence of radicals produced from the SiH_4. The nanocrystals can then be removed from the plasma cell into a UHV chamber and deposited on to a suitable substrate. Figure 1(b) shows an SEM image of a ~300 nm thick film of Si nanocrystals where the Si core diameter is ~8 nm, deposited on a Si substrate. The nanocrystal size can be controlled precisely by optimising the gas flow rate, pressure, VHF power and dilution conditions. It is possible to control the nanocrystal size distribution with great accuracy using this method, e.g. for nanocrystals with an average size of 8 nm, the size variation can be as small as ±1 nm. The nanocrystals may be oxidised after deposition to reduce the Si core diameter. This process is self-limiting, with stress at the silicon/oxide interface ultimately preventing reduction of the nanocrystal Si core diameter. The well-controlled size of these nanocrystals makes them of particular interest in investigations of electron transport process in nanocomposite systems [55, 56].

3. Conduction in continuous nanocrystalline Si films:

The conduction mechanism in continuous nc-Si or polycrystalline Si thin films, ignoring the influence of charging and quantum-confinement effects on the grains, is influenced strongly by potential barriers at the GBs. 'Schottky-like' potential barriers may be formed at the GBs, created by the electric field associated with free carriers trapped in the large numbers of defect states at the GBs [57-60]. The process also reduces the carrier density

within the grains. Furthermore, segregation of dopant atoms at the GBs can reduce the effective carrier density in the grains even further [59, 61, 62]. A detailed review of conduction mechanism in polycrystalline Si films, with regards to the characteristics of thin film transistors (TFTs) in these materials, is provided by Brotherton [63].

Consider a 1-D chain of *n*-type nc-Si grains (Fig. 2), where the GB thickness is small relative to the grain size 'D'. We now assume a uniform donor concentration N_d (per unit volume) in the grain (Fig. 2(a)), and GB traps with a density N_t (per unit area) at an energy E_t with respect to the intrinsic Fermi level E_i. The value of E_t lies within the bandgap in the GB (Fig. 2(c)). N_t can be ~10^{11} – 10^{12} /cm^2 in large-grain polycrystalline Si films [60, 64]. Electrons trapped at the GBs leave ionised donors in the grains (Fig. 2(b)). For low doping levels, all the dopant electrons in the grain are trapped in the GBs and the grain is fully depleted. The trapped charge/ionised dopants form a Schottky-like potential barrier of height E_{GB} (Fig. 2(c)). If N_d is increased, more charge is trapped at the GB, increasing the electric field and potential barrier height until at $N_d = N_d^* \approx N_t / D$, the conduction band in the centre of the grain lies near the Fermi energy E_F. Free carriers can now exist in the grain and E_{GB} is at its maximum value. Any further increase in N_d reduces E_{GB}. Furthermore, any variation in the values of D, N_t, and N_d from grain to grain leads to a distribution of GB barrier heights and widths across the film [65].

Electron transport across the GBs occurs by thermionic emission. For fully depleted grains, $N_d < N_d^*$, and the conductivity σ has the form [59, 60]:

$$\sigma = \frac{e^2 D^2 N_c N_d v}{2k_B T(N_t - DN_d)} \exp\left(-\frac{0.5E_{GB} - E_t}{k_B T}\right) \qquad (1)$$

Here N_c is the effective conduction band density of states, $v = (k_B T/2\pi m^*)^{1/2}$ is a thermal 'collection' velocity with electron effective mass m^*, E_G is the band gap, and k_B is Boltzmann's constant.

For partially depleted grains, $N_d > N_d^*$, the conductivity has the form [60]:

$$\sigma = \frac{e^2 D n_o v}{k_B T} \exp\left(- \frac{E_{GB}}{k_B T} \right) \qquad (2)$$

Here n_0 is the concentration of free carriers in the grain and $E_{GB} \approx e^2 N_t^2 / 8\varepsilon N_d$, where ε is the permittivity of the semiconductor (here, polycrystalline Si).

Equations 1-2 give the thermionic emission current across the GB and predict a linear Arrhenius plot, ln(σ) v.s. $1/T$ (Fig. 2(d)). The conduction mechanism may be assisted by tunnelling via defect states within the barrier. As the temperature is reduced, the thermionic emission current falls and tunnelling effects begin to dominate, leading to a comparatively temperature-independent section of the Arrhenius plot (below temperature T_1 in Fig. 2(d)). The slope of the temperature dependent section of the plot may be used to extract the activation energy, here a measure of the barrier height E_{GB}. At low temperatures, variable range hopping transport may also occur [66]. In addition, any variation in the barrier heights and widths across the film can result in a network of current percolation paths across the film [65, 66], along low resistance paths through GBs with low potential barriers.

Carrier scattering occurs at the GB potential barriers, lowering the carrier mobility of an nc-Si film. The grains in nc-Si films are only ~10 – 50 nm in size, much smaller than in polycrystalline Si films (~1 μm or greater) [63]. The greater density of GBs in nc-Si compared to polycrystalline Si may then lower the mobility further. It is, however, possible to observe high carrier mobility in nc-Si TFTs, comparable to poly-Si TFTs [63]. In recent work, very high field-effect mobility values for electrons, $\mu_{e,FE}$ ~450 cm^2/V.s and for holes, $\mu_{h,FE}$ ~100 cm^2/V.s, were observed in devices fabricated in high-quality nc-Si films [67]. This was attributed to low oxygen content in the films, causing a reduction in GB trapping states with energies corresponding to the bandgap in the grains. This reduced GB carrier trapping and hence E_{GB} (Fig. 2(c)). The values of mobility in these devices were comparable to high quality poly-Si TFTs, where $\mu_{e,FE}$ ~300 – 566 cm^2/V.s and $\mu_{h,FE}$ ~200 cm^2/V.s has been reported [68-71].

The thermionic emission model may be sufficient if the grain size and associated capacitance C are large. However, as the grain size is reduced to the nanometre scale, single-electron charging effects [26, 27] begin to influence the conduction process. At temperatures where electron transport occurs by tunnelling through the GB potential barriers, the nc-Si film forms an array of nanoscale tunnel capacitors and can show single-electron effects. In a grain isolated by two tunnel barriers of capacitance C_1 and C_2 (Fig. 3(a)), the energy associated with the addition of a single electron to the grain is given by [26]:

$$E_c = \frac{e^2}{2C} \tag{3}$$

Here $C = C_1 + C_2$ is the total capacitance of the grain and e is the electronic charge. If $C \sim 10^{-15}$ F then $E_c \sim 80$ μeV, which is greater than the thermal energy k_BT only at cryogenic temperatures. If $E_{GB} >> k_BT$, and the GB tunnelling resistance $R_{GB} > R_Q = h/e^2 \sim 22.5$ kΩ, then at cryogenic temperatures, electrons are quasi-localised on the grains and the addition of even one electron onto the grain requires that E_c is overcome [26, 27]. This leads to the well-known 'Coulomb blockade' of conduction in the I_{ds}-V_{ds} characteristics across the grain (Fig. 3(b)), where current flow is suppressed within a region V_{cg} where V_{ds} is not enough to overcome E_c. If the tunnelling rates through the two barriers are very different, then a series of current steps, the 'Coulomb staircase', occurs in the I_{ds}-V_{ds} characteristics (Fig. 3(b))). In contrast, if the tunnelling rates are similar, then the current increases linearly outside the Coulomb gap. Each step corresponds to the charging of the grain with an additional electron. Adding a gate electrode (Fig. 3(c)), coupled to the grain by a capacitance C_g, forms the single-electron transistor (SET). Sweeping the gate voltage leads to single-electron current oscillations in the drain current, with a period e/C_g (Fig. 3(d)). Each oscillation corresponds to the charging of the grain with an additional electron.

If the grains are ~10 nm in size, then it is possible for C~1 aF such that $E_c > k_BT$ ~26 meV at room temperature. In crystalline Si materials, techniques such as controlled oxidation and/or etching processes, combined with high-resolution electron-beam lithography, have been used to define islands of this scale [72-75]. In contrast, the grains in nc-Si films 'naturally' form islands ~10 nm in size [53]. Furthermore, discrete electron energy levels caused by quantum-confinement of electron by the GB tunnel barriers may exist on the grain, creating a quantum-dot [76, 77]. Figure 4 plots the single-electron charging energy $E_c = e^2/2C$ and the quantum-confinement energy [20] $E_k \sim \frac{\pi^2 \hbar^2}{2m^*(D/2)^2}$ for an isolated spherical grain

imbedded in SiO_2, of diameter D, electron effective mass m^* and self capacitance $C = 2\pi\varepsilon_r\varepsilon_0 D$. It is seen that both E_k and E_c are ~k_BT at room temperature for D ~10 nm, and that in particular, E_k increases rapidly with reducing D. In large numbers of nanocrystals, variations in the grain size and the GB tunnel barriers may smear-out these effects. Furthermore, percolation conduction through the lowest resistance transport paths may occur in large numbers of nanocrystals. This process may bypass grains with large single-electron energy or high GB tunnel barriers [78, 79]. Therefore, single-electron devices in nc-Si usually require a reduction in the number of current paths, e.g. by defining nanowires or 'point-contacts' (a short nanowire where the length ~ width).

4. Conduction in discrete Si nanocrystal films:

The macroscopic conduction mechanism in thin films of discrete semiconductor nanocrystals varies strongly as function of temperature. Space-charge limited currents [80] (SCLC), tunnelling currents, percolation hopping, and single-electron effects [20, 55, 56, 81, 82] have all been observed in a range of semiconductor nanocrystal films. In Si nanocrystals prepared by pulsed laser ablation, SCLC and tunnelling conduction mechanisms have been suggested [81]. A SCLC mechanism is also observed in many investigation of porous Si films [83] (which can also contain Si nanocrystals [84]), and in other semiconductor nanocrystal films [85, 86]. At high electric fields, it is possible to observe electron emission from thin Si nanocrystal films [87]. At lower temperatures, various hopping conduction mechanism are possible. Fujii *et al* [88], in ~2 nm Si clusters dispersed in SiO_2 films, have observed that the conductivity σ follows a $\ln(\sigma)$ v. s. $1/T^{1/4}$ temperature dependence from 120 K – 300 K. This was attributed to a Mott variable range hopping (M-VRH) mechanism. In thin films of ultra-small discrete Si nanocrystals ~3 nm in size, strong single-electron

effects occur even at room temperature [6, 9]. We will discuss single-electron effects in Si nanocrystals in Secs. 5-6.

We now consider investigations of the conduction mechanism in discrete Si nanocrystal films by Rafiq *et al* [55, 56], where the nanocrystal size and separation was relatively well-controlled. The films were 300 nm-thick, and formed by discrete, undoped ~8 nm diameter Si nanocrystals (Fig. 1(b)), prepared using plasma decomposition of SiH_4 [4, 5]. Different conduction mechanisms determined the *I-V* characteristics as the temperature was varied from 300 K to 30 K. From 300 K to ~200 K, conduction occurred through a SCLC transport mechanism, in the presence of an exponential distribution of trapping states [55]. The trap density was found to be similar to the nanocrystal number density, suggesting that the nanocrystals trapped single carriers, or at most a few carriers. From ~200 K – 30 K, the conductivity followed a $\ln(\sigma)$ v. s. $1/T^{1/2}$ dependence, attributable to a percolation hopping conductance mechanism [56].

I-V measurements were performed using Al/Si nanocrystal film/*p*-Si/Al 'mesa' structures, where current flow was vertically across the film. Devices with contact areas from 35 μm × 35 μm to 200 μm × 200 μm were defined by electron-beam lithography and reactive ion etching. The nanocrystals were undoped, with diameter 8 nm ± 1 nm and a thin (~1 – 2 nm) surface SiO_2 layer (Fig. 1(a)). The nanocrystal number density N_{nc} ~1.2×10^{18} /cm^3. Figure 5(a) shows a section of the forward bias (positive voltage applied to the substrate, magnitude above a threshold voltage ~1 V) *I-V* characteristics of a 35 μm × 35 μm diode at 280 K, 240 K, and 200 K, on a log-log plot [55]. For voltages below the threshold voltage, the characteristics (not shown here) are determined by rectifying contacts at the Al back contact, and/or at the *p*-Si substrate-Si nanocrystal interface. For applied voltage above the threshold

voltage (Fig. 5(a)) and for temperatures from 300 K – ~200 K, the data lie along straight lines, corresponding to a $I \propto V^m$ dependence. For this temperature range, m increases in value from 1.8 – 4. The increase in m leads to convergence of this section of the *I-V* characteristics, towards a 'cross-over' point V_c [89] (Fig. 5(a)). Below 200 K (not shown), the curves do not converge to V_c, instead appearing to converge towards a constant slope. An Arrhenius plot of σ (Fig. 5(b)) at 4 V bias in a similar device shows two distinct regimes. Above ~180 K, a single, steep slope is observed, (marked by the solid line). This is attributable to thermally activated transport across potential barriers along the conduction path, with activation energy ~200 meV. Below 180 K, the data can be fitted to a ln(σ) vs. $T^{1/2}$ dependence.

Rafiq *et al* [55] explained the characteristics from 300 K to ~200 K using a space charge limited current (SCLC) model with an exponential density of traps [80, 90]. Here, free carriers (in this case, holes) are injected from the substrate into transport states in the valence band in the nanocrystals. An exponential distribution of hole traps above these states reduces the number of free carriers. The total number of carriers available for transport varies with temperature and applied voltage, as the number of trapped carriers changes. Assuming constant mobility, an exponential trap distribution, and a free carrier concentration much less than the trapped carrier concentration, the SCLC current density J is given by [90]:

$$J = q^{1-l} \mu_p N_v \left(\frac{2l+1}{l+1} \right)^{l+1} \left(\frac{l}{l+1} \frac{\varepsilon_s \varepsilon_0}{N_t} \right)^l \frac{V^{l+1}}{d^{2l+1}} \qquad (4)$$

Here, N_t is the trap density, ε_0 the permittivity of free space, ε_s the dielectric constant, μ_p the hole mobility, N_v the density of transport states, d the sample thickness, and $l = T_t / T$, where T is the measurement temperature and T_t is the 'characteristic temperature'. T_t is a measure of the characteristic energy $E_t = k_B T_t$ of the trap distribution. Equation 4 predicts a J-V^m dependence, where $m=l+1$. Figure 5(a) shows J-V^m fits (solid lines) to the data, from

280 K to 200 K. The data converges to the cross-over point V_c and the slopes give the exponent m. The values of m may be used to extract T_t = 1670 K and E_t = 0.14 eV. Kumar *et al* [89] have shown that the cross-over point V_c is given by:

$$V_c = \frac{qN_t d^2}{2\varepsilon_s \varepsilon_0} \quad (5)$$

In Fig. 5(a), V_c = 17 V, which gave $N_t = 2.3\times10^{17}$ cm^{-3} [55]. This value of N_t was very similar to the nanocrystal number density, N_{nc} ~1.2×10^{18} cm^{-3}, implying that only a few carriers were trapped per nanocrystal. Rafiq *et al* [55] suggested that single-electron effects or the existence of only a few trapping states in the nanocrystal/SiO_2 shell limited the number of carriers trapped per nanocrystal.

The experimental values of T_t = 1670 K and $N_t = 2.3\times10^{17}$ cm^{-3} may be compared to those in amorphous Si, and in other nanocrystal systems. In bulk or nanoparticle amorphous Si, T_t is very different (T_t ~300 K – 1300 K) and N_t is two orders of magnitude larger [91]. However, comparable values (T_t ~1750 K and N_t ~ 10^{16} – 10^{17}cm^{-3}) have been observed in CdSe nanocrystals of similar size [85].

We now consider the temperature range from ~200 K – 35 K in these Si nanocrystal devices. In this range, the curves tend to a constant m and the SCLC model does not fit. This is because the thermal energy is not sufficient to ionise carriers between the traps and the transport states. Carrier transport at these temperatures occurs by hopping conduction [56]. Figure 6 shows a ln(σ) vs. $1/T^{1/2}$ plot at 4 V, from 35 K to 200 K, where the data follows a straight line. For higher applied bias, the slope of the hopping temperature dependence can be reduced due to an increasing field effect [92]. The ln(σ) vs. $1/T^{1/2}$ dependence gives:

$$\sigma \propto \exp\left[-\left(\frac{T_0}{T}\right)^{\frac{1}{2}}\right] \qquad (6)$$

where T_0 is a constant of the material. This behaviour, observed in metal-insulator nanocomposite films [93, 94] and in amorphous or doped semiconductor materials [66, 95], may be explained by the percolation hopping transport model of Šimánek [93] or by an Efros and Shklovskii variable range hopping (ES-VRH) model [95].

The percolation hopping transport model considers thermally activated carrier tunnelling between adjacent nanocrystals and has been used to explain the conductivity over a wide temperature range in Ge nanocrystals, embedded in SiO_2 [20]. This model considers the activation energy E_a for hopping to be associated with the difference between the energies of the first electron levels E_1 on neighbouring nanocrystals. Here, $E_1 = E_c + E_d$, where E_c is the single-electron charging energy and E_d is the quantum-confinement energy. Variation in the nanocrystal separation s and diameter d lead to variation in E_1 and therefore in E_a. As the resistance between the nanocrystals varies strongly with E_a, the nanocrystal film may be modelled as a three-dimensional random resistor network, described by a critical percolation conductance. Šimánek has used this to derive Eq. 6, with T_0 given by [93]:

$$T_0 = \frac{2P_c s_{\max} E_{a,\max}}{k_B \alpha} \qquad (7)$$

Here, P_c is the percolation threshold [96], s_{max} is the maximum particle separation, $E_{a,max}$ is the maximum value of the activation energy (given by the largest value of E_1 in the film minus the smallest value of E_1) and α is the carrier wave function decay length in the insulating matrix. Rafiq *et al* calculated $T_0 \approx 1.15 \times 10^4$ K for their Si nanocrystal films (Fig. 1(b)), using $s_{max} \approx 3$ nm, variation in d from 7 nm – 9 nm, and approximating $P_c = 0.25$, the

average value for a range of typical lattices (P_c varies from 0.12 – 0.39) calculated by Ziman [96]. This was in good agreement with the experimental value, $T_0 = 1.23 \times 10^4$ K.

We now discuss the ES-VRH model. This model considers the contribution of the Coulomb interactions associated with electron-hole pairs created during the hopping process, implying that E_a is proportional to $1/r$, where r is the hopping length. The model also predicts a temperature-dependence similar to Eq. 6, with T_o given by [95]:

$$T_0 = \frac{2.8e^2}{4\pi\varepsilon\varepsilon_0 k_B \alpha} \quad (8)$$

Rafiq *et al* [56] have estimated $T_0 = 1.18 \times 10^5$ K for their films, an order of magnitude larger than the experimental value. The ES-VRH model also predicts a critical temperature $T_c = \frac{e^4 g_0 \alpha}{k_B (4\pi\varepsilon\varepsilon_0)^2}$, where g_0 is the density of states. Above T_c, Coulomb interactions may be neglected and a transition to a Mott variable range hopping [66] process occurs. Rafiq *et al* estimated that $T_c \approx 6$ K, far lower than the ~200 K maximum temperature of their dependence (Fig. 6). The percolation hopping model appears to explain the low temperature (<200 K) conduction mechanism in the system of Rafiq *et al* better than an ES-VRH mechanism.

The hopping parameters in the Si nanocrystal films may be compared to those extracted for Ge and CdSe nanocrystal films [20, 97]. Fujii *et al* [20] have used the percolation hopping model to describe the conduction in ~9 nm Ge nanocrystals in SiO_2 films. They observed a $\ln(\sigma)$ vs. $1/T^{1/2}$ dependence up to 300 K, with $T_0 = 1.08 \times 10^5$ K. This compared well with the theoretical value of T_0 using the percolation hopping model. In contrast, Yu *et al* [97] have used an ES-VRH model to explain a $\ln(\sigma)$ vs. $1/T^{1/2}$ dependence in ~5 nm CdSe crystals in

solution, with $T_0 = 6.2 \times 10^3$ K. Here, T_c ~400 K for the ES-VRH process, far higher than in the Si nanocrystal system of Rafiq *et al* [56].

5. Single-electron effects in nanocrystalline silicon films:

Nanocrystalline Si films provide a means to fabricate single-electron devices with islands ~10 nm in diameter, where the capacitance is ~1 aF. At these scales, single-electron charging effects can occur even at room temperature, and it becomes possible to fabricate room-temperature SET [53] and single-electron memory devices [9]. A 'nanowire' channel region defined in a nc-Si film forces current to flow through a series of nanoscale grains. The *I-V* characteristics are then dominated by single-electron charging of nc-Si grains isolated by GB tunnel barriers. In the following, we discuss work on SETs in nc-Si films. We consider single-electron effects in 'nanochains' of discrete Si nanocrystals prepared by growth techniques in Sec. 6.

Nanocrystalline Si SETs can be defined using nanowires ~50 nm or less in width, fabricated in nc-Si films ~50 nm or less in thickness, deposited on SiO_2-on-Si substrates. The nanowire current can be gated using a variety of techniques, e.g. using trench-isolated side-gates, deposited polycrystalline Si or metal top-gates, or using the back-gate formed by the Si substrate. We consider first SETs using nanowires with lateral side-gates defined by trench-isolation [98, 99]. Figure 7 shows a TEM image of this type of device. The nanowire is ~400 nm long and ~50 nm wide. The device was fabricated in 50 nm-thick heavily-doped (*n*-type, 5×10^{19} cm^{-3}) polycrystalline silicon material, prepared using plasma enhanced chemical vapour deposition (PECVD). The grain size in the film varied from ~20 nm – 100 nm in size. The device was fabricated by electron-beam lithography and reactive-ion-etching in

$SiCl_4/CF_4$ plasma, and then oxidised to reduce the Si nanowire cross-section and passivate surface states. Figure 8(a) shows the drain-source I_{ds}-V_{ds} characteristics of a device with a ~1 μm × ~40 nm nanowire at 4.2 K, as V_{gs} is varied from 0 – 5.2 V. A Coulomb gap of width ~7 mV is seen at V_{gs} = 0 V. As V_{gs} is increased to 5.2 V, the Coulomb gap is periodically overcome, leading to an increased current within the gap, e.g. at V_{gs} = 0.4 V (second curve from the bottom). Figure 8(b) shows single-electron current oscillations in the I_{ds}-V_{gs} characteristics in a similar device at 4.2 K, with a period ΔV_{gs} ~1 V. The oscillations correspond to the addition of electrons one-by-one to a dominant charging grain. The period corresponds to a gate capacitance $C_g = e/\Delta V_{gs}$ = 0.16 aF. The single-electron current oscillations in these devices may be complex, due to multiple periods associated with the formation of a multiple-tunnel junction (MTJ) along the nanowire. The device of Fig. 8(b) had a rather low maximum operating temperature of ~15 K, due to the comparatively large grain size and the low GB tunnel barrier height.

The doping concentration in nanowire SETs can effect the formation of the tunnel barriers in these devices. Fluctuations in the doping concentration at the local level may lead to depleted regions along a nanowire, forming tunnel barriers at least at low temperature. This behaviour has been identified experimentally in crystalline Si nanowires by Altebaeumer and Ahmed [100], using nanowires doped *n*-type at 2×10^{19} cm^{-3}. Here, a pattern-dependent oxidation effect was believed to form tunnel barriers at the ends of the nanowire. However, as a function of gate voltage, the single-electron current oscillations showed a transition from a single island to a double island system. This was attributed to fluctuation in the potential along the length of the nanowire, which introduced an additional tunnel barrier for part of the gate voltage range. The fluctuations in potential were attributed to fluctuations in the doping concentration along the nanowire. The effect of potential fluctuations in nanowire SETs, and

the transition from a single dot to a MTJ, has also been investigated theoretically [101, 102]. Furthermore, for very high doping concentrations ~5×10^{20} cm^{-3}, Tilke *et al* [103] have observed very regular, quasi-metallic single-electron oscillations in crystalline Si nanowire SETs. Here, dopant segregation effects may also cause fluctuations in the doping density along the nanowire.

Tan *et al* [104] have fabricated 'point-contact' SETs in ~30 nm thick nc-Si films where the grain size was much smaller, ~4–8 nm. The GBs in these films as-deposited were thin ~1 nm amorphous Si tissues. The film was heavily-doped *n*-type, with a room temperature carrier concentration of 3×10^{20} $/cm^3$. These devices used nanowires with both length and width reduced to below ~50 nm, forming a point contact. Only a few grains lay within the active area of the device, improving the electrical characteristics. For devices fabricated in the nc-Si film as-deposited, the Coulomb gap was 40 mV and single-electron effects persisted up to ~60 K. Here, the operating temperature was limited not by the grain size but by the GB potential barrier height and tunnel resistance. The low operating temperature in these SETs, even though the grain size was small enough for higher temperature operation, was attributed to low GB barriers. The maximum barrier height was only ~40 meV, measured using Arrhenius plots of the device conductance. This value was not high enough, relative to k_BT ~26 meV at room temperature, to confine electrons at room temperature.

Selective oxidation of the GBs from amorphous silicon into SiO_x may be used to raise the operating temperature of point-contact SETs to room temperature [53, 105, 106]. Oxidation at 750°C, followed by high-temperature annealing at 1000°C, selectively oxidises the GBs, raising the GB potential barrier height to ~170 meV ~$7k_BT$ at room temperature [53]. This process relies on the higher rate of diffusion of oxygen atoms into GB defect states at lower

temperatures, compared to the diffusion rate into the crystalline silicon grains. Single-electron current oscillations may be observed at 300 K in such a device, associated with a single dominant charging island [53]. While the oscillations persist up to 300 K with an unchanged period, there is usually a fall in the peak-valley ratio as the temperature increases, due to a thermally activated increase in the tunnelling probability.

Control of the GB barrier height strongly effects conduction in a nc-Si film. For single-electron devices, high GB barriers confine electrons on the grains at higher temperatures, essential for room temperature SETs. By contrast, reduction of the GB potential barrier helps to reduce the film resistivity, improving the effective carrier mobility. This is of great interest in the fabrication of better thin-film transistors. Different 'GB engineering' processes address these requirements, e.g. oxidation and annealing processes may be used to modify the GB tunnel barrier. Oxidation at 650–750°C may oxidise the GBs selectively, subsequent annealing at 1000°C increasing the potential barrier height and resistance [107]. In contrast, hot H_2O-vapor annealing may reduce the GB barrier height by reducing the GB dangling bond density [108].

The nanowire and point-contact SETs discussed above were fabricated in continuous nc-Si films. In such a film, the GBs are narrow, and single-electron effects tend to be overcome thermally by a reduction the GB resistance. Single-electron charging may occur more easily at higher temperatures in films formed by a layer of discrete, separated Si nanocrystals. Here, higher potential barriers can exist between the grains and electrons may be localised more strongly. In one of the earliest demonstrations of a single-electron device operating at room temperature, Yano *et al* [6] fabricated SETs using nanowires defined in ultra-thin (~3 nm), nc-Si layers, where the layers were strongly granular and formed by discrete grains only

~1 nm in size. In a similar room temperature SET design, Choi *et al* [109] used a <30 nm long section of a thin, discontinuous, PECVD film with grains 8–10 nm in diameter. SETs with more precisely defined island have been fabricated using Si nanocrystals prepared by the plasma decomposition of SiH_4 [4, 5]. SETs using ~8 nm islands prepared by this technique have been used to fabricate SETs in a number of different configurations [110-114]. For example, planar devices may be defined in SOI material, where a few nanocrystals lie in a narrow ~30 nm gap between source and drain contacts and the current is controlled by a top gate supported on a deposited oxide layer [112]. An alternative approach is to deposit Si nanocrystals in a nanoscale hole etched in a silicon dioxide layer, and then top-fill the hole with polycrystalline silicon to form a contact to the nanocrystals [113].

We now consider the effect of quantum-confinement of electrons in nc-Si SETs. The presence of discrete energy levels within Si nanocrystals may be used to explain observations of light-emission from the nanocrystals [14]. Nanocrystalline Si grains where discrete energy levels exist, with energy spacing > k_BT, may be regarded as quantum-dots [76, 77]. A nc-Si SET formed by these grains would show resonant tunnelling peaks in the gate dependence of the drain-source current, with peak separation corresponding to the sum of the single-electron and quantum-confinement energy and peak height determined by the coupling of the electron wave function of the energy level with the contacts. Coupled quantum-dot behaviour is also possible, where electrostatic and electron wave function interactions occur between two or more quantum-dots [114, 115].

It is possible to investigate, at low temperatures, electronic interactions between two or more Si nanocrystals using nc-Si point-contact SETs of various channel widths. Varying the dimensions of the point-contact controls the number of nanocrystals taking part in the

transport process. Furthermore, the interaction of electrons on neighboring nanocrystals can be controlled by GB selective oxidation. Khalafalla *et al* [114, 115] have fabricated point-contacts ~30 nm × 30 nm × 40 nm in size, using ~40 nm-thick heavily-doped LPCVD films, with grain size from ~10 – 30 nm. Two side-gates were used to control the point-contact current. Only a few grains existed within the channel at most, and different grains contributed in varying degrees to the device conduction. If the device was oxidised at 650°C – 750°C, followed by annealing in argon at 1000°C, then this created a high and wide GB tunnel barrier (>100 meV). Electrostatic coupling effects were observed in such a device at 4.2 K [114]. If the device was oxidised only, without annealing, then the GB tunnel barriers remained low (~40 meV) and narrow and the grains were more strongly coupled. These devices showed both electrostatic and electron wavefunction coupling effects at 4.2 K [115]. If the dimensions of the point-contact were increased, more grains could influence the *I-V* characteristics. In conduction through a region formed by ~10 grains, it was possible to identify the presence of percolation paths across the nc-Si grains [116].

Finally, we comment briefly on Si nanocrystal non-volatile memory cells. There has been considerable interest in the development of few-electron memory cells using Si nanocrystals to store charge [7, 117-123]. These memory cells are analogues of non-volatile 'FLASH' memory cells, where the charge is stored on a 'floating-gate' formed by a discontinuous Si nanocrystal layer [7], or even a single nanocrystal [120], rather than on a continuous polycrystalline Si layer. Si nanocrystals may be sandwiched in the gate-stack of a silicon MOSFET [117], separated from the channel by a thin layer of oxide and from the top-gate electrode by an additional, thicker layer of oxide. Charge may be injected into the nanocrystals by direct tunnelling from the channel across the thin oxide, by application of a

voltage to the gate. This charge can be then be sensed as a threshold voltage shift of the MOSFET.

6. Single-electron effects in Si nanochains:

In recent years, there has been great interest in single crystal silicon nanowires (SiNWs) and ‘nanochains’ of Si nanocrystals prepared by growth techniques, for the ‘bottom-up’ fabrication of nanoscale electronic devices [124-126]. Single-crystal SiNWs, prepared by vapour-liquid-solid (VLS) growth [127, 128], or by thermal evaporation of solid sources [125], have been widely-investigated for the fabrication of nanoscale field-effect transistors and circuit application [126, 129, 130]. Less well investigated are Si nanochains, consisting of a one-dimensional (1-D) array of ~10 nm diameter Si nanocrystals separated by narrow SiO_2 regions, prepared by thermal evaporation of SiO_x [125]. Si nanochains ‘naturally’ form a series of nanoscale islands or quantum-dots (the Si nanocrystals) isolated by tunnel barriers (the SiO_x regions), providing a means to fabricate single-electron devices by growth techniques.

Single-electron transistors (SETs) have been fabricated in single crystal SiNWs formed by VLS growth [130], with a maximum operating temperature ~30 K. In these devices, the tunnel barriers were defined by lithographically-defined contacts to the SiNW. A ~100 – 400 nm SiNW section between the contacts behaved as a single quantum-dot, with capacitance C ~10 aF. Here, C was not small enough for room temperature single-electron effects. In contrast, in measurements of large bundles of nanochains and SiNWs [131], a Coulomb staircase current–voltage (*I-V*) characteristic was observed at room temperature, attributed to single-electron effects in nanocrystals within the bundle.

Rafiq *et al* [132] have observed strong single-electron effects at room temperature in devices using single Si nanochains, prepared by thermal evaporation of SiO. The Si nanocrystals along the nanochains were ~10 nm in diameter, separated by narrow SiO_2 regions. Each nanochain defined a multiple-tunnel junction (MTJ) [26, 133]. Single-electron charging in the MTJ led to a Coulomb staircase *I-V* characteristic at 300 K. The single-electron charging energy for a nanocrystal within the MTJ, $E_c = e^2/2C_{eff} \sim 0.32$ eV $\sim 12k_BT$ at 300 K. In the following, we discuss these experiments in more detail.

The Si nanochains were synthesised by thermal evaporation of a SiO powder solid source at 1400°C in a quartz tube furnace [134]. Ar gas carried the vapour through the tube. Undoped Si nanowires and nanochains were synthesised in a cooler part of the furnace at 900°C – 950°C. Depending on the growth conditions, 50% – 90% of the material formed nanochains, with Si nanocrystals separated by SiO_2 'necks'. Nanochain material from the furnace was then dissolved in IPA (0.1 mg / 3 ml IPA) using ultrasonic tip agitation, and spun onto a SiO_2-on-Si substrate at 5000 rpm. Figure 9(a) shows an SEM image of deposited nanochains. The Si nanocrystal diameter in different nanochains varied from <10 nm to ~30 nm, and the separation varied from ~15 nm – 40 nm. The width of the 'necks' varied from approximately the diameter of the Si nanocrystals to well below this value.

Single Si nanochain devices were fabricated by defining Ti/Al contacts to selected single nanochains by electron-beam lithography. The devices were defined on silicon-on-insulator (SOI) material with a ~50 nm thick SiO_2 capping layer, grown thermally on the top Si layer of the SOI material. The top-Si layer, 300 nm thick and doped *n*-type to a concentration of 1×10^{19} /cm^3, formed a conducting back plane and potentially, the back-gate of a SET. The

device was fabricated as follows. Initially, an array of Cr/Au alignment marks was defined by electron-beam lithography on the SiO_2 capping layer. Nanochain material from the furnace, dissolved in IPA (0.1 mg / 3 ml IPA) using ultrasonic tip agitation, was then spun onto the sample at 5000 rpm. Hexamethyldisilisane (HMDS) vapour treatment of the surface was used to improve surface adhesion. Individual nanochains were then selected with reference to the alignment marks by SEM inspection. Finally, 20 nm Ti / 75 nm Al contacts were defined on to the nanochain using electron-beam lithography. Figure 9(b) shows a scanning electron micrograph of a device with a source-drain separation of ~300 nm.

Figure 9(c) shows the drain source I_{ds}-V_{ds} characteristics (Experimental data: circles) of a nanochain device at 300 K [132]. The source-drain separation in this case was ~180 nm, the nanochain width was ~20 nm and there were 7 SiNCs along the nanochain. A multiple-step Coulomb staircase [26, 133] is seen in the characteristics. Three current steps (arrowed) can be identified in the characteristics, at approximately 0.45 V, 1.5 V and 3 V. The threshold voltage for current flow $V_t \approx 0.45$ V, corresponding to the edge of the Coulomb blockade region.

Rafiq *et al* have investigated the Coulomb staircase characteristics using single-electron Monte Carlo simulations [132, 135]. An N junction MTJ circuit, with equal junction capacitances C and island stray capacitances C_0 for simplicity, was used to model the nanochains (Fig. 9(d)). Here, C_0 corresponded mainly to the SiNC to back-plane capacitance. The clarity of the Coulomb staircase suggested a strong asymmetry in the junctions along the MTJ. This was modelled by means of a random variation in the tunnel junction resistances R_n, associated with the observed variation in nanocrystal separation.

Figure 9(c) also shows the simulation results (solid line) for an MTJ with $N = 8$, corresponding to the 7 nanocrystals in this device. The values of C and C_0 were 0.12 aF and 0.12 aF respectively, allowing a close match with the experimental values of $V_t \approx 0.35$ V, and the step positions, $V_{ds} = 1.9$ V and 3.6 V. The average tunnel resistance $R_{av} = 6$ GΩ and a 60% random variation in R_n was applied to the individual junction. This simulation reproduced V_t and the step positions in the experimental characteristics but did not explain the non-linear increase in current along the staircase. This is because effects such as a reduction in the tunnel resistances with V_{ds}, or a Schottky barrier-like potential in series with the MTJ, were not considered [136]. A comparison of C and C_0 to the nanocrystal size, using the self capacitance of a sphere for the nanocrystal, suggested that the conducting core of the nanocrystal was only ~3 nm in diameter. Furthermore, a significant value of C_0 was necessary to reproduce both the low observed values of V_t and the wide step widths in the Coulomb staircase. Simulations where C_0 was increased from zero to 1.2C led to a reduction in V_t, from 4.6 V to ~0.25 V. This was because as C_0 increased, a greater proportion of V_{ds} dropped across the first tunnel junction, due to the voltage divider formed by the first junction capacitance C, and the first stray capacitance C_0 in parallel with the equivalent capacitance of the rest of the MTJ [133].

The single-electron charging energy of the nanocrystals in the nanochain may be estimated using MTJ theory [26]. For a nanocrystal in the centre of the MTJ, approximating the two halves of the MTJ as semi-infinite capacitive networks, the nanocrystal effective capacitance $C_{eff} = (C_0^2 + 4CC_0)^{1/2}$. For $C = C_0 = 0.12$ aF, $C_{eff} = 0.27$ aF and the single-electron charging $E_c = e^2/2C_{eff} \sim 0.30$ eV $\sim 11 k_B T$ at 300 K. Here, C_{eff} is lower than the total capacitance attached to an island, $C_t = 2C + C_0 = 0.36$ aF. Therefore, E_c is higher for a SiNC embedded within a MTJ, as compared to a single SiNC, leading to an improvement in the Coulomb staircase.

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7. Conclusion:

This paper has reviewed electronic transport in Si nanocrystals and nanochains, and the development of single-electron devices using these nanostructures. Si nanocrystals prepared by material synthesis provide a means to define nanoscale devices using 'bottom-up' growth techniques rather than high-resolution lithography. The electronic and optical properties of the nanocrystals are associated with quantum-confinement and single-electron charging effects, with the nanocrystal surface, and in thin films of nanocrystals, with the grain boundary (GB) regions. These properties may be exploited for the fabrication of Si light emitting devices, and nanoscale devices such as single-electron transistors (SETs) and memory.

The paper reviews briefly various Si nanocrystal preparation techniques. Si nanocrystals from a few nanometres to tens of nanometres in diameter may be prepared using the ion implantation of Si into SiO_2 films, sputtering, aerosol deposition, PECVD or LPCVD of nanocrystalline Si thin films, pulsed plasma growth from SiH_4, and by the crystallisation or phase separation of amorphous Si layers within an amorphous Si/SiO_2 layer superlattice. Optimisation of these processes can allow control over the size and shape of the nanocrystals at the nanometre-scale.

Electronic conduction in large-area, continuous, nanocrystalline Si thin films occurs by thermionic emission across potential barriers formed at the GBs in the films. The thermionic emission model may be sufficient if the grain size and associated capacitance C are large. However, as the grain size is reduced to the nanometre scale, single-electron charging and quantum-confinement effects begin to influence the conduction process, particularly at low

temperature. In thin films of discrete Si nanocrystals, depending on the temperature range, the conduction mechanism can be dominated by space-charge limited currents, tunnelling currents, hopping conduction, or single-electron charging effects.

Si nanocrystals may be used to define the charging island in single-electron devices using material growth techniques. If the nanocrystals are <10 nm in size, then $C \sim 1$ aF or less and the single-electron charging energy $e^2/2C$ may be large enough for single-electron effects at room temperature. Both nanocrystalline Si films, and discrete Si nanocrystals, may be used to fabricate SETs and memory devices operating at room temperature. SETs can be fabricated using nanowires, or nanoscale point-contacts, in nanocrystalline Si films. At 4.2 K, these devices can show both electrostatic and electron wavefunction coupling effects between adjacent Si nanocrystals in the film. It is also possible to fabricate few-electron memory cells where charge is stored on Si nanocrystals. Here, a 'floating-gate' for storing charge may be formed by a discontinuous Si nanocrystal layer. Alternatively, charge may be stored, and sensed, within the same nanocrystalline Si film. Recently, strong single-electron charging effects have been observed at room temperature in Si nanochains. The nanochains consist of a series of Si nanocrystals ~10 nm in diameter, separated by SiO_2 regions. Multiple step Coulomb staircase current-voltage characteristics are observed at room temperature in single nanochains. These devices illustrate the potential of Si nanocrystal systems for the fabrication of room-temperature SETs and memory.

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Figure Captions:

Figure 1. (a) Transmission electron micrograph of a ~30 nm thick nanocrystalline Si film, prepared by PECVD [11]. (b) Scanning electron micrograph of a ~300 nm thick film of Si nanocrystals covered by SiO_2 shells, prepared by a VHF pulsed-plasma process [53]. The Si core diameter is ~8 nm.

Figure 2. (a) Schematic diagram in one-dimension, across a *n*-type nanocrystalline Si film. One grain and the two grain boundaries on either side are shown. (b) Charge distribution in the grain and grain boundaries. (c) Energy bands across the grain and grain boundaries. (d) Arrhenius plot, ln(σ) vs. $1/T$ (shown schematically), of conductance σ in a nanocrystalline Si film, as a function of temperature T.

Figure 3. Single-electron effects in a single island, double-tunnel junction system. (a) Circuit diagram, double-tunnel junction (b) Coulomb staircase I_{ds}-V_{ds} characteristics (shown schematically). (c) The single-electron transistor (SET). (b) Single-electron current oscillations in the I_{ds}-V_{gs} characteristics of a SET (shown schematically).

Figure 4. Single-electron charging energy E_c and the quantum-confinement energy E_k, for an isolated spherical Si nanocrystal embedded in SiO_2, as a function of nanocrystal diameter.

Figure 5. (a) Space charge limited current [54] in a ~300 nm thick Si nanocrystal film, consisting of ~8 nm diameter nanocrystals prepared by a VHF pulsed-plasma process. (b) Arrhenius plot of conductance σ as a function of temperature T, at 4 V bias across the film.

Figure 6. Hopping transport [55] in a ~300 nm thick Si nanocrystal film, consisting of ~8 nm diameter nanocrystals prepared by a VHF pulsed-plasma process. A $\ln(\sigma)$ vs. $(1/T)^{1/2}$ dependence is observed.

Figure 7. Transmission electron micrograph of a nanowire SET in nanocrystalline Si. The nanocrystalline Si grain size varies from ~20 nm – 100 nm.

Figure 8. (a) Coulomb blockade I_{ds}-V_{ds} characteristics of a nanowire SET in nanocrystalline Si, at 4.2 K. The curves are offset by 20nA / 0.4 V step in V_{gs} (b) Single-electron current oscillations in the I_{ds}-V_{gs} characteristics of a similar device, at 4.2 K.

Figure 9. (a) Scanning electron micrograph of Si nanochains, deposited on a SiO_2 substrate. (b) Scanning electron micrograph of a single Si nanochain device. (c) Coulomb staircase I_{ds}-V_{ds} characteristics [122] of a single Si nanochain device at 300 K. Solid line: Single-electron Monte-Carlo simulation. Circles: Experimental data. The curves are offset from each other by 5 pA. (d) Multiple tunnel junction model of a nanochain.

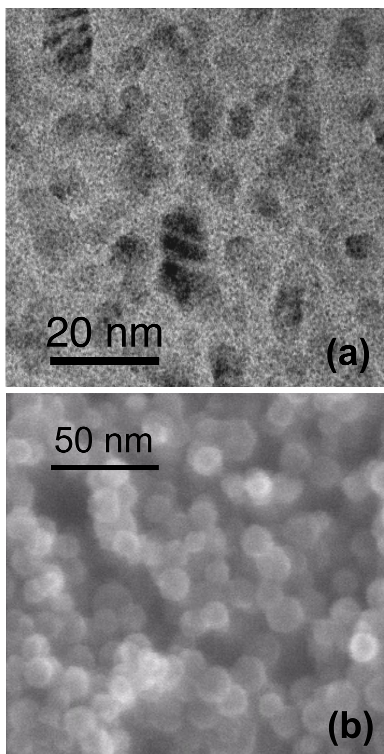


Fig 1

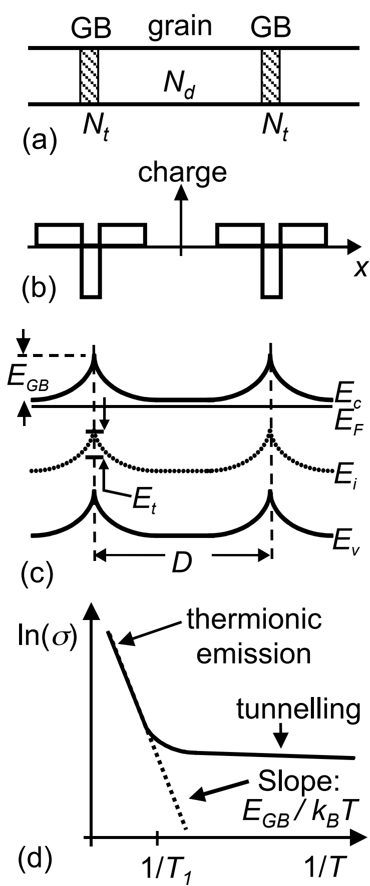
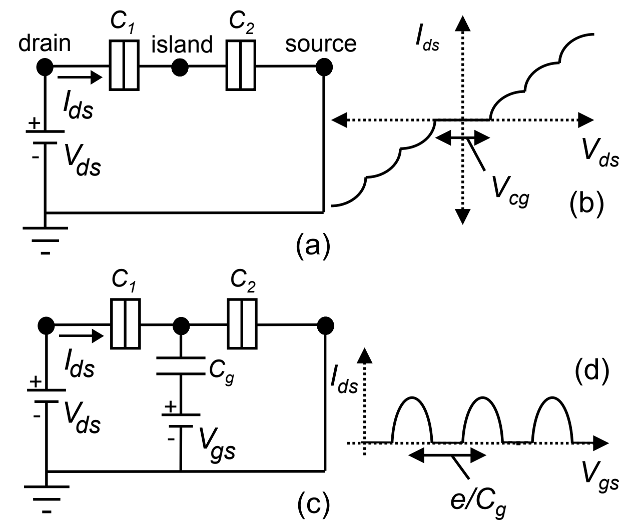


Fig 2



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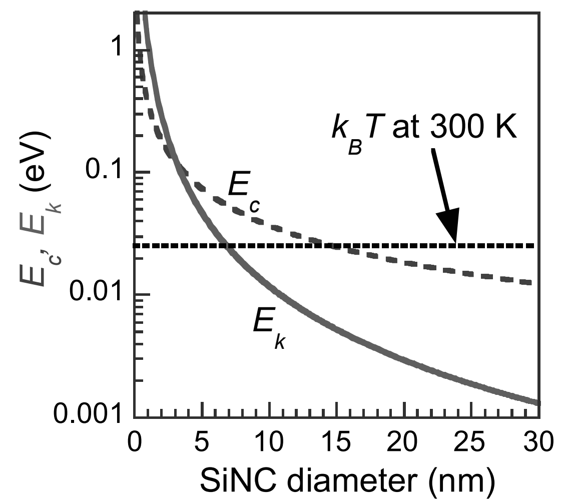

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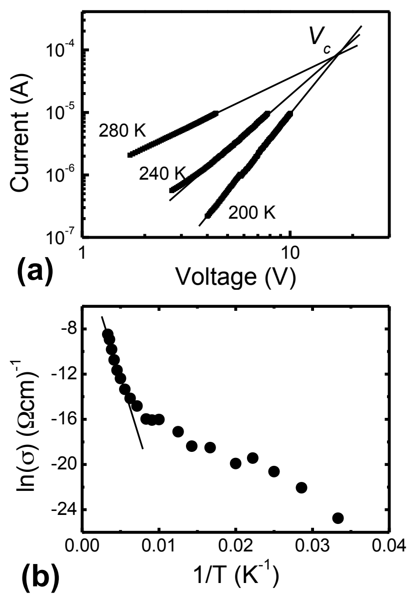

Fig 5

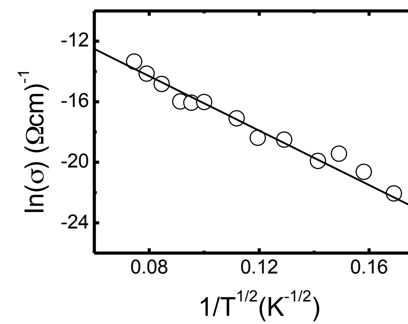

Fig 6

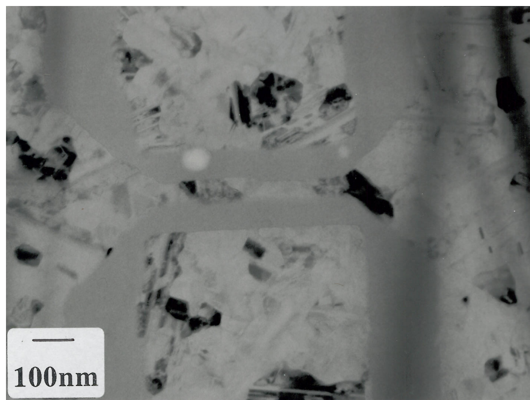

Fig 7

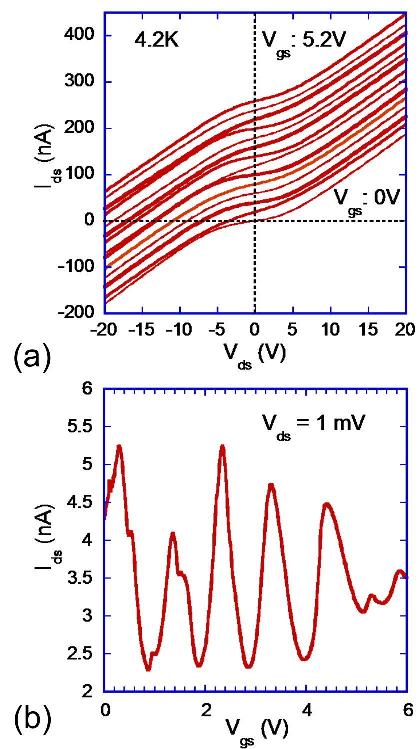

Fig 8

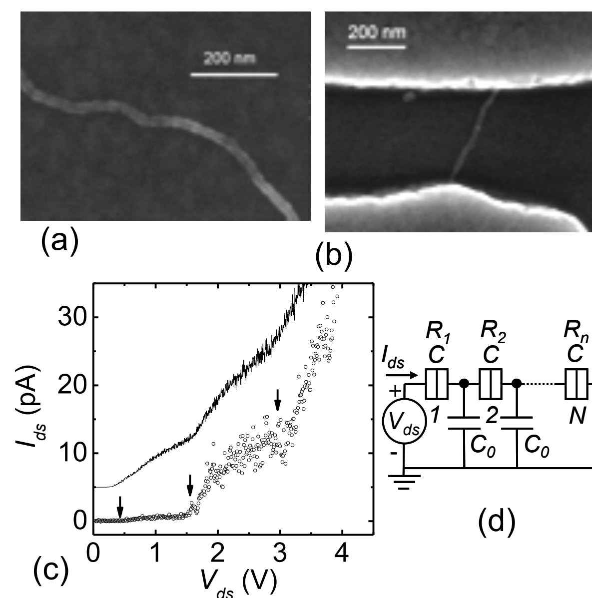

Fig 9