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Electrical Properties of High-k Oxide in Pd/Al_2O_3/InGaAs Stack

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The paper presents the results of capacitance-voltage (C-V) characterization of metal-oxide-semiconductor (MOS) structure, namely Pd/Al_2O_3/ $In_{0.53}Ga_{0.47}As$/InP. It is shown that MOS structure under study exhibit both electron and hole trapping with permanent and temporary charge trapping contributions. The interfacial transition layer between the high-k oxide and InGaAs has the greatest influence on this charge trapping phenomenon.

Keywords: High-k oxide, InGaAs, MOS structure, MOSFET, C-V, ALD, Interface states.

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1. INTRODUCTION

Searching for ultrathin gate dielectric materials is one of the major challenges associated with further downscaling in CMOS technology. High dielectric constant (high-κ) materials with higher permittivity than SiO_2 can be grown thicker providing the same equivalent oxide thickness (EOT) and significant decreasing of gate leakage currents.

While high speed logic and RF applications require implementing of high mobility channel materials such as Ge or InGaAs into CMOS technology the use of high-κ dielectric materials in conjunction with III-V substrate is highly required for the demands of future progress and improvement of MOSFET performance.

It has been reported [1, 2] that high-κ materials often suffer from the charge trapping and poor electrical quality of the dielectric-semiconductor interface as compared to SiO_2. In addition the high-κ/InGaAs MOS system exhibits a relatively high level of interface states (D_{it}) and fixed oxide charges (QF) [3, 4], both of which induce threshold voltage shifts and degrade carrier mobility in InGaAs MOSFETs. The understanding of interface (D_{it}) and bulk defects in the high-κ/$In_xGa_{1-x}As$/InP metal-oxide-semiconductor (MOS) system will be essential for the successful implementation of high mobility channel materials in MOS Field Effect Transistor (MOSFET).

In this work we present results of a study focused on the characterization of interface defects and bulk electron/hole traps in the high-κ/$In_{0.53}Ga_{0.47}As$/InP MOS system.

2. EXPERIMENTAL

The studies were performed on Pd/Al_2O_3/ $In_{0.53}Ga_{0.47}As$/InP MOS structures with high-κ Al_2O_3 oxide layers formed by atomic layer deposition (ALD) of nominal physical thickness of 5, 10, 15 and 20 nm. The top Pd gate metallization was obtained by a shadow mask process. The samples received no post-metallization annealing treatment. To investigate hole and electron trapping in the bulk of oxide film, samples with both *n*- and *p*- type doped (4×10^{17} cm^{-3}) $In_{0.53}Ga_{0.47}As$ epitaxial layers were examined.

MOS capacitors were characterized by capacitance-voltage (C-V) measurements at room temperature using an Agilent E4980A Precision LCR meter.

3. RESULTS AND DISCUSSION

Fig. 1 presents the relation between inverse of maximum accumulation capacitance, $1/C_{max}$, and oxide thickness, t_{OX}, for Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS structure with t_{OX} ranging from 5 nm to 20 nm.

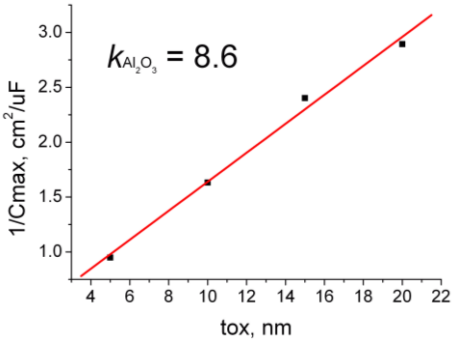

Fig. 1 – $1/C_{max}$ versus oxide thickness (t_{OX}) for MOS structures with t_{OX} ranging from 5 nm to 20 nm

The Al_2O_3 κ-value (8.6) was obtained from the slope of the capacitance equivalent thickness in accumulation versus the oxide thickness t_{ox}. The cross-sectional high resolution transmission electron microscopy (HRTEM) image through the gate oxide region confirmed a nominal thickness of 10 nm (Fig. 2).

The high-κ/$In_{0.53}Ga_{0.47}As$ system typically exhibit interface state densities (D_{it}) to be in the range mid-10^{12} to 10^{13} cm^{-2} eV^{-1} [4-6]. Analysis of the capacitance-voltage (C-V) response indicates interface states of predominantly donor type with D_{it} ranging from 0.8×10^{13} to 1.5×10^{13} cm^{-2}. These results are consistent with As_{Ga} antisite defects based on hybrid density functional calculations of point defects in III–V compounds [7]. Recent studies show that similar C-V responses are obtained for a wide range of oxides ($SrTa_2O_6$, HfO_2, Si_3N_4) which could be the result of the defects originating from $In_{0.53}Ga_{0.47}As$ surface.

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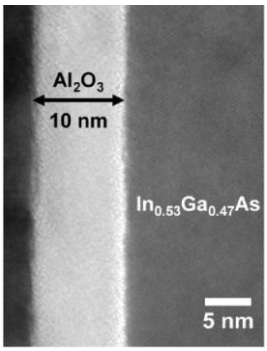

Fig. 2 – Cross sectional HRTEM image of the structure with t_{OX} = 10 nm.

High-frequency C-V characteristics were measured on MOS capacitors at room temperature (Fig. 3). The results indicate that both electrons and holes are trapped for *n*- and *p*- $In_{0.53}Ga_{0.47}As$ MOS structures, respectively. The flatband voltage shift corresponds to charge trapping (Q_T) level of ~$1x10^{13}$ cm^{-2} which is comparable to, or larger than, the interface state density (D_{it}) integrated across the $In_{0.53}Ga_{0.47}As$ band gap.

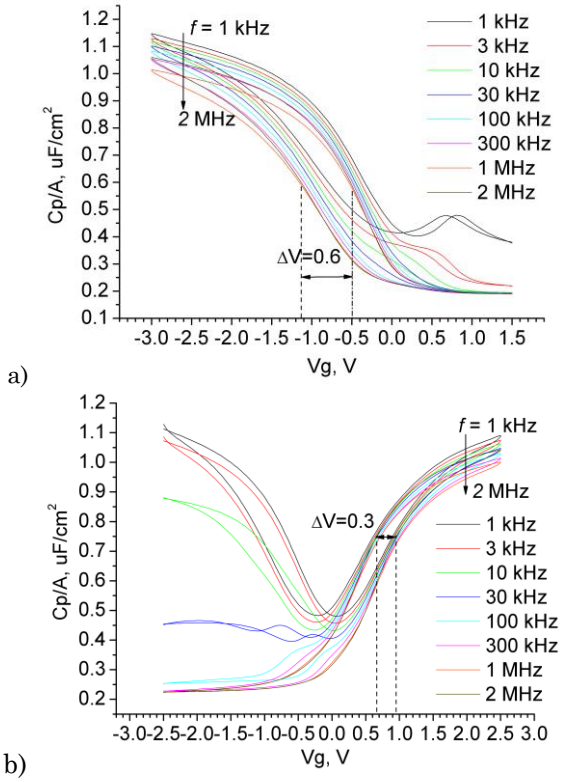

Fig. 3 – Frequency dependence of C-V characteristic for a Pd/Al_2O_3(5nm)/*p*- (a) *n*- (b) $In_{0.53}Ga_{0.47}As$/InP MOS structure at room temperature.

Moreover, the trapping is primarily a reversible process, where the trapped charge removed at the onset of a second C-V hysteresis sweep. More C-V sweeps were carried out with charging in accumulation regime within hold time of 1, 3, 10, 30, 100, 300 and 1000 seconds which showed no presence of degradation after tests (Fig. 4).

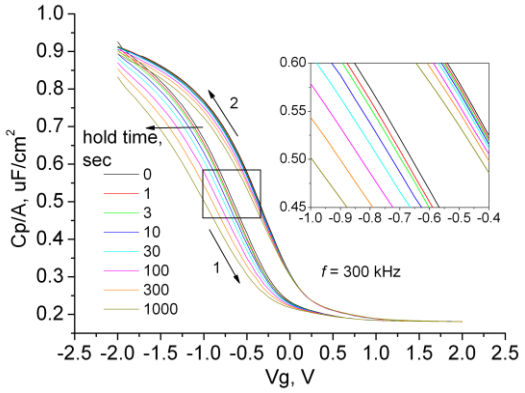

Fig. 4 – High-frequency (300 kHz) C-V characteristics biased at accumulation regime within hold time of 1, 3, 10, 30, 100, 300 and 1000 seconds at room temperature.

The trapped charge density also depends on the hold time and maximum gate bias. Based on samples with variable high-κ thickness, C-V hysteresis studies reveal a linear increase in C-V hysteresis with increasing oxide thickness (Fig 5). All of these experimental observations and analysis are consistent with the charge trapping taking place primarily as a line charge at the high-κ/$In_{0.53}Ga_{0.47}As$ interface, which can contain native oxides of Ga, In and As [8].

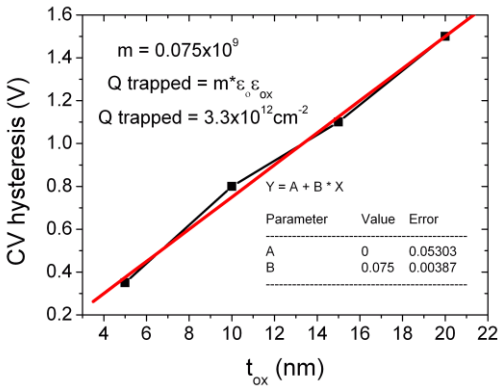

Fig. 5 – C-V hysteresis as a function of oxide thickness for Pd/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$/InP MOS structure. The linear increase in C-V hysteresis (or ΔV) with increasing oxide thickness indicates the trapping charge is primarily a sheet charge, $\Delta V = Q_{trapped} * (t_{ox}/\varepsilon_0\varepsilon_{ox})$. From the gradient $Q_{trapped}$ = 3.3 x 10^{12} cm^{-2} (negative charge).

In summary, Pd/high-κ/$In_{0.53}Ga_{0.47}As$/InP MOS capacitors exhibit both electron and hole trapping with permanent and temporary charge trapping contributions. The interfacial transition layer between the high-κ oxide and $In_{0.53}Ga_{0.47}As$ has the greatest influence on this charge trapping phenomenon.

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