PIEZOTRONIC DEVICES AND INTEGRATED SYSTEMS

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PIEZOTRONIC DEVICES AND INTEGRATED SYSTEMS

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To my mother

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CPU	central processing unit
CMOS	complementary metal-oxide-semiconductor
SEM	scanning electron microscope
MOSFET	metal-oxide-semiconductor-field-effect-transistor
PLD	pulse laser deposition
HMTA	hexamethylenetetramine
MEMS/NEMS	micro/nano-electromechanical-system
AFM	atomic force microscopy
FEM	finite element method
PDMS	polydimethylsiloxane
LED	light-emitting-diode
SBH	Schottky-barrier height
SGT	strain-gated transistor
SGI	strain-gated inverter
SVTC	strain-voltage transfer characteristic
PRM	piezotronic resistive memory
ITO	Indium tin oxide

SUMMARY

Novel technology which can provide new solutions and enable augmented capabilities to CMOS based technology is highly desired. Piezotronic nanodevices and integrated systems exhibit potential in achieving these application goals. By combining laser interference lithography and low temperature hydrothermal method, an effective approach for ordered growth of vertically aligned ZnO NWs array with high-throughput and low-cost at wafer-scale has been developed, without using catalyst and with a superior control over orientation, location/density and morphology of as-synthesized ZnO NWs. Beyond the materials synthesis, by utilizing the gating effect produced by the piezopotential in a ZnO NW under externally applied deformation, strain-gated transistors (SGTs) and universal logic operations such as NAND, NOR, XOR gates have been demonstrated for performing piezotronic logic operations for the first time. In addition, the first piezoelectrically-modulated resistive switching device based on piezotronic ZnO NWs has also been presented, through which the write/read access of the memory cell is programmed via electromechanical modulation and the logic levels of the strain applied on the memory cell can be recorded and read out for the first time. Furthermore, the first and by far the largest 3D array integration of vertical NW piezotronic transistors circuitry as active pixel-addressable pressure-sensor matrix for tactile imaging has been demonstrated, paving innovative routes towards industrial-scale integration of NW piezotronic devices for sensing, micro/nano-systems and human-electronics interfacing. The presented concepts and results in this thesis exhibit the potential for implementing novel nanoelectromechanical devices and integrating with MEMS/NEMS technology to achieve augmented functionalities to state-of-the-art CMOS technology such as active interfacing between machines and human/ambient as well as micro/nano-systems capable of intelligent and self-sufficient multi-dimensional operations.

CHAPTER 1

INTRODUCTION

1.1 Complementing device miniaturization with functional diversification

There has been an increasing demand in developing micro/nano-systems (MNS) for wireless and personal applications and it is predicted that the market for wireless sensor network (WSN) will grow rapidly from $0.45 billion in 2011 to $2 billion in 2021[1]. In addition to the conventional technology trajectory of miniaturizing components dimensions for enhanced operation performance as per Moore's law, which has been the principal roadmap that drives and directs the advancement of information technology in the last few decades, enormous efforts have been recently focused on integrating individual micro/nano-devices with diversified functionalities into multi-functional MNS and further into large-scale networks for potential applications in ultrasensitive chemical sensing[2], remote and mobile environmental monitoring[3], structural health monitoring[4], homeland security[5], portable/wearable biomedical devices and personal electronics [6,7]. In order to fulfill these application promises, each device/system node within the network should consist of low power microcontroller unit, high-performance data processing/storage components, wireless signal transceiver, ultrasensitive micro/nano-electromechancial system (MEMS/NEMS) based sensors, and embedded energy powering units[8-12].

Integration of these discrete devices with dedicated functionality toward self-powered smart systems is prospected to be one of the major roadmaps for electronics[13]. The miniaturized dimensions of nanomaterials together with the capability of modulating their compositions and obtaining unprecedented properties compared to bulk counterparts in well-controlled manners not only exhibit the potential for addressing some of the critical challenges faced by silicon-based microelectronics as technology node advances,

but also enable the possibility of incorporating diversified functionalities which do not necessarily scale as per Moore's Law into the systems to complement digital signal/data processing with augmented functional capabilities, such as interactions between machine and human/environment (Figure 1). Numerous nodes of such device/system can be spatially distributed and embedded virtually anywhere ranging from remote field, civil structures, to even human body for fulfilling respective purposes.

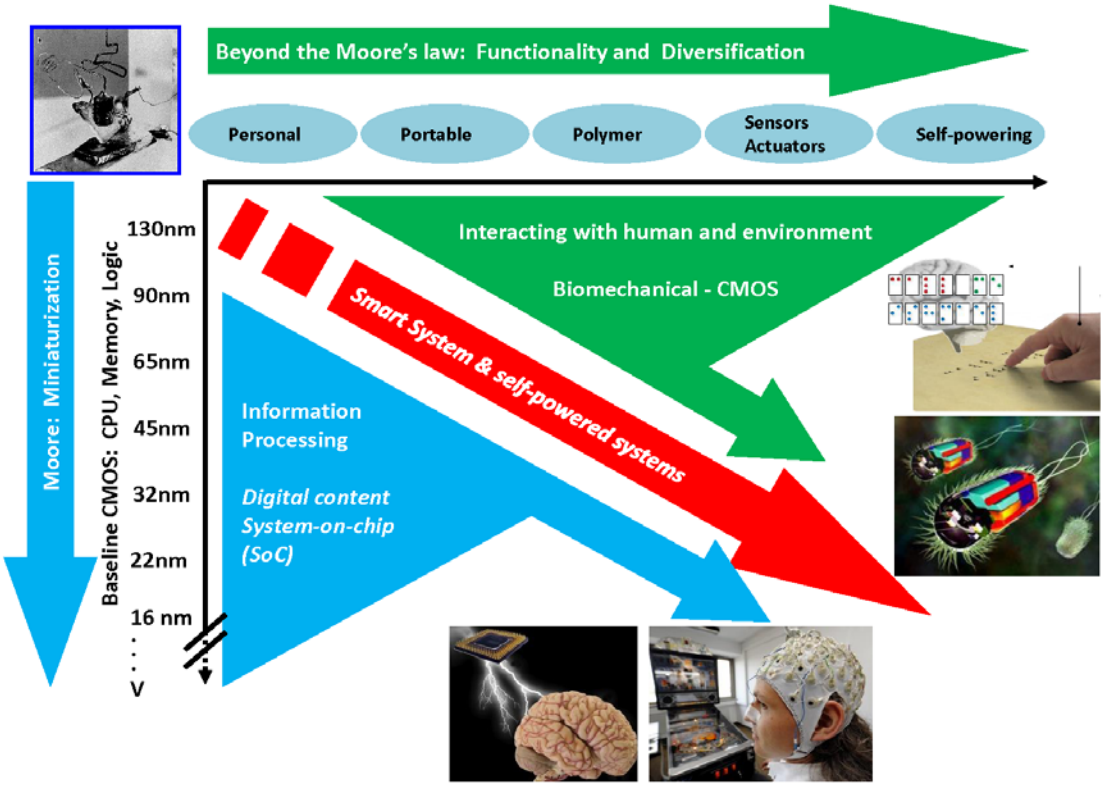


Figure 1. Future perspective of electronics beyond Moore's law. The vertical axis represents a miniaturization and increase of device density, CPU speed and memory capacity. The horizontal axis represents the diversity and functionality for personal and portable electronics. The future of electronics is an integration of CPU speed and functionality[14].

1.2 Interface between electronics and human/ambient

As the complement of digital signal/data processing, the aforementioned diversified functionalities include interaction between the device and ambient through appropriate transduction mechanism as well as embedded energy scavenging/storage

components for powering the device operations. In prospective applications such as prosthetics, artificial intelligence and robotics, electronic systems need to directly interface the ambient environment like the human body itself, which is abundant with activities and "signals" such as mechanical actions and electrical signals[13]. Transmission of electrical signals via neuron system inside human body have been investigated for decades and various approaches have been developed for interfacing neuron activities with silicon based electronics[15-18]. Mechanical actions, whereas, is not easy to be directly interfaced with silicon electronics without innovative design and approaches. Traditionally, signals from transducers sensitive to strain variation can be probed and acquired by electronic devices. These signals, however, cannot be directly utilized to control silicon electronics.

One major focus in current research of flexible electronics is to minimize and eliminate the effect of strain introduced by the substrate on the performance of the electronic components built on a substrate, which can be termed as the passive flexible electronics. On the other hand, the deformation introduced by the substrate can be utilized to induce electrical signals that can be used directly for controlling Si based electronics. A "mediator" or "translator" is needed for the conjunction of bio-mechanical action and operation of silicon based electronics. The piezotronics and piezo-phototronics are invented for such purposes, and they are considered as the active flexible electronics or bio-driven electronics[19-21], which enables novel approach for directly generating digital signals and electronic control using mechanical actions.

The role anticipated to be played by piezotronics is similar to the mechanosensation in physiology[22]. Mechanosensation is a response mechanism to mechanical stimuli. The physiological foundation for the senses of touch, hearing and balance, and pain is the conversion of mechanical stimuli into neuronal signals; the former is mechanical actuation and the latter is electrical stimulation. For instance,

mechanoreceptors of the skin are responsible for touch while tiny cells in the inner ear are responsible for hearing and balance.

1.3 Thesis outline

This thesis consists of seven chapters. Following this introduction chapter is a discussion on the fundamental physics and concepts, such as piezopotential and piezotronic effect, in the field of piezotronics and related applications. The modulation effect of piezopotential on transport of charge carriers in metal-semiconductor contact and *p*-*n* junction, both of which are the essential building blocks for modern electronics, are also addressed and discussed in details in Chapter 2. Chapter 3 investigates the various synthesis processes for growing one-dimensional ZnO nanostructures for piezotronic applications. Synthesis methods based on vapor-solid (VS) and solution phase hydrothermal (HT) processes are discussed with more emphasis, since ZnO NWs obtained from VS process constitute the majority materials for fabricating single-NW based piezotronic applications, and ZnO NW arrays derived from HT process provide the material platform for realizing large-scale piezotronic array applications, particularly on flexible substrates. Other synthesis methods such as vapor-solid-solid (VSS) and pulsed laser deposition (PLD) processes are also discussed in Chapter 3 and their potential in realizing ZnO NWs array with high crystallinity, adjustable dopant type, doping levels and controllable bandgap engineering is also investigated. Chapter 4 demonstrates for the first time the piezotronic logic operations by utilizing the gating effect produced by piezopotential in a ZnO NW under externally applied deformation. Universal strain-gated logic operations such as NAND, NOR and XOR gates have been implemented by integration of ZnO NW based strain-gated transistors (SGTs). In contrast to the conventional CMOS logic units, the SGT based logic units are driven by mechanical agitation and rely only on *n*-type ZnO NWs without the presence of *p*-type semiconductor components. The mechanical-electronic logic units can be integrated with

NEMS technology to achieve advanced and complex functionalities in nanorobotics, microfluidics and micro/nano-systems, in which mechanical actions such as the movement of robots, fluidic flow and hydrostatic pressure induced in the micro-channels or micro-valves might be utilized for performing electromechanical logic operations for controlling and processing purposes. In Chapter 5, a novel nanoelectromechanical memory device has been presented. By utilizing the strain-induced polarization charges created at the semiconductor/metal interface under externally applied deformation as a result of piezotronic effect, the switching characteristics of the ZnO NW resistive switching devices can be modulated and controlled. It is further demonstrated that the logic levels of the strain applied on the memory cell can be recorded and read out for the first time utilizing the piezotronic effect, which has the potential for implementing novel nanoelectromechanical memories and integrating with NEMS technology to achieve micro/nano-systems capable of intelligent and self-sufficient multi-dimensional operations such as tactile sensing and imaging. As a critical step towards practical applications, Chapter 6 presents the first and by far the largest 3D array integration of vertical NW piezotronic transistors circuitry as active pixel-addressable pressure-sensor matrix for tactile imaging. The demonstrated highest spatial resolution and tactile sensitivity with the smallest pixel dimension and pitch size present the landmark breakthrough in implementing 3D piezotronic transistor arrays and pave innovative routes towards industrial-scale integration of NW piezotronic devices for sensing, micro/nano-systems and human-electronics interfacing. Finally, Chapter 7 concludes this thesis and provides discussions and prospects on potential future work in related field.

CHAPTER 2

PIEZOPOTENTIAL AND PIEZOTRONIC EFFECT

In order to realize augmented capabilities such as interfacing between machine and human/ambient, a direct control over the operation of electronic devices by mechanical action is highly desired. Since silicon-based CMOS devices operate via electrically-modulated charge transport process, it is necessary to utilize electric signal which can be generated by mechanical action.

2.1 Piezopotential

Piezoelectricity is a phenomenon which produces electrical potential in the material upon variations of applied pressure/stress. The piezoelectric effect can be interpreted as the linear electromechanical coupling/interaction between mechanical and electrical state in materials which lack inversion symmetry[23]. Piezoelectricity has been observed in a wide range of materials from ceramics, synthetic polymers to biological materials in response to applied mechanical stress. The most well-known piezoelectric material is Perovskite -structured $Pb(Zr_xTi_{1-x})O_3$ (PZT), which has numerous applications in electromechanical sensing, actuating and energy harvesting [24-26]. Traditionally, investigation and application of piezoelectric materials have been largely carried out by the ceramics community. PZT, however, is electrically-insulating and hence less useful for building electronic devices. In addition, the extremely brittle nature of ceramic PZT films and existence of lead impose issues such as reliability, durability and safety for long term sustainable operations and hinder its applications in areas such as biomedical devices.

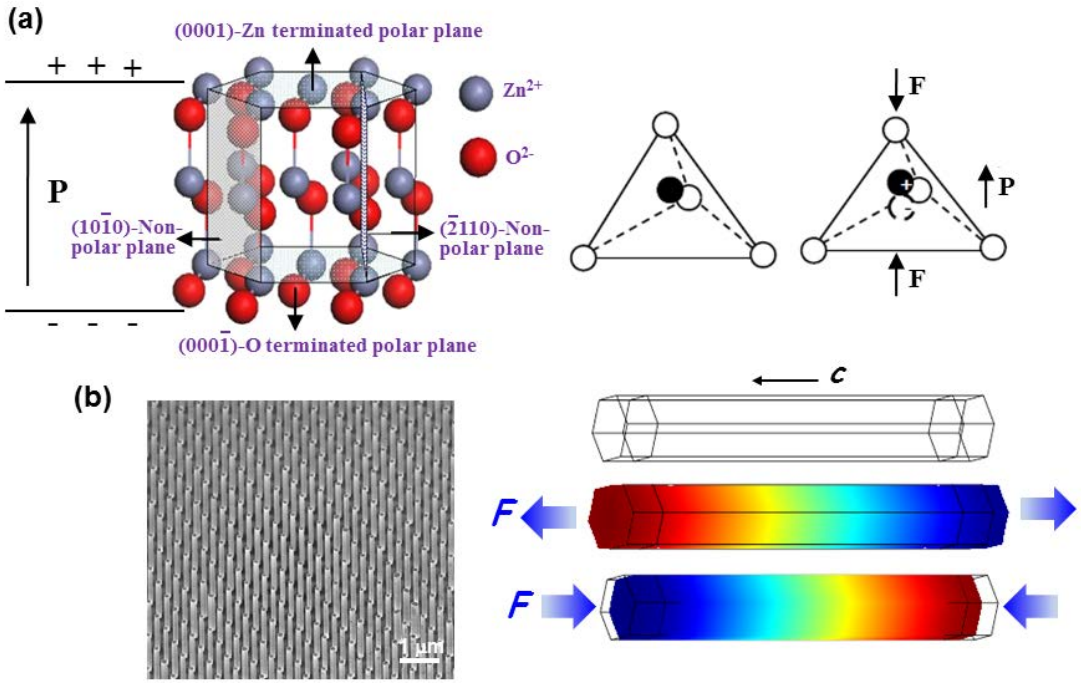


Figure 2. Piezopotential in Wurtzite crystal. (a) Atomic model of the Wurtzite-structured ZnO. (b) Left, large-scale aligned ZnO nanowire (NW) arrays by solution based hydrothermal approach[27]. Right, distribution of piezopotential along a ZnO NW under axial strain calculated by numerical methods[28]. The growth direction of the NW is along *c*-axis.

On the other hand, semiconductor materials with Wurtzite structures such as ZnO, GaN, InN and ZnS also possess piezoelectric properties but are not as extensively utilized in piezoelectric sensors and actuators as PZT due to their relatively small piezoelectric coefficients[29]. ZnO, for example, has a crystal structure with non-central symmetry, which naturally produces piezoelectric effect upon strained. The unique properties of ZnO, such as photo-excitation, biocompatibility and degradability[30], in addition to its semiconductor, pyroelectric and piezoelectric characteristics, enable the wide utilizations and applications of ZnO nanomaterials in sensing[31], energy conversion and scavenging[32], light-emitting diodes[33] and piezotronics[11,29].

Wurtzite ZnO crystal has a hexagonal structure with a large anisotropic property in *c*-axis direction and perpendicular to the *c*-axis. The Zn^{2+} cations and O^{2-} anions are tetrahedrally coordinated and the centers of the positive ions and negatives ions overlap

with each other. If a stress is applied at an apex of the tetrahedron, the centers of the cations and anions are relatively displaced, inducing a dipole moment (Figure 2a). A constructive addition of all the dipole moments within all of the units in the crystal results in a macroscopic potential drop along the straining direction in the crystal. This is the piezoelectric potential (*piezopotential*) (Figure 2b)[29].

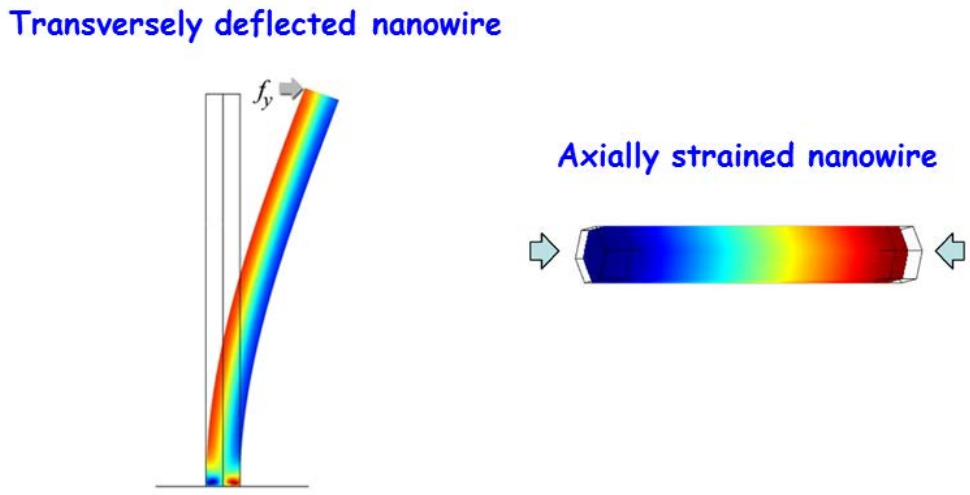


Figure 3. Distribution of piezopotential in two typical configurations of NW devices. The color gradient represents the distribution of piezopotential in which red indicates positive piezopotential and blue indicates negative piezopotential.

Piezopotential is the strain-induced inner crystal field, which is created by non-mobile and non-annihilative ionic charges. Therefore piezopotential exists as long as the applied strain maintains. Piezopotential can also drive the flow of electrons in the external load when the materials are subjected to mechanical deformation, which is the fundamental of the nanogenerator[34,35]. The distribution of piezopotential has been investigated based on two typical configurations of NW devices: transversely deflected NW and axially strained NW (Figure 3). The transversely deflected NWs are normally utilized in nanogenerator applications[32], while the axially strained NWs are used in piezotronic applications on flexible substrates[30]. The following sections will briefly discuss the fundamental theory for calculating the distribution of piezopotential in nanostructures without and with considering the presence of finite doping. The finite

conductivity possessed by the material can partially screen the regional piezopotential accordingly, but cannot completely cancel the effect of polarization charge due to the dielectric property of the material and the moderate doping level.

2.1.1 Piezopotential distribution in transversely deflected NW

Numerous efforts have been put into investigating piezoelectricity in one-dimensional nanostructures, including first-principle calculations[36,37], molecular dynamics (MD) simulations[38] and modeling based on continuum theory[39]. However, it is rather cumbersome to implement first-principle theory and MD simulation for studying piezoelectricity in nanoscale system due to the huge number of atoms incorporated in these systems (typical dimension of a nanoscale system is ~ 50 nm in diameter and ~2 micron in length). The continuum model, however, is insightful since it provides the criterion for distinguishing between mechanically dominated regime and electro-statically dominated regime[39]. Wang's group previously established a continuum model for evaluating the electrostatic potential in a laterally bent NW[40].

The configuration of laterally bent NW is commonly utilized in nanogenerator and potential novel piezotronic applications[41-43]. The theoretical objective is to derive the relationship between the piezopotential distribution in a laterally bent NW and the dimensionality of the NW as well as the magnitude of the applied force at the tip. The governing equations for a static piezoelectric material include mechanical equilibrium equation (Equations 1), constitutive equation (Equations 2), geometrical compatibility equation (Equation 3) and Gauss equation of electric field (Equation 4)[40]. The mechanical equilibrium condition when there is no body force $\vec{f}_e^{(b)} = 0$ acting on the nanowire is:

$$\nabla \cdot \sigma = \vec{f}_e^{(b)} = 0 \tag{1.1}$$

Here σ is the stress tensor, which is related to strain ε, electric field E and electric displacement D by constitutive equations:

$$\begin{cases} \sigma_p = c_{pq}\varepsilon_q - e_{kp}E_k \\ D_i = e_{iq}\varepsilon_q + \kappa_{ik}E_k \end{cases} \tag{1.2}$$

Here c_{pq} is the linear elastic constant, e_{kp} is the linear piezoelectric coefficient, and k_{ik} is the dielectric constant. The contribution of spontaneous polarization resulting from the polar charges on the ±(0001) polar surfaces, which are the top and bottom ends of the NW, are not taken into consideration here in equation 1.2[44]. By considering the C_{6v} symmetry of Wurtzite-structured ZnO crystal, c_{pq}, e_{kp} and k_{ik} can be expressed in the following reduced forms:

$$c_{pq} = \begin{pmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{13} & 0 & 0 & 0 \\ c_{13} & c_{13} & c_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \dfrac{(c_{11}-c_{12})}{2} \end{pmatrix} \tag{2.1}$$

$$e_{kp} = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \tag{2.2}$$

$$\kappa_{ik} = \begin{pmatrix} \kappa_{11} & 0 & 0 \\ 0 & \kappa_{11} & 0 \\ 0 & 0 & \kappa_{33} \end{pmatrix} \tag{2.3}$$

Meanwhile, strain ε_{ij} must also satisfy the geometrical constraint set by the compatibility equation:

$$e_{ilm}e_{jpq}\frac{\partial^2 \varepsilon_{mp}}{\partial x_l \partial x_q} = 0 \tag{3}$$

Here e_{ilm} and e_{jpq} are Levi-Civita anti-symmetric tensors[40].

Finally, for simplicity of derivation, Gauss equation must be satisfied by assuming no free charge $\rho_e^{(b)}$ in the NW:

$$\nabla \cdot \vec{D} = \rho_e^{(b)} = 0 \tag{4}$$

This indicates that the governing equation (4) only applies to insulating piezoelectric materials, while in reality, piezoelectric materials such as ZnO is intrinsically *n*-type doped due to the unavoidable native defects[45]. More sophisticated models considering finite doping in ZnO NWs will be discussed later.

The above governing equations (1-4) together with appropriate boundary conditions will give the complete description of a static piezoelectric system. However, solution to these equations is rather complex, and analytical solution does not exist in many cases. In order to derive an approximate solution to these equations for providing the basic physical picture, Gao *et al* carried out perturbation expansion of the linear equations to simplify the analytical solution[40]. The NW is assumed to have a uniform cylindrical shape with diameter *2a* and length *l*. The strain and stress relation is thus given by[40]:

$$\begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{zx} \\ 2\varepsilon_{xy} \end{pmatrix} = \sum_q a_{pq}^{isotropic} \sigma_q = \frac{1}{E} \begin{pmatrix} 1 & -\nu & -\nu & 0 & 0 & 0 \\ -\nu & 1 & -\nu & 0 & 0 & 0 \\ -\nu & -\nu & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2(1+\nu) & 0 & 0 \\ 0 & 0 & 0 & 0 & 2(1+\nu) & 0 \\ 0 & 0 & 0 & 0 & 0 & 2(1+\nu) \end{pmatrix} \begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{pmatrix} \quad (5)$$

where E is Young's modulus and υ is Poisson ratio.

In the configuration of transversely deflected NW, the lateral force f_y is assumed to be applied uniformly on the top surface of NW so that there is no effective torque which twists the NW[40]. By applying Saint-Venant principle to simplify the boundary condition, the maximum potential on the surface ($r = a$) of the NW at the tensile (T) side ($\theta = -90^o$) and the compressive (C) side ($\theta = 90^o$) has been obtained in the following expression:

$$\varphi_{\max}^{(T,C)} = \pm \frac{1}{\pi} \frac{1}{\kappa_0 + \kappa_\perp} \frac{f_y}{E} [e_{33} - 2(1+\nu)e_{15} - 2\nu e_{31}] \frac{1}{a} \quad (6)$$

Here $\kappa_\perp = \kappa_{11} = \kappa_{22}$ and κ_0 is the permittivity in vacuum. Furthermore, by applying fundamental elastic theory, the lateral force f_y is related to maximum deflection of the NW tip $\upsilon_{max} = \upsilon(z = l)$ under small deflection by:

$$v_{\max} = \frac{f_y l^3}{3EI_{xx}} \tag{7}$$

Consequently, the maximum potential at the NW surface can be expressed as[40]:

$$\varphi_{\max}^{(T,C)} = \pm \frac{3}{4(\kappa_0 + \kappa_\perp)} [e_{33} - 2(1+\nu)e_{15} - 2\nu e_{31}] \frac{a^3}{l^3} v_{\max} \tag{8}$$

Since Saint-Venant principle is applied to simplify the boundary condition, equation (8) is valid only for regions far away from the fixed end of the NW. Subsequent full numerical calculation shows the above equation is feasible when the distance from the fixed end is larger than twice the NW diameter[40]. Equation (8) indicates that electric potential (in cylindrical coordinates) is independent of vertical height *z*, which suggests that the potential is uniform along *z* direction except for regions very close to the fixed end of the NW. Moreover, electrostatic potential is directly related to the aspect ratio of the NW instead of its absolute dimensionality. For a NW with a fixed aspect ratio, the induced piezopotential is proportional to the maximum deflection at the NW tip.

The validity of derived analytical equation (8) in describing the piezopotential distribution in transversely deflected NW has also been verified by comparing results obtained from equation (8) and finite element method (FEM) calculation for a fully coupled electro-mechanical system using equations (1-4)[40]. Figure 4 shows the comparison between results given by both methods and it reveals that the difference between results derived from analytical equation and those from full numerical calculation is only 6%.

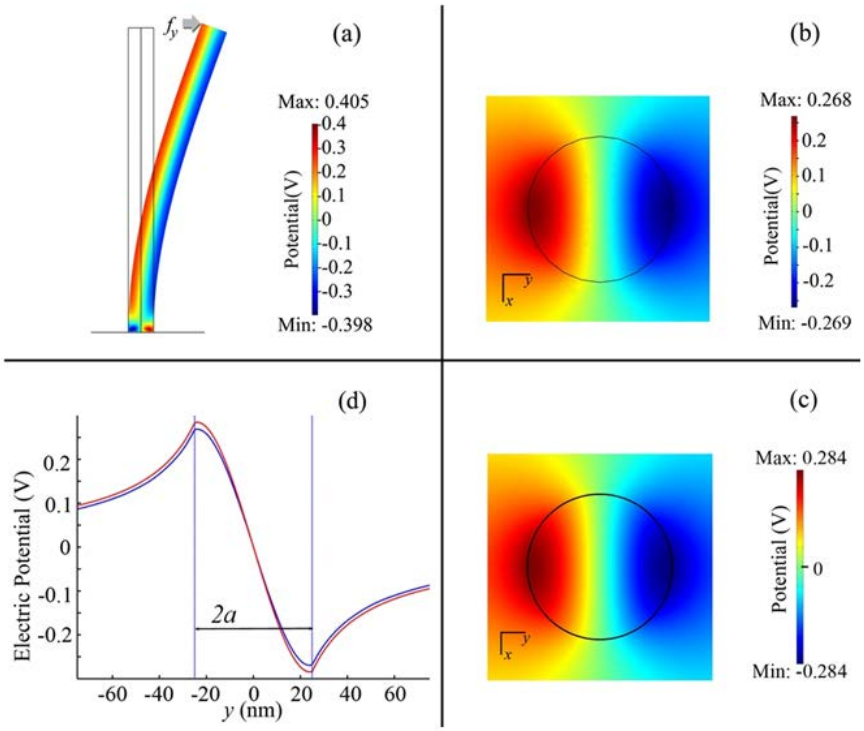


Figure 4. Potential distribution for a ZnO NW with d = 50 nm and l = 600 nm experiencing a lateral bending force of 80 nN. (a) and (b) are the side and top cross-sectional (at z_0 = 300 nm) piezopotential output in the NW obtained by finite element calculation using fully coupled equations (1-4), while (c) is the cross-sectional piezopotential output calculated by analytical equation (8). (d) gives a comparison of the line-scan profiles from both (b) and (c), showing the accuracy of equation (8) and approximations applied for deriving it (blue line is for result obtained from full finite element method (FEM) and red line is for result given by equation (8))[40].

2.1.2 Piezopotential distribution in axially strained NW

Another commonly encountered configuration for ZnO NW based nanoelectronic device incorporates the horizontally placed Wurtzite ZnO NW, with its two ends and regions close to the ends fully covered by metal electrodes on the substrate (normally flexible material). The dimension of NWs is orders of magnitude smaller than that of the supporting substrates so that the mechanical behavior of the entire device is dictated by the substrate. In reality, various kinds of forces, including tensile, compression, twisting and combinations of them, might act on the NW during operation[28]. The fully coupled

equations (1-4) can be solved with finite element method (FEM) and corresponding distribution of piezopotential throughout the NW under these forces can then be obtained[28]. For simplicity and concentrating on how the piezopotential would vary under different strains, it is assumed that there is no body force and no free charge carriers in the NW. Figure 5 (top) shows a ZnO NW without any applied force. The total length of the NW is 1200 nm with a 100 nm length of contact domain at each end, and the side length of the hexagon is 100 nm. When an axial stretching force of 85 nN uniformly acts on the NW in the direction parallel to *c*-axis, as shown in Figure 5 (middle), a potential drop of approximately 0.4 V is induced between the two ends of the NW. When the applied force changes to compressive type, the magnitude of the induced piezopotential remains at 0.4 V while its polarity reverses (Figure 5, bottom)[28]. It can be seen clearly that piezopotential continuously drops from one side of the NW to the other, indicating that electron energy also continuously increases from one end of the NW to the other. Meanwhile, the Fermi level remains flat all over the NW at equilibrium. Consequently, the electron energy barrier between ZnO and metal electrodes will be raised at one side and lowered at the other side, which should lead to experimentally observable asymmetric I-V characteristics for the NW device. This is the governing principle for understanding the experimental results presented in later sessions of this thesis.

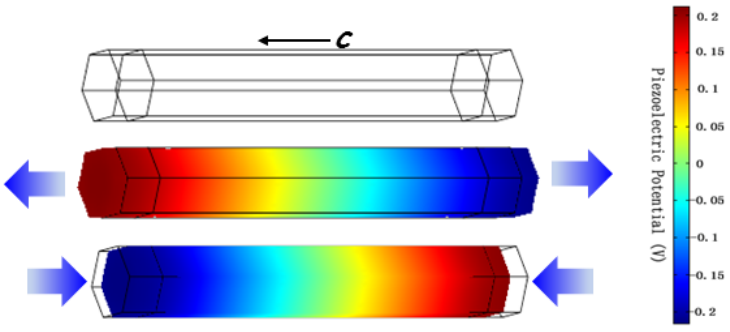


Figure 5. Numerical calculation results of the piezopotential distribution in a ZnO NW without considering the doping. (Top) An unstrained ZnO NW grown along *c*-axis. (Middle) Distribution of piezopotential together with deformed shape for the NW by stretching force and (Bottom) by a compressing force of same magnitude[28].

The effect of piezoelectricity on transport properties of metal-ZnO NW device contains two parts: one is the spontaneous polarization charge effect induced by the Zn^{2+} and O^{2-} terminating layers at the +*c* and -*c* end surfaces of NW structure[44]; the other is the piezopotential effect introduced by piezoelectric polarization charges. Strain will not only induce piezoelectric effect in ZnO, but also cause variations in band structure. The induced deformation potential can also change the height of Schottky barrier formed between ZnO and metal electrodes: under tensile strain the barrier will be lowered, and under compressive strain the barrier will be raised. However, variations at the two ends of NW caused by change in band structure are identical, which cannot switch the I-V characteristics of the device from linear Ohmic type to nonlinear rectifying type. This is the conventionally-known piezoresistive effect[46].

2.1.3 Piezopotential distribution in doped semiconductor NW

It is also important to point out that the above results are all based the assumption that there are no free charge carriers in the materials[28]. The as-synthesized ZnO nanostructures are, however, intrinsically *n*-type with a typical donor concentration of $1\times10^{17}cm^{-3}$ [47]. Taking into account the statistical electron distribution, the distribution of piezopotential in a bent ZnO NW (of which the dimension is not too small) with moderate charge carrier density can be calculated, showing that free electrons tend to accumulate at the positive piezopotential side of the NW at thermal equilibrium[48]. Therefore, the effect of negatively charged carriers is partially, if not all, screening the positive piezopotential, while no change to the negative piezopotential can be observed. Figure 6 shows the calculated piezopotential when the donor concentration in the ZnO NW is $1\times10^{17}cm^{-3}$, which clearly presents the screening effect of finite donor concentration on the distribution of piezopotential[48]. The piezopotential maximum in the positive side is significantly reduced from ~0.3 V in Figure 6d, which corresponds to the case when ZnO in assumed to be insulating, to less than 0.05 V in Figure 6b, which

considers the moderate doping in ZnO. Meanwhile it can be seen clearly that the induced piezopotential in negative side is very well preserved[48]. This is also consistent with the experimental observation that only negative pulses can be observed in an AFM based nanogenerator experiment using *n*-type ZnO NWs and the output negative potential peak appears only when the AFM tip touches the compressed side of the NW[32]. For even smaller systems, strong confinement effect requires quantum mechanical considerations due to discrete bound states in the materials. In such a case, an elaboration in theory similar to two-dimensional-electron-gas (2DEG) in GaN/AlGaN high-electron-mobility-transistors (HEMTs) is necessary for investigating the effect of piezopotential[49].

In addition to the *n*-type doping normally observed for as-synthesized ZnO NWs, it is also possible to receive stable *p*-type ZnO NWs[50-52]. The stability of *p*-type doping in ZnO NWs is possible due to the dislocation free volume and the presence of high concentration of vacancies near the surface of the NWs[53]. The distribution of piezopotential in a bent *p*-type ZnO NW has also been theoretically investigated previously. With a finite *p*-type doping, the holes tend to accumulate at the negative piezopotential side. The negative side is thus partially screened by holes while the positive side of the piezopotential preserves. For a typical ZnO NW with diameter of 50 nm, length of 600 nm and acceptor concentration of $1\times10^{17}cm^{-3}$ under a bending force of 80 nN, the piezopotential in the negative side is ~ -0.05 V and is ~ 0.3 V at the positive side (Figure 7). This suggests that the piezopotential in *p*-type ZnO NW is dominated by the positive piezopotential at the tensile side of surface[50].

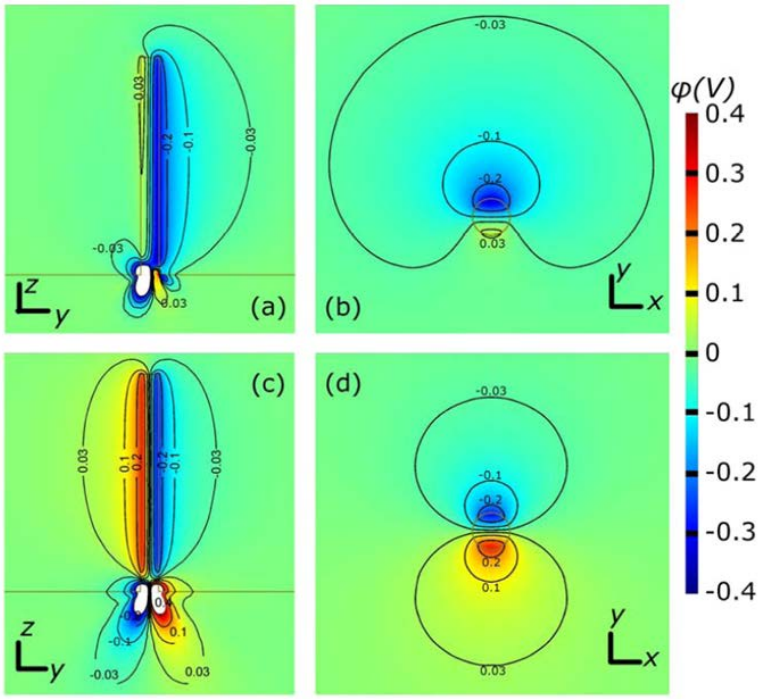


Figure 6. Numerical calculation results of the piezopotential distribution in a ZnO NW considering finite doping with donor concentration of 1×10^{17}cm^{-3}. The dimension of the NW is: a = 25 nm, l = 600 nm and the external force is f_y = 80 nN. (a) Piezopotential distribution of the cross section at x = 0. (b) Cross section plot of the piezopotential at z = 400 nm. (c and d) Calculation results for the case without considering the doping inside ZnO NW. (c) shows the cross section plot of piezopotential at x = 0. (d) shows the cross section plot of the piezopotential at z = 400 nm[48].

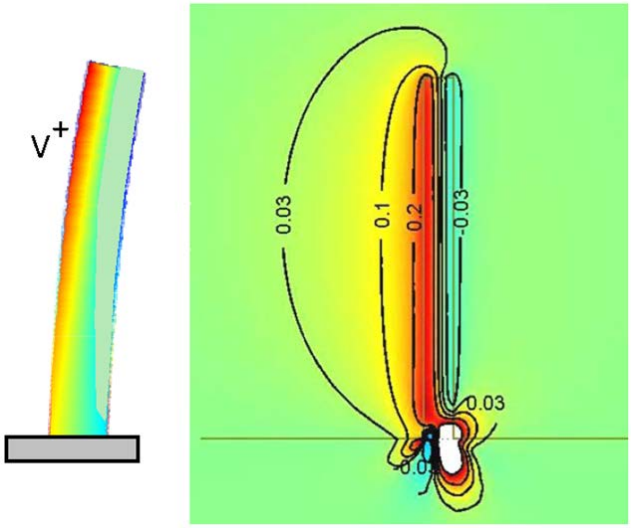


Figure 7. Calculated distribution of piezopotential in a *p*-type ZnO NW when transversely deflected[50].

2.2 Piezotronic effect

Due to the coupling of piezoelectric and semiconducting properties, nano/micro-wires of piezoelectric semiconductor have been used as basic building blocks for fabricating various innovative devices, such as nanogenerators[32,41,42], piezoelectric field effect transistors[54] and piezoelectric diodes[55]. When a strain is applied along the ZnO NW which grows in the *c*-axis direction, piezoelectric charges created at its two ends induce the piezopotential inside the NW. This potential is capable of modulating characteristics of the contact formed between the NW and the electrodes by modifying the height of local Schottky barrier[29]. Consequently, the transport of charge carriers in the device can be tuned by the externally applied strain. This is the piezotronic effect[13,29,56]. Electronics fabricated by using the inner-crystal piezopotential as a "gate" voltage to modulate the charge transport across a metal-semiconductor interface or a *p*-*n* junction is named piezotronics, which is different from the basic design of CMOS field effect transistor (FET) and has potential applications in force/pressure triggered/controlled electronic devices, sensors, micro-electromechanical systems (MEMS), human-computer interfacing and nanorobotics. A better understanding of piezotronic effect can be obtained by comparing it with the fundamental concepts and device structures in conventional semiconductor physics, which is to be elaborated in details in the following sections.

2.2.1 Effect of piezopotential on metal-semiconductor contact

Metal-semiconductor (M-S) contact is a fundamental and vital structure of virtually all semiconductor materials based electronic and optoelectronic devices[57]. When metal and semiconductor come into contact to form a M-S interface, a significant redistribution of charge takes place due to the overlap of wave functions from both the metal and semiconductor[58]. When the system reaches thermal equilibrium, Fermi levels on either side of the interface must be aligned and thus a net charge transfer will occur at the interface. If the electron affinity of the semiconductor $e\chi$ (relative to free electron

energy or vacuum level E_0) is appreciably smaller than the work function of metal $e\phi_m$, then electrons will be transferred from the metal into the semiconductor, resulting in the formation of an abrupt discontinuity or energy barrier at the interface (Figure 8), which is the Schottky barrier with barrier height of $e\phi_{SB}$. Ideally, the intrinsic Schottky barrier height (SBH) can be determined by (for *n*-type semiconductor)

$$e\phi_{SB} = e(\phi_m - \chi) \quad (9)$$

Due to the fact that charge is depleted from the metal/semiconductor interface into the bulk of the semiconductor, the intrinsic band bending ϕ_i in the semiconductor is given by

$$e\phi_i = e(\phi_m - \phi_s) \quad (10)$$

This region of band bending, in which the charge is modified from that in the bulk semiconductor, is called the depletion or space-charge region. SBH is a measure of the mismatch of energy levels for majority carriers across the M-S interface, which dictates the transport of charge carriers across M-S interface and is, therefore, of vital importance to successful operation of related semiconductor device. Current can only pass through the barrier if the externally applied positive bias on the metal is larger than the threshold value ϕ_i (for *n*-type semiconductor).

If the semiconductor material also possesses piezoelectric property, once a strain is induced in the semiconductor, the negative piezoelectric polarization charges and hence the negative piezopotential induced at the semiconductor side near the interface can repel the electrons away from the interface, resulting in further depleted interface and increased local SBH (Figure 9b); on the other end, if the polarity of induced strain is reversed, the positive piezoelectric polarization charges and hence the positive piezopotential created at the semiconductor side near the interface can attract the electrons towards the interface, resulting in less depleted interface and hence decreased local SBH (Figure 9c)[29,59].

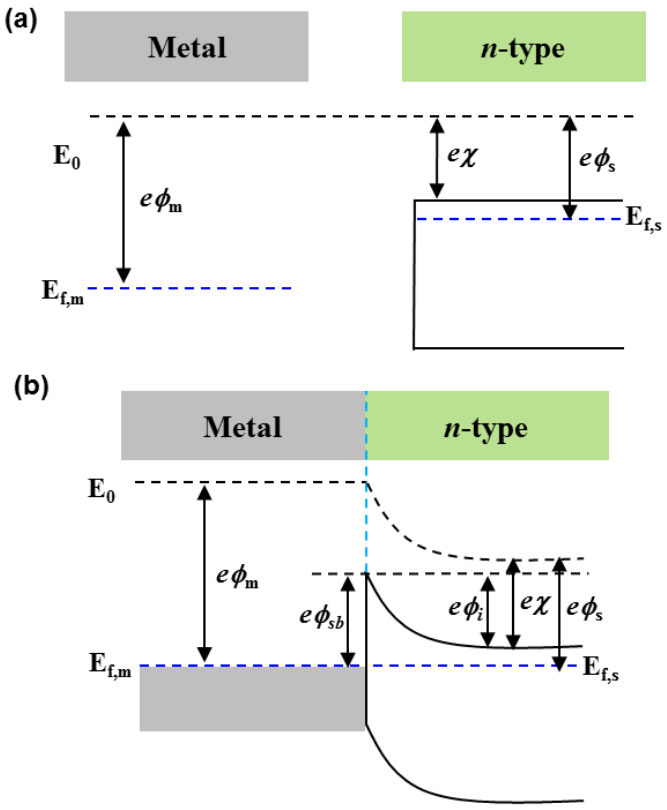


Figure 8. Schematic of an ideal metal/semiconductor contact. (a) Before forming the contact. (b) Creation of Schottky barrier after metal and semiconductor form close contact.

It is well-known that transport of charge carriers across the Schottky barrier is sensitively dictated by the SBH[58]. Small amount of change in SBH can be amplified and reflected in the transport characteristics of the device approximately through the exponential relation. It can therefore be seen from the band-diagrams shown in Figure 9 that piezopotential is able to effectively modulate the local contact characteristics through an internal field, depending on the crystallographic orientation of the piezoelectric semiconductor material and the polarity of the applied strain[29]. Consequently, the transport of charge carriers across the M-S contact can be effectively modulated by the piezoelectric polarization charges, or more specifically, the local contact characteristics can be tuned and controlled by varying the magnitude and polarity of externally applied

strain. The modulation/gating of the charge transport across the interface by the strain-induced piezopotential is the core of piezotronics[29].

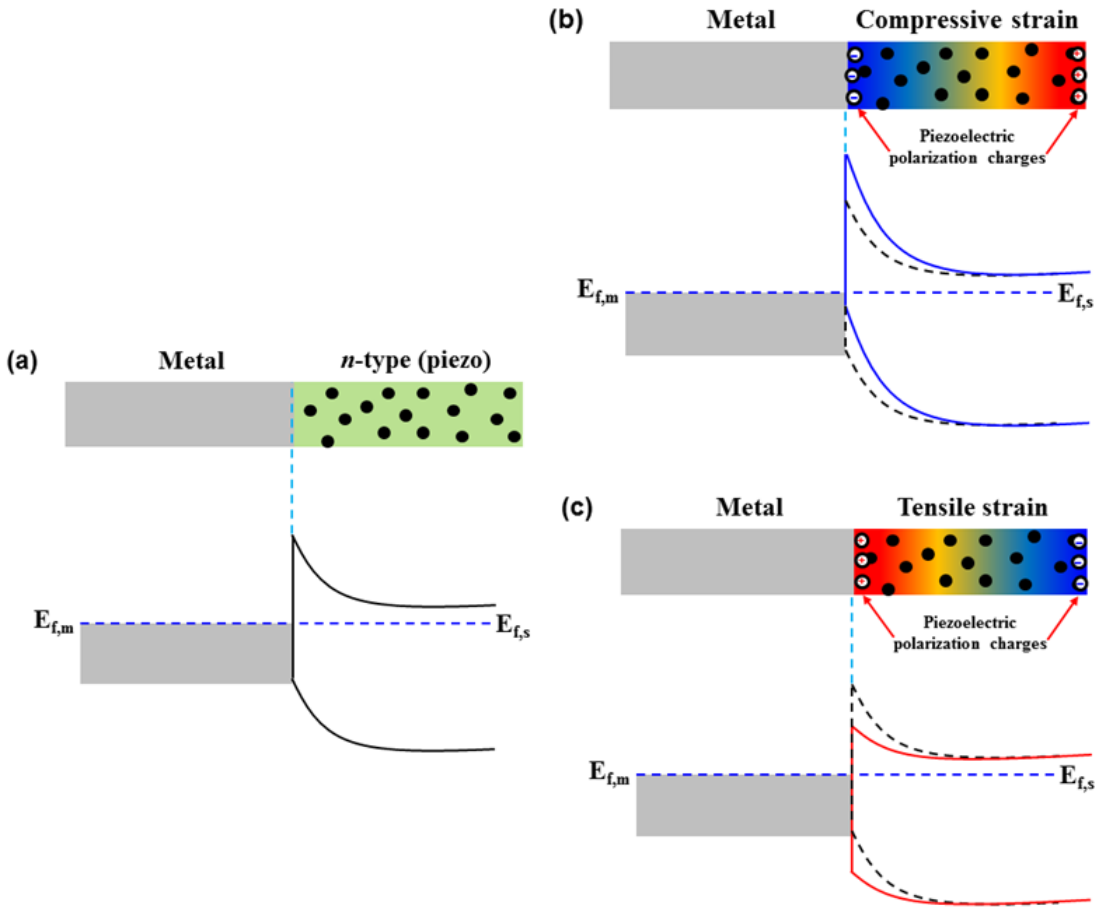


Figure 9. Schematic of energy diagram illustrating the effect of piezopotential on modulating the metal-semiconductor characteristics. (a) Schottky barrier induced at the interface between metal and n-type piezoelectric semiconductor material, without strain applied. Black dots represent the free charge carriers in the bulk semiconductor. (b) With compressive strain applied, the negative piezoelectric polarization ionic charges induced near the interface (symbols with "-") increases the local SBH. (c) With tensile strain applied, the positive piezoelectric polarization ionic charges induced near the interface (symbols with "+") decreases the local SBH. The color gradients in (b) and (c) indicate the distribution of piezopotential, with red representing positive piezopotential and blue representing negative piezopotential[59]. The band diagrams for the M-S contact with and without the presence of piezotronic effect are shown using red solid and black dashed curves, respectively.

2.2.2 Effect of piezopotential on *p*-*n* junction

A *p*-*n* junction consists of two semiconductor regions with opposite doping type is another fundamental building block in modern electronics and optoelectronics[60]. When *p*-type and *n*-type semiconductors form a junction, the holes on the *p*-type side and the electrons on the *n*-type side adjacent to the metallurgical junction tend to diffuse across the junction into the *n*-type/*p*-type region where few holes/electrons are present and redistribute to balance the local potential and reach thermal equilibrium. This diffusion process leaves ionized donors or acceptors behind, creating the charge depletion zone close to the junction which is depleted of mobile carriers (Figure 10b). The ionized donors and acceptors induce an electric field which in turn results in the drift of charged carriers, moving in the opposite direction to that of diffusion process. The diffusion of carriers continues until the drift current balances the diffusion current, thereby reaching the thermal equilibrium of the system, as indicated by the aligned Fermi energy across the system (Figure 10b). As per the discussions on piezopotential in previous sections, the presence of such a carrier depletion zone can significantly enhance the piezotronic effect, due to the fact that the piezoelectric polarization charges and hence the piezopotential, if induced, will be preserved without being screened by regional residual free carriers, of which the amount is negligible in the charge depletion zone[29].

Based on the above concepts, we can proceed to investigate how the presence of piezopotential can affect the characteristics of a *p*-*n* junction and consequently the operation of *p*-*n* junction based devices such as transistors, solar cells or light-emitting diodes (LEDs). To start with, the *p*-*n* junction is assumed to be homojunction in which the bandgaps for both *p*- and *n*-type materials are same. Meanwhile, only the *n*-type material is piezoelectric. More complicated situations involving *p*-*n* heterojunctions (in which the bandgaps for both *p*- and *n*-type materials are different) will be discussed later. Similar discussions can also be easily extended to cases including *p*-type piezoelectric semiconductor materials.

Once strain is induced in the *n*-type semiconductor, the positive piezoelectric polarization charges and hence the positive piezopotential induced in the *n*-type region close to the junction interface can attract the electrons towards the interface, resulting in the trapping or accumulation of electrons adjacent to the interface and thus a dip in the local band profile (Figure 10c)[29]. This modification of local band can be effective for trapping electrons so that the electron-hole recombination rate can be largely enhanced in the device, which turns out to be beneficial for improving the efficiency of LED applications[61]. Furthermore, the inclined band profile can also modulate the mobility of charged carriers moving toward the junction. On the other end, if the polarity of induced strain is reversed, the negative piezoelectric polarization charges and hence the negative piezopotential created in the *n*-type region close to the junction interface can repel the electrons away from the interface, resulting in the depletion of electrons adjacent to the interface and thus a shoulder in the local band profile (Figure 10d)[29]. This consequent modification of local band may result in suppression of electron-hole recombination rate in the device, which could be detrimental for related optoelectronic applications[61].

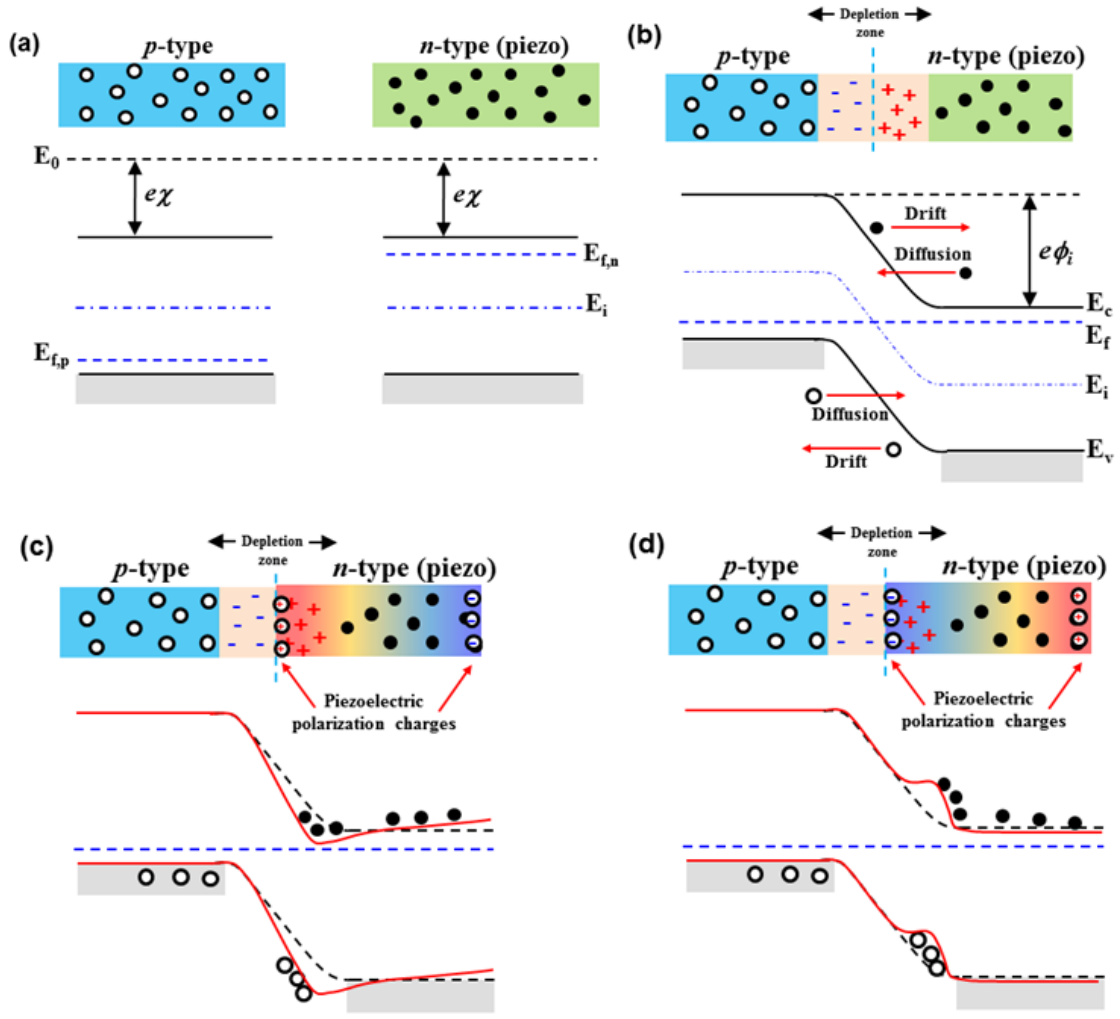


Figure 10. Schematic of energy diagram illustrating the effect of piezopotential on modulating characteristics of *p*-*n* homojunction. (a) Before the contact/junction is formed. Black dots and empty circles represent the free charge carriers in semiconductor. $E_{f,\,n}$ and $E_{f,\,p}$ are the Fermi levels in *n*-type and *p*-type materials respectively. E_0 and E_i are the vacuum level and intrinsic Fermi level. (b) Charge depletion regions forms when thermal equilibrium of the system is reached. Symbols "+" and "-" represent the ionized donors and acceptors in respective regions. (c) and (d) With strain applied, the piezoelectric polarization ionic charges are induced near the junction interface. The color gradients in (c) and (d) indicate the distribution of piezopotential, with red representing positive piezopotential and blue representing negative piezopotential[59]. The band diagrams for the *p*-*n* junction with and without the presence of piezotronic effect are shown using red solid and black dashed curves, respectively.

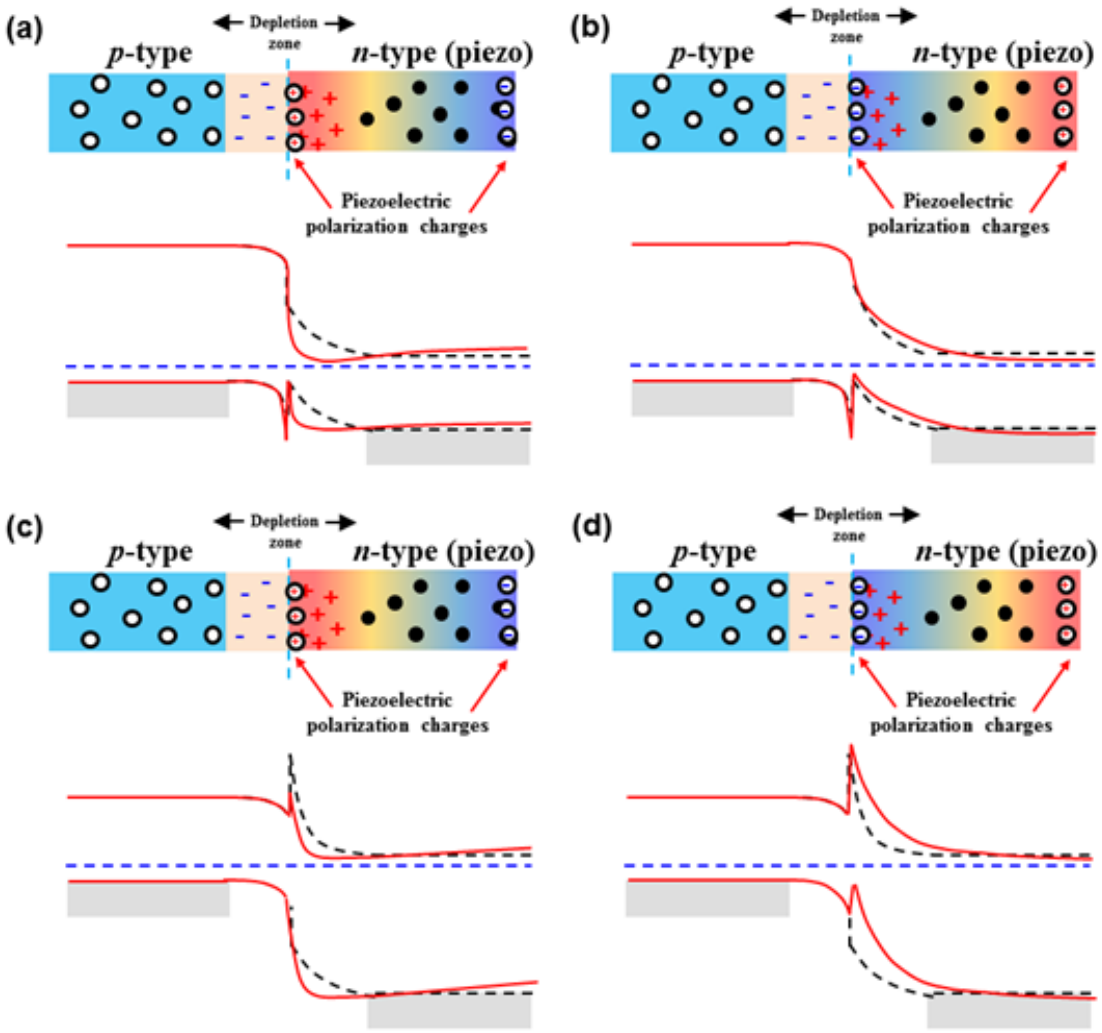


Figure 11. Schematic of energy diagram illustrating the effect of piezopotential on modulating characteristics of *p*-*n* heterojunction. In (a) and (b), *p*-type semiconductor material has larger bandgap than *n*-type piezoelectric semiconductor material. (a) Positive piezoelectric polarization charges are induced near the junction interface and (b) negative piezoelectric polarization charges are induced near the junction interface. In (c) and (d), *p*-type semiconductor material has smaller bandgap than *n*-type piezoelectric semiconductor material. (c) Positive piezoelectric polarization charges are induced near the junction interface and (d) negative piezoelectric polarization charges are induced near the junction interface. The band diagrams for the *p*-*n* junction with and without the presence of piezotronic effect are shown using red solid and black dashed curves, respectively.

Optoelectronics devices as well as practically all other semiconductor devices made from compound semiconductor materials always incorporate heterojunctions[62]. For

p-n junction made of two semiconductor materials with distinctly different bandgaps, local piezoelectric polarization charges can also effectively modulate the band profile, as shown in Figure 11[13]. Consequently the charged carriers transport across the junction interface can be significantly modified. Figure 11 considers two possible cases of type I heterojunctions for investigating the effect of piezoelectric polarization charges on *p-n* heterojunction. In Figure 11 (a) and (b), discontinuity occurs in valence bands while discontinuity occurs in conduction bands in Figure 11 (c) and (d). If strain is induced in the *n*-type semiconductor, the positive piezoelectric polarization charges and hence the positive piezopotential induced in the *n*-type region can reduce the barrier height at the interface created by band misalignment so that the electrons can be effectively transported across the interface, or resulting in the trapping or accumulation of electrons adjacent to the interface and thus a dip in the local band profile (Figure 11a and c)[29]. On the other end, if the polarity of induced strain is reversed, the negative piezoelectric polarization charges and hence the negative piezopotential created in the *n*-type region can repel the electrons away from the interface, resulting in the depletion of electrons adjacent to the interface and thus increase of height and width of the barrier at the interface (Figure 11b) or even additional discontinuity in band profile (Figure 11d)[29].

It is therefore evident that the presence of piezoelectrically induced polarization charges at the *p-n* junction can effectively modify the local band profile and consequently modulate the transport, separation or recombination of charged carriers in the device. By varying either the magnitude of polarity of applied strain, the efficiency of carrier transport, separation or recombination can be effectively tuned. By introducing photon excitation to the context, a coupling among semiconductor properties, photon excitation and piezoelectricity of the materials engenders a new field of research called piezo-phototronics[13]. Although research on piezo-phototronics and related applications will not be the focus of this thesis, it is still worthwhile briefly introducing the concept here. The piezo-phototronic effect is the tuning and modulation of charge carrier generation,

separation or recombination at a *p-n* junction by the strain-induced piezopotential[29], which has been effectively utilized to improve the performance of LEDs, solar cells and photon detectors[61,63,64].

2.3 Summary

The basic physics and fundamental concepts of piezotronics have been discussed in details. The role anticipated to be played by piezotronics in the era of "Beyond Moore's law" is similar to mechanosensation in physiology which provides a direct/active "interfacing" between CMOS technology and human/ambient[19].

The core of piezotronics relies on piezopotential which is induced in a piezoelectric semiconductor material upon straining and generated by the polarization of ions in the crystal. *Piezotronics* is about the devices fabricated using the piezopotential as a "gate" voltage to modulate/control charge carrier transport at a contact or junction. It is prospected that piezotronics will present a paradigm shift for developing revolutionary technologies for force/pressure triggered/modulated electronic devices, sensors, MEMS, human-computer interfacing, nanorobotics, active flexible electronics, solar cell, photon detector and light emitting diodes[13]. The role played by piezotronics in interfacing human-CMOS technology is similar to the mechanosensation in physiology.

CHAPTER 3

RATIONAL SYNTHESIS OF ZINC OXIDE NANOWIRE AND ARRAY

Since the successful synthesis of oxide semiconductor nanobelts in 2001[65], low-dimensional nanostructured functional oxide materials have attracted enormous attentions and research efforts. Among the various functional oxide materials, ZnO exhibits an abundance of novel nanostructures which can be derived by selectively modulating the growth rates along different crystallographic directions, mainly $<2\bar{1}\bar{1}0>$, $<01\bar{1}0>$ and $\pm[0001]$[66]. ZnO nanostructures such as nanobelt, nanowire (NW), nanosprings, nanohelix and nanoring[65,67,68] have demonstrated significant potential in applications such as sensing, optoelectronics, detector, catalysis and energy harvesting due to the shape induced unique electrical and optical properties[41,69-73]. ZnO nanobelts and NWs, of which the growth is dominated by either non-polar surfaces $\{01\bar{1}0\}$, $\{2\bar{1}\bar{1}0\}$ or polar surfaces $\{0001\}$, are the two most common one-dimensional (1D) ZnO nanostructures investigated for applications[74]. Synthesis of ZnO nanostructures in controllable and repeatable manners is crucial for fabricating related nanodevices and achieving the prospected novel applications, such as piezotronic devices and integrated systems investigated in this thesis. In this chapter, rational synthesis of individual free-standing ZnO NWs as well as patterned ZnO NW arrays via various routes, specifically the physical-vapor-deposition (PVD) methods based on vapor-solid-solid (VSS), vapor-solid (VS) and pulsed laser deposition (PLD) processes as well as the solution-phase method based on hydrothermal (HT) decomposition, will be discussed in details, with a focus on the development of wafer-scale high-throughput ordered growth of vertically aligned ZnO NWs array based on HT method. Each technical method has its own target applications as well as limitations. Individual free-standing ZnO NWs synthesized by VS

methods are feasible for fabricating single-NW based devices and investigating fundamental properties of these novel applications[11,30,31,75]. VSS process has been employed for achieving aligned ZnO NWs with good crystallinity and other properties on various substrates, such as sapphire[76], GaN[77,78] and AlGaN/AlN[79]. PLD technique has been utilized for synthesizing ZnO NWs array with adjustable dopant type, doping level and band-gap engineering, which paves routes for simultaneously controlling the doping concentration and band-gap tuning of ZnO NWs for high-efficiency optical/electronic applications[80,81]. The chemical solution-based HT method, on the other hand, enables fabrication of large-scale ZnO NWs array on various substrates, especial flexible polymer substrates, at low temperatures and low cost[27,82,83].

3.1 Physical-vapor-deposition (PVD) method

Crystallization from vapor phase has been widely utilized for forming 1D nanostructures due to the fact that transportation and concentration control of the constituent substances are relatively easy. Three primary mechanisms of NW nucleation and growth from vapor phase are generally acknowledged in the community: the vapor-solid (VS), vapor-liquid-solid (VLS) and vapor-solid-solid (VSS) processes. The following sections will focus on mechanisms and results of synthesizing ZnO NWs based on VS and VSS processes.

3.1.1 Vapor-solid (VS) process

Although the exact mechanism for 1D growth of nanostructures directly from vapor phase is still under debate, vapor-solid process has been widely investigated and explored for synthesizing 1D oxide nanostructures without using catalyst[84,85]. The efforts for investigating 1D microstructures derived from VS process date back to the research on growing single-crystalline whiskers in 1950s[86], while the subsequent endeavors in both theory and experiment on kinetic growth of whiskers are recognized to inspire and guide the tremendous upsurge of interests in synthesizing 1D nanostructures since

1990s[87-89]. In a typical vapor-solid process, the vapor sources for deposition and growth can be obtained by thermal vaporization, chemical reduction, laser ablation and other methods. These vaporized sources can then be transported to receiving substrates in low-temperature zones by carrier gas and deposited on the substrates. It is widely accepted that VS crystallization process is a kinetically-driven anisotropic one. Based on previous experimental and theoretical research on the kinetics of whisker growth[87,88], the two-dimensional (2D) nucleation probability (P_N) on the surface of NW can be expressed as:

$$P_N = B\exp(-\frac{\pi\sigma^2}{\kappa^2 T^2 \ln\alpha}) \quad (11)$$

where B is a constant, σ is the surface energy of NW, k is the Boltzmann constant, T is the absolute temperature and α is the super-saturation ratio[87]. It can be seen from the above expression that when surface energy of NW decreases, the probability of 2D nucleation increases. Meanwhile, atoms on the low-energy surfaces possess lower binding-energy and hence correspondingly lower absorption probability for accommodating vapor source atoms which subsequently arrive at these surfaces. It can also be known from the above relation that higher temperatures and larger super-saturation ratios favor the 2D nucleation, which facilitates the growth of thin-film structures rather than 1D nanostructures. As can be seen from later experimental results, temperature and super-saturation ratio are the two dominant factors which can be manipulated to control the morphology of as-grown materials in VS process. The initial stage of VS growth is generally considered as a “self-catalytic” process, in which no catalysts are required for forming 1D nanostructures. Specifically, a proposed mechanism for growing ZnO nanostructures via VS process is depicted in Figure 12[90], in which the ZnO molecules vaporized at high-temperature zone of the horizontal tube furnace are transported to substrates in low-temperature zones by carrier gas and condensed onto the substrates (Figure 12a). The cations and anions are arranged in such a way to minimize the system

energy that proper cation-anion coordination is preserved and local charge neutrality as well as structural symmetry is balanced, with nucleus formed locally, as shown in Figure 12b. Subsequent arriving vaporized sources are continuing to deposit on the existing nucleus while local vapor super-saturation is maintained (Figure 12c). Finally, due to the fact that the imperfect structure of growth fronts favors the rapid accumulation of arriving source molecules, anisotropic 1D growth occurs with time (Figure 12d).

A typical VS process for synthesizing dispersed long free-standing ZnO NWs investigated in this thesis is carried out without using metallic catalysts. Briefly, 3 grams of ZnO powder (Alfa Aesar, 99.99%) are placed in the central zone of the alumina horizontal tube furnace (Thermolyne 79500) as the reaction source. The flow rate of carrier gas (Argon) is 50 standard cubic centimeter per minute (sccm). The pressure inside the tube is maintained at 0.09868 atm throughout the synthesis process. Alumina plates placed at a distance of 18-20 cm away from the ZnO source at the downstream side function as the substrates for depositing and growing ZnO NWs. The furnace is heated up to 800 ^{o}C at a rate of 50 ^{o}C. After 10 minutes at 800 ^{o}C, the temperature is ramped up at a rate of 20 ^{o}C to 1475 ^{o}C, which is the temperature synthesis reaction occurs at. After typical growth duration of 2 hours, the dimension of as-synthesized ZnO NWs with hexagonal structure is normally around tens to a few hundred μm in length and a few hundred nm to a few μm in diameter, as shown in Figure 12e. The relatively large dimension of the as-grown dispersed ZnO NWs obtained via VS process makes it feasible to manipulate these NWs for fabricating single-NW based nanogenerators[91], biochemical sensors[92], optoelectronic detectors[93] as well as piezotronic devices[10,11] (details of related piezotronic applications will be discussed in corresponding chapters of this thesis).

In the VS growth, control of NW diameter is accomplished mainly by adjusting the evaporation and synthesis temperature, as well as the vapor pressure inside the reaction tube. While fabrication of various hierarchical semiconductor nanostructures through the

VS growth has been reported in the literature[44,90,94,95], no tight control of the spatial arrangement and nucleation site has been achieved thus far and the exact mechanisms responsible for VS growth are still not completely elucidated.

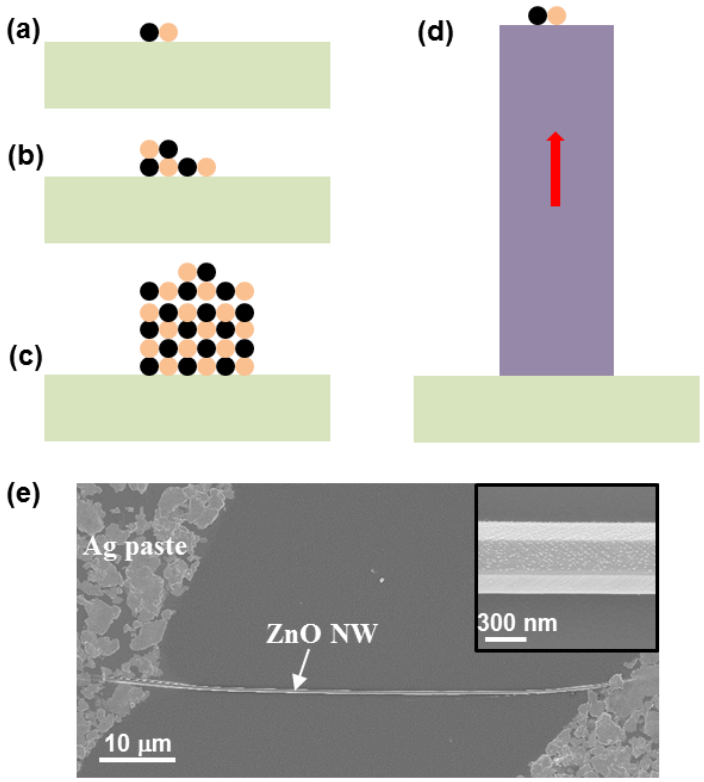


Figure 12. (a-d) A proposed growth mechanism for ZnO nanostructure via VS process. Adapted from [90]. (e) A single-NW device fabricated by forming contacts between the as-synthesized ZnO NW and metal electrodes (Ag paste). Inset: magnified view of the ZnO NW, which clearly shows the facets of the as-grown hexagonally structured NW. Scale bars: 10 μm for (e) and 300 nm for the inset.

3.1.2 Vapor-solid-solid (VSS) process

Growth of 1D ZnO nanostructures can be optimized, in terms of controlling the nucleation site and dimensions of the as-grown structures, by introducing metal catalysts into the process. The mechanism of synthesizing metal-catalyzed ZnO NWs array by thermal deposition process was conventionally believed to be *via* the "vapor–liquid–solid" (VLS) process, which was initially demonstrated and proposed back to 1960s by

Wagner *et al* for explaining the growth and morphology of whiskers[96,97]. VLS process starts with the dissolution of gaseous precursor materials in the molten droplets of catalyst metal, followed by nucleation and subsequent growth of 1D single-crystalline structure on the substrates. A suitable operating temperature range can be chosen for metal catalyst to absorb the vapor sources and form eutectic compounds, according to the pseudo-binary phase diagram between the metal and the material for NW growth[98]. The carrier gas transporting the growth material flows through the reaction tube, and the continuous dissolution of precursor materials into the liquid droplet leads to super-saturation of the materials. Consequently, crystal growth occurs at the solid-liquid interface by precipitation of precursor materials. This process was later justified thermodynamically and kinetically[99], and recently re-investigated and utilized to fabricate NWs from a wide variety of inorganic materials[76,98,100]. Many groups worldwide subsequently adopted similar methods for synthesizing aligned ZnO NW arrays on various substrates[101-103].

The recent in-depth investigation on growth process of ZnO NWs array through thermal vapor deposition, whereas, reveals the growth mechanism for Au-catalyzed process (which is utilized and investigated in this thesis) is vapor-solid-solid (VSS) process rather than VLS process[104]. It is discovered that lattice parameters of Au catalyst remain constant from samples exposed to ZnO vapor source and control samples, indicating that Au catalyst has not formed alloy with zinc since solid solutions of solute atoms in a solvent lattice will alter the lattice parameters for both interstitial and substitutional solid solutions. In addition, the operation temperature for growing ZnO NWs using Au catalyst is at 800~960 ºC, much lower than the melting point (~1031 ºC) of 33 nm pure Au nanoparticles[105]. Au nanoparticles are found to be larger than 30 nm in diameter at the synthesis temperature for growing Au-catalyzed ZnO NWs[104], and it is well-known that melting temperature of Au nanoparticles decreases with decreasing

particle size[105]. In addition, the maximum possible Zn content in Au nanoparticles under the experimental conditions has been determined as1.3 at%[104], which leads to the fact that melting temperature of Au nanoparticles with1.3 at% Zn is ~1015ºC according to the Au-Zn phase diagram[106], still much higher than the operation temperature for growing ZnO NWs using Au catalyst. Moreover, *in situ* XRD technique has been utilized to reveal the status of Au catalyst particles in the growth process[104], revealing that Au {111} reflection is clearly present at all elevated temperatures up to1018 ºC, which indicates that Au nanoparticles do not melt up to 1018 ºC. All of these results confirm the absence of Zn in Au nanoparticles during the growth and suggest that Au-catalyzed growth of ZnO NWs via thermal deposition could be a VSS process which involves the surface diffusion of Zn rather than the bulk diffusion. Actually, VSS process has been reported previously in Al-catalyzed Si NWs[107] as well as Au-catalyzed InAs and GaAs NWs[108,109], while Sn-catalyzed growth of ZnO NWs array via thermal deposition has been suggested to be a VLS process[104].

A typical VSS process for synthesizing aligned ZnO NWs array investigated in this thesis is carried out using Au catalysts. Briefly, undoped 2 μm thick *c*-plane oriented GaN film grown on sapphire wafer is used as substrate, due to the match of crystal orientation and lattice parameter between GaN and ZnO. A thin layer of Au (5-6 nm) is coated on GaN via plasma sputtering to serve as the catalyst. The mixture of 0.5 g ZnO power (Alfa Aesar, 99.99%) and 0.5 g graphite power (Alfa Aesar, 200-mesh, 99.9999%) are used as source materials and put into an alumina boat. Then the boat is placed in the central zone of the alumina horizontal tube furnace (Thermolyne 79300), and the substrate is placed 5-6 cm away from the source material on the downstream side. After pumping the system down to 5×10^{-2} mbar, a premixed gas (Ar and O_2) is introduced into the system at a flow rate of 50 sccm to bring the pressure to 160 bar. The furnace is then heated to 960°C at a heating rate of 50°C /min and the temperature is held at the peak temperature for 30

minutes, which is the growth duration. Finally, the system is slowly cooled down to room temperature at a rate of 50°C /min under flow gas. After typical growth duration of 30 minutes, the dimension of as-synthesized ZnO NWs is normally around tens of nm in diameter and tens of μm in length, as shown in Figure 13a. These well-aligned as-grown ZnO NWs array obtained via VSS process have found applications in direct-current nanogenerators[32,41] and solar cells[110].

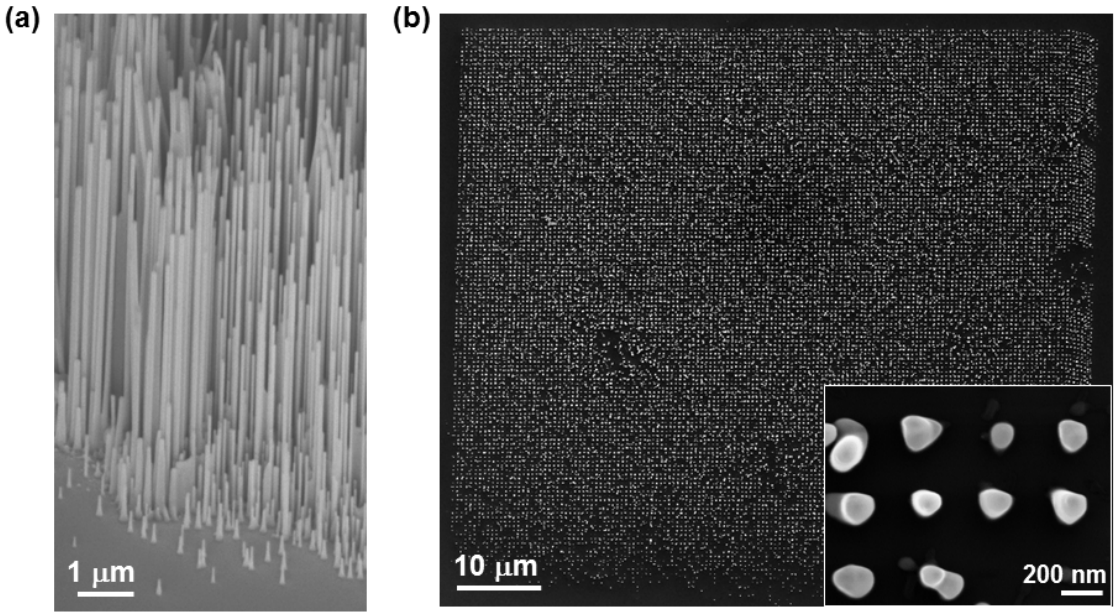


Figure 13. (a) Tilted-view (30 ^{o}) of vertically-aligned ZnO NWs array grown via VSS process. (b) Top view of site-specific growth of vertically-aligned ZnO NWs array via VSS process. Inset: zoom-in view of the as-grown samples. Images in (b) by courtesy of Dr. Y. G. Wei.

It has been demonstrated that size of the catalyst directly affects the cross-section of the resultant 1D nanostructures[67,111]. Additionally, site-specific growth is possible in VSS process since catalyst acts as the preferential sites for nucleation and growth of NWs, allowing for patterned arrays of vertically-aligned1D nanostructures to be synthesized. Preliminary results of such attempt can be seen in Figure 13b, in which the Au catalyst was patterned by electron beam lithography (EBL), and the demonstrated control over

dimension, location, and density of the as-grown ZnO NWs array exhibits potential for future applications.

Although single crystalline as-grown ZnO NWs array with few defects can be obtained by the above process, which enables the realization of potential high-performance electronic and optoelectronic applications[76], there are still several issues to be addressed and elucidated. Possible influence of Au incorporated on the properties of NWs is under investigation. Besides, substrate materials are still limited to those which can sustain substantially high temperature and possess matching orientation and lattice parameters. Moreover, the throughput and yield are largely constrained by the size and load capacity of the reaction tube. Finally, it is still difficult to synthesize 1D nanostructures with complex components via VSS process.

3.1.3 Pulsed laser deposition (PLD) method

It is highly desirable to achieve controllable doping (especially *p*-type doping) and band-gap engineering in ZnO nanomaterials in order to realize all-ZnO-NW-based high performance electronic, optoelectronic and piezotronic devices[50,51,112,113]. Reliable and controllable doping for ZnO still remains difficult despite the numerous efforts devoted[114-116]. Pulsed laser deposition (PLD) has been a sophisticated technique for thin film deposition ever since its initial utilization in growing high-quality superconducting thin films[117,118]. PLD can be used for depositing a wide range of materials, such as ceramic oxides, nitride films and metallic films. A growing interest has been emerging in synthesizing semiconductor NWs using PLD technique[89,119-121] and in particular phosphorus doped $Zn_{1-x}Mg_xO$ NW arrays have been recently obtained by PLD method[80], exhibiting the possibility and capability of using PLD technique for synthesizing ZnO NWs array with adjustable dopant type, doping level and band-gap engineering, paving routes for simultaneously controlling the doping concentration and band-gap tuning of ZnO NWs for high-efficiency all-ZnO based optical/electrical applications and high-

output nanogenerators[50].

In a typical PLD process of synthesizing phosphorus doped $Zn_{1-x}Mg_xO$ NW arrays, a KrF excimer laser is used as the ablation source to focus on the ceramic target. ZnO nanostructures are deposited on Si (100) or polycrystalline quartz substrates with a typical growth time of 40 minutes. The key step for growing vertically aligned NWs is the *in situ* deposition of a textured ZnO buffer layer on the substrate before switching to synthesis of NWs. Parameters like substrate temperature, growth pressure, the flow ratio of respective gases, and laser repetition frequency dictate the morphology and other properties of the resultant NWs. When the same target is used ($Zn_{0.9}Mg_{0.1}O$:P (0.8 at%)), NWs with different doping levels and band-gaps can be achieved simply varying the growth pressure, flow ratio and laser repetition frequency, as shown in Figure 14. The obvious difference in the morphology and surface roughness of the as-grown NWs under different growth conditions indicate the phosphorus atoms are incorporated into the NW lattice at different levels, which induce the lattice distortion[80]. The shifts in the obtained photoluminescence (PL) spectra for as-grown samples suggest successful band-gap engineering. NWs obtained in Figure 14a possess larger band-gap compared to that of NWs in Figure 4b.

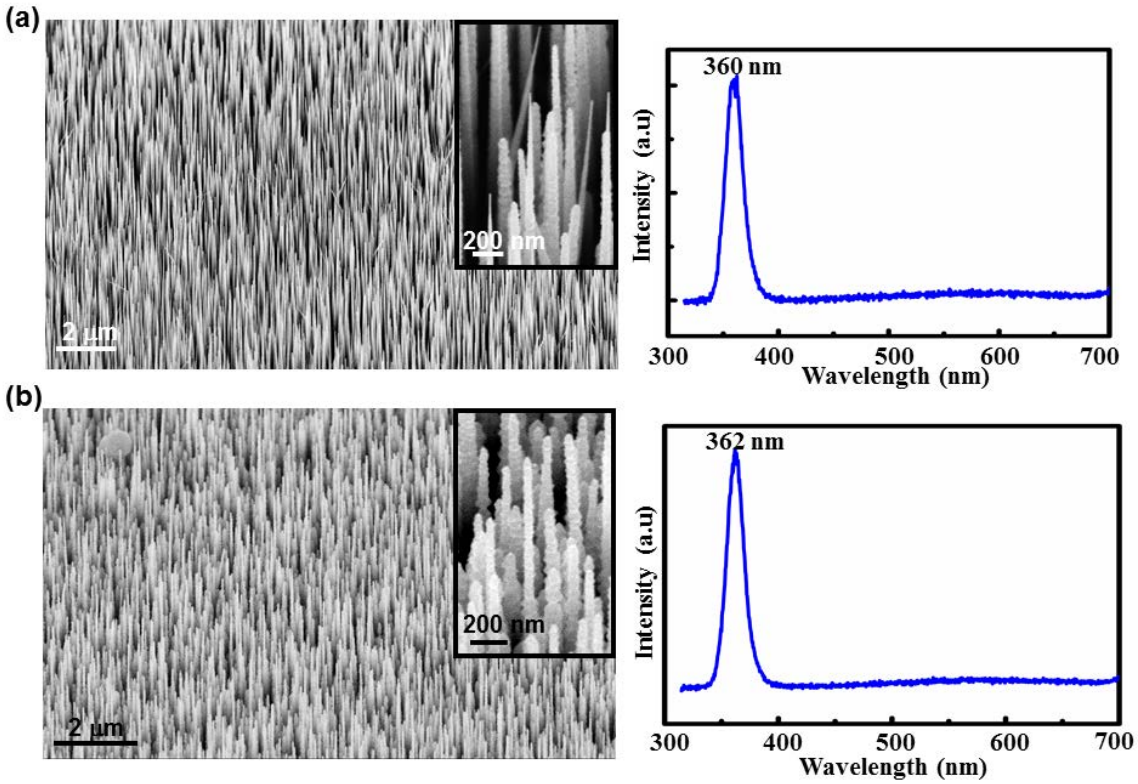


Figure 14. (a) Left: Tilted view of the as-grown NWs. The corresponding growth parameters are 795 ^{o}C, 4.5 Torr, Ar = 40 sccm, O_2 = 6 sccm, deposition time = 40 minutes, laser repetition frequency = 5 Hz. Right: PL spectra obtained for this sample. (b) Left: Tilted view of the as-grown NWs. The corresponding growth parameters are 795 ^{o}C, 4.1 Torr, Ar = 30 sccm, O_2 = 10 sccm, deposition time = 40 minutes, laser repetition frequency = 3 Hz. Right: PL spectra obtained for this sample. Images by courtesy of Dr. S. S. Lin.

Among all the available techniques for synthesizing ZnO NWs, PLD offer the best crystal quality and the least defects of the as-grown NWs. In addition, the capability of controlling the dopant type, doping level as well as band-gap engineering in the synthesized NWs by PLD is highly desirable in investigating and achieving not only all-ZnO-NW-based electronic and optoelectronic devices, but also the emerging piezotronic and piezophototronic applications[13,56,122]. However, due to the heating requirement, substrate materials are restricted to those which can sustain high temperature. The throughput and yield are also constrained by the size and load capacity of the reaction chamber and the reaction cycle time. In addition, as an emerging technique for

synthesizing nanostructures, the effects of interplay among the various experimental parameters and the underlying mechanisms are yet to be clearly elucidated.

3.2 Solution-phase hydrothermal (HT) method

The major disadvantages of high-temperature physical approaches to synthesize ZnO NWs include the high cost of fabrication, the incapability to be scaled-up and incompatibility with flexible polymer substrates. Recent progress using solution-phase techniques has resulted in the fabrication of ZnO NWs at high throughput via selective capping mechanisms, through the hydrolysis of zinc salts in the presence of amines under relatively mild conditions (i.e. low temperature and pressure)[123]. Following this work, hexamethylenetetramine (HMTA, formula $(CH_2)_6N_4$) has been used widely to synthesize dense arrays of ZnO NWs by thermal decomposition of methylamine and zinc nitrate in aqueous solution[124,125]. Most significantly, these oriented NWs can be prepared essentially on various kinds of substrates since the synthesis temperate is normally below 100 ^oC.

3.2.1 General growth mechanism

The main approach for achieving growth of 1D Wurtzite-structured ZnO NW is to exploit the difference in surface chemistry between the polar {0001} and non-polar {1010} and {1120} surfaces. By selectively promoting or suppressing growth on these facets, rational 1D growth can be achieved via solution-phase HT method. The dominant zinc species present varies in the aqueous system depending on the solution. The addition of amines to control the pH and morphology introduces additional zinc/amine complexes[126]. It is widely accepted that the following reactions take place in the aqueous systems for growing ZnO NWs via HT methods[127]:

$$(CH_2)_6N_4 + 6\ H_2O \leftrightarrow 4\ NH_3 + 6\ HCHO \qquad (12)$$

$$NH_3 + H_2O \leftrightarrow NH_3 \cdot H_2O \quad (13)$$

$$NH_3 \cdot H_2O \leftrightarrow NH_4^+ + OH^- \quad (14)$$

$$Zn^{2+} + 2\ OH^- \leftrightarrow Zn(OH)_2 \quad (15)$$

$$Zn(OH)_2 \rightarrow ZnO + H_2O \quad (16)$$

Briefly, zinc salt (e.g. zinc nitrate) provides Zn^{2+} ions for synthesizing ZnO NWs and water molecules in the solution supplies O^{2-} ions. The detailed role of HMTA, however, is still not clear and under debate. It is generally accepted that HMTA acts as a pH buffer and source slowly and steadily releasing hydroxide ions, which further react with Zn^{2+} to form zinc complexes[124]. HMTA gradually decomposes into formaldehyde and ammonia to release the strain energy built in the structure and meanwhile the ammonia creates the basic environment, thus facilitating the formation of zinc hydroxide, which subsequently undergoes dehydration and decomposes into ZnO. It is hypothesized that formation of ZnO NWs with high aspect ratios via the above process could be explained by preferential adsorption of non-ionic HMTA on the non-polar surfaces of the ZnO NWs, allowing the deposition of precursor zinc species onto the polar facets for continuous anisotropic growth[128].

3.2.2 Wafer-scale high-throughput ordered growth of vertically aligned ZnO NWs array

The wet chemical methods have been demonstrated as a very powerful technique for growing 1D ZnO nanostructures over various substrates; however, previously reported solution-phase synthesis provided poor control over the area density of the NWs and the as-grown NWs normally have smaller aspect ratios than those obtained by vapor-phase methods. Besides, the as-grown NWs suffer worse vertical alignment compared to those obtained by physical routes[76,80]. Assembly and integration of highly-ordered NW arrays

with decent properties at large scale on various substrates, especially the non-conventional flexible or degradable substrates, is essential for building multi-functional devices and systems[129-133].

Significant efforts have been previously devoted to assemble large quantity NWs through parallel processes, which can be grouped into two categories: grow-and-place (GAP) and grow-in-place (GIP). The GAP approach includes but is not limited to alignment induced by dielectrophoresis[134] and methods utilizing magnetic fields[135], microfluidic channels[136], electrostatic forces[137], molecular forces[138] and shear forces[139-141]. Although the GAP technique can be used to fabricate a finite number of devices, it is rather challenging to assemble the as-synthesized NWs into desired configurations at large scale. In GIP technique, on the other hand, nanostructures are synthesized *in-situ* at the pre-patterned catalyst/seed sites created through lithography, such as electron beam lithography (EBL)[125], nanoimprint lithography (NIL)[142], and nanosphere lithography (NSL)[76]. Engineering control over the growth substrate can guide the size, placement, and orientation of the as-grown NWs. Patterned growth of aligned ZnO NWs has also been achieved via HT method[125] and physical vapor deposition (PVD) method[76]. However, none of the above approaches provides a reliable, high-throughput, and low-cost solution for large-scale fabrication of patterned ZnO NWs array at a level required for practical applications.

Driven by the above application needs and challenges, an approach for patterned growth of vertically aligned ZnO NWs array with high-throughput and low-cost at wafer-scale has been explored[27]. Periodic patterns are generated using laser interference lithography on substrates coated with SU-8 photoresist. ZnO NWs are selectively grown through the openings via a modified low temperature hydrothermal method without using catalyst and with a superior control over orientation, location/density and as-synthesized morphology. Furthermore, a facile technique is developed to synthesize textured ZnO

seed layer for replacing single crystalline GaN and ZnO substrates, which extends the large-scale fabrication of vertically aligned ZnO NWs array onto substrates of other materials such as polymers, Si and glass. Details of this combined approach will be discussed in the following sections.

3.2.2.1 Fabrication process

To achieve controllable growth of highly-ordered and aligned ZnO NWs array with high-throughput and low-cost at large scale, it is necessary to adopt feasible combinations of patterning techniques and synthesis methods. Laser interference lithography (LIL) is a large-scale, fast, maskless and noncontact nanopatterning technique[143]. The patterns for synthesizing ZnO NWs array here are prepared by LIL of the photoresist, which is essentially a photochemical process similar to that routinely utilized in the state-of-art photolithography process. The epoxy-based negative photoresist SU-8, commonly used in microelectronics industry, is adopted in our experiment. The LIL technique can generate periodic patterns on the photoresist masklessly. When exposed, SU-8's long molecular chains cross-link, which cause the solidification of the exposed areas. After development, the exposed areas of SU-8 layer remained and served as the mask for the subsequent growth of ZnO NWs. The experimental setup for the laser interference patterning is shown in Figure 15a. A 10-ns pulsed Nd: YAG laser (Quanta-Ray PRO 290, Spectra Physics) with wavelength of 266 nm is used as the laser source. The primary laser beam (266 nm) is split into two coherent light beams (Figure 15a). Interference between the two beams forms a grating pattern (Figure 15b) on the photoresist layer under a single laser pulse (10 ns) irradiation. The period of the pattern line spacing d is determined by the wavelength (λ) of the light and the half-angle (θ) between the two incident beams through the relationship $d = \lambda/2\sin(\theta)$[143]. The sample is then rotated by 90 ^{o} followed by a second exposure, and patterns of periodic nanodot arrays are formed on the photoresist layer (Figure 15c).

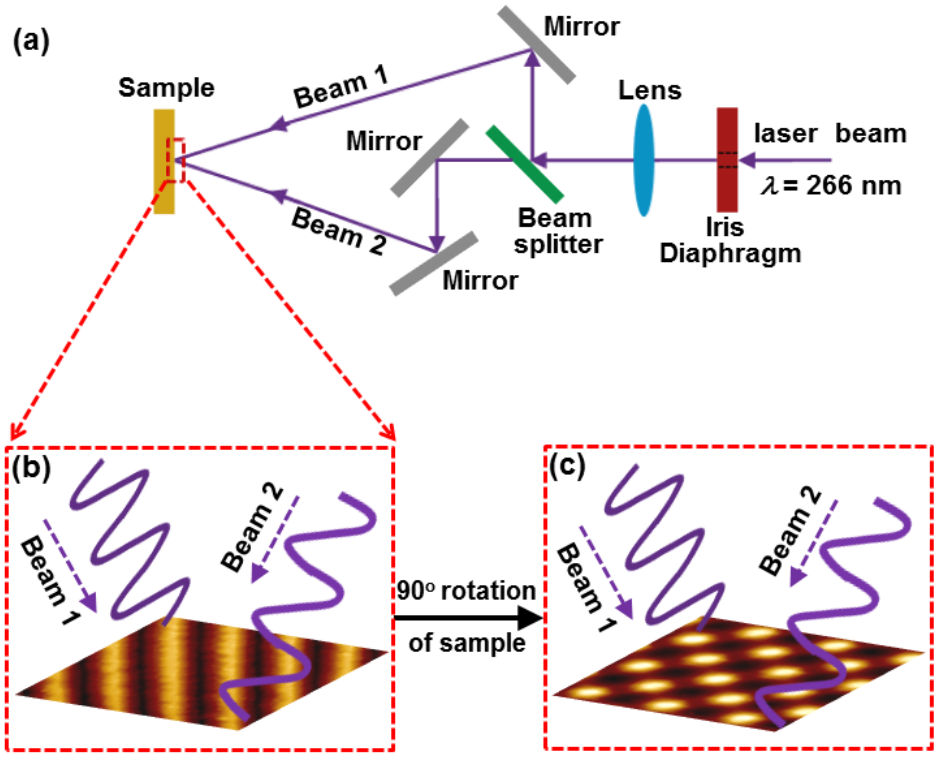


Figure 15. (a) Schematics of experimental setup for the laser interference patterning. (b) The interference between beam 1 and beam 2 forms a grating pattern on the photoresist layer under a single laser pulse (10 ns) irradiation. (c) The sample is then rotated for 90 ^{o} or at an arbitrary angle with a second exposure, and patterns of periodic nanodot arrays are formed on the photoresist layer or the substrate. The grating and nanodot patterns in b and c are fabricated on SU 8 via LIL approach and acquired by scanning probe microscope (SPM, Veeco Dimension 3100).

Figure 16a depicts the process sequence of fabricating vertically aligned ZnO NWs array using combination method of LIL patterning and HT growth. LIL technique is used for forming patterns on the SU-8 layer, in a way described in Figure 15. The negative photoresist SU-8 is spin-coated onto a 2-inch silicon or sapphire wafer, on top of which is a layer of ZnO texture or GaN film with (0001) surface orientation, respectively. The pattern of holes array is formed uniformly at the unexposed locations of SU-8 layer over the whole wafer area after two consecutive laser exposures with 90 ^{o} rotation of the substrate between exposures. As can be seen in Figure 16a, the (0001) surface of ZnO or GaN layer has been selectively exposed for the subsequent growth of aligned ZnO NWs

array. The substrate with patterned SU-8 layer is then put facing-downwards into the growth solution, floating on top of the nutrient solution surface for NWs growth. Vertically aligned ZnO NWs array are then synthesized in a solution containing 5 mM zinc nitrate (Alfa Aesar) and 5 mM hexamethylenetetramine (HMTA) (Fluka) at 85 °C for 24 hours in a Yamato convection box oven. ZnO NWs grow at the substrate sites not covered by SU-8 layer and uniformly patterned ZnO NWs array are hence obtained at large-scale. The morphology of as-synthesized ZnO NWs can be tuned by varying solution concentration, growth temperature and growth time[124]. The perfectly vertical alignment of ZnO NWs array is achieved due to the lattice match between the grown ZnO (0001) plane and the substrate plane (either ZnO texture or GaN layer). Both LIL and HT methods are carried out at low temperature (below 100 ^{o}C) and ambient pressure. It is also straightforward to extend this approach to fabrication of nanostructure arrays of other materials like Si, CdSe, and III-V compounds on various other substrates, such as glass, flexible materials and metals.

The formed patterns on SU-8-coated substrate after LIL patterning are imaged by a thermally-assisted field emission scanning electron microscope (SEM) (LEO 1530), as shown in Figure 16. Figure 16b is the optical image of a 2-inch Si wafer with SU8 open-hole pattern over the whole surface area. Figure 16c is the top-view of a patterned SU-8 film (500 nm thick). The presented pattern has a period of 2 μm and circular holes with diameter of 600 nm are opened over the surface uniformly with irradiation fluence of 3.5 mJ/cm^2 for the laser beams. The sidewalls of the holes are approximately vertical and the substrate is selectively exposed in an ordered and uniform manner (top-view in Figure 16c and 45^{o}-tilted view in 16d). The shapes, periods of the pattern, and scales of the hole can be adjusted by varying the laser interference patterning parameters, such as the fluence and the aperture size, and other experimental parameters like the angle of rotation applied to the samples between exposures. A detailed study on pattern generation will be

discussed later in this section.

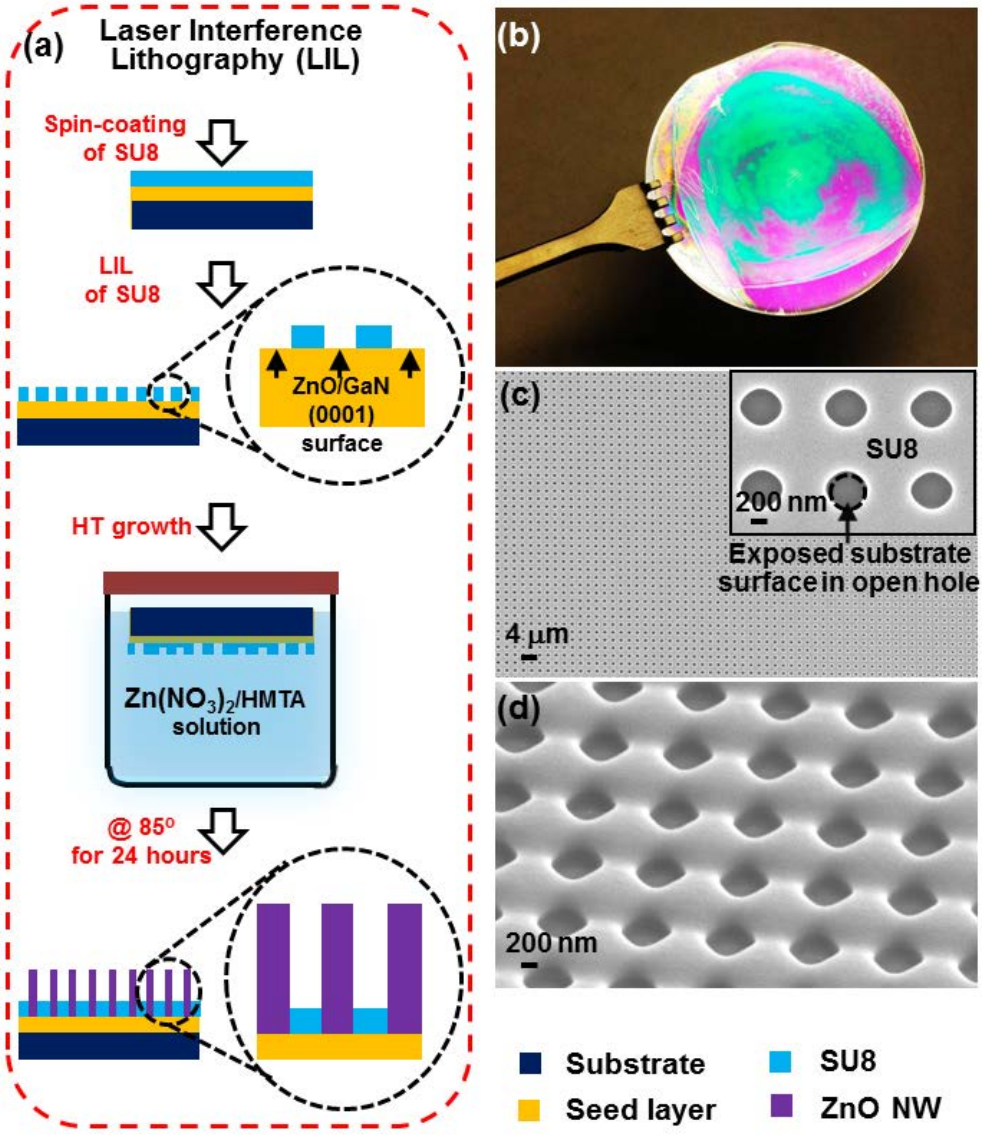


Figure 16. Schematics of the fabrication sequences of vertically aligned ZnO NW arrays using laser interference techniques. (a) Fabrication sequence using LIL approach for large-scale patterned vertically aligned ZnO NW arrays. (b) Optical image of a 2-inch Si wafer with SU 8 open-hole pattern over the whole surface area. The iridescence dispersion demonstrates the excellent periodicity over the entire wafer surface.(c) Top-view SEM image of patterned SU-8 film. Inset, zoom in top-view SEM image of patterned SU-8 film. (d) 45°-tilted-view SEM image of patterned SU-8 film.

3.2.2.2 Characterization results

The heteroepitaxial growth of vertically aligned ZnO NWs array on GaN substrate is investigated first. The morphology and uniformity of the patterned NW arrays via LIL approach are examined and confirmed by SEM images (Figure 17). Almost all of the NWs have the same diameter and height. The aligned ZnO NW arrays are uniformly grown following the patterned holes with high-fidelity at diameter of ~600 nm (Figure 17b). All the NWs are perfectly aligned normal to the substrate and have the same height of ~5 μm (Figures 17c and d).

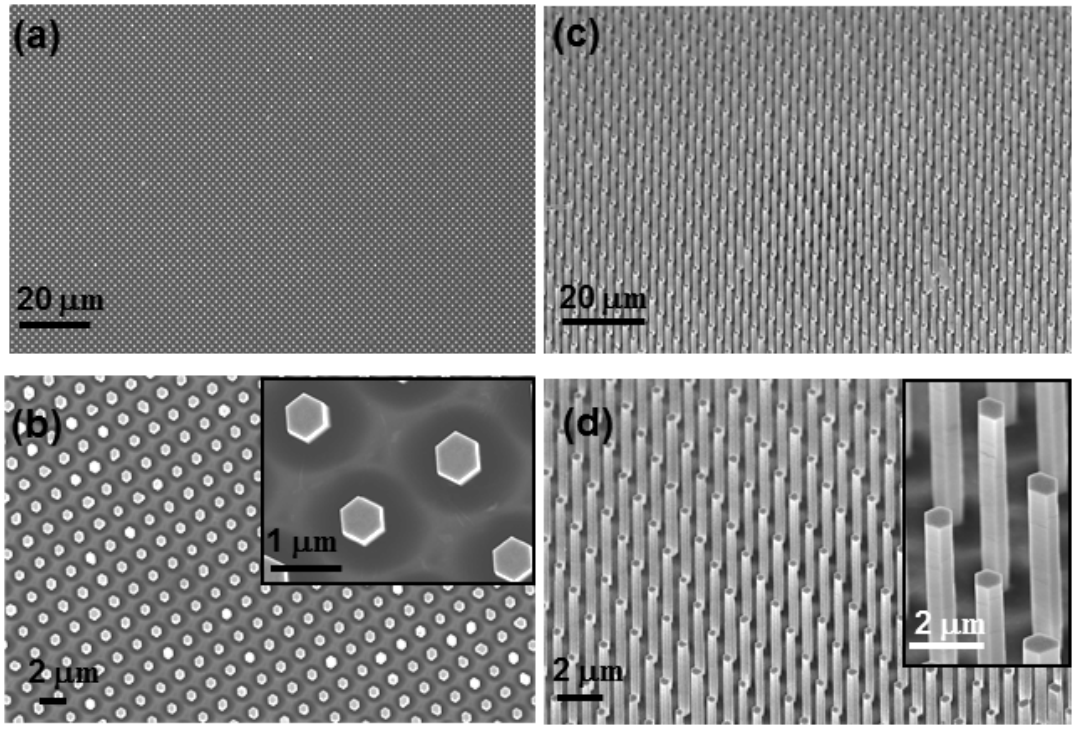


Figure 17. The heteroepitaxial growth of vertically aligned ZnO NW arrays on GaN substrate via LIL approach. (a) and (b) Top-view SEM images of vertically aligned ZnO NW arrays on GaN substrate in large-scale uniform pattern at different magnifications. (c) and (d) 45^{o}-tilted-view SEM images of vertically aligned ZnO NW arrays on GaN substrate in large-scale uniform pattern at different magnifications.

LIL-Patterned growth of ZnO NW arrays are also performed with different periods and sizes of opened-holes (Figure 18) on GaN substrate. An interesting phenomenon is

observed when comparing the ZnO NW arrays grown from patterns with different diameters of holes. When the diameter of opened holes is smaller than 600 nm (Figure 18a-d and Figure 17), an individual ZnO NW grows out of each hole. All of the NWs have perfect vertical alignment with the same diameter and height. When the diameter of opened holes is larger than 1 μm, random growth of ZnO NWs is observed (Figure 18e-h) on the substrate, with different diameters and heights for the grown ZnO NWs, which is similar to the result obtained for ZnO NWs growing on un-patterned bare GaN substrates.

This selective-area growth may be understood from the nucleation and growth process. The nuclei form at the beginning of the growth, which initiate and guide the subsequent growth of NWs when the sizes of the nuclei exceed the critical size. A competition exists between the NW growth and nucleus formation. The competition in open space leads to random growth of NW arrays due to its large size and multiple nucleations. When the surface for NW growth is confined in small areas separated at a certain distance from each other, one nucleus is formed in each confined spot, which then grows into a single NW. A 2D model proposed by Coltrin *et al*[144] describes a similar selective-area growth by introducing a diffusion mechanism of reaction by-product in their model. The mechanism of selective-area growth can be further investigated for patterns with different dimensions using the LIL approach described above. A more in-depth understanding of selective-area growth can enable fabrication of large-scale patterned ZnO NW arrays in a more controllable way.

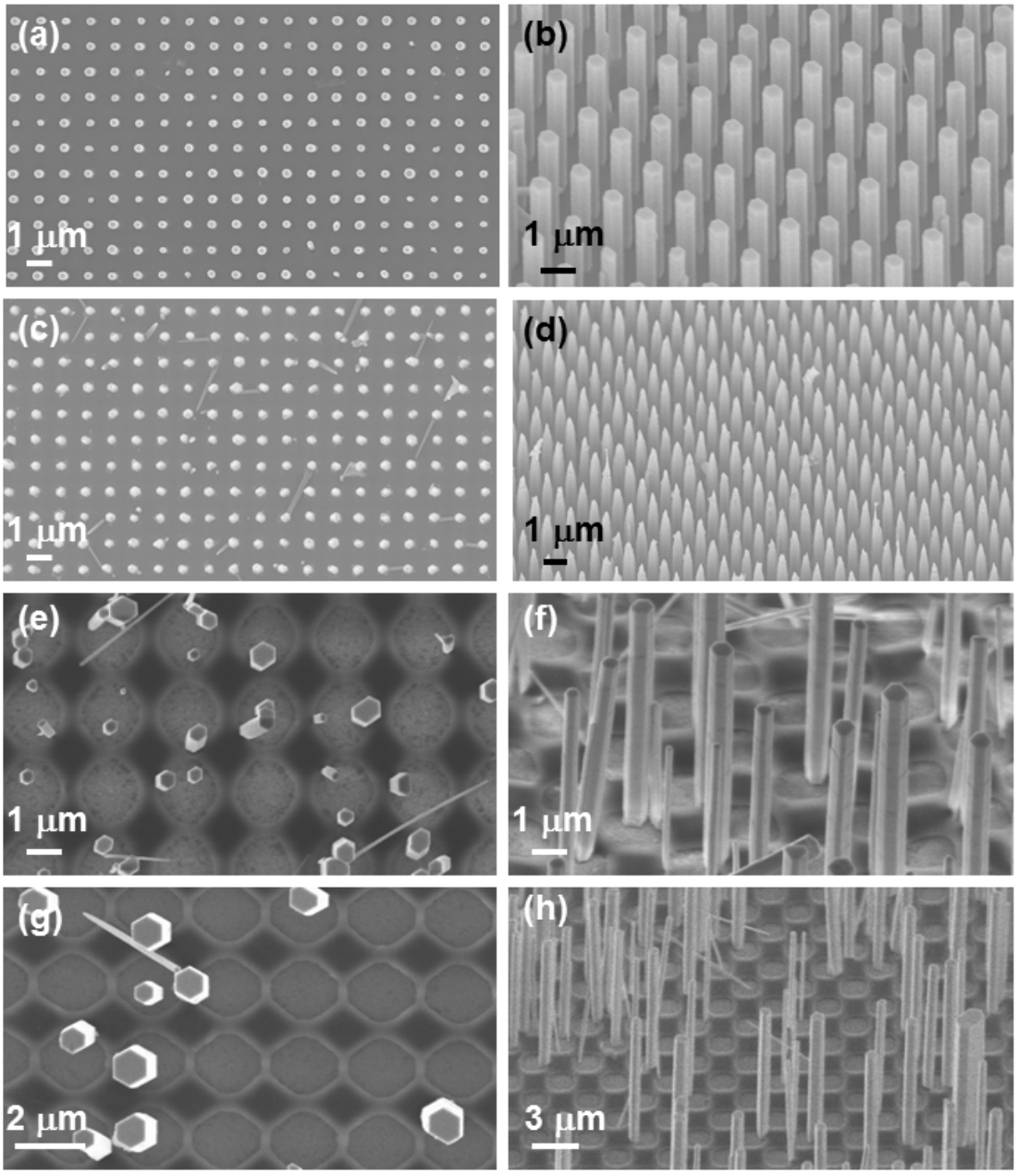


Figure 18. LIL-Patterned growth of ZnO NWs array on GaN substrate with different periods and sizes of opened-holes. (a) and (b) Top-view and 45^{o} side-view SEM images of vertically aligned ZnO NWs array on GaN substrate with 200 nm opened-holes and 1 μm period synthesized at 85 °C. (c) and (d) Top-view and 45^{o} side-view SEM images of vertically aligned ZnO NWs array on GaN substrate with 200 nm opened-holes and 1 μm period synthesized at 95 °C. (e), (f), (g) and (d) Top-view and 45^{o} side-view SEM images of vertically aligned ZnO NWs array on GaN substrate with >1 μm opened-holes and 2.4 μm period synthesized at 80 °C.

3.2.2.3 Extending fabrication to any substrates via ZnO texture layer

In order to achieve aligned ZnO NWs array, either by HT or PVD method, matches in the crystallographic orientation and lattice parameter between the substrate material and ZnO are required. Substrates such as single crystalline GaN[76] or ZnO[145] were previously adopted. However, the high cost of these substrates limits potential large-scale applications. Furthermore, applications using substrates of other materials such as polymers and glass have been of more interests[7,72]. It is hence highly desirable to develop a general method for fabricating vertically aligned ZnO NW arrays on essentially any substrates of low cost.

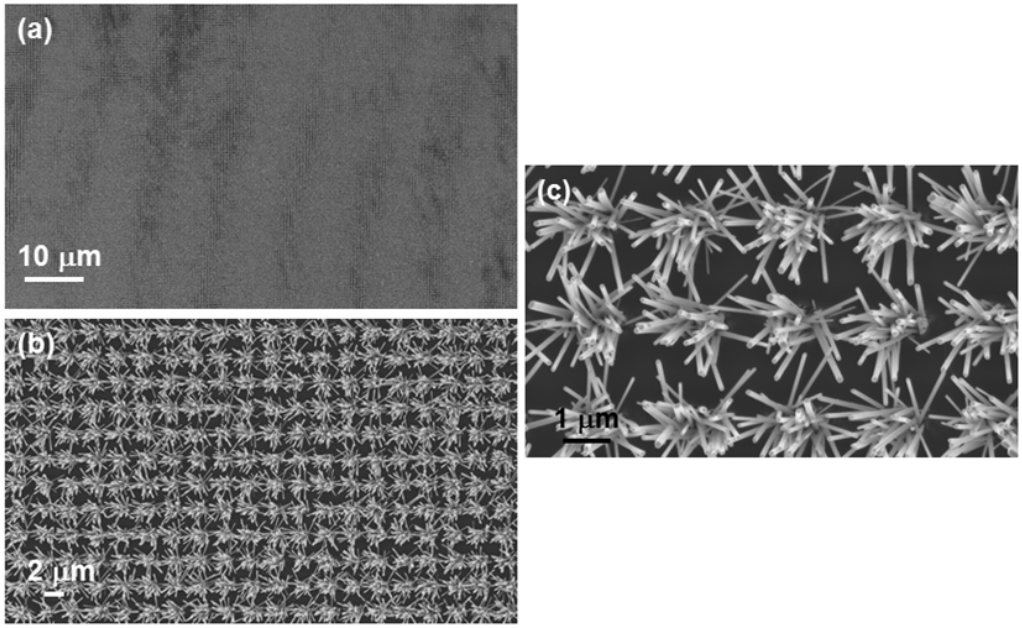


Figure 19. The homoepitaxial growth of randomly aligned ZnO NWs array on a silicon wafer covered with a polycrystalline ZnO seed layer via LIL approach. (a) , (b) and (c) Top-view SEM images of randomly aligned ZnO NWs array on Si substrate in large-scale uniform pattern at different magnifications.

The same LIL patterning and HT NW growth sequences are performed on a silicon wafer covered with a polycrystalline ZnO seed layer prepared by RF magnetron sputtering. As can be seen from Figure 19, multiple ZnO NWs grow out of each hole due

to the random in-plane orientations of the polycrystalline ZnO seeds deposited on the silicon wafer. A textured ZnO seed layer with a flat (0001) surface is hence desirable for

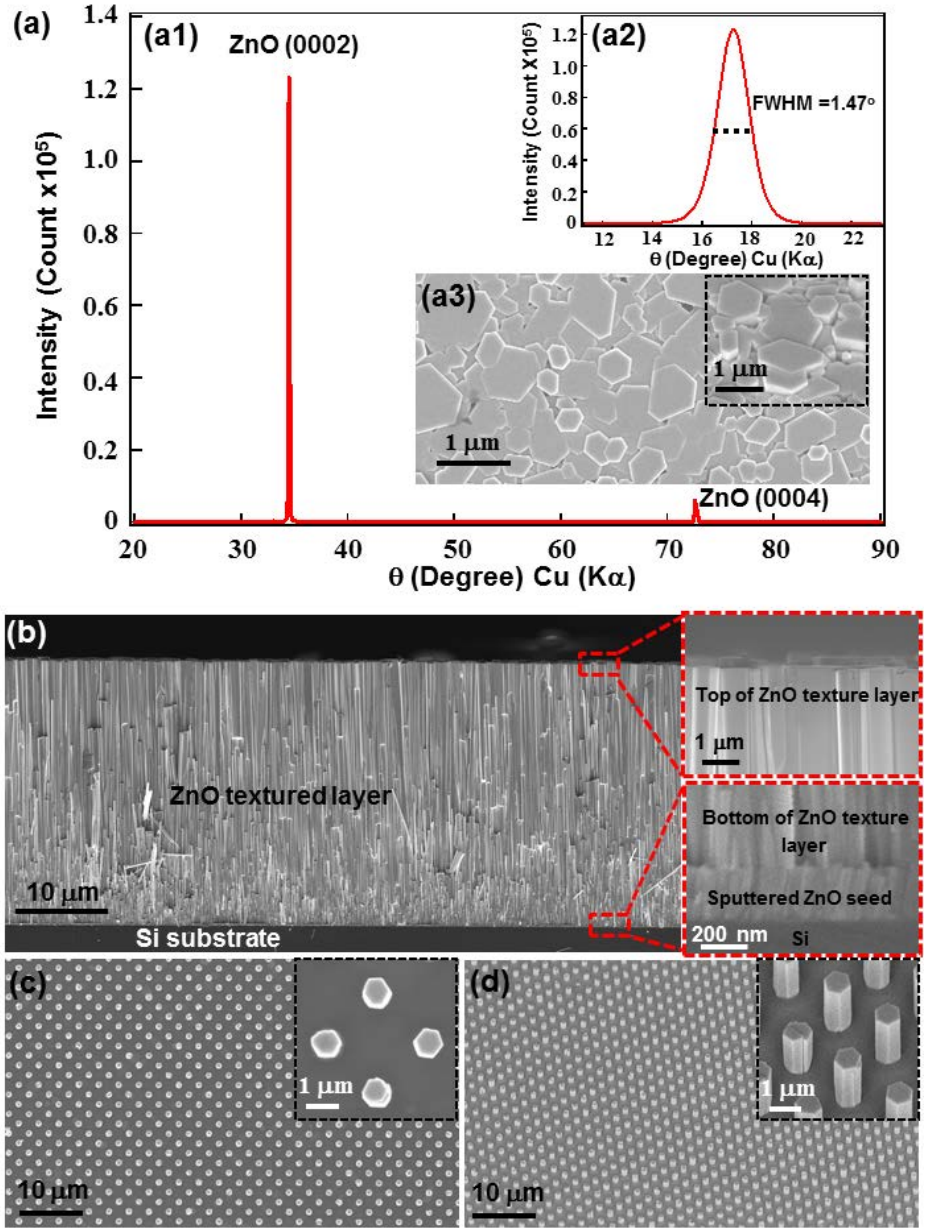


Figure 20. The homoepitaxial growth of large-scale vertically aligned ZnO NWs array via LIL approach on textured ZnO seed layer. (a) X-ray diffraction (XRD) measurements investigating the crystal structure and orientation as well as SEM image of the as-grown textured ZnO seed layer. (b) Cross-section of the as-grown dense textured ZnO layer. (c), (d) and insets, Top-view and 45^{o}-tilted-view SEM images of vertically aligned ZnO NWs array on silicon substrate with textured ZnO layer in large-scale uniform pattern at different magnifications.

subsequent growth of vertically aligned ZnO NW arrays and a facile way has thus been developed to prepare large-scale textured ZnO seed layer with a flat (0001) surface at low cost.

First, the silicon wafer is sputtered with a layer of ZnO with thickness around 200 nm (Figure 20b) in a RF magnetron sputtering system. The wafer is then put facing-downwards into the growth solution, floating on top of the nutrient solution surface for growth. A dense layer of aligned ZnO NWs is synthesized in a solution containing 20 mM zinc chloride ($ZnCl_2$) and 20 mM HMTA at 95 °C for 16 hours in a Yamato convection box oven. Ammonium hydroxide (NH_4OH) is also added into the solution at a volume concentration of around 4%.

The cross-section of this dense layer of aligned ZnO NWs is shown in Figure 20b. Figures 20a3 and its inset are the top view and 45^o-tilted view of as-prepared textured ZnO seed layer, respectively. The ZnO seed layer is formed by tightly compact ZnO NWs grown along [0001] direction. Those NWs have flat top (0001) surfaces (Figure 20a3) and small variation in height steps (Figures 20a3 inset and b). The crystal structure and orientation of the as-grown textured ZnO seed layer are studied by x-ray diffraction (XRD) measurements. The XRD θ-2θ scan (Figure 20a1) shows only two dominant peaks at 34.45° and 72.59°, attributed to the ZnO (0002) and ZnO (0004) planes, respectively. The XRD θ-2θ scan indicates that the surface of textured ZnO seed layer is (0001) oriented. The XRD θ-rocking curve (Figure 20a2) of textured ZnO seed layer is also investigated for peak at 34.45°, with a full width at half maximum (FWHM) value of 1.47°. The small FWHM value indicates good alignment among different (0001) oriented domains of the textured ZnO seed layer. The textured ZnO seed layer is then used for subsequent growth of vertically aligned ZnO NWs via LIL patterning and HT NW growth sequences as described previously. The perfectly vertical alignment of ZnO NW arrays is homoepitaxially achieved (Figure 20c and d) due to ideal match between

the (0001) facets of the dense ZnO NWs achieved in the first growth step and the ZnO NWs grown on top of them during the second step. The hexagonal shape of the NW indicates that it is single crystal with growth direction along [0001]. The NWs have the same diameter of around 1 μm. All of the NWs are perfectly aligned normal to the substrate and have the same height of around 2 μm.

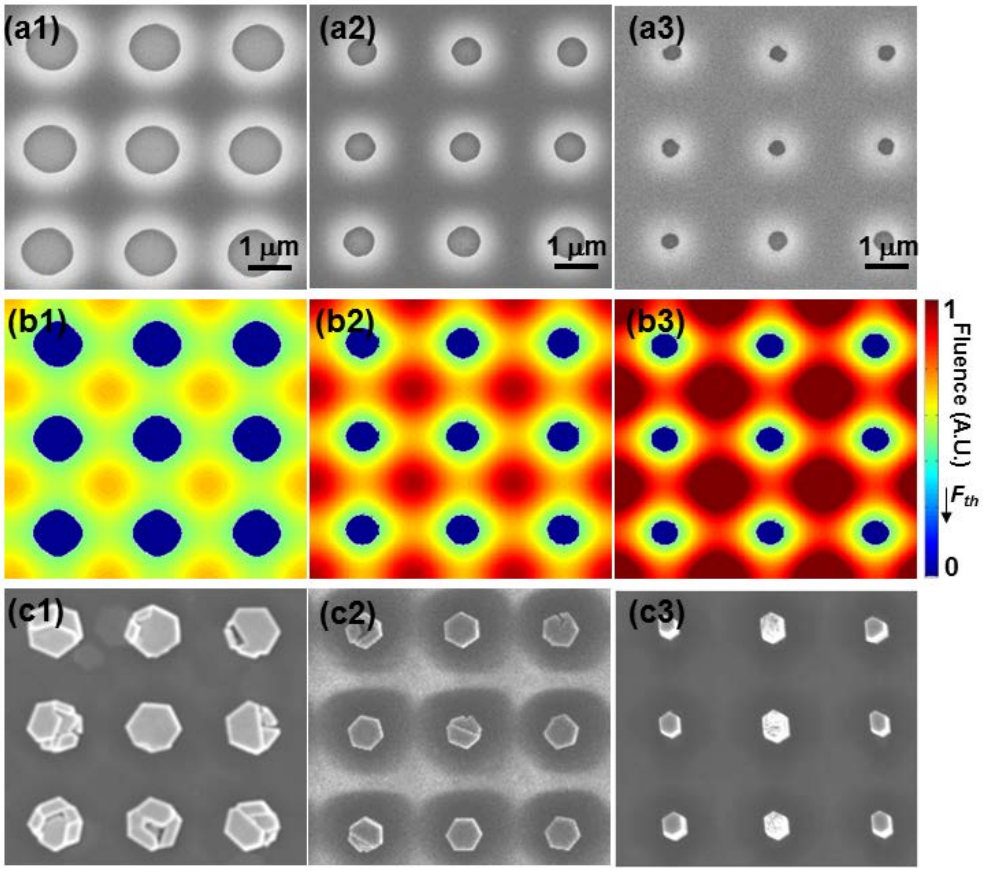


Figure 21. (a1-a3) Top-view SEM images of SU-8 patterns of different hole-opening sizes on Si substrate with textured ZnO seed layer, and the interference light fluence is 1.6, 3.2 and 6.0 mJ/cm^2, respectively. (b1-b3) Simulated laser fluence distribution in SU-8 using the same laser fluencies as those in a1-a3. (c1-c3) Top-view SEM images of vertically aligned ZnO NW arrays, which follow the pre-defined pattern of SU-8 layer with high-fidelity.

The opening dimension and periodicity of the pattern array can be controlled by varying the fluence of the primary laser beam and the angle between the interfering

beams, respectively. We have studied the growth of ZnO NW arrays with different hole diameters on Si substrate with textured ZnO seed layer. Patterns with a fixed period of 2.5 μm but with varying hole diameters are obtained at a fixed angle of 6.3^{o} between the interfering beams. The diameters of the holes are 1 μm, 700 nm and 350 nm respectively in Figures 21a1-a3, which are generated at fluencies of 1.6, 3.2 and 6.0 mJ/cm^2, respectively. For a negative photoresist, the hole diameter decreases with increasing exposure dose, as can be seen from Figure 21.

The fluence distribution on the SU-8 substrate after two successive patterning exposures is also simulated using the same exposure parameters as those in Figures 21a1-a3. Figures 21b1-b3 show the corresponding calculated fluence distribution, through which the holes are created at the locations where the exposure dose is lower than the threshold fluence (F_{th}) for photo-curing of SU-8, shown as the circular areas in dark blue in all three simulated results. SU-8 will not be photo-cured in these areas and hence will be dissolved in the subsequent developing process to holes. The simulation results are in good agreement with the experimental results. Synthesis of vertically aligned ZnO NW arrays is then carried out and the results are shown in Figures 21c1-c3. It can be seen that the as-grown NWs array follow the pre-defined pattern of SU-8 layer with high-fidelity. When the hole size is large (1 μm), distinct boundaries can be observed in as-grown NWs, which are attributed to the finite size of the domains in the underneath ZnO texture layer (Figure 20a3). Fewer boundaries exist with decreased size of hole-openings and it is observed that when the hole size lies below the average domain size in the underneath ZnO texture layer (around 500 nm), single intact ZnO NW grows out of each hole without any grain-boundaries observed at the top facet (Figure 21c3). Vertically aligned single crystalline ZnO NW arrays can therefore be achieved by engineering the ZnO texture layer and the corresponding hole diameter in the patterned photoresist layer.

In summary, an effective approach for controllable wafer-scale fabrication of ZnO

NW arrays has been demonstrated. Laser interference patterning is employed to control the position, size and orientation of synthesized ZnO NWs, while HT chemical method is used to control the morphology and material properties of NWs. More importantly, combinations of both laser interference patterning and HT method allow more available access to large-scale uniformly patterned nanostructures at a high-throughput rate and substantially reduced cost, both in time and in equipment resources, providing an efficient approach for fabricating highly-ordered one-dimensional nanostructures at wafer-scale. The development of textured ZnO seed layer for replacing single crystalline GaN and ZnO substrates can not only reduce the cost, but also extend the large-scale fabrication of vertically aligned ZnO NW arrays on substrates of other materials such as polymers, Si and glass. This combined large-scale nanofabrication approach paves path towards integrating nanostructures into devices or technology platforms, which are compatible with state-of-art micro/nanofabrication technologies, for applications in energy harvesting, sensing, electronics, optoelectronics, piezotronics and plasmonics. In addition, the solution growth process ensures that a majority of the NWs are in direct contact with the substrate and provides a continuous pathway for carrier transport, which is important for practical applications. A major limitation of solution synthesis, however, is that most capping agents have been chosen via an empirical trial-and-error approach.

CHAPTER 4

STRAIN-GATED PIEZOTRONIC LOGIC NANODEVICES

A self-powered [32]autonomous intelligent nanoscale system should consist of ultrasensitive nanowire (NW) based sensors[146-148], integrated high-performance memory and logic computing components for data storage and processing as well as decision making[149-153], and energy scavenging unit for sustainable, self-sufficient and independent operation[12,41,91,154-156]. The existing semiconductor NW logic devices are based on electrically-gated field effect transistors, which function as both the drivers and the active loads of the logic units by adjusting the conducting channel width[157]. Moreover, the currently existing logic units are "static" and are almost completely triggered or agitated by electric signals, while the "dynamic" movable mechanical actuation is carried out by another unit possibly made of different materials.

In this chapter, the piezoelectrically trigged mechanical-electronic logic operation using the piezotronic effect is presented, through which the integrated mechanical electrical coupled and controlled logic computation are achieved using only ZnO NWs[11]. By utilizing the piezopotential created in a ZnO NW under externally applied deformation, strain-gated transistors (SGTs) have been fabricated, using which universal logic components such as inverters, NAND, NOR, XOR gates have been demonstrated for performing piezotronic logic calculations, which have the potential to be integrated with the NEMS technology for achieving advanced and complex functional actions in applications of vital importance in portable electronics, medical sciences and defense technology, such as in nanorobotics for sensing and actuating, in microfluidics for controlling the circuitry of the fluid flow, in other micro/nano-systems for intelligent control and action.

4.1 Background

ZnO is unique because of its coupled piezoelectric and semiconductor properties, which is the piezotronic effect dealing with the piezopotential tuned/gated charge carrier transport process in a semiconductor material[13,158]. The piezopotential created inside a ZnO NW under strain can be effectively used as a gate voltage, which has been applied for fabricating a range of piezotronic nanodevices[30,75], and therefore, the mechanic-electrical coupled and controlled actions can be performed in one structure unit made of a single material. Mechanical straining can create a piezopotential inside ZnO due to the polarization of the non-mobile ions, owing to the piezoelectric effect. In addition, the piezopotential can act as a "controller" for gating the transport behavior of the charge carriers, which is the fundamental principle for strain-gated electronic devices, based on which ZnO-NW electromechanical switch has been fabricated[31].

4.2 Strain-gated transistor (SGT)

A strain gated transistor (SGT) is made of a single ZnO NW with its two ends being fixed by metal contacts, which are the source and drain electrodes, on a polymer substrate (Figure 22a). The thickness of the Dura-Lar film is 0.5 mm. The ZnO NWs are synthesized via a physical vapor deposition method based on VS process (see chapter 3) and typically have diameters of 300 nm and lengths of 400 μm (Figure 22a). The films are first cleaned with acetone, isopropyl alcohol and DI water by sonication, after which, the Dura-Lar films are dried by nitrogen gas blowing. One ZnO NW is placed flat on the top surface of the Dura-Lar film first using a probe station (Cascade Microtech, Inc.) under an optical microscope (Leica Microsystems, Inc.). Silver paint (Ted Pella, Inc.) is applied at both ends of the ZnO NW for electrical contacts.

Once the substrate is bent, a tensile/compressive strain is created in the NW since the mechanical behavior of the entire structure is determined by the substrate. Utilizing

the piezopotential created inside the NW, the gate input for a NW SGT is an externally-applied strain rather than an electrical signal. I_{DS}-V_{DS} characteristic for each single ZnO-NW SGT is obtained as a function of the strain created in the SGT (Figure 22a) before further assembly into logic devices. A NW SGT is defined as forward biased if the applied bias is connected to the drain electrode (Figure 22a).

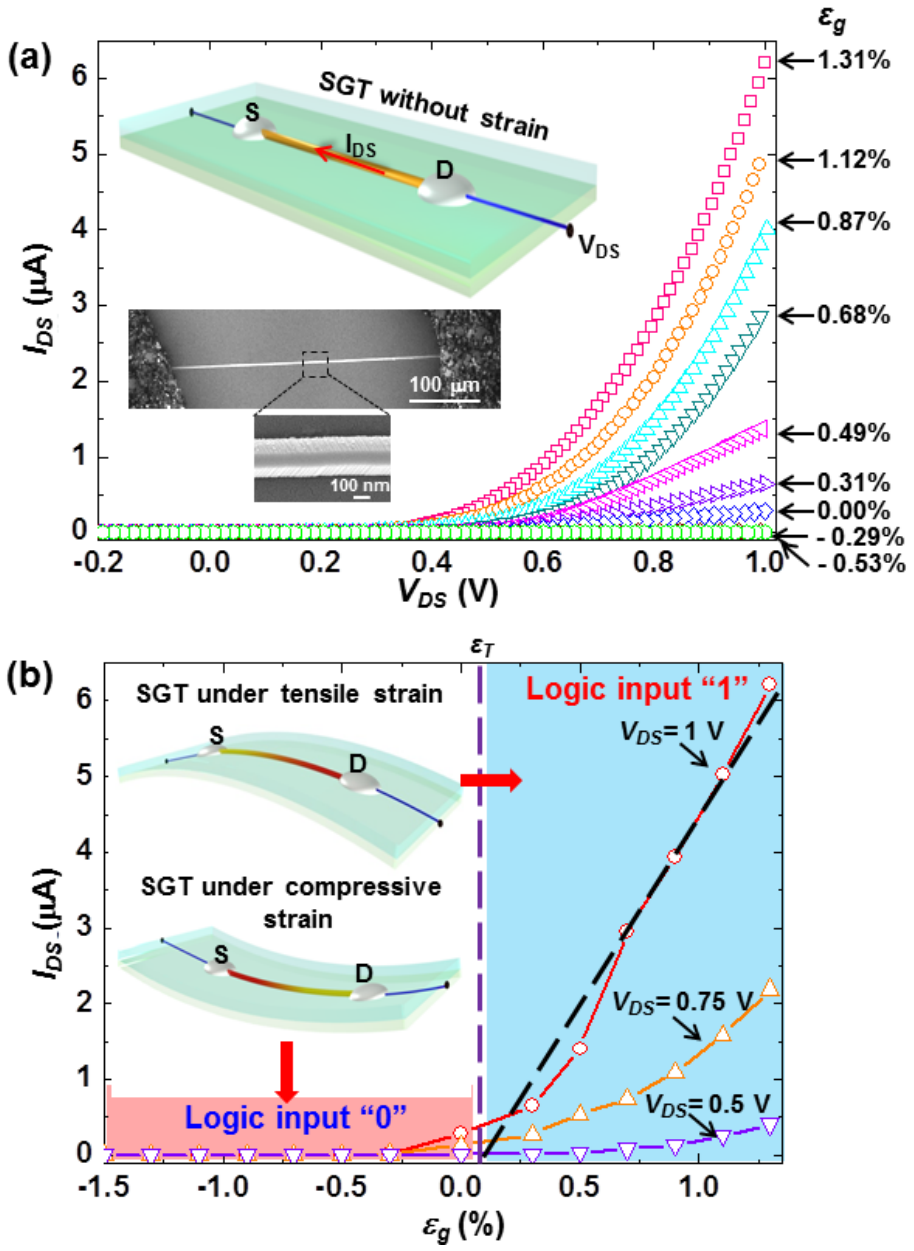


Figure 22. Single ZnO NW strain-gated transistor (SGT). a) $I_{DS} - V_{DS}$ output characteristic for a ZnO SGT device. b) $I_{DS} - \varepsilon_g$ transfer characteristic for the same ZnO SGT device under three different V_{DS} bias values: 1 V, 0.75 V and 0.5 V, respectively.

4.2.1 Calculation of strain for ZnO strain gated logic devices

For a SGT, the external mechanical perturbation induced strain (ε_g) acts as the gate input for controlling the "on"/"off" state of the NW SGT. The positive/negative strain is created when the NW is stretched/compressed. Since the mechanical behavior of the Dura-Lar film substrate is not affected by the ZnO wire due to the much smaller sizes of ZnO NWs, a simple estimation of the strain induced in the ZnO NWs can be obtained using the Saint-Venant theory for small deflections[159]. The shape of the plastic substrate can be approximated as a beam, with thickness 2*a*, width *w* and length *l*. For easiness of derivation, the origin of the coordinate system is set at the center of the cross section of one side of the film, while the *z* axis is parallel to the length *l* and *x* axis is parallel to the width *w*. In order to determine how the NW deforms as the substrate is deflected under an external bending force f_y, only the ε_{zz} component of the strain tensor needs to be calculated, where $\varepsilon_{zz} = \Delta L_{\text{wire}}/L_{\text{wire}}$. Meanwhile, $\sigma_{zz} = - f_y/I_{xx}y(l\text{-}z)$, $\sigma_{xx} = \sigma_{yy} = 0$, where I_{xx} is the geometrical moment of inertia for the beam cross section. Therefore, $\Delta L_{\text{wire}}/L_{\text{wire}} = \varepsilon_{zz} = \sigma_{zz}/E$. The lateral deflection D_{max} of the substrate is experimentally easier to measure than the bending force f_y and the relationship between D_{max} and f_y is $D_{max} = f_y l^3/3EI_{xx}$. Therefore we can obtain[160]

$$\varepsilon_{zz} = -3\frac{y}{l}\frac{D_{\max}}{l}(1-\frac{z}{l}) \qquad (17)$$

With $y = \pm a$ and $z = z_0$ is the vertical distance between the fixed end of the Dura-Lar film substrate and the middle point of the ZnO NW. The positive and negative sign for *y* stand for the compressed side and tensile side of the beam, respectively.

4.2.2 Characteristics of SGT

The I_{DS}- ε_g curves at a fixed V_{DS} show that I_{DS} increases as the gate strain ε_g increases and the threshold gate strain ε_T is around 0.08% (Figure 22b), which show that the SGT behaves in a similar way to a *n*-channel enhancement-mode MOSFET. The

threshold gate strain ε_T is determined from the intercept (on the ε_g axis) of the tangent of the maximum slope region (shown as the black dashed line in Figure 22b) of the I_{DS}-ε_g curve. The I_{DS}-ε_g transfer curve obtained for drain bias voltage V_{DS} = 1 V (Figure 23) demonstrates that the NW SGT has a peak pseudo transconductance, $g_m = dI_{DS}(V_{DS})/d\varepsilon_g$, which is 6 μA for a strain change of $\Delta\varepsilon_g$ = 1%. The on and off currents I_{on} and I_{off} for the NW SGT can be determined as the values obtained at $\varepsilon_{g\,(on)} = \varepsilon_g$ - 0.3% and $\varepsilon_{g\,(off)} = \varepsilon_g$ + 0.7%, so that 70% of the ε_g swing above the threshold strain ε_g turns the ZnO NW SGT on, while the remaining 30% defines the "off" operation range, which is demonstrated in Figure 23. I_{on} = 3.38 μA and I_{off} =0.03 μA are hence obtained with I_{on} / I_{off} ratio of 112 for V_{DS} = 1 V; this ratio is comparable to the reported value for the Ge/Si NW based device that was electrically driven[157].

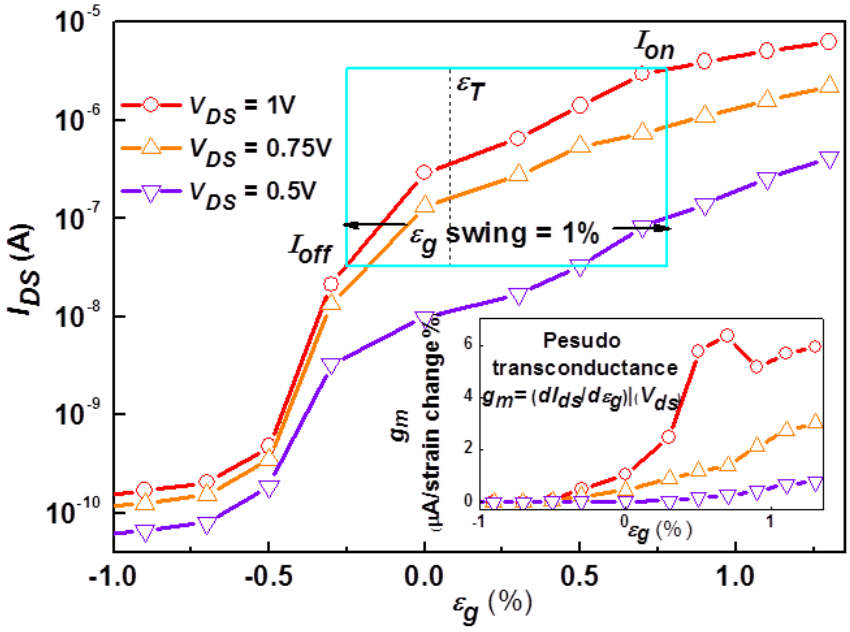


Figure 23. I_{DS}-ε_g transfer characteristic for the ZnO SGT device under three different V_{DS} bias values: 1 V, 0.75 V and 0.5 V, respectively. The blue square defines the 1% gate strain window. (Inset) Pseudo transconductance for this ZnO NW SGT with V_{DS} bias values of 1 V, 0.75 V and 0.5 V, respectively, from top to bottom.

4.2.3 Working principle of SGT

The working principle of a SGT is illustrated by band structure of the device. A strain free ZnO NW has Schottky contacts at its two ends with the source and drain

electrodes but with different barrier heights of Φ_S and Φ_D, respectively (Figure 24a). The Fermi level inside the ZnO NW is considered flat here for illustration purpose, which is valid in our devices since the most majority of the bias falls at the reversed biased junction[30]. When the drain is forward biased, the quasi-Fermi levels at the source ($E_{F,S}$) and drain ($E_{F,D}$) are separated by the value of eV_{bias}, where V_{bias} is the applied bias (Figure 24b). An externally applied mechanical strain (ε_g) results in both the band structure change and piezopotential field inside a ZnO NW. The change in band structure leads to the piezoresistive effect, which is a non-polar and symmetric effect at both the source and drain contacts. Since ZnO is a polar structure along *c*-axis, straining in axial direction (*c*-axis) creates a polarization of cations and anions in the NW growth direction, resulting in a piezopotential drop from V^+ to V^- inside the NW (Figure 24c), which produces an asymmetric effect on the changes in the Schottky barrier heights (SBHs) at the drain and source electrodes. Under tensile strain, the SBH at the source side decreases from Φ_S to $\Phi'_S \cong \Phi_S - \Delta E_P$ (Figure 24c), where ΔE_P denotes the change from the locally created piezopotential and it is a function of the applied strain, resulting in increased I_{DS}. For the compressively strained SGT, the sign of the piezopotential is reversed, and thus the SBH at the source side is raised from Φ_S to $\Phi''_S \cong \Phi_S + \Delta E'_P$ (Figure 24d), where $\Delta E'_P$ denotes the piezopotential effect on the SBH at source side, resulting in a large decrease in I_{DS}. Therefore, as the strain ε_g is swept from compressive to tensile regions, the I_{DS} current can be effectively turned from "on" to "off" while V_{DS} remains constant. This is the fundamental operating principle of the SGT.

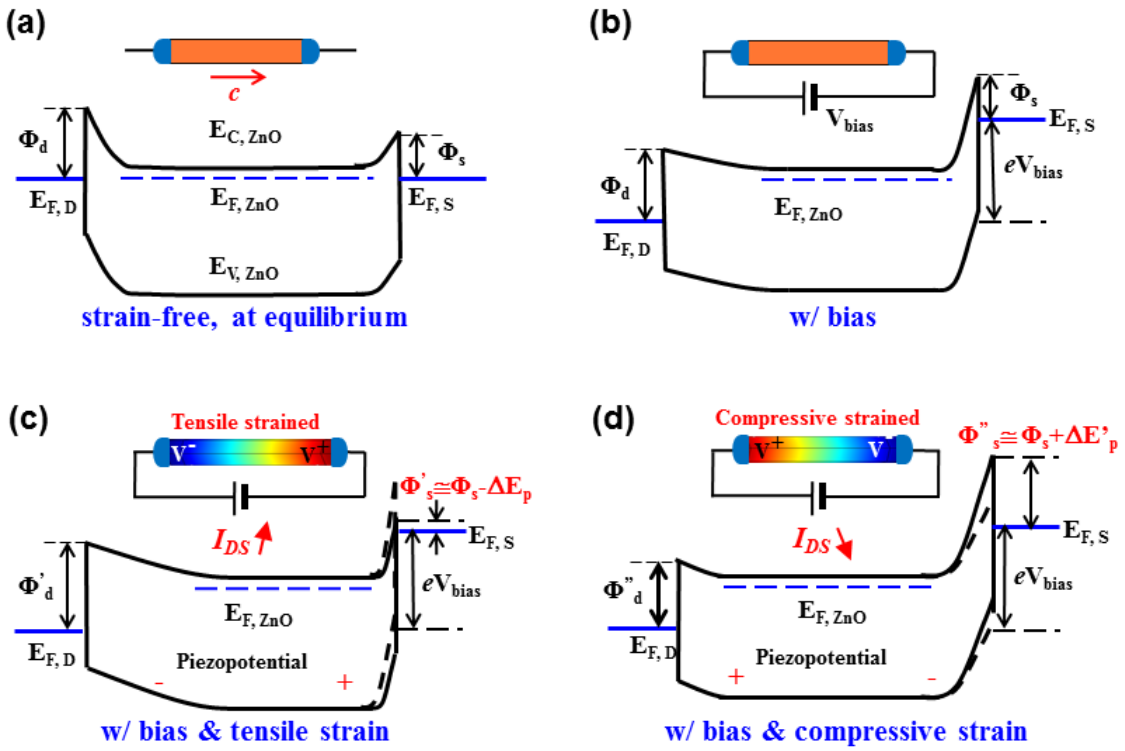


Figure 24. The band structures of the ZnO NW SGT under different conditions for illustrating the mechanism of SGT. a) The band structure of a strain-free ZnO NW SGT at equilibrium with different barrier heights of Φ_S and Φ_D at the source and drain electrodes, respectively. b) The quasi-Fermi levels at the source ($E_{F,S}$) and drain ($E_{F,D}$) of the ZnO SGT are split by the applied bias voltage V_{bias}. c) With tensile strain applied, the SBH at the source side is reduced from Φ_S to $\Phi'_S \cong \Phi_S - \Delta E_P$. d) With compressive strain applied, the SBH at the source side is raised from Φ_S to $\Phi''_S \cong \Phi_S + \Delta E'_P$.

Theoretical efforts have also been carried out to derive analytical expressions which can reveal the working principle of SGT[158]. By ignoring the surface states and other anomalies, charge distribution in the M-S contact can be simplified as shown in Figure 25a, in which W_n is the width of region where ionized donors distribute in the *n*-type semiconductor (ZnO here). In conventional piezoelectric theory, since the region within which the piezoelectric polarization charges distribute is much smaller than the volume of the bulk crystal, it is reasonable to assume that piezoelectric polarization charges distribute at the surface region with zero thickness of the bulk piezoelectric material. Such an assumption, however, does not apply for NW devices. It is therefore more reasonable to assume that piezoelectric polarization charges distribute in the region with

width of W_{piezo} near the barrier interface (Figure 25a). When strain is introduced in the semiconductor, the induced polarization charges at the interface not only change the height of the Schottky barrier, but also the width of depletion region.

The carriers transport in M-S contact is dominated by the majority carriers according to the diffusion theory for Schottky barrier, the current under forward bias can be expressed as[161]

$$J_n \approx J_D \exp(-\frac{q\phi_{Bn}}{kT})[\exp(\frac{qV}{kT})-1] \tag{18}$$

where $J_D = \frac{q^2 D_n N_C}{kT}\sqrt{\frac{2qN_D(\psi_{bi}-V)}{\varepsilon_s}}\exp(-\frac{q\phi_{Bn}}{kT})$ is the saturation current density. We can define J_{D0} as the saturation current density with the absence of piezoelectric polarization charges:

$$J_{D0} = \frac{q^2 D_n N_C}{kT}\sqrt{\frac{2qN_D(\psi_{bi0}-V)}{\varepsilon_s}}\exp(-\frac{q\phi_{Bn0}}{kT}) \tag{19}$$

where ψ_{bi0} and ϕ_{Bn0} are built-in potential and SBH with the absence of piezoelectric polarization charges. The effect of piezoelectric charge can be considered as perturbation to the conduction-band edge E_C[158]. The change in effective SBH induced by piezoelectric polarization charges can then be derived as:

$$\phi_{Bn} = \phi_{Bn0} - \frac{q^2 \rho_{piezo} {W_{piezo}}^2}{2\varepsilon_s} \tag{20}$$

The current density across the Schottky barrier formed between metal and strained *n*-type piezoelectric semiconductor can hence be rewritten as:

$$J_n \approx J_{D0} \exp(\frac{q^2 \rho_{piezo} {W_{piezo}}^2}{2\varepsilon_s kT})[\exp(\frac{qV}{kT})-1] \tag{21}$$

This indicates that charge carriers transported across the contact between metal and strained *n*-type piezoelectric semiconductor is an exponential function of the localized piezoelectric polarization charges. For the SGT under investigation here, we can make the above result more specific to reflect effect of piezopotential on metal-Wurtzite semiconductor contact. For the ZnO NW used in SGT which grows along the *c*-axis, the piezo-coefficient matrix can be expressed as:

$$(\mathbf{e})_{ijk} = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \tag{22}$$

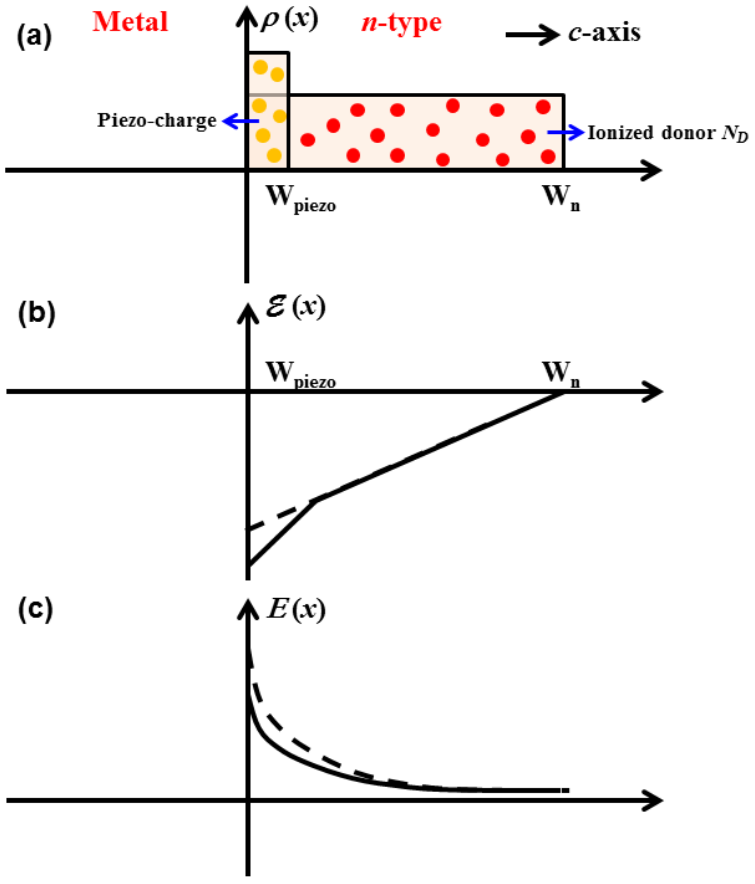


Figure 25. (a) Space charges distribution; (b) electric field and (c) energy band diagram for ideal metal-semiconductor Schottky contacts with the presence of piezoelectric polarization charges at applied voltage V = 0 (thermal equilibrium). Dashed lines indicate electric field and energy band with the absence of piezoelectric charges. Adapted from [158].

If the induced strain is s_{33} along the *c*-axis, the piezoelectric polarization can then be obtained from $P_z = e_{33}s_{33} = q\rho_{piezo}W_{piezo}$, where ρ_{piezo} represents the density of created piezoelectric polarization charges. The current density across the Schottky barrier can now be expressed as:

$$J = J_{D0}\exp(\frac{qe_{33}s_{33}W_{piezo}}{2\varepsilon_s kT})[\exp(\frac{qV}{kT})-1] \quad (23)$$

It can be seen clearly that current transported across the M-S interface is directly related to the exponential of the local strain, not only by the magnitude of the strain, but also by the polarity of the induced strain. When positive piezoelectric polarization charges (positive ρ_{piezo}) due to tensile strain (positive s_{33}) are introduced locally to the Schottky barrier at work, current transported across the barrier increases. This is consistent with experimental results observed in Figures 22 and 23. Similar conclusion can also be achieved when the polarity of induced strain is switched to compressive type. This is the fundamental mechanism of SGT.

4.2.4 Comparison between SGT and traditional field-effect-transistor (FET)

A better illustration of the basic concept of piezotronics can be obtained by comparing SGT with conventional metal-oxide-semiconductor-field-effect transistor (MOSFET). For the traditional thin-film based MOSFET, the two highly doped regions of the substrate are the drain and source areas; a thin dielectric layer is deposited on region between source and drain to serve as the gate dielectrics, on which the gate electrode is made. The electrons flowing from source to drain under an applied external voltage V_{DS} is controlled by the applied gate voltage V_G, which modulates the width and shape of conduction channel for transporting the charge carriers (Figure 26a). The similar structure and operation mechanism can also be applied to a semiconductor NW based FET (Figure 26b).

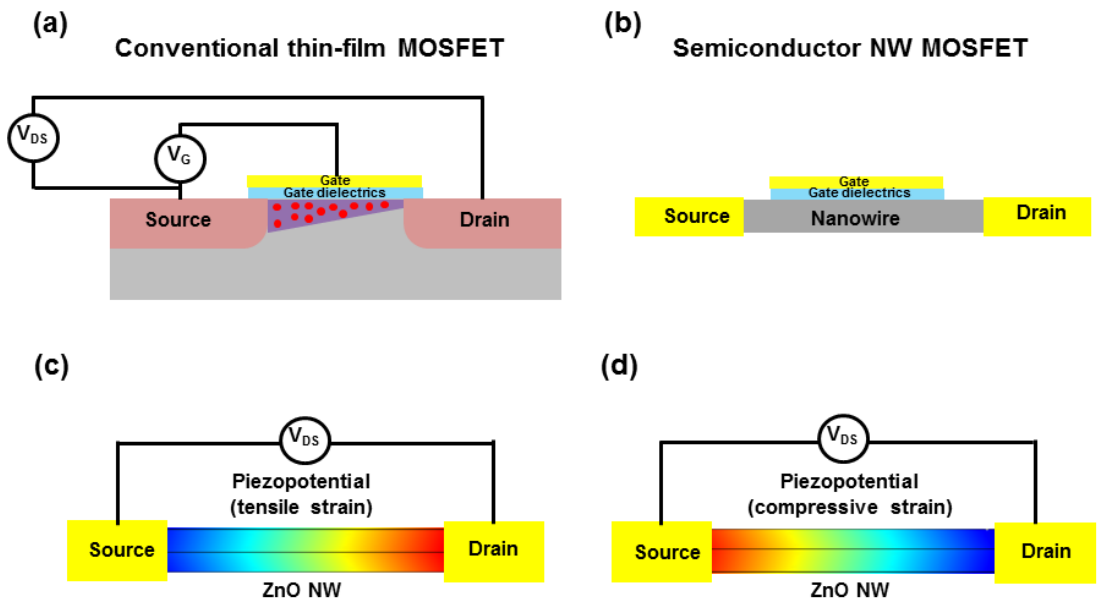


Figure 26. Schematics of (a) conventional thin-film based MOSFET and (b) a semiconductor NW based FET; Schematics of a SGT under tensile strain (c) and compressive strain (d), where the gate voltage which controls the channel width in MOSFET is replaced by a piezopotential that modulates the transport across the MS interface[29].

In contrast, a SGT or piezotronic transistor possesses the two-terminal metal-NW-metal structure, such as Au-ZnO-Au or Ag-ZnO-Ag as shown in Figure 26c and d. The fundamental principle of the SGT or piezotronic transistor is to modulate the carrier transport at M-S interface by piezopotential induced in the semiconductor under mechanical strain[29]. SGT is distinctly different from the design of conventional MOSFET. First of all, the externally applied electrical gate voltage is replaced by an inner crystal piezopotential created under strain; consequently the "gate" electrode is eliminated. Secondly, the control over conducting channel width in traditional MOSFET is replaced by a modulation at the interface. Since the current transported across the M-S interface is the exponential of the local SBH, the ON/OFF ratio of the device can be significantly enhanced due to the non-linear effect. Finally, a voltage-controlled device is replaced by an external strain/stress controlled device, which might enable complimentary functionalities to conventional CMOS devices.

4.3 Strain-gated inverter (SGI)

4.3.1 Fabrication and operation of SGI

The piezotronic strain-gated complementary logic gates can then be built using back-to-back packaged *n*-type ZnO NW SGTs on the top and bottom surfaces of the same flexible substrate. The first demonstration is to illustrate the ZnO-NW strain-gated inverter (SGI) (Figure 27). The SGI was fabricated by bonding two ZnO NWs laterally on a Dura-Lar film. The thickness of the Dura-Lar film is 0.5 mm. The ZnO NWs were synthesized via VS physical vapor deposition method described in Chapter 3 and typically have diameters of 300 nm and lengths of 400 μm. The films were first cleaned with acetone, isopropyl alcohol and DI water by sonication, after which, the Dura-Lar films were dried by nitrogen gas blowing. One ZnO NW was placed flat on the top surface of the Dura-Lar film first using a probe station (Cascade Microtech, Inc.) under an optical microscope (Leica Microsystems, Inc.). Silver paint (Ted Pella, Inc.) was applied at both ends of the ZnO NW for electrical contacts. The second ZnO NW was placed on the bottom surface of the Dura-Lar film in the same way.

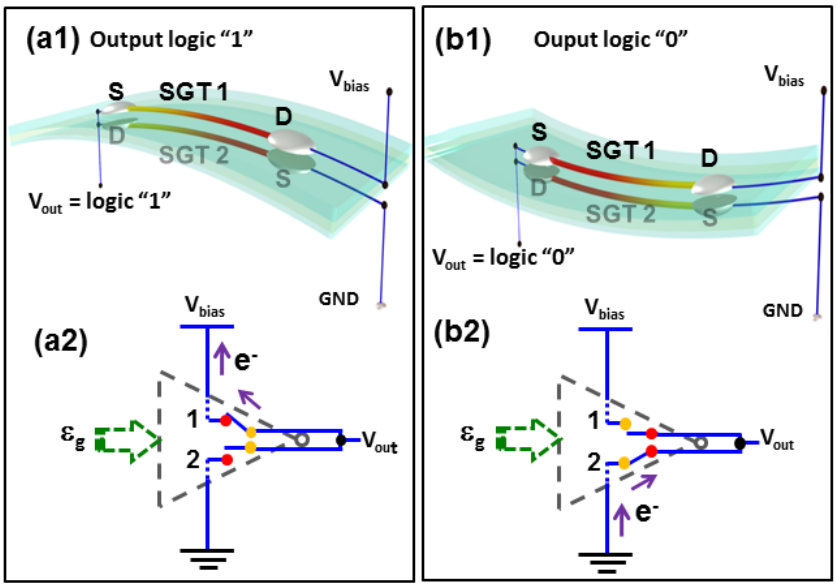


Figure 27. Schematics and corresponding symbols of a ZnO NW strain-gated inverter (SGI) performing logic operations on responding input strain.

When the substrate is bent downward (Figure 27a1), a tensile strain of 0.05-1.5% is created in SGT 1, while a compressive strain with the same magnitude is simultaneously produced in SGT 2, which results in a complementary “on” and “off” status in the two SGTs, respectively. Alternatively, if the substrate is bent upward (Figure 27b1), the two SGTs have a complementary “off” and “on” status, respectively. Therefore, these two SGTs behave in a similar way to the operation of the NMOS and PMOS transistors in the conventional complementary-metal-oxide-semiconductor (CMOS) inverters.

4.3.2 Characterization of SGI

The strain-voltage transfer characteristic (SVTC) and noise margins of the NW SGI are obtained by plotting the measured output voltages versus corresponding gate strains (Figure 28). V_{OH} and V_{OL} represent the high and low output voltages of the SGI, with ideal values of $V_{OH} = V_{DS} = 1$ V and $V_{OL} = 0$ V. The experimental values for V_{OH} and V_{OL} are 0.98 V and 0.0001 V respectively. The smaller measured value for V_{OH} than the applied 1 V is due to the voltage drop across the SGT that is at “on” status. The logic swing of the SGI defined to be (V_{OH} - V_{OL}) is 0.98 V. The switching threshold strain of the SGI, ε_I, at which the output of the SGI switches between logic high and low status, is obtained at point C with strain value of -0.6% in Figure 28. The slope value of the dashed line connecting the origin point and point C in Figure 28 is 1. In order to characterize the effect of input gate strain on the SGI output, the largest input strain for generating output logic “1”, ε_{IL}, and the smallest input strain for inducing output logic “0”, ε_{IH}, are determined at the pseudo unit gain points A and B (Figure 28) with strain values of -0.8% and -0.38%, respectively. ε_{IL} and ε_{IH} are defined as pseudo unity gain points on SVTC curve for the following considerations.

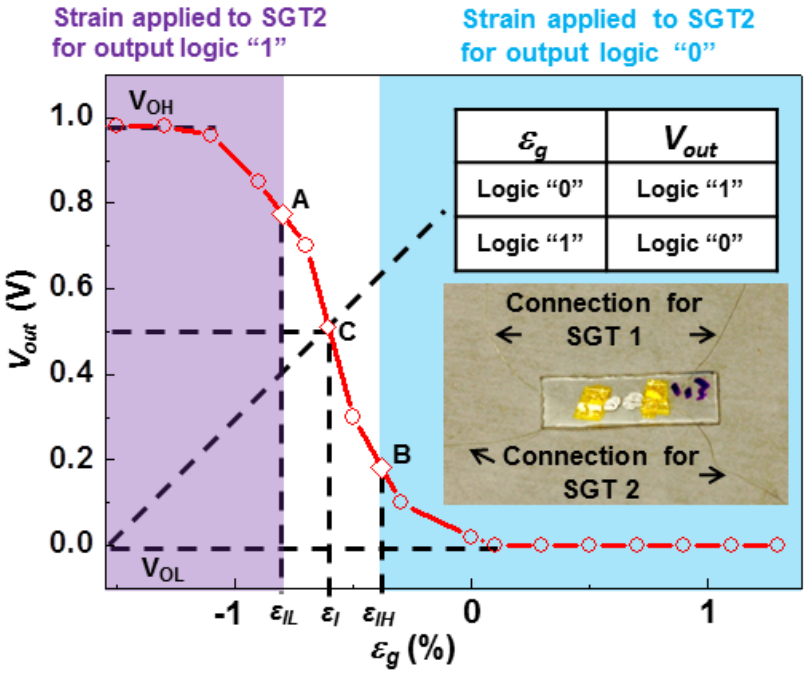


Figure 28. The strain-voltage transfer characteristic (SVTC) and noise margins of the ZnO NW SGI with V_{DS} = 1 V. Inset, optical picture of a ZnO NW SGI, with two SGTs and four connecting wires.

Assume there is noise perturbations on gate input strain ε_g, then $V_{out} = f(\varepsilon_g + \varepsilon_{noise})$. Using first-order approximation and Taylor series expansion:

$$V_{out} = f(\varepsilon_g) + (dV_{out}/d\varepsilon_g)\,\varepsilon_{noise} \qquad (24)$$

If the absolute value of pseudo gain ($dV_{out}/d\varepsilon_g$) is larger than 1, noise signal will be "amplified" and might compromise the SGI performance. If, however, the absolute value of pseudo gain ($dV_{out}/d\varepsilon_g$) is smaller than 1, noise signal will then be "filtered" and hence the obtained logic low input and logic high input regions ensure the gain of SGI operating within these two regions is smaller than 1. The slopes of the SVTC curve (red line) at points A and B are both -1. The input strain zone with $\varepsilon < \varepsilon_{IL}$ (= -0.8%) (purple color region in Figure 28) induces the logic output of "1" for the SGI, while input strain zone with $\varepsilon > \varepsilon_{IH}$ (= -0.38%) (bluish color region in Figure 28) induces logic output "0" for the SGI. The negative values for ε_{IL} and ε_{IH} may be due to the fact that some initial strains are unintentionally introduced in the SGTs during the fabrication process. In the logic low input region (purple color region in Figure 28), SGT 1 is on and SGT 2 is off; while in

the logic high input region (bluish color region in Figure 28), SGT 1 is off and SGT 2 is on. The response time of the SGI is dictated by the straining rate, which is an application-dependent factor and the transient property has been investigated for ZnO NW SGI (Figure 29).

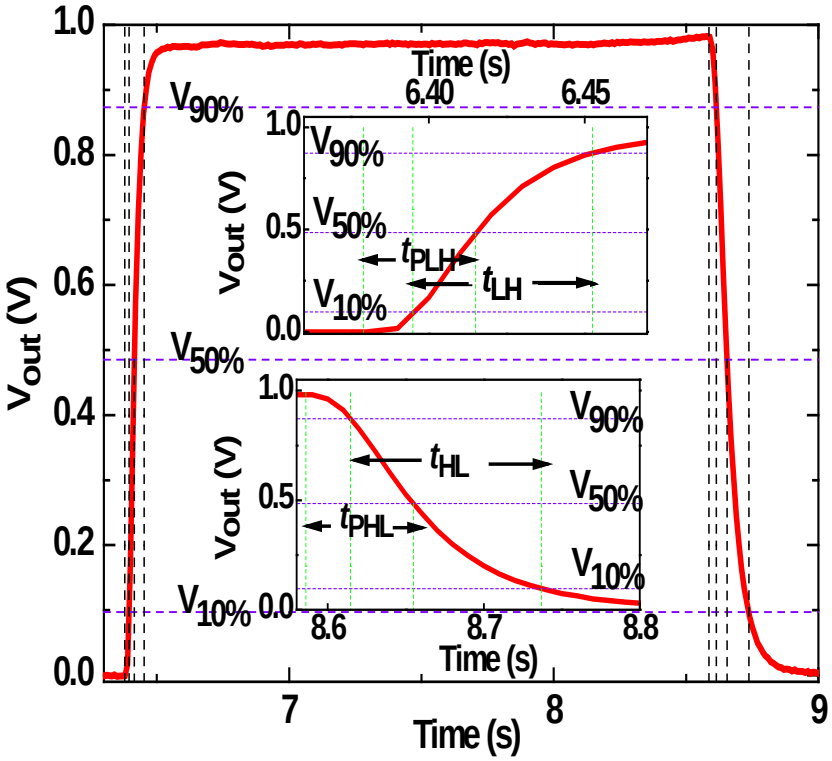


Figure 29. Transient analysis of the ZnO NW SGI. Low-to-high time t_{LH} and high-to-low time t_{HL} represent the minimum response time of the NW SGI. t_{LH} and t_{HL} for a typical ZnO-NW SGI are determined as 0.06s and 0.11s respectively. The maximum switching frequency is hence computed from $f_{max} = 1/(t_{LH} + t_{HL}) = 5.88$ Hz. The propagation delay t_P for the gate is the average time required for a change in the gate input strain to be reflected at the output, which is computed using the time intervals t_{PHL} and t_{PLH} from $t_P = (0.5)(t_{PHL} + t_{PLH}) = 0.249$ s.

The strain-gated logic devices are designed to interface with the ambient environment, which is associated with low-frequency mechanical actions, and the aim and targeting applications are different from those of conventional silicon devices which aim at speed. Switching frequency is not the critical issue as long as the strain-gated logic devices can respond to and process the mechanical signals in a timely manner, such as in applications of nanorobotics, transducers and micro-machine. The applications of SGTs

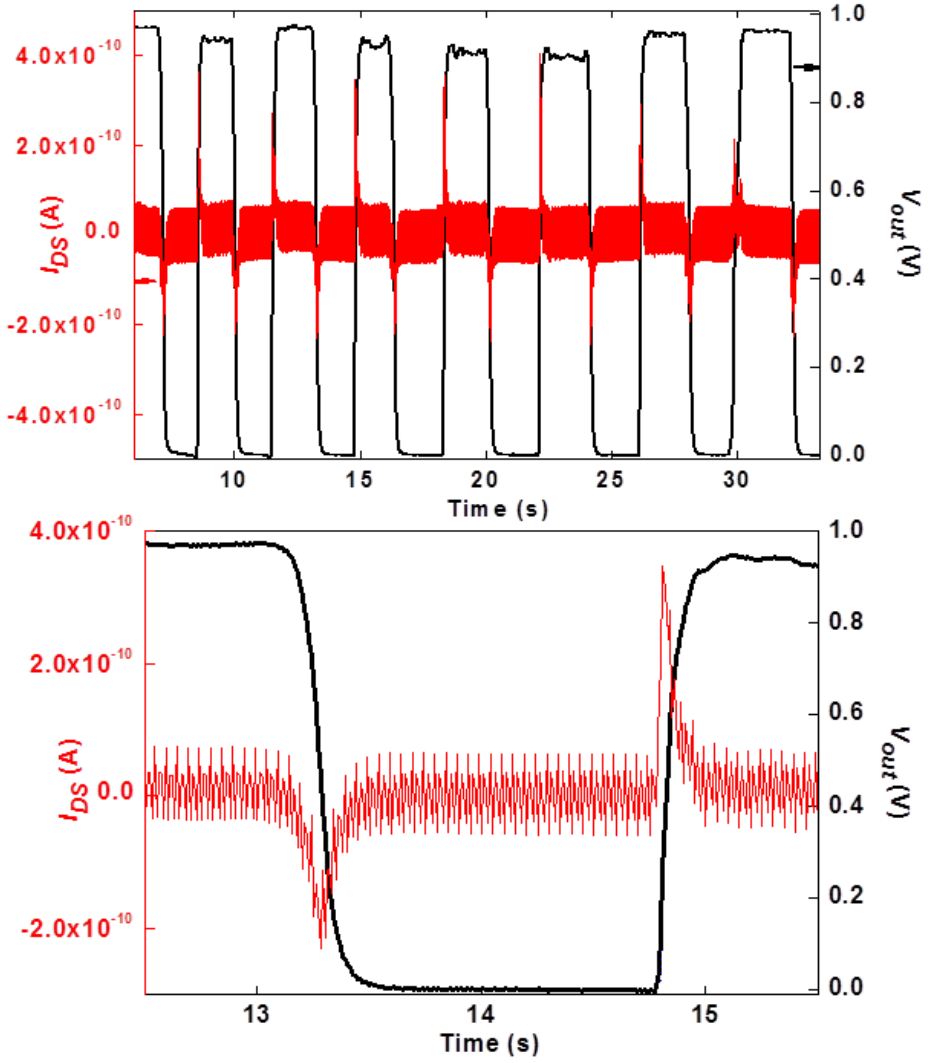


Figure 30. Temporal characteristics of current and voltage on a typical ZnO-NW SGI. The absolute charges for the two current spikes in the magnified part are $1.99\times10^{-11}C$ (negative spike) and $2.97\times10^{-11}C$ (positive spike), respectively. The current spikes resulted from current generating process in the NWs can be negative or positive here depending the sign of straining rate, while the spikes of I_{dp} should be all positive. Therefore, I_{dp} can be determined as around 50 pA using simple superposition calculation.

are complimentary to those provided by conventional CMOS technology. Although there is no electrical gate in the ZnO-NW SGT and hence the gate leakage current can be ignored in the ZnO-NW SGI, unlike conventional CMOS inverter, there is one possible power dissipation source in ZnO-NW SGIs, direct path short-circuit current, I_{dp}. I_{dp} occurs due to the finite slope of the input strain signal, which causes a direct current path between V_{DD} and GND for a short period of time during switching when both the ZnO-

NW SGTs in a SGI are on. The preliminary investigation revealing the existence of I_{dp} can be seen in Figure 30.

4.4 Strain-gated universal logic gates

More sophisticated strain-gated logic operations such as NAND and NOR gates can be realized by further integrating two NW SGIs, which are gated individually by the applied strains, according to corresponding connection rules (Figures 31a1 and a2 for NAND gate and Figures 31b1 and b2 for NOR gate). The output voltages of NAND and NOR gates versus the input gate strains are shown in Figure 31a3 for NAND gate and Figure 31b3 for NOR gate. Two types of transitions occur during the switching operation of both the ZnO NW strain-gated NAND and NOR gates, which have been tabulated (Tables 1 and 2). It can also be seen that NW strain-gated NAND and NOR gates with active loads, which are the NWs, (Figures 31a3 and b3) exhibit better overall performance, such as larger logic swing, compared to passive-load NAND and NOR gates (Figures 32a and b).

The strain-gated ZnO NW XOR logic was also realized by connecting two SGTs in parallel (Figs. 4a). The drain electrode of SGT 1 in Fig. 4a is connected to the electrical input V_A while the drain electrode of SGT 2 is connected to $V_{\bar{A}}$, which is the logically complement electrical input to V_A. If the strain gated input logic for SGT 2 is B, then the strain input logic for SGT 1 is $\overline{B}$. The change in the connections of the electrodes from those demonstrated in the NW SGI results in different logic functions. When the substrate is bent downward or upward, the electric output would be either V_A or $V_{\bar{A}}$, with the overall output of the device logically expressed as $V_{out} = \overline{B}\,V_A + BV_{\bar{A}}$, which is the XOR logic. The output voltages of the XOR gate versus the input gate strains are shown in Figure 33b.

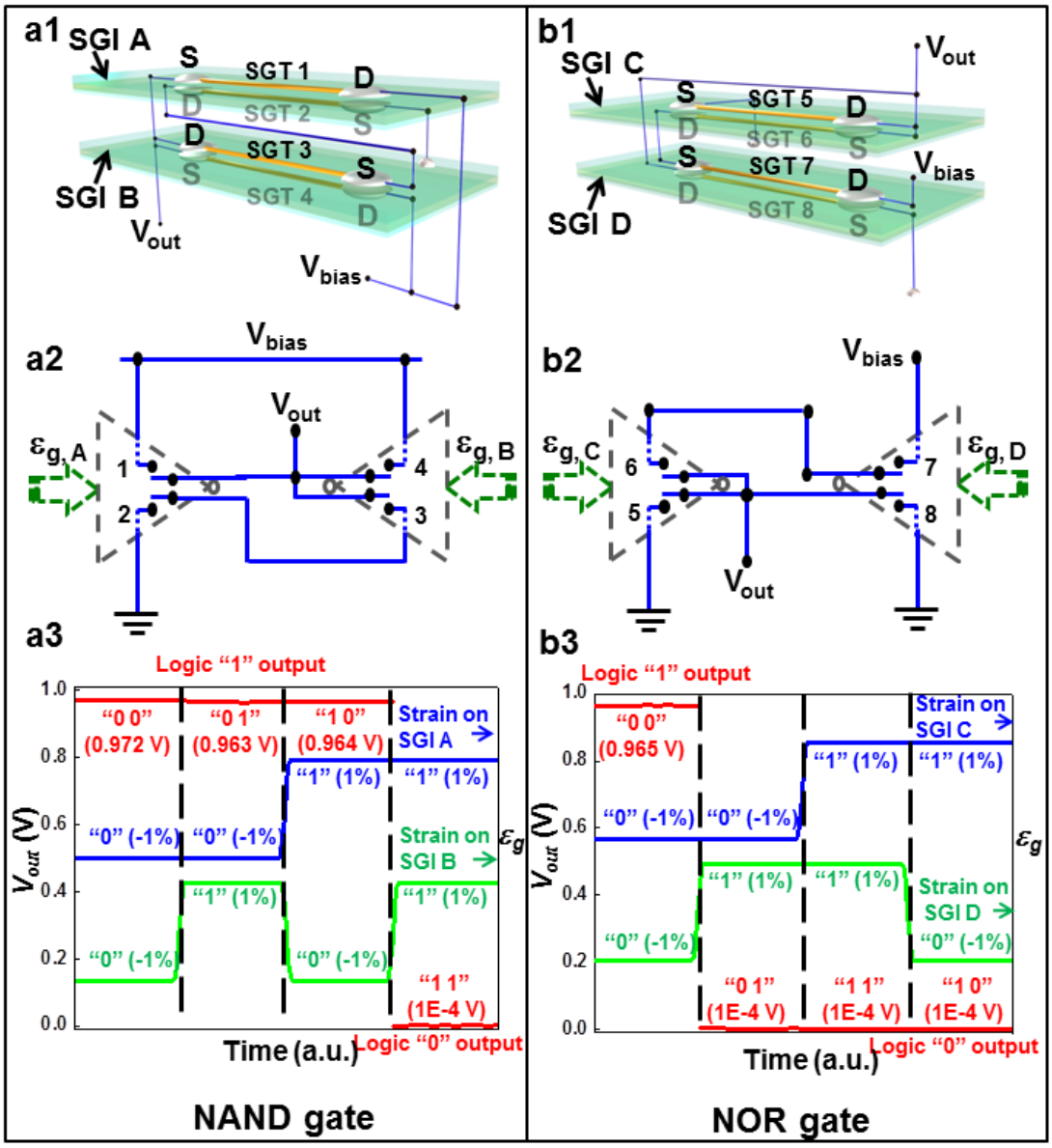


Figure 31. Schematics and operations of ZnO NW strain-gated NAND and NOR logic gates. a1-a3) ZnO NW strain-gated NAND gate. b1-b3) ZnO NW strain-gated NOR gate. a.u., arbitrary units.

If drain electrodes of SGT 1 and SGT 2 in Figure 33a are connected independently to arbitrary electrical input signals D_1 and D_0 rather than logically complements (V_A and $V_{\bar{A}}$), the XOR gate demonstrated above is essentially a 2:1 multiplexer (MUX), with a control bit B that is the input strain logic applied on SGT 2. Analogously, an n:1 MUX enables us to pick one of the n inputs and direct it to the output. When B is logic "1", SGT 1 is off and the output is determined by the input

connected to the drain electrode of SGT 2. Conversely, when B is logic “0”, SGT 2 is off and the output is determined by the input connected to the drain electrode of SGT 1. Reversely, if the inputs D_1 and D_0 act as the output ports and the output for MUX as the input side, the device acts as a demultiplexer (DEMUX). The circuit can be expanded easily to create larger MUXs based on the above basic structures. The NW strain gated MUXs and DEMUXs are critical logic components for processing mechanic-electrical signals.

Table 1. One kind of transition changes the on/off status for all four SGTs, such as the case happening in the first two columns of Table S1 (with purple color). The other kind of transition changes the on/off status for only two SGTs, like the cases happening in the last four columns of Table S1 (with bluish color). The two numbers in the quotation marks represent the logic levels for strain inputs on the SGIs in a ZnO NW strain gated NAND gate.

	“0 0” → “1 1”		“0 1” → “1 1”		“1 0” → “1 1”	
SGT 1	**On**	**Off**	**On**	**Off**	**Off**	**Off**
SGT 2	**Off**	**On**	**Off**	**On**	**On**	**On**
SGT 3	**Off**	**On**	**On**	**On**	**Off**	**On**
SGT 4	**On**	**Off**	**Off**	**Off**	**On**	**Off**

Table 2. One kind of transition changes the on/off status for all four SGTs, such as the case happening in the first two columns of Table S2 (with purple color). The other kind of transition changes the on/off status for only two SGTs, like the cases happening in the last four columns of Table S2 (with bluish color). The two numbers in the quotation marks represent the logic levels for strain inputs on the SGIs in a ZnO NW strain gated NOR gate.

	“0 0” → “1 1”		“0 0” → “1 0”		“0 0” → “0 1”	
SGT 5	**Off**	**On**	**Off**	**On**	**Off**	**Off**
SGT 6	**On**	**Off**	**On**	**Off**	**On**	**On**
SGT 7	**On**	**Off**	**On**	**On**	**On**	**Off**
SGT 8	**Off**	**On**	**Off**	**Off**	**Off**	**On**

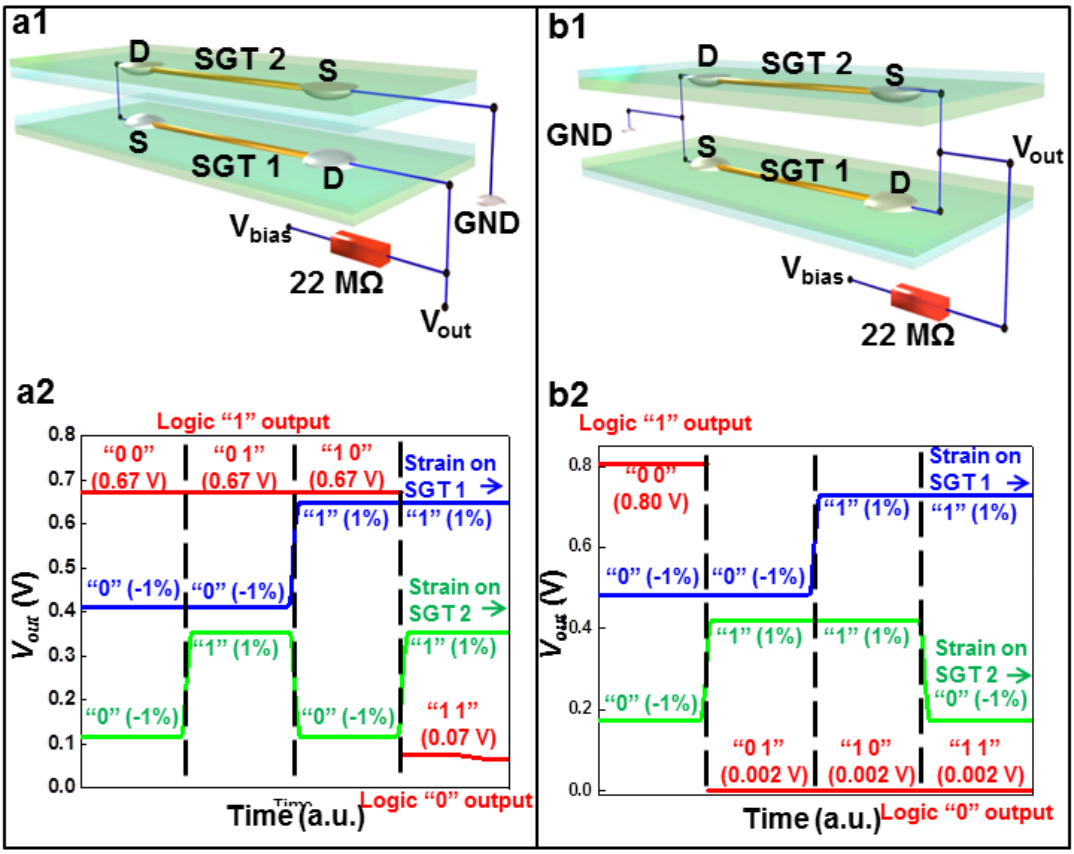


Figure 32. a1) Schematic of a resistive-load ZnO NW NAND gate constructed from serial connection of two ZnO NWs. a2) Logic operations and experimental truth table of the resistive-load ZnO NW NAND logic gate. b1) Schematic of a resistive-load ZnO NW NOR gate constructed from parallel connection of two ZnO NWs. b2) Logic operations and experimental truth table of the resistive-load ZnO NW NOR logic gate.

4.5 Summary

In summary, by utilizing the gating effect produced by piezoelectric potential in a ZnO NW under externally applied deformation, SGTs have been fabricated, using which the universal logic operations such as NAND, NOR and XOR gates have been demonstrated for the first time for performing piezotronic logic operations. In contrast to the conventional CMOS logic units, the SGT based logic units are driven by mechanical agitation and relies only on *n*-type ZnO NWs without the presence of *p*-type semiconductor components. The mechanical-electronic logic units can be integrated with NEMS technology to achieve advanced and complex functionalities in nanorobotics,

microfluidics and micro/nano-systems. Recently, the integration of the other two important components in self-powered autonomous intelligent nanoscale system, the energy harvesting and the sensing/detecting parts, has been demonstrated[22] and ZnO piezotronic logic devices can be further integrated with the ultrasensitive ZnO NW sensors and ZnO NW based nanogenerators to achieve self-sustainable, all nanowire based, multifunctional self-powered autonomous intelligent nanoscale system.

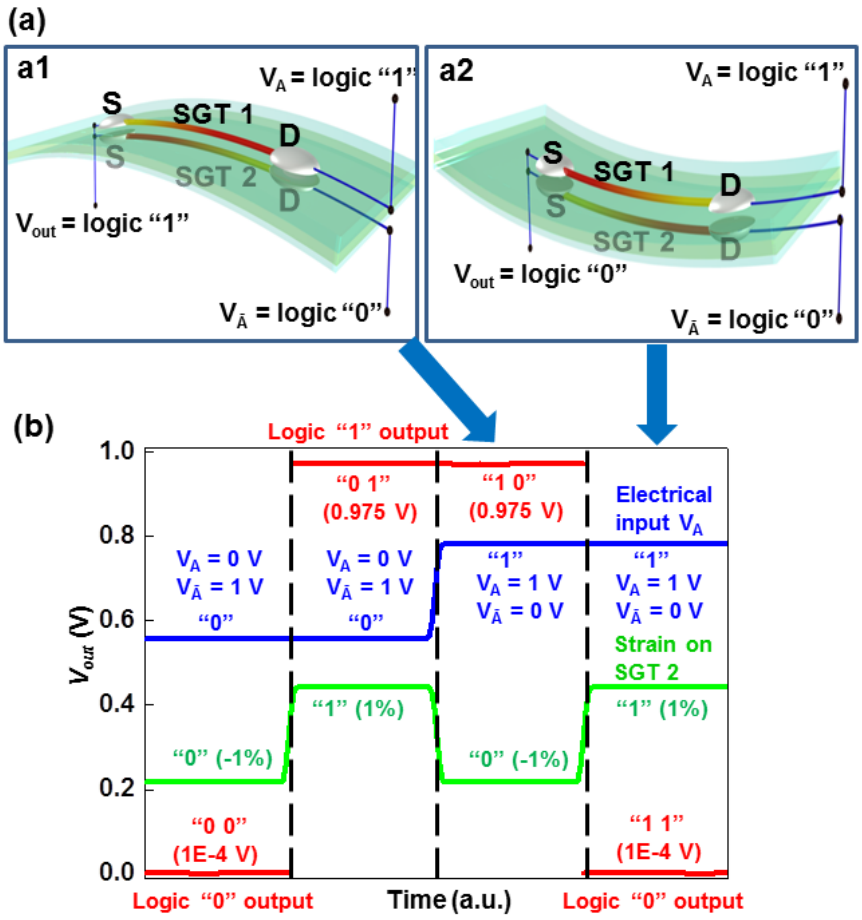


Figure 33. ZnO NW strain-gated XOR logic gate. a1-a2) Schematics of a ZnO NW XOR logic gate performing logic operations on strain and electrical inputs. b) Logic operations and experimental truth table of the ZnO NW strain-gated XOR logic gate.

CHAPTER 5

PIEZOTRONIC NANOWIRE BASED RESISTIVE SWITCHES AS PROGRAMMABLE ELECTROMECHANICAL MEMORIES

5.1 Background

The concept of complementing field effect transistors (FETs) with two-terminal hysteretic resistive switches has recently attracted a great interest in implementing and scaling novel nonvolatile resistive memories[162-166] for ultrahigh density memory storage[167,168] and logic applications[169,170] with characteristics such as high-density, low cost, fast write/read accessing speed and long endurance/retention time[171]. Notably, previous existing non-volatile resistive memories are all based on electrically switchable resistance change[171] by means of formation of conductive filaments [166,172], charge-transfer-induced conformational change[173], electrochemical processes[174], or field-assisted drift/diffusion of charged ions[164,165,167,175] in various oxides and ionic conductors[176-178]. These devices are electrically programmed and they are not suitable for direct interfacing with actuation/triggering other than electrical inputs. For applications such as human-computer interfacing, sensing/actuating in nanorobotics, and smart MEMS/NEMS[11,179], a direct interfacing of electronics with mechanical actions is required.

In this chapter the first piezoelectrically-modulated resistive switching device based on piezotronic ZnO nanowire (NW) will be presented, through which the write/read access of the memory cell is programmed via electromechanical modulation. Adjusted by the strain-induced polarization charges created at the semiconductor/metal interface under externally applied deformation by the piezoelectric effect, the resistive switching characteristics of the cell can be modulated in a controlled manner, and the logic levels of the strain stored in the cell can be recorded and read out, which has the

potential for integrating with NEMS technology to achieve micro/nano-systems capable for intelligent and self-sufficient multi-dimensional operations[10,179,180].

5.2 Structure and fabrication of piezoelectrically-modulated resistive memory

The basic structure of the piezoelectrically-modulated resistive memory (PRM) is shown in Figure 34a1 (Inset), which consists of a ZnO piezotronic NW that is in contact with Au electrodes fabricated by lithography on a flexible PET substrate (from DuPont, thickness ~ 1.25 mm). The two electrodes are labeled as the drain (D) and source (S) electrodes of the PRM cell. The single-crystalline ZnO NWs used in PRM devices were synthesized via a physical vapor deposition process[65] with diameters of 500 nm and lengths of 50 μm (Figure 34a1 Inset). ZnO NWs grown on alumina plates were transferred to the PET receiving substrate by sweeping the PET substrate across the NWs. ZnO NWs were detached from alumina plate and aligned on the PET substrate along the sweeping direction due to the applied shear force, with an estimated average density of 500 cm^{-2} (Figure 35), and the average density of drain/source electrodes pair is around 350 cm^{-2}. An optimized density of transferred ZnO NWs is important to insure that single ZnO NW is patterned between the same group of drain/source electrodes for subsequent photolithography and characterization steps. If the density is too high, multiple NWs are readily patterned between the drain/source electrodes, which can complicate the device configuration and obscure the subsequent characterization as well as the analysis of the device characteristics. On the other hand, if the density is too low, then the fabrication yield of the process shrinks significantly. Electrode patterns over the transferred ZnO NWs were defined using photolithography and then followed by evaporating 350 nm thick Au film (E-beam evaporation). After lift-off step, a substantial amount of the ZnO NWs was patterned with ordered Au electrodes (Figure 35). Au electrodes form Schottky contacts with the ZnO NWs, which are critical for a working piezotronic device. Finally,

the entire substrate can be further packaged with a thin layer of PDMS to enhance mechanical robustness.

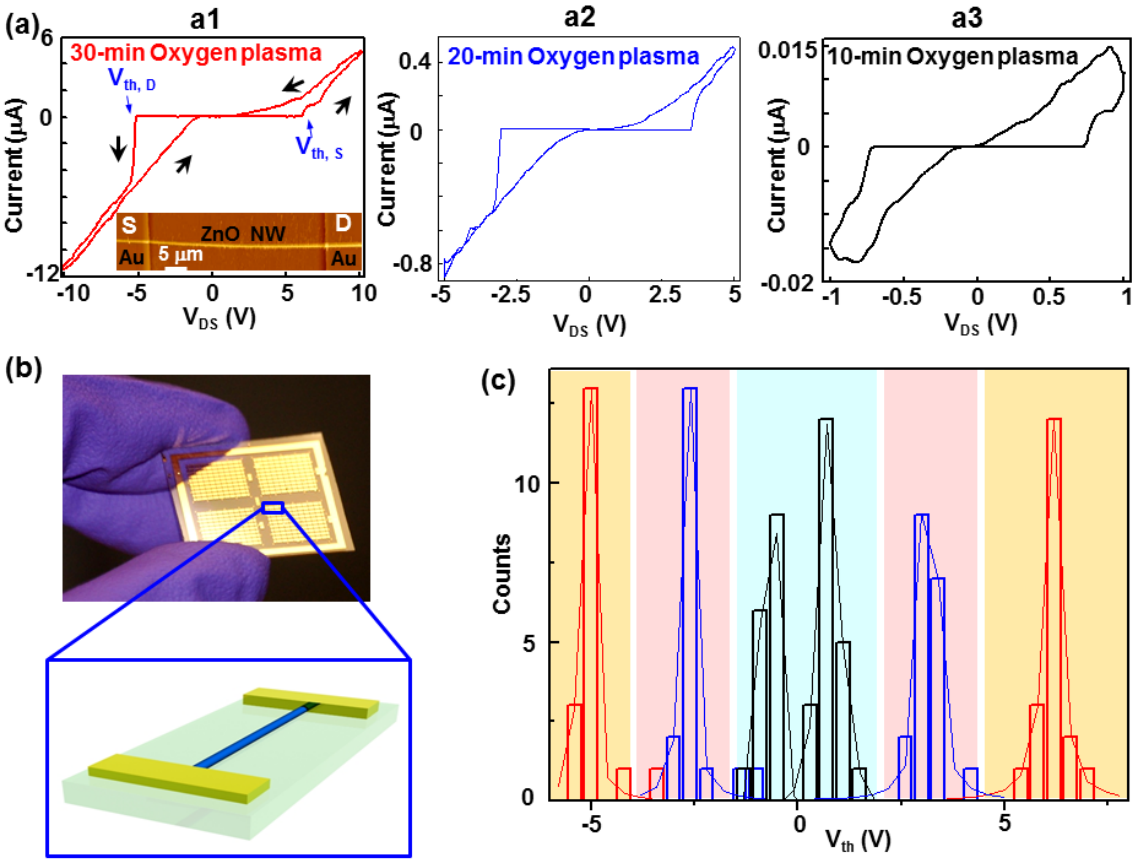


Figure 34. Effects of oxygen plasma treatment on electrical properties of ZnO PRM cells. (a) a1-a3 *I-V* characteristics of ZnO PRM cells after 30, 20 and 10 minutes oxygen plasma treatment. a1 Inset, Atomic force microscopy (AFM) image of one ZnO PRM cell. (b) Optical image of the large-scale as-fabricated PRM cells after printing transfer of ZnO NWs and lithography patterning of metal electrodes. (c) Statistical distributions of the $V_{th,S}$ and $V_{th,D}$ peaks for PRM cells with different periods of oxygen plasma treatment. Red, blue and black lines are for PRM cells with 30, 20 and 10 minutes oxygen plasma treatment, respectively.

The PRM cells were then treated in oxygen plasma for 30 minutes before further characterization. Plasma treatment using argon or oxygen gas was performed on a plasma cleaning system (South Bay Technology, Inc., PC-150) in order to investigate the effect of pre-treatment on the performance and consequently the underlying working mechanism of the PRM cell. For both the argon and oxygen plasma treatment, the

chamber pressure was maintained at 170 mTorr during the process. The forward power used was 30 Watts with the reflected power of 0 Watt. The duration time of plasma treatment was programmed to be from 10 to 30 minutes for different groups of PRM cells investigated.

5.3 Characterization of PRM

5.3.1 Electro-mechanical characterization

A typical PRM cell used for the electro-mechanical characterizations consisted of a single ZnO NW with diameter of 300-500 nm and length of 50-100 mm. The mechanical deformations were applied onto the PRM cells using a 3-axis linear stage (Newport, Inc., 460P-XYZ-05). Electrical measurements were carried out with a computer-controlled data acquisition system, which consists of a function generator (Stanford Research Systems, Inc., DS345), a low-noise current preamplifier (Stanford Research Systems, Inc., SR570) and a shielded connector block with signal-labeled BNC connectors (NI BNC2120). For each strain state of the PRM cell, the output current was obtained by sweeping the DC bias across the device at a fixed frequency of 0.1 Hz. Once the substrate is deformed, a pure tensile/compressive strain is created in the NW since the mechanical behavior of the entire cell structure is determined by the substrate (Figure 34b). All of the *I-V* curves presented was measured at a sweeping frequency of 0.1 Hz at room temperature unless otherwise noted.

Several key features can be observed from the representative hysteretic *I-V* curve obtained for a single ZnO PRM cell (treated with 30-minute oxygen plasma) without applying an external strain (Figure 34a1). First, as the bias voltage increased from 0 to 10 V, the output current of the PRM cell increased abruptly at 5.73 V, which is defined as the threshold point $V_{th,S}$. An abrupt transition and switching from high-resistance state (HRS) to low-resistance state (LRS) occurred at $V_{th,S}$. Secondly, as the voltage was subsequently decreased towards negative values, the PRM cell switched back to the high-

resistance OFF state. Thirdly, when the bias voltage exceeded certain negative values ($V_{th,D}$ = - 5 V in Figure 34a1), the PRM cell was turned to the ON state again and subsequent decrease in magnitude of the negative bias voltage switched the PRM cell back to the OFF state. This hysteretic sweeping sequence is indicated by arrowheads in Figure 34a1. The overall resistive switching observed for a single PRM cell is unipolar since the switching sequence is independent of the polarity of the bias voltage[171] (Figure 34a1), which can be understood by the symmetry in structures of the PRM cells. Current rectification, which can minimize cross talk between individual memory cells and solve the sneak path problem in potential large-scale ultra-high density applications[181,182], was also observed, suggesting that the PRM cell can be modeled as two back-to-back Schottky barriers connected in series with the NW in the metal-semiconductor-metal (M-S-M) configuration and the LRS state of the cell is dictated by Schottky-like transport at one of the Au/ZnO interfaces, which will be discussed in details later.

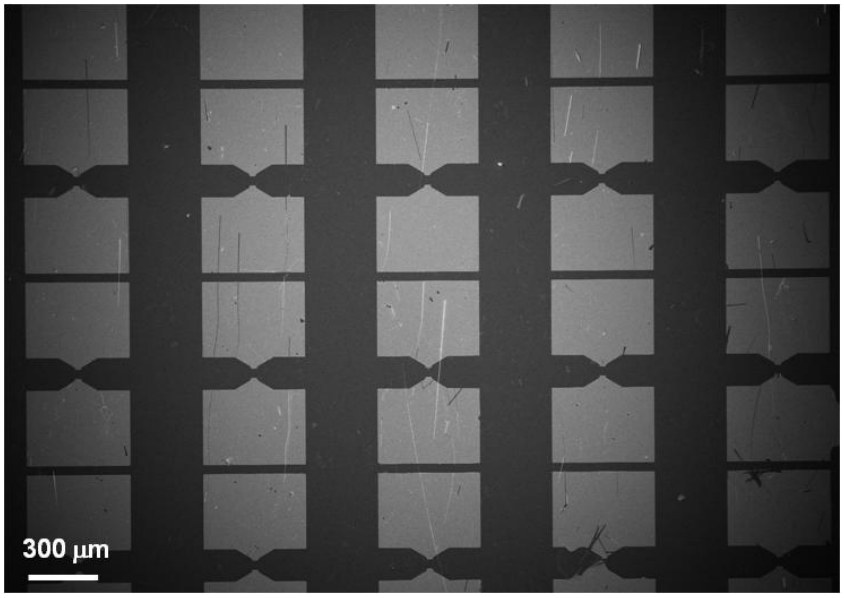


Figure 35. SEM image of the PRM cells array.

5.3.2 Effect of plasma pre-treatment

Noticeably, the *I-V* characteristic of the PRM cell is significantly different from those observed in previous single ZnO NW based piezotronic devices[11,179](orange line in Figure 36), which is proposed to result from the oxygen-plasma treatment prior to the measurement, as elaborated in the following.

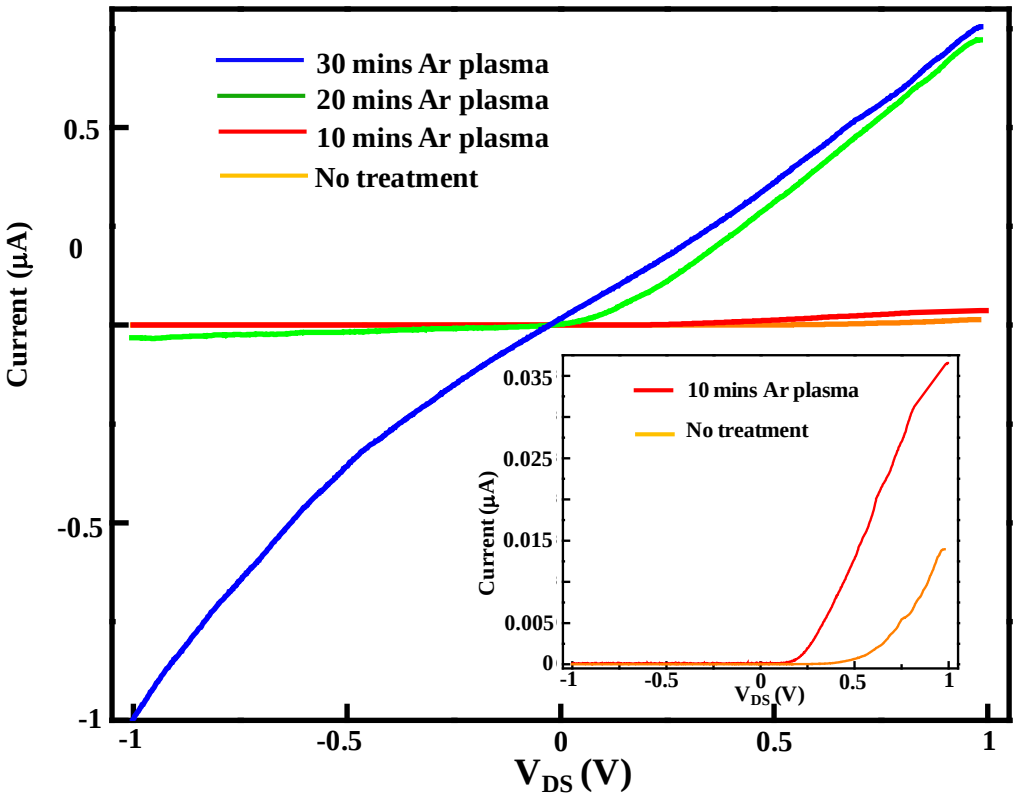


Figure 36. *I-V* curves of PRM cells with argon plasma treatment. For PRM cells treated with argon plasma, the threshold voltages decreased and the conductance increased with respect to the pristine one, as the treatment time increased. The rectification disappeared in the *I-V* curve for PRM cell treated with 30 minute argon plasma. Inset, magnified plot for pristine PRM cell and cell with 10-minute argon plasma treatment.

In order to investigate the effect of pre-treatment on the performance of the PRM cell, six groups of PRM cells were electrically characterized after different plasma pre-treatments. The first three groups were treated with oxygen plasma for 30, 20 and 10 minutes, respectively and the typical *I-V* curves are shown in Figure 34a1-a3. The rest three groups of PRM cells were treated with argon plasma for 30, 20 and 10 minutes and

their individual typical *I-V* curves are shown in Figure 36, respectively. The *I-V* curve of the PRM cell directly assembled without pre-treatment (pristine PRM cell) is also plotted in Figure 36 for comparison. It can be seen clearly that significant changes occur in the shape, threshold voltage and current range of the *I-V* curves for these samples. With increasing the period of time of treatment with oxygen plasma, the threshold voltage of the PRM cell increased accordingly, and increased hysteresis was also observed in the *I-V* curve (Figure 34a1-a3). If the PRM cell was treated with argon plasma, the threshold voltage decreased and the conductance increased with respect to the pristine one, and finally the rectification disappeared in the *I-V* curve (Figure 36). The observed variations in the *I-V* curves of the PRM cells, which were fabricated using the ZnO NWs synthesized under the same experimental condition, are due to the fact that oxygen vacancies are capable of influencing the Schottky contacts between ZnO and metal electrodes[183]. The synthesis condition (argon atmosphere at high temperature[65]) for ZnO NWs used in the reported piezotronic devices[19, 26, 32] and pristine PRM cells tended to create a large amount of oxygen vacancies in the ZnO NWs, which possibly induced the observed lower threshold voltages of 0.5 - 0.7 V due to the high density of oxygen vacancies near the metal-ZnO interface and pinning of the ZnO Fermi level close to the $V_O^{\bullet\bullet}$ defect level[183]. If, however, the pristine ZnO NWs were treated with additional oxygen plasma for prolonged period of time, the concentration of oxygen vacancies could be largely reduced, which contributed to the observed increase in threshold voltages as well as the hysteresis loop of the *I-V* curves, as shown in Figure 34a1-a3.

The capability in designing the switching characteristics of the PRM cell in a controllable manner is further confirmed by the sharp and distinct statistical distributions of the $V_{th,S}$ and $V_{th,D}$ peaks for PRM cells with different periods of oxygen plasma treatment, with $V_{th,S}$ = 6.15 ± 0.39 V and $V_{th,D}$ = -5.12 ± 0.03 V, $V_{th,S}$ = 3.18 ± 0.20 V and $V_{th,D}$ = -2.67 ± 0.22 V as well as $V_{th,S}$ = 0.74 ± 0.51 V and $V_{th,D}$ = -0.68 ± 0.20 V for PRM cells with treatment for 30, 20 and 10 minutes, respectively, by oxygen plasma

(Figure 34c). The predictable electrical properties of these ZnO NWs with controlled treatment process enable the reproducible assembly of NW structures at large quantity for further applications. The slight difference and asymmetry observed between $V_{th,S}$ and $V_{th,D}$ within each group of PRM cells is possibly induced by the non-uniform geometry of the ZnO NW, as indicated by the AFM image inset in Figure 34a1. It is well known that the Schottky barrier height (SBH) induced at metal/semiconductor interface can be affected by factors such as the geometry and effective areas of the contact[184]. The interface/surface states can also shift the SBH[184]. Moreover, it has been previously reported that Zn-polar surface tends to form higher-SBH barrier than O-polar surface does, even with the same metals[185]. In addition, the morphology of the ZnO NWs has been monitored before and after the plasma treatment and no obvious variations are observed (Figure 37).

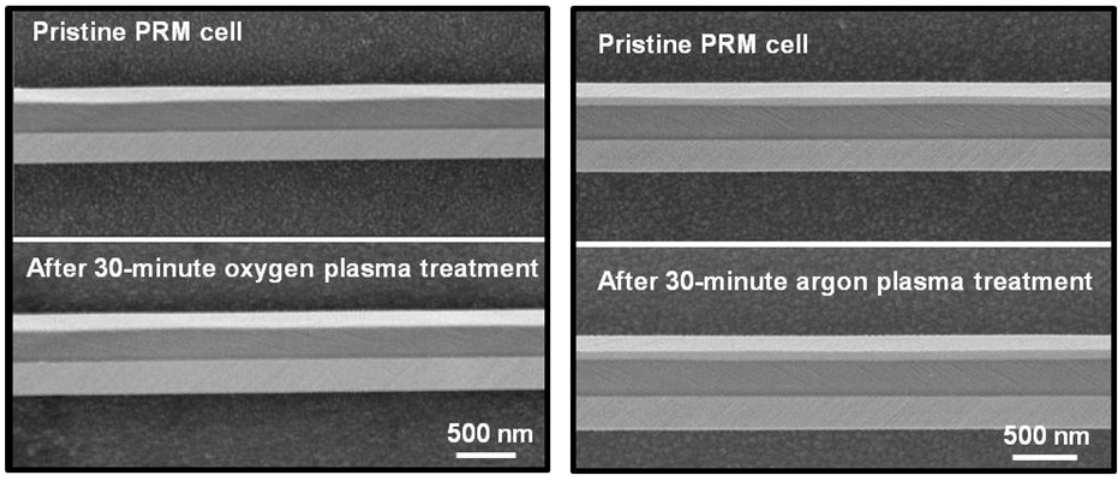


Figure 37. Morphology of ZnO NWs before and after plasma treatment. No obvious variations can be observed in morphology for ZnO NWs before and after plasma treatments.

Notably, as can be seen from the semi-logarithmic curves (Figure 38) for Figure 34a1-a3, the PRM cells gradually lose its non-volatility as the period of oxygen plasma treatment increases. The non-volatility of PRM cells with 10-minute oxygen plasma treatment can be observed by sweeping only positive voltages (0 V-1 V) and the high-

conductance state is not lost at small bias with subsequent sweeps (for 20 cycles) following the high-conductance curve well, which indicates this kind of cells do have the memory effect (Figure 39a). The PRM cells with 30-minute oxygen plasma, however, did not show the same non-volatility in current experiment. Results for retention test are also shown in Figure 39b, which demonstrates the stability of as-fabricated device.

5.3.3 Temperature-dependent *I-V* measurements

Temperature-dependent *I-V* measurements were performed to obtain further insight into the switching mechanism of the PRM cell without applying external deformations. A custom designed 10-pin probe card equipped with BNC interfaces, in addition to the above electrical measurement system, was used to electrically access the PRM cells in the temperature-dependence *I-V* characterization.

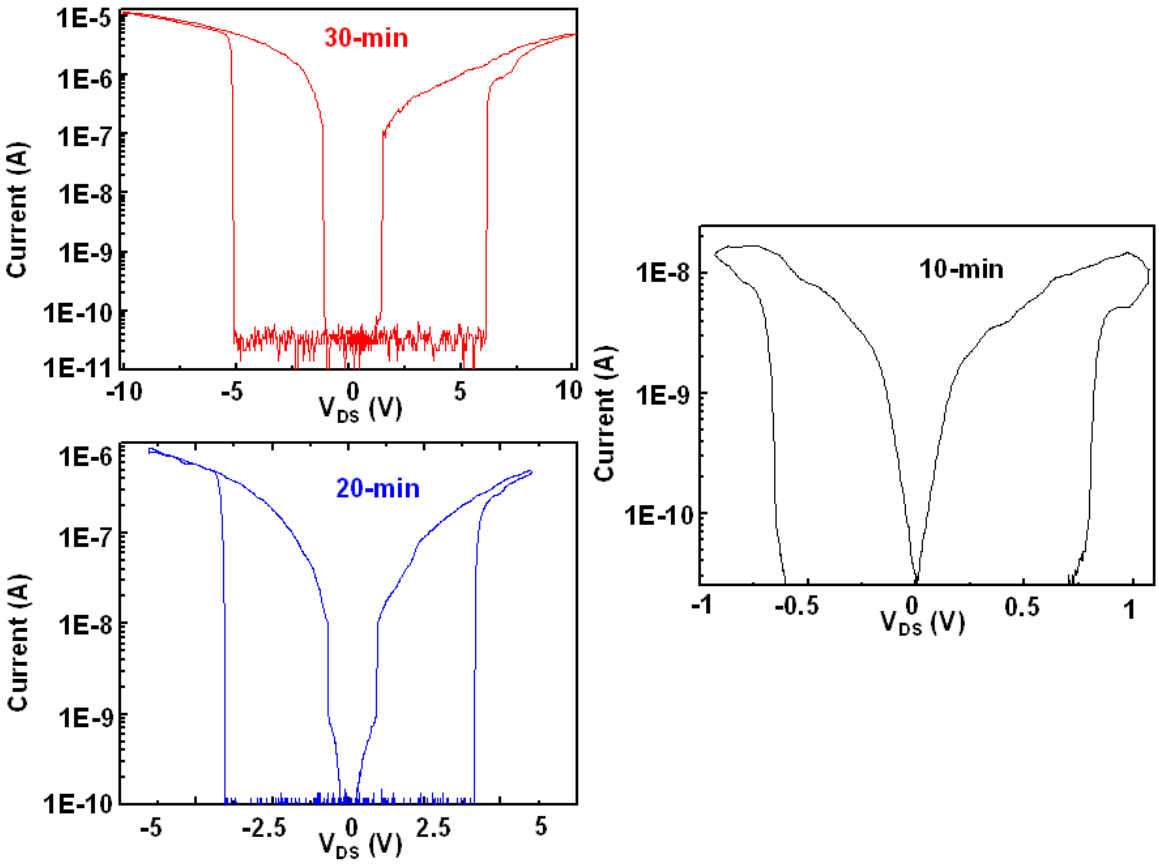


Figure 38. I-V characteristics of ZnO PRM cells after 30, 20 and 10 minutes oxygen plasma treatment.

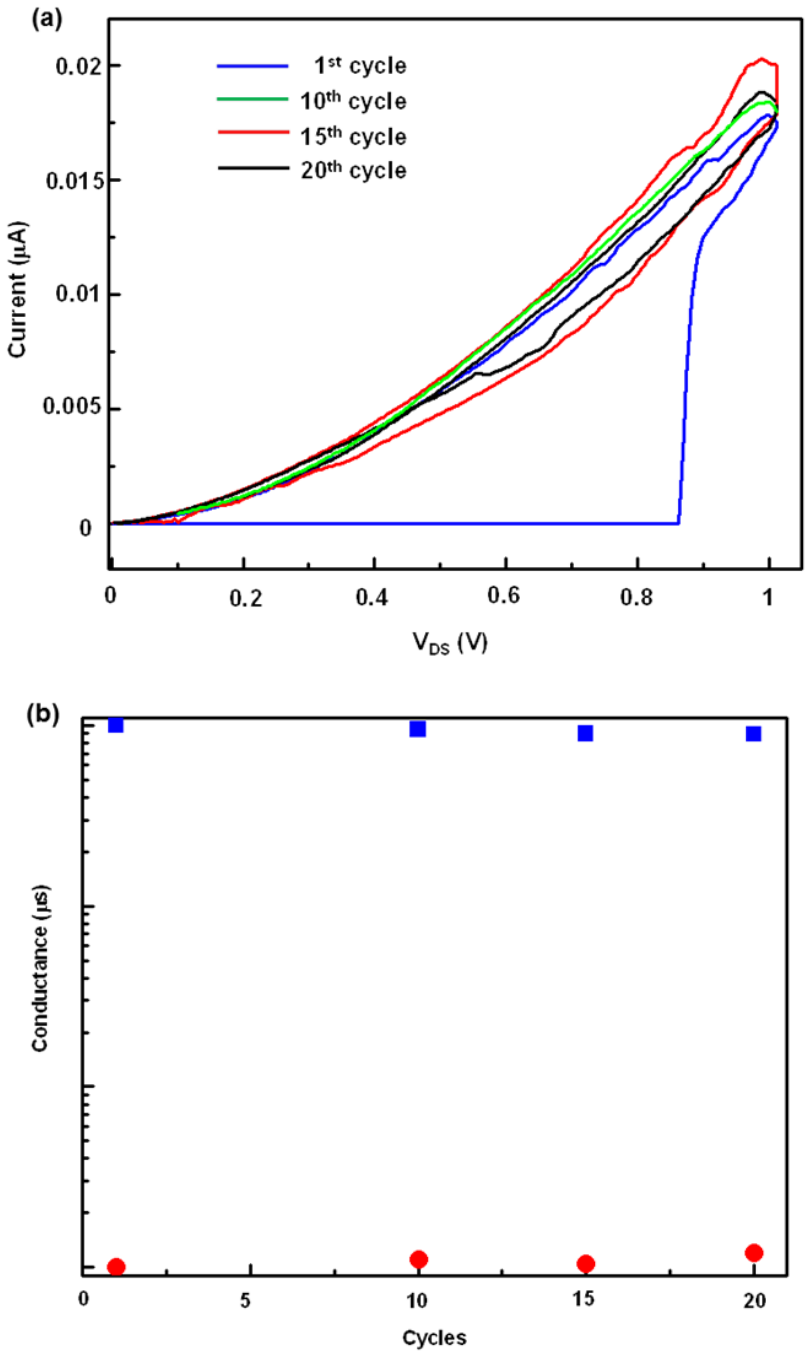


Figure 39. (a) I-V characteristics of ZnO PRM cell (10-minute oxygen plasma treatment) for 20 cycles. The non-volatile characteristic of the ZnO PRM cell with 10-minute oxygen plasma treatment can be seen here. (b) Retention cycle test of ZnO PRM cell (10-minute oxygen plasma treatment) for 20 cycles.

The system used for varying the device temperature consists of a dewar (Janis VPF-800) with a mechanical pump and a precision temperature controller (LakeShore 331). Liquid nitrogen was used to cool down the system temperature. Representative

result acquired from an Au/ZnO-NW/Au PRM cell clearly demonstrates the variations with temperature in the hysteretic *I*-*V* switching characteristics (Figure 40a). The threshold turn-on voltage for the reversely biased Schottky barrier of the PRM cell increased almost linearly with the decreasing temperature (Figure 40b), and the hysteresis loop increased with the decreasing temperature. The magnitudes of the current for PRM cell at very large bias (V = ±10 V) were almost constant and independent of temperature from 350 K to 90 K (Figure 40a).

Although the nature of resistive switching and related charge transport process at microscale in M-S-M structures is still under debate[1-5], the movement of charged species that modulates the current flow seems to be a dominant mechanism[164]. Drift/diffusion of defects such as positively charged oxygen vacancies under applied electrical field has been suggested to change the electronic barrier at the metal/semiconductor interface, which possibly results in the observed resistive switching[165]. Oxygen vacancies are known to be one of the predominant ionic defects in ZnO[186] and can influence the Schottky contacts between ZnO and metal electrodes[183]. On the basis of the experimental results, a general model based on the coupled transport of charged dopants and electrons under applied electric field[165] is adopted and modified to explain the hysteretic switching behavior of the PRM cell without external deformation applied. The drift/diffusion of the oxygen vacancies towards the interface effectively reduces the local SBH, while the drift/diffusion of vacancies away from the interface increases the SBH.

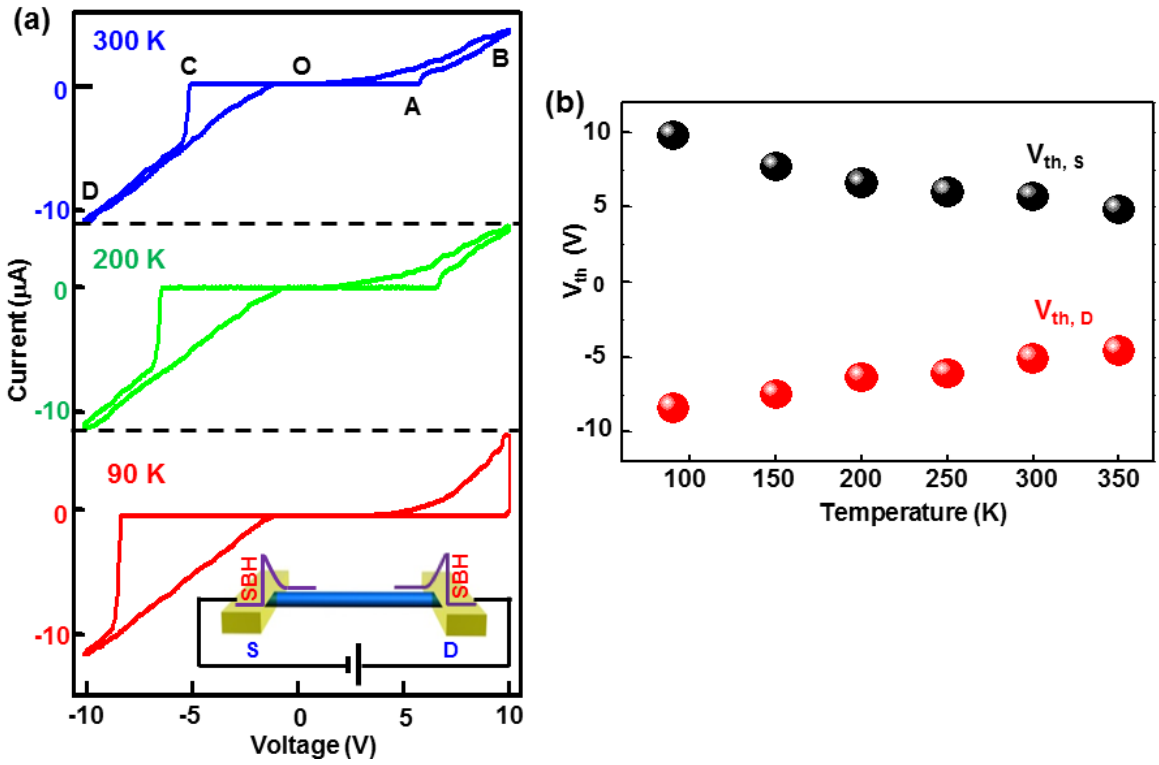


Figure 40. Temperature-dependent *I-V* measurements of PRM cells at strain-free condition. (a) *I-V* characteristics of ZnO PRM cells at 300 K, 200 K and 90 K, respectively. (b) Dependence of threshold voltages on temperature. Both $V_{th,S}$ (in black) and $V_{th,D}$ (in red) increased in magnitudes almost linearly with the decreasing temperature.

The hysteretic switching sequences obtained at different temperatures can be characterized by four typical regions: (1) O-A (2) A-B-O (3) O-C and (4) C-D-O, as labeled in Figure 40a as an example. For easy discussion, the bias is set to be applied on the drain (D) electrode with respect to the source (S) side (Inset sketch in Figure 40a). The overall macroscopic resistance of the PRM cell is $R_{PRM} = R_S + R_{NW} + R_D$, where R_S and R_D are the electrical resistances contributed by Schottky barriers at source and drain sides that may vary during the experiment and R_{NW} is the intrinsic resistance of the ZnO NW. It has been previously demonstrated that for semiconductor NW based M-S-M structure, the *I-V* transport characteristic is normally dictated by the reversely-biased Schottky barrier side[11,187,188]. As the bias voltage sweeps from O to A with the drain side forward-biased, the voltage drops mainly at the reversely biased source side. The total

resistance of PRM cell is $R_{PRM} \sim R_S$ (with $R_S >> R_{NW}, R_D$), which is the HRS state. The lower voltage at the source side attracts oxygen vacancies towards the interface to modify the contact barrier at the source. The switching from HRS to LRS state occurs at a larger bias beyond point A, in corresponding to a largely reduced SBH at the source side. When the bias voltage sweeps from point A to point O through point B, the ln(I)-V curve for region B-O (empty circle in Figure 41), shows that ln(I) relates to $V^{1/4}$, as confirmed by the numerical fitting curve (purple line in Figure 41). This indicates that the thermionic emission-diffusion model dominates the transport at the reverse-biased source barrier[189]. An accelerated diffusion of the oxygen vacancies toward the source side at a large applied voltage and their accumulation are considered as the cause of the hysteresis observed in I-V curve.

As the applied bias switches the polarity from point O to point C, the source side is now forward-biased and the bias voltage drops mainly at the reversely-biased drain side with the total resistance of PRM cell $R_{PRM} \sim R_D$, which is the new HRS state. Oxygen vacancies near the drain side are attracted towards and accumulated at the reversely-biased drain barrier to modify the interface contact, while oxygen vacancies previously piled up at the source side are drifting away. Similar to the case in region O-A, the switch from HRS to LRS state occurs only after a larger bias beyond point C is applied. When the bias voltage sweeps from point C to point O through point D, the ln (I)-V curve for region D-O (empty triangle in Figure 41) can again be numerically fitted using the $\ln(I) \sim V^{1/4}$ relationship (blue line in Figure 41), indicating that the thermionic emission-diffusion model also dominates the transport at the reverse-biased drain barrier.

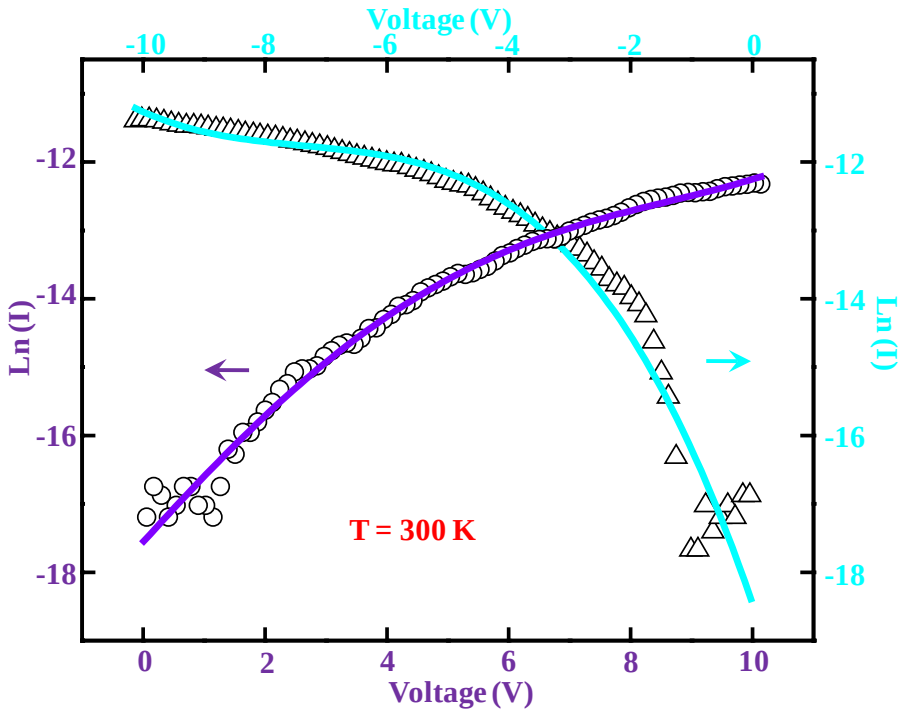


Figure 41. *I-V* characteristic for PRM cell in region O-B and D-O in Figure 40. The numerical fitting curves show ln(*I*) linearly depends on $V^{1/4}$, which indicate thermionic emission-diffusion dominates the transport at the reverse-biased barriers.

It can also be observed that both $V_{th,S}$ and $V_{th,D}$ and hence the width of the HRS window increased as the temperature decreased from 350 K to 90 K (Figure 40b). Qualitatively, this can be understood since the drift/diffusion of the charged ions/dopants and electrons are thermally activated processes. Employing the rigid point ion model derived by Mott and Gurney[190], the diffusion coefficient of oxygen vacancy is given by $D = D_0 \cdot \exp(-E_a/kT)$ and the drift velocity is $v = a \cdot f \cdot \exp(-E_a/kT) \cdot \sinh(qE_a/2kT)$, where E_a is the activation energy, k is the Boltzmann constant, a is the effective hopping distance for the ion to hop between potential wells, f is the attempt-to-escape frequency. At decreased temperatures, larger bias is required to attract sufficient oxygen vacancies towards the respective reversely-biased barrier to switch the PRM cell from HRS to LRS state within the timescale in the experimental setup (the sweeping frequency of the bias signal was 0.1 Hz). The characteristic of PRM cells under sweeping of different rates has also been

investigated primarily for two different frequencies (0.1 Hz and 0.01 Hz). It is interesting to notice that the hysteresis loop shrinks for larger sweeping frequency, while no significant variations can be observed for the turn-on threshold voltage (Figure 42).

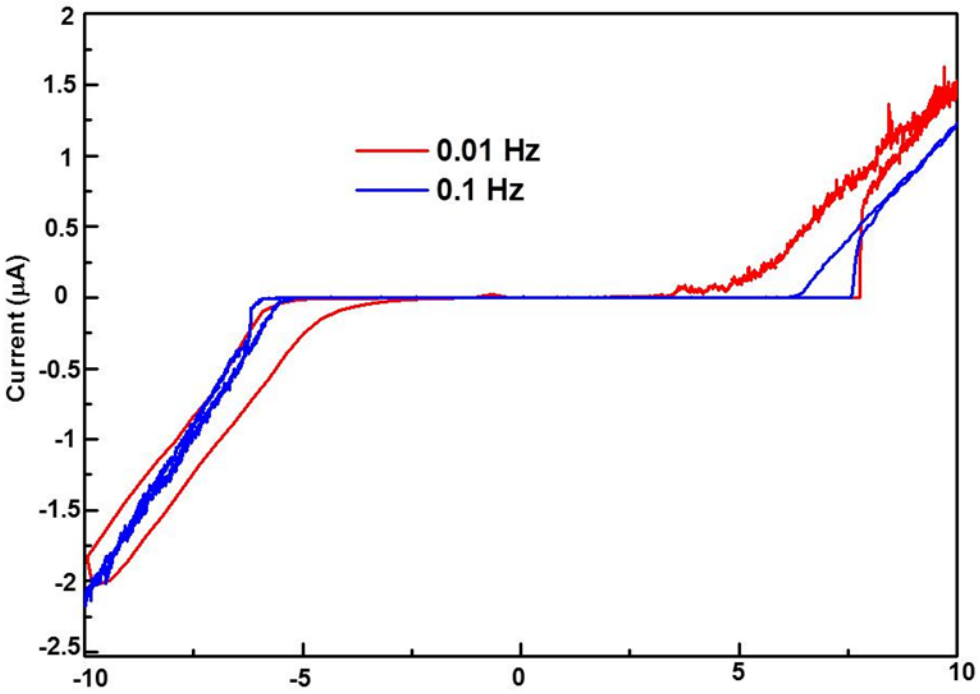


Figure 42. *I-V* characteristics of PRM cell under sweeping of different rates.

5.3.4 Stain-modulated hysteretic switching of PRM cell

The external mechanical perturbation induced strain (ε_g) acts as the programming input for modulating the hysteretic *I-V* characteristics of the PRM cell. A positive/negative strain is created when the ZnO NW is stretched/compressed. Interesting phenomena was observed when a PRM cell experienced straining (Figure 43a). When the PRM cell was tensile stretched (ε = 1.17%), the hysteretic switching curve shifted towards lower voltage side by 1.49 V (red line in Figure 43a); when the cell was compressively deformed (ε = -0.76%), the hysteretic switching curve shifted towards higher voltage side by 1.18 V (blue line in Figure 43a). $V_{th,S+}$, $V_{th,S0}$, $V_{th,S-}$ and $V_{th,D+}$, $V_{th,D0}$, $V_{th,D-}$ are the threshold switching voltages for the PRM cell with tensile, zero and

compressive strains, respectively. The same hysteretic switching curves can then be plotted in a semi-logarithmic current scale to illustrate and highlight the characteristics of the curves (Figure 44a). The ratios of conductance between LRS and HRS for the PRM cell remain steady at high values (~ 10^5) under different strains (Figure 44b), demonstrating the stable performance of the cell and its potential feasibility for applications in flexible memory and logic operations[11].

The intrinsic rectifying behavior of the PRM cell may solve the sneak path problem as well as reduce the static power consumption[182], which allows for construction of large passive resistive-switching device arrays. The changes in threshold switching voltages of the PRM cell with different strains have been plotted in Figure. 3b. It can be seen that the change in both the $V_{th,S}$ and $V_{th,D}$ almost linearly depends on strain applied to the PRM cell, while the width of the HRS window ($V_{th,Si}$ - $V_{th,Di}$, where i = +, 0, -) remains almost constant for different strain values. This strain-modulated change in the threshold switching voltages was also observed for other PRM cells with oxygen plasma treatment.

It is well known that ionic polarization in ZnO can be induced by strain owing to the lacking of center symmetry in ZnO, which can strongly affect the charge transport[179]. Novel effects[191] and applications[11,187,192] have been observed and implemented utilizing the piezotronic effect in ZnO[179]. The fundamental concept of the piezotronic effect is that the SBH at the metal-semiconductor contact can be effectively tuned by the strain-induced piezoelectric polarization charges at the interface. The local conduction band profile can then be modified by shifting the local Fermi level. The change in SBH induced by piezoelectric polarization is given approximately by $\Delta\phi_B = \sigma_{pol} \cdot D^{-1} \cdot (1 + 1/(2q_s w_d))^{-1}$, where σ_{pol} is the volume density of the polarization charge and directly related to the piezoelectric polarization P vector, D is the two-dimensional density of interface states at the Fermi level at the Schottky barrier, q_s is the two-dimensional screening parameter and w_d is the width of the depletion layer[193]. Thus the mechanical strain can

effectively change the local contact characteristics as well as the charge carrier transport process.

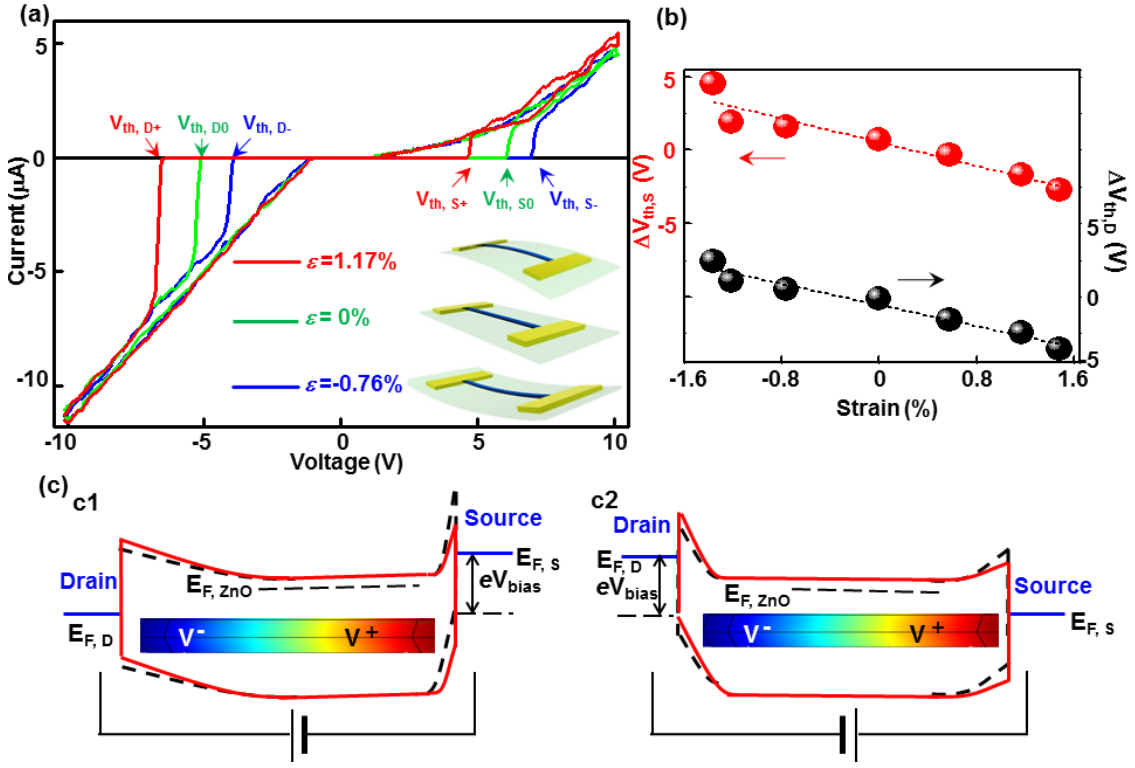


Figure 43. Stain-modulated hysteretic switching of PRM cell. (a) *I-V* characteristics of ZnO PRM cells under tensile, zero and compressive strains respectively. (b) Dependence of threshold voltages on applied strains. (c) Schematic of band-diagram of PRM cell under tensile strain. c1, Schottky barrier at drain side is forward biased. c2, Schottky barrier at drain side is reversely biased. Red solid lines represent band-diagrams after tensile strain is applied. Black dashed lines represent band-diagrams under strain free condition.

Based on the above discussions, the modulation effect of strain on the hysteretic switching behavior of the PRM cell, as shown in Figure 43a-b, can then be understood and explained using the band-diagram of the working device (Figure 43c). If the PRM cell is under tensile strain with the Schottky barrier at drain side being forward-biased (V > 0 in Figure 43a), the positive piezoelectric potential resulting from the positive strain-induced polarization charges reduced the SBH at the reverse-biased source barrier; while the negative piezoelectric potential resulting from the negative strain-induced

polarization charges increased the SBH at the forward-biased drain barrier (red line in Figure 43c1). Since the *I-V* characteristic in this situation is dictated by the reversely-biased source barrier, the existence of strain-induced piezoelectric potential results in the shift of switching threshold voltage from $V_{th,S0}$ to $V_{th,S+}$, indicating only a smaller bias is required to switch the PRM cell from HRS to LRS state. Alternatively, if the Schottky barrier at drain side is reverse-biased ($V < 0$ in Figure 43a), the SBH is still reduced at the source barrier while it is increased at the drain barrier (Figure 43b2) since the polarity of the strain did not change, and hence the piezoelectric potential remained negative and positive at source and drain barriers, respectively. The *I-V* characteristic is now dictated by the reversely-biased drain side in this case, and a shift of switching threshold voltage from $V_{th,D0}$ to $V_{th,D+}$ was observed, indicating a larger bias has to be applied in order to switch the PRM cell from HRS to LRS state. By the same token, in the case of applying a compressive strain to the PRM cell, the shift of switching threshold voltage from $V_{th,S0}$ to $V_{th,S\_}$ and $V_{th,D0}$ to $V_{th,D\_}$ can be explained.

Under strain free condition and if the applied external bias exceeds the threshold voltage, the device is in LRS, and the concentration of oxygen vacancies in the NW can significantly influence the total conductance of the NW as well as the SBHs at the source/drain (see Figures 34 and 36). Now we consider the case that a strain is applied to the PRM cell. The effect of piezopotential can be equivalently taken as applying a positive voltage at the barrier interface if the local piezoelectric polarization charges are positive, which in effect decreases the value of the external bias required to overcome the SBH at the interface. Alternatively, a negative voltage is created to act on the interface if the polarization charges are negative, which increases the value of the external bias required to overcome the barrier at the interface.

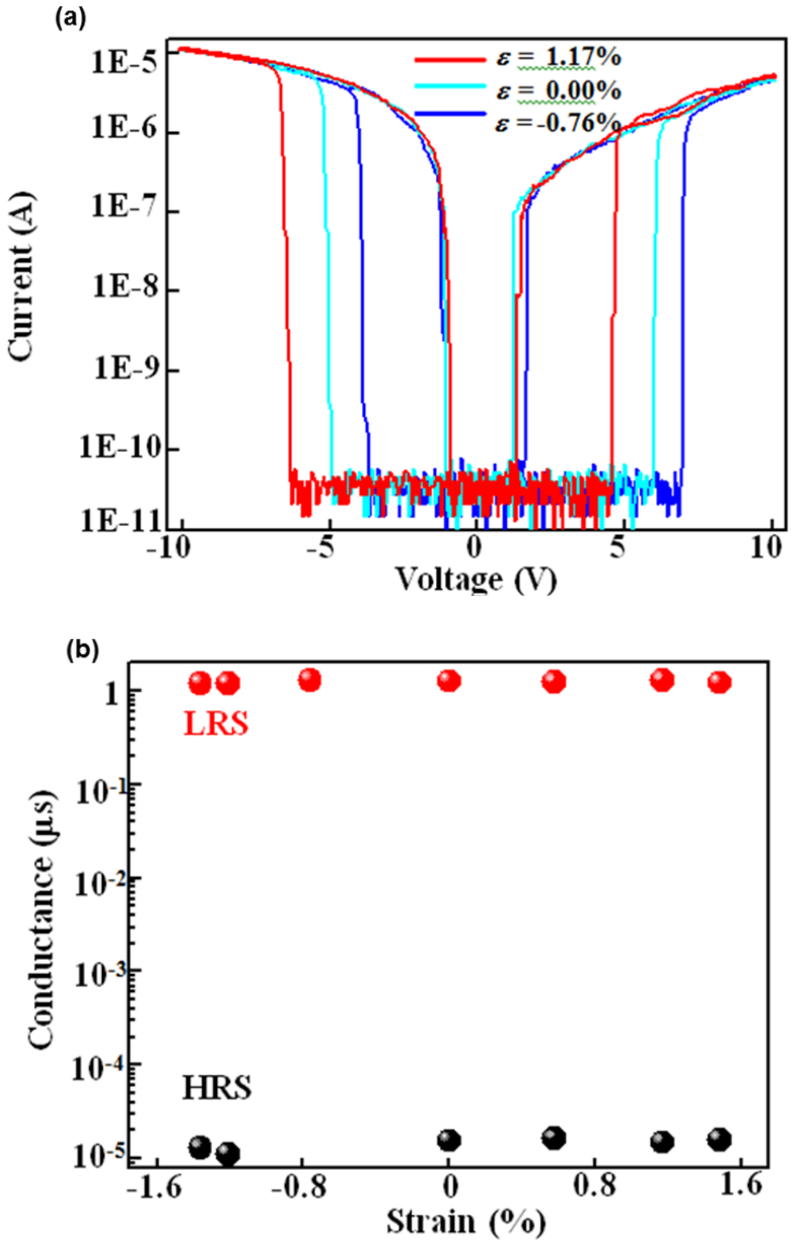


Figure 44. (a) Stain-modulated hysteretic switching curves of PRM cell in a semi-logarithmic current scale. (b) Ratio of conductance at LRS and HRS for the PRM cell under different strains. The ratio of conductance at LRS and HRS remain steady at high values (~ 10^5) under different strains, demonstrating the stable performance of the PRM cell.

From the data shown in Figure 43a, the HRS window remains almost constant regardless the magnitude and sign of the applied strain, indicating the shifts in the observed threshold voltages under different strains are dictated by the piezoelectric

polarization charges at the interfaces and the contribution from the diffusion of the oxygen vacancies has negligible effect. This is because the oxygen vacancies are distributed in the entire NW, while the piezoelectric charges are accumulated right at the very near barrier interface in a region less than a sub-nanometer. The diffusion force contributed by the piezoelectric charges on the oxygen vacancies is a long-range interaction force, thus a variation of the vacancy concentration at the interface owing to piezoelectric effect is rather small. Furthermore, the entire *I-V* curves are "translated" for a constant voltage that is the change of threshold switch voltage caused by the piezoelectric charges. For the samples pre-treated in oxygen plasma, the concentration of the oxygen vacancies was largely reduced in the NW, thus, the screening effect of the free charge carriers to the piezoelectric charges was significantly reduced, and the effect of the piezoelectric charges is enhanced[48]. Therefore, the shifts in threshold switch voltages due to piezoelectric polarization at both drain and source sides for a fixed strain have the same magnitude but opposite polarities, provided that the doping level is low. This indicates that the magnitude of the piezopotential at the interface is as large as 1.2 V at 0.5% ~ 0.76% of strain. The oxygen plasma pre-treatment to the ZnO NWs may also improve the output of the nanogenerator[34].

5.3.5 Operation of PRM cell as electromechanical memory

The fabricated PRM can function as an electromechanical memory, in which the write/read access can be programmed via mechanical actuation. A pulse train consisting of several write/read/erase pulses is applied to the PRM cell to record and read out the polarity/logic levels of the "stored" strain in the cell, by monitoring the characteristic patterns in the output current (Figure 45). The data shown in Figure 45 was obtained for the same PRM cell under different strain status, which is equivalent to the cases of three identical PRM cells under tensile strain (A cell), zero strain (B cell) and compressive strain (C cell), for easy description. First, a positive write pulse (10 ms) with $V_{th,S0}$ <

$V_{write1} < V_{th,S\_}$ is applied to these three cells. This short pulse sets the A and B cells switch from the HRS to the LRS state, while the C cell remains in the HRS state. The status of the three cells are then read out by a read pulse (2 s) with a small magnitude ($V_{read1} < V_{th,S+}$). Subsequently, a negative erase pulse (10 ms) with $V_{th,D0} < V_{erase1} < V_{th,D\_}$ resets the A and B cells from the LRS to the HRS state, while sets the C cell into the LRS state. A follow-up read pulse (2 s) with a small negative value ($V_{read1} > V_{th,D\_}$) is applied to read the new states of the cells. In the third step, a positive erase pulse (10 ms) with $V_{th,S+} < V_{erase2} < V_{th,S0}$ sets the A cell from the HRS to the LRS state again, while keeps the B and C cells in the HRS state. The same V_{read1} pulse is then applied to read the new states of the cells. Finally, a negative write pulse (10 ms) with $V_{th,D+} < V_{write2} < V_{th,D0}$ resets the A cell into the HRS state, while sets the B and C cells into the LRS state. The same V_{read2} pulse is then applied to read the new states of the cells. After the above series of pulse train is applied, the waveform of the output currents of the cells is monitored and analyzed (Figure 45). If the logic levels of the output currents with positive, almost zero and negative values are labeled as “1”, “0” and “-1”, the logic pattern of “1 0 1 0” indicates the positive nature of the “stored” strain in A cell. The logic patterns of “1 0 0 -1” and “0 -1 0- 1” represent the zero and negative strain status of the B and C cells, respectively. A quantitative analysis of the magnitudes of the output currents can give the absolute values of the strains stored in the PRM cells.

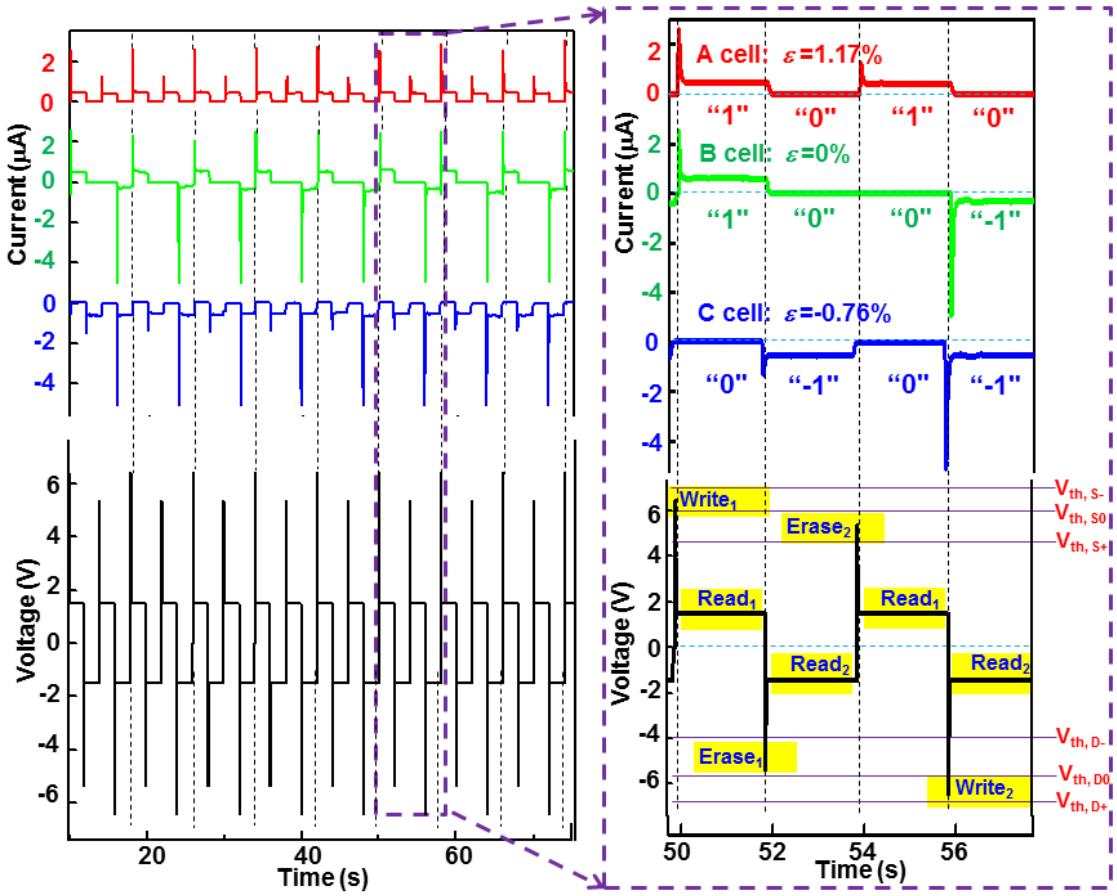


Figure 45. Write/read access of PRM cell as an electromechanical memory.

Although there have been numerous research as well as commercial products on strain detection and measurements such as semiconductor MEMS/NEMS piezoresistive strain gauges[194,195], the PRM cells demonstrated here are fundamentally different from the previous devices. Piezoresistive effect is a non-polar and symmetric effect resulting from the band structure change while the PRM cells are based on the asymmetric piezotronic effect. ZnO is a polar structure along *c*-axis, straining in axial direction (*c*-axis) creates a polarization of cations and anions in the NW growth direction, resulting in a piezopotential drop from V^+ to V^- along the NW, which produces an asymmetric effect on the changes in the Schottky barrier heights (SBHs) at the drain and source electrodes. The strain sensor based on piezotronic effect has been reported to possess much higher sensitivity than previously reported devices[31].

In summary, by utilizing the strain-induced polarization charges created at the semiconductor/metal interface under externally applied deformation as a result of piezotronic effect, the switching characteristics of the ZnO NW resistive switching devices can be modulated and controlled. We further demonstrated that the logic levels of the strain applied on the memory cell can be recorded and read out for the first time utilizing the piezotronic effect[18], which has the potential for implementing novel nanoelectromechanical memories and integrating with NEMS technology to achieve micro/nano-systems capable of intelligent and self-sufficient multi-dimensional operations[179,180]. Taking advantage of the recently developed large-scale fabrication technique of ZnO NW arrays[27], nonvolatile resistive switching memories using ZnO NW array as the storage medium may be readily engineered and implemented for applications such in flexible electronics and force/pressure imaging. Non-Boolean neuromorphic computing might also be realized by integrating arrays of high-density resistive memory cells[196,197] on flexible substrates.

CHAPTER 6

PIXEL-ADDRESSABLE TRANSPARENT-AND-FLEXIBLE MATRIX OF VERTICAL-NW PIEZOTRONIC TRANSISTORS FOR TACTILE IMAGING

6.1 Background

Developing large-scale integration of miniscule functional components on mechanically deformable and optically transparent substrates may lead to revolutionary applications in mechanosensational human-electronics interfacing, sensing and energy harvesting[22,133,198-201]. Significant progress has been achieved recently in implementing flexible pixel-array based pressure sensors for mimicking tactile sensing capabilities of human skins[202-205], in which electronic components like traditional field-effect-transistors (FETs) act as read-out elements for detecting pressure-induced property change in the pressure-sensitive media. Intensive efforts have been devoted to minimize the effect of substrate strain on performance of these electronic components while preserving the deformability of the substrate, forming a newly emerging field of flexible electronics[202-204,206]. This scheme of pressure sensing, whereas, not only requires complicated system integration of heterogeneous components but also lacks proficiency in directly interfacing electronics with mechanical actions in an *active* way that mechanical straining can be utilized to generate new electronic control/feedback. Moreover, the as-fabricated pixel sizes are of hundreds of microns to even tens of millimeters, severely limiting device density and spatial resolution.

Recently, the nanowire (NW) piezotronic transistor was introduced[11,13,30,59] (also see Chapters 4 and 5), based on two-terminal metal-semiconductor-metal (MSM) structure in which the charge carrier transport is modulated by the piezoelectric-polarization-induced inner-crystal potential in the NW at the contacts without applying

the gate voltage as in traditional FET; therefore the transport property of a piezotronic transistor is directly controlled by the local applied force/stress. In addition, the elimination of wrap gate in piezotronic transistors offers an innovative approach for 3D structuring.

In this chapter, the first and by far the largest 3D array integration of vertical NW piezotronic transistors circuitry (92 x 92 pixels in 1 cm^2) as *active* pixel-addressable pressure-sensor matrix for tactile imaging will be demonstrated, enabling a 15-to-25-fold increase in pixel density compared to previous reports[207]. The highest spatial resolution with pixel dimension (20 x 20 μm^2) and pitch size (100 μm) as well as the tactile sensitivity (2.1 $\mu s \cdot kPa^{-1}$) have been demonstrated. The fabricated sensors are capable of mapping profiles of small pressure changes (< 10 kPa). This landmark breakthrough in implementing 3D piezotronic transistor arrays paves innovative routes towards industrial-scale integration of NW piezotronic devices for sensing, micro/nano-systems and human-electronics interfacing.

6.2 Materials, working principles and design strategies

The miniaturized dimensions of nanomaterials together with the capability of modulating their compositions and properties in well-controlled manners not only exhibit the potential for addressing some of the critical challenges faced by silicon-based microelectronics, but also enable the possibility of incorporating diversified functionalities into the systems to complement digital processing with augmented capabilities, such as interactions between machine and human/environment[13,208].

Implementing arrays of transducers in flexible forms that are highly conformable to dynamically curved surfaces and sense the environmental inputs such as ambient mechanical actions is of pivotal importance for developing intelligently accessible interfaces in applications such as robotics and prosthetics. Despite of the numerous efforts devoted to achieve uniformly ordered assembly of various low-dimensional

nanomaterials for addressing the above application needs, planar metal-oxide-semiconductor field-effect-transistor (MOSFET) is still the dominant configuration for implementing functional nanodevices[136,206,209]. Novel architecture like 3D integrated circuits, originally proposed for boosting performance of microelectronic devices as a complement to scaling, has also been adopted to facilitate integration of nanostructure-based planar building blocks, possibly with diverse functionalities, by sequentially assembling them into vertically stacked layers[210-213]. Nevertheless, lack of cost-effective technology for aligning and integrating these nanodevices into circuitry with sufficiently high density hinders further practical applications. Although extending electronic components into vertical dimension with the wrap-gate configuration presents an attractive approach to achieve high-density assembly of functional nanodevices[214], it is cumbersome to fabricate the gate electrode and manage interconnect layout for effectively addressing and controlling individual FET within a high-density device matrix owing to limited space (schematic of a representative wrap-gate 3D NW FET is shown in Figure 46a (left)).

Strain-gated piezotronic transistor operates based on modulation of local contact characteristics and charge carrier transport by strain-induced ionic polarization charges at the interface of metal-semiconductor contact, which is the fundamental of piezotronics[10,11,13,29,158,215,216] (also see Chapter 4). The basic structure of a strain-gated vertical piezotronic transistor (SGVPT) is depicted in Figure 46a (right), consisting of one or multiple vertically-grown ZnO NWs in contact with bottom and top electrodes. ZnO NW experiences strain when subjected to external mechanical deformation, with piezopotential induced inside the NW due to polarization of non-mobile ions[29,158]. The local contact profile and carrier transport across the Schottky barrier, formed between ZnO NW and metal electrodes, can be effectively controlled by the polarization-charge-induced potential. Electrical characteristics of the two-terminal SGVPT are therefore

modulated by external mechanical actions induced strain, which essentially functions as a *gate* signal for controlling carrier transport in SGVPT.

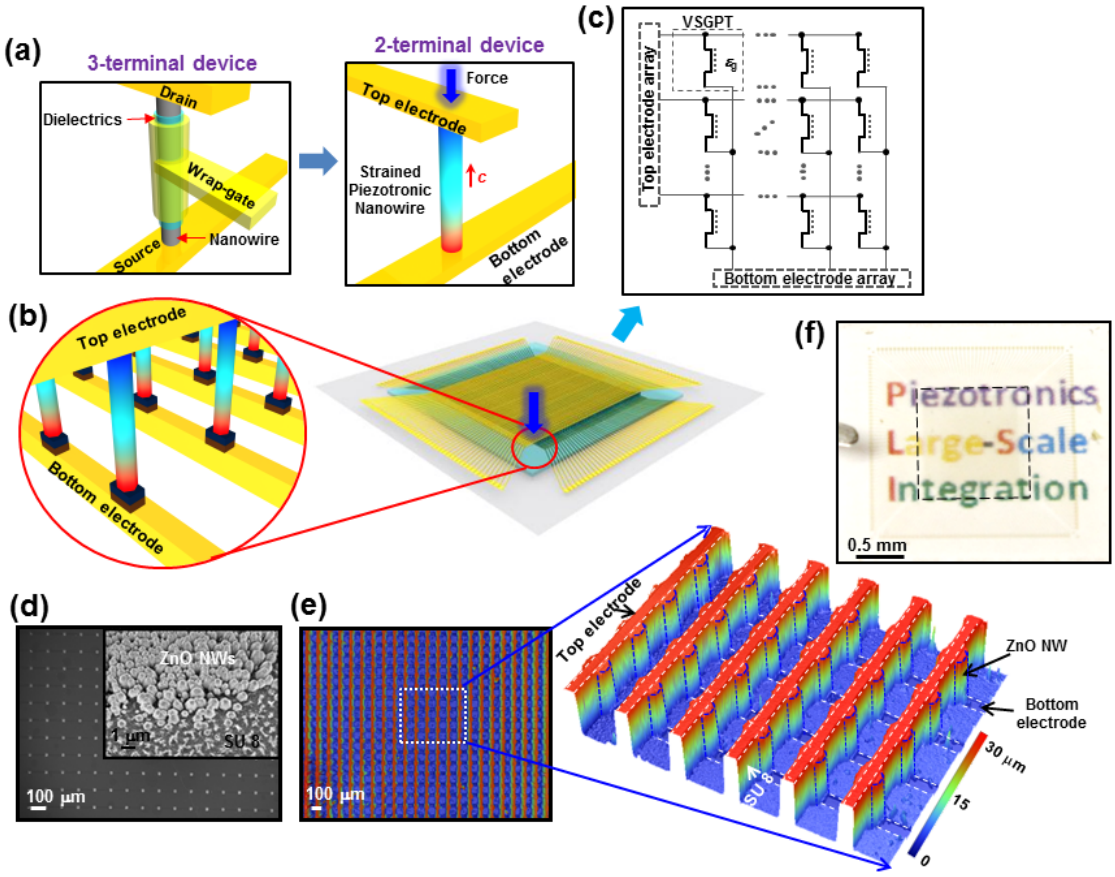


Figure 46. Schematic illustration, optical and SEM images, and topological profile image of 3D SGVPT array assembly. (a) Structural transformation from three-terminal configuration of wrap-gate 3D NW FET (left) into two-terminal configuration of SGVPT (right). (b) Schematic illustration of a 3D SGVPT array with pixel density of 92 x 92 and scheme for spatial profile imaging of local stress. (c) Equivalent circuit diagram of the 3D SGVPT array. (d) SEM image of SGVPT array taken after etching-back the SU 8 layer and exposing top surfaces of the ZnO NWs. Inset, 30^{o}-tilt view of the exposed ZnO NWs for single pixel. (e) Topological profile image of the SGVPT array (Top view). Inset, 3D perspective view of the topological profile image reveals the vertical hierarchy of the SGVPT assembly in which the color gradient represents different heights. (f) Optical image of the transparent 3D SGVPT array on flexible substrate.

6.2.1 Fabrication of SGVPT array

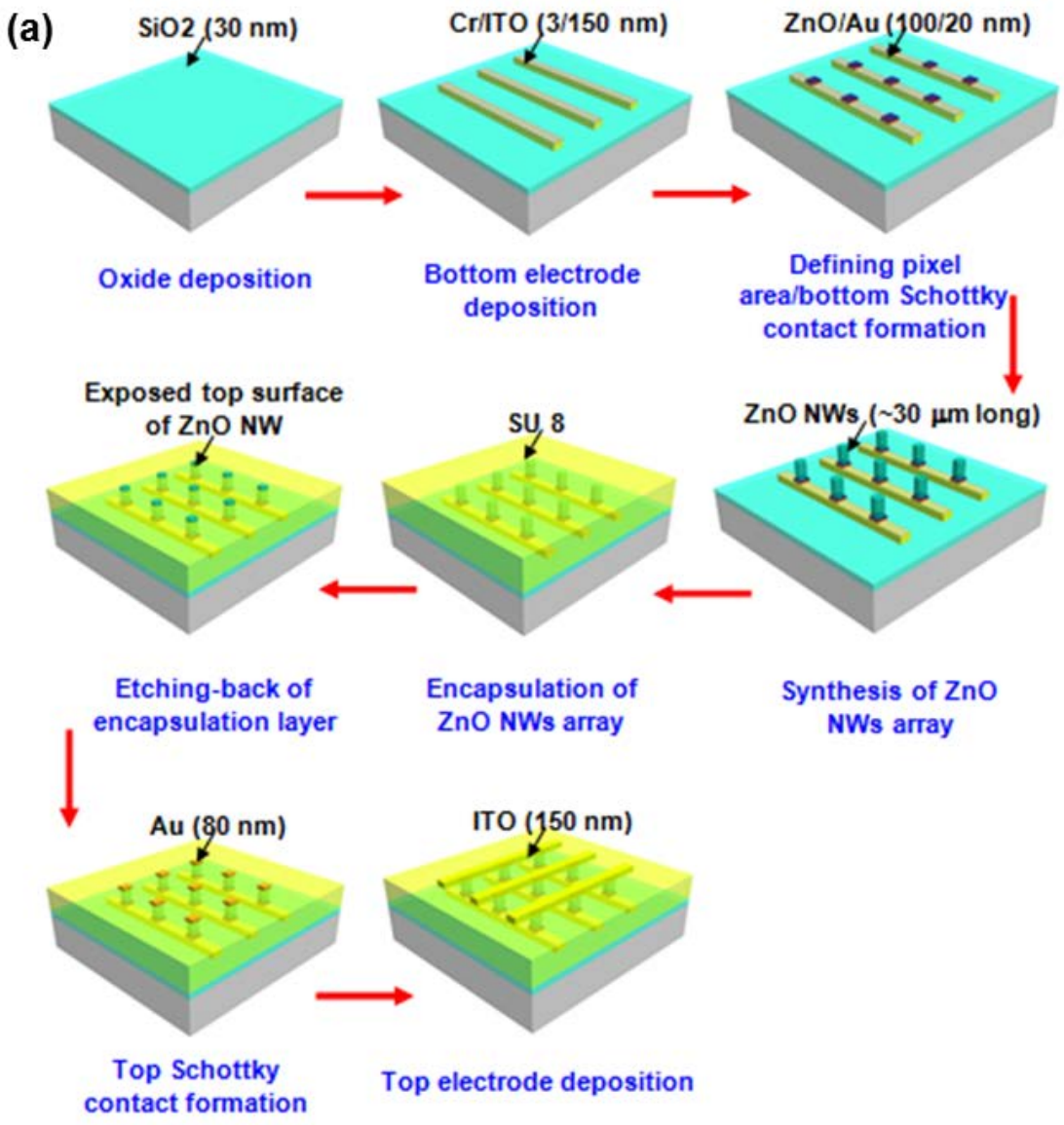
By combining the patterned in-place growth of vertically aligned ZnO NWs with state-of-the-art microfabrication techniques, large-scale integration of SGVPT array can

be obtained. Figure 46b illustrates the schematic of the SGVPT array with pixel density of 92 x 92 in 1 cm^2 (234 pixels per inch (PPI)) and its equivalent circuit diagram is displayed in Figure 46c to demonstrate the operation scheme of the SGVPT devices circuitry, in which ε_g represents the mechanical strain *gate* signal. Detailed device fabrication process is described and shown in Appendix A and Figure 47. Briefly, the active array of SGVPTs is sandwiched between the top and bottom Indium Tin Oxide (ITO) electrodes, which are aligned in orthogonal cross-bar configurations. A thin layer of Au is deposited between the top/bottom surfaces of ZnO NWs and top/bottom ITO electrodes, respectively, forming Schottky contacts with ZnO NWs. Well-aligned ZnO NWs, synthesized by low-temperature hydrothermal method [28] (also see Chapter 3), function as the active channel material of SGVPT and help reduce the stochastic pixel-to-pixel variation to ensure uniform device performance, which is shown in the scanning electron micrographs (Figure 46d and Figure 48) of the SGVPT array taken after etching-back the SU 8 layer and exposing top surfaces of the ZnO NWs (see Appendix A for fabrication details).

6.2.2 Structure characterization of SGVPT array

The three-dimensional nature of the SGVPT assembly is revealed by topological profile imaging (Figure 46e) obtained by optical noncontact profilometer (Wyko Profilometer NT3300), which measures the phase change of light reflected from various heights in the structure by interferometry. The high degree in alignment and uniformity of SGVPT array in three dimensions (~ 30 μm in height and 20 μm × 20 μm in pixel size), enabled by process control in both the bottom-up synthesis of NWs and top-down fabrication of circuitry, ensures the integration of large-scale NW electronics for functional systems with high degree of complexity for potential industrial scale-up and future practical applications. The structural transformation from three-terminal configuration into two-terminal configuration by taking advantage of piezotronic effect

significantly simplifies the layout design and circuitry fabrication while maintains effective control over individual devices. Transparency and flexibility of SGVPT array devices (Figure 46f and Figure 49) are also critical properties for future applications such as artificial skin, personal electronics and potential integration with compliant energy harvesting modules for self-powered flexible functional systems[19,133].



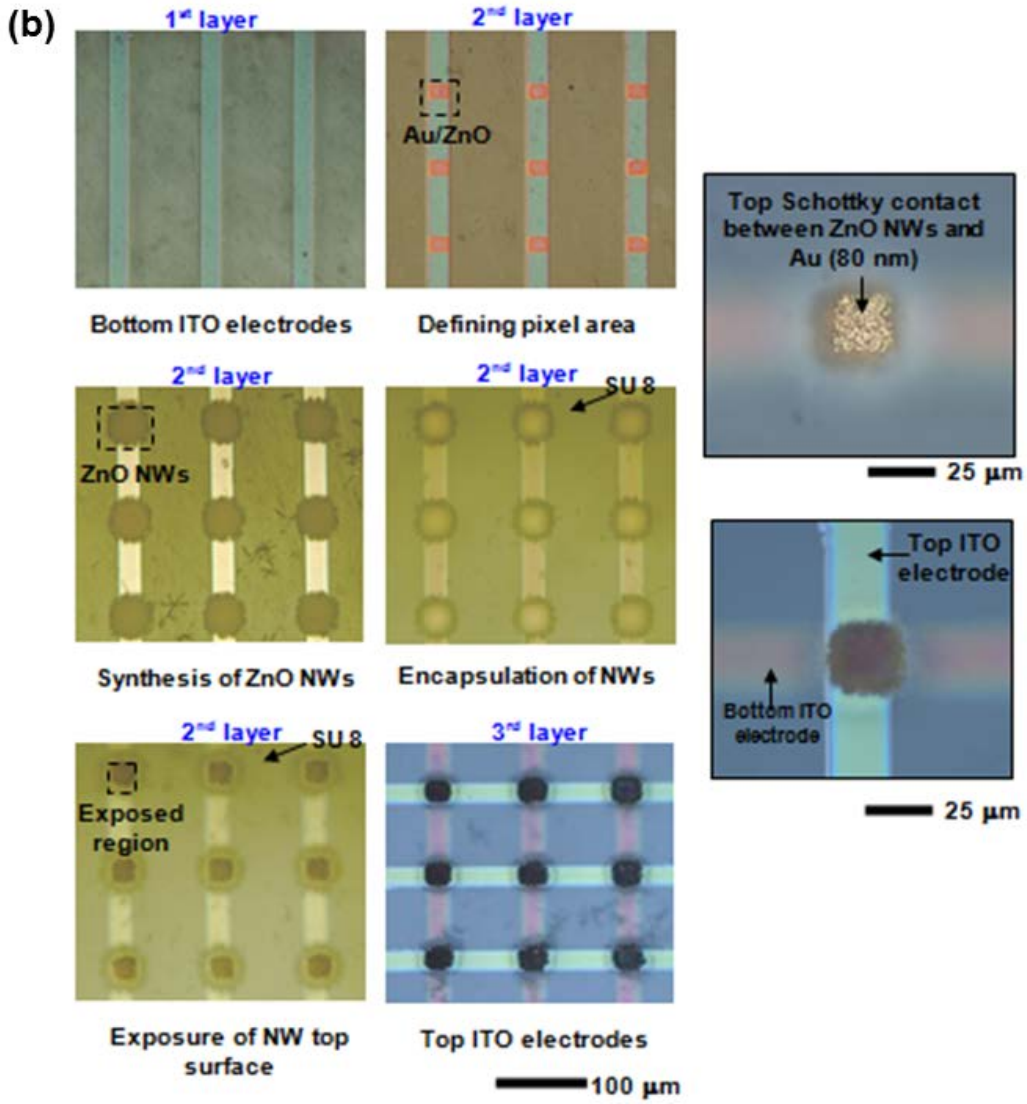


Figure 47. (a) Schematic illustration of processing steps for fabricating 3D vertical piezotronic transistors array on a PET substrate. (b) Optical micrographs of 3D vertical piezotronic transistors array on a PET substrate. Inset (right) shows magnified image of top Schottky contacts and single pixel after 3rd layer processing.

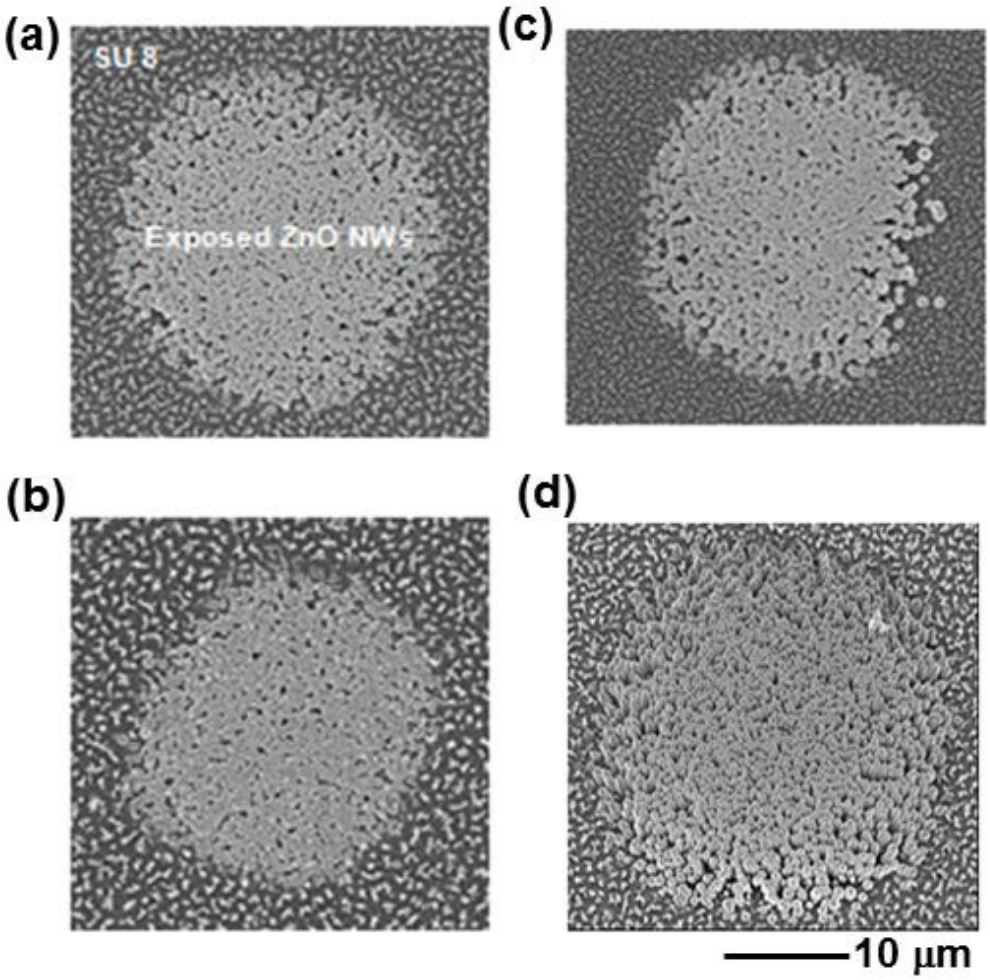


Figure 48. (a-d) Scanning electron micrographs of 3D vertical piezotronic transistors array encapsulated by SU 8, with top surfaces of ZnO NWs exposed. (a-c): Top views of three selected pixels with SU 8 etched back. (d): 30^{o} tilted view of single pixel with top surfaces of ZnO NWs exposed.

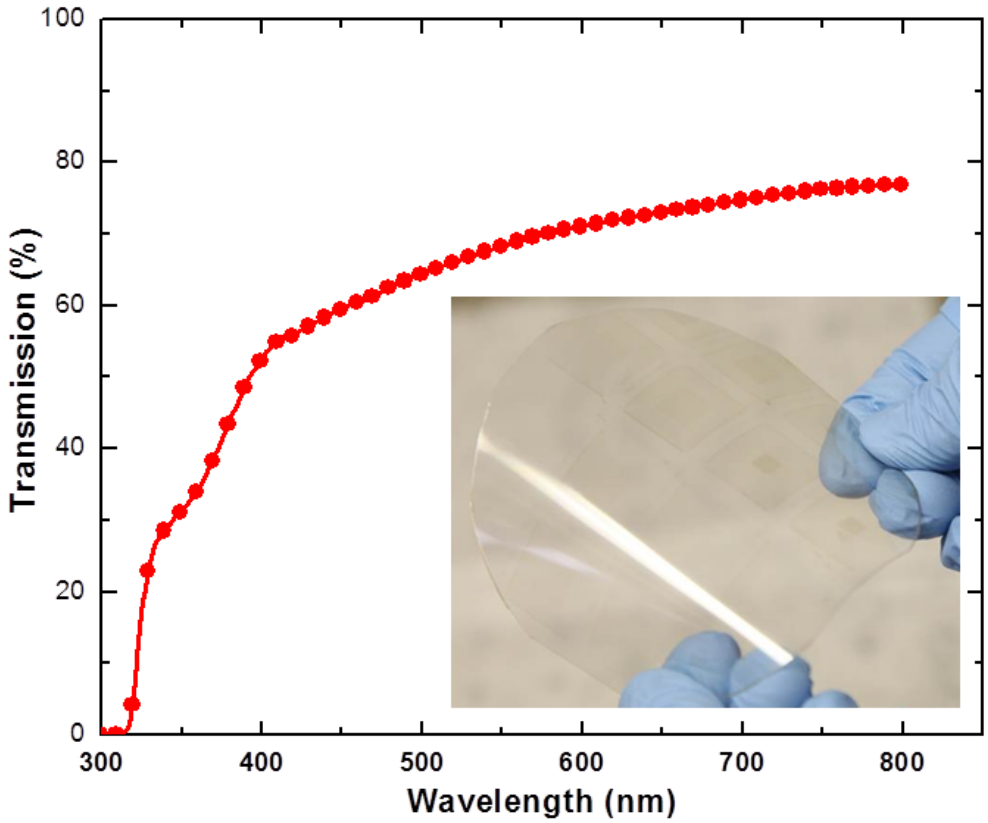


Figure 49. Measured normal incidence transmission (T) spectra of 3D vertical piezotronic transistors array on a PET substrate. Inset: Optical image of 3D vertical piezotronic transistors arrays on a 4-inch PET substrate.

6.3 Single-channel and full array response characterization

6.3.1 Single-channel response characterization

Typical single-channel line-scan (1 x 92) measurement results for SGVPT array device are shown in Figure 50, by locating one top electrode and addressing the 92 bottom electrodes so that all 92 pixels along this top electrode can be characterized individually. The electrical characterization platform interfaced with the 3D VSGPT array through a customized 200-pin probe card (Accuprobe Inc.) installed on the probe station (Cascade Microtech). All of the 8464 pixels were individually-addressable by iteratively switching two multiplexer matrixes (NI PXI-2530) and output current from each SGVPT pixel under bias was measured and averaged within a short duration

window of 10 ms by a 6½-digit digital multimeter (NI PXI-4072). The synchronized operations among the PXI modules as well as the data acquisition were controlled by the customized LabVIEW (National Instruments) code. The electrical characterization platform was connected to a computer for data registration and post-processing of acquired image. The background noise for the measurement system is also characterized and found to be significantly smaller than the measured responses (Figure 52c).

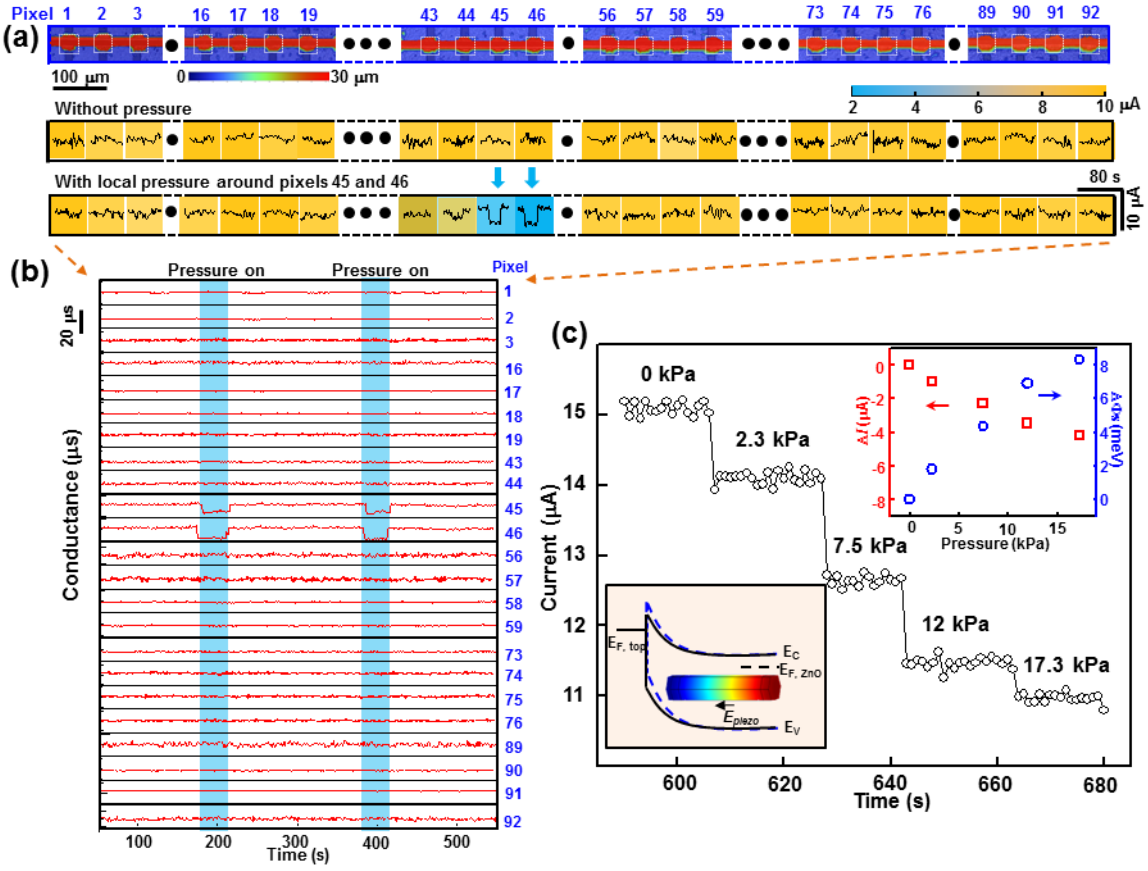


Figure 50. Single-channel line-scan (1 x 92) electrical measurement for SGVPT array device. (a) Topological profile images (top view) and the current response from these 23 pixels under 1 V bias with and without external stress applied to certain localized region. (b) Single-channel conductance measurement in temporal domain with and without pressure applied. (c) Current responses for pixel 46 under different pressures. Top right inset, current variations (red squares) and derived changes in SBHs (blue circles) for the reversed biased top contact, both versus the applied pressures. Bottom left inset, schematic band-diagram illustrating the change in SBH of the reversed biased top contact due to the modulation effect of strain-induced piezopotential.

Representative data from 23 pixels in this channel is listed here. Topological profile images (top view) of the selected pixels are organized at the top of Figure 50a. Current response from each pixel under 1 V bias, with and without external pressure (20 kPa) applied to certain localized region (around pixels 45 and 46), is recorded and plotted with color representing ratio of the response amplitude for each pixel in an 80-sec window. It can be seen clearly that for this single-channel array of SGVPTs, pressure variations can be distinguished with both high sensitivity and spatial resolution (pixel periodicity ~ 100 μm). Data from single-channel conductance measurement in temporal domain are compiled and shown in Figure 50b to further illustrate the dynamic response of SGVPT devices. Distinctive changes in conductance can be observed for pixels 45 and 46 before and after applying the localized pressure. The pressure sensitivity of a single SGVPT is also probed and shown in Figure 50c (for pixel 46). From the measured variations in current responses by consecutively increasing the pressure load applied at fixed location, the SGVPT device demonstrates high sensitivity for detecting pressure change, particularly in low-pressure regions (< 10 kPa).

The modulation effect of applied pressure, which essentially functions as the controlling *gate*, on the electrical characteristics of SGVPT is exhibited by plotting current variations against pressure changes (red squares in top right inset of Figure 50c). The sensitivity for SGVPT, defined as $S = dG_{SGVPT}/dP$, is around 2.1 $\mu s \cdot kPa^{-1}$, which arises from the change in carrier transport of the SGVPT by applied pressure due to corresponding modulation of barrier height at the reversed biased Schottky contact by strain-induced piezopotential[11,29,158]. Specifically, the conductance of SGVPT device is dictated by the reversed biased Schottky contact, which is formed between ZnO NWs and top electrodes in this case. Upon applying the normal stress, accumulations of piezoelectric charges at both Schottky contacts induce the distribution of piezopotential. Due to the orientation of polar *c* axis in the as-synthesized ZnO NWs here (indicated by

the red arrowhead in Figure 46a, right), negative piezopotential is induced at the reversed biased top Schottky contact, which raises the barrier height at that contact and hence decreases the transport conductance of the SGVPT pixel, as depicted by the schematic band diagram in Figure 50c (bottom left inset). The corresponding theoretically derived changes in Schottky barrier height for the reversed biased top contact are also plotted in Figure 50c (blue circles in top right inset)[30].

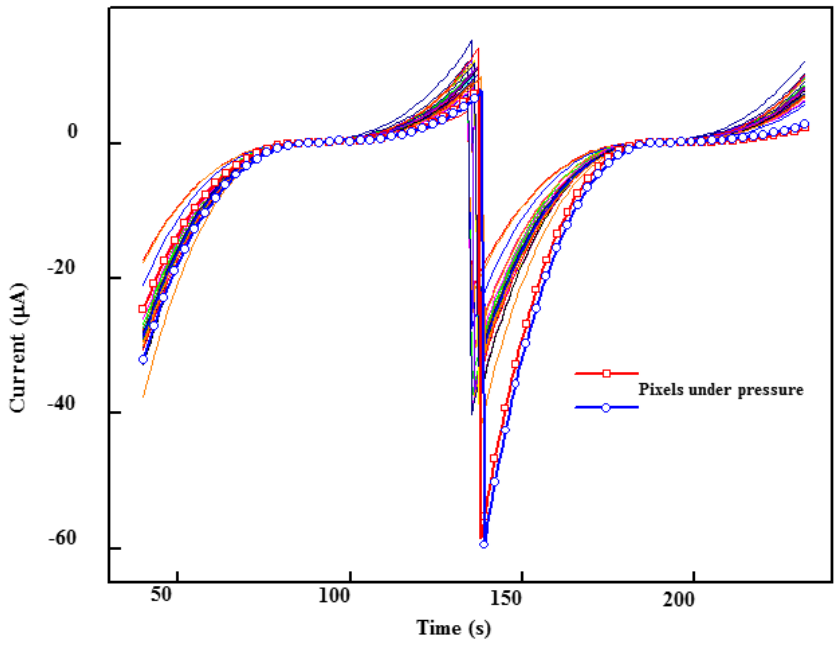


Figure 51. Single-channel measurement confirming the piezotronic rather than piezoresistive characteristics of the conductivity change for SGVPT pixels under strain.

Piezotronic effect differs from the conventionally utilized piezoresistive effect in that the latter results from change in bandgap, charge carrier density or density of states in the conduction band of the strained semiconductor material that functions as a scalar "resistor", while piezotronic effect arises due to the polarization of ions in the crystal and can directly affect the local contacts asymmetrically. This means that piezoresistive effect is a symmetric volume effect without polarity, while piezotronic effect is an interface effect that asymmetrically modulates local contacts at different terminals of the device due to the polarity of the piezopotential[29,158]. The magnitude and polarity of

piezopotential within corresponding SGVPT changes according to the local stress/force, resulting in a direct control over local Schottky barrier heights and hence the corresponding conducting characteristics of the SGVPT by induced strain. The asymmetric change in current response of SGVPT pixels under strain confirm that the underlying mechanism here is piezotronic effect at the contact interface, rather than the conventional piezoresistive effect in the bulk, as shown in Figure 51[31]. The operation of SGVPT device is therefore based on barrier-interface-modulation that enables enhanced sensitivity and efficiency compared to the channel-modulation operation in conventional FETs. By monitoring the output current of each independently-functioning SGVPT in the matrix, spatial profile of applied pressure can be readily imaged by multiplexed-addressing all of the pixels.

6.3.2 Full-array response characterization

The feasibility and scalability of the proposed integration scheme is demonstrated by the successful fabrication of the 92 x 92-pixel SGVPT array, which presents the largest integration of ordered NW devices so far for tactile sensing applications, enabling a 15-to-25-fold increase in pixel density compared to previous results[202-204]. The output current of each individual SGVPT pixel is measured and averaged within a short duration window of 10 ms. Two-dimensional current contour plot is thus obtained by registering the measured current to the corresponding pixel coordinates along *x* (bottom electrode) and *y* (top electrode) axes. Metrology mapping has then been performed on the fully integrated SGVPT array without applying pressure (Figure 52a, inset), demonstrating that all of the 8464 SGVPTs within the array are functional at a yield of 100%! The subsequent statistic investigation reveals the superb uniformity in electrical characteristics among all of the pixels, with 95% of the SGVPTs possessing current values in the narrow range of 13.7±2.73 μA under 1 V bias (Figure 52a). The high yield in device fabrication and uniformity in device performance demonstrated here ensure

later large-scale integration of SGVPTs for practical applications. The uniformity in current distribution of SGVPTs can be further improved by optimizing the fabrication process, such as achieving uniform amount of ZnO NWs within each pixel and obtaining even profiles in the etch-back step of SU 8 layer. To demonstrate the tactile sensing capability of the integrated SGVPT array, a normal stress of ~ 25 kPa is applied to the device by pressing a hexagonal-shape mold onto the device. As depicted in Figure 52b, which presents the difference between current values for each pixel before and after applying the normal stress, the profile of applied stress can be spatially imaged.

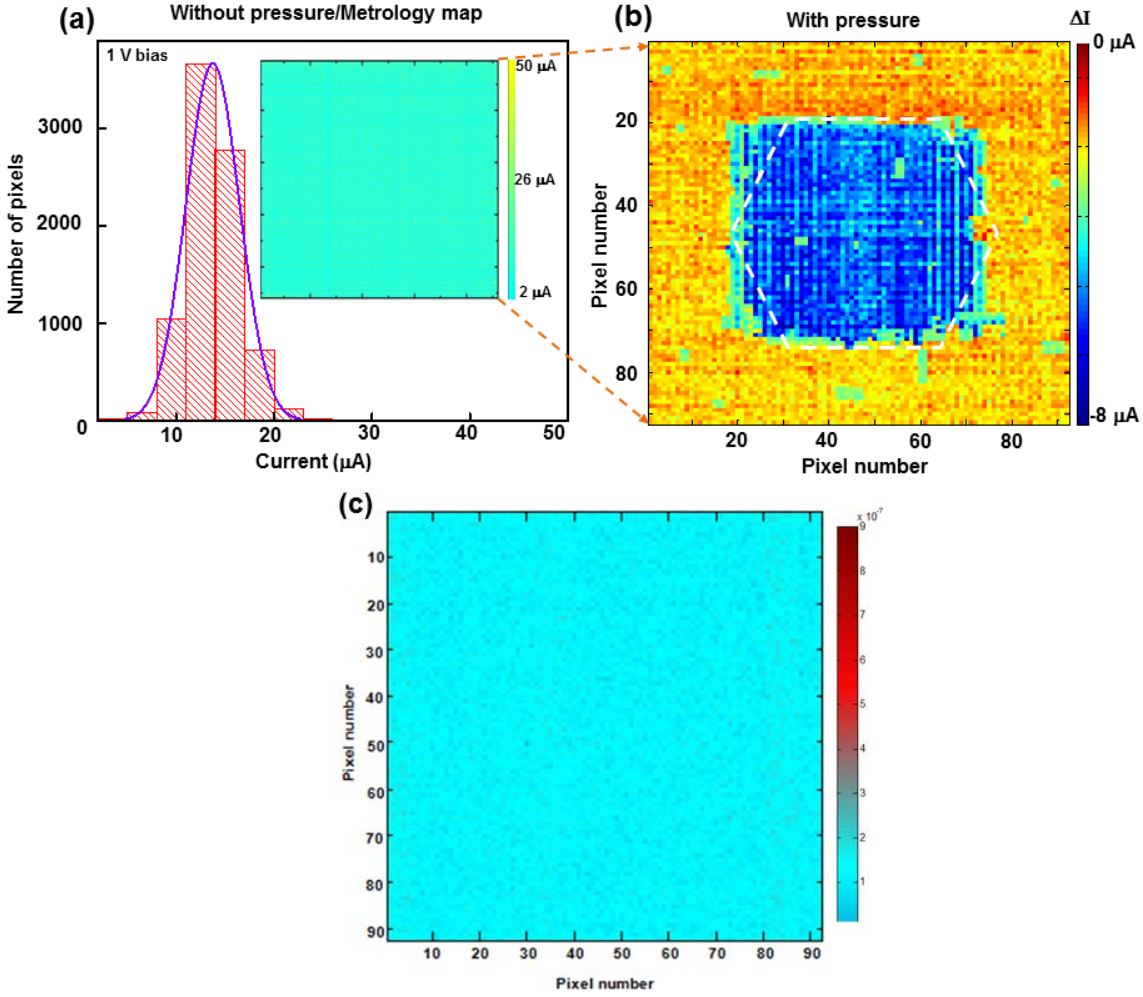


Figure 52. Tactile imaging by fully-integrated 92 x 92 SGVPT array. (a) Metrology mapping (Inset) and statistic investigation of the fully integrated SGVPT array without applying stress. (b) Current responses contour plot illustrating the capability of SGVPT array for imaging the spatial profile of applied stress. (c) Background noise test for the measurement system under 1 V bias.

6.4 Summary

In summary, by introducing the two-terminal piezotronic transistors, we achieved the first large-scale array of strain-gated vertical piezotronic transistors using patterned and vertically-aligned NWs, which are advantageous over the traditional FETs in two folds. By replacing the externally applied voltage with the inner-crystal piezopotential and eliminating the gate electrode, it is possible to fabricate arrays of SGVPT at very high density. The SGVPT devices can also function as active tactile sensors by directly converting mechanical stimulations into electrical signals utilizing the piezopotential without applied bias , which emulates the physiological operations of mechanoreceptors in biological entities, such as human hair follicles and hair cells in the cochlea[217]. The measurement system is shown in Figure 53.

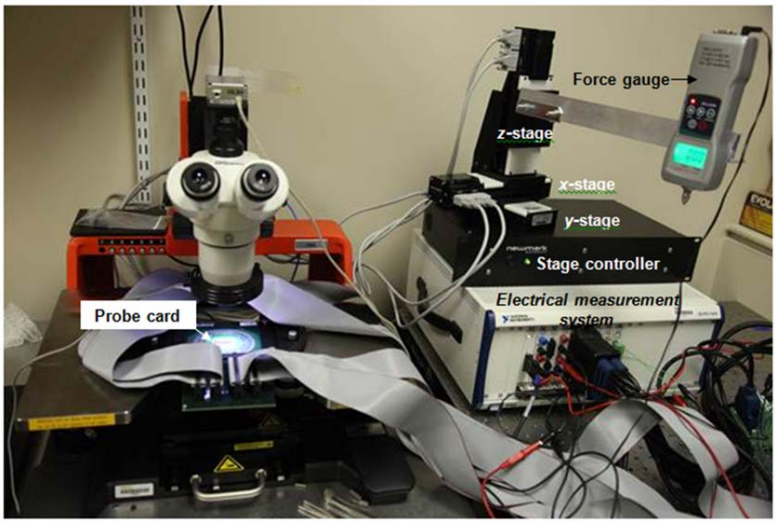


Figure 53. Experimental setup for multichannel multiplexed measurement and programmed mechanical inputs.

The SGVPT array demonstrated here presents the largest integration of ordered 3D vertical NW transistors array as active components with the highest array density and spatial resolution for functional applications in transparent flexible electronics and active sensor arrays. The pixel size can be readily pushed down to the lithographic limits for realizing functional applications with even higher spatial resolution and precisely-

controlled number of NWs within each pixel. It is prospected that SGVPT devices can be further integrated with silicon-based CMOS technology for achieving augmented functionalities in smart systems in the era of "More Than Moore"[208]. The scalability of this platform in integrating in-place synthesized single-crystalline NWs in controllable manners together with its demonstrated compatibility with state-of-the-art microfabrication techniques enables future implementation of Wurtzite NWs for practical applications in micro/nano-systems capable of self-sufficient intelligent multi-dimensional operations[19].

CHAPTER 7

CONCLUSION

The rapid advancement in micro/nanotechnology nowadays will gradually shift its focus from demonstrating discrete devices to developing integrated system of certain complexity, which is capable of performing multi-functions such as sensing, actuating/responding, communicating and controlling by integrating individual devices via state-of-art microfabrication technologies.

Throughout the past four years, as a research assistant in Prof. Wang's group, I have been working towards developing technology that will provide new solutions and enable augmented capabilities to MEMS/NEMS by exploring piezotronic nanodevices and integrated systems. My research endeavors, as discussed in this thesis, encompass the following topics:

1. Nanowire growth

To move forward toward the goals, the first task we have taken is to synthesize high quality ZnO NW samples, either for discrete devices or array-based integrated systems. We have developed an effective approach for patterning growth of vertically aligned ZnO NWs array with high-throughput and low-cost at wafer-scale. Different substrates are patterned using either laser interference lithography of the photoresist or direct laser interference ablation of the substrate, on which ZnO NWs are grown via a low temperature hydrothermal method without using catalyst and with a superior control over orientation, location/density and morphology of as-synthesized ZnO NWs. This approach demonstrates a novel method of manufacturing large-scale patterned one-dimensional nanostructures for applications in energy harvesting, sensing, optoelectronics and electronic devices. Other synthesis processes for growing one-dimensional ZnO nanostructures for piezotronic applications have also been investigated. ZnO NWs

obtained from VS process constitute the majority materials for fabricating single-NW based piezotronic applications. Synthesis methods such as vapor-solid-solid (VSS) and pulsed laser deposition (PLD) processes are also discussed and their potential in realizing ZnO NWs array with high crystallinity, adjustable dopant type, doping levels and controllable bandgap engineering is also investigated.

2. Strain-gated piezotronic logic nanodevices

We have also developed a brand new approach toward logic operation that performs mechanic-electrical coupled and controlled actions in one structure unit using a single material, which is ZnO. ZnO is unique because of its coupled piezoelectric and semiconductor properties, which is the piezotronic effect dealing with the piezopotential tuned/gated charge carrier transport process in a semiconductor material. The piezopotential created inside a ZnO NW under strain can be effectively used as a gate voltage. By utilizing the gating effect produced by the piezopotential in a ZnO NW under externally applied deformation, strain-gated transistors (SGTs) have been fabricated, using which the universal logic operations such as NAND, NOR, XOR gates and MUX/DEMUX have been demonstrated for the first time for performing piezotronic logic operations. This is the very first demonstration of mechanical action induced electronic logic operation with the introduction of a new driving mechanism in comparison to the existing silicon based logic operations. This is also the first demonstration of its kind using nanowires. In contrast to the conventional CMOS logic units, the SGT based logic units are driven by mechanical agitation and rely only on *n*-type ZnO NWs without the presence of *p*-type semiconductor components. The mechanical-electronic logic units can be integrated with NEMS technology to achieve advanced and complex functionalities in nanorobotics for sensing and actuating, and in microfluidics for controlling the circuitry of the flowing fluid. Furthermore, ZnO piezotronic logic devices can be further integrated with the ultrasensitive ZnO NW sensors and ZnO NW based nanogenerators to achieve self-sustainable, all nanowire

based, multifunctional self-powered autonomous intelligent nanoscale system (SPAINS). This has vitally important applications in portable electronics, medical sciences and defense technology.

3. Piezotronic strain memory device

We have presented the first piezoelectrically-modulated resistive switching device based on piezotronic ZnO NWs, through which the write/read access of the memory cell is programmed via electromechanical modulation. By utilizing the strain-induced polarization charges created at the semiconductor/metal interface under externally applied deformation as a result of piezotronic effect, the switching characteristics of the ZnO NW resistive switching devices can be modulated and controlled. We further demonstrated that the logic levels of the strain applied on the memory cell can be recorded and read out for the first time, which has the potential for implementing novel nanoelectromechanical memories and integrating with NEMS technology to achieve micro/nano-systems capable of intelligent and self-sufficient multi-dimensional operations. To a broad impact, taking advantage of the recently developed large-scale fabrication technique of ZnO NW arrays, nonvolatile resistive switching memories using ZnO NW array as the storage medium may be readily implemented for applications such in flexible electronics and force/pressure imaging. Non-Boolean neuromorphic computing might also be realized by integrating arrays of high-density resistive memory cells on flexible substrates.

4. Large-scale 3D array integration of vertical piezotronic NW transistors

We have presented an important breakthrough on the first and by far the largest 3D array integration of vertical NW piezotronic transistors circuitry (92 x 92 pixels with 234 pixels per inch) as active/adaptive pixel-addressable pressure-sensor matrix for tactile imaging, enabling a 15-to-25-fold increase in pixel density and spatial resolution compared to previous reports. This landmark breakthrough in implementing 3D piezotronic transistor arrays paves innovative routes towards industrial-scale integration

of NW piezotronic devices for sensing, micro/nano-systems and human-electronics interfacing.

In summary, this dissertation presents systematical research on piezotronic devices and integrated systems. As the core of this dissertation, piezotronic effect induced by the piezopotential-modulated charge transport across contact/junction upon externally applied mechanical strain has been investigated and utilized. From the synthesis of aligned ZnO NWs array at large scale to characterize the electromechanical property of as-fabricated devices for novel piezotronic applications, the work in this dissertation not only help strengthen the understanding of piezotronics, but also pave routes towards further implementation of piezotronic transistor arrays for sensing, micro/nano-systems and human-electronics interfacing[207] as well as large-scale integration of piezotronics with silicon-based CMOS technology for achieving augmented functionalities in smart systems in the era of “More Than Moore”.

APPENDIX A

PROCESSING SCHEME FOR FABRICATING 3d VERTICAL PIEZOTRONIC TRANSISTORS ARRAY

Substrate preparation

1. Clean the Polyethylene terephthalate (PET) substrate or silicon wafer (acetone, isopropyl alcohol (IPA), deionized (DI) water).

2. Deposit a thin layer of SiO_2 (30 nm) to the substrate via electron-beam evaporation.

Bottom electrode formation

3. Spin-coat negative-tone photoresist (Futurrex NR9-1500PY) onto the substrates and soft-bake at 150 ^{o}C for 60 s.

4. Expose the samples with 365 nm UV lithography using first layer pattern.

5. Post-bake the samples at 100 ^{o}C for 60 s.

6. Develop the exposed samples in aqueous base developer (Futurrex Resist Developer RD6).

7. Rinse and blow-dry the samples.

8. Deposit 150 nm ITO as the bottom electrodes through RF magnetron sputtering.

9. Immediately deposit 3 nm Cr onto the ITO electrodes through electron beam evaporation.

10. Lift-off ITO/Cr in acetone.

Bottom Schottky contact formation and active area defining

11. Clean the processed samples in step 10 (acetone, IPA, DI water).

12. Pattern photoresist using second layer mask (steps 3-7).

13. Deposit 20 nm Au through electron beam evaporation.

14. Deposit 100 nm ZnO through RF magnetron sputtering.

15. Lift-off Au/ZnO in acetone.

Synthesis of vertical ZnO NWs array

16. Clean the processed samples in step 15 (acetone, IPA, DI water).

17. Immerse the samples into the growth solution (25 mM $ZnCl_2$ and 25 mM Hexamethylenetetramine (HMTA, $(CH_2)_6N_4$)) at 85 ^oC for 6 hrs.

Encapsulation of vertical ZnO NWs array

18. Clean the processed samples in step 17 (acetone, IPA, DI water).

19. Spin-coat encapsulation polymer (Microchem SU 8 2025) onto the samples.

20. Expose the samples with 365 nm UV lithography.

21. Cure the samples at 150 ^oC for 1 hr.

Exposure of top surfaces of ZnO NWs

22. Clean the processed samples in step 21 (acetone, IPA, DI water).

23. Dry etch the SU 8 layer in a reactive ion etcher.

Top Schottky contact formation

24. Clean the processed samples in step 23 (acetone, IPA, DI water).

25. Pattern photoresist using second layer mask (steps 3-7).

26. Deposit 80 nm Au through electron beam evaporation.

27. Lift-off Au in acetone.

Top electrode formation

28. Clean the processed samples in step 27 (acetone, IPA, DI water).

29. Pattern photoresist using third layer mask (steps 3-7).

30. Deposit 150 nm ITO through RF magnetron sputtering.

31. Lift-off ITO in acetone.

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VITA

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