Analysis of non-uniform polar quantisers in a Sigma Delta transmitter architecture

Vandana Bassoo[1], Lance Linton[2] and Mike Faulkner[2]
[1] School of Innovative Technologies and Engineering, University of Technology-Mauritius, La Tour Koenig, Pointe-aux-Sables, Mauritius
[2] School of Engineering and Science, Victoria University, Australia
E-mail: vbassoo@umail.utm.ac.mu and mike.faulkner@vu.edu.au

***Abstract*—The drive signals for radio frequency switch mode amplifiers can be directly generated by digital circuits using pulsewidth modulation and pulse position modulation. The quantisation noise that occurs when the pulsewidths are quantised to the timing grid can be shaped using sigma delta ($\Sigma\Delta$) modulation combined with polar quantisation. This paper analyses the behaviour of the resulting non-uniform polar quantisation and predicts the signal to noise ratio (SNR) performance of both Cartesian and polar filtered $\Sigma\Delta$ architectures. Practical measurements and simulations support the analysis. Orthogonal frequency division multiplexing and wideband code division multiple access signals are shown to have an increasing SNR with signal strength of 0.5 dB/dB at low signal levels, and 1 dB/dB at medium signal levels prior to entering the overload region. The schemes trade-off improved quantiser fidelity for higher oversampling requirements. They have reduced transitions, better coding efficiency and generally outperform the traditional bandpass $\Sigma\Delta$ scheme. Their complexity grows linearly with the number of quantisation points.**

I. Introduction

The need for power reduction in radio frequency (RF) power amplifiers (PAs) has led researchers to consider switching architectures as a replacement to traditional amplifier structures based on class A and class B designs. Improvements in device technology in the form of reduced parasitic capacitance make switch-mode techniques such as class S and D (and also class E and F) more competitive at higher carrier frequencies, because of the reduction in switching losses [1]. Switch mode PAs require on an 'on' and 'off' drive signal and this gives the opportunity of digital control. Since process technology has improved, it is therefore now possible to directly generate a modulated IF or RF signal from a digital source with frequencies ranging from tens MHz up to the low GHz [2]- [3]. This paper considers the replacement of the traditional direct up-conversion architecture by a digital architecture. The proposed new architecture (Fig 1(bottom)) eliminates many analog components in the transmitter chain and replaces them with a single predominantly digital sigma delta ($\Sigma\Delta$) up-conversion circuit [4]- [6]. The output of which is a discrete representation (-1,1) or as in this paper (-1,0,1) of the modulated carrier signal. The new circuit exploits the high speed capabilities of modern digital circuits to eliminate many analog difficulties of the traditional analog architecture. Such problems include gain-phase imbalance of the IQ modulator, carrier leak, the need for an analog RF synthesiser and the need for frequency dependant gain and phase matching of the two lowpass filters [7]. These problems are all eliminated by the all-digital $\Sigma\Delta$ digital drive upconversion architecture.

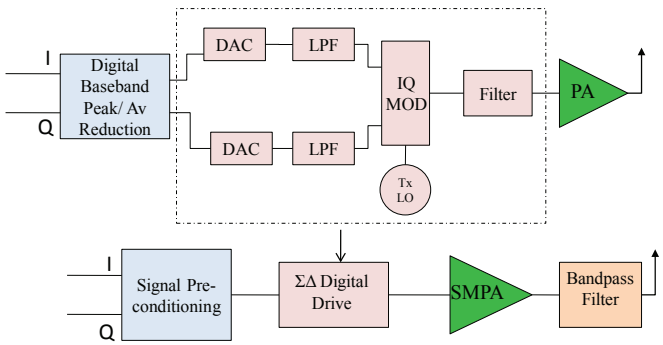

Fig. 1. Traditional and potential $\Sigma\Delta$ up-conversion architecture.

The drive signal to an RF switch mode PA consists of a train of discrete pulses whose pulse widths determine the amplitude (pulse width modulation (PWM)) of the RF carrier and whose pulse positions (pulse position modulation (PPM)) determines the phase of the RF signal (Fig. 2). If these signals are to be generated from a synchronous digital circuit, then the pulse edges must be quantised to the internal timing grid of the digital circuit. This leads to quantisation noise. $\Sigma\Delta$ techniques can be used to shape this noise out of band, hence it can be filtered away by a bandpass filter. The $\Sigma\Delta$ processs can be applied in polar form [4], or in Cartesian [6]- [8]. The latter usually gives superior results as the $\Sigma\Delta$ filtering is performed on non-bandwidth expanded signals. Wang [9], Jeong and Wang [10] avoided phase quantisation effects altogether by only quantising the signal amplitude, but this re-introduced analog componentry such as the quadrature modulator; hence the all-digital architecture was no longer possible.

This paper analyses the quantisation noise generated by the all-digital structures of [4] and [6] and then predicts their performance when embedded in a $\Sigma\Delta$ loop. There have been many papers describing the quantisation noise associated with one dimensional $\Sigma\Delta$ ADCs and DACs [11]. The traditional analysis models the quantisation noise as a white error process which is fed into the $\Sigma\Delta$ loop. The quantisers are generally linear and the noise power is given by $\frac{\Delta^2}{12}$ where Δ represents the quantisation step-size. Improvements can be made by using semi-uniform quantisers with smaller steps at the

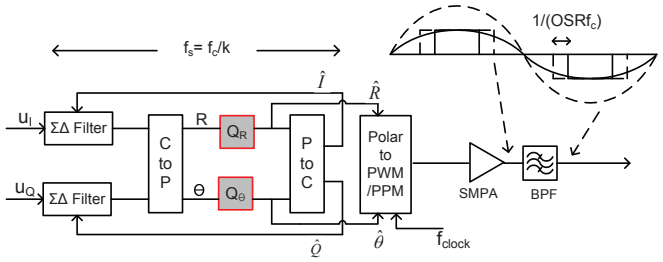

Fig. 2. Cartesian ΣΔ modulator (polar quantiser blocks are highlighted). The switched mode PA boosts output power. It is not necessary for low level up-converters.

lower signal levels [12]. However, there has been no analysis of a non-uniform polar quantiser with a two-dimensional circular symmetric Gaussian input signal having a Rayleigh envelope. The latter is a good approximation for signals such as orthogonal frequency division multiplexing (OFDM) and wideband code division multiple access (WCDMA) which are common modulation schemes for today's wireless systems. In this paper, the architecture of the Cartesian ΣΔ is briefly explained in Section II. The non-uniform polar quantisation process is explained in Section III. The mean square error (MSE) of the non-uniform polar quantiser with a circular symmetric Gaussian signal having Rayleigh envelope is derived in Section IV. Section V compares the theoretical and simulated MSE results for a stand-alone quantiser. Section VI gives an analysis of a polar quantiser with and without ΣΔ modulator. The noise associated with the ΣΔ modulator is derived and superimposed on a measured spectrum plot. In Section VII, the low signal level behaviour of the ΣΔ modulator is discussed. Section VIII discusses implementation issues and gives some performance comparisons.

II. The Architecture

The Cartesian ΣΔ architecture shown by Fig. 2 proposed by the authors in [6] is an improvement over the polar ΣΔ modulator of [4]. The main objective of the new architecture is to eliminate the bandwidth expanded signals from the ΣΔ process. This is achieved by moving the non-linear Cartesian to polar conversion of [4] to the output of the ΣΔ filters. This Cartesian structure performs ΣΔ filtering on individual u_I and u_Q Cartesian signals. After ΣΔ filtering, the u_I and u_Q signals are then converted to polar coordinates $[R, \theta]$ and separately quantised in blocks Q_R and Q_θ. The output of the quantisers $[\hat{R}, \hat{\theta}]$ are converted to pulse widths and pulse positions in the 'polar to PWM/PPM' block. Moreover, the output of the quantisers $[\hat{R}, \hat{\theta}]$ is converted back to Cartesian coordinates $[\hat{I}, \hat{Q}]$ (removing bandwidth expansion) and fed back to ΣΔ filters. The output of the 'polar to PWM/PPM' block is a pulse train to be fed directly to the SMPA and band-pass filtered to remove the quantisation and out-of-band distortion products [5]. Some of the harmonic distortions can be cancelled by using a bridge amplifier structure in push-pull. The on-off two-level waveform driving the "push" arm can be delayed by π and sent to the "pull" arm to give an effective 3-level signal (+1,0,-1) as shown in (Fig. 2) and (Fig. 4) [13]. The waveforms are repeated k times before being updated by the next quantised amplitude and phase output $[\hat{R}, \hat{\theta}]$ from the Cartesian ΣΔ system. Therefore the ΣΔ sample rate is $f_s = f_c/k$, where f_c is the nominal carrier frequency.

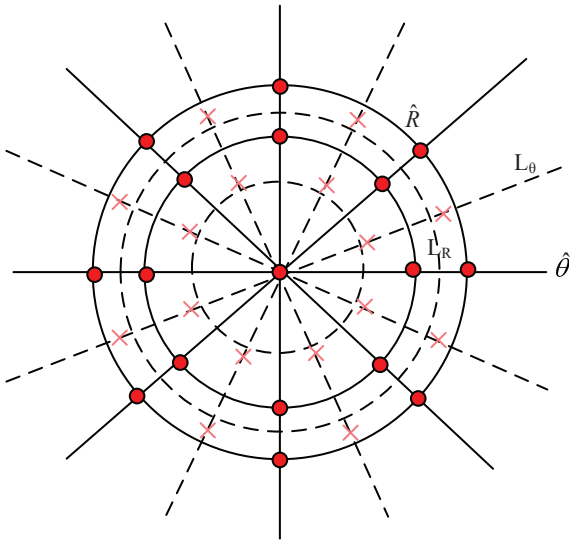

Fig. 3. An example of the polar quantisation plane with N_A=3, N_P=8 and N_q=17 for even pulse widths. Additional quantisation points are added if odd pulse widths are included (marked X).

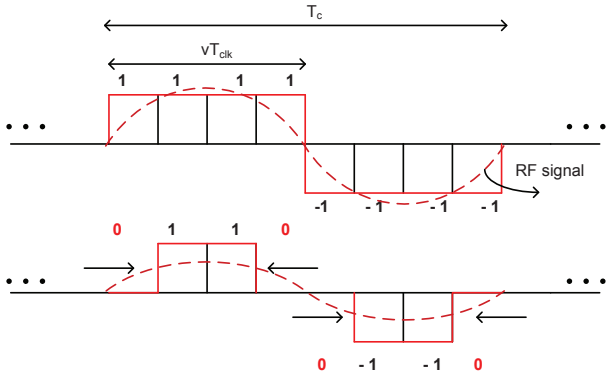

Fig. 4. Quantisation amplitude level calculation. T_{clk} corresponds to the time period of system digital clock. The signal $y(v, n_p)$ covers one carrier period, $T_c = (OSR)T_{clk}$.

III. Non-uniform Polar Quantisers and the Polar Quantisation Plane

The quantisation phase plane of Fig. 3 illustrates the functions carried out by blocks Q_R and Q_θ. It shows a series of concentric circles sliced at equal angles. The circles represent the quantised amplitude and the slices represent the quantised phases. The dots at the intersection of the circles and the slices represent the quantisation points. The dotted circles and dotted lines represent the threshold levels used in the quantiser. The number of quantised steps (N_A, N_P) can be increased or decreased depending on the accuracy requirement.

The phase is uniformly quantised into N_P phase increments from zero to 2π. The quantised phase,

$$\hat{\theta} = n_p \frac{2\pi}{N_p} \quad \text{(rad)} \tag{1}$$

where $n_p = 0 \ldots N_p - 1$ and represents the PPM delay in clock periods.

However, it must also be noted that increasing the number of levels implies a higher oversampling rate (OSR). There are OSR clock periods in one cycle of f_c and OSR is equal to N_p. This eventually constrains the maximum f_c, because of technology limitation on the maximum f_{clock} (2).

$$f_{clock} = OSR \times f_c. \tag{2}$$

$$OSR = N_P. \tag{3}$$

The amplitude, R, is quantised into N_A levels,

$$N_A = \left(\frac{OSR}{4} + 1\right), \tag{4}$$

corresponding to pulsewidths having an even number of clock periods, $\left(0, \frac{2}{OSR}, \frac{4}{OSR}, \frac{6}{OSR} \cdots \frac{OSR/2}{OSR}\right)\frac{1}{f_c}$. The pulsewidths have two sample increments in order to decouple the amplitude response from the phase response, avoiding an amplitude modulation (AM) to phase modulation (PM) conversion, and so simplifying the quantising process into two independent one-dimensional selections (amplitude and phase). On the other hand, including both the odd and even pulse widths will require a more difficult two-dimensional selection process to identify the closest quantisation point, but will lead to an almost doubling of the number of quantisation points, N_q. The value of N_q is given by $N_q = OSR^2/4+1$ for the even pulse widths and $N_q = OSR^2/2 + 1$ for the combined even and odd pulse widths. The +1 is the (0,0) quantisation point and crosses mark the odd quantisation points in Fig. 3. This paper will assume even pulse widths, unless specifically mentioned.

A. Calculation of the Amplitude Quantisation Levels

The quantised amplitude levels, $\hat{R}$, are calculated by evaluating the fundamental spectral component of the repeating three-level waveform, $y(v, n_p)$ as shown in Fig 4. The waveform has OSR clock cycles and covers exactly one period, $T_c = (OSR)T_{clk}(= 1/f_c)$, of the RF carrier. v is the pulsewidth in number of clock cycles and n_p is the pulse position. The pulse width is varied in increments of two clock periods, to calculate the different RF envelope values, $\hat{R}$. The three-level pulse wave can be mathematically represented by

$$y(v, n_p) = \sum_{\alpha=-\infty}^{\infty} \text{rect}\left(\frac{n_p T_{clk} + \alpha T_c}{vT_{clk}}\right) - \text{rect}\left(\frac{n_p T_{clk} + \alpha T_c - \frac{T_c}{2}}{vT_{clk}}\right) \tag{5}$$

where

$$\text{rect}\left(\frac{t_r}{\tau}\right) = u\left(t_r + \frac{\tau}{2}\right) - u\left(t_r - \frac{\tau}{2}\right). \tag{6}$$

Since $y(v, n_p)$ is a repeating waveform, the amplitude of the fundamental can be calculated from one period only ($\alpha = 0$) using Fourier series, (or the FFT of an appropriately sampled version of the signal).

$$Y(v, n_p) = \frac{1}{T_c}\text{FFT}(y_{\alpha=0}(v, n_p)). \tag{7}$$

The amplitude of the fundamental of the pulse wave is given by

$$\hat{R}\left(\frac{v}{2}\right) = 2[|Y(v, n_p)|], \tag{8}$$

where $(\frac{v}{2})$ is the index for the different pulse widths. The decision threshold levels for the quantiser are given by the midpoint of two quantised levels,

$$L_R\left(\frac{v}{2}, \frac{v}{2} + 1\right) = \frac{R(\frac{v}{2}) + R(\frac{v}{2} + 1)}{2}. \tag{9}$$

Similarly, the threshold for the quantised phase is given by

$$L_\theta(n_p, n_p + 1) = (n_p + 0.5)\frac{2\pi}{OSR}. \tag{10}$$

TABLE I
$\hat{R}$ VALUES FOR OSR = 4, 8, 16 AND 32.

OSR	4	8	16	32
$\hat{R}_0$	0	0	0	0
$\hat{R}_1$	1.2752	0.9018	0.4880	0.2488
$\hat{R}_2$	-	1.2752	0.9018	0.4880
$\hat{R}_3$	-	-	1.1782	0.7086
$\hat{R}_4$	-	-	1.2752	0.9018
$\hat{R}_5$	-	-	-	1.0604
$\hat{R}_6$	-	-	-	1.1782
$\hat{R}_7$	-	-	-	1.2508
$\hat{R}_8$	-	-	-	1.2752

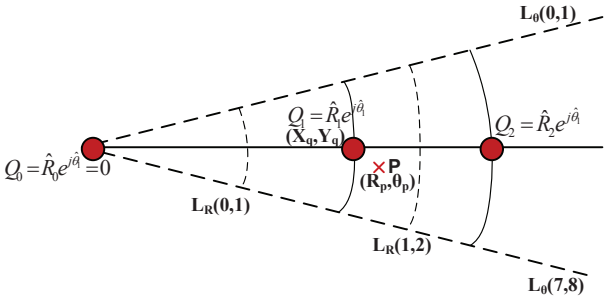

Fig. 5. An expanded view of a slice of the polar quantisation plane, OSR=8.

B. Non-Linear Amplitude Quantisation Levels

Table I lists the amplitude quantisation levels, $\hat{R}$, for a quantiser with OSR of 8 (Fig. 3),16 and a quantiser with OSR of 32. The uneven separation between the quantised levels indicates that increasing the pulsewidth has less effect on the RF carrier magnitude when the pulsewidths are already large. The pulse extremities contribute less to the signal amplitude compared to the central sections of the pulse.

Rayleigh distributed signals have amplitude probability density functions (PDFs) that are concentrated around the lower signal levels. It can be noted from Table I that the low amplitude levels are coarsely quantised and higher amplitudes

are more finely quantised. Therefore, the quantisation noise is larger for such signals than would be normally expected using a linear quantiser. Signals whose PDFs are concentrated at medium to high amplitude levels (such as $\frac{\pi}{4}$ quadrature phase shift keying (QPSK) and enhanced data rates for GSM evolution (EDGE) modulation) are more suited to this type of non-linear quantiser.

However the phase error behaves in an opposite way; increasing the amplitude produces a bigger MSE for the same phase error. To some extent, this neutralises the non-linear quantisation of the magnitude error. These effects will now be quantified in the next sections.

IV. Derivation of Polar Quantiser MSE

In this section, an expression is derived for the MSE for the non-linear polar quantiser with a circular symmetric Gaussian input signal of arbitrary power. The MSE for each of the amplitude quantisation levels has to be calculated separately as the area associated with each quantisation level is not uniform. However, the MSE of only one slice (one phase quantisation level) needs to be calculated due to the phase symmetry. This procedure helps to minimise mathematical complexity. The MSEs obtained for each of the amplitude quantisation levels are summed. The resulting MSE is multiplied by the number of slices, N_p, to obtain the final MSE.

Point P in Fig. 5 is used to further illustrate the quantisation and MSE derivation procedure. As shown in Fig. 5, three MSEs corresponding to $Q_0 = \hat{R}_0 e^{j\theta_1}$, $Q_1 = \hat{R}_1 e^{j\theta_1}$ and $Q_2 = \hat{R}_2 e^{j\theta_1}$ are calculated. Q_0 is selected when P lies between the amplitude limits 0 and $L_R(0,1)$ and phase limits $L_\theta(-1,1)$ and $L_\theta(1,2)$. Q_1 is selected when P lies between the amplitude limits of $L_R(0,1)$ and $L_R(1,2)$ and the phase limits of $L_\theta(-1,1)$ and $L_\theta(1,2)$. Q_2 is selected when P lies between the amplitude limits of $L_R(1,2)$ and infinity and the phase limits of $L_\theta(-1,1)$ and $L_\theta(1,2)$. The MSEs are summed and multiplied by N_p which corresponds to eight in the example of Fig. 3.

Assuming the input signal has a Rayleigh envelope, the MSE of the non-uniform polar quantiser is derived. The derivation process starts by finding the probability of the occurrence of a point, P. The probability of the occurrence of a point, P, is given by the probability of occurrence of amplitude, R_p, and the probability of occurrence of angle, θ_p.

Assuming the signal is Rayleigh, the PDF of the envelope is given by

$$P(R_p) = \frac{R_p}{\sigma^2} e^{\frac{-R_p^2}{2\sigma^2}}, \tag{11}$$

where $2\sigma^2$ is the average power of the input signal.

The probability of θ_p is given by

$$P(\theta_p) = \frac{1}{2\pi}. \tag{12}$$

Therefore, the MSE of point P with polar coordinates (R_p, θ_p) with respect to the nearest quantisation point $Q_{\frac{v}{2}}$ with Cartesian coordinates ($X_{\frac{v}{2}} = \hat{R}_{\frac{v}{2}} \cos\hat{\theta}_1$, $Y_{\frac{v}{2}} = \hat{R}_{\frac{v}{2}} \sin\hat{\theta}_1$) is given by

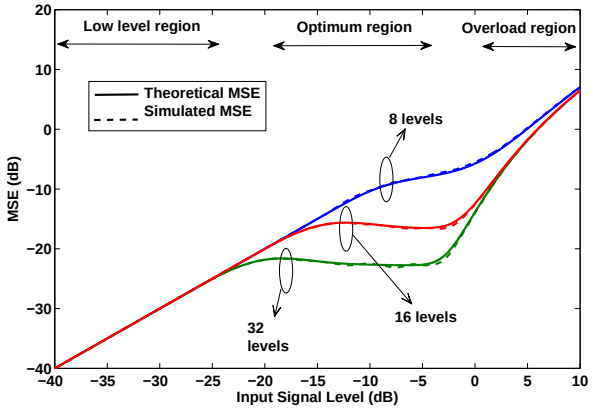

Fig. 6. Theoretical and simulated results of MSE for a stand-alone polar quantiser with three OSR levels. Note, dB values are with respect to 1.0 (the pulse power).

$$MSE\left(Q_{\frac{v}{2}}\right) = \frac{1}{2\pi} \int_{L_\theta(-1,1)}^{L_\theta(1,2)} \int_{L_R\left(\frac{v}{2}-1,\frac{v}{2}\right)}^{L_R\left(\frac{v}{2},\frac{v}{2}+1\right)} [(X_q - R_p cos\theta_p)^2 + (Y_q - R_p sin\theta_p)^2] \times \frac{R_p}{\sigma^2} e^{\frac{-R_p^2}{2\sigma^2}} dR_p d\theta_p. \tag{13}$$

Solving and simplifying the integral gives the MSE for a given amplitude quantisation level (with boundaries $L_R(\frac{v}{2} - 1, \frac{v}{2})$ and $L_R(\frac{v}{2}, \frac{v}{2} + 1)$) and a phase quantisation level (with boundaries by $L_\theta(-1,1)$ and $L_\theta(1,2)$). The boundary limits have previously been defined by the threshold equations (9) and (10) and they are midway between the quantisation points.

$$MSE\left(Q_{\frac{v}{2}}\right) = \frac{1}{2\pi\sigma^2} \left[-\sigma^2 e^{\frac{-R_p^2}{2\sigma^2}} (X_q^2 + Y_q^2) - \sigma^2 (2\sigma^2 + R_p^2) e^{\frac{-R_p^2}{2\sigma^2}} \right]_{L_R(\frac{v}{2}-1,\frac{v}{2})}^{L_R(\frac{v}{2},\frac{v}{2}+1)} \times \left[\theta_p\right]_{L_\theta(-1,1)}^{L_\theta(1,2)} + \frac{1}{2\pi\sigma^2} \left[-X_q^2 sin\theta_p + Y_q^2 cos\theta_p \right]_{L_\theta(-1,1)}^{L_\theta(1,2)} \times \left[-R_p \sigma^2 e^{\frac{-R_p^2}{2\sigma^2}} + \frac{1}{2}\sigma^3 \sqrt{\pi}\sqrt{2} \text{erf} \frac{\sqrt{2}R_p}{2\sigma} \right]_{L_R(\frac{v}{2}-1,\frac{v}{2})}^{L_R(\frac{v}{2},\frac{v}{2}+1)} \tag{14}$$

The final MSE of the phase plane is given by

$$MSE_{final} = N_p \sum_{\frac{v}{2}=0}^{N_A} MSE\left(Q_{\frac{v}{2}}\right), \tag{15}$$

where N_P and N_A are the number of amplitude and phase levels which are related to OSR through (4) and (3). Equation (15) gives the total MSE as a function of the average input power ($2\sigma^2$) and the OSR.

V. Theoretical and Simulated Results of Stand-Alone Polar Quantiser

The non-uniform polar quantiser is simulated to verify the validity of the derived MSE equation. A QPSK-modulated OFDM signal was chosen as input to the simulated quantiser

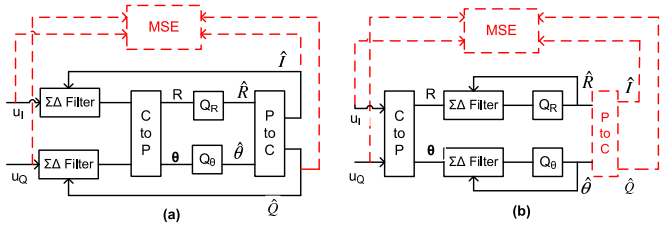

Fig. 7. Block diagrams showing the MSE calculation steps for the Cartesian ΣΔ architecture (a) and the polar one(b).

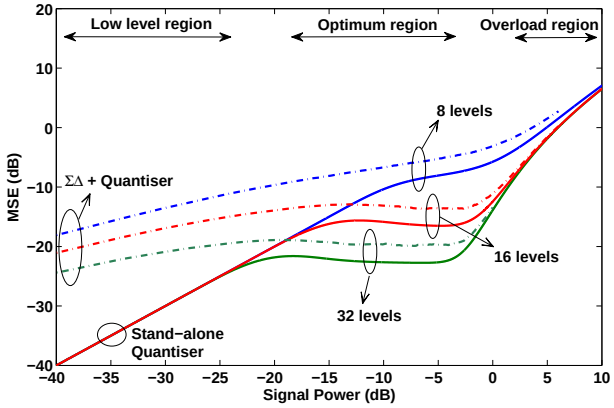

Fig. 8. Simulated results of polar quantiser with and without ΣΔ modulators for different OSR values (Polar ΣΔ architecture).

as it approximates a Rayleigh envelope and hence satisfies the assumption made during the derivation of the MSE equation.

Fig. 6 shows plots of signal power against MSE for the theoretical and simulated quantisers with three different OSR values. It can be observed that the simulated MSE and the theoretical MSE curves are almost indistinguishable.

The MSE is exactly equal to the signal power at low signal levels for all three plots. When the input signal is increased and crosses the first threshold level, the MSE plateaus. The plot with the highest OSR (32 levels) plateaus sooner as its first threshold level is closest to zero. The average MSE is also less for this plot as it has more quantisation levels (N_A and N_P). For the two higher OSR curves (16 and 32), the plateaus have a slightly reducing MSE with increasing signal power: caused by the clustering of the amplitude quantisation levels at larger magnitudes (see Table I). In this region, a 1 dB increase in signal power will give a slightly greater than 1 dB improvement in SNR.

As the signal power is increased beyond the largest quantisation level, the MSE errors again increase. The final quantisation level represents the maximum pulsewidth corresponding to a square wave and is therefore the same for all OSR values. At very high signal levels (the overload region), the MSE will eventually equal the signal power again as shown by the asymptotic curve shape (top right of Fig. 6).

VI. Analysis of Polar Quantiser with and without ΣΔ Modulators

In this section, the MSE of the combined ΣΔ and the polar quantiser is studied. The simulations are carried out on

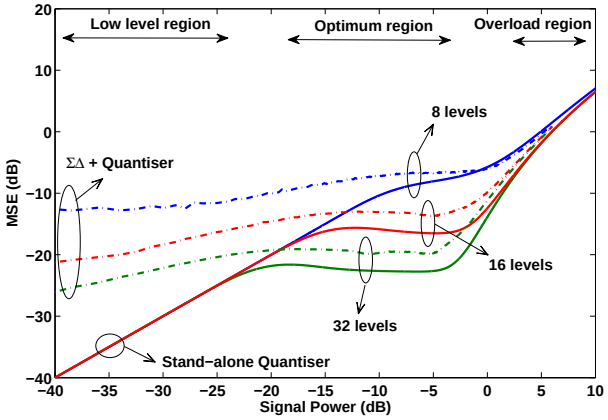

Fig. 9. Simulated results of polar quantiser with and without ΣΔ modulators for different OSR values (Cartesian ΣΔ architecture).

both the polar ΣΔ architecture [4] and the Cartesian ΣΔ architecture [6]. The MSE is measured between the input signal and the quantised output signal as shown in Fig. 7 and includes both in-band and out-of-band components. The latter will eventually be filtered out by the bandpass filter of Fig. 2. The simulations are performed for three different OSR levels (8, 16 and 32) and the results obtained from the polar and Cartesian ΣΔ architectures are shown in Fig. 8 and Fig. 9 respectively. The ΣΔ filters used in both architectures are first order (MOD-1 [14]), with sample rate $f_s = \frac{f_c}{k}$ giving one ΣΔ sample update for every k periods of the RF carrier (k is a positive integer). In this example, k=1 and the input OFDM signal has 16 subcarriers with a combined bandwidth of $\frac{f_s}{64}$.

The MSE plots also plateau but at a level 3 dB higher than the stand-alone quantiser. This trend can be observed for all the three OSR levels but is more evident for the plot with an OSR of 32 as the plateau covers a wider range of signal power. The peak signal quality (signal power/MSE) is obtained when the curves reach a slope of unity. Plots with higher OSR cover a wider range of signal power at a lower MSE. Additionally, the performance at low signal levels is significantly different. The MSE drops at a lower rate as the signal power is reduced. The result is a significant increase in MSE at very low signal levels compared to the stand-alone quantiser. The phenomena are analysed in the following subsections.

A. Mathematical Derivation of Noise Associated with ΣΔ Modulator

The noise increase over the plateau region can be explained from the noise transfer function (NTF) of the ΣΔ modulator. The NTF of a first order lowpass ΣΔ modulator is given by $(1 - z^{-1})$ [14] and its power gain is:

$$|NTF|^2 = \left(1 - e^{j2\pi \frac{f}{f_s}}\right)\left(1 - e^{-j2\pi \frac{f}{f_s}}\right), \qquad (16)$$
$$= 2\left(1 - cos\left(2\pi \frac{f}{f_s}\right)\right).$$

Following the traditional analysis for ΣΔ ADCs, we make the assumption that the quantisation noise is spectrally white.

The MSE can then be calculated by integrating the $|NTF|^2$ over the range of $-f_u/2$ to $f_u/2$, where f_u is the useful band near the desired signal. When the limits are $-f_s/2$ to $+f_s/2$ the overall (total) MSE is calulated as shown below:

$$MSE_{\Sigma\Delta} = 2\int_0^{\frac{f_s}{2}} N_o(f) \times 2\left(1 - cos\left(2\pi\frac{f}{f_s}\right)\right)df, \quad (17)$$

where $N_o(f)$ is the quantisation noise power spectral density introduced by the quantiser (15)

$$N_o(f) = \frac{MSE_{final}}{f_s}. \quad (18)$$

Substituting (18) in (17) and evaluating the integral gives

$$MSE_{\Sigma\Delta} = \frac{MSE_{final}}{f_s} \times 4 \times \left[f - \frac{f_s}{2\pi} sin(2\pi\frac{f}{f_s})\right]_0^{0.5f_s}, \quad (19)$$

$$MSE_{\Sigma\Delta} = MSE_{final} \times 2,$$

which explains the 3 dB noise increase in the plateau region of Fig. 9. Higher order $\Sigma\Delta$ modulators would expect an even greater noise enhancement. It is for this reason that low order $\Sigma\Delta$ modulators are often preferred, since the noise must be filtered out at the amplifier output with low insertion loss RF bandpass filters.

The output spectrum of the quantiser is plotted at an input power of -10 dB for the Cartesian $\Sigma\Delta$ architecture. The first order lowpass $\Sigma\Delta$ NTF is superimposed on the simulation plot and agreement between the theoretical and simulation plots is observed as shown in Fig. 10. The analysis clearly predicts the correct performance of the $\Sigma\Delta$ modulator when the signal power is in the plateau region. However the PWM/PPM drive signal shows small distortion shoulders at the edge of the OFDM signal. These are caused by folded back distortion products from higher harmonics created by the rectangular pulse shape of the signal [13].

B. Practical measurements

The waveforms were generated on a $Tektronix\ DTG5274$ data timing generator with f_{clock} = 2.048 GHz. Two channels of the data timing generator are set to output two streams of data simultaneously. The data of one of the channels is inverted and phase shifted by π radians. A passive combiner circuit then sums the two streams to produce a three-level waveform. The carrier frequency and signal bandwidth was scaled down to 64 MHz and 1 MHz respectively with OSR=32. The measured spectrum adjacent to the signal band shows a slight degradation of about 2 dB compared to the simulated spectrum, but agrees with predictions elsewhere (Fig. 11). The probable causes of the disparity are slight imbalances between the two channels in the analog combiner and slew rate limitations on the digital waveforms. The latter will become more of a problem at higher clock frequencies. Lower OSRs will be needed for higher carrier frequencies. For information, the bandwidth-scaled WLAN and WCDMA spectrum masks are shown. The WLAN specifications can be met if the RF bandpass filter cuts off at about 4.5 channel bandwidths out from the centre frequency. A much narrower bandpass filter is required to meet the tougher WCDMA mask ($\approx$ 1.2 channel bandwidths from the centre frequency).

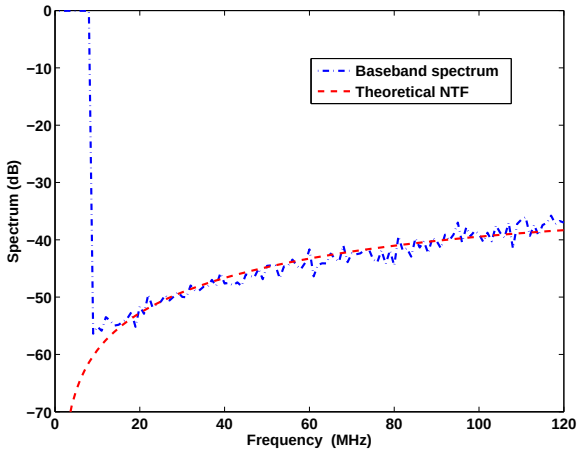

Fig. 10. Simulated output spectrums of the Cartesian $\Sigma\Delta$ modulators superimposed on a theoretical NTF plot of a first order $\Sigma\Delta$ modulator. The modulation is OFDM with 16 sub-carriers and the OSR is 32. Only positive frequencies are shown.

VII. Low Signal Behaviour of $\Sigma\Delta$ Modulators

The 3 dB MSE increase derived in (19) does not forecast the operation of the $\Sigma\Delta$ in the low signal region as shown in Fig. 8 and Fig. 9. A different analysis is required for that section of the graph and is discussed next.

At low signal levels limit cycles are produced. The output of the $\Sigma\Delta$ modulator is characterised by a string of zero valued samples, $\hat{R}_0$, followed by an occasional jump to $\hat{R}_1$. It is the jump to $\hat{R}_1$ that causes the higher than expected MSE. This jump can be attributed to the integrator loop inside the $\Sigma\Delta$ modulator.

The operation can be explained by just considering the magnitude component of the polar $\Sigma\Delta$ [4]. Consider a first order $\Sigma\Delta$ with a constant input signal, $u = \delta$; $\delta \ll L_R(0,1)$ as shown in Fig. 12. The error across the quantiser $(R - \hat{R})$ is fed back in to the $\Sigma\Delta$ causing the quantiser input signal, R, to ramp up in steps of δ. When the first threshold is reached, the output changes from $\hat{R}_0(=0)$ to $\hat{R}_1$ causing a large pulse in the quantiser output, resetting R to a value close to $\frac{\hat{R}_1}{2}$. The system works like a relaxation oscillator. [1] The output pulse occurs every $N_T = \frac{\hat{R}_1}{\delta}$ samples. The error between the analog input and the quantised output $(u - \hat{R})$ is also shown in the Fig. 12(c). The MSE is therefore given by:

$$MSE(\delta) = \frac{N_T\delta^2 + (\hat{R}_1 - \delta)}{N_T + 1}. \quad (20)$$

When the input signal is replaced by a Rayleigh distributed envelope signal, the amplitude, δ, can be approximated by the mean signal level, $\sigma\sqrt{\frac{\pi}{2}}$, and the power of the signal, δ^2, is

[1] Limit cycles are often associated with unwanted spurs in the band of interest and the traditional solution is to smooth out the spectrum by adding dither signals [15]. In this work, we only consider the MSE and not its frequency distribution.

TABLE II
SIMULATION CONDITIONS AND RESULTS.

Curve	Quantisation	N_q	OSR	$\Sigma\Delta$ Order	Edges /RF Period	Coding Efficiency
(a)	Bandpass $\Sigma\Delta$	4	4	1	2	4%
(b)	Cartesian $\Sigma\Delta$, Even	5	4	1	0.82	10.2 %
(c)	Bandpass $\Sigma\Delta$	4	4	2	2	4 %
(d)	Cartesian $\Sigma\Delta$, Even	5	4	2	1.7	4.8 %
(e)	Cartesian $\Sigma\Delta$, Both	9	4	2	1.53	7.8 %
(f)	Cartesian $\Sigma\Delta$, Both	33	8	2	1.66	8 %

approximated by $2\sigma^2$. This gives:

$$N_T \approx \frac{\hat{R_1}}{\sigma\sqrt{\frac{\pi}{2}}}, \tag{21}$$

$$MSE(\sigma) \approx \frac{N_T(2\times\sigma^2) + (\hat{R_1} - \sigma\sqrt{\frac{\pi}{2}})^2}{N_T + 1}. \tag{22}$$

Equation (22) is superimposed over the simulated MSE vs. signal power plots of an OFDM signal generated from polar $\Sigma\Delta$ modulator (Fig. 13). The signal power axis of the simulated values is extended to -60 dB to observe the low signal behaviour of the $\Sigma\Delta$ modulators. The plots show that the derived equation is almost a straight line and asymptotic to the simulation results at low signal levels. The gradient is 0.5. The simulation results start to deviate from the theoretical analysis when the first threshold level is reached and in Fig. 13 this phenomenon is more evident with an OSR of 32 as the threshold level is attained at a lower signal power.

It should be noted that phase quantisation effects have almost no contribution to the MSE at low signal levels. This is because the dominant contribution to MSE is the $(\hat{R_1} - \delta)^2$ term. If the phase of $\hat{R_1}$ changes the resultant power variation is small since δ is very small.

Equation (22) can be simplified when σ is much less that $\hat{R_1}$. The numerator can be approximated with $\hat{R_1}^2$ and the unity term can be neglected in the denominator giving

$$MSE = \frac{\hat{R_1}^2}{\frac{\hat{R_1}}{\sigma\sqrt{\frac{\pi}{2}}}},$$

$$10\log(MSE) = 0.5(10\log(2\sigma^2)) + 5\log(0.5) + 10\log\left(\hat{R_1}\sqrt{\frac{\pi}{2}}\right), \tag{23}$$

$$MSE(dB) = 0.5 \times SignalPower(dB) + C. \tag{24}$$

Equation (24) indicates a straight line with gradient of 0.5 dB/dB as shown in Fig. 13. A 1 dB increase in signal power will improve the SNR by only 0.5 dB. This gradient is less than the stand-alone quantiser and indicates that the $\Sigma\Delta$ process boosts noise beyond that predicted by traditional $\Sigma\Delta$ analysis. The boosted noise will lead to degrading SNR values as the signal power is reduced and could have implications on transmitters with a wide power control range, such as those found on W-CDMA handsets.

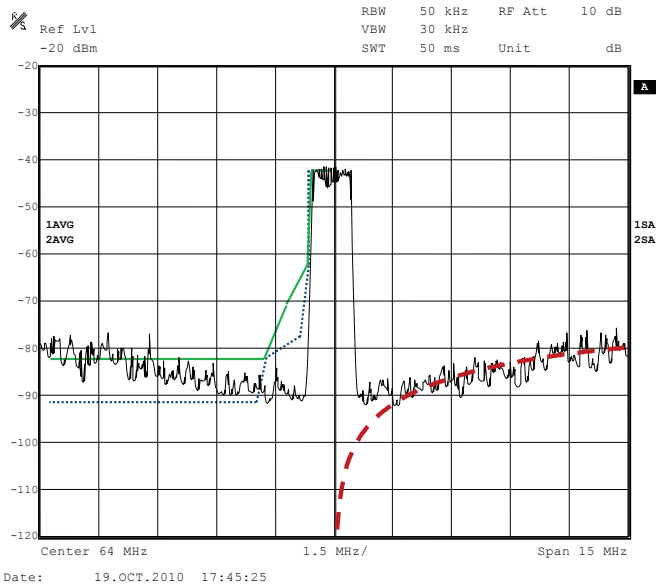

Fig. 11. Measurement result, OSR=32. The theoretical NTF is shown dashed. Spectrum mask: WCDMA - dotted and WLAN - full line.

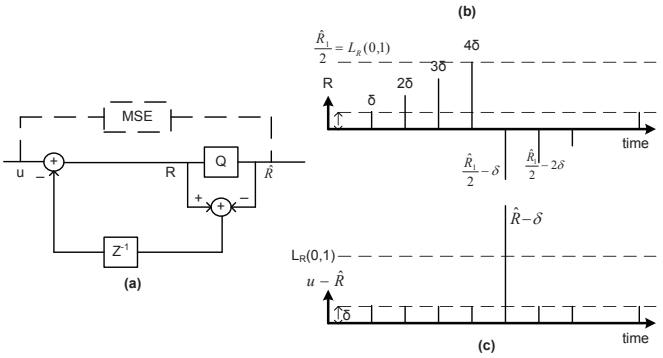

Fig. 12. (a)shows a simplified first order $\Sigma\Delta$ modulator. (b) shows a plot of the input, R, to the quantiser and (c) plots the difference between u and the quantiser output, $\hat{R}$.

VIII. Practical Applicability

A. Implementation Issues

Fig 2 shows that the quantiser is within the $\Sigma\Delta$ feedback loop and so increasing the quantiser complexity could slow down the loop sample rate, f_s. The non-linear polar quantiser must quantize OSR phases and $OSR/4$ amplitudes. Up to eight phases can be identified by comparing the sign and magnitudes of the I and Q signals. The coordinate rotation digital computer (CORDIC) is used to calculate the signal amplitude (and also the phase when OSR $>$ 8) [16]. Four CORDIC iterations gives an amplitude accuracy of 1% . The quantized Cartesian feedback values (I,Q) are obtained from

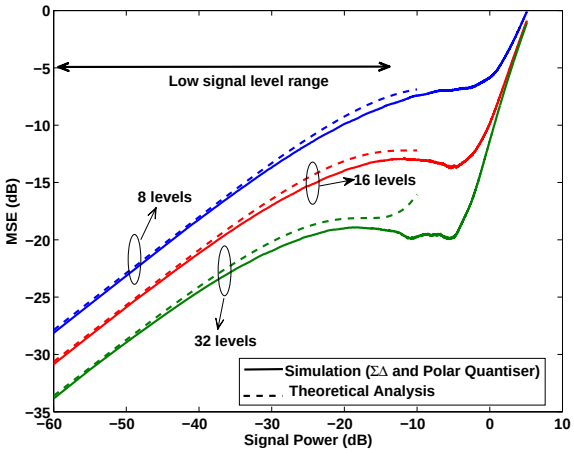

Fig. 13. Simulated and theoretical analysis of low-signal behaviour of ΣΔ modulators on MSE.

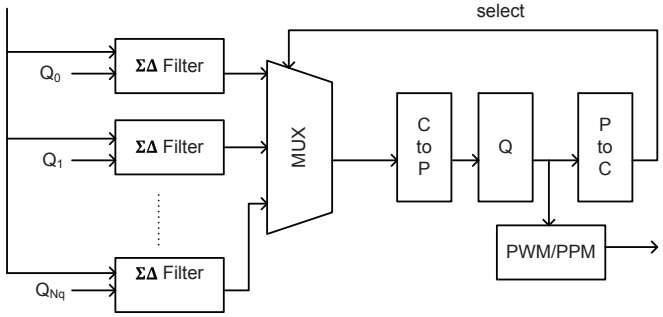

Fig. 14. Low latency Cartesian ΣΔ structure for FPGA implementation.

a look-up-table with N_q entries. The PWM/PPM outputs are obtained from a look-up table in a similar manner, and passed to a serialiser to generate the bit stream.

The architecture was synthesized for FPGA implementation targeted at the Altera Stratix IV. An OSR=8, MOD-2 system implemented in 16-bit fixed point arithmetic took 13 cycles, at a 0.65 GHz cycle rate. The filters took 7 cycles and the polar quantiser took 6 cycles giving a ΣΔ sample rate of f_s = 52.3 MHz. Note that the bandpass ΣΔ structure would not have the 6 cycle quantiser overhead and consequently a higher f_s = 86.9 MHz. Higher sample rates are generally preferable since they allow higher bandwidth signals. The speed disadvantage of the polar system can be overcome by implementing a parallel ΣΔ structure (Fig. 14) in which the ΣΔ filters do not wait for the quantiser output, but operate on all possible N_q quantiser states at once. When the quantiser completes its decision then it selects the appropriate ΣΔ filter output (including its internal states). The other ΣΔ filter outputs are discarded. The N_q ΣΔ filters operate in parallel with the quantiser and the longest latency sets the sampling frequency; in this case the 7 cycles of the ΣΔ filter. The new sample rate is now f_s = 86.9 MHz, the same as the bandpass ΣΔ structure. The downside of the Cartesian ΣΔ structure is therefore either reduced f_s or increased chip-area and power consumption. Even so, the circuit used up less than 1% of the EP4S40G2F40I2 parts total FPGA area (361 combinational ALUTs and 483 logic registers).

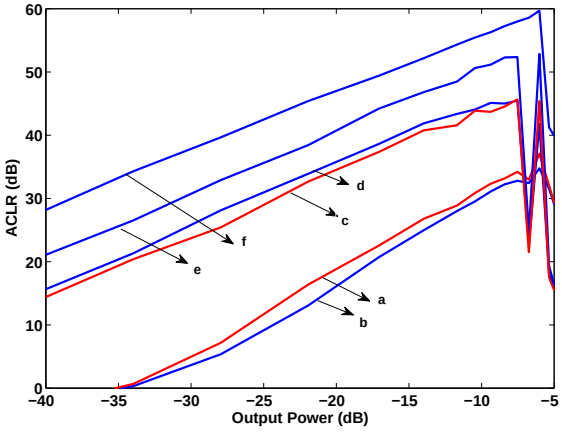

Fig. 15. ACLR vs. Output power. Bandpass ΣΔ (red) and Cartesian ΣΔ (blue) as per Table II.

FPGAs with on-board serializers are now available. Potential clock speeds are in the tens of GHz [18], indicating the possibility of carrier frequencies above 1 GHz for an OSR of 8. Note that if $f_s = 86.9MHz$ (as above) then k $\geq$ 12 would be also be required. FPGA's are not particularly power efficient and so ASIC designs would be preferable in this regard.

B. Performance Comparisons

The non-linear polar quantiser of the Cartesian ΣΔ enables a trade off between carrier OSR and quantiser fidelity. In this subsection we illustrate the design trade-offs and compare the Cartesian ΣΔ to the well known bandpass ΣΔ schemes of [19]- [20]. The latter schemes use a lowpass ΣΔ to convert the input I and Q signals to bipolar (+1 or -1) bitstreams which then invert (or otherwise) the digital in-phase (+1,0-1,0+1, ..) and quadrature (0,+1,0,-1,0, ..) carriers prior to their summation. The all-digital process is very simple but requires OSR = 4 (i.e. $f_c = f_{clock}/4$). The two states of each I and Q output can be represented in the phase plane by $N_q = 4$ equal amplitude quantisation points separated with phase increments of $\pi/2$. In the following simulations, an OFDM signal is upconverted to a normalised centre frequency of $f_c = 1024$. It has a bandwidth of $W = 8$ (or $f_c/128$) and 8 sub-carriers; in this way the peak to average power ratio (PAPR) is limited to 9 dB. In this simulation k = 2, so the ΣΔ sample rate is $f_s = f_c/2 = 512$ which oversamples the signal by 64. Parameters for the simulated schemes are shown in Table II. We use the adjacent channel leakage ratio (ACLR) of Fig 15 to compare the close in-band performance of the schemes, while a broader spectrum view is obtained from Fig 16.

The traditional bandpass ΣΔ schemes have similar in-band performance to the basic 'even' quantised, OSR = 4, Cartesian ΣΔ scheme. This is as expected since they have almost the same number of quantisation points ($N_q = 4$ for bandpass ΣΔ and $N_q = 5$ for Cartesian ΣΔ). The MOD-1 version of the Cartesian ΣΔ scheme (trace b) generates about 1.5 dB more ACLR compared to the Bandpass ΣΔ(trace a) scheme. The situation reverses with the higher order MOD-2 filter

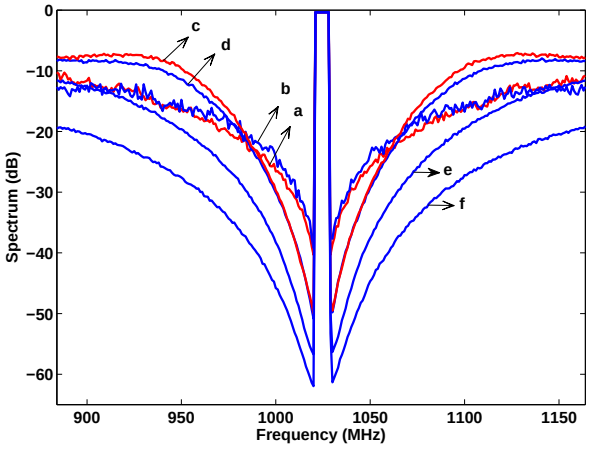

Fig. 16. Normalised OFDM spectrum vs frequency, output power = 8 dB.

(traces c and d). However, in both cases the Cartesian $\Sigma\Delta$ has better out-of-band performance, better coding efficiency and a reduced number of transitions, which stems from the additional (0,0) quantisation point. Note, the overall effect of the higher order $\Sigma\Delta$ filter for both schemes is to reduce the in-band noise, at the expense of out-of-band noise. However, increasing the complexity of the quantiser from $N_q = 5$ to $N_q = 9$ by allowing both even and odd pulse widths (trace e) gives both a 5 dB reduction in ACLR and significant reductions in out-of-band noise. Increasing the OSR to 8 (trace f) makes $N_q = 33$, giving a further 6 dB noise reduction across the whole band. Any reduction in out-of-band noise will directly ease the final band-pass filter requirements leading to reduced insertion loss.

The quantisation point (0,0) produces a null output without transitions and so reduces the switching activity and improves the coding efficiency of the Cartesian $\Sigma\Delta$ schemes (Table II). Switching loss associated with the charging and discharging of parasitic capacitors in the following amplification stages is therefore reduced. This was one of the motivations behind the development of the schemes [4], [13]. First order $\Sigma\Delta$'s benefit most, with switching activity more that halved from 2 edges to 0.82 edges per period of the RF carrier, but there is less reduction (15% to 20%) when the $\Sigma\Delta$ filter order is increased. The latter can be put down to the increased signal level into the quantiser caused by the enhanced noise amplification of the MOD-2 NTF [14]. The reduced edge count is also a factor in the improvement in coding efficiency (defined as the useful signal power to the total signal power, [21]). The results indicate coding efficiency improves with quantisation resolution (N_q), but reduces with filter order.

IX. Conclusion

MSE expressions have been derived for a non-linear polar quantiser when transmitting OFDM/CDMA-like signals. The expression predicts the noise behavior of the $\Sigma\Delta$ upconversion process. At low signal levels a first order $\Sigma\Delta$ upconverter is dominated by limit cycle behavior and the SNR increases by only 0.5 dB for every 1 dB increase in signal strength. In the medium range, the MSE from the quantiser does not depend on signal power and is amplified by the NTF. Here the SNR increases at a rate slightly greater than 1 dB per 1 dB increase in signal strength. In the overload region, the MSE increases with increasing signal power with a slope greater than 1, so the SNR reduces by $>$ 1 dB per 1 dB increase in signal power. The OSR determines the number of quantisation points, N_q, in the signal phase plane. These points are concentrated in the high signal power region, which will particularly benefit modulations with lower peak to average power variations (e.g. $\pi/4$ shift QPSK or SC-FDMA which is used in the LTE uplink). Even so, we show through analysis, simulations and measurements that a first order $\Sigma\Delta$ with an OSR of 32 comfortably meets the WLAN mask for OFDM transmission. We show through simulations comparing Cartesian $\Sigma\Delta$ with the traditional bandpass $\Sigma\Delta$ methods that nonlinear polar quantisation, reduces the number of transitions per RF period, improves coding gain, and gives the designer another degree of freedom in determining spectral performance. In-band noise performance can now be improved by both increasing the $\Sigma\Delta$ order (as per bandpass $\Sigma\Delta$), or by increasing quantiser fidelity with a higher OSR. The former degrades out-of-band performance, while the latter improves out-of-band performance (by 6dB per octave of OSR) but has a complexity that grows with OSR squared. Hardware technology places a limit on the OSR f_c product, but recent product announcements by FPGA vendors [18] indicate the growing feasibility of carrier frequencies above 1 GHz.

References

[1] V. Bassoo, K. Tom, A.K. Mustafa, E. Cijvat, H. Sjoland, and M. Faulkner: "A Potential Transmitter Architecture for Future Generation Green Wireless Base Station", *EURASIP Journal on Wireless Communication and Networking*, 2009.

[2] Intel, "World's first 2- Billion transistor microprocessor." Internet: http://www.intel.com/technology/architecture-silicon/ 2billion.htm?id=tech mooreslaw+rhc 2b, Jan 2010, [Apr. 20 2010].

[3] P.M. Asbeck, I. Galton, L.E. Larson, X. Zhang, M. Iwamoto, J. Hinrichs and J. Keyzer,"Digital Control of Power Amplifiers for Wireless Communications" in Proc. European Microwave Conference vol., no., pp.1-4, 24-26 Sept. 2001.

[4] J. Keyzer, R. Uang, Y. Sugiyama, M. Iwamoto, I. Galton, P.M. Asbeck: "Generation of RF Pulsewidth Modulated Microwave Signals using Delta-Sigma Modulation",in *Proc. Microwave Symposium Digest, 2002 IEEE MTT-S International*, vol.1, no., pp.397-400, 2002.

[5] B.Razavi. *RF Microelectronics*, Prentice-Hall, 1998.

[6] V. Bassoo and M. Faulkner, "Sigma-delta digital drive signals for switch-mode power amplifiers," *Electronics Letters*, vol.44, no.22, pp.1299-1300, Oct. 2008.

[7] J. Tuthill, A.Cantoni, "Efficient compensation for frequency-dependent errors in analog reconstruction filters used in IQ modulators", *IEEE Trans. on Communications*, vol. 53, n0. 3, pp 489-496, 2005.

[8] M. Helaoui, S. Hatami, R. Negra, and F. Ghannouchi, "A novel architecture of Delta-Sigma Modulator Enabling All-Digital Multiband Multistandard RF Transmitters Design", *IEEE Trans. Circuits and Systems II.*, vol. 55, no.11, pp 1129-1133, 2008.

[9] Y. Wang, "A class-S RF amplifier architecture with envelope delta-sigma modulation," In *Proc. IEEE-RAWCON 2002*, pp.177-179, 2002

[10] J. Jeong, and E.Y. Wang, "A Polar Delta-Sigma Modulation Scheme for High Efficiency Wireless Transmitters" in *Proc. IEEE IMS Int. Microwave Symposium*, Honolulu, USA, pp.73-76, Jun. 2007.

[11] J. C. Candy and G. C. Temes, "Oversampling methods for A/D and D/A conversion," in *Oversampling Delta-Sigma Converters*, J.C. Candy and G.C. Temes, Ed. New York:IEEE Press, 1991.

[12] B. Li and H. Tenbunen, "Sigma delta modulators using semi-uniform quantizers," in *Proc. ISCAS 2001*, vol.1, pp.456-459, May 2001.

[13] V. Bassoo, L. Linton and M. Faulkner, "Analysis of Distortion in Pulse Modulation Converters for Switching Radio Frequency Power Amplifiers," *IET Microwaves, Antennas and Propagation*, to be published.
[14] R. Schreier, and G.C. Temes. *Understanding Delta-Sigma Data Converters* Wiley-IEEE Press, 2004.
[15] W. Chou and R. M. Gray,"Dithering and its effects on sigma-delta and multi-stage sigma-delta modulation", *IEEE Trans. Inform. Theory*,vol. 37, pp.500-513, 1991.
[16] J. Volder, "The CORDIC Trigonometric Computing Technique", *IRE Transactions on Electronic Computers*, pp. 330-334, September 1959.
[17] Altera Corporation, "Introducing Innovations at 28 nm to Move Beyond Moores Law" Internet: http://www.altera.com/literature/wp/wp-01125-stxv-28nm-innovation.pdf, July 2010 [9 Jan 2012]
[18] Altera Corporation, "Stratix V FPGAs: Built for Bandwidth" Internet: http://www.altera.com/devices/fpga/stratix-fpgas/stratix-v/stxv-index.jsp, February 2012.
[19] R. Schreier and M. Snelgrove, "Bandpass sigma-delta modulation," *Electron. Letters*, vol.25, pp. 1560–1561, Nov. 1989.
[20] S. P. Stapleton, "High efficiency RF Power Amplifiers Using Bandpass Delta-Sigma Modulators," *Agilent Technologies*, Mar. 2003.
[21] T. Blocher, P. Singerl, "Coding efficiency for different switched-mode RF transmitter architectures," *Proc. IEEE MWSCAS Int. Midwest Symposium*, Cancun, Mexico, pp.276-279, Aug. 2009.