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Design of a 300-Watt Isolated Power Supply with Minimized Circuit Input-to-Output Parasitic Capacitance

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Abstract

This paper presents the design of a 300-Watt isolated power supply for MOS gate driver circuit in medium and high voltage applications. The key feature of the developed power supply is having a very low circuit input-to-output parasitic capacitance, thus maximizing its noise immunity. This makes it suitable for modular stacking applications. The converter is a voltage-controlled current source, utilizing a transformer that has an extremely low inter-winding parasitic capacitance. The experiments show that an overall circuit input-to-output parasitic capacitance of 10 pF can be achieved. Design analysis and experimental results are provided to prove the feasibility of the converter.

1 Introduction

Research on common-mode noise mitigation has received great attention since the introduction of electromagnetic interference (EMI) regulations [1-8]. Among the existing approaches, design of transformers with minimized inter-winding parasitic capacitance and utilization of suitable topologies is a very typical approach. In [1], an unusual transformer winding structure and an unconventional converter topology were proposed. The system achieved 1 pF parasitic capacitance at its output power of 36 V, 0.2 A. Later on, similar approaches [2]-[4] were proposed using a similar transformer structure. Nevertheless, the reported previous works provided neither experimental results nor elaborate analysis of the converter's operation.

This paper seeks to further investigate and validate the merit of the converter topology in Fig. 1 which was firstly proposed in [1]. A higher output power rating is aimed, which is 300 W per module. The prototype is built in a way that minimizes the circuit input-to-output parasitic capacitance, making it less susceptible to noise and suitable for modular stacking. The overall circuit input-to-output parasitic capacitance is 10-pF, which, to the authors' best knowledge, is the lowest of their kind with 300 W output power rating.

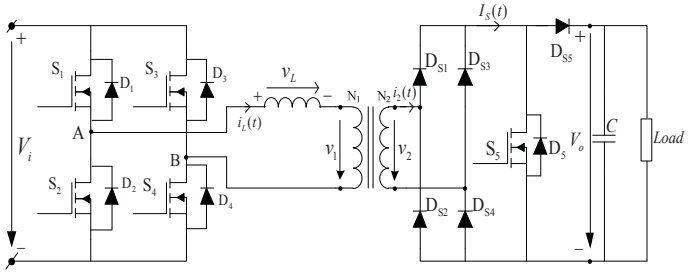


Fig. 1. Topology of the proposed converter.

2 System requirements

Referring to the converter in Fig. 1, the input dc supply voltage of the converter is usually the output of a power factor correction converter which converts a single phase 220-V ac voltage into 400 V dc voltage. Therefore, a dc input of 400 V is chosen in the design. The output voltage is chosen to be 60 V dc, since it allows a variety of power switch selections which have a breakdown voltage of 100 V dc. If, for example, higher output voltage is desired, then more than one converter modules can be stacked in series. The output current is designed to be 5 A maximum. This specification means the maximum output power that is available in the output terminals is 300 W. Furthermore, an extremely low total circuit input-to-output parasitic capacitance of 10 pF is aimed. All of these specifications are stated in Table 1.

Input voltage	400 V
Output voltage	60 V
Output current	5 A
Maximum output power	300 W
Circuit input-to-output capacitance	10 pF

Table 1. Design specification

3 Common mode noise paths

The common mode noise paths are shown in Fig. 2. In this topology, the nodes that have high dv/dt are nodes A, B, X, Y, and Z. In nodes A and B, there are changes of voltage from $\pm V_i$ to $\mp V_i$ with respect to the primary side return. Nodes X, Y, Z see a change of 0 V to 60 V with respect to the

secondary side return. These nodes are the sources of common mode noise currents. In the developed prototype, there are two heat-sinks used, one for each side to reduce the capacitive coupling between the two sides. Since the drains of switch S_2 and S_4 are switching nodes and they are both attached to heat-sink 1, the coupling paths include capacitances from drains of S_2 and S_4 to heat-sink 1, and capacitance from heat-sink 1 to chassis/earth. In implementation practice, the heat-sink can be electrically connected to the return path (not the chassis/earth) to further mitigate the transmission of common mode noise current. The coupling paths in the secondary side include the capacitances from cathode of $D_{S1}, D_{S2}, D_{S3}, D_{S4}$ and the drain of S_5 to heat-sink 2, and capacitance from heat-sink 2 to chassis/earth. The coupling path caused by the transformer is from the inter-winding capacitance C_{int}. It can be clearly seen that, C_{int} is in series with the other coupling capacitances, forming a loop of common mode noise paths. Therefore, the value of C_{int} determines the overall common mode noise performance. The typical value for the other coupling capacitances but the inter-winding capacitance falls into the range from 100 pF to tens of micro farads [9]. If C_{int} can be made much smaller than the other coupling capacitances, then the overall circuit input-to-output capacitance is governed by C_{int}.

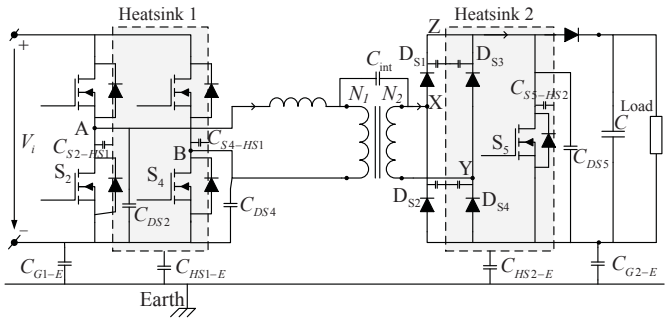


Fig. 2. Common mode noise paths

4 Transformer specification, configuration and validation

The proposed transformer's general structure is illustrated in Fig. 3a, whereas the transformer under test's photo is in Fig. 3b. In its winding configuration, the winding that has smaller number of turns will be place in the geometry centre of the core, forming a rectangular frame symmetrically around the core. The remaining winding with most number of turns is wounded tightly around the core. This is respectively the case of the secondary winding and primary winding in Fig. 3. With this structure, the two winding are separated from each other by a reasonably high distance. Moreover, the die-electric material between them is only the surrounding air, which has the second lowest permittivity to vacuum. All of these features results in an extremely low inter-winding parasitic capacitance that the transformer possesses.

To arrive at a design procedure or guideline of making a transformer that has a specific inter-winding parasitic capa-

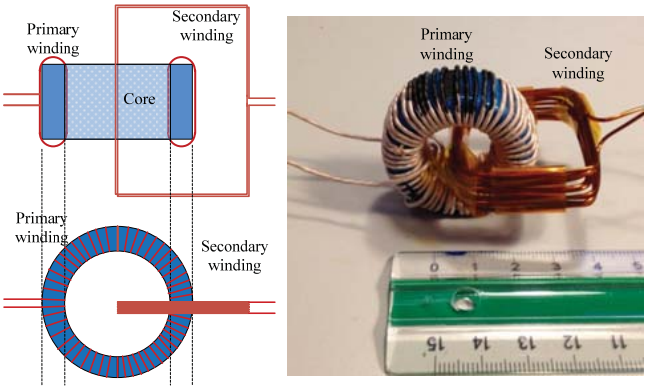


Fig. 3. Transformer structure: a) conceptual structure b) the transformer under test.

-citance, it usually requires mathematic modelling and solving, or simulation based on finite-element method. Apart from that, the design of the transformer is a compromise of different issues like its power losses and physical size of the whole circuit. The transformer is often the most bulky part in the prototype of a power electronics converter. As a result, the size of the transformer highly affects the size of the prototype. It is preferable to go for smaller size of transformer so that the prototype is smaller, and therefore, the parasitic capacitance coupling to earth is smaller. The derivation of the transformer design procedure can be treated as a separated issue. This issue, however, is not addressed in this paper, which focuses on system analysis and experiment validation of the converter as a whole.

Material	N87
Dimension	36 mm×25 mm×13 mm
Turn ratio	55:11
Primary winding	Litz-wire 60×0.2 mm
Secondary winding	Copper 1 mm

Table 2. Transformer parameters

The specifications of the developed transformer are provided in Table 2. Fig. 4. shows the experimental data of the inter-winding impedance magnitude and phase of the transformer. It is done with both terminals of each winding shorted. As can be seen, the impedance magnitude has a constant slope with -20dB/dec roll off, and the phase is around -90^0. Therefore, the inter-winding is capacitive and it is appropriate to model the inter-winding impedance as a lump-element circuit with an inter-winding-capacitor. The measured data are in the form of digital values of impedance's magnitude and phase at a sweep of different frequencies. They are imported into MATLAB and processed by proper scripts to yield the interpreted coupling capacitance, whose values are shown in Fig. 5. It can be seen that the capacitance value is around 10 pF in the wide range of frequency from dc to 10 MHz. It is validated that with the distinct configuration of the transformer, an extremely low inter-winding parasitic capacitance can be achieved.

The process is repeated for the measurement of the impedance between two terminals of the primary side while the two terminals of the secondary side shorted. This impedance can be modelled as a leakage inductor. The impedance magnitude and phase are shown in Figs. 6a and 6b. The impedance behaves like a resistor at frequency up to 1 kHz due to winding ohmic resistance, like a leakage inductor from 2 kHz to 1.5 MHz due to leakage flux, and like a capacitor from above 1.5 MHz due to the self-capacitance of the leakage inductor. The interpreted magnitude of the leakage inductor is shown in Fig. 6c. The leakage inductance value is 170 uH in the range of 100 kHz to 300 kHz. The consequential relatively high leakage inductance can be explained as being caused by the high geometry separation of the two windings which produces relatively large leakage flux outside the core. Hence, the proposed topology as well as its associated control approach should be able to utilize the leakage inductor. The control approach will be presented in the next section.

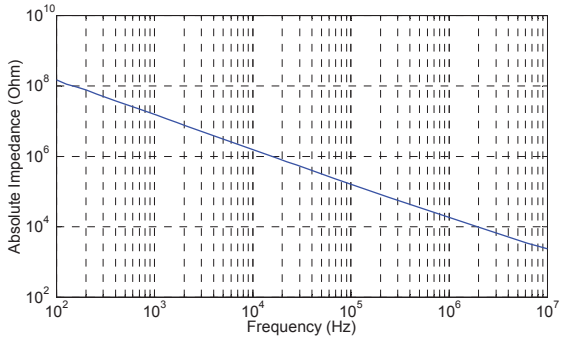


Fig. 4 (a)

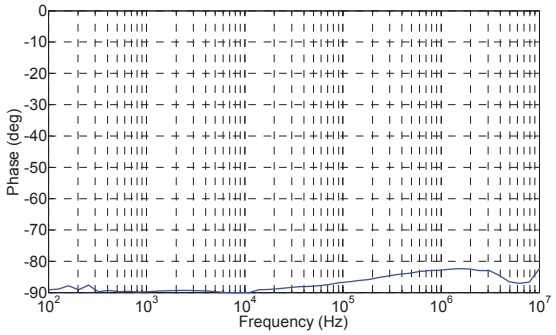


Fig. 4(b)

Fig. 4. Inter-winding impedance measurement: a) magnitude, b) phase

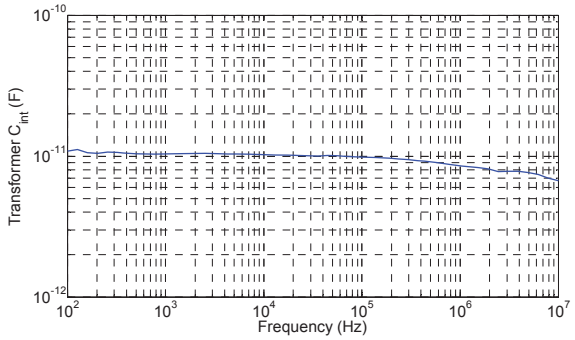
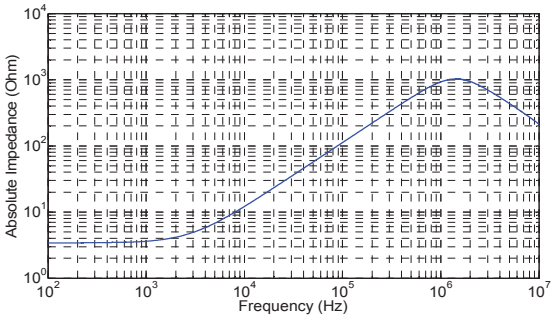
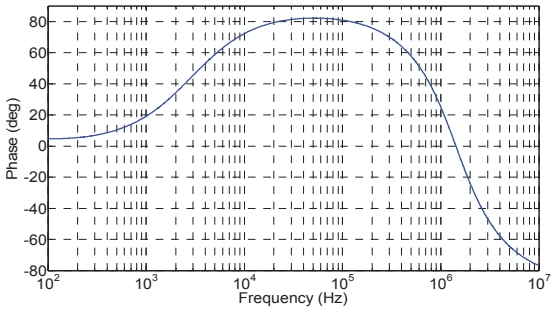


Fig. 5. Interpreted parasitic capacitance



(a)



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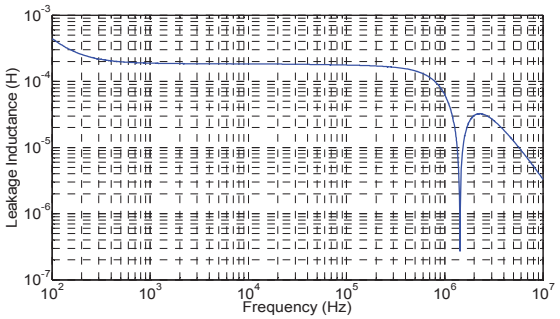


(c)

Fig. 6. Primary winding impedance: a) magnitude, b) phase, c) interpreted leakage inductance

5 Converter operation and control

In this paper, the control approach without an isolated feedback is adopted as to achieve minimum circuit input-to-output parasitic capacitance. The proposed physical configuration of the converter is shown in Fig. 7. There are two control loops where one resides in the primary and the other one resides in the secondary. The secondary side controller regulates the output voltage to be constant at 60 V. The primary side controller controls the primary-side inductor current; thus, indirectly regulate the nominal output current. The secondary side circuit can be seen as a current source supplying the output capacitor in parallel with the load. Because of the diode rectification in the secondary side, the output current is the result of the rectified inductor current multiplying with the inversion of the turn ratio.

$$I_S(t) = \frac{N_1}{N_2}\left|i_L(t)\right| \tag{1}$$

The secondary side controller regulates the output voltage to be constant at 60 V. The output voltage is sensed by a voltage divider, compared to a hysteresis reference to switch on and off the shunt switch S_5. When switch S_5 is on, shunting the

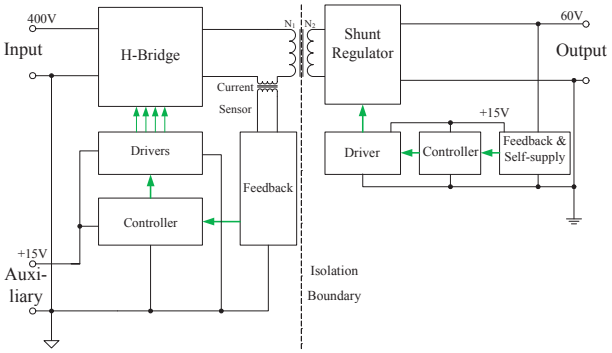
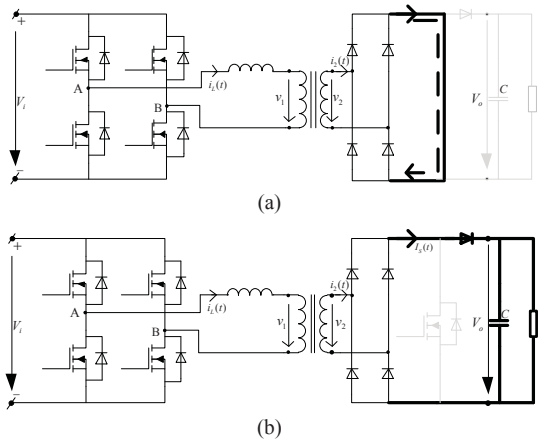


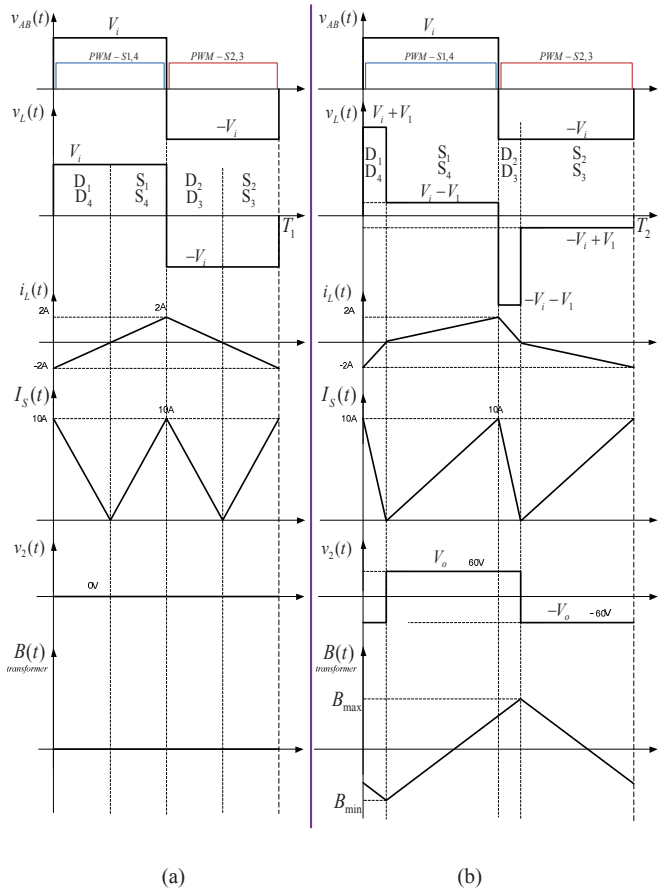
Fig. 7. Block diagram of the physical layout of the converter



(a)

(b)

Fig. 8. Operation modes: a) shunt mode, b) power mode.



(a) (b)

Fig. 9. Analytical waveforms when converter operates in a) shunt mode, b) power mode.

secondary side, the converter operates in its shunt mode (Figs. 8a and 9a); the output voltage decreases. Vice versa, when S_5 is off, the converter operates in its power mode, which is shown in Figs. 8b and 9b; the output voltage increases. In the primary side, since the leakage inductance is relatively high, which is 170 uH; it is utilized as the main inductor in the circuit and there is no external inductor added. The primary side inductor current can be controlled by either adjusting one variable among the three variables of the primary switches: frequency, phase shift, or duty cycle. In this paper, the frequency modulation is chosen. The duty cycle of the switches is kept at 50%, and the phase-shift is therefore at zero degree. The primary side current i_L is sensed and rectified. After that, it is low-pass filtered (LPF) to get the rectified-dc value. This value is then compared to a rectified-dc reference and processed by an analogue proportional-integral (PI) compensator. The output of the PI compensator is fed to a voltage-controlled oscillator (VCO) to keep the rectified primary dc current to be constant at 1 A dc. With a turn ratio of 5:1, the rectified dc current at the secondary side is controlled at 5 A dc. The control block diagrams are presented in Fig. 10.

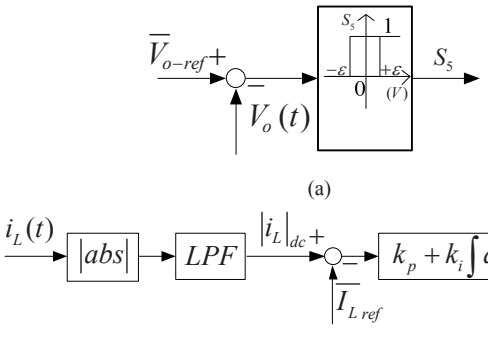
The switching frequency that ensure the primary side to be regulated at the peak value of $\hat{i}_L$ can be derived by equating the product of voltage across the inductor and time when the current is negative to the one during which the current is positive. It can be proved that:

$$f = \frac{V_i}{4\hat{i}_L L}\left(1-\frac{V_1^2}{V_i^2}\right) \tag{2}$$

In the power mode, the voltage across the primary winding of the transformer V_1 is reflected from the output voltage from the secondary side multiplied by the turn ratio if forward voltage drops from the rectifier stage diodes are neglected. In the shunt mode, this voltage becomes zero. As a result, the two switching frequencies at power mode and shunt mode are:

$$f_{power} = \frac{V_i}{4\hat{i}_L L}\left(1-\frac{(N_2V_0/N_1)^2}{V_i^2}\right) \tag{3}$$

$$f_{shunt} = \frac{V_i}{4\hat{i}_L L} \tag{4}$$



(a)

(b)

Fig. 10. Control block diagram: a) hysteresis control in the secondary side b) average current control in the primary side

6 Experimental results

6.1 Circuit input-to-output parasitic capacitance

The circuit input-to-output is measured with instrument Agilent 4294A precision impedance analyzer. The accuracy claimed is ±3% in the measured range. The two input terminals are shorted; and so do the two output terminals. Then the ground planes of the primary side and secondary side are measured with the instrument. Fig. 11 shows the circuit input-to-output impedance magnitude and phase measurement data. Its magnitude slope of -20db/dec and a phase around -90^0 makes it appropriate to be modeled as a capacitor. The measured value of the capacitance is around 10 pF, which is shown in Fig. 12. In short, an extremely low value of circuit input-to-output capacitance is achieved and it is proved to be dominated by the inter-winding parasitic capacitance.

6.2 Converter's transient response

In this section, two key measurement waveforms are presented and discussed. They are the leakage inductor current in the primary side and the output voltage in the secondary side. The measurement of the inductor current is performed with LeCroy AP015 current probe, which has a claimed accuracy of ±1%. In addition, the measurement of the output voltage is done with SI-9000 differential probe with a claimed accuracy of ±2%.

Fig. 13 shows the transient response from power mode to shunt mode, whereas the transient from shunt mode to power mode is shown in Fig. 14. The value of threshold ε is set to 0.5 V. It can be observed that, both the inductor current and the output voltage are well regulated at their desired steady state values, which are 2 A peak and 60 V dc, respectively. The transient of the inductor current from power mode to shunt mode and vice versa finishes within about 30 us and 40 us, respectively. The time needed for the inductor current to settle is due to the dynamic of the average current control scheme described in Fig. 10b. Nevertheless, the transient and steady state are both stable and satisfactory, and the behavior of the circuit matches accurately with the aforementioned circuit analysis.

6.3 Converter's power efficiency

The power measurement is done with instrument PPA5530 precision power analyzer. The accuracy claimed by the manufacturer is ±0.4% in the operation condition under test. The measured efficiency as well as the calculated value at different power output is shown in Fig. 15. At the nominal output of 300 W, the converter operates entirely in its power mode. The switching frequency in the primary side is then the smaller one f_{power}. Therefore, primary switching loss, shunt MOSFET S_5 conduction loss and switching loss are reduced. That's the reason why peak efficiency is attained at the no-

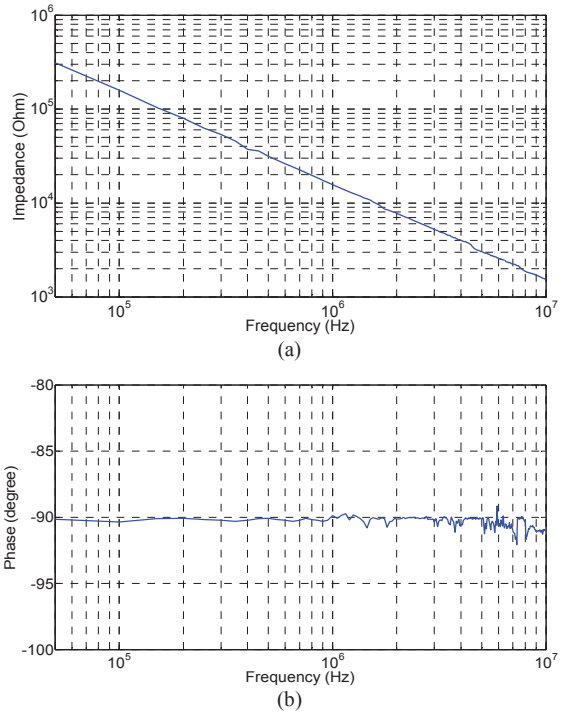


Fig. 11. Circuit input-to-output impedance measurement a) magnitude b) phase

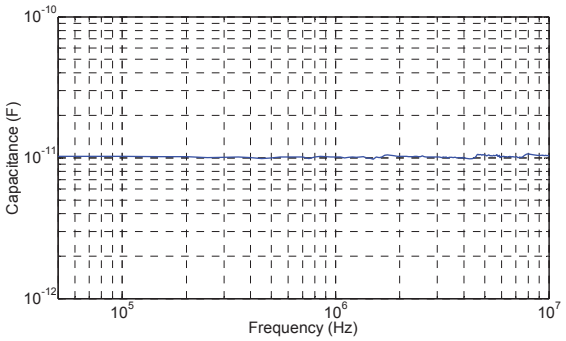


Fig. 12. Circuit input-to-output parasitic capacitance

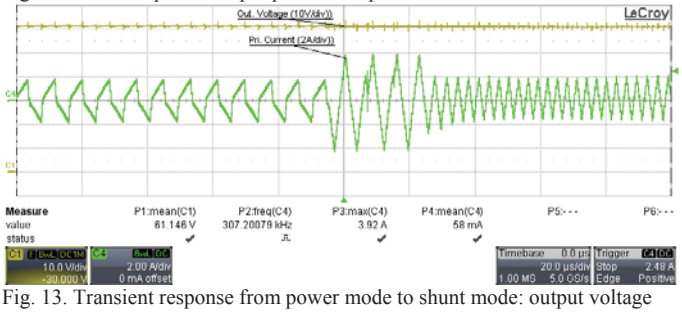


Fig. 13. Transient response from power mode to shunt mode: output voltage (10V/div), inductor current (2A/div), time scale: 20us/div)

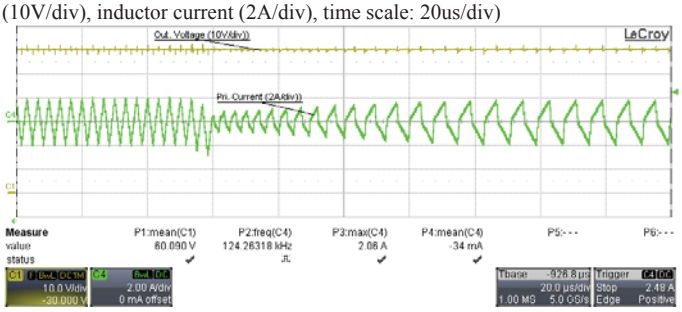


Fig. 14. Transient response from shunt mode to power mode: output voltage (10V/div), inductor current (2A/div), time scale: 20us/div)

minal output power. This value is 92.4 %. As output power reduces, the duration in which the converter operates in shunt mode increases linearly; the loss increases slightly as shown in Fig. 16. Thus, the efficiency drops. Zero efficiency is attained at zero output power when the converter fully operates in its shunt mode. In general, the overall efficiency of the converter is satisfactory particularly in the range of 1/3 of the nominal power to the nominal power. The efficiency in this range is from 77.5 % to 92.4 %.

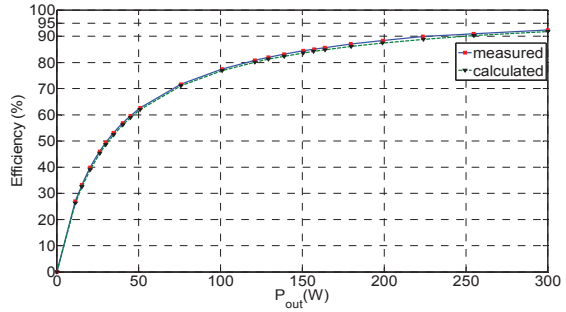


Fig. 15. Converter's power efficiency

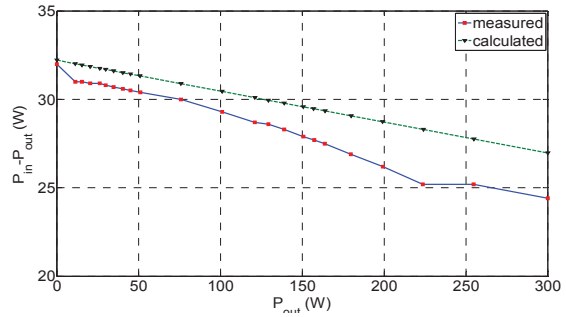


Fig. 16. Converter's power loss

7 Discussion

The several advantages of the developed converter's prototype are as follows. First, the topology and its control allow zero voltage switching at the turn on transitions of the switches (refer to Fig. 9). Second, this topology has higher power (60V/300W) per channel compared to 36V/5W of prior art with a similar topology. This allows the converter to be capable of supplying wider range of load, from 0 to 60 V and up to 5 A. Third, the achieved circuit input-to-output capacitance is extremely low of 10 pF. This is claimed based on observation that existing transformers in the literature, for example, in a 1.2 kW converter was reported to have 1.5 nF inter-winding capacitance [9], and an E-core transformer used in fly-back converter with a power rating of 30 W was reported in [10] to have 34 pF of inter-winding capacitance. Finally, the topology and its control allow zero output voltage and zero output power.

There are two main disadvantages of the topology. First, the MOSFETs at the primary side turn off at their peak currents, which results in higher turn-off loss. Second, the slightly increased loss at lighter load makes the converter's efficiency relatively low at low output power. Solutions might include the use of synchronous rectifier stage in the secondary side to reduce the loss.

8 Conclusion

In this paper, the authors have presented the design of a 300 Watt isolated power supply. The main advantage of the power supply is to have an extremely low inter-winding capacitance in the transformer, making the circuit input-to-output capacitance ultra-low considering its output power. Circuit operation and control have been demonstrated and experimental data are also provided, that proved to match well with expectations. Furthermore, the advantages as well as the disadvantages of the converter are also discussed. In summary, the converter is suitable for a wide range of power supply applications and especially for modular stacking applications, where minimization of the circuit input-to-output capacitance is vital.

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