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Ultrafast Switching Superjunction MOSFETs for Single Phase PFC Applications

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***Abstract*—This paper presents a guide on characterizing state-of-the-art silicon superjunction (SJ) devices in the 600V range for single phase power factor correction (PFC) applications. The characterization procedure is based on a minimally inductive double pulse tester (DPT) with a very low intrusive current measurement method, which enables reaching the switching speed limits of these devices. Due to the intrinsic low and non-linear capacitances in vertical SJ MOSFETs, special attention needs to be paid to the gate drive design to minimize oscillations and limit the maximum dv/dt at turn off. This paper investigates the latest SJ devices in order to set a reference for future research on improvement over silicon (Si) attained with the introduction of wide bandgap devices in single phase PFC applications. The obtained results show that the latest generation of SJ devices set a new benchmark for its wide bandgap competitors.**

I. Introduction

Power semiconductor devices in the 600V range are about to be replaced with new devices based on wide bandgap materials. As shown in Table I, Gallium Nitride (GaN) and Silicon Carbide (SiC) materials present higher electrical field strength and higher electron mobility compared to Silicon (Si). This allows for a reduction in the die size [1]. Moreover, these materials present a lower dielectric constant. This, coupled with the die size reduction, makes it possible to decrease the parasitic capacitances, directly enhancing the device switching performance.

Bulk GaN is an expensive material (100 $€/cm^2$) compared to SiC (10 $€/cm^2$) and Si (0.1 $€/cm^2$) [2]. However, epitaxial growth of GaN on Si substrate, together with higher electron mobility and electrical field strength compared to SiC, has made GaN devices to be an attractive solution in the 600V range.

On the other hand, Si based devices represent a very mature technology. This often overcomes the material disadvantages compared to wide bandgap devices, whose manufacturing processes are still far from reaching the theoretical material limits [3]. This paper investigates the dynamic performance of state-of-the-art Si devices in the 600V range for single phase PFC applications.

TABLE I
WIDE BANDGAP VS. SILICON PROPERTIES

Properties	Si	4H-SiC	GaN
Bandgap E_G [eV]	1.12	3.26	3.39
Critical field E_{crit} [MV/cm]	0.23	2.2	3.3
Thermal conductivity λ [W/cm·K]	1.5	3.8	1.3
Electron mobility μ [cm^2/V·s]	1500	650	2000

II. Superjunction Si MOSFETs

Vertical SJ MOSFETs based on charge balance have set a new benchmark for high voltage Si devices, enabling a reduction of the on resistance and parasitic capacitances [4]. These switches are characterized by very low and highly nonlinear drain to source and drain to gate capacitances. These characteristics will produce extremely fast di/dt and dv/dt at turn off, with close to zero voltage switching (ZVS) operation when a low resistive/inductive gate drive circuit is employed [5], [6]. Under this condition the dv/dt will be determined by the current level, the circuit parasitic inductance and the charge of the MOSFET output capacitance. Exceeding the dv/dt can cause self-destruction due to the activation and thermal runaway of the parasitic bipolar junction transistor (BJT) [7]. This behavior is potentially dangerous in PFC circuits with average input current control, where a grid voltage transient can result in an abnormal inductor current level. The aforementioned issues are taken into account in the switching loss characterization to ensure that the maximum dv/dt ratings of the devices are not exceeded.

III. Double Pulse Tester Design

Printed circuit board (PCB) layout, package selection and other circuit parasitics are critical in modern power electronics [8]. Increasing the switching frequency to enable higher power densities is only possible under careful design of the PCB layout. A four layer PCB is used to reduce the area of the critical ac current loops. Special care has been taken to minimize parasitic inductances in the MOSFET and diode current paths as well as in the driving circuitry. Moreover, as proposed in [6], the capacitive coupling between drain and gate has been minimized to reduce gate oscillations.

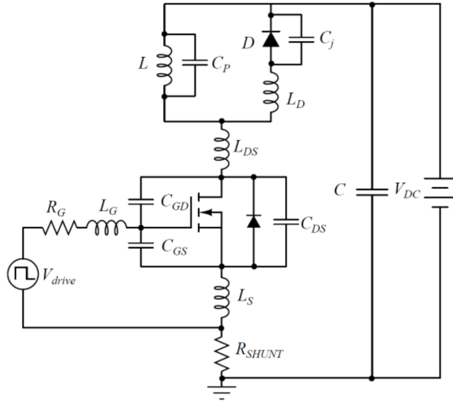

Figure 1. Double pulse tester schematic with components' parasitic capacitances

Fig. 1 shows the DPT schematic with the parasitic components. The PCB is designed to accommodate DPAK (TO-252) and leadless 8x8mm packages for the power MOSFET. DPAK and D^{2}PAK (TO-263) can be accommodated for the freewheeling diode. Flat mounted packages allow cancelling or reducing some of the package parasitic inductances and are preferred in this work.

In order to extract the switching energy, both voltage across and current through the device need to be measured. An overview of different current sensing solutions for integration in PCB or power modules is presented in [9]. One of the most adopted solutions is based on coaxial resistors [10]. State-of-the-art current measurement in high switching speed applications is based on the SDN coaxial current shunt series from T&M Research Products, claiming bandwidths up to 2GHz. This solution has been previously adopted for SiC and GaN characterization, as presented in [11] and [12]. However, due to the large parasitic inductance inserted in the loop by this device (2.2 nH [11]), the flat distributed shunt approach presented in [13] and [14] is used instead. This current shunt consists of an array of paralleled surface mount resistors (SMD). A pick-up wire placed as shown in Fig. 2, reduces the inductive coupling and increases the bandwidth of the measurement. However, as presented in [14], this shunt structure can present current distribution problems, limiting the accuracy and bandwidth of the current measurement. In order to overcome this problem, a high shunt resistance value is selected, which also reduces the inductive effect in the current measurement. The designed shunt structure is composed by 10x10Ω thin film resistors (0603 package) mounted in parallel. Since the resistive element in the resistor package is placed on top, these components are mounted upside down to reduce the distance from the resistive element to the PCB current return path. Fig.3 shows a Finite Element Analysis (FEA) of the current measurement structure to evaluate its bandwidth. The analysis shows that the bandwidth of the current measurement is well above B_ω= 500MHz. As presented in [15] and shown in Eq. (1), the obtained bandwidth makes it possible to measure signals with a rise time down to t_r = 0.7ns.

$$t_r = \frac{0.35}{B_\omega} \quad (1)$$

Fig. 4 shows the implemented DPT prototype with the integrated current shunt. The MOSFET driver used in this prototype is a 9A FAN3122 from Fairchild Semiconductor. Fig. 5 shows the designed low capacitive inductor. This component is implemented using two K6527E040 cores from Magnetics in a single layer configuration with a total magnetizing inductance of 213μH and a parasitic capacitance of 2.9pF.

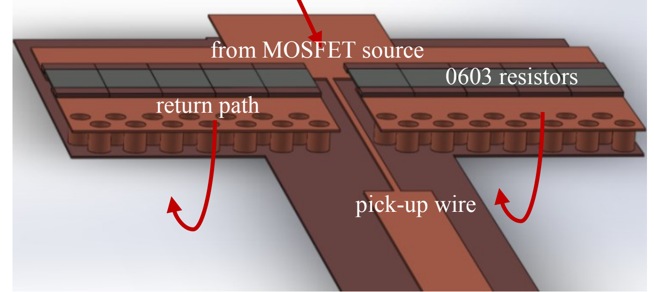

Figure 2. Integrated flat shunt 3D model used for FEA simulation

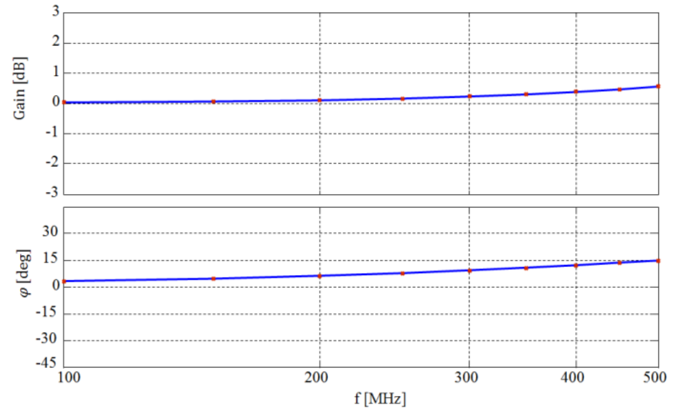

Figure 3. FEA current measurement transfer function

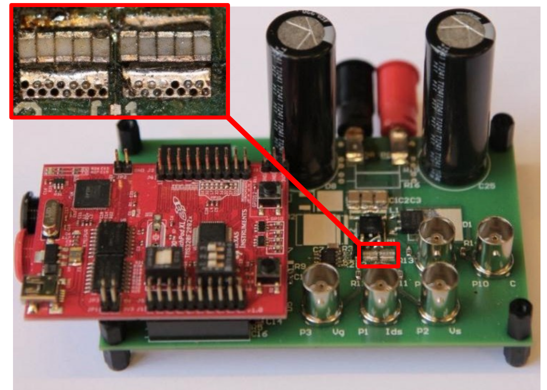

Figure 4. Double pulse tester prototype with integrated current shunt

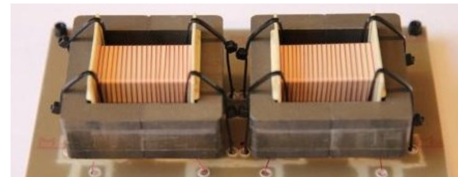

Figure 5. Low capacitance inductor prototype

IV. CHARACTERIZATION RESULTS

In this work, five SJ devices and six SiC diodes with different die sizes in the 600V range have been selected. The MOSFETs have been chosen based on their input gate charge and on resistance. Three of the devices (Fairchild and STMicroelectronics) are mounted in DPAK and the other two (Infineon C7) in a flat 8x8mm package with kelvin connection for the gate drive source. Table II shows the manufacturer specified gate charges and internal gate resistances together with the measured on resistance at 25°C. The SiC diodes are selected from two different manufacturers. The smaller die sizes are CREE C3D0X060E in 2, 3 and 4A versions, while the larger die sizes are Infineon IDDXXSG60C in 6, 8 and 10A versions. Fig. 6 presents the measured diodes' I-V curves at 25 °C.

The two smaller SJ devices (FCD9N60NTM and STD13NM60N) are characterized with the small CREE SiC diodes and the large die sizes with the Infineon SiC diodes.

The DPT prototype is based on the digital signal processor (DSP) evaluation platform C2000™ Piccolo Launchpad. An automatic characterization procedure has been developed. The switching waveforms are automatically saved on each trigger event and post processed using MATLAB. Switching energy, voltage and current derivatives for different inductor current levels are extracted. Fig. 7 and Fig. 8 show the DPT turn on and turn off waveforms with a 5 ns time scale. Fig. 9 and Fig. 10 show the post processed voltage and current waveforms for different inductor current levels.

TABLE II
CHARACTERIZED SUPERJUNCTION DEVICES

Device	V_{DSS} [V]	R_{DS} @ 25°C [mΩ]	Q_G [nC]	R_g [Ω]
FCD9N60NTM	600	391	18 @ V_{GS} = 10V & V_{DS} = 380V	-
STD13NM60N	600	348	27 @ V_{GS} =10V & V_{DS} = 480 V	4.7
STD18N65M5	650	182	31 @ V_{GS} =10V & V_{DS} = 520V	3
65R230C7	650	231	20 @ V_{GS} =10V & V_{DS} =400V	1
65R130C7	650	118	35 @ V_{GS}= 10V & V_{DS} = 400V	1

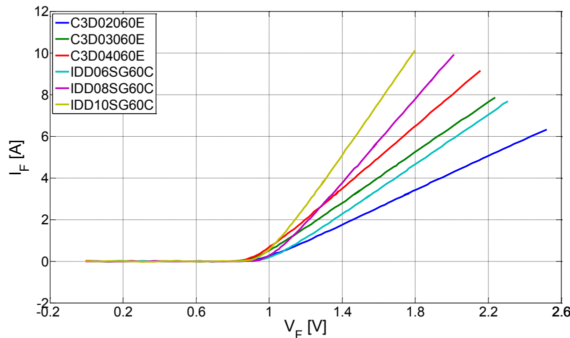

Figure 6. Diode V_F - I_F curves @ 25 °C

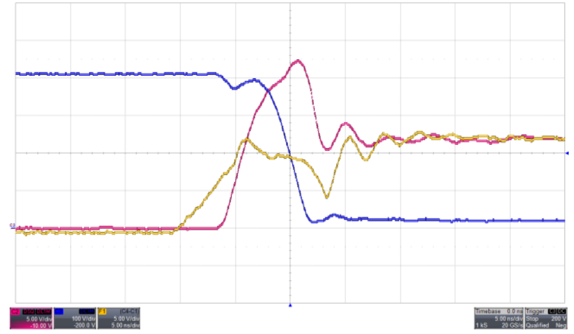
Figure 7. FCD9N60NTM and IDD10SG60C turn on waveforms. Light brown V_{GS} (5V/div), red I_D (5A/div), blue V_{DS} (100V/div). Time scale (5ns/div)

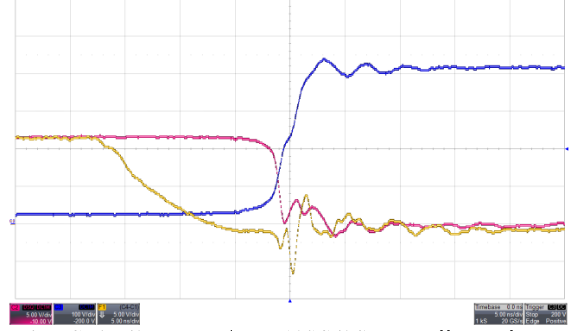
Figure 8. FCD9N60NTM and IDD10SG60C turn off waveforms. Light brown V_{GS} (5V/div), red I_D (5A/div), blue V_{DS} (100V/div). Time scale (5ns/div)

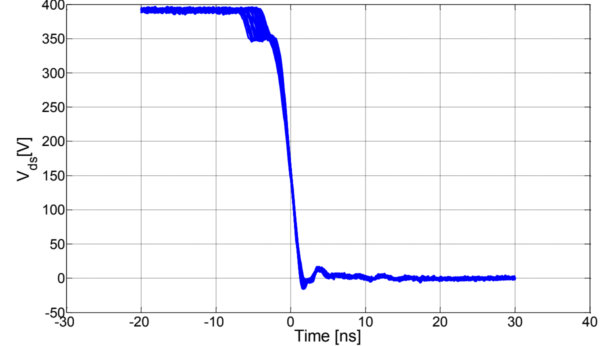

Figure 9. MOSFET drain to source voltage waveform during turn on for different inductor current levels

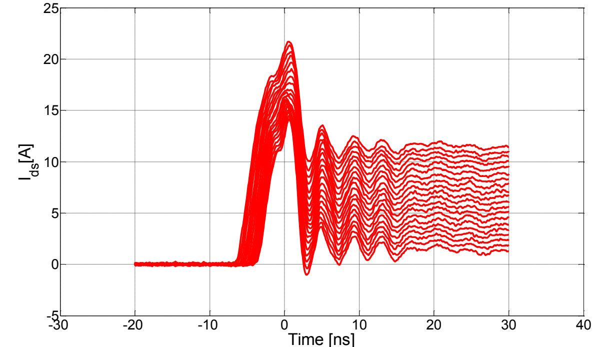

Figure 10. MOSFET current waveform during turn on for different inductor current levels

The switching waveforms are measured for different current levels, gate resistances and devices' junction temperatures. The junction temperature is controlled by a hot plate with temperature control based on thermocouple feedback. In this way it is possible to create a 4D space

solution for the devices' turn on and turn off energy loss and V_{DS} voltage derivatives. In this research, the effect of the gate resistance on the maximum dv/dt at the turn off of the MOSFET is considered. As presented in [6], due to the large MOSFET output capacitance at low voltage levels, SJ devices will exhibit a quasi ZVS (QZVS) behavior when very low gate resistance is used in the drive circuitry. Under these conditions, the current will be removed from the MOSFET channel under almost zero voltage conditions and the gate drive will not be in control of the device's dv/dt (now limited by the inductor current level and the device output capacitance value).

SJ manufacturers often specify the MOSFET dv/dt ruggedness rating related to BJT parasitic activation and gate activation by the C_{GD} charge at the MOSFET turn off. Moreover, as shown in [16], degraded blocking voltage capabilities were observed in the first generations of SiC diodes. However, as presented in [17], [18] and [19], these issues have been solved and reliability reports show safe operation over 100V/ns. Therefore, in this characterization the gate resistance at turn off will be adjusted to limit the maximum dv/dt to 100V/ns, regardless of the inductor current level. As shown in Fig. 11, a QZVS behavior is observed for 0Ω gate resistance with a switching energy loss corresponding to the MOSFET's output capacitance charge.

Fig. 12 and Fig. 13 show the instantaneous di/dt and dv/dt slope at turn off. When the gate resistance is equal to zero, it can be seen that the dv/dt only depends on the inductor current level. However, when the gate resistance is increased, the dv/dt is limited by the gate turn off speed. Fig. 14 shows the negative dv/dt slope dependence with the junction temperature. Fig. 15 shows a contour plot of the dv/dt slope vs. inductor current and gate resistance. Thus, the minimum gate resistance that limits the dv/dt can be obtained. Afterwards, the switching energy loss at turn off can be calculated by performing a 2D interpolation of the switching energy surface as a function of the gate resistance and inductor current level as shown in Fig. 16.

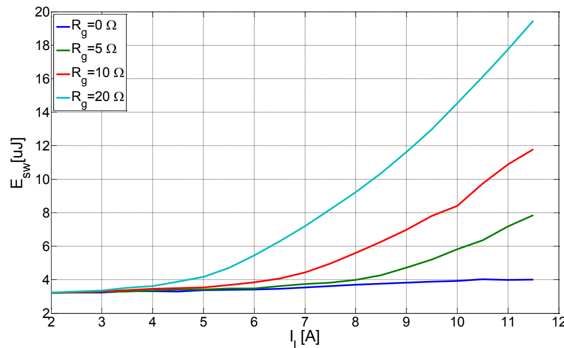

Figure 11. FCD9N60NTM and C3D02060E turn off energy loss vs. inductor current level for different gate resistances

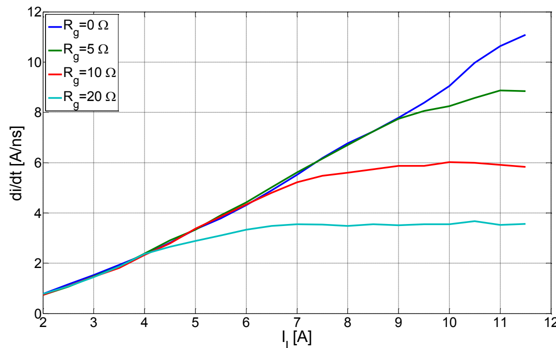

Figure 12. FCD9N60NTM and C3D02060E maximum instantaneous di/dt at turn off vs. inductor current level for different gate resistances

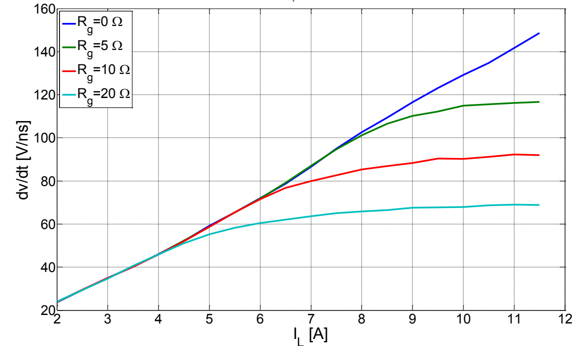

Figure 13. FCD9N60NTM and C3D02060E dv/dt slope at turn off vs. inductor current level for different gate resistances

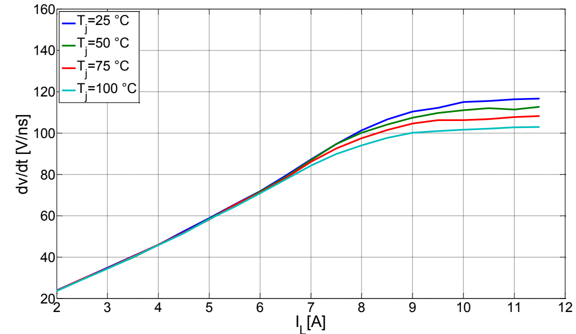

Figure 14. FCD9N60NTM and C3D02060E dv/dt slope at turn off vs. inductor current level for different junction temperatures

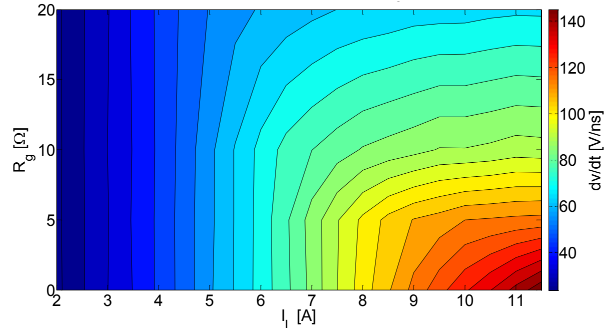

Figure 15. FCD9N60NTM and C3D02060E dv/dt at turn off vs. inductor current level as a function of the gate resistance

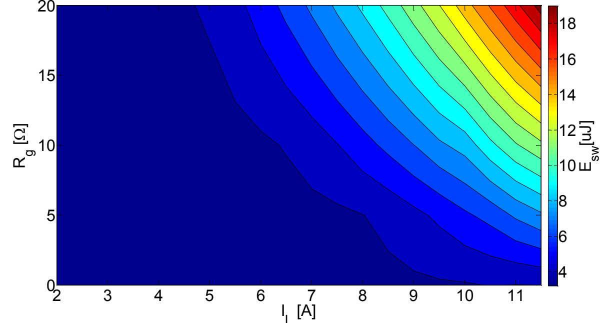

Figure 16. FCD9N60NTM and C3D02060E turn off energy loss vs. inductor current level as a function of the gate resistance

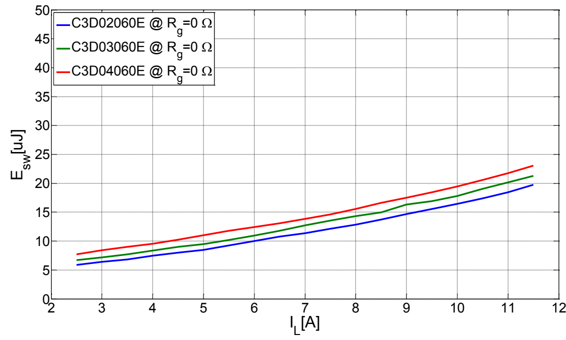

Figure 17. FCD9N60NTM turn on energy loss vs. inductor current level

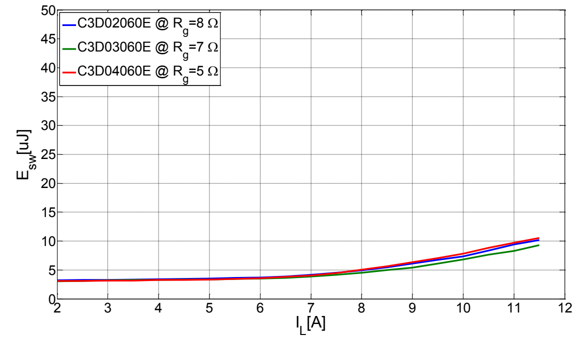

Figure 18. FCD9N60NTM turn off energy loss vs. inductor current level

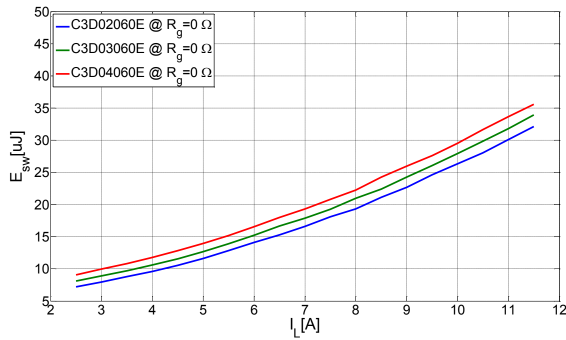

Figure 19. STD13NM60N turn on energy loss vs. inductor current level

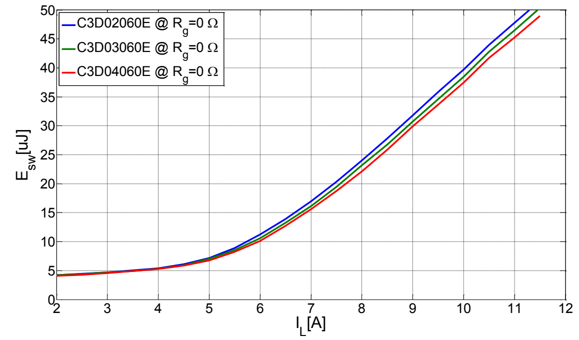

Figure 20. STD13NM60N turn off energy loss vs. inductor current level

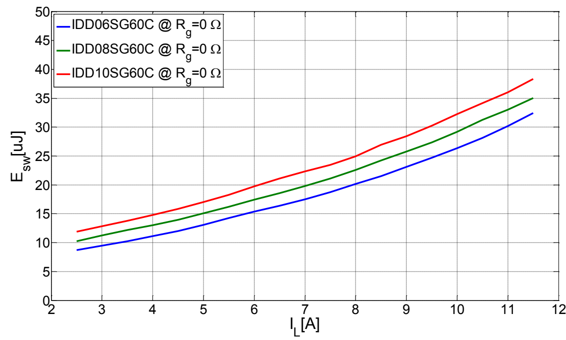

Figure 21. STD18N65M5 turn on energy loss vs. inductor current level

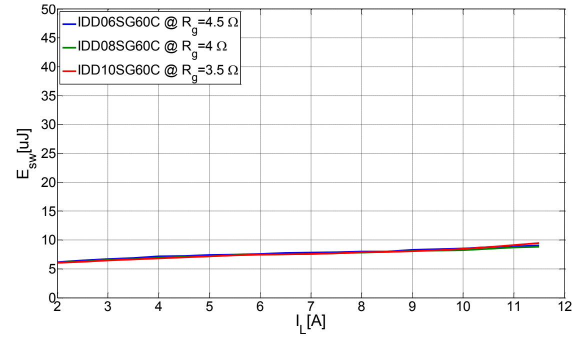

Figure 22. STD18N65M5 turn off energy loss vs. inductor current level

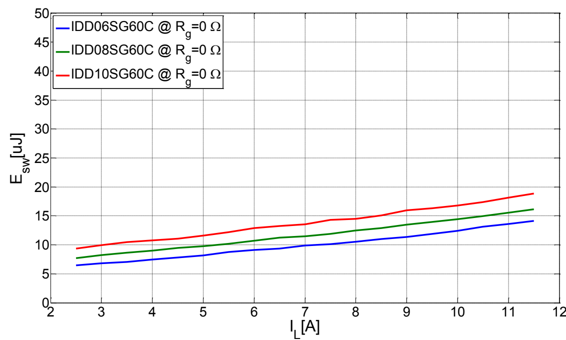

Figure 23. 65R230C7 turn on energy loss vs. inductor current level

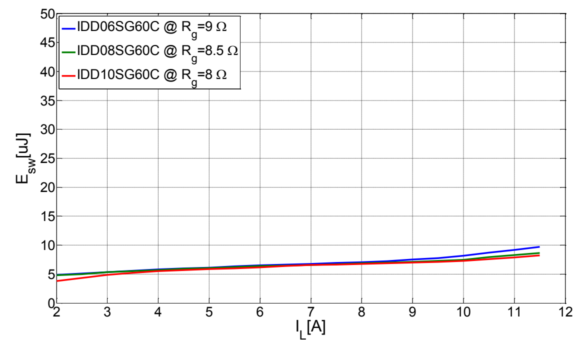

Figure 24. 65R230C7 turn off energy loss vs. inductor current level

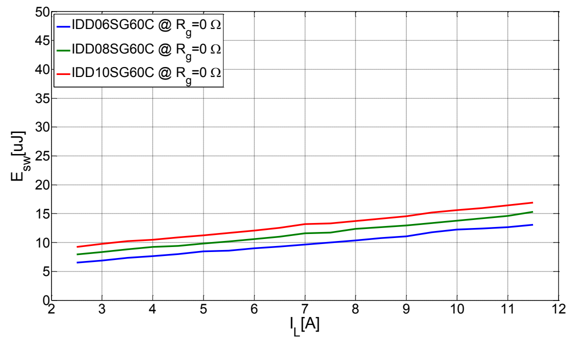

Figure 25. 65R130C7 turn on energy loss vs. inductor current level

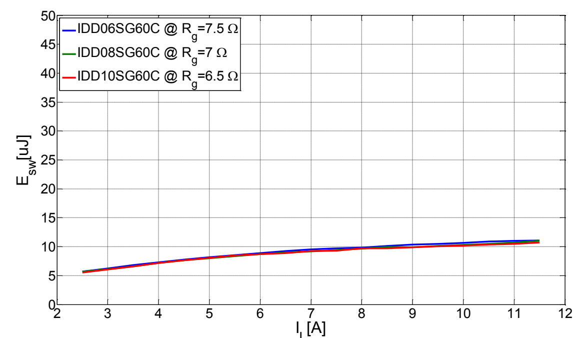

Figure 26. 65R130C7 turn off energy loss vs. inductor current level

Fig. 17 to Fig. 26 show the characterization results for the different analyzed SJ and SiC devices at a junction temperature of 25°C. The turn on loss energy curves are obtained at 0Ω gate resistance. The turn off loss corresponds to the calculated-interpolated gate resistance values in order not to exceed 100V/ns at turn off.

The difference in the diode junction capacitance charge can be observed in the turn on energy loss of the different MOSFETs, where the energy difference between the different diodes measurements is constant and independent of the current level.

From Fig. 20 it can be observed that MOSFET STD13NM60N is turned off with 0Ω gate resistance. This is due to the large internal gate resistance of the device (4.7Ω), which limits the maximum dv/dt to 35V/ns and has a negative effect on the switching loss.

The results obtained for the smallest device (FCD9N60NTM) show very low energy loss at both turn on and turn off. More remarkable are the results from the C7 devices from Infineon. It can be observed that the 65R130C7 presents lower turn on losses compared to the smaller 65230C7 device. In fact, attending to the results from the device 65R130C7, the obtained turn on losses for a 130mΩ are quite remarkable. This device in combination with the 6A diode from Infineon (IDD06SG60C Q_C =8nC at 400V) presents a lower turn on loss than the Fairchild device with the 4A diode from Cree (C3D04060E Q_C =8.5nC at 600V). This result can be compared with the results obtained in [20] corresponding to a 600V GaN High-Electron-Mobility-Transistor (HEMT) in cascode configuration with 150mΩ on resistance. In [20] the device switching energy is measured at dc voltage of 240V and a current range from 0 to 10A. The device measured in this work, 65R130C7 presents similar on resistance than the GaN device, but much smaller switching energy losses.

V. Discussion

The QZVS turn off capabilities of SJ devices need to be investigated as a very interesting feature for high frequency boundary conduction mode (BCM) operation in PFC applications. BCM makes possible to operate the switch under zero current switching (ZCS) conditions at turn on. If this operation is combined with a SJ device with 0Ω gate resistance and operated under QZVS conditions, the turn off energy loss will be independent of the current level.

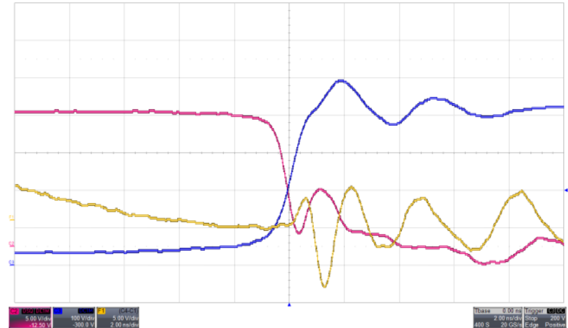
Figure 27. Turn off event FCD9N60NTM and C3D032060E. Light brown V_{GS} (5V/div), red I_D (5A/div), blue V_{DS} (100V/div). Time scale (2ns/div)

Is the author's experience that is possible to exceed the dv/dt manufacturer specified limits if a very low impedance gate drive is implemented to avoid gate activation due to the charge of the parasitic C_{GD} capacitance.

Fig. 27 shows a turn off event measured for FCD9N60NTM with CD032060E. In this experiment a 9A Zetex 3002 totem pole 9A driver was located in close proximity to the gate and source terminals to reduce the gate drive impedance. The inductor current level was increased until an absolute maximum dv/dt was found. The figure shows a drain to source voltage with a slope of more than 250V/ns on a 100V/ns rated device. (It is important to notice that this measurement may not represent the real waveforms due to the 500MHz bandwidth limitation of the oscilloscope voltage probes).

A last test was performed on FCD9N60NTM and CD032060E with a controlled junction temperature of 100°C. More than 10000 switch off events at 200V/ns dv/dt were measured without failure of the devices. These results are not concluding and more experiments need to be performed to clarify the device reliability when the maximum dv/dt is exceeded.

VI. Conclusion

This work evaluates state-of-the-art Si switches in the 600V range for single phase PFC applications setting a performance reference for the new wide bandgap materials. Several issues have to be addressed to ensure optimal switching performance. The DPT parasitic inductances and some of the packages' inductances are minimized by using a four layer

PCB design to minimize the ac current loops. Moreover a low intrusive current measurement method is used to minimize the insertion of parasitic inductances that would degrade the switching performance of the characterized devices.

The devices switching waveforms are saved and post processed in MATLAB to create a 4D map that can be used to calculate the switching energy and voltage derivatives by performing a curve fitting or a linear interpolation of the 4D space solution.

This work shows the obtained results for five SJ devices in combination with six different SiC diodes where dv/dt limitation at turn off has been taken into account to avoid parasitic BJT activation at turn off. The obtained results show that the latest SJ devices present very low switching energy loss together with a very low on resistance that makes these devices compete with some of the latest 600V GaN HEMT transistors.

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