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DESIGN OF THE ALAMOUTI SCHEME FOR A MIMO RECEIVER AND ITS IMPLEMENTATION ON AN FPGA

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Abstract: This paper analyses the Alamouti scheme for different antenna configurations and different modulation types, namely BPSK, QPSK and QAM. All configurations were modeled and simulated in MATLAB. A MIMO receiver for a 2×1 antenna configuration and BPSK modulation was implemented in a FPGA. The FPGA results indicate that the Alamouti scheme is a good design option for hardware implementation of a MIMO receiver. The receiver uses only about 10% of the resources of a medium-sized FPGA and achieves almost 300 Msymbols per second.

1 Introduction

Currently, there is an increasing offer of services based on wireless communications, which require high speeds to ensure the quality of service without compromising the transmission power of the system or the bandwidth. MIMO (Multiple Input Multiple Output) technology offers increased capacity to these systems without requiring an increase in bandwidth or transmitted power. This technology is based on the channel space exploration using multiple antennas at both ends of the communications system, offering various gains: beam forming, array gain, spatial diversity gain, spatial multiplexing gain and interference reduction.

The spatial diversity technique is the most efficient and effective to combat the effects of multipath fading, achieving in this way an improved system reliability. Spatial diversity gain arises from the use of space-time coding of the transmitted/received signals, where time, which is the natural dimension of digital communication systems, is complemented with the spatial dimension, from the use of multiple antennas on the part of the system. There are several space-time encoding schemes [2], as for example: Space-Time Block Codes (STBC), Space-Time Trellis Codes (STTC), Space-Time Turbo Trellis Codes (STTTC) and Layered Space-Time Codes (LSTC). In STBC it is possible to reach a maximum order of spatial diversity (equals the number of transmit antennas, M_T) using a simple and linear processing on the decoding. A well-known type of STBC scheme is the Alamouti Scheme [1].

The paper is organized as follows. In section 2, the Alamouti scheme is briefly described. In section 3, we describe the implementation of a MIMO receiver based on the Alamouti scheme on an FPGA. Section 4 reports the results of the implementation in terms of area and performance. Finally, section 5 concludes the paper and proposes some future improvements.

2 Alamouti Scheme

The original Alamouti scheme [1] is a transmit diversity technique using two transmitting antennas and one receiving antenna, and can be divided into three parts: (1) the encoding and transmission sequence of information symbols at the transmitter, where the bits of information are encoded into symbols in the domains of space and time and then transmitted, one for each transmit antenna; (2) the scheme for combining the received signals at the receiver, which prepares the symbols for the maximum likelihood detector and (3) the decision rule for maximum likelihood detection for the sent symbols.

Figure 1 shows the Alamouti scheme for the 2×1 antenna configuration.

In this transmitting scheme, two signals are simultaneously transmitted from both antennas (antenna one and two) in two steps. In the first step, signals s_1 and s_2 are transmitted from antennas one and two, respectively. Then, in the second step antenna one transmits $-s2^*$ and antenna two transmits s_1^* (the mark * stands for the conjugate of the symbol) (see figure 1).

At the receiver side, two signals are received, r_0 and r_1, from antenna one and antenna two, respectivelly. These signals are expressed as:

$$r_0 = h_0 S_0 + h_1 S_1 + n_0 \quad (1)$$
$$r_1 = -h_0 S_1^* + h_1 S_0^* + n_1 \quad (2)$$

where h_0 and h_1 are the channel responses between each of the transmiting antenna and the receiving antenna. n_0 and n_1 represent complex noise and interference of the channel.

Estimations of the sent signals, $\widetilde{s_0}$ and $\widetilde{s_1}$, are then determined from the received signals and also using the channel responses, h_0 and h_1, as follows:

$$\widetilde{s_0} = (|h_0|^2 + |h_1|^2) S_0 + h_0^* n_0 + h_1^* n_1 \quad (3)$$
$$\widetilde{s_1} = (|h_0|^2 + |h_1|^2) S_1 - h_0 n_1^* + h_1^* n_0 \quad (4)$$

This operation is implemented at the receiver by a block designated *combiner*.

Finally, the sent bits are obtained from the received symbols using a demodulator (the demodulator block in figure 1).

The Alamouti scheme can be generalized to the case of two transmitting antennas and N_R receiving antennas, achieving in this way a diversity gain of $2 \times N_R$. For example, in the 2×2 antenna configuration the received signals, r_0, r_1, r_2 and r_3, are expressed as:

$$r_0 = h_0 S_0 + h_1 S_1 + n_0 \quad (5)$$
$$r_1 = -h_0 S_1^* + h_1 S_0^* + n_1 \quad (6)$$
$$r_2 = h_2 S_0 + h_3 S_1 + n_2 \quad (7)$$
$$r_3 = -h_2 S_1^* + h_3 S_0^* + n_3 \quad (8)$$

where h_0, h_1, h_2 and h_3 are the channel responses between each of the transmiting antennas and receiving antennas.

The combiner would then calculate an estimative of the sent symbols from these signals as follows:

$$\begin{aligned} \widetilde{s_0} &= (|h_0|^2 + |h_1|^2 + |h_2|^2 + |h_3|^2) S_0 \\ &\quad + h_0^* n_0 + h_1 n_1^* + h_2^* n_2 + h_3 n_3^* \\ \widetilde{s_1} &= (|h_0|^2 + |h_1|^2 + |h_2|^2 + |h_3|^2) S_1 \\ &\quad - h_0 n_1^* + h_1^* n_0 - h_2 n_3^* + h_3^* n_2 \end{aligned} \quad (9)$$

The Alamouti scheme for different antenna configurations was implemented in MATLAB in order to validate their theoretical concepts. Figure 2 presents the Alamouti scheme for multiple antenna configurations for BPSK modulation.

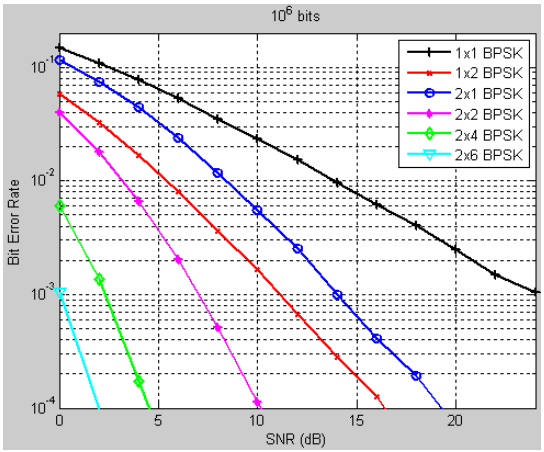

Figure 2: Alamouti scheme for various antenna configurations using BPSK.

An important aspect is the difference in power between the configuration of one transmitting antenna and two receiving antennas (1×2) to two transmitting antennas and one receiving antenna (2×1). Considering that the transmitted power is normalized to 1, the power transmitted by each transmit antenna in the case of the 2×1 is half the power transmitted by the antenna of the 1×2 case. This means that there is then a 3 dB difference between the 1×2 and 2×1 configurations. The increase in the number of receiving antennas also makes the order of diversity increases, $2 \times N_R$.

The Alamouti scheme was also implemented with modulations QPSK and 16 QAM. In Figure 3 it can

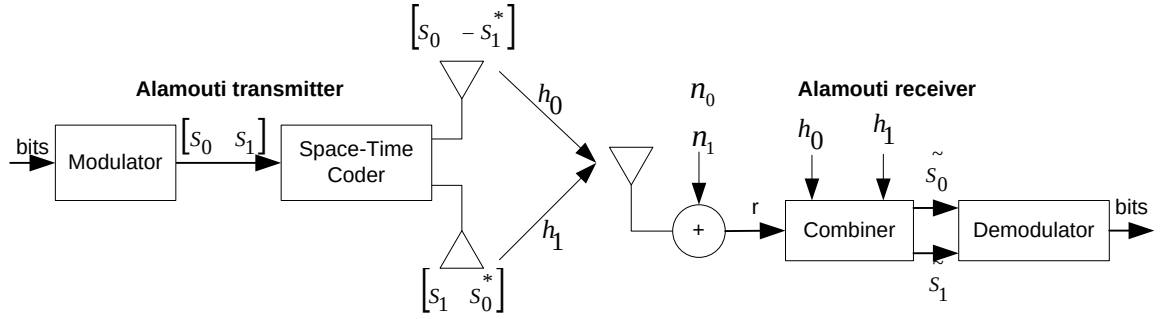

Figure 1: Alamouti scheme.

be seen that modulations with higher levels require a better SNR ratio, that is, for the same BER, a higher modulation has a higher SNR.

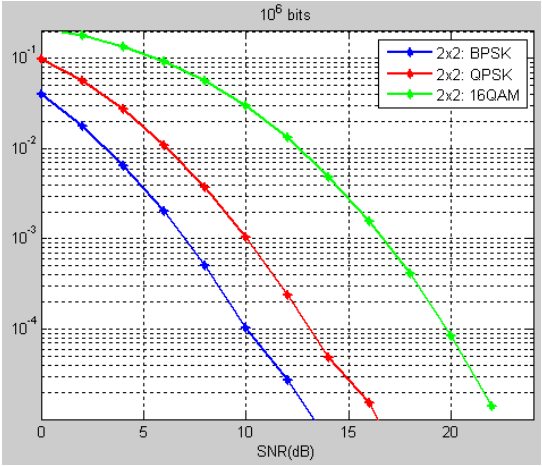

Figure 3: Alamouti scheme with BPSK, QPSK and QAM modulations.

3 FPGA receiver for a 2×1 antenna configuration with BPSK

In this section we desribe the FPGA implementation of the Alamouti receiver for a 2×1 antenna configuration and BPSK modulation (see figure 4).

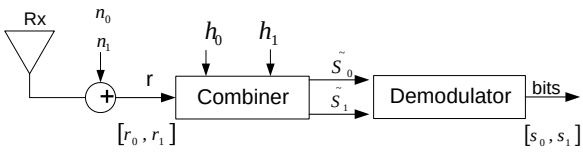

Figure 4: Alamouti receiver scheme.

From section 2 we know that the received signals in figure 4 are given by

$$r_0 = h_0 S_0 + h_1 S_1 + n_0 \quad (10)$$
$$r_1 = -h_0 S_1^* + h_1 S_0^* + n_1 \quad (11)$$

and the estimated symbols at the receiver are given by

$$\widetilde{s_0} = (|h_0|^2 + |h_1|^2) S_0 + h_0^* n_0 + h_1^* n_1 \quad (12)$$
$$\widetilde{s_1} = (|h_0|^2 + |h_1|^2) S_1 - h_0 n_1^* + h_1^* n_0 \quad (13)$$

From equations (3) and (4), we see that $\widetilde{s_0}$ and $\widetilde{s_1}$ are the result of mathematical operations between complex numbers. The complex multiplication between two complex numbers, x and y, is given by:

$$x \times y = (a + bi) \times (c + di) =$$
$$(a \times c - b \times d) + (a \times d + b \times c)i$$

Based on equation (5) the block diagram of the complex multiplier is given in figure 5.

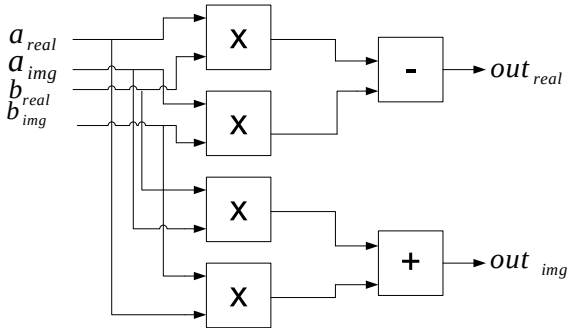

Figure 5: Block diagram of a complex multiplier.

This complex multiplier will serve as the basis for the construction of the combiner block (see figure 6).

To recover the original transmitted bits from $\widetilde{s_0}$ and $\widetilde{s_1}$ is then necessary to carry out the demodulation of the received symbols. For the demodulation method we have used hard decision. Using the hard decision process to perform the BPSK demodulation, it is enough to consider only the most significant bit (MSB) of the real part of the complex symbol, that is, the signal bit. If the real part of the estimated symbol is positive, then the most significant bit of the symbol is a '0'. On the other side, if the real part of the estimated symbol is negative, then the most significant

Size	LUT	DSP	Freq	Throughput
16 bits	2058 (6%)	8 (4%)	29 MHz	29 Msymbols/s
23 bits	2986 (9%)	8 (4%)	24 MHz	24 Msymbols/s

Table 1: FPGA results for a 2×1 antenna configuration with BPSK without pipeline.

Size	LUT	DSP	Latency	Freq	Throughput
16 bits	2268 (7%)	8(4%)	11	285 MHz	285 Msymbols/s
23 bits	3230 (10%)	8(4%)	17	263 MHz	263 Msymbols/s

Table 2: FPGA results for a 2×1 antenna configuration with BPSK with pipeline.

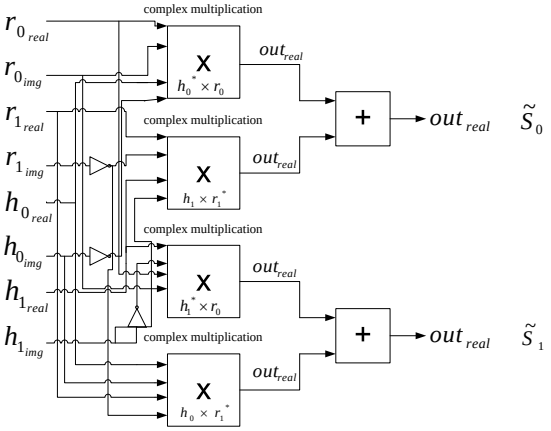

Figure 6: Block diagram of the Alamouti receber using BPSK modulation.

bit is a '1'. Therefore, if the MSB is '0', then the recovered bit is '0', otherwise is '1'.

In this implementation, all numbers were represented in two different custom floating-point formats: 16 bits (5 bits for the exponent and 11 bits for the mantissa) and 23 bits (6 bits for the exponent and 17 bits for the mantissa).

4 Results

The system was implemented in a Virtex4-SX35 FPGA with speed grade -12. Two architectural implementatiosn were considered: with and without pipeline (see tables 1 and 2).

The results show that the receiver uses less than 10% of the available resources of a medium sized FPGA. Wihout pipeline the receiver decodes upto 29 Msymbols per second. The pipelined version increases the decode ratio to about 10 times more with only a marginal increase in the utilized resources.

5 Conclusion

In this work we have modulated and simulated in MATLAB the Alamouti scheme for various antenna configurations and different modulations. The results are as expected and show the advantages of using this STBC scheme. The good throughputs achieved when implemented in an FPGA even using floating point arithmetic and multiple antennas show that the method is a good design option for a MIMO implementation using an STBC scheme. In the future, we will do a detailed study about the precision of the used arithmetic in order to improve the area and throughput of the hardware implementation.

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