Journal of Engineering Science and Technology
Vol. 13, No. 1 (2018) 265 - 279

A GRAPHICAL APPROACH TO DESIGN AND OPTIMIZATION OF MOS AMPLIFIER

PAROMITA BHATTCHARJEE, ABIR J. MONDAL*, ALAK MAJUMDER

Department of Electronics & Computer Engineering, National Institute of Technology Arunachal Pradesh, Yupia, 791112, Papumpare, Arunachal Pradesh, India
*Corresponding Author: abir.ece@nitap.in

Abstract

The component values and transistor dimensions of a single stage amplifier are the only designable parameters which can be adjusted to achieve optimum performance. The resulting parameters can be set to form an objective function and constraint equations to graphically shape a feasible region which is a polytope. The required optimum value of design parameters is then derived by navigating over each of the corner and internal points of the polytope shaped. Accordingly, the amplifier design problem is conveyed as an optimization problem termed Non Linear Programming (NLP) enlisting decipherable global optimization methods. The present technique yields an automatic analysis of single stage amplifiers inferred from the specification values. In this paper, the proposed technique is first used to express the design problem of a particular amplifier circuit as NLP and then applied to a varied amplifier designs. Comparison of result with existing work implies a superior outcome with respect to achievement of required small signal gain (Av) and unity gain frequency (*UGF*). The optimal trade-off curves related to performance metrics such as Av, power and *UGF* are derived in order to observe the corresponding dependencies.

Keywords: Non Linear Programming, Simplex Method, Amplifier Circuits, Small Signal Gain, Slew Rate, Unity Gain Frequency.

1. Introduction

Design of analog circuits is crucial owing to its contribution to mixed mode integrated circuit (IC). Though in mixed mode IC, maximum functionality is implemented through digital circuits, design of analog part remains as the bottleneck because it takes the maximum of effort and design time.

Nomenclatures

Av	Voltage gain
C_{gd}	Gate to drain junction capacitance, $F(CV^{-1})$
C_{gs}	Gate to source junction capacitance, $F(CV^{-1})$
C_L	Load capacitance, $F(CV^{-1})$
f_T	Unity gain frequency, $Hz(s^{-1})$
GBW	Gain bandwidth product, $Hz(s^{-1})$
g_m	Trans-conductance, AV^{-1}
g_{mb}	Body conductance, AV^{-1}
i_d	Inversion level
I_d	Drain current, A
I_{in}	Input current, A
I_{out}	Output current, A
K	Boltzmann's constant, JK^{-1}
L	Channel length, m
L_{min}	Minimum allowed channel length, m
L_{max}	Maximum allowed channel length, m
P_{max}	Maximum allowed power dissipation, $W(Js^{-1})$
R_d	Drain resistance, ohm
r_o	Drain output resistance, ohm
R_S	Source resistance, ohm
SR	Slew rate, AF^{-1}
T	Absolute temperature, K
UGF	Unity gain frequency, $Hz(s^{-1})$
V_1	Gate to source voltage, V
V_b	Bias voltage, V
V_{DD}	Power supply, V
V_{in}	Input voltage, V
V_n	Thermal noise voltage, V
V_{out}	Output voltage, V
V_{ov}	Overdrive voltage, V
V_{th}	Threshold voltage, V
W	Channel width, m
W_{min}	Minimum allowed channel width, m
W_{max}	Maximum allowed channel width, m
W/L	Aspect ratio

Greek Symbols

ω	Angular frequency, rad s^{-1}

Abbreviations

CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
DC	Direct Current
GP	Geometric Programming

IC	Integrated Circuits
LT	Linear Technology
MATLAB	Matrix Laboratory
MOS	Metal Oxide Semiconductor
NLP	Non-Linear Programming
TSMC	Taiwan Semiconductor Manufacturing Company

Few of the analog circuits used in electronics system are biasing circuits, amplifiers, filters, converters, etc. In particular, single stage amplifiers constitute a vital part of analog system. An operational amplifier (op-amp) is realized by cascading the single stage amplifiers with differential amplifiers. They even act as buffer at the output of an op-amp for impedance matching. The working of a single stage amplifier is ascertained by factors such as small signal gain (Av), slew rate (*SR)*, unity gain frequency (*UGF)*, power dissipation *(P_{max})* and noise. Estimating the optimal dimension of a transistor and component values for an explicit design implicates a trade-off among the above stated performance measures. Also, the operation of the components has a non-linear dependence on the voltage across its nodes and current flowing through it. In addition to these complications, the circuit conditions and performance specifications differ from system to system. Thus a global design technique is highly solicited for design optimization and authentication of analog circuits and to distinguish the non-linear stochastic nature of the analog design space. Evidently the optimization problem called non-linear programming (NLP) presented in this work defends it.

The present method is firstly detailed for the problem formulation of common gate (CG) architecture and then applied for varied amplifier architectures. After the optimum design values are obtained from the methodical approach, simulation of the design of CG amplifier circuit is done using Taiwan Semiconductor Manufacturing Company (TSMC) 180nm technology in Linear Technology (LT) spice. For a given design specification, the performance metrics obtained in both cases outline the relevancy of the proposed method.

Section 2 discusses the various aspects related to existing approaches and techniques in the field of analog circuit designing. Section 3 introduces NLP with relevance to analog design space. The process of transistor modelling has been analysed in Section 4, while the detailed problem formulation for CG amplifier has been given in Section 5. Section 6 shows the final constrained optimization problem, followed by analysis of results in Section 7. The conclusions are drawn in Section 8.

2. Literature Survey

It has been observed that biasing metal oxide semiconductor (MOS) circuits in moderate inversion region can make it usable in applications requiring low-level of power and higher speed because a realistic power-speed compromise can be reached. Silveira *et al*. proposed a method which can be used for an operation of MOS circuits in the whole inversion region [1]. The method takes benefit of the relation between the ratio of transconductance over drain current, g_m/I_d and drain current over aspect ratio, $I_d/(W/L)$.

Cunha et al. [2, 3] suggested a design method based on g_m/I_d, for MOS operating in saturation [4]. The drain current, I_d and aspect ratio, W/L of the amplifier were expressed in terms of capacitive load, C_L gain bandwidth product, *GBW* and

inversion level, i_d. With an assumed value of i_d, I_d and W/L values are chosen for adequate area and power specifications. Difficulty is with the selection of proper value of i_d and authentication of gain. Farag [5] fixed the first issue by presenting a method accounting for *SR*, where *SR* expressed in terms of *GBW* and i_d, enables to obtain the required value of i_d. Mal et al. [6] demonstrated the design of analog circuits using simulated *I*/*V* plots of a sample device of known dimension, wherein only gain requirement has been dealt with. In addition, factors that degrade circuit performance and trade with power and speed include that of [7]. Ou [8] presented a technique for reducing device noise based on g_m/I_d design flow. However, Alvarez et al. [9] presented a technique expressing normalized noise with respect to g_m/I_d, as MOS noise is not directly related to g_m/I_d. The values for de-normalization have to be then retrieved for circuit designing.

Fakhfakh et al. [10] presented a stochastic search algorithm for performance optimization which they later extended into a pareto front based multi-objective optimization algorithm [11]. Pareto front provides a set of non-dominated ideal solutions with suitable trade-off between the specifications. Also, mathematical optimization method, such as linear programming, nonlinear programming, geometric programming (GP), etc., widely used for constrained optimization problem [12, 13] is applicable for analog designing purpose. Recently, analog circuit optimization has been done using GP [14-16]. Using their synthesis method [14], Mandal et al. [16] proposed op-amp sizing method using GP formulation [16]. Hershenson et al. [15] also proposed a similar optimal design approach for op-amp using GP. GP uses circuit equations in posynomial form and it can be transformed to a convex problem by using log transformation [13]. GP only allows minimization of the objective function and thus limits its form. On the other hand, NLP [12, 17] permits the objective to take any of the minimization or maximization form and accepts convex as well as concave problem. This present work demonstrates how an amplifier design problem can be conveyed as NLP in accordance with [18].

3. Non-Linear Programming

Non-linear programming as a method to resolve an optimization problem, comes under the class of such a greater field of mathematical optimization, where non-linear nature of problem persists. It denotes minimizing or maximizing an objective function, f, subject to some constraint equations, g_i, where the objective function and/or some of the constraint equations can exist in non-linear form. In typical mathematical form, NLP can be expressed as,

$$\text{minimize or maximize } f(x_1, x_2, x_3, ..., x_n) \tag{1}$$

subject to

$$g_i(x_1, x_2, ..., x_n) \left\{ \begin{matrix} \geq \\ = \\ \leq \end{matrix} \right\} b_i \text{ for } i = 1, 2, ..., n. \tag{2}$$

wherex_1, x_2, ……, x_n are decision variables. NLP is subjective to give optimum result in any sort of non-linear situation. Hence, it can be pursued for optimizing an analog circuit problem which is articulated through non-linear and linear equations expressed in terms of current, voltage or additional design parameters. Design

algorithms based on NLP guarantee to give anticipated objective and also meet various performance conditions over a range of technology and process parameters.

4. Transistor Modelling

MOS transistor modelling involves the job of circuit sizing and determination of component values. Lately, the transistor modelling has been casted as an optimization problem, wherein the behaviour of a circuit has to be modelled with circuit equations. These analytical equations are expressed in terms of design parameters and then the optimization problem has to be solved considering the allowed limits on the design parameters. The modelling approach that has been considered in this work takes in the following form for the performance measures.

1. Output voltage swing for required biasing, V_{out} as a linear equation in terms of overdrive voltage, V_{ov}, I_d and load resistor, R_d.
2. A_v expressed as a linear equation in terms of V_{ov}, I_d and R_d.
3. UGF expressed as a linear equation in terms of V_{ov}, I_d and capacitive load, C_L.
4. *SR* expressed as a linear equation in terms of I_d and C_L.
5. P_{max} expressed as a linear equation in terms of I_d and power supply voltage, V_{DD}.
6. Thermal noise voltage, V_n expressed as a nonlinear equation in terms of V_{ov}, I_d and R_d.

It is a well-known fact that the I_d is a function of not only technology related parameters but also input voltage, V_{in} channel width, W and L. In order to obtain an optimal result in terms of above designable parameters, the proposed modelling approach varies the values of V_{in}, L and W along with the values of components, R_d and C_L.

5. Common Gate Architecture

The schematic of CG amplifier is shown in Fig. 1. CG stage has its gate biased at a desired potential ensuring proper operating condition. The circuit senses the input at its source terminal and produces V_{out} at drain terminal by transforming the variations in V_{ov} to I_d which flows through R_d. As established in [17], the performance metrics and design constraints for a CG amplifier with resistive load are conveyed in terms of parameters V_{ov}, I_d, R_d, W and L. Different process and technology associated bounds related with MOS model, for example, V_{DD} and other parameters as C_L are to be considered in the design formulation. To express the working of a CG amplifier with resistive load as a NLP problem, the subsequent design constraints and specifications linked with the performance of the circuit are needed to be contemplated.

5.1. Device dimension constraints

For a particular process file designs have limitations on device dimensions because of layout design rules. The bounded constraints on dimensions for M1 in Fig. 1 can be stated as

$$L_{\min} \leq L \leq L_{\max} \tag{3}$$

$$W_{\min} \leq W \leq W_{\max} \tag{4}$$

where, W and L are channel width and channel length of M1, correspondingly**.**

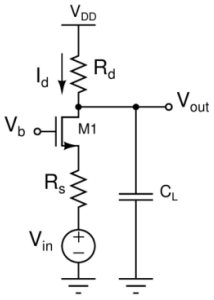

Fig. 1. CG amplifier with resistive load.

5.2. Constraint on bias and signal swing

Trans-conductance, g_m represents the acuteness of a device and MOS biased in saturation delivers a higher I_d in the circuit leading to a higher g_m. The minimum output voltage swing attainable with M1 in saturation should be

$$V_{out} \geq V_b - V_{th} \tag{5}$$

5.3. Constraints on small signal parameter

Output voltage of a MOS, having quadratic dependency on the input signal and responsible for the nonlinearity allows small-signal gain to have minimum dependence on g_m.

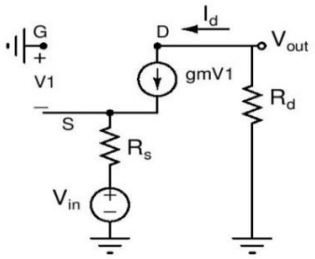

Fig. 2. Small-signal equivalent of Fig. 1 neglecting body bias and channel length modulation.

For M1, the gain equation is derived in the following manner. From Fig. 2, it is observed that

$$V_1 = -(V_{in} + V_{Rs}),\ I_d = \frac{-V_{out}}{R_d} = g_m V_1$$

$$\Rightarrow \ |\mathrm{A_V}| = \left|\frac{V_{out}}{V_{in}}\right| = g_m R_d,\ \text{neglecting potential drop across } Rs$$

Therefore, gain can be expressed as

$$g_m R_d \geq |\mathrm{Av}| \tag{6}$$

The *UGF* which signifies the frequency at which the circuit provides a gain equal to one and beyond which no further amplification by the circuit set up is possible is derived from Fig. 3 in the following manner. It is noted that

$$I_{out} = -g_m V_1 + \frac{V_{gd}}{1/\, j\omega C_{gd}} = -(g_m - j\omega C_{gd})V_1 + j\omega C_{gd} V_{in},$$

$$I_{in} = -j\omega C_{gs} V_1 - g_m V_1 = -(g_m + j\omega C_{gs})V_1$$

Thus, $\frac{I_{out}}{I_{in}} = \frac{-(g_m - j\omega C_{gd})V_1 + j\omega C_{gd} V_{in}}{-(g_m + j\omega C_{gs})V_1}$

$$\approx \frac{g_m}{g_m + j\omega(C_{gs} + C_{gd})} \approx \frac{g_m}{j\omega(C_{gs} + C_{gd})} \approx \frac{g_m}{j\omega C_L}$$

Hence, $f_T = \frac{g_m}{2\pi C_L} \geq UGF$ (7)

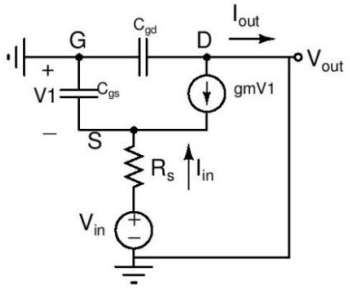

Fig. 3. Small-signal equivalent of Fig. 1 neglecting body bias and channel length modulation with interconnecting capacitances considering output short.

5.4. Constraints on power dissipation and slew rate

One of the most important factors influencing the overall efficiency of a system is power dissipation and thus is considered as a constraint as well as an objective function. In order to achieve least possible power dissipation, we must have

$$V_{DD} I_d \leq Max\ Power\ Dissipation \tag{8}$$

Limitations in slew rate, defined as the minimum permissible deviation in V_{out} with respect to time, leads to nonlinear issues. Thus, in order to achieve a proper operation, we must have

$$\frac{I_d}{C_L} \geq Slew\ Rate \tag{9}$$

5.5. Thermal noise

Voltages across any conductor waver as temperature increases since electrons move randomly inside it [6]. Also, reduced temperature does not decrease thermal noise as well because an increased mobility of electrons increases current. Thus, optimal scheme of design parameters is needed to decrease thermal noise. For the considered CG amplifier, thermal noise created by the load, R_d and the MOS, M1 can be conveyed as

$$V_n = \sqrt{4KT\left(\frac{2}{3g_m} + \frac{1}{g_m{}^2 R_d}\right)} \tag{10}$$

where, K is Boltzmann's constant and T is absolute temperature.

6. Constrained Optimization Problem

In order to formulate an optimization problem, constant parameters like permittivity of free space, permittivity of silicon dioxide, Boltzmann constant, temperature in degree Kelvin and capacitive load are required to be considered. Further, various process and technology parameters associated with the MOS model needs to be defined. With respect to the available design parameters, a linearly constrained nonlinear optimization problem can be framed as

$$\min \sqrt{4KT\left(\frac{2}{3g_m} + \frac{1}{g_m{}^2 R_d}\right)} \tag{11}$$

Subject to

$$I_d R_d \le V_{DD} - (V_b - V_{th}) \tag{12}$$

$$2I_d R_d \ge \text{Av}(V_b - V_{in} - V_{th}) \tag{13}$$

$$I_d \ge \pi UGF(V_b - V_{in} - V_{th})C_L \tag{14}$$

$$I_d \ge SR \times C_L \tag{15}$$

$$I_d \le \frac{P_{\max}}{V_{DD}} \tag{16}$$

$$I_d \ge 0 \tag{17}$$

It is seen from Eq. (11) that noise, the objective function, quadratically depends on g_m, marking its nonlinear accord with I_d and V_{ov}, though Eq. (12) - (17) show that the constraint equations have linear dependency with I_d and V_{ov}.

7. Results and Analysis

The above formulated performance metrics and constraint equations of a CG amplifier graphically create a feasible region which is a polytope. The required optimum value of design parameters is then derived by navigating over each of the corner and internal points of the polytope by simplex method and interior point based method, respectively [18]. The proposed algorithm declares an infeasible result if the

constraints are impracticable. Using simplex method, the optimum value of our objective function at one of the corner points for a particular value of R_d is first obtained, assuming that the optimal value lies at one of the corners and likewise for every R_d. The most optimal value is observed from among those obtained for every R_d. Further, the optimality is confirmed by interior point based method.

Figure 4 shows the feasible region, i.e., polytope shaped by using the Eq. (11) - (17) for R_d = 7.2kΩ. Feasible region means the plane where each paired value of I_d and V_{ov} fulfills the constraint equations. The feasible half-plane for each constraint is specified by the arrows, eventually leading to the creation of polytope. The points A, B, C and D bound the polytope. The design scheme for the method presented in this work is described in Figs. 5 and 6, where the design flow of Fig. 5 is used to obtain the sought after intersection point that results in optimum performance. The design flow shown in Fig. 6 is further used to verify whether any optimum result exists within the design space or not. It is notable that until now there were no specifics available regarding the design space in collected works.

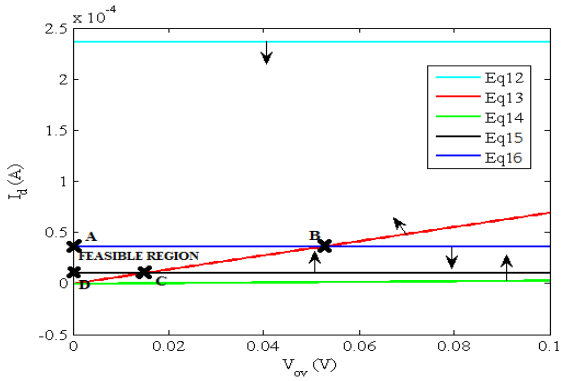

Fig. 4. Plot showing the generation of polytope.

According to Fig. 5, the objective function along with all the constraint equations are conveyed in terms of I_d and V_{ov} based on the specification values provided in Table 1. These objective functions and the constraints are derived from design related circuit equations. For a particular R_d, V_{ov} is first traversed over an acceptable range of values and I_d is marked for each value of V_{ov}. The intersection points are found by equating the array of I_d for every single pair of Eq. (12) - (17). The number of iterations, x, required to determine the points depend on the way V_{in} is scaled. A specific set of I_d and V_{ov} mutual to a pair of Eq. (12) - (17) are acquired and the objective function is measured at each of these intersection points. The minimum value of objective function is then derived from the set of calculated objective functions along with the corresponding I_d and V_{ov}. This intersection point is then checked to verify whether it satisfies all the constraint equations or not. If not, the subsequent minimum objective value in the set is selected as per Fig. 5. The minimum objective function obtained to fulfill the constraint equations is achieved using y iterations, where y may extend to total number of intersection points attained. Firstly, the I_d and V_{ov} values corresponding to the minimum objective function are found and the aspect ratio is then obtained. Thereafter, it is checked whether the channel width is within the defined limits. When the minimum objective function is identified, the

corresponding I_d, R_d, W/L, L, W and output specifications are distinguished. This procedure is continual for every single R_d, and the optimum result attained at the end of z iterations are presented in Table 2.

With the circuit specifications given in Table 1, it is observed that the optimal solution is attained at a corner point, as no interior point fulfils the channel width requirements. Once the optimal design values are obtained using the proposed method, the CG amplifier design is simulated using TSMC 180nm technology in LT spice. Table 3 presents the quantitative comparison of the simulated, proposed design set up and existing works. Assessment of result with existing work implies a superior outcome with respect to achievement Av and *UGF*. The deviance in experimental result attributes to shorter channel length of the device, negligence of body effect, g_{mb}, drain output resistance, r_o along with the parasitic capacitances of the device. Moreover, no considerable deviance is seen among the simulated and proposed results and subsequently the design method presented here can be used for a first order calculation of bias current and transistor dimensions. Besides in only 3-4 seconds the entire design flow is executed in Matrix Laboratory (MATLAB), which illustrates the run time efficiency of the presented method. The product of x, y and z iteration specify the computational complexity in its worst case. In other words, the scaling of the consecutive terms of V_{in}, W, L and R_d basically controls the competence of the method.

Table 1. Design specification values for CG amplifier with resistive load.

Constraints	Specifications
Minimum channel length, L_{min}	≥180 nm
Maximum channel length, L_{max}	≤360 nm
Minimum channel width, W_{min}	≥180 nm
Maximum channel width, W_{max}	≤35 µm
Small-signal gain, Av	≥10
Unity gain frequency, *UGF*	≥10 MHz
Slew rate, *SR*	≥10 V/µs
Power dissipation, P_{max}	≤65 µW
Gate bias voltage for M1, V_b	0.5 V
Capacitive load, C_L	1 pF
Resistive load, R_d	100-50 kΩ

Table 2. Optimum values for design of CG amplifier.

Design variables/Output specifications	Specification
R_d	7.2kΩ
V_{ov}	0.0520V
V_{in}	0.0480V
I_d	36.111µA
W/L	123.1886
W	22.174µm
L	180nm
V_n	3.0234nV/$\sqrt{Hz}$
UGF	221.2MHz
Av	20dB
SR	36.111V/µs
P_{max}	65µW

Table 3. Design comparison for CG amplifier between the measures obtained with NLP, LT spice and existing works.

Design variables /Output Specifications	Specification	NLP	LT spice	Paper [3]	Paper [18]
I_d	≥0	36.1µA	20.246 µA	1.6 µA	3.9 µA
V_n	Minimize	3.02 nV/$\sqrt{Hz}$	17 nV/$\sqrt{Hz}$	-	-
UGF	≥ 10MHz	221.2 MHz	89 MHz	9.7 MHz	-
Av	≥ 10	20 dB	11.9 dB	9.5 dB	1.9 dB
SR	≥ 10V/µs	36.1 V/µs	20.2 V/µs	-	-
P_{max}	≤ 65µW	65 µW	36.44 µW	-	-
Complexity	≥ 10MHz	3-4 sec	-	-	-

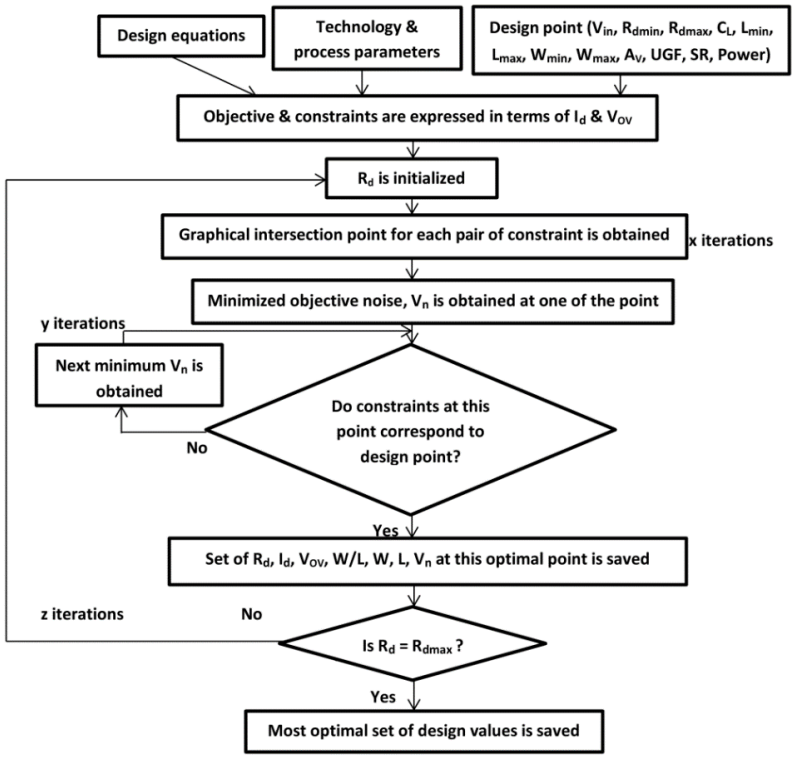

Fig. 5. Design flow to obtain the optimal point using simplex method.

It is seen from Fig. 7 that with increase in the *W*, GBW increases as an increased *W* leads to an increased I_d thereby raising g_m. This further leads to a rise in *UGF*. Again, an increase in I_d is accompanied by a rise in power. So, the variation in device dimension results in negligible influence on *UGF* in low power region. Henceforth, for a certain *W*, *UGF* rises with rise in power. It can be deducted that *UGF* has a quadratic dependence on power when conveyed with respect to *W*/*L*. Figure 8 shows that the influence of Av on *UGF* is substantial only at high power since *UGF* is linearly correlated to both power and Av here.

Figure 9 illustrates that when the value of W is raised, V_n falls for arise in g_m as it has inverse dependency with V_n. Again, as mentioned previously, an increase in I_d is accompanied by a rise in power. So, V_n falls with rise in power, for a specific W. It can be seen that V_n has quadratic dependence on power when expressed with reference to W/L. Finally it can be noted that the value of g_m has the major impact on V_n and other performance metrics considered for a CG amplifier. The trade-off curves show a similar trend to that observed in [18] for a common source (CS) amplifier.

Using the design specifications provided in Table 1, various performance metrics obtained for varied single stage amplifiers on the application of NLP is shown in Table 4. It is established from the outcomes that all of the amplifier circuits can certainly be conveyed as NLP problem and resulting performance metrics simply show the uniqueness of the proposed technique**.**

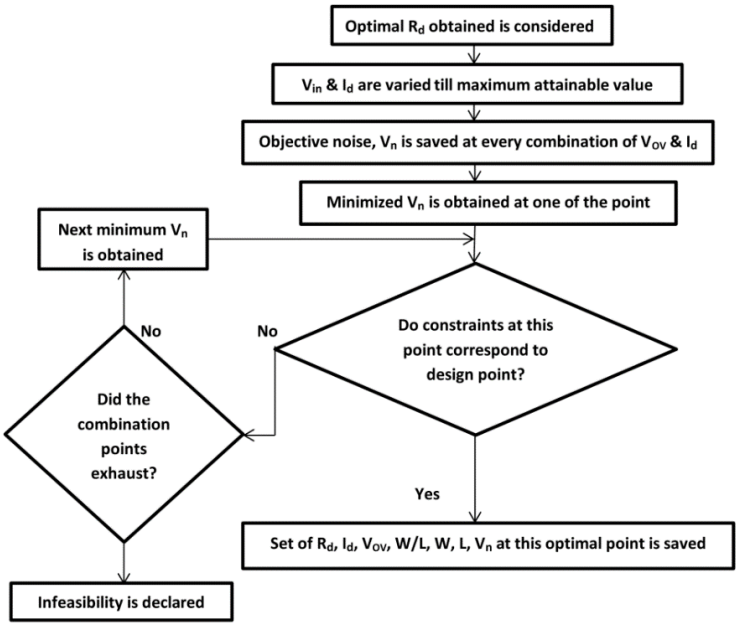

Fig. 6. Feasibility of the design flow using interior point based method.

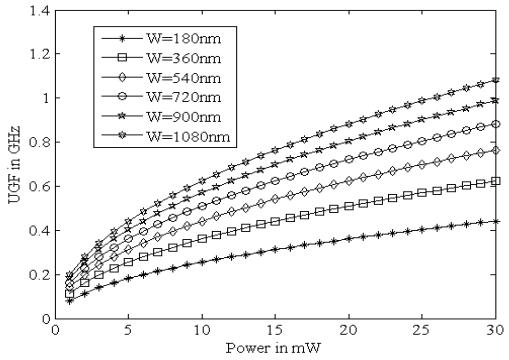

Fig. 7. Plot of UGF vs. power for different aspect ratios.

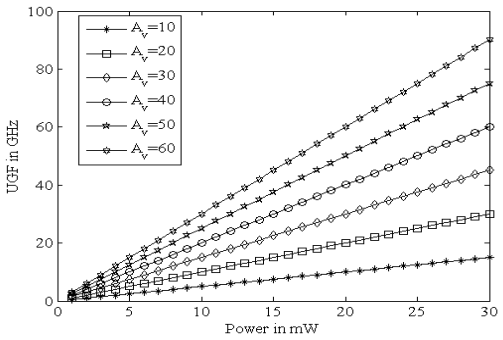

Fig. 8. Plot of UGF vs. power for different gain.

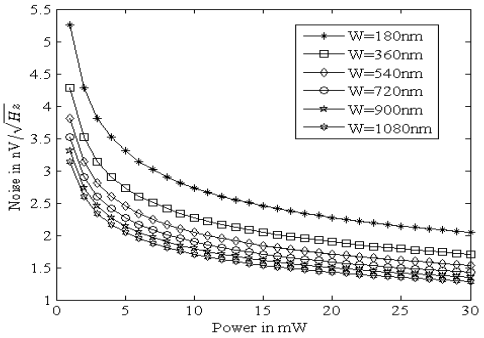

Fig. 9. Plot of *thermal noise* vs. *power* for different aspect ratios.

Table 4. Optimal design values for common source and common drain.

Design variable/Output specifications	Common source with resistive load	Common source with diode connected load	Common drain
R_d	48.3kΩ	-	-
R_s	-	-	700Ω
V_{ov1}	0.0560V	0.0800V	0.0433V
V_{in}	0.4560V	0.4800V	0.4686V
V_{ov2}	-	0.8000V	-
I_d	36.108µA	31.108µA	36.111µA
W1/L1	106.2086	44.8355	177.3915
W2/L2	-	1	-
W1	19.118µm	8.0704µm	31.930µm
L1	180nm	180nm	180nm
W2	-	180nm	-
L2	-	180nm	-
V_n	2.961nV/$\sqrt{Hz}$	4.040nV/$\sqrt{Hz}$	4.069nV/$\sqrt{Hz}$
UGF	205.3MHz	123.8MHz	265.39MHz
Av	35.8dB	20dB	5.3769dB
SR	36.108V/µs	31.108V/µs	36.111V/µs
P_{max}	64.9µW	55.9µW	65µW
Complexity	2-3sec	3-4sec	4-5sec

8. Conclusions

A global method for the design and optimization of a common gate amplifier is evaluated in this paper. The non-linear and linear parameters accompanying the operation of MOS as constraint equations are included by means of conveying the amplifier design problem as a non-linear program. The constraint equations geometrically shape a feasible region, polytope, for which simplex method determines an optimum value by navigating every corner point of the polytope formed and subsequently the optimum value is confirmed by means of an interior point based technique. Therefore, the amplifier design problem is conveyed as a form of mathematical optimization problem, for which global optimization methods have been established. The exclusivity of the proposed method is confirmed by obtaining results for varied amplifier circuits and superior outcome in comparison with that obtained by existing methods.

References

1. Silveira, F.; Flandre, D.; and Jespers, P. (1996). A g_m/I_d based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. *IEEE Journal of Solid-State Circuits*, 31(9), 1314-1319.
2. Cunha, A.I.A.; Gouveia-Filho, O.C.M.; Schneider, C.; and Galup-Montoro, C. (1997).A current-based model for the MOS transistor. *Proceedings of 1997 IEEE International Symposium on Circuits and Systems, ISCAS'*97, 3, 1608-1611.
3. Cunha, A.; Schneider, M.; and Galup-Montoro, C. (1998). An MOS transistor model for analog circuit design. *IEEE Journal of Solid-State Circuits*, 33(10), 1510-1519.
4. Oliveira Pinto, R.; Cunha, A.; Schneider, M.; and Galup-Montoro, C. (1998).An amplifier design methodology derived from a MOSFET current-based model. *Proceedings of 1998 IEEE International Symposium on Circuits and Systems, ISCAS'98*, 1, 301-304.
5. Farag, F.A. (2002). CMOS amplifier design methodology for optimum slew rate. *11th Mediterranean Electrotechnical Conference, MELECON 2002*, 532-536.
6. Mal, A.K.; and Mal, A. (2016). Amplifier Design Approximations in Submicron CMOS. *International Conference on Microelectronics, Computing and Communications (MicroCom)*, 1-4.
7. Razavi, B. (2001). *Design of Analog CMOS Integrated Circuits* (1st ed.) McGraw-Hill.
8. Ou, J. (2011). g_m/I_d based noise analysis for CMOS analog circuits. *IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 1-4.
9. Alvarez, E.; and Abusleme, A. (2012). Noise power normalisation: extension of g_m/I_d technique for noise analysis. *Electronics Letters*, 48(8), 430-432.
10. Fakhfakh, M.; Loulou, M.; and Masmoudi, N. (2007).Optimizing performances of switched current memory cells through a heuristic. *Analog Integrated Circuits and Signal Processing*, 50(2), 115-126.

11. Kotti,M.; Sallem,A.; Fakhfakh,M.; and Loulou, M. (2010).A novel multi-objective algorithm: application to the optimal sizing of current conveyors. *XIth International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD)*, 1-5.
12. Vanderbei, R.J. (2001). *Linear programming foundations and extensions*. Springer.
13. Boyd, S.; Kim, S.J.; Vandenberghe, L.; and Hassibi, A. (2007).A tutorial on geometric programming. *Optimization and Engineering*, 8(1), 67-127.
14. Mandal, P.; and Visvanathan, V. (1999). A new approach for CMOS op-amp synthesis. *Proceedings Twelfth International Conference on VLSI Design*, 189-194.
15. Hershenson, M.D.; Boyd, S.P.; and Lee, T.H. (2001).Optimal design of a cmos op-amp via geometric programming. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 20(1), 1-21.
16. Mandal, P.; and Visvanathan, V. (2001). CMOS op-amp sizing using a geometric programming formulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 20(1), 22-38.
17. Buchanan, C. (2007).*Techniques for solving nonlinear programming* problems *with emphasis on interior point methods and optimal control problems*, M.Phil. Thesis, University of Edinburgh.
18. Bhattacharjee, P.; Mondal, A.J.; Majumder, A.; and Metya, S.K. (2016). Amplifier design and optimization using Non Linear Programming. *IEEE 26th International Conference Radioelektronika (RADIOELEKTRONIKA)*, 22-27.