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The Interface and Control System of the Upgraded HVOpto/HVRemote Card of the *TileCal*

C. Rato[a], J. Sabino[a], L. Gurriana[b], L. Seabra[b], A. Gomes[ab], G. Evans[ac], J. Soares Augusto[ad], A. Maio[ab]
[a]Faculdade de Ciências da Universidade de Lisboa, Portugal; [b]LIP, Portugal
[c]BioISI, Universidade de Lisboa, Portugal; [d]Inesc-ID, Portugal

***Abstract*—To comply with the increase in luminosity of the LHC (Large Hadron Collider) in the next decades, the electronics of the ATLAS (A Toroidal LHC Apparatus) experiment is being upgraded. Included in the upgrade is the interfacing and control electronics system of the *HVOpto/HVRemote* cards in the *TileCal* (Tile Calorimeter) detector, which provides high voltages to about 10^4 photomultipliers (PMTs). This paper presents the new interfacing architecture for the system and details the design of a prototype control board (*HVRemote-Ctrl*) used for test and validation of the new architecture. The tests evaluate the system multiplexing capabilities needed to monitor all the *TileCal* PMTs in real time. The communication channels involved, supported in Ethernet and SPI interfaces/protocols, have been fully tested. Some results from the tests already completed are presented.**

Keywords: Instrumentation for High-Energy Physics, Electronic Control, Ethernet/SPI Interfacing.

I. Introduction

An electronic system currently being upgraded at the ATLAS experiment[1] is the one in charge of the control and distribution of high-voltage (HV) to the approximately 10^4 PMTs of the *TileCal* detector. Its core comprises two cards [1]: the *HVOpto* and the *HVMicro*. In the current ATLAS setup, this system is located inside the detector, so it operates under high doses of radiation. Current *TileCal* HV (High Voltage) electronics is in operation for more than 10 years and, as a result, it is ageing despite its design took into account radiation hardness. Another severe constraint is the difficulty in maintaining and replacing faulty *HVOpto* or *HVMicro* cards: it is never possible to do this when the LHC is running, the maintenance is possible only when the LHC stops at least for a few months and radiation levels decrease to values tolerable by the staff.

To alleviate these constraints, one of the proposed upgrade options [2][3] moves the *TileCal*'s *HVOpto* electronic control system from the detector innards, for a location in the USA15 room which is a low radiation environment far away (100 m) from the detector. This will improve the lifetime of the system and provides for immediate maintenance and replacement. On the other hand, the power supplies of the *HVRemote*[2] board will now be connected through a bunch of 100 m cables, what worsens its stability and noise levels. Since the current electronic design is about 20 years old, some components in the *HVOpto*, such as the ADCs and DACs[3], are obsolete and have to be replaced by modern alternatives.

The *HVRemote* board has some caveats, noticeably the fact that very high voltages (in the -800 to -1000 V range), low level analogue signals, several digital control lines and a low speed processor, all share the board. So, the overall noise in the board, which is highly shaped by components' and traces' layout, shielding and cabling, is significant and difficult to predict before actual measurements are performed.

In this paper it is described the upgrade of the control system of the HV cards for the *HVRemote* version. Most of the tests presented in this paper, which aim at evaluating and validating several of our design options, were based in a prototype board, called *HVRemote-Ctrl* card, which contains a downsized replica of the hardware used in the communications interface of the full *HVRemote* board. That prototype is described below.

It should be noted that there is a concurrent effort related with the TileCal's HV system at the *TileCal*'s community [4] that intends to keep the HV electronics in the detector.

II. The *HVRemote* Control System

A. The HVRemote Control Path and Hardware

The architecture of the upgraded electronics system of the *TileCal* is shown in fig. 1. The control master is a PC/workstation configured as a node of the DCS (Detector Control System) of ATLAS. The DCS commands sent to, and the data read from the *HVRemote* boards flow through a tree of Ethernet links, joining the PC and 256 boards, each of these managing 24 PMT channels.

The control software consists in DCS (high-level commands), C++ and Python programs, running in the PC, which use the DCS API (Application Programming Interface), and also C programs running in the *Tibbo* EM1206 modules (described below). These modules, one of them attached to each *HVRemote* board, are used to read commands from the Ethernet channel, convert them into raw digital signals and send them to *HVRemote*'s digital control circuits through a SPI (Serial Peripheral Interface) link. The *Tibbo* EM1206 modules also manage the reverse data flow (from the *HVRemote* to the upstream DCS computers.)

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[2]To keep things clear, we call to the "old" HV system, now in operation, the *HVOpto*, and we call to the upgraded system the *HVRemote*.

[3]DAC refers to a generic Digital-Analogue Converter; ADC refers to a generic Analogue-Digital Converter.

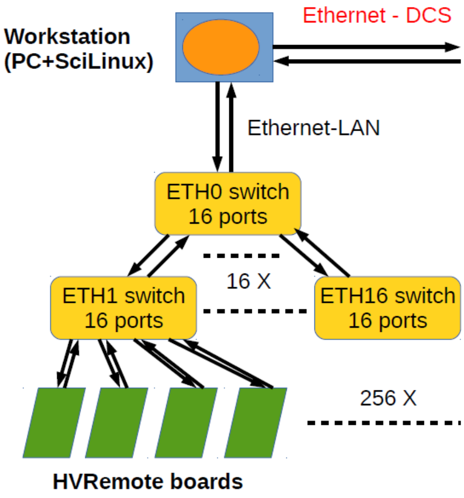

Fig. 1. Architecture of the *HVRemote* control tree.

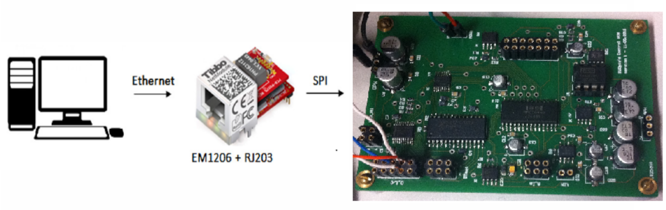

Fig. 2. Protocols in the *HVRemote* monitoring, supervising and control system. The *HVRemote-Ctrl* prototype is shown at right.

B. The HVRemote-Ctrl Testing Card

To evaluate the supervising and control system of the *HVRemote*, before this complex and costly board is fully assembled, it was built a test card, called *HVRemote-Ctrl* (figs. 2 and 3), which has the same control/interfacing components of the *HVRemote*, but misses front-end electronics of the 24 PMTs. This provides means to test both the digital control hardware and the *Tibbo* module, and to assess the transfer speeds. The *HVRemote-Ctrl* has already been assembled and the tests are undergoing. The DAC and ADC in this card are platforms for evaluating the test algorithms.

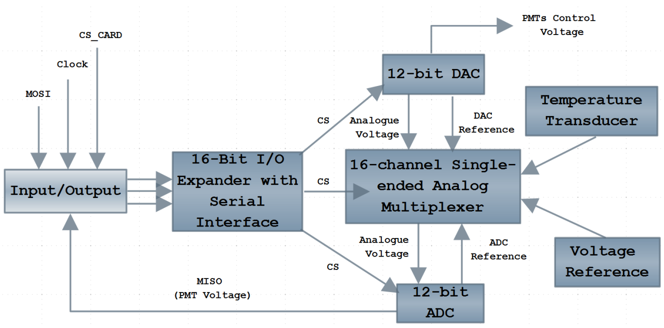

Fig. 3. Simplified block diagram of the *HVRemote-Ctrl* card. Not all signals are shown.

1) The hardware of the HVRemote-Ctrl card: A DC level translator MAX3002[4] is used to make compatible the 3.3 V and 5 V levels in the signals shared by the *Tibbo* module and the CMOS hardware. The *HVRemote-Ctrl* card has a 16-bit port expander with SPI interface (MCP23S17), a 12-bit DAC (DAC7568), a 16-bit analogue multiplexer (MPC506), an instrumentation amplifier (INA128), a 12-bit ADC (TLV2541), a temperature sensor (TMP17) and a voltage reference (AD589).

These are the same components (but in less quantity), and interfacing architecture, found in the *HVRemote* full card undergoing fabrication at the moment. The *HVRemote-Ctrl* card also allows applying the histogram test to each individual data converter using several digital pseudorandom uniform noise generators (UNGs). In some of the current test settings used with the card, an *Arduino Uno* replaces the commercial module EM1206+RJ203 (shown in the centre of fig. 2) as the SPI master and so the DC/DC converter MAX3002 is not needed and is tested separately.

To access and control the electronic components in the *HVRemote-Ctrl* card, the serial data from the SPI is converted to a parallel format. This has really to be done due to the modest pin-count of the *Tibbo* module. That serial-to-parallel conversion occurs in the MCP23S17 expander: the data in parallel configures the DAC, ADC and multiplexer's parameters (fig. 4). The MCP23S17 has 16 general purpose input/output pins (two byte-wide ports, GPA and GPB) backed and configured by several internal registers. The signals relayed by the expander link the *Tibbo* module to the functional devices. There are four lines dedicated to the SPI protocol (CS, SCK, SI and SO) which interface with the *Tibbo* module.

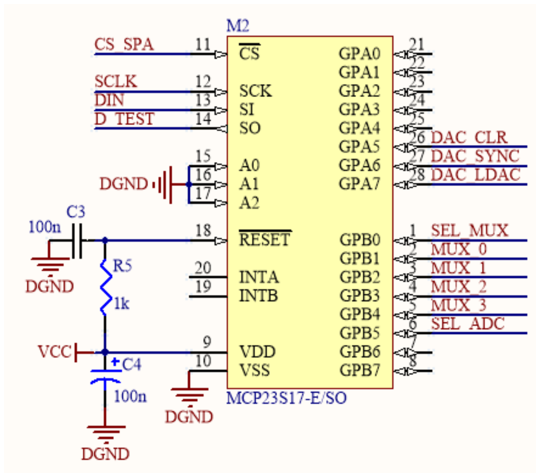

Fig. 4. MCP23S17 signals in the *HVRemote-Ctrl* card.

2) Software for testing the HVRemote-Ctrl card: An user interface written in Python is being developed to test the board's components. The test of the expander has already been completed with success. In the user interface window where the test of the expander is performed (fig. 5), the user sends

[4]The data sheets of the components in the *HVRemote-Ctrl* card are easily found in the Internet, and as such we abstain from providing their references.

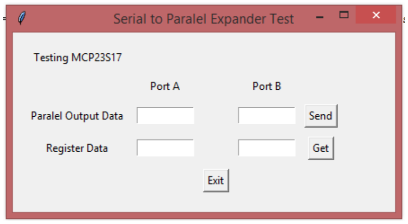

Fig. 5. User interface for testing the MCP23S17 in the *HVRemote-Ctrl* card, developed in Python.

16 bits as two-byte strings (corresponding to the two ports, GPA and GPB) and the data written in the ports will be sent back, received by the *Arduino Uno* and saved in a file.

The communication with the expander is done through the *Arduino IDE*. Since the user interface is developed in Python and runs in the PC, a logical serial communication channel is established between the *Arduino* and the Python user interface, such that this interface can send/receive the data to/from the expander which is in the *HVRemote-Ctrl* card. It is used the MCP23S17 library for *Arduino* [5] in this task.

In the user interface, the received data is assembled in an array, processed and saved to a file. All the read/write tests already done were successful, and so it was concluded that it is safe to use the expander to configure and test the other components in the *HVRemote-Ctrl* card.

3) Testing of converters with pseudorandom noise generators and histogram tests: The MCP23S17 expander is currently the only component totally tested in the *HVRemote-Ctrl* card, but this card is also supposed to be a platform for the individual testing of both DACs and ADCs and its static characterization with histogram tests, performed with different digital pseudorandom uniform noise generators (NGs). Both converter types will be characterized using a Mersenne-Twister algorithm [6] for the uniform NG and a Box-Muller algorithm [7] for the digital Gaussian NG. Digital pseudorandom noise generators can be a powerful method to characterize converters [8], [9]. These noise generators were simulated in MATLAB and saved in files. The user interface for testing, already done, reads these files in the process of characterizing the converters.

The converters' characterization algorithm is based on the histogram test [8] and comprises two independent steps. The first one is done only once at the beginning of the test task. It consists in the characterization of the selected NG using simulated histograms saved in files. Its uniformity or Gaussian errors are computed and afterwards considered in the characterization of the converters. This calibration/correction step allows to mitigate the error due to intrinsic NGs non-idealities which perturbs the converters test results.

After the characterization of the NGs, a histogram is computed and the converter's offset voltage and gain error are obtained. After the correction of the offset voltage and gain error, the differential (DNL) and integral non-linearities (INL) are calculated, and these are the last steps in the test of the converters.

The user interfaces for orderly applying these tests and characterizing the converters are being finished at present, but the test algorithm is already fully operational and has been used.

C. Evaluation of the Tibbo EM1206+RJ203 Module and the Connection with the DCS System

In parallel with the testing of the hardware in the interface of the *HVRemote* card, a task performed in the *HVRemote-Ctrl* prototype card as described in the previous section, the full logic communication link between the DCS system and the *HVRemote* interface has also been tested. This means that the Ethernet link between the DCS and the *Tibbo* module, as well as the operation of this module acting as a SPI Master device, have been tested. This comprises the two channels and protocols shown in fig. 2. The important systems in this test task are the *Tibbo* module EM12016+RJ203 (or the evaluation board), the DCS software and the MCP23S17 expander.

1) Testing Ethernet communication with the Tibbo module: In preliminary tests, to probe the Ethernet interfacing solution, it was used a *Tibbo* EM1206-EV evaluation board and, in more recent tests, the *Tibbo* module EM12016+RJ203 itself (see fig. 2). One of these modules will be soldered to each *HVRemote*. *Tibbo* supplies an integrated development system for the board, which includes C libraries for sockets programming and SSH communications, two important libraries for our work. *Tibbo* also supplies a standalone tool, the *IO Ninja*, which allows testing the Ethernet communication channel between the *Tibbo* module or evaluation board and the PC.

The *Tibbo* module is programmed either in C or in BASIC. A raw Ethernet client using sockets was developed in C and deployed in the module. It succeeded in communicating with an Ethernet master in the PC, programmed in Python, and with the *IO Ninja* also working as an Ethernet/sockets master.

The programs (or scripts) used in these preliminary tests followed closely the reference implementations suggested by the board vendors.

2) Interfacing DCS with HVRemote-Ctrl: Recently it was prepared in our laboratory a workstation where the DCS system is installed and runs with full functionality. This platform was used to perform more communication tests. The main goal was to exercise the hand-shaking between DCS and the *Tibbo* Ethernet hardware.

A DCS panel was developed, which sends/receives commands and data for/from the *Tibbo* module. These commands are applied to external hardware, the MCP23S17 expander, a process that simulates the access to the *HVRemote* interface through an SPI channel. In fig. 6 is shown a small part of a DCS control panel prepared to drive each channel of the *HVRemote* board which was are developed using the WinCC language, a programming tool belonging to the SCADA SIMATIC development system [10].

Since only one *HVRemote-Ctrl* board was fabricated, and when these tests were done it was not yet available, the *Tibbo* module communicated with a single MCP23S17 expander mounted in a breadboard (fig. 7).

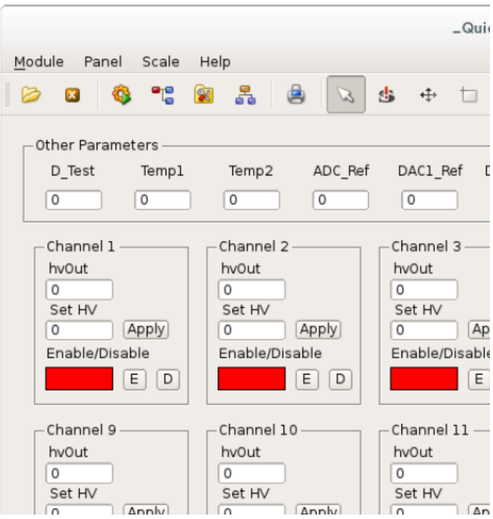

Fig. 6. Partial view of the DCS panel developed for the *HVRemote* card.

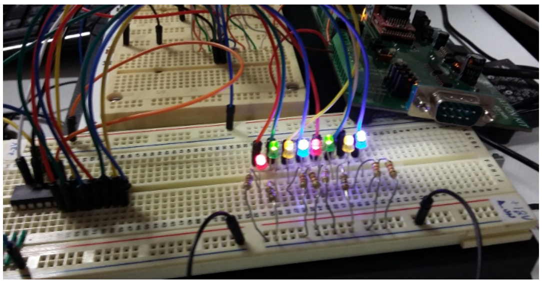

Fig. 7. *Tibbo* evaluation card communicating with an MCP23S17 through an SPI channel. The *Tibbo* evaluation card is driven by DCS commands coming from the workstation.

3) The Tibbo module and SPI: The performance of the SPI interface in the *Tibbo* module was tested in several experiments. For instance, SPI connection with two devices in a same SPI bus was established using two *Arduino* boards as SPI slaves, because when linked to the full *HVRemote* card the module will have to manage three MCP23S17 port expanders. In fig. 8 it is seen a signal from one experiment, where the SPI clock in the *Tibbo* was set to a frequency of 200 kHz.

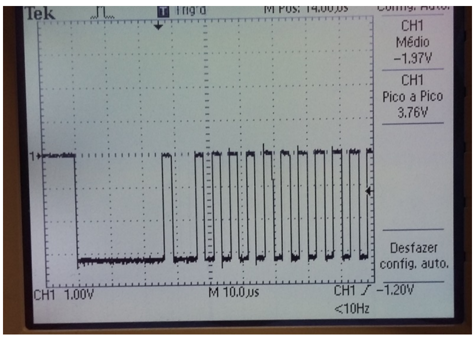

Fig. 8. SPI signal (MOSI or SI) during communication. The transmission clock in the *Tibbo* was set to a period of about 5 μs (2 periods per oscilloscope division in this image).

III. Results and Conclusion

The development of the *HVRemote*, already finished, was driven by the knowledge gained from evaluating the *HVRemote-Ctrl* card. The following tasks have been completed:

- Development and assembly of the *HVRemote-Ctrl* card, to evaluate the digital control and supervising system. This prototype card is already partially tested (fig. 2).
- Development, in Python, of a panel to manage the *HVRemote-Ctrl* card.
- Evaluation of the *Tibbo* EMS1206 module as a suitable Ethernet controller for the *HVRemote* board.
- Evaluation of the *Tibbo* EMS1206 module as SPI master, using multiple Arduinos configured as SPI slaves.
- Development of a DCS control panel, underlying functions, and establishment of Ethernet communications between DCS and the *Tibbo* module (fig. 6).

The speeds measured in both Ethernet and SPI communications with the *Tibbo* module are suitable to monitor in real time all the 256 *HVRemote* boards and 10^4 PMTs in the *TileCal* (each PMT is monitored each few seconds).

The prototype of a full *HVRemote* card is almost finished and the software already developed will be adapted and scaled to target that board instead of the *HVRemote-Ctrl* test board. Hopefully, the new *HVRemote* control system will comply with the requirements needed to cope with the escalade in *TileCal* data flow triggered by the increase in luminosity of the LHC, and will be installed in the ATLAS experiment.

References

[1] R. Chadelas et al., "High voltage distributor system for the Tile hadron calorimeter of the ATLAS detector", ATLAS-TILECAL-2000-003, 2000.
[2] F. Vazeille, "Performance of a remote High Voltage power supply for the Phase II upgrade of the ATLAS Tile Calorimeter", JINST 11 C02050, 2016.
[3] A. Gomes, "The new front-end electronics for the ATLAS Tile Calorimeter Phase 2 Upgrade", JINST 11 C02015, 2016.
[4] G. Drake, "The New Front-End Electronics for the ATLAS Tile Calorimeter Phase 2 Upgrade", ATLAS note ATL-TILECAL-PROC-2015-023, https://cds.cern.ch/record/2114792/files/ATL-TILECAL-PROC-2015-023.pdf
[5] C. Buffington, "MCP23S17 Class for Arduino", http://playground.arduino.cc/Main/MCP23S17, retrieved in January 2017.
[6] M. Matsumoto, and, T. Nishimura, "Mersenne Twister: A 623-Dimensionally Equidistributed Uniform Pseudorandom Number Generator", ACM Transactions on Modeling and Computer Simulation, vol.8, no. 1, pp.3–30, 1998.
[7] D.-U. Lee, J. D. Villasenor, W. Luk and P. H. W. Leong, "A Hardware Gaussian Noise Generator Using the Box-Muller Methods and Its Error Analysis", IEEE Transactions on Computers, vol. 55, no. 6, pp. 659-671, June 2006.
[8] J. Alves and G. Evans, "Digital Pseudorandom Uniform Noise Generator for ADC Histogram Test", DCIS 2015 – XXX Conference on Design of Circuits and Integrated Systems, pp. 1- 6, Estoril, Portugal, November 2015, DOI: 10.1109/DCIS.2015.7388592.
[9] J. D. Alves and G. Evans, "A Digital Pseudorandom Uniform Noise Generator for ADC Built-In Self-Test", 2015 10th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS), pp. 1-5, Naples, Italy, April 2015.
[10] http://w3.siemens.com/mcms/human-machine-interface/en/visualization-software/scada/pages/default.aspx, https://en.wikipedia.org/wiki/WinCC, retrieved in January 2017. WinCC is a part of the SIMATIC SCADA system from Siemens.