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The Design of High Performance, High Resolution Two-Order Delta-Sigma Modulator

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Abstract: The design of single loop two-order Delta-Sigma modulator with feed forward structure is presented in this thesis. Oversampled analog-to-digital converters based on second-order delta-sigma modulation are attractive for VLSI implementation because they are especially tolerant of circuit nonidealities and component mismatch. The noise shaping and oversampling are used in this modulator, the oversampling rate (OSR) is 256 and the resolution could be reached 14 bits. The integrally design of Delta-Sigma modulator is argued in deep in the paper, since the behavior model is tested efficiently by Simulink, the time of design has been cut to the bone. As the fully differential structure is used, the system to inhibit the ability of common-mode interference improved and the sampling rate is also raised, the fully differential switching capacity structure is used in the circuit design of modulator. And because of the fully differential structure, the input noise is reduced, the output slewrate of op-amp is greatly improved and the whole circuit is more stable. The 0.5 μm CMOS process is used in simulation of circuit, the results of simulation are shown that the amplifier gain is 82.3 dB, the Phase Margin is 71.34°, the output slewrate of op-amp is 202 V/μs, the unit GainBandWidth is 102 MHz. the whole circuit of modulator is tested with 10.24 MHz of the clock frequency, the SNDR reached to 93.2 dB, the Dynamic Range (DR) is 100 dB. In summary, this Delta-Sigma modulator could be used in Portable, Audio system and so on. *Copyright © 2013 IFSA.*

Keywords: Delta-Sigma ADC, Delta-Sigma modulator, OP-AMP.

1. Introduction

Currently, the oversampling techniques is widely used in analog-to-digital converter [1], compare with the Nyquist frequency, the oversampling reduce the harsh requirement of analog circuit and greatly improve the resolution [2-4]. In an oversampled A/D converter based on delta-sigma modulation, the input signal is sampled at many times its Nyquist rate. The sampled input signal is quantized by a modulator that consists of a low-pass analog filter and a coarse quantizer embedded in a feedback loop. The analog filter and the feedback around the modulator shape the large quantization noise produced by the coarse quantizer, moving most of its energy to frequencies above the desired signal band, or baseband. A digital low-pass filter then removes this shaped quantization noise so that the signal may be resampled at a lower rate to produce the final high-resolution Nyquist rate output. The combined functions of digital low-pass filtering and resampling are commonly referred to as decimation filtering.

In addition to their tolerance for circuit non-idealities, oversampled A/D converters simplify system integration by reducing the burden on supporting analog circuitry. Because they sample the analog input signal at well above the Nyquist rate, precision sample and hold circuitry is unnecessary. Also, the burden on the analog anti-aliasing filter is considerably reduced. Much of its function is

transferred to the digital decimation filter, which can be designed and manufactured to precise specifications, including a linear phase characteristic.

A variety of delta-sigma modulator architectures have been explored recently. Among these, perhaps the most robust is a second delta-sigma modulator wherein two integrators are combined with a single two-level quantizer [5]. The present work examines the application of the second order delta-sigma modulator to signal acquisition with digital audio performance, which is taken to mean a dynamic range of 14 bit or more and signal bandwidths exceeding 20 kHz.

The Delta-Sigma modulator is a key part of the Delta-Sigma ADC. As we know that the higher order, the higher accuracy of the ADC realization, but the circuit structure of Delta-Sigma modulator is more complex. The system performance could be easily affected with many non-ideal factors. And it would be bringing a heavy workload [6-7].

To sum up, for design a high speed, high performance, high efficiency, low power consumption delta-sigma modulator, we should give fully consideration to the various non-ideal factors, such as clock jitter, charge injection, and the non-linear of operation amplifier and so on, and complex problems of circuit in the simulation of the behavior level, analysis of these non-ideal factors how impact on work of delta-sigma modulator. And then ensure and trade-off the performance parameter for circuit design by the simulation of Behavior level, therefore, system level really greatly reducing the workload of the circuit-level design.

Because of that the device precision components mismatch and nonlinear which due to restrictions in the manufacturing are overcame, the oversampling and noise shaping are used in delta-sigma modulator. Hence, a lower bits and easy cell parts are realized in the analog circuit of delta-sigma modulator [8]. As the delta-sigma modulator has especially tolerant to circuit non-idealities and component mismatch, it is could be achieve higher accuracy [9].

In the circuit level design, Delta-Sigma modulator is consisted with low-pass filter and quantizer, the sampling signal is sent into the quantizer, and then output after quantification. Because of the oversampling frequency that higher than Nyquist frequency is used in the Delta-Sigma modulator, the sample-hold circuit is not required exactly. At the same time, analog anti-filter is cut down [10].

In the modulator loop, the quantizer quantify the noise, the quantification noise is pushed out the higher frequency that out of the bandwidth by the low-pass filter. And then the quantization noise which out of bandwidth was removed by low-pass filter after the delta-sigma modulator. Except to considerate the non-ideal factors, the various barriers of analog circuit must be reduced as far as possible.

In this thesis, a feed forward two order Delta-Sigma modulator is designed. It is composed with two filters, a 1bit quantizer and DAC. The delta-sigma modulator had been argued completely which had been designed from behavior level to circuit level in this essay. The next article will declare the design theory of delta-sigma modulator, and the third part would be argued the design and simulation of the behavior level. The forth part of paper would be described the design and simulation of the circuit level, the most important technical is that the circuit design is based on 0.5 μm CMOS process. At the last of the paper, the design results and performance analysis of delta-sigma modulator would be illustrated.

2. Principle of Delta-Sigma Modulator

It is the most important breakthrough that delta-sigma modulator is adopted the oversampling frequency, it greatly higher than Nyquist frequency. After sampling, the output signal is compared with sampling value of the last moment. The differential value is quantified, and then modulator output the low bit code, according to the output of quantizer decide which value of feedback will be returned.

The simplest form of delta-sigma modulator structure combines a low-pass analog filter consisting of a single integrator with a 1-bit quantizer [11-12]. The block diagram of delta-sigma modulator is shown in Fig. 1 [13]. Through the above analysis we can get that the number of order and integrator are equally. Therefore, for the L order model, the output of modulator [14] in Z-domain is:

$$Y(z) = z^{-L}X(z) + (1-z^{-1})^{L}E(z), \quad (1)$$

where X(z) is the input signal, Y(z) is the output signal, E(z) is the quantization noise.

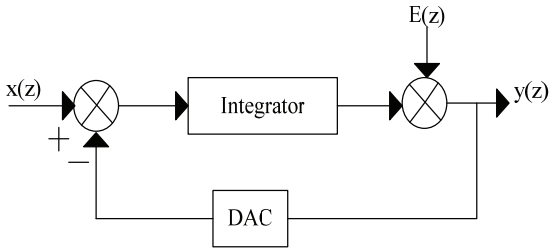

Fig. 1. Delta-Sigma modulator frame chart.

The oversampling is measured by OSR, accordingly $OSR = F_s / (2f_b)$, wherein f_b is Nyquist frequency, F_s is oversampling frequency. The quantizer is acquiesced unit quantizer, the Dynamic Range (DR) [15] is described in equation (2):

$$DR \approx \frac{3}{2} \cdot \frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}} \quad (2)$$

Turn (2) to dB, that is shown in formula (3):

$$DR|_{dB} \approx 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10\log_{10}(OSR) \quad (3)$$

For aforementioned formulas, we can get that increase the number of order and oversampling Rate (OSR), the DR will be raised and the efficiency bits will be enhanced at the same time, $R = (DR - 1.76)/6.02$. For an ideal model of L order Delta-Sigma modulator, the highest SNR could be expressed in formula (4):

$$SNR = \frac{3\pi}{2}(2^R - 1)^2(2L+1)\left(\frac{OSR}{\pi}\right)^{2L+1} \quad (4)$$

The oversampling ratio required to meet a specific level of performance may be decreased below that needed in a second-order delta-sigma modulator by increasing the order of the modulator. Higher order noise shaping can be accomplished by including a higher order filter, such as additional integrators, in the forward path of the modulator.

3. Modulator Architecture

A species of two-order delta-sigma modulator could be used in Audio system, which is hoped design in this paper. Expected accuracy arrive to 14 bit, SNR is 90 dB. The architectures of two-order feed forward Delta-Sigma modulator without local feedback path are chosen in this paper. The idea behavior level model of second-order Delta-Sigma modulator is shown in Fig. 2 that consists of two sampled-data integrators, a 1-b A/D converter, and a 1-b D/A converter. In the ideal model, the higher SNR, higher resolution and the higher speed etc. could be achieved easily. But actually, there must be a lot of non-ideal factors in the practical model, for example KT/C noise, clock jitter, and op-amp noise etc. therefore, to make the simulation results are more closed to the real application that the typically non-ideal factors are imitated at the input of Delta-Sigma modulator. The non-ideal Feedforward two-order Delta-Sigma modulator is shown in Fig. 3.

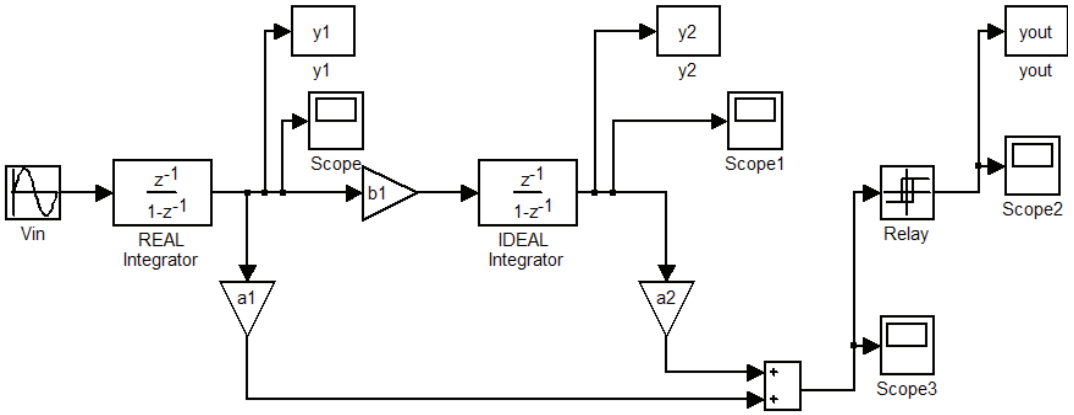

Fig. 2. The ideal feedforward two-order Delta-Sigma modulator.

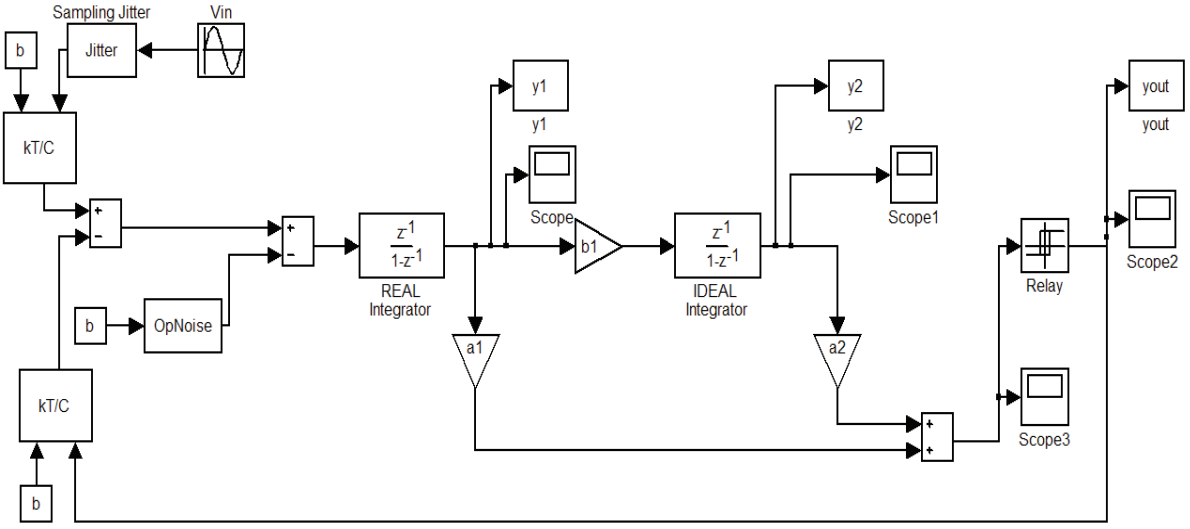

Fig. 3. The non-ideal Feedforward two-order Delta-Sigma modulator.

The first stages must have large capacitances to satisfy the SNR requirement, and the performance requirements of first integrator are rigorous than the other integrator. Therefore the op-amp for the first stage becomes power consuming design to drive large capacitances with sufficient speed. The noise shaping requirement on the second stage is far smaller than the first stage, because of that the quantization noise would be eliminated by noise shaping technique, required capacitances on the second stage is smaller than the first stage [16]. For reduce the design time and workload, the affect of whole modulator with several of non-ideal factors must be considered in detail.

At the initial stage of behavior level, according to the block diagram of two-order delta-sigma modulator draw out the equation of transfer function, Signal Transfer Function (STF) and Noise Transfer Function (NTF), compare with the equation which is synthesized by MATLAB, then ensure the coefficients of open loop: a_i and b_i. Secondly, build a completely structure of feedforward two-order delta-sigma modulator with Simulink.

The ideal model of delta-sigma modulator is simulated. The PSD curve is shown in Fig. 4. From the ideal results that we can get the SNR is more than 100 dB, the resolution is more than 16 bit and other results are also satisfactory.

For the non-ideal model of delta-sigma modulator, the KT/C noise, jitter noise and op-amp noise etc non-ideal factors are analyzed and added to the input of modulator. Ultimately, the value of SNR and efficiency bit are calculated, the simulation result is shown in Fig. 5. That the SNDR is 94.7 dB and the resolution arrived to 15 bits. Compare with the ideal results, the SNR of the non-ideal model is reduced to 94.7 dB, there are 8.3 dB consumption. But from the behavior level results we had got that the design is also suitable the expectation results.

3. Circuit Implementation

Among the modulator architectures discussed in the previous section, second-order Delta-Sigma modulators are particularly attractive for digital-audio signal acquisition because of their stable operation and tolerance of circuit non-idealities. All the elements of the second-order delta-sigma modulator shown in Fig. 3, which are ready implemented with switched capacitor circuit techniques. Fig. 6 shows a fully differential implementation of the two order delta-sigma modulator, which consisting with two identical parasitic insensitive switched capacitor integrators, a comparator, and a distributed two-level D/A converter. The use of a fully differential configuration attenuates power supply noise, clock feed through, and even-order harmonic distortion. Additionally, the differential architecture doubles the dynamic range of the modulator, which is especially important when using a single 5-V power supply.

The CMOS switch circuits and NMOS switch circuits are used in the modulator circuit. The system supply voltage is 5 V and the reference voltage of DAC is 2.5 V. According to the design, analysis and simulation of the behavioral level of feedforward two order delta-sigma modulator, we can get that the feedbach coefficients of modulator are $C_{S1}=C_{S2}=0.2C_F$, $C_{b1}=0.3C_F$, $C_{b2}=0.08C_F$. The differences of operation speed enable the operational amplifier sharing among the two stage integrators.

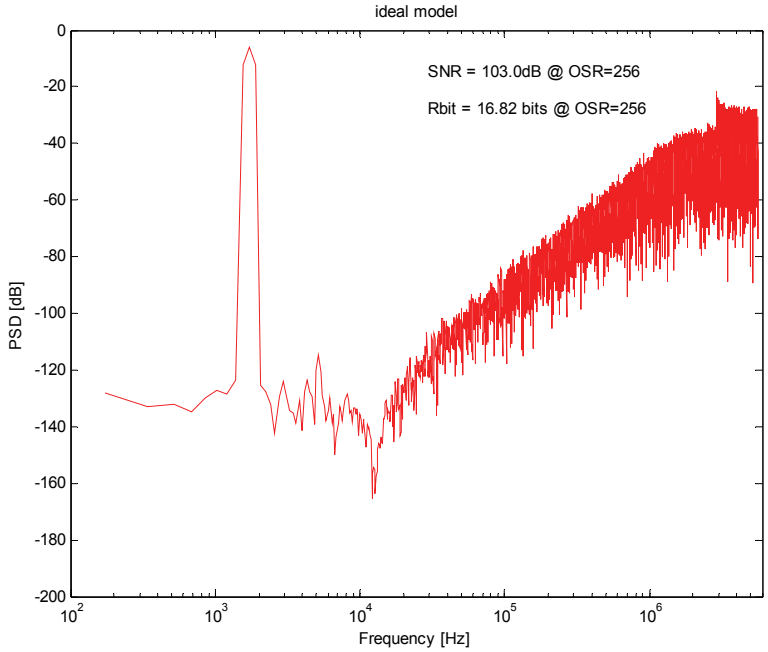

Fig. 4. The PSD curve of ideal model.

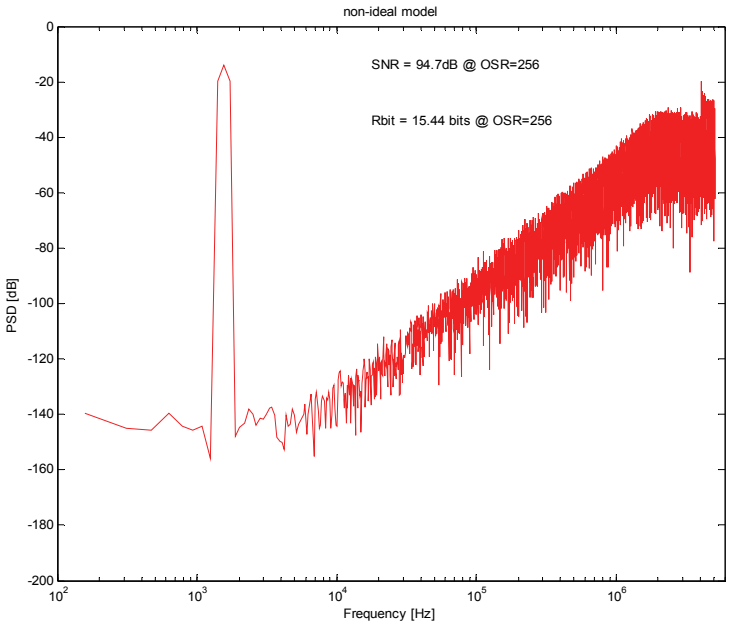

Fig. 5. Simulation result of non-ideal model.

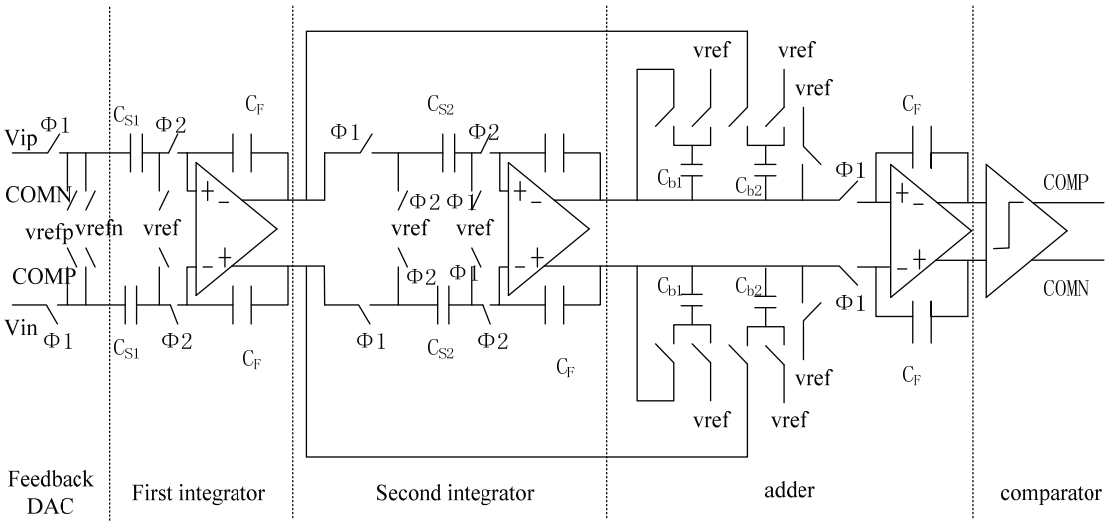

Fig. 6. The circuit structure of two-order Delta-Sigma modulator.

The hold mode period of the second and the third stage is half of the first stage. This short hold mode period is achieved by the differences of the stage characteristics. Therefore, the hold modes of the two integrator stages without an overlapped period in a T_{sample} clock cycle can share an operational amplifier. In this thesis, the two order delta-sigma modulator is operated on a two-phase non-overlapping clock circuit as the structure is detailed in Fig. 7.

3.1. Fully Differential Op-amp

The operational amplifier used in the integrators is the most critical element of the single feed forward two order delta-sigma modulator, in this paper. But the second integrator is looser than the first integrators, which because the second integrator is in the loop of the delta-sigma modulator, and the most quantize noise are shaped. In conclusion, the requirement of op-amp in the second integrator is lower than the first ones, and the design is more easily. As it was discussed in the previous section, the settling time of operational amplifier should not be limited by slewrate. From the simulations, it is indicated that a slewrate of 200 V/μs is sufficient to meet the performance objectives. For reduce the harmonic distortion, and decrease the non-linearity of the amplifier, the fully differential structure is adopted in the circuit design of integrator.

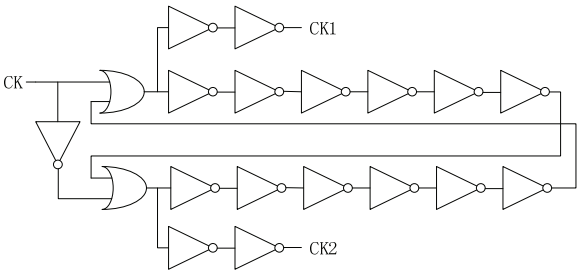

Fig. 7. Two non-overlapping clock circuits.

To get higher gain, wider bandwidth and higher speed, the two stage operational amplifier is adopted, and the first stage of the operational amplifier is the structure of telescopic cascade. It is not only enhanced the gain, but also raised the output slewrate and unit gain bandwidth. As we know, the switch-capacitor of Delta-Sigma modulator is worked in discrete time. The signal is sampled at the Φ2 phase, filter complete charge metastasis by op-amp. Thus, the amp must own higher voltage transfer rate, faster settling time and lower amplifier noise [17-18]. In this essay, the clock period is 97.66 ns, so the filter settling time must be less than half of clocking period—48.83 ns.

The gain of amplifier is required to less than 80 dB in the paper, so the first stage is telescopic cascade amplifier and the second stage is common source amplifier, which could be raised the gain, the unit gain bandwidth and output slew. The structure of two stage operational amplifier is shown in Fig. 8. Since the output slew is enhanced, the overload of filter is limited and the dynamic range of modulator is greatly raised at the same time. For this reason, the high speed, high gain, high gain bandwidth and wide output slew amplifier could be realized as we hope [19].

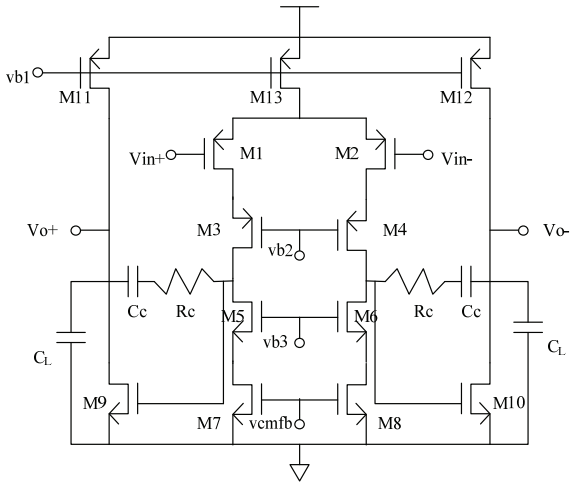

Fig. 8. Two-stage op-amp.

In Fig. 7, Cc is compensation capacitor, and Rc is compensation resister. The operational amplifier could be worked in stable with the pole-zero compensation. The two stage amplifier in Fig. 6 is simulated and analyzed with the Cadence spectre, under the 0.5 μm CMOS process. The simulation results are shown in Fig. 9. Those results shown that the amplifier gain is 82 dB, phase margin is 71.34°, the others simulation results are shown in Table 1.

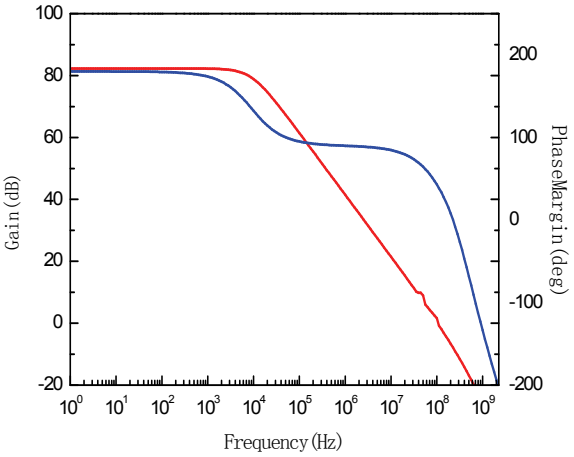

Fig. 9. AC simulation result.

Table 1. The simulation results of the two-stage op-amp.

Gain	82.3 dB
PhaseMargin	71.34°
SR	202 V/μs
Settling time	43 ns
GBW	102 MHz
CMRR	93.4 dB
PSRR	96.7 dB

3.2. Quantizer

The quantizer of Delta-Sigma modulator is consisted of comparator and SR latch. The structure of quantizer is shown in Fig. 10. Since the comparator can be designed to be quite fast, the settling speed of the integrator ultimately limits the achievable sampling rate of the modulator, even if complete settling is not required.

The need for high speed, coupled with a relatively modest gain requirement of 60 dB to suppress harmonic distortion, encouraged the use of a single stage amplifier. Constrain of a single 5-V power supply dictated a low-noise, large output swing architecture. This operational amplifier provides a large output current and output voltage range while maintaining a gain comparable to that of alternative single stage designs.

The performance of the modulator is relatively insensitive to comparator offset and hysteresis since the effects of these impairments are attenuated by the same two-order noise shaping that attenuates more quantization noise, which in the bandwidth. The SR latch, after the comparator is shown in Fig. 8, which has been used to implement the quantizer. The SR latch is reset during Φ1 and the result of each comparison is stored in Φ2.

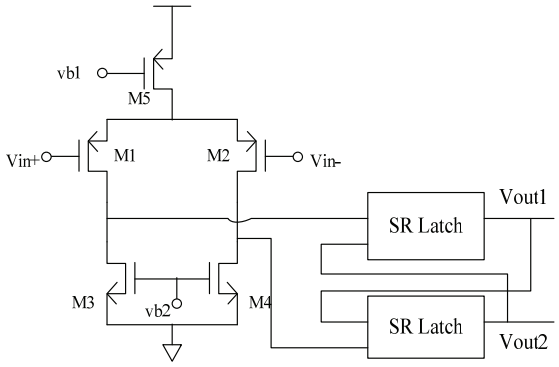

Fig. 10. Quantizer.

3.3. Simulation Results

The feedforward two order delta-sigma modulator of Fig. 3 has been fabricated in a 0.5 μm CMOS technique with capacitors. The performance of the two order delta-sigma modulator was evaluated by driving its input with a high quality differential sinusoidal signal source, acquiring its 1-bit output code, and transferring the acquired data to a workstation for subsequent processing.

The frequency of the input sine wave is 3.5 KHz and the delta-sigma modulator sampling rate is 10.24 MHz at an oversampling ratio of 256. The modulator achieved a 110 dB dynamic range and a peak SNDR of 93.1 dB. The PSD curve of the non-ideal delta-sigma modulator is shown in the Fig. 11. When compared to the ideal spectrum, it is seen that the dynamic range of the experimental modulator is not limited by quantization noise. Indeed, an ideal second order delta-sigma modulator achieves a 110 dB dynamic range. Analysis indicates that the cause of the experimental modulator's increased noise floor at low frequencies is flicker noise in the first operational amplifier. Flicker noise was controlled simply by increasing the gate area of the transistors in the operational amplifiers. Special techniques such as chopper stabilization could be employed to further increase the dynamic range. The SNR of circuit-level of delta-sigma modulator is consummated about 1.6dB. But it is also satisfied the expectation, in conclusion, the two-order delta-sigma modulator could be used in digital Audio etc.

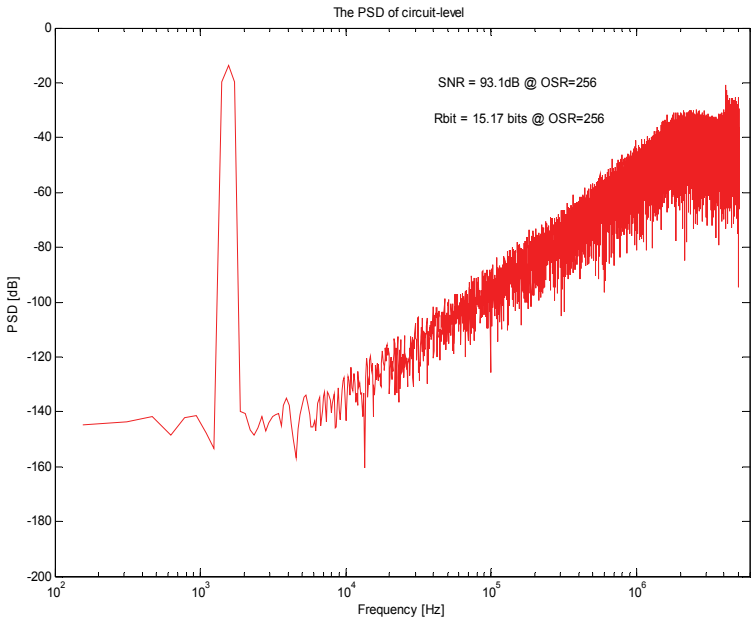

Fig. 11. The PSD curve of delta-sigma modulator.

4. Conclusions

In this paper, the principle of the modulator, and the whole process of design and analysis of two order delta-sigma modulator is described in detail. Therefore, we can get that two-order delta-sigma modulators efficiently exchange the high speeds of CMOS VLSI technique for high analog resolution without sacrificing modulator stability or placing severe constraints on the precision of the analog circuits.

Because of oversampling and noise shaping techniques are used, delta-sigma modulator is more stable, and have higher SNR, which have low power consumption, high speed, high resolution, and so on advantage properties. A principle concern with the use of two order delta-sigma modulator is the presence of discrete noise peaks, or tones in their output spectrum for certain inputs. Simulations and measurements have shown that the SNDR is 93.1 dB at an oversampling ratio of 256, the DR is arrived to 110 dB, and power consumption is lower than 186 mW, those results beyond the expected results.

An experimental implementation has demonstrated that a feed forward two order delta-sigma modulator could provide digital audio signal acquisition in a 0.5 μm CMOS technique. A more difficult task would be reduced the device noise, such as both thermal and flicker, offset the non-idea factors, for instance non-linear of operational amplifier, clock jitter, etc., at the input of the delta-sigma modulator. Those are the problems common to all high resolution CMOS A/D converters. It is also an urgent problem to dispose, for delta-sigma modulator.

Acknowledgements

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