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Design of a New Random Equivalent Sampling Technology Based on Vernier Method

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Abstract: Random equivalent sampling technology was used to solve the high cost of high speed data acquisition issue. Random equivalent sampling uses multi-sampling technology to convert high-frequency periodic or quasi-periodic signals to low-frequency ones. This technique while is based on the vernier caliper principle is realized by measuring the interval of the trigger point and the first sampling pulse of the next sampling period, the equivalent sampling rate can be up to 10 GSps. It includes the trigger clock generator module, the sampling clock generator module, the equivalent time sampling measurement module and the data storage module. This technique has highly practical value and has been applied to the portable digital Storage oscilloscope. *Copyright © 2013 IFSA.*

Keywords: Random equivalent sampling, Vernier Method, Trigger signal, Digital Storage Oscilloscope, Reconstructed waveform.

1. Introduction

With the rapid development of digital technology, the acquisition of high-frequency signals gradually increased, but because of the limitations of the existing components, the low-speed analog-to-digital converter is difficult for real-time acquisition of high-frequency signals. Therefore, the equivalent sampling technique is used to solve this problem. This technology can achieve digitization of periodic signal or quasi-periodic signal and reconstruct original one by multi-sampling data. It is achieved by using the periodicity of the signal and relies on reducing the sampling rate to increase the acquisition time [1-3]. Equivalent sampling is not easy to achieve for portable digital storage oscilloscope (DSO), because of its low power consumption, low cost and small circuit board area requirements. The application of traditional capacitor charging and discharging technique is not advisable. This new idea and innovative point based on vernier caliper principle achieves the random equivalent sampling (RES) technology by using FPGA and a small number of integrated devices.

2. Random Equivalent Sampling

The equivalent sampling has sequential equivalent sampling and random equivalent sampling. The principle of sequential equivalent sampling was given in Fig. 1. The sequence of the sampling points' acquisition is fixed. The first sample point is immediately collected after the arrival of a triggering event, and is stored in the memory. When the second triggering event arrives, a delay system

will work, this delay system will generate Δt delay , then the Second sample point will be collected; When the third triggering event arrives, the delay system will generate $2\Delta t$ delay, then the third sample points will be collected, And so on, displayed waveform is constituted by a fixed order sampling point, the first sampling point is on the left-most of the screen, and then each sample point sequence constituting the displayed waveform to the right. The disadvantage of this method has no pre-trigger information.

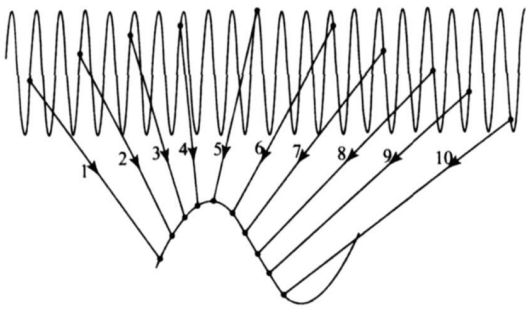

Fig. 1. Sequential equivalent sampling diagram.

RES can provide pre-trigger and trigger information as well as triggered information. The basic principle of RES was given in Fig. 2. Given a repetitively signal will be sampled as shown in the diagram on the top row, the sampling clock is taken by the immediate sampling pulse after the sampling signal. The interval time between all the sampled data is the sampling period. When the DSO is waiting for a trigger event, A/D converter was continuous acquisition and the sampled data was stored. The time between the trigger point and the first sampling pulse of the next sampling period was measured when the trigger event arrives. The time of all the sampled data relative trigger time will be deduced by the sampling period and the time between the trigger point and the first sampling pulse of the next sampling period. After a number of the above process, the waveform can be reconstructed. The key of RES is the measurement of the time between the trigger point and the first sampling pulse of the next sampling period [4-7].

The time between the trigger point and the first sampling pulse of the next sampling period was obtained by vernier caliper [8], as shown in Fig. 3. T1 is the cycle of sampling clock, T2 is the cycle of triggering clock, and the frequency of T1 is less than T2. This two clocks were counted, when the two clocks have the same phase, if T1 of counting to n1, T2 of counting to n2, then the time between the trigger point and the first sampling pulse of the next sampling period is measured as

$$t = n_2 \times T_2 - n_1 \times T_1 \tag{1}$$

The implementation of RES not only achieves its logic function, but also considers its data collection and storage [9, 10]. Its structure was given in Fig. 4. The sampling data will be stored in internal memory cell of the FPGA with the sampling clock frequency that will be read by microprocessor. The implementation of RES mainly depends on the module to measure the time. This time is between the trigger point and the first sampling pulse of the next sampling period. The signal is continuously sampled by 101.01 MHz, when the trigger point comes immediately to start the trigger clock, the measurement module of equivalent sampling will calculate the time which is between the trigger point and the first sampling pulse of the next sampling period by the principle of vernier caliper.

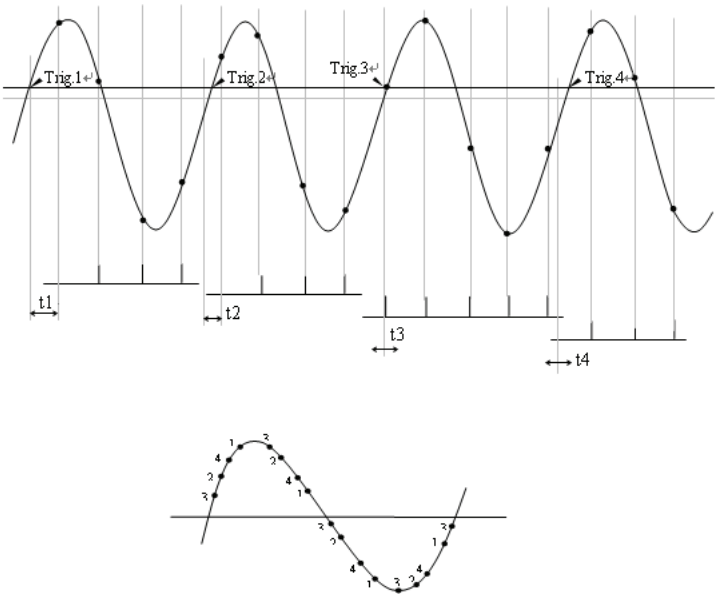

Fig. 2. Random equivalent sampling diagram.

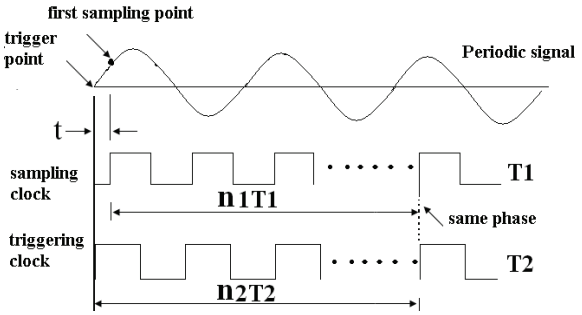

Fig. 3. The vernier caliper law principle diagram.

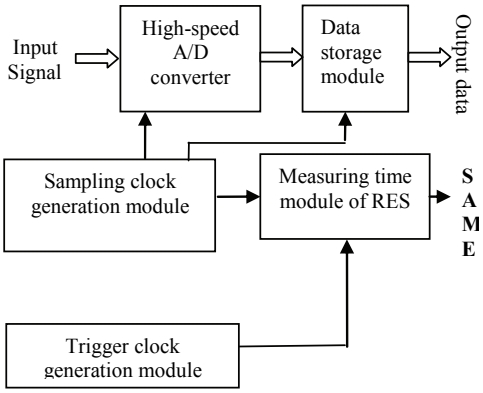

Fig. 4. The structure of RES diagram.

3. Researches

3.1. Trigger Clock Generation Module

Based on the vernier caliper principle, trigger clock is equivalent to the scale of the vernier caliper. The key of trigger clock is immediately starts, when trigger point comes on. The CDC421A100 is a high-performance, low-phase-noise clock generator. It has an integrated low-noise, LC-based voltage-controlled oscillator (VCO) that operates within the 1.75 GHz to 2.35 GHz frequency range. It will be used to generate 100 MHz single for trigger clock. CE controls its output's clock time that is less than 35 ps, when CE is high. Trigger clock generation module as shown in Fig. 5.

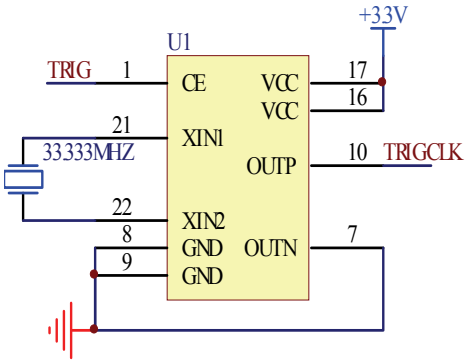

Fig. 5. Trigger clock generation module.

3.2. Measurement Time Module of RES

When the system enters RES, the sampling clock is always keeping a fixed frequency (101.01 MHz). When the input signal meets the trigger condition, the trigger signal immediately drives the trigger clock generation module to start up. Phase monitoring module is used to detect a trigger clock with sampling clock to same phase, while the system was counting these two clocks. When there are same phases, the time of between the trigger point and the first sampling pulse of the next sampling period will be calculated according to counting value of two clocks, thereby by deducing the time relationship of all the sampling points and trigger timing, waveform will be reconstructed.

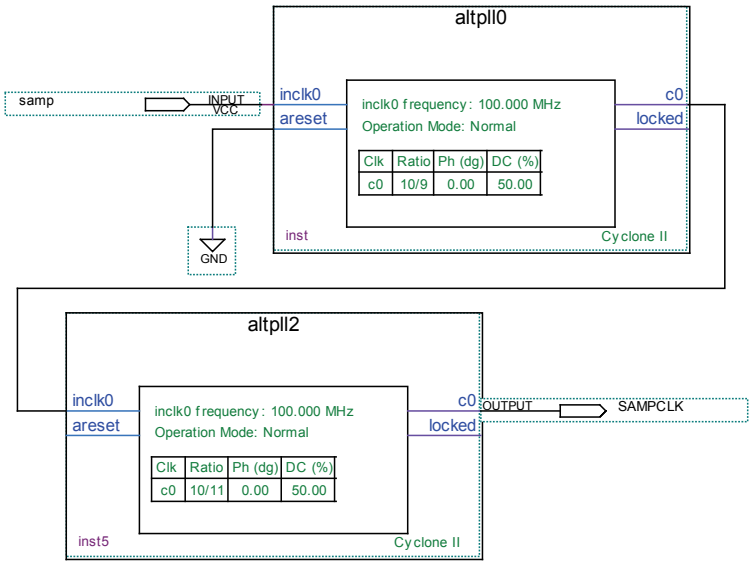

Fig. 6. Sampling clock generation module.

The measurement module of Equivalent sampling used vernier caliper principle, because trigger clock's frequency is 100 MHz, two phase-locked loops (PLL) in the EP1K30QC208-3 of Altera can be used to generate sampling clock, as shown in Fig 6.Trigclk is input clock, its frequency is 100 MHz. The setting of first PLL is 10/9 of the relationship between the input signal and the output signal, second PLL sets 10/11 relationship of input signal and output signal. These two PLL are series of relations, and then the input signal SAMPCLK is 101.01 MH_Z as sampling clock. When the input signal meets the trigger condition, the trigger signal immediately drives the trigger clock generation module to start up, the difference of phase between the sampling clock and trigger clock can be measured by phase monitoring module. After 0 to 100 clocks, trigger clock must be the same phase as the sampling clock, so equivalent sampling rate will achieve 10 GSps. Phase monitoring module and simulation diagram were given in Figs.7, 8.

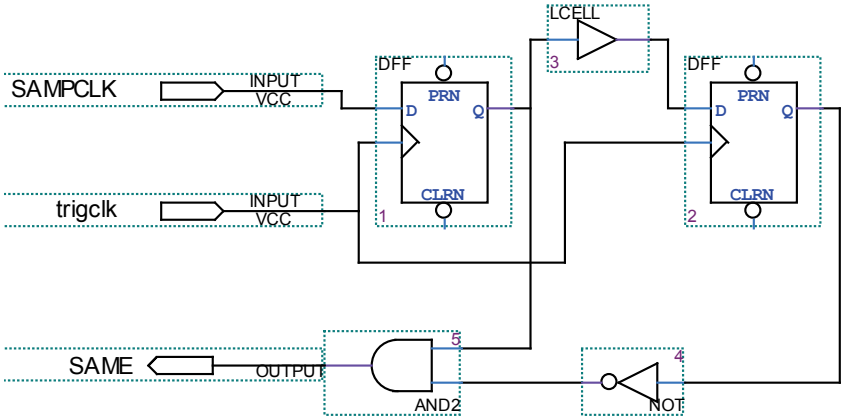

Fig. 7. Phase monitoring module.

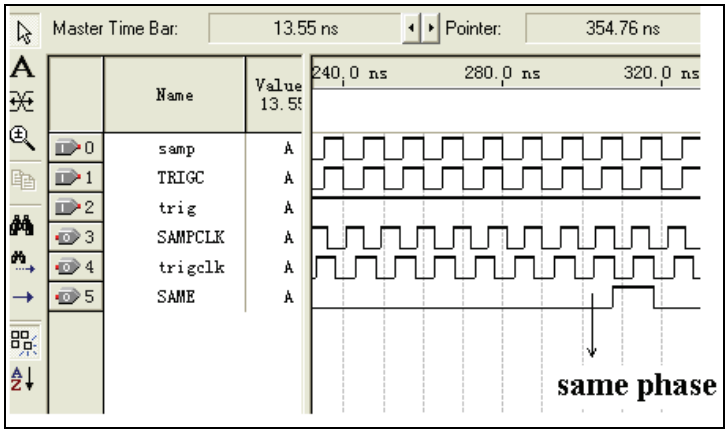

Fig. 8. Simulation diagram.

3.3. Data Storage Module

The data storage module stored the output data on request of the A/D converter that is mainly depend on the internal logic unit of the FPGA to complete the peak value sampling and storing. Maximum peak value sampling schematic diagram was given in Fig. 9. It includes two pieces of D trigger 74273, two pieces of the 8-bit selector 2 × 8 mux, an internal memory of FPGA LPM_RAM_DP, and a piece of 8-bit comparator LPM_COMPARE.

The labels 1 trigger 74273b latched CHA_D [7...0] data of high speed A/D converter output by 100 MHz latch clock /CLK_RTN with same sampling clock. The 8-bit comparator LPM_COMPARE compares dataa and datab, when the datab group data is greater than dataa, output agb sets 1.LPM_RAM_DP is a RAM in FPGA, its data storage address is generated by the counter sampling clock, and the storage pulse TRANS_LATCH frequency determines the peak value sampling depth that decided after comparing the number of points to store peak value. The frequency of the stored pulses is lower than the sampling clock, and if the stored pulses are more lower than the sampling clock, it compares more data in the same time and the stored data is relatively less, the stored pulses determined by

time base are usually less than 20 MHz, Therefore, an effective maximum value comes to five points at least will be stored. The SEL control terminal of 8-bit selector 2 × 8 mux is generated through the output of OR gate by TRANS_LOAD and agb. TRANS_LOAD is the same signal as the storage pulse, and its duty cycle is 0.2, this signal will store the first sampling signal as the default maximum. After that, the SEL signal will be controlled by the agb that is used to store the compared maximum value obtained every time by the labels 2 trigger 74273b, this 74273b used to give the pre-compared-maximum value to the comparator LPM_COMPARE, its frequency of latch clock CLK_100M_H is equal to the frequency of the sampling clock, which is 100 MHz, but their phase difference is 180° to store data through the comparison latched.

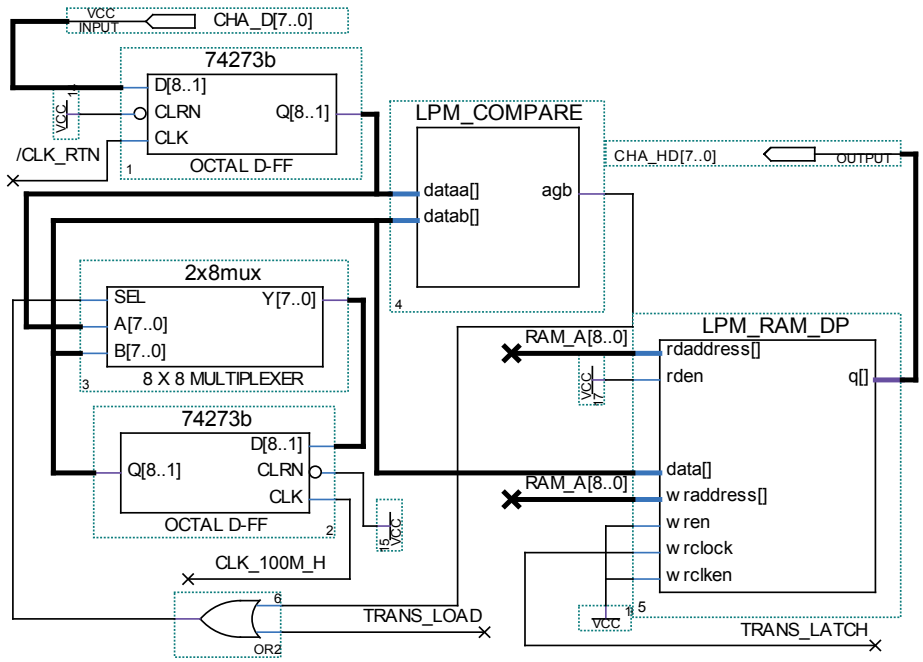

Fig. 9. Maximum peak value sampling schematic.

4. Experimental Results

When the settings of the time base is less than 1 μs, the system begins the equivalent sampling, microprocessor sends control commands to FPGA for receiving the sampling data, the address of RAM is generated by 20 MHz clock. Before the arrival of the trigger signal the collected data were stored to the frontal 256 bytes of RAM. When the 256 bytes of RAM is full, the trigger signal will be allowed to be generated. If valid trigger signal and trigger signals are valid, the time between the trigger point and the first sampling pulse of the next sampling period will be measured. The hinder 256 bytes of the RAM will be used to store sampling data which was sampled after the trigger signal arrived. When the RAM memory is full, all the sampled data will be read, the time between the trigger point and the first sampling pulse of the next sampling period has been measured to calculate the interval of all sampled data relative to triggering time. After a number of the above-mentioned process, the microprocessor can reconstruct waveform based on the needs of users. Reconstructed waveform is shown in Fig. 10.

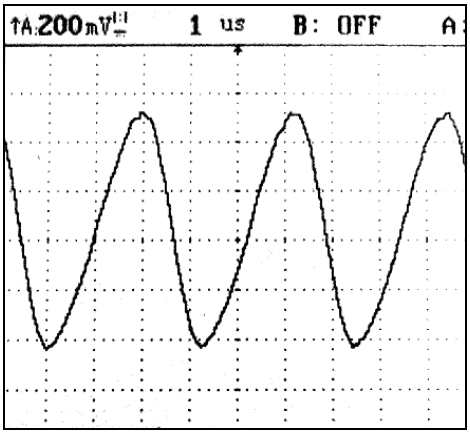

Fig. 10. Reconstructed waveform.

5. Conclusions

The RES module is proposed for sampling and reconstructing high frequency signal. The RES sampling rate can reach 10GSps in the portable DSO, this technology has been successfully used in the WX4452 portable DSO, and achieved good results.

Acknowledgements

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