Translation Lookaside Buffer on the 65-nm STG DICE Hardened Elements

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***Abstract* — This paper presents the design of hardened translation lookaside buffer based on Spaced Transistor Groups (STG) DICE cells in 65-nm bulk CMOS technology. The resistance to impacts of single nuclear particles is achieved by spacing transistors in two groups together with transistors of the output combinational logic. The elements contain two spaced identical groups of transistors. Charge collection from particle tracks by only transistors of just one of the two groups doesn't lead to the cell upset. The proposed logical element of matching based on the STG DICE cell for a content-addressable memory was simulated using TCAD tool. The results show the resistance to impacts of single nuclear particles with linear energy transfer (LET) values up to 70 MeV×cm2/mg. Short-term noise pulses in combinational logic of the element can be observed in the range of LET values from 20 to 70 MeV×cm2/mg.**

***Keywords* — content-addressable memory, logical element, memory cell, noise immunity, single nuclear particle, topology.**

I. Introduction

THE translation lookaside buffer (TLB) is used to speed up the virtual-to-physical address translation. The power consumed by TLB is a significant part of the power consumed by the microprocessor as a whole [1]. Failures in TLB with high probability manifest themselves at the system level [2], [3]. They result in user-visible errors with a probability of over 30% [2]. Software and algorithmic methods [2], [4] can reduce this probability by only 20-50%, but not eliminate.

CMOS logical elements of matching for a content-addressable memories (CAM) are currently constructed on 6T memory cells and "Exclusive OR" logic gates. The cells [5], [6] suggested for the ternary content-addressable memory do not solve the problem of fault tolerance in content-addressable memories that work under the influence of nuclear particles. The hardened ternary CAM cell designed in [6] consists of CMOS 6T memory cells which is why problems of data upsets under impacts of single nuclear particles still remain.

The new approach to hardening TLB's design against impacts of single nuclear particles is based on the novel circuits developed using STG DICE cell. The STG DICE memory cell (Spaced Transistor Groups DICE) [7], [8] is distinguished from the DICE (Double Interlocked Cell) [9] in that its transistors are separated into two groups. The charge collection from the tracks of single nuclear particles by transistors of just one group does not lead to the cell upset. The purpose of this work is to design TLB on hardened elements resistant to single nuclear particles.

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II. The Basic Blocks of the Translation Lookaside Buffer

The translation lookaside buffer (Fig. 1) contains the 64-words content-addressable memory array (CAM) and the 64-words random access memory array (RAM). The input "Register selection" of the decoder (DEC) sets the number of the register to write or read data. The block of read and write buffers (R/W BUF) includes write buffers and sense amplifiers for the CAM and the RAM. The control logic (CONTROL) provides clock and control signals in the TLB. The encoder (ENCOD) indicates the search result (hit or miss) and shows the number of the register in which the data matched.

Each register of CAM contains [10] three blocks of matching (BM) and two blocks of masking and matching (BMM). The block of matching (Fig. 2a) includes four double CAM cells ("2 CAM cells") and decoder 8NAND of the output bits of matching. Each block of matching and

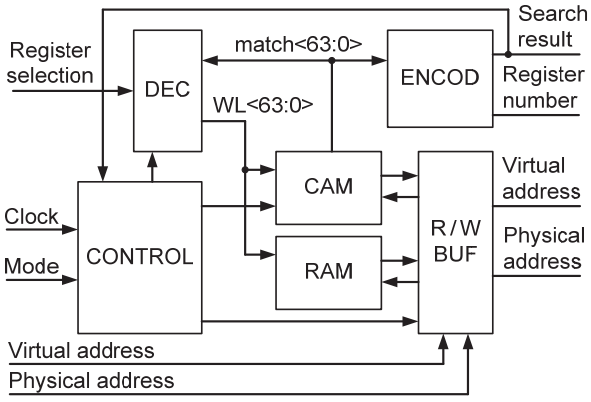


Fig. 1. The diagram of the translation lookaside buffer.

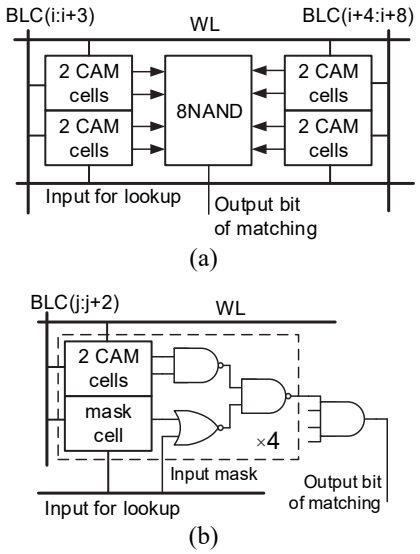


Fig. 2. The main blocks of CAM registers: (a) – the block of matching (BM); (b) – the ¼ part of the block of matching and masking (BMM).

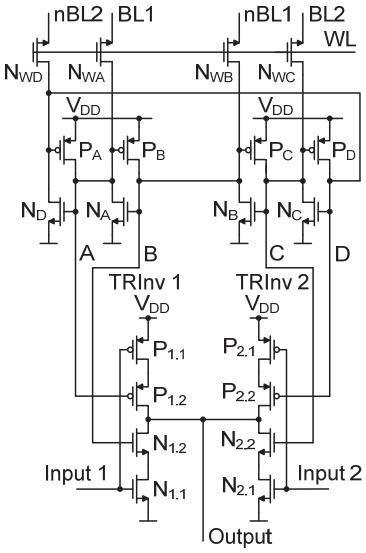


Fig. 3. The element of matching based on the STG DICE cell and the "Exclusive NOR" logic gate on two tristate inverters TRInv 1 and TRInv 2.

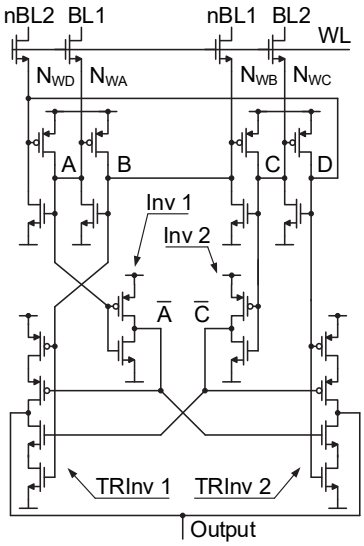
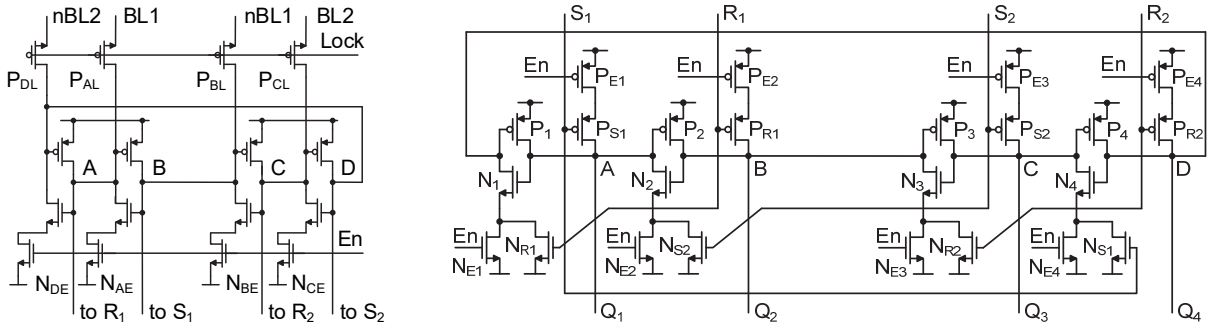


Fig. 4. The scheme of the memory element for masking with the combinational circuit for correct data reading in steady and unsteady states of STG DICE nodes.



(a) (b)

Fig. 5. The scheme of the latch-type sense amplifier based on the STG DICE cell and the synchronous STG RS-latch: (a) – trigger on the STG DICE cell; (b) – the synchronous STG RS-latch clocked by the enable signal En.

masking (BMM) includes four "2 CAM cells", four mask cells as two "2 mask cells" and the combinational logic for combining match outputs and bits of the input for lookup. Fig. 2b shows the ¼ part of the block BMM.

III. Schemes of the Hardened Elements

The element of data matching for associative memories [10] was developed using the STG DICE cell. Interleaving [11] of transistors groups belonging to adjacent STG DICE cells allows to increase the distance between the mutually sensitive pairs of transistors of the one cell and to improve fault tolerance. In the previous work [12] the simulation of the noise immunity was carried out using the SPICE models of transistors.

Experimental studies [13] demonstrate the fault tolerance of 65-nm STG DICE cells compared with the 6T memory cells and standard DICE cells during collection of charge generated by laser pulses. TCAD simulations [14] confirm the high fault tolerance of the STG DICE cell during charge collection from tracks of single nuclear particles.

Fig. 3 demonstrates the scheme of the element of matching on the STG DICE cell and the "Exclusive NOR" logic gate, which consists of two tristate inverters TRInv 1 and TRInv 2. This element of matching is a half of unit "2 CAM cells" in Figs. 2a, b. The placement of the one group of the STG DICE cell and the one tristate inverter together into the joint group (see the Sect. V) provides the possibility of minimum effect of a single particle impact on the cell.

The charge collection from tracks of single nuclear particles in one of the STG DICE transistors groups inside the element of matching does not lead to a failure at linear energy transfer values up to 70 MeV×cm2/mg, but may lead to a temporary unsteady state of STG DICE cell [15].

Fig. 4 shows the scheme of the memory element for masking with the combinational circuit for correct data reading during steady and unsteady states of STG DICE nodes. The reading circuit consists of two tristate inverters TRInv 1, TRInv 2 and two normal inverters Inv 1, Inv 2. When STG DICE cell is in an unsteady state caused by a particle impact, the reading circuit forms the correct output signal.

TABLE 1 PARAMETERS OF THE BASIC ELEMENTS FOR THE CONTENT ADDRESSABLE MEMORY REGISTER

Basic element	BM	BMM	2 CAM cells	2 mask cells	8-input NAND
Dimensions (μm×μm)	4.74×23.24	4.74×39.71	2.37×9.48	4.74×6.16	4.74×4.28
Element's area (μm^2)	110.15	188.22	22.47	29.19	20.29
Number of transistors	196	316	40	48	36
Number of base elements in CAM register	3	2	20	4	3
Portion of the area of CAM register (%)	44	50	59	15	8

TABLE 2 PARAMETERS OF THE BLOCKS

Block	CAM	RAM	DEC	ENCOD	R/W BUF	CONTROL
Dimensions (μm×μm)	303×158	303×86	303×10	303×24	50×239	23×29
Block area (μm^2)	47874	26058	3030	7272	11950	667
Portion of TLB area (%)	48	27	3	7	12	0.7
Number of transistors	75136	46080	3288	720	19500	367
Write power consumption (mW)	17.87	0.46	0.94	0.00004	16.21	1.86
Search power consumption (mW)	27.54	0.05	1.40	2.06	9.17	2.91
Read power consumption (mW)	1.16	0.05	4.15	0.00008	11.82	2.77

The correct reading is provided by unchangeable logic levels of two from four nodes A, B, C, D. These two nodes keeping their initial logic levels belong only to the group of transistors that does not collect the charge from the track of a nuclear particle. The charge collection at linear energy transfer values up to 70 MeV×cm2/mg leads to no data upsets of the memory element for masking [14].

Fig. 5 presents a latch-type sense amplifier consisting of the trigger on STG DICE cell (Fig. 5a) and the synchronous STG RS-latch (Fig. 5b). It's clocked by the enable signal En. Fig. 5b presents the scheme of the STG RS-latch [16] on four pairs of Ni and Pi transistors (i = 1; 2; 3; 4), which are in the identical state - closed or open as in STG DICE cell; S_1, S_2, R_1, R_2 – set inputs and reset inputs, Q_{11}, Q_{12}, Q_{21}, Q_{22} – outputs of the STG RS-latch. The latch-type sense amplifiers are used in the CAM and the RAM arrays for data reading out of the bit lines.

TCAD simulation [16] of the STG RS-latch shows that the threshold linear energy transfer value LET_{THR} is 55 MeV×cm2/mg in case when no interleaving of groups is applied, and LET_{THR} value exceeds 100 MeV×cm2/mg when interleaving of groups is used.

We try to improve the reliability of STG-type elements using the common approach: the separation of the transistors of such logical elements into two groups (or blocks), and subsequent interleaving of these groups belonging to the adjacent logical units [10].

IV. THE PARAMETERS OF ELEMENTS AND BLOCKS

Table 1 presents the parameters of the block of matching and the block of matching and masking, which cover 94% of the CAM-register's area. In units "2 CAM cells" and "2 mask cells" we use interleaving of the joint groups of the transistors to increase the minimum distance between the sensitive nodes of STG DICE cell. It provides the minimum distance of 4.15 μm for the unit "2 CAM cells" and of 3 μm for the unit "2 mask cells".

In the RAM array we use interleaving of groups belonging to four STG DICE cells. Thus, three groups of adjacent STG DICE cells are situated between two groups

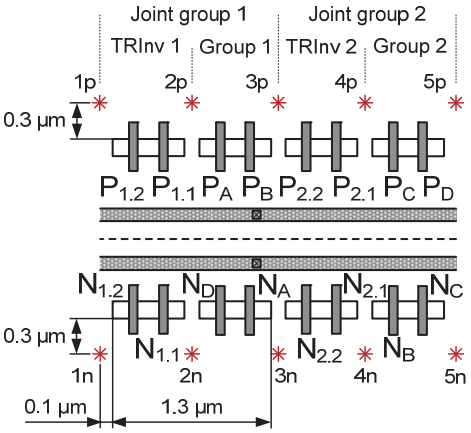


Fig. 6. The layout of the element of matching based on the tristate inverters TRInv 1 and TRInv 2 and STG DICE cell, whose transistors are separated into two joint groups without spacing between them; asterisks indicate the location of the input track points.

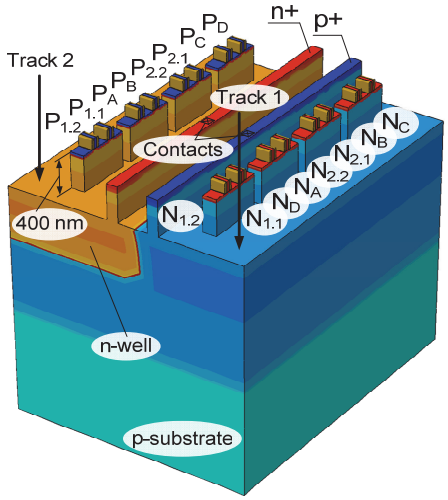


Fig. 7. The 3-D device physical model STG DICE cell; *n*+ и *p*+ guard bands are for mutual insulation of p- and n-regions; the tracks are directed along the normal to the surface of p-region (Track 1) or n-well (Track 2). The distance between the transistors N_A and N_C is 1.35 μm.

of one STG DICE cell. It provides the minimum distance between cell's mutual sensitivity nodes of 2.95 µm.

Parameters of blocks were simulated in Cadence Virtuoso using 65-nm CMOS transistors at tt technological corner after extraction of layout parasitics. Supply voltage is 1.0 V, temperature is 25°C and the clock frequency is 1.0 GHz. Table 2 presents the values of the power consumption of blocks for different operating modes: write, search and read of data. The maximum power consumption takes place in the CAM array (27.54 mW) at the search mode. This is due to the switching of all logical elements in each register during a parallel search in TLB. In our case, the power consumed in the search mode is 0.43 mW for each register at the clock of 1 GHz. This exceeds the power consumption of the traditional CAM register (0.074 mW) with pre-charging match-lines [17] by 6 times.

V. The Methodology of TCAD Simulation

Single event effects that can be observed in the element of matching on the STG DICE cell during 3-D TCAD simulation depend on the linear energy transfer and the direction of the track. The results were obtained using Sentaurus Device simulator at the temperature of 25°C and the supply voltage of 1.0 V for 65 nm CMOS bulk structure. The 3-D device was comprised of transistors (width of channels is 150 nm) developed taking into account the models presented in the work [18].

Table 3: Maximum deviations of voltages on STG DICE cell nodes at LET = 70 MeV×cm2/mg

ABCD	0101	1010	Track
$\Delta V_{MAX.A}$ on node A (V)	0.12	0.31	3n
$\Delta V_{MAX.B}$ on node B (V)	0.49	0.11	4n
$\Delta V_{MAX.C}$ on node C (V)	0.10	0.36	5n
$\Delta V_{MAX.D}$ on node D (V)	0.37	0.11	2n

Fig. 6 shows the layout of the element of matching realized as of two identical joint groups. One joint group contains transistors of the first tristate inverter TRInv 1 ($N_{1.2}N_{1.1}P_{1.2}P_{1.1}$) and the first cell's Group 1 ($N_DN_AP_AP_B$). The second joint group contains the transistors of tristate inverter TRInv 2 ($N_{2.2}N_{2.1}P_{2.2}P_{2.1}$) and the transistors of the second Group 2 ($N_BN_CP_CP_D$) of STG DICE. In Fig. 6 the layout is without spacing between joint groups; asterisks indicate the location of the input points of the particle track. In this case, the distance between the transistors N_A and N_C is 1.35 µm. To ensure a high level of noise immunity, the transistors of two joint groups may be spaced on the adequate distance using interleaving the joint groups of the adjacent elements.

Fig. 7 shows the 3-D device physical model of STG DICE. Guard bands (n+ and p+) are for insulation n- and p-regions. The direction of the particle tracks is indicated by arrows with labels – Track 1 and Track 2. These tracks are directed along the normal to the chip surface. Track 1 is the particle trajectory at normal direction to the surface of the p-region. Track 2 is the trajectory at normal direction to the surface of the chip's n-well. The area of the 3-D device model is 6.4 µm × 10.9 µm, the depth is 3.0 µm.

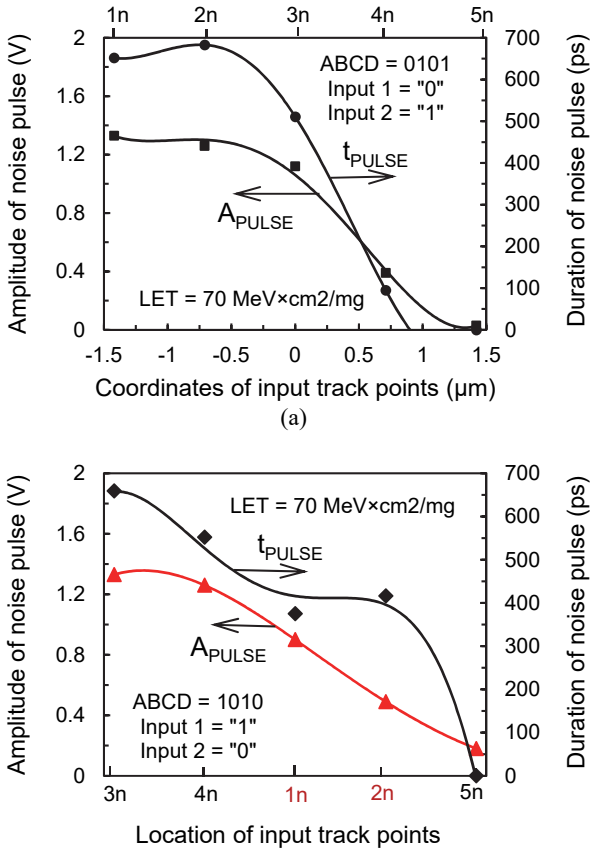


Fig. 8 Amplitudes and durations of the noise pulses on the output, LET = 70 MeV×cm2/mg: (a) – the STG DICE cell is in the initial state ABCD = 0101, Input 1 is "0"; (b) – the cell is in the state ABCD = 1010, Input 1 is "1"

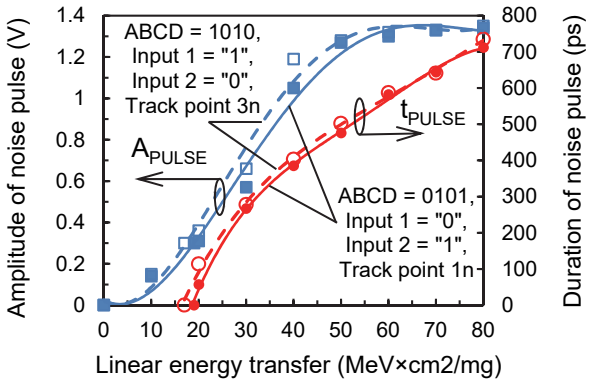


Fig. 9 Amplitudes and durations of the output noise pulses as functions of linear energy transfer. Curves are obtained for the input track point 1n at the state ABCD = 0101 and for the input track point 3n at ABCD = 1010.

Table 4: Maximum amplitudes of noise pulses on output of the element of matching at LET = 70 MeV×cm2/mg

ABCD	0101	0101	1010	1010
Input 1 / Input 2	**0 / 1**	**1 / 0**	**0 / 1**	**1 / 0**
Output match level	**1**	**0**	**0**	**1**
$A_{MAX.PULSE}$, impacts on N transistors (V)	1.33	0.29	0.26	1.33
$A_{MAX.PULSE}$, impacts on P transistors (V)	0.06	0.16	0.20	0.05

VI. The results of TCAD simulation

A. Effects in STG DICE cell

In the steady state of STG DICE, the logic levels of nodes A and C are the same. The logic levels of B and D nodes are the same too. The impact of a nuclear particle on Group 1 or Group 2 inside STG DICE (Fig. 6) does not lead to a failure, but may lead to a temporary unsteady state [8]. Table 3 presents the maximum deviations of the voltage on the nodes A, B, C, D inside the element of matching (Fig. 3) during the charge collection from tracks with the input points 1n, 2n, 3n, 4n, 5n (Fig. 6). In spite of the change in the voltage on the node B (the deviation $\Delta V_{MAX.B} = 0.49$ V on the node B in table 3) the output level "1" is unchanged. STG DICE cells significantly increase the reliability of the matching procedure during storage time.

B. Noise impulses on output of combinational circuit

When the voltage levels of the nodes are practically unchanged, the memory cell stores the recorded data securely and the main reason for noise pulses at the output of the element of matching is the charge collection by the transistors of the combinational circuit.

For the initial state of nodes ABCD = 0101 and Input 1 = "0" (Input 2 = "1") the indicator of matching the data is the Output = "1". In this case the inverter TRInv 1 is in the logical state "1", the transistors P1.1, P1.2, N1.2 are open, and the transistor N1.1 is closed (Fig. 3). The output of TRInv 2 is in the high-impedance condition and it does not shunt the output of the inverter TRInv 1.

In this mode, the charge collection from each of tracks 1n, 2n, 3n leads to a temporary switching of the inverter TRInv 1 from the level "1" down to "0" at LET values in range from 20 to 70 MeV×cm2/mg. These processes take place as in a normal inverter: the charge collection by the transistor N1.1 causes the temporary decrease of voltage on the Output. If the input track point is 4n (Fig. 6), the charge is collected only by the transistor N_B of the STG DICE cell. The voltage deviation on the node B is $\Delta V_{MAX.B} = 0.49$ V, but the Output keeps "1".

Table 4 presents the maximum amplitudes of the output noise pulses appeared due to charge collection by transistors of the combinational circuit for all logic states of the element of matching at LET value equal to 70 MeV×cm2/mg. The cases when the input data matches the stored data (the Output logic level is "1") are more sensitive to the generation of large noise pulses (with the amplitude up to 1.33 V) at the Output. The small noise pulses are observed in two cases. The first case is the particle impact on PMOS transistors (the amplitude of noise pulses is up to 0.20 V). The second case is the particle impact on NMOS transistors (the amplitude of noise pulses is up to 0.29 V) when the input data doesn't match the stored data (the Output logic level is "0").

Curves in Fig. 8 demonstrate the parameters of noise pulses depending on the coordinate of the input track point at LET = 70 MeV×cm2/mg. Fig. 8a presents dependencies of the amplitudes A_{PULSE} and durations t_{PULSE} of the output pulses for the initial state of nodes ABCD = 0101 and Input 1 equal to "0". Fig. 8b shows dependencies for ABCD = 1010 and Input 1 equal to "1". The noise pulses in both cases (Fig. 8a and Fig. 8b) are due to charge collection by NMOS transistors of tristate inverters. Curves in Fig. 8b are characterized by the same amplitudes and the durations of the noise pulse as in Fig. 8a.

Characteristics of the Joint group 1 (Fig. 6) obtained for input track points 1n and 2n at the state ABCD = 0101 and Input 1 = "0", and the characteristics of the Joint group 2 obtained for input track points 3n and 4n at the state ABCD = 1010 and Input 1 = "1" are practically the same. The reactions of these Joint groups are changed. This fact is confirmed by the dependencies in Fig. 8, where the characteristics in Fig. 8b, converted into another sequence of tracks inputs, namely 3n; 4n; 1n; 2n, are similar to the characteristics in Fig. 8a. Fig. 9 presents amplitudes and durations of the output noise pulses as functions of linear energy transfer (LET). Dependencies are obtained for the input track points characterized by the largest pulse response. They are 1n at the initial state of nodes ABCD = 0101 and 3n at the state ABCD = 1010.

VII. The topology of TLB

Fig. 10 shows the floorplan of the designed translation lookaside buffer. It takes five layers of metallization, all inputs and outputs are placed along one side of the TLB. There are guard rings on the borders of n-well and p-substrate for preventing a latch-up effect. The chip dimensions are 353×278 μm^2 (Fig. 10) and the area is 0.098 mm^2. Proposed TLB contains only one element of the parity calculation (instead of one element per word), which is placed in the block R/W BUF. It also reduces the CAM area by 11%. Blocks of CAM, RAM and the block of R/W BUF contain only hardened elements and occupy 87% of the chip area; 5% of the area is with non-hardened elements, 8% of the area contains no transistors.

Table 5 presents the main parameters of the TLB: the chip area, the power consumptions in write, search and read modes; the delays in the search and read modes. The energy consumption of the content addressable memory is measured in figure-of-merit as FOM = [Power × (Clock Period)/(Total Number of bits)] for evaluating of the design efficiency. Typical values of the energy consumption for a traditional 65 nm CMOS CAM are 0.77-2 fJ/bit/search [17]. The hardened block of CAM expends 9.15–12.6 fJ/bit/search. It exceeds the consumption of CAM with traditional design by 5–6 times since the power consumed in the search mode for each our register exceeds the power consumed of the non-hardened register. Efficient use of the chip area can be estimated using the parameters of "Area on bit". The values of the "Area on bit" for non-hardened CAM designs are 7.6–16.9 μm^2/bit. In our case, "Area on bit" is 21.1 μm^2/bit for the hardened 65-nm CAM design. In contrast to the conventional CAM design, the block of matching is realized as the static combinational circuit but not as the dynamic circuit with a pre-charged match-line. This allows to increase the reliability but leads to additional costs of the power consumption.

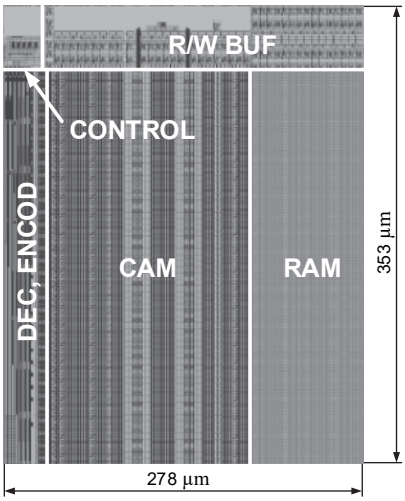


Fig. 10 The floorplan of the translation lookaside buffer

TABLE 5. PARAMETERS OF TLB

Parameter	Value
Technology node (nm)	65
Supply (V)	1.0
Chip area (mm^2)	0.098
Frequency (GHz)	1.0
CAM Capacity (bit)	64×47
RAM Capacity (bit)	64×59
Write power consumption (mW)	37.25
Search power consumption (mW)	43.13
Read power consumption (mW)	20.42
Search delay (ns)	1.19
Read delay (ns)	1.15
FOM of CAM (fJ/bit/search)	12.6

VIII. CONCLUSION

Presented translation lookaside buffer is the first project based fully on the STG DICE memory cells. This fault-tolerant solution was used in the CAM, the RAM, and the read and write buffers. The special separation of the transistors into two groups and spacing them on the chip provides the resistance of the elements of matching and the elements for masking to the impacts of single nuclear particles. The STG DICE cell reliably stores the logical state of the proposed elements under the influence of ions with LET up to 70 MeV×cm2/mg. Short-term noise pulses can occur at the outputs of these elements exposed to ions with LET in the range from 20 to 70 MeV×cm2/mg.

REFERENCES

[1] Y. Chang, and M. Lan, "Two New Techniques Integrated for Energy-Efficient TLB Design," *IEEE Trans. VLSI Syst*., vol. 15, no. 1, pp. 13–23, Jan. 2007.

[2] A. Biswas, P. Racunas, R. Cheveresan, J. Emer, S. Mukherjee, and R. Rangan, "Computing architectural vulnerability factors for address-based structures," in *Proc. of the 32nd Int. Symposium on Computer Architecture* (ISCA'05), Jun. 2005, pp. 532–543.

[3] K. F. Ng, and K. W. Hsu, "A parallel-segmented architecture for low power Content-Addressable Memory," *Int. Conf. on Very Large Scale Integration* (*VLSI-SoC*), Oct. 2009, pp. 1–4.

[4] F. Li, and M. Kandemir, "Increasing data TLB resilience to transient errors," in *Proc. of IEEE Symposium on VLSI: New Frontiers in VLSI Design* (ISVLSI'05), May 2005, pp. 1–2.

[5] N. Azizi, and F. Najm, "A family of cells to reduce the soft-error-rate in ternary-CAM," in *Proc. of Design Automat. Conf.*, 2006, pp. 779–784.

[6] N. Eftaxiopoulos, N. Axelos, and K. Pekmestzi, "Low leakage radiation tolerant CAM/TCAM cell," *IEEE Int. On-Line Testing Symposium* (IOLTS), Jul. 2015, pp. 206–211.

[7] Yu. V. Katunin, V. Ya. Stenin, and P. V. Stepanov, "Modeling the characteristics of trigger elements of two-phase CMOS logic, taking into account the charge sharing effect under exposure to single nuclear particles," *Russ. Microelectronics*, vol. 43, no. 2, pp. 112–124, Mar. 2014.

[8] V. Ya. Stenin, "Simulation of the characteristics of the DICE 28-nm CMOS cells in unsteady states caused by the effect of single nuclear particles," *Russ. Microelectronics*, vol. 44, no. 5, pp. 324–334, Sep. 2015.

[9] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci*., vol. 43, no. 6, pp. 2874–2878, Dec. 1996.

[10] V. Ya. Stenin, A. V. Antonyuk, Yu. V. Katunin, and P. V. Stepanov, "Design of logical elements for the 65-nm CMOS translation lookaside buffer with compensation of single events effects," in *Proc. of Int. Siberian Conf. on Control and Communication*, Jun. 2017, pp. 1–6.

[11] V. Ya. Stenin, and P. V. Stepanov, "Basic memory elements using DICE cells for fault-tolerant 28 nm CMOS RAM," *Russ. Microelectronics*, vol. 44, no. 6, pp. 368–379, Nov. 2015.

[12] V. Ya Stenin, and A. V. Antonyuk, "Design of the CMOS comparison elements on STG DICE for a Content-Addressable memory and simulation of single-event transients," *Telfor Journal*. vol. 9, no. 1, pp. 61−66, 2017.

[13] V. Ya. Stenin, Yu. V. Katunin, and P. V. Stepanov, "Upset-Resilient RAM on STG DICE Memory Elements with the Spaced Transistors into Two Groups," *Russ. Microelectronics*, vol. 45, no. 6, pp. 419−432, Nov. 2016.

[14] Yu. V. Katunin, and V. Ya. Stenin, "Simulation of Single Event Effects in STG DICE Memory Cells," *Russ. Microelectronics*, vol. 47, no. 1, pp. 20−33, Jan. 2018.

[15] Yu. V. Katunin, and V. Ya. Stenin, "TCAD simulation of single-event transients in the 65-nm CMOS element of matching for a content-addressable memory," *25th Telecommunications Forum (TELFOR)*, Belgrade, 2017, pp. 1–4.

[16] Yu. V. Katunin, and V. Ya. Stenin, "Design and simulation of the CMOS RS logical elements with spacing between transistor groups for minimization of single-event upsets," in *Proc. of 2018 Workshop on Electronic and Networking Technologies (MWENT)*, 2018, pp. 1–4.

[17] A. T. Do, C. Yin, K. Velayudhan, Z. C. Lee, K. S. Yeo, and T. T-H. Kim, "0.77 fJ/bit/search content addressable memory using small match line swing and automated background checking scheme for variation tolerance," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1487–1498, Jul. 2014.

[18] R. Garg, and S. P. Khatri. *Analysis and design of resilient VLSI circuits: mitigating soft errors and process variations*. New York: Springer, 2010, pp. 194–205.

[19] V. Ya. Stenin, A. V. Antonyuk, P. V. Stepanov, and Yu. V. Katunin, "Design of the 65-nm CMOS translation lookaside buffer on the hardened elements," *25th Telecommunications Forum (TELFOR)*, Belgrade, 2017, pp. 1–4.