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Designing an Efficient WCDMA Compliant Fractional-N Frequency Synthesizer

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Abstract

In this paper, fractional-N PLL is introduced to generate 1.965 GHz according to WCDMA specification , where a proposed deterministic 4th order MASH structure that guarantees a long sequence length to be used with simple stochastic dithering at the last stage as a noise shaping technique achieving hardware budget compared with classical dithering that used long linear feedback shift register LFSR . Modulator in band phase noise is -100dBc/Hz within the loop bandwidth of 1MHz, the PLL lock time is less than 25 µs. C++ language is used in the simulation of the system behavior for all blocks of the synthesizer due to its flexibility and high speed of execution, then data is post processed using MATLAB R2011a.

The proposed MASH structure consumes 89% FFs and 90% LUTs of the Dithered MASH reported in ref.[9] for identical number of bits achieve significant hardware cost reduction .

Keywords: phase-locked loop (PLL), phase noise, quantization noise suppression, MultistAge noise SHaping (MASH).

1. Introduction

In modern wireless communication system, Fractional-N PLL based frequency synthesizer is widely used due to high frequency resolution (narrow channel spacing) for spectrum concerns and fast switching time between frequencies (low settling/lock time) for high speed requirements. This ability (higher frequency resolutions with a highly flexible frequency range) comes from the fact that the division ratio can be any number and is not restricted to be an integer as in the case of integer-N PLL frequency synthesizer. Fig.(1) depicts Block diagram of both an integer and a fractional-N PLL with a digital accumulator to control the division [1] .The architecture consists of a phase-frequency detector (PFD), a charge-pump (CP), a loop filter, a voltage-controlled oscillator (VCO), and a programmable frequency divider.

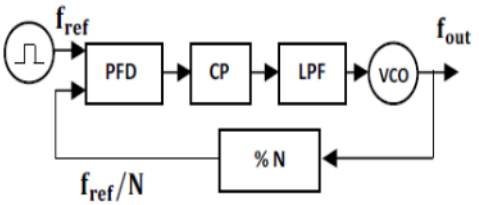

Fig. 1 .a. Block diagram of an integer-N PLL [1]

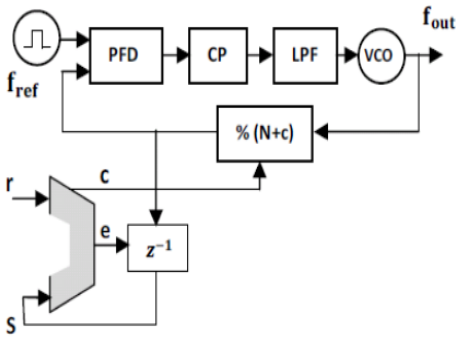

Fig. 1.b . Block diagram of a classical fractional-N PLL [1]

The classical fractional-N PLL synthesizers dithers the divide ratio with an a ımulator [3]. But it suffers from the appearan_e of fractional spur (spurious tones) due to the switching behavior of the system between N and N+1 division, since the accumulator is a finite state machine, it cycles through its states in a periodic manner, the spurs appear at Phase Frequency Detector (PFD) frequency offsets from the carrier and at their harmonics [1]. The positions of these spurs are in the fractional multiples of f_{ref} . Since the synthesizer output frequencies are much more than f_{ref} , these spurs are very close to the carrier frequency making it difficult to filter them out [3]. The output frequency of an integer-N frequency synthesizer if the PLL is locked is a multiple of the reference frequency;

$$f_{out} = f_{ref} \cdot N \quad \ldots (1)$$

In the other hand the output frequency of a fractional-N frequency synthesizer is [4];

$$f_{out} = f_{ref} \cdot \left(N + \frac{r}{2^{n_o}}\right) \quad \ldots (2)$$

Where, n_o is the accumulator word length, the sequential integer numbers control the division of the divider so that the desired fractional ratio is obtained. The deviation between the integer number and the fractional number is called quantization noise which has a high-pass feature in frequency domain [4] and often dominates at high offset frequencies, the quantization noise of the fractional-divider can be pushed away to the higher frequencies by the aid of using Delta-Sigma frequency synthesizers DSMs, these act as the controller of the multi-modulus frequency divider in the feedback loop of the frequency synthesizer as depicted in Fig.(2). So the most attractive property of DSMs is that they push most of the quantization noise to higher frequencies and hence out of the useful frequency band thus the noise can simply be filtered without affecting the input signal.

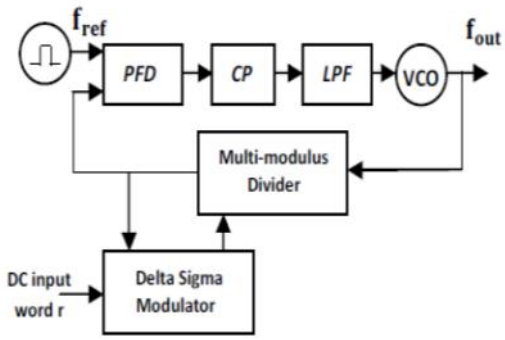

Fig. 2 . Block diagram of a DSM fractional -N PLL [1] .

When the delta-sigma modulation is performed on a digital input signal (n_o bits) and produced a digital output signal (m bits) such system is called digital delta-sigma modulator (DDSM) and results in a quantization error that is often modeled as an addition of white noise as showing in Fig.(3) . DDSMs fall into two categories: single-loop delta-sigma modulators and Multi-stAge noise SHaping (MASH) delta-sigma modulators [6]. Disadvantage of the single-loop DSM is the instability because of the feedback loop inherent within the architecture [6]. In contrast, the MASH DDSM (Fig.4) has been proven to be unconditionally stable.

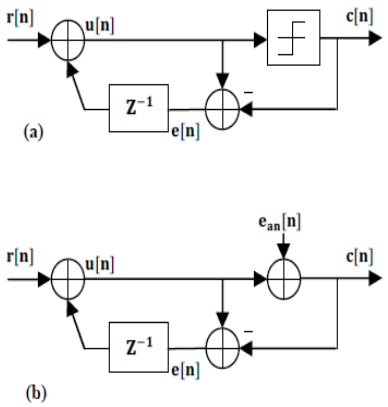

Fig. 3. a) Block diagram of a first-order error feed back modulator EFM1 b) The linearized model when the quantizer is replaced by an additive noise source [4]

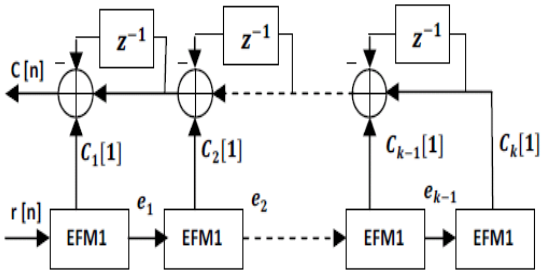

Fig. 4. Architecture of MASH DDSM ,

EFM1 is error feedback modulator given in fig.3

For frequency synthesizer PLL applications the input is a DC rational constant [9], the output is always a repeating pattern with limit cycle since the DDSM is a finite state machine, the quantization noise is periodic. When a sequence length is short, the power is distributed among spurious spurs that appear in the DDSM output spectrum. There are two classes of technique for whitening quantization noise and break short sequences, *stochastic* and *deterministic* [4]. The dithering [6] method is one of the most common stochastic approaches employed. It uses a random dither sequence to disrupt the periodic cycle and thereby effectively increase the sequence length. However, it requires extra hardware and inherently introduces additional noise in the useful frequency band, dither signal may be added at the input (Fig.5) or in loop where d[n] is a 1-bit pseudorandom dither sequence and H (z) is a shaping filter. In the other hand the *deterministic* technique recently has been proposed to maximize the sequence length. Ref. [4] Introduced a digital delta-sigma modulator structure termed the HK-MASH with a very long sequence and the period of such a sequence.

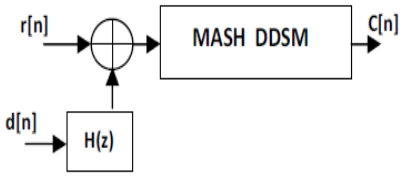

Fig. 5. MASH DDSM with shaped dither at the input .

This paper investigates an efficient proposed PLL frequency synthesizer with 20 bit 4th MASH as a Delta-sigma modulator with simple 8 bit register introduced at the LSBs input of the final stage to suppress quantization noise , the system is investigated in a PLL frequency synthesizer to be used for WCDMA applications .

2. MASH Delta Sigma Modulator

HK-EFM (Fig. 6.a) can be obtained by adding simple feedback $\alpha\, z^{-1}$ block to the first order Error Feedback Modulator (EFM) the sequence length is maximized and first order EFM effectively gives a prime modulus while the modulus of the quantizer itself is a power of 2. Fig.(6.b) is a model of the digital accumulator the quantizer block corresponds to the overflow operation of the digital accumulator;

$$c[n] = 1 \text{ , for } u[n] \geq M \text{ and } 0 \text{ , otherwise } \ldots (3)$$

Where n_o is the accumulator word length and $M = 2^{n_o}$, the modulator shapes the spectrum of the quantizer error (noise), thereby distributing the power into higher frequency components. To simplify the analysis, one can build an approximate linear model of the modulator in which the quantizer is replaced by an additive quantization noise source $e_{an}[n]$

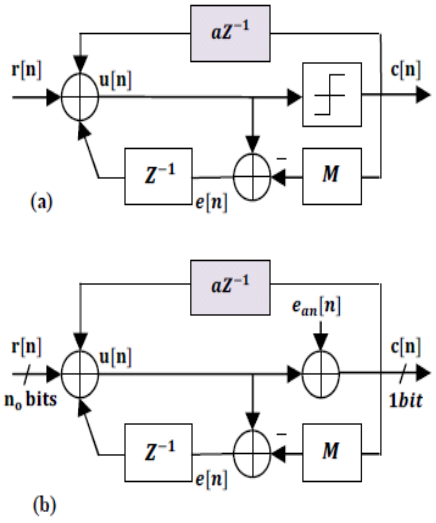

Fig. 6. a) Block diagram of a first-order digital KH-EFM1
b) The linearized model when the quantizer is replaced by an additive noise source [4] .

The linear Z - domain output can be written as follows:

$$C(z) = U(z) + E_{an}(z) \quad \ldots . (4)$$

$$E(z) = U(z) - C(z) \quad \ldots . (5)$$

so we have $E(z) = -E_{an}(z)$ $\ldots \ldots (6)$

For the first summing node;

$$U(z) = R(z) + \alpha\, z^{-1}C(z) + z^{-1}E(z) \quad \ldots . (7)$$

From (6) & (7) we obtain,

$$U(z) = R(z) + \alpha\, z^{-1}C(z) - z^{-1}E_{an}(z) \quad \ldots . (8)$$

From (4) & (8) we obtain,

$$C(z) - E_{an}(z) = R(z) + \alpha\, z^{-1}C(z) - z^{-1}E_{an}(z) \ldots . (9)$$

or; $C(z) = \frac{R(z)}{1-\alpha\, z^{-1}} + \frac{1-z^{-1}}{1-\alpha\, z^{-1}}\, E_{an}(z)$ $\ldots . (10)$

So the signal transfer function is;

$$STF(z) = \frac{1}{1-\alpha\, z^{-1}}$$

And the noise transfer function is;

$$NTF(z) = \frac{1-z^{-1}}{1-\alpha\, z^{-1}}$$

It's well known that transfer function of a classic EFM1 (without $\alpha\, z^{-1}$ feedback block) can be expressed as;

$$C(z) = R(z) + (1 - z^{-1})\, E_{an}(z) \quad \ldots . (11)$$

Comparing (11) with (10) we inferring that a pole at $z = \alpha$ is added to both the signal transfer function and the noise transfer function to suppress the high-frequency noise without significantly effecting the overall operation of the modulator in the in-band. α is a small integer selected to make $M - \alpha$ the maximum prime number below 2^{n_o} , sequence length of the structure is [4]; $M - \alpha$ for all constant inputs .

The proposed deterministic MASH structure (HK-MASH) with dithering is showing in Fig.(7) , where all the signals are normalized to unity for the purpose of the linear analysis, hence the scalar M disappeared from all the EFM blocks and α is a/M. So for *k_th* order modulator we obtain;

$$C_1(z) = \frac{R(z)}{1-\alpha\, z^{-1}} - \frac{1-z^{-1}}{1-\alpha\, z^{-1}}\, E_1(z) \quad \ldots . (12)$$

$$C_2(z) = \frac{E_1(z)}{1-\alpha\, z^{-1}} - \frac{1-z^{-1}}{1-\alpha\, z^{-1}}\, E_2(z) \quad \ldots \ldots (13)$$

$$C_k(z) = \frac{E_{k-1}(z)}{1-\alpha\, z^{-1}} - \frac{1-z^{-1}}{1-\alpha\, z^{-1}}\, E_k(z) \quad \ldots (14)$$

For last summing point;

$$C_o(z) = C_1(z) + C_2(z)(1-z^{-1}) + \cdots + C_{k-1}(z)(1-z^{-1})^{k-1} \quad \ldots . (15)$$

Comparing (16) with (11) for first order error feedback modulator , one inferring that the signal transfer function of this MASH1-1-1-1 structure is same as HK-EFM1 , in the same time the noise transfer function increased to the order of k so we obtain the desired fraction and the high

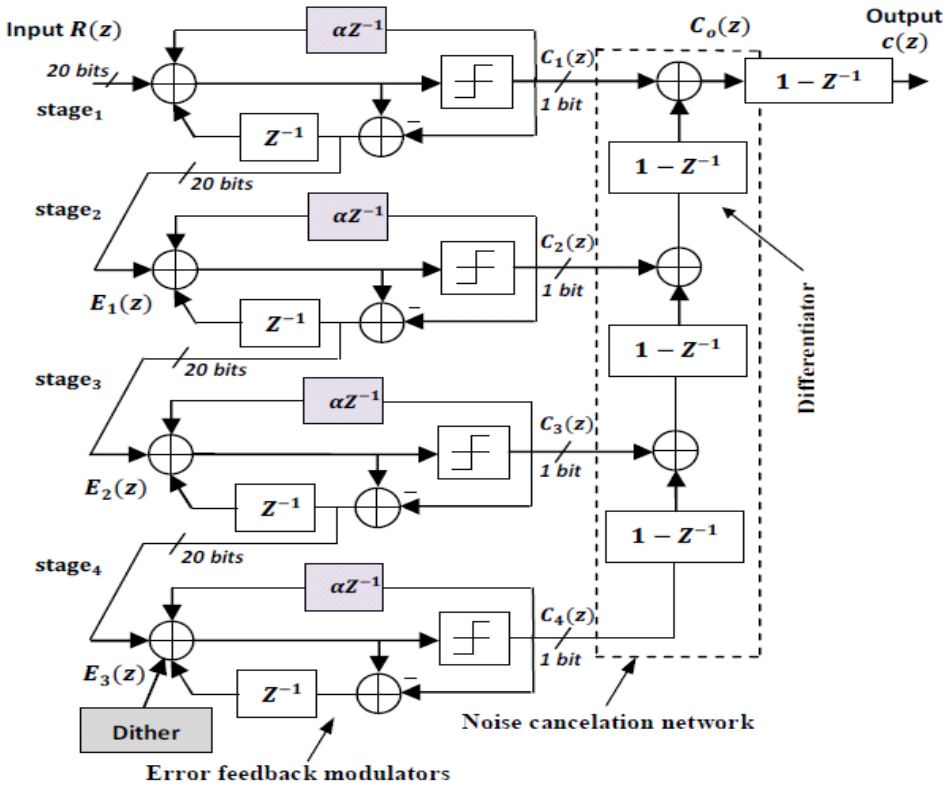

Fig. 7. Block diagram of the proposed Delta Sigma modulator to be used in 1.956Ghz frequency synthesizer .

Using (12) into (15);

$$C_o(z) = \frac{R(z)}{1-\alpha z^{-1}} - \frac{(1-z^{-1})^k}{1-\alpha z^{-1}} E_k(z) \quad \ldots.(16)$$

$$C(z) = R(z) - (1-z^{-1})^k E_k(z) \quad \ldots..(17)$$

Or in other expression;

$$C(z) = R(z) + (1-z^{-1})^k E_{ank}(z) \quad \ldots..(18)$$

Comparing (16) with (11) for first order error feedback modulator , one inferring that the signal transfer function of this MASH1-1-1-1 structure is same as HK-EFM1 , in the same time the noise transfer function increased to the order of k so we obtain the desired fraction and the high order noise-shaping operation. If the dither signal is added at the showing node, then;

$$C(z) = R(z) + (1-z^{-1})^k D(z) + (1-z^{-1})^k E_{ank}(z) \quad \ldots\ldots.(19)$$

So the dither signal D (z) does not affects the input signal, i.e. the constant modulated signal is not affected by the dither addition. In this proposed dithering scheme a very simple 8 bits linear feedback shift register LFSR can be used to reduce the spur tone magnitude for the high frequencies offset from the carrier (to make the quantization error appear more randomized) instead of a very long pseudorandom generator used in classical dithering schemes or a one LSB dither in the DC input word which shifts the output frequency by 19 Hz (for a 20-bit accumulator $\frac{f_{ref}}{2^n}$) thereby limiting the ultimate resolution of the synthesizer hence the proposed dithering is more efficient .

Fig.(8) depicts noise density for 1st and 2nd order delta sigma modulator, the noise transfer function describes a high-pass filter function

3. PLL phase noise contributors

The contributions of the different terms to the PLL phase noise versus frequency can be summarizes in Fig.(9), for a narrow and wide bandwidth filters. Close to the central frequency fo, the reference source is the main contribution to phase noise, whereas the VCO contribution is dominant outside the loop bandwidth. In between, a region corresponds to the contribution of the

PLL noise, where the level of the zone is proportional to N. Then, there is an overshoot, for

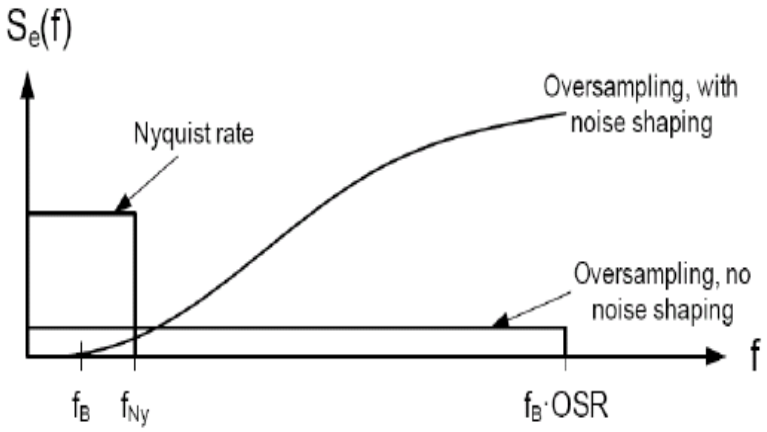

Fig. 8 Noise density of sigma-delta modulation for 1st and 2nd order noise shaping compared to Nyquist rate and oversampling.

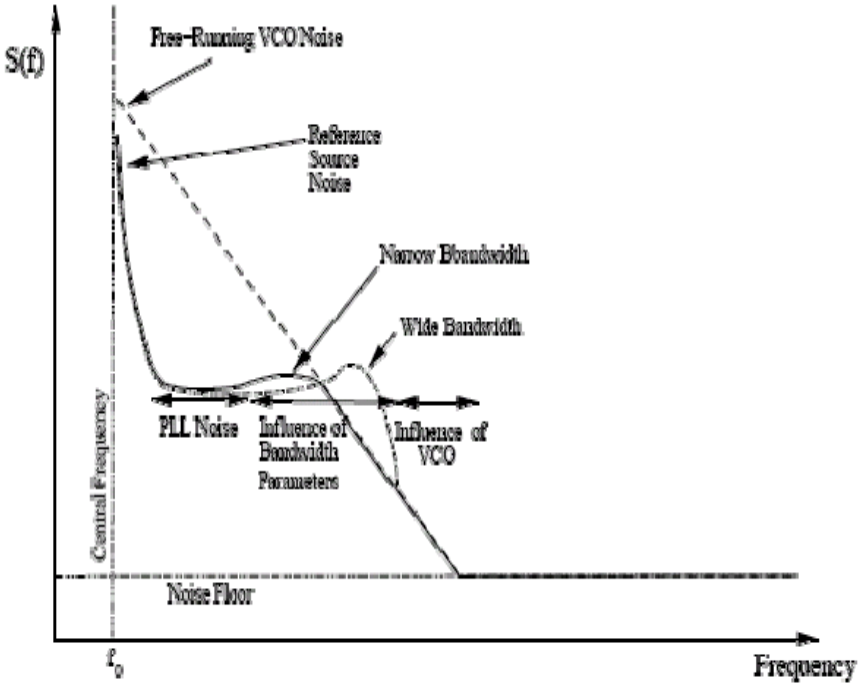

Fig. 9 Overall Noise Contribution [13] .

Which the frequency depends on the bandwidth chosen, that is, for a wide bandwidth, the overshoot is placed in a higher frequency than that for a narrow bandwidth, with an increased flat-zone

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4. Behavioural Simulation of The PL Frequency Synthesizers

The design procedure for the proposed WCDMA frequency synthesizer is summarized by the flow chart of Fig.(10).

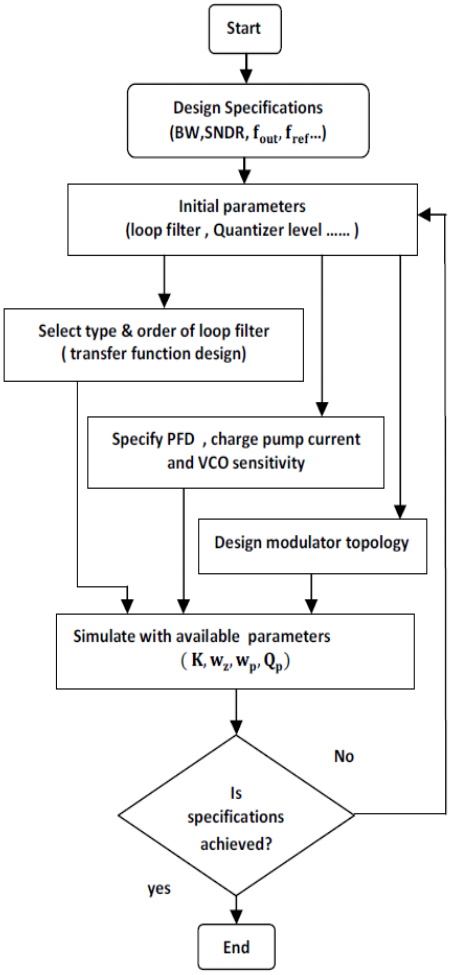

Fig.10 PLL frequency Synthesizer Design flowchart .

Initial parameters assumed according to IEEE standard for Wide Code Division Multiple Access [6], CppSim behavioral simulator is used to build an evolving model of the proposed synthesizer with non-idealities (mismatch) in individual circuit blocks, where C++ behavioral simulator model allows us to quickly evaluate architectural changes that help alleviate the impact of these non-idealities and therefore eases the circuit design process.

As a target for the system performance, we desire a 1MHz closed loop synthesizer bandwidth that exhibits < −129dBc/Hz phase noise at a 3.5MHz offset from the carrier and <-96dBc/Hz in-band phase noise [6] for a 1.956GHz carrier (output frequency) for input reference frequency of 20MHz.

The PFD topologies that will be used is Tristate approach since it produces narrow pulses such that the charge pump need only be on during a small portion of the reference cycle (reducing charge pump noise and reference spur).

The loop filter can be adjusted according to the parameters from the PLL Design Assistant (PDA) tool described in [5], where type II, 3rd order passive filter with Butterworth response is used as low-pass filter LPF.

The first step is to design the closed loop transfer function of the PLL G(f) according to desired specifications, and then calculate the open loop response A(f) required to realize the desired closed loop behavior where,

$$G(s) = \frac{A(S)}{1 + A(s)} \qquad \dots (20)$$

Which is the transfer function of a negative feedback system also,

$$A(s) = \frac{k_v I_{cp} H(s)}{s\, N_{mean}} \qquad \dots (21)$$

k_v is the VCO gain in Hz/V , I_{cp} is the charge pump current in Amp and is typically constrained by limits on the loop filter component values or power dissipation , N_{mean} is the geometric mean of the maximum and minimum division ratio required to span the desired frequency band ,

$$N_{mean} = {f_{out}}/{f_{ref}} \qquad \dots (22)$$

In this case $N_{mean} = \frac{1956}{20} = 97.95$ for order three type II filter we have [5],

$$H(s) = \frac{K_{LP}(1+w_z)}{K(1+s/w_p Q_p)\,(s/w_p)^2} \qquad \dots (23)$$

$K_{LP} = K\,\frac{N_{mean}}{k_v I_{cp}}$ is DC gain of the loop filter, K is gain term , $w_z = 2\pi f_z$, $w_p = 2\pi f_p$, the next step is to calculate the parameters of the transfer function (K, w_z, w_p, Q_p) and then the component values using the PLL Design Assistant software ,these values used in C++ model for block diagram Fig.(2) ,where the behavioral simulation is performed then results post-processed with MATLAB program tool R2011a

5. Performance Investigation

5.1 Response Investigation

Fig.(11.a), Shows the response of the open loop transfer function

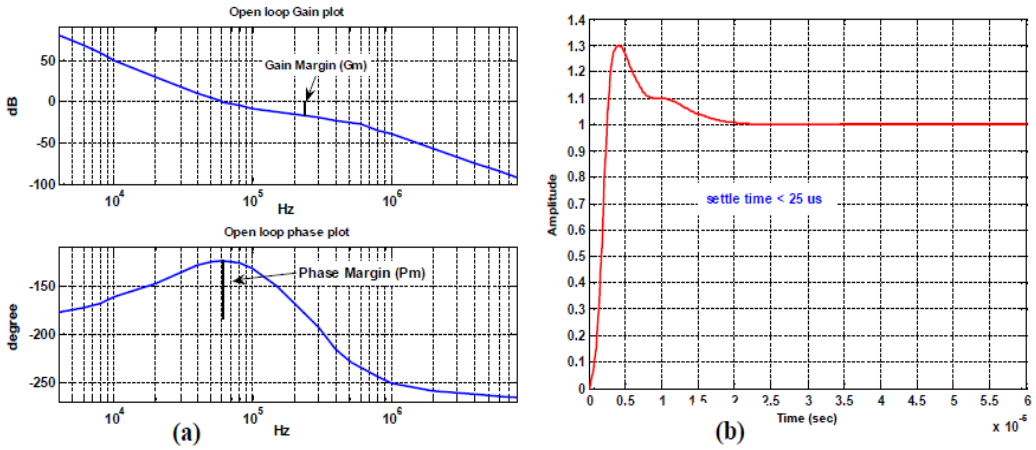

Figure (11): a.Bode plot for loop filter b. step response

Phase margin of 56 degree indicated for unity gain (0dB) @ 376.8 krad/sec (60kHz) cross over frequency, Gain margin of 17dB indicated for phase response of -180° @ 1.44Mrad/sec. Fig.(9.b) Shows the closed loop time response of the system , here we must remember that in a wireless transceiver system, the frequency synthesizer lock time (settling time) should be less than the required time for channel switching (frequency synthesizer to be locked from one frequency to the other in its operation band) according to the wireless standards , from Fig.(9.b) settling time is less than 25usec.

5.2. Delta Sigma Quantization Noise spectrum

Fig.(12), shows the output spectrums of the proposed 4th MASH modulators. This modulator presents a low quantization noise in the bandwidth and noise is shaped to high frequencies, this spectrum of bit stream output result form 20 bit static DC input of 917504 which is 87% of the total range (2^{20} =1048576) , the simulation was run on 2^{19} sample , as expected a slope of 80dB/decade of high pass noise shaping is achieved since we used 4th order modulator , for fairly comparison a spectrum of dithered MASH (20 bit accumulator) [6] is associated , the proposed scheme outperforms classical MASH (at least for low frequencies).

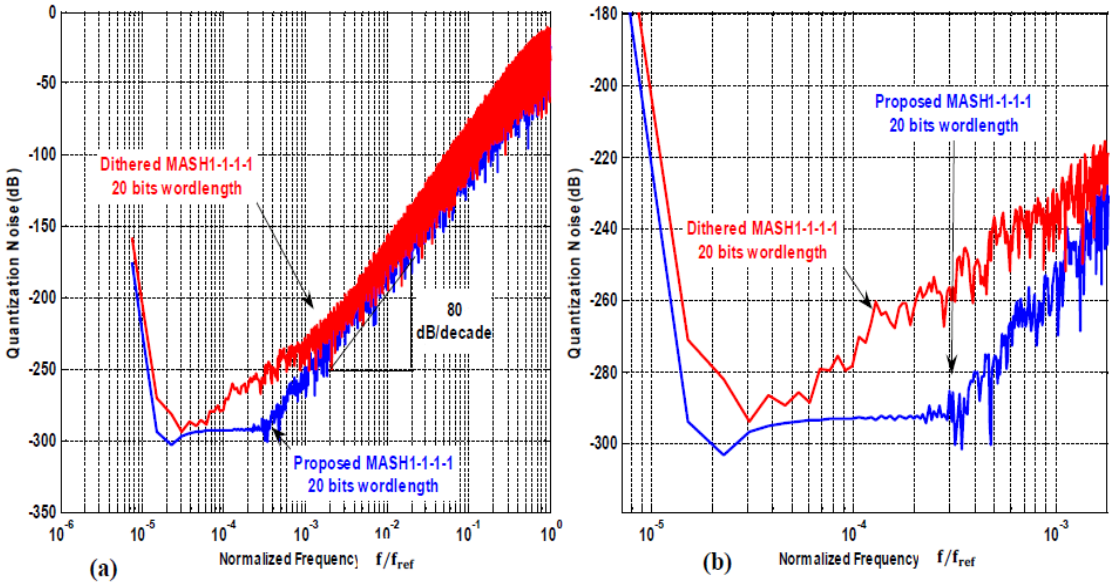

Figure (12): a. Output spectrums of the proposed 4th MASH modulators. b. Zoomed in

5.3. Quantization Errors Sequence length

The autocorrelation sequence is the best form to explore the periodicity of a discrete sequence; Fig.(13) compares the proposed system with that of classical dithered MASH ref.[6] in terms of sequence length. The sequence length of the proposed structure is greater and hence preferable where a longer sequence length means the noise spur is further out of the required modulation spectrum.

5.4 PLL Output Spectral Investigation

Fig.(14) shows a plot of the phase noise of the system (Spectrum SimulationL(f)) the results of the CppSim simulation are over layered on the PLL Design Assistant PDA (theoretical) calculations. There is excellent agreement between the calculated noise response and simulated result, the slight discrepancy at very low frequency can be attributed to a very small DC component left in the PSD calculation of the behavioral simulation results, the reference spur at 20MHz (-105dBc/Hz or -40dBc below the carrier), which is not included in the analytical PDA calculations .

In terms of the noise contribution by different blocks of the PLL, Fig.(12) shows that the phase noise is dominated by VCO and the modulator noise from cut off frequency up to almost 10MHz frequency offset from carrier, however the noise from PFD/CP and divider is dominating in the range of cut-off frequency 1MHz offset.

Table 1 summarizes the fractional-N PLL frequency synthesizer performance.

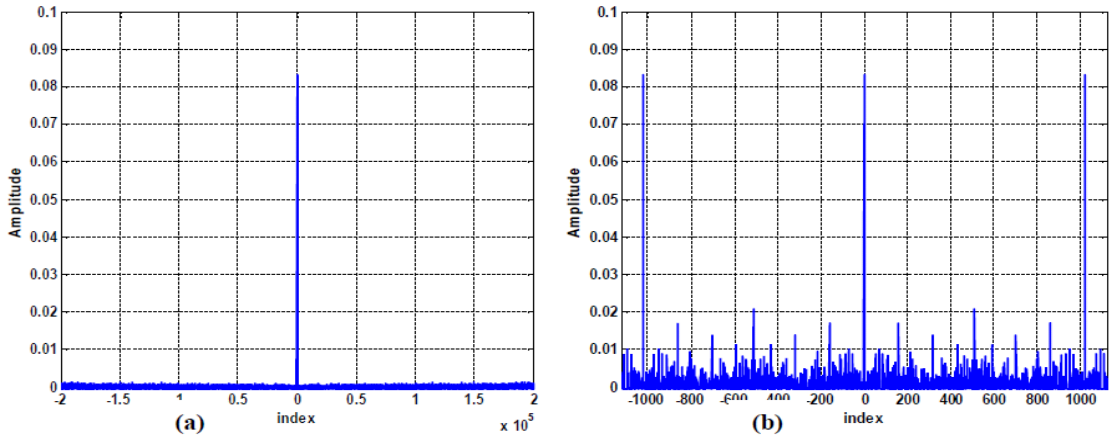

Figure (13): Quantization Error autocorrelation of the: a. proposed modulator. b. classical MASH

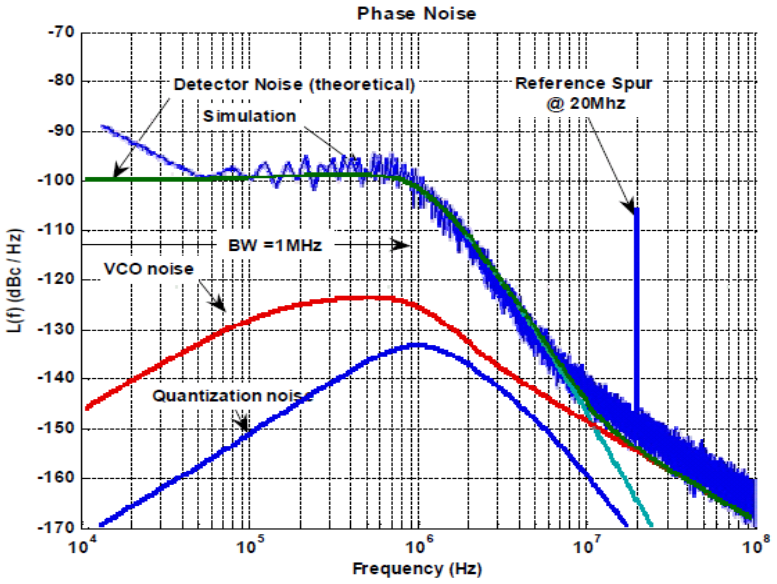

Figure (14): Phase noise spectral

5.5 Hardware cost

Table 2 shows the summary of the hardware requirements where the overall proposed frequency synthesizer : phase-frequency detector (PFD), charge-pump (CP),loop filter, voltage-controlled oscillator (VCO) and DSM have been coded in VHDL and compiled, simulated and synthesized using a Xilinx Spartan-2E FPGA.

Table (1): frequency synthesizer performance summary

Parameter	Proposed system	Ref.[6]	Ref.[12]	Comments
Reference frequency	20MHz	85MHz	26MHz	Low reference freq. for less noise jitter
Output frequency	1.965GHz	1.965GHz	1.965GHz	
Loop band width	1MHz	200KHz	200KHz	Wide frequency range
Lock time	< 25 usec	< 25 usec	Not available	Suitable For wireless applications
Phase margin	56°	52°	Not available	> 45° for stability
In band phase noise	-100dBc/Hz	-98dBc/Hz	-96dBc/Hz	
Out band phase noise	-127dBc/Hz	-129dBc/Hz	-128dBc/Hz	@3.5MHz offset from carrier
Spur at the output	No spur	No spur	-66dBc/-70dBc	Suppressed by dithering
Accumulator word length n	20 bits	26 bits	20 bits	Hard ware budget
Quantizer level	1 bit	1 bit	3-4 bits	
Frequency resolution $\frac{f_{ref}}{2^n}$	< 20 Hz	< 10 Hz	< 100 Hz	Channel space

Table (2): Hardware consumption summary report of the overall frequency synthesizer

SDM4_DITHER Project Status			
Project File:	SDM4_dither.ise	Current State:	Programming File Generated
Module Name:	top_sigma	• Errors:	No Errors
Target Device:	xc2s50e-6ft256	• Warnings:	31 Warnings
Product Version:	ISE 9.2i	• Updated:	الخميس 29. اذار 2012 22:54:09

SDM4_DITHER Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	286	1,536	18%	
Number of 4 input LUTs	772	1,536	50%	
Logic Distribution				
Number of occupied Slices	462	768	60%	
Number of Slices containing only related logic	462	462	100%	
Number of Slices containing unrelated logic	0	462	0%	
Total Number of 4 input LUTs	780	1,536	50%	
Number used as logic	772			
Number used as a route-thru	8			
Number of bonded IOBs	18	178	10%	
IOB Flip Flops	16			
Number of GCLKs	2	4	50%	
Number of GCLKIOBs	2	4	50%	
Total equivalent gate count for design	10,579			
Additional JTAG gate count for IOBs	960			

Table 3 shows hardware complexity for the Delta Sigma Modulator Block alone ,the hardware consumption is reported as the number of flip-flops (FFs) ,the number of four input lookup tables (LUTs) (synchronous logic and the asynchronous logic, respectively) ,and the total equivalent gate (TEG) count for the design based on the map report from the Xilinx ISE 9.2i program , the DSM coded in VHDL for two topology (classical dithered MASH ref.[9] and proposed MASH of Fig. 7)

Table (3): Comparison of hardware consumption

DSM topology	Hardware consumption		
	FFs	LUTs	TEGs
Proposed scheme	103	130	2056
Classical dithered MASH	115	148	2503

6. Conclusions

ΣΔ fractional-N PLL technique is selected to WCDMA system since, step size is smaller than an integer-N PLL, loop bandwidth is large and settling time is short. The quantization noise is perfectly cancelled by using deterministic 4^{th} order digital ΣΔ modulator that guarantees a long sequence length with simple stochastic dithering (8 bit) at the last stage as noise shaping technique which does not affect the input DC signal and achieve better performance than conventional LFSR-dithering technique that requires extra hardware as simulation shows, modulator in band phase noise is , -100 dBc/Hz within the loop bandwidth of 1MHz, the lock time is less than 25 μs.

In terms of hardware cost from Table III, we see that the proposed MASH consumes 89% FFs and 90% LUTs of the Dithered MASH of ref. [9] with identical number of bits.

7. Future work

CDMA system offers a high immunity to interferences during transmission where the signal energy is spread over a large bandwidth. The larger ratio of the spread bandwidth to the original data bandwidth (processing gain) the higher interference immunity. In order to obtain a more efficient system the effects of band spreading on the frequency synthesizer performance needs to be investigated with different spreading codes e.g. pseudorandom PN and Walsh.

In order for the proposed architecture to comply with practical wireless communication system, more emphasis on the synthesizer noise performance is needed when there is interference from other CDMA subscribers use same bandwidth hence, some attention is required to enhance the frequency synthesizer noise performance .

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تصميم مركب تردد كسري كفؤ مطاوع لمنظومة تقسيم الشفرة متعددة الوصول ذات الطيف العريض

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الخلاصة:

في هذا البحث تم تقديم مركب تردد كسري يستخدم حلقة أقفال الطور لتوليد تردد 1.965 كيكاهرتز مطاوع لمنظومة تقسيم الشفرة متعددة الوصول ذات الطيف العريض , حيث تم أستخدام مكيف الضوضاء متعدد المراحل من الرتبة الرابعة والذي يضمن سلسلة طويلة ,مع أضافة أشارة ترددية عشوائية بسيطة عند المرحلة النهائية كتقنية لتكيف الضوضاء وبحجم صغير للمكون المادي للنظام مقارنة مع المنظومة التقليدية التي تستخدم سجل تزحيف تغذية عكسية خطية طويلة . ضوضاء الطور للمضمن داخل حزمة 1MHz هي -100dBc/Hz . زمن الأستجابة هوأقل من 25 µs. تم أستخدام C++ في محاكات سلوك أجزاء مركب التردد المختلفة لأن هذه اللغة ذات مرونة وسرعة تنفيذ عالية . تم معالجة البيانات النهائية بأستخدام MATLAB R2011a .

مكيف الضوضاء متعدد المراحل المقترح يستخدم 89% من النطاطات وأيظا 90% من جداول LUTs التي يستخدمها Dithered MASH المنشور في المرجع [9] لنفس العدد من bits محققا تقليل مهم في الكلفة المادية .