VARIABILITY ANALYSIS OF 6T AND 7T SRAM CELL IN SUB-45NM TECHNOLOGY

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ABSTRACT : This paper analyses standard 6T and 7T SRAM (static random access memory) cell in light of process, voltage and temperature (PVT) variations to verify their functionality and robustness. The 7T SRAM cell consumes higher hold power due to its extra cell area required for its functionality constraint. It shows 60% improvement in static noise margin (SNM), 71.4% improvement in read static noise margin (RSNM) and 50% improvement in write static noise margin (WSNM). The 6T cell outperforms 7T cell in terms of read access time (T_{RA}) by 13.1%. The write access time (T_{WA}) of 7T cell for writing "1" is 16.6 × longer than that of 6T cell. The 6T cell proves it robustness against PVT variations by exhibiting narrower spread in T_{RA} (by 1.2×) and T_{WA} (by 3.4×). The 7T cell offers 65.6% saving in read power (R_{PWR}) and 89% saving in write power (W_{PWR}). The R_{PWR} variability indicates that 6T cell is more robust against process variation by 3.9×. The 7T cell shows 1.3× wider write power (W_{PWR}) variability indicating 6T cell's robustness against PVT variations. All the results are based on HSPICE simulation using 32 nm CMOS Berkeley Predictive Technology Model (BPTM).

KEY WORDS: *Cell ratio, Pull-up ratio, Static noise margin (SNM), Read access time, Write access time, Static random access memory (SRAM), Drain-induced barrier lowering (DIBL)*

INTRODUCTION

Due to aggressive scaling of device dimensions, random variations in process, supply voltage and temperature (PVT) poses major challenges to the future high performance circuits and system design [1-3]. The microscopic variations in number and location of dopant atoms in the channel region of the device induce deviations in device characteristics [4-6]. These fluctuations are more pronounced in minimum-geometry devices commonly used in area-constraint circuits such as SRAM cells [7]. The intrinsic fluctuations are independent of transistor location on a chip. The threshold voltage (V_t) mismatch between neighbouring cell transistors due to intrinsic fluctuations typically

contributes to larger reductions in static noise margin (SNM) [7]. The SNM model in [8] assumes identical device threshold voltages across all cell transistors, making it unsuitable for predicting the effects of threshold voltage mismatch between adjacent transistors within a cell. Therefore, designers will require reevaluation and analysis of static noise margin in scaled technologies to ensure stability of SRAM cell. The PVT variations affect the device threshold voltage (V_t), which in turn modulates the drain to source current (I_{DS}). The variation is normally (as it is called Gaussian or Normal distribution) distributed and its $\pm 3\sigma$ variation is about 30 mV at 32 nm technology node. The spread in read access time (T_{RA}), write access time (T_{WA}), read power (R_{PWR}) and write power (W_{PWR}) is due to variation in I_{DS}. PVT variations can be mitigated by various design techniques. Adaptive body biasing is one such technique [9]. Circuit design technique such as body biasing will help, but their effect diminishes with technology scaling [10]. SRAM is a highly used circuit in modern chips — it is used in caches, register files, FIFOs, etc. Consequently, SRAM constitutes more than half of chip area and more than half of the number of devices in modern designs [11]. Hence, the analysis and evaluation of SRAM cell in terms of its design criteria is not only important but also its robustness against PVT variations is essential in nanometer regime.

This work analyses 6T and 7T SRAM cells and compares various SRAM design metrics. In standby mode SRAM cells are inactive and consume power for data retention due to various leakage components. This paper investigates leakage power consumption and the impact of PVT variations on SRAM's design metrics at 32 nm technology node. It presents analysis of SNM, T_{RA}, T_{WA}, R_{PWR}, W_{PWR} and their variations due to the impact of process parameters, voltage and temperature variations. The analysis shows that the standard 6T SRAM cell outperforms 7T SRAM cell in terms of robustness against PVT variations with respect to most of its design metrics.

The remainder of this paper is organized as follows. Section 2 briefly discusses impact of Drain-Induced Barrier Lowering (DIBL) on NMOS transistor at 32 nm technology. Various stability metrics, failure mechanisms and operations of SRAM are briefly reviewed in Section 3. Section 4 presents a brief discussion on 7T SRAM cell, and its device/technology parameters. Section 5 explores the impact of PVT variation on SRAM's various design metrics. Simulation measurements and comparisons between 6T and 7T SRAM cell are detailed in Section 6. Finally, the conclusion of the paper appears in Section 7.

2. IMPACT OF DRAIN-INDUCED BARRIER LOWERING ON SCALED DEVICES

Reevaluation and computation of voltage ripple (V_{QB}) developed at storage node QB in Fig. 2(a) at scaled technology is a necessity as threshold voltage (V_t) of a small-sized transistor depends not only on substrate doping concentration (N_A) and other process parameters but also on DIBL effect. Analytical expression of V_t is given by:

$$V_t = V_{t0} + \gamma\left(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right) \quad (1)$$

where V_{t0} is the threshold voltage at V_{SB} = 0 V and is mostly a function of the manufacturing process, difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc; V_{SB} is the source-bulk voltage; $\phi_F = V_T \ln(N_A/n_i)$ is the bulk Fermi potential (where V_T = kT/q = 26 mV at 300 K is the thermal voltage, N_A is the acceptor doping concentration, n_i is the intrinsic carrier concentration in pure silicon); $\gamma = \sqrt{(2qN_A\varepsilon_{si})}/C_{ox}$ is the body-effect coefficient (where ε_{si} is the relative permittivity of silicon, C_{ox} is the gate oxide capacitance). Equation (1) is not suitable for predicting V_t at scaled technology where impact DIBL is pronounced. The impact of DIBL on V_t is modeled as:

$$V_t = V_{t0} - \eta_{DIBL} V_{DS} \quad (2)$$

where V_{t0} is the threshold voltage at V_{DS} = 0 V, and η_{DIBL} is the DIBL coefficient. For NMOS at 32 nm technology node, the DIBL effect on V_t is plotted in Fig. 1(a), which shows the dependency of V_t on V_{DS}. It particularly, shows that the V_t is 0.6292 V at V_{DS} = 0 V and the V_t drops to 0.4381 V at V_{DS}=1 V. As is well known, drain to source saturation voltage (V_{DSAT}) depends on both gate to source voltage (V_{GS}) and V_{DS}. The V_{DSAT} of NMOS at V_{GS}=1 V versus V_{DS} is plotted in Fig. 1(b). It shows the dependency of V_{DSAT} on V_{DS}. It particularly shows that V_{DSAT} is 0.2711 V at V_{DS} = 0.2 V. It is also evident from Fig. 1(b) that the V_{DSAT} increases to 0.3338 V at V_{DS}=1 V.

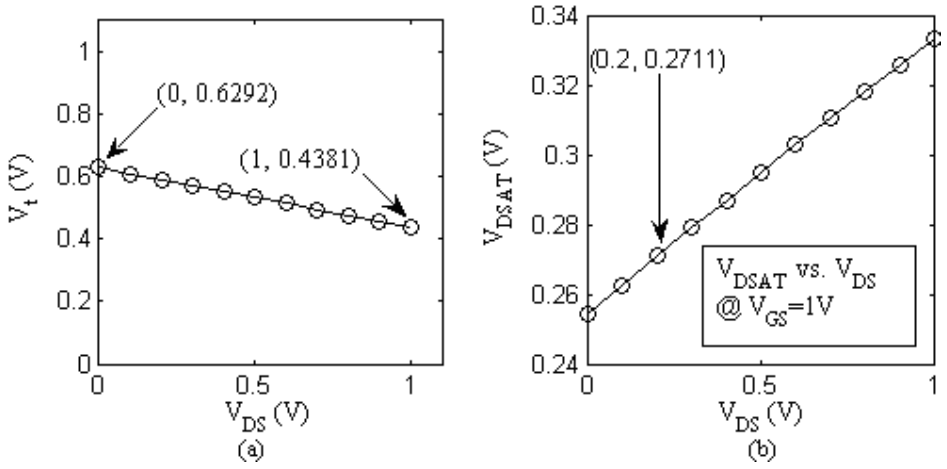

Fig. 1: (a) Threshold voltage (V_t) versus drain to source voltage (V_{DS}) of NMOS transistor. It shows V_t variation due to DIBL. (b) Drain to source saturation voltage (V_{DSAT}) versus drain to source voltage (V_{DS}) of NMOS transistor at 32 nm technology node.

3. SRAM CELL DESIGN METRICS, FAILURE MECHANISMS AND OPERATIONS

3.1 SRAM Design Metrics

Design of SRAM requires the smallest transistors, which are particularly sensitive to process variations. Balancing the trade-offs between small areas, low powers, fast reads/writes are an essential part of any SRAM design. That is, SRAM design requires balancing among various design criteria such as minimizing cell area using smaller transistor, maintaining read/write stability, minimizing power consumption by reducing power supply, minimizing read/write access time, minimizing leakage current, reducing bitline swing to reduce power consumption, improving soft error immunity, etc. Some of the design criteria are conflicting in nature. For example, higher cell ratio (CR) defined in [12] prevents read failure, but results in larger area and increased leakage.

3.2 SRAM Failure Mechanisms

The designer of SRAM should take care of the above design criteria along with various SRAM cell parametric failures which may occur mainly due to [13, 14] read, write access and hold failures. **Read Failure** – This failure occurs while reading the content of an SRAM cell. Assume that node QB in Fig. 2(a) is storing a "0" and BLB is discharging through MN3 and MN1. If the resistance of pull-down transistor MN1 is higher than that of pass transistor MN3, a voltage ripple V_{QB} is developed due to resistive divider formed by MN1 and MN3. If V_{QB} exceeds the switching threshold of the inverter formed by MP2 and MN2, the cell state flips while reading. The read failure can be reduced by increasing the difference between the voltage rise at the node storing "0" and the trip-point of the inverter associated with the node storing "1". **Write Failure** – It is an unsuccessful write to the SRAM cell. Write failure occurs if the node storing "1" cannot be discharged through the access transistors during the wordline turn on time. The write failure can be reduced by increasing the wordline turn on time with write access time increased, which unfortunately makes SRAM slower. **Access Failure** – Access failure occurs if the voltage difference between the two-bitlines at the time of sense amplifier firing remains below the offset voltage of the sense amplifier [12, 15]. Access failure occurs due to the reduction of the bit-line discharging current through the pass transistor and pull-down transistor. Clearly, a faster bitline discharge can be achieved by reducing the resistance in the discharge path by making the pull-down transistor stronger. However, such improvements come at the price of larger cell area which is not recommended for high density SRAMs. **Hold Failure** - The hold failure occurs due to high-leakage of the pull-down NMOS transistors connected to the node storing "1". In scaled technology, at lower supply voltage (V_{DD}), due to high leakage of the pull-down transistor, the node storing "1" reduces from V_{DD}. If that voltage becomes lower than the trip-point of the inverter storing "0" the cell flips in the hold mode. This failure can be avoided by reducing leakage in standby mode using high-V_t pull-down transistors. This improvement comes at the price of read delay.

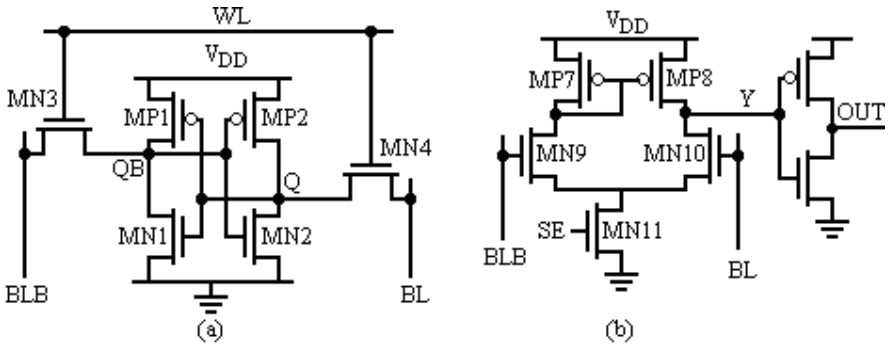

Fig. 2(a): Standard 6T SRAM cell [12]. (b): Sense amplifier [12].

3.3 SRAM's Mode of Operations

An SRAM cell offers the following basic modes of operation: **Data retention** or **Standby mode:** An SRAM cell is able to retain the data indefinitely as long as it is powered. **Read mode:** An SRAM cell is able to communicate its stored data. This operation does not affect the data i.e., read operation is non-destructive as compared to DRAM's read operation. **Write mode:** The data of an SRAM cell can be set to any binary value regardless of its original stored value.

Read Operation – During correct read operation, the stored data in Q (say, storing "1") and QB (storing "0") are transferred to the bitline (BL) and bitline bar (BLB) leaving BL at its precharged value and by discharging BLB through MN3 and MN1 (Fig. 2(a)). A careful sizing of MN1 and MN3 is needed to avoid accidental read upset due to building up of V_{QB} at QB. Minimum-sized transistors are necessary to design small-sized bitcell, which will result in longer T_{RA} (read access time) because of slow discharging of large bitline capacitance through small-sized transistor (offering higher resistance). As the difference between BL and BLB builds up, the sense amplifier shown in Fig. 2(b) [12] is activated by asserting sense enable (SE) high to accelerate the reading process. Boundary condition on MN1 and MN3 sizing to avoid read upset is achieved by equating discharging currents through MN3 and MN1 as given below:

$$\beta_{n,MN3}\left\{\left(V_{DD}-V_{QB}-V_{tn}\right)V_{DSATn}-\frac{V_{DSATn}^2}{2}\right\}=\beta_{n,MN1}\left\{\left(V_{DD}-V_{tn}\right)V_{QB}-\frac{{V_{QB}}^2}{2}\right\} \tag{3}$$

which simplifies to

$$V_{QB}=\left\{\begin{matrix}V_{DSATn}+CR\left(V_{DD}-V_{tn}\right)\\-\sqrt{V_{DSATn}^2\left(1+CR\right)+CR^2\left(V_{DD}-V_{tn}\right)^2}\end{matrix}\right\}\div CR \tag{4}$$

where CR is called cell ratio (CR) or β ratio defined as

$$CR=\frac{(W/L)_{MN1}}{(W/L)_{MN3}} \tag{5}$$

With the assumption that voltage ripple (V_{QB}) developed at QB will lie near zero and hence V_{DS} is arbitrarily taken to be 0.2V with the corresponding V_{DSAT} = 0.2711V and V_{tn} = 0.59V. The value of V_{QB} as a function of CR using 32 nm CMOS BPTM is computed on the basis of these assumption using (4) and (5). Fig. 3(a) plots the value of V_{QB} versus CR. In Section V, we have analyzed standard 6T SRAM cell and estimated static noise margin (SNM) to be 150 mV and read static noise margin (RSNM) to be 140 mV. At this technology node, where V_{tn} ranges from 0.4381 V to 0.6292 V for V_{DS} ranging from 1 V to 0 V (Fig. 1(a)), read upset may not occur due to voltage rise while reading, but as is evident from the Fig. 3(a), cell failure may occur due to static noise if CR is not kept greater than 0.7, because V_{QB}=147 mV at CR=0.7. Static noise is DC disturbance such as offsets and mismatches due to processing and variations in operating conditions. An SRAM cell should be designed such that under all conditions some SNM is reserved to cope with dynamic disturbances caused by α particles, crosstalk, voltage supply ripple, and thermal noise.

Write operation – A reliable write operation is possible if node storing "1" (say, Q) is pulled low enough – below the threshold voltage of MN1, so that writing a "1" is possible on to the other storage node (say, QB) by flipping the cell state. Sizing of the transistors MP2 and MN4 should be such that this occurs causing flipping of state, failing which will cause write failure. Sizing constraint on MP2 and MN4 to avoid write failure is obtained by equating currents passing through PM2 and MN4 as given below:

$$\beta_{n,MN4}\left\{(V_{DD}-V_{tn})V_Q-\frac{V_Q^2}{2}\right\}=\beta_{n,MP2}\left\{(V_{DD}-V_{tp})V_{DSATp}-\frac{V_{DSATp}^2}{2}\right\} \tag{6}$$

which simplifies to

$$V_Q=V_{DD}-V_{tn}-\sqrt{(V_{DD}-V_{tn})^2-2\frac{\mu_p}{\mu_n}PR\left\{(V_{DD}-V_{tp})V_{DSATp}-\frac{V_{DSATp}^2}{2}\right\}} \tag{7}$$

where PR is called pull-up ratio (PR) or γ ratio defined as

$$PR=\frac{(W/L)_{MP2}}{(W/L)_{MN4}} \tag{8}$$

Figure 3(b) plots voltage rise V_Q versus PR. To avoid write failure, PR must be chosen such that V_Q falls below threshold voltage of MN1. According to 32 nm CMOS Berkeley Predictive Technology Model (low power), $V_{tn} \approx 0.438$ V @ $V_{DS} = 1$ V. As can be seen from Fig. 3(b), $V_Q = 0.392$ V at PR = 2.1, which implies that PR can be raised up to 2.1 without write failure. But write static noise margin (WSNM) of 6T SRAM cell found later in Section V is 160 mV. Therefore, PR should be judiciously set below 2.1 so that some SNM is reserved to cope with dynamic disturbances caused by α particles, crosstalk, voltage supply ripple, and thermal noise.

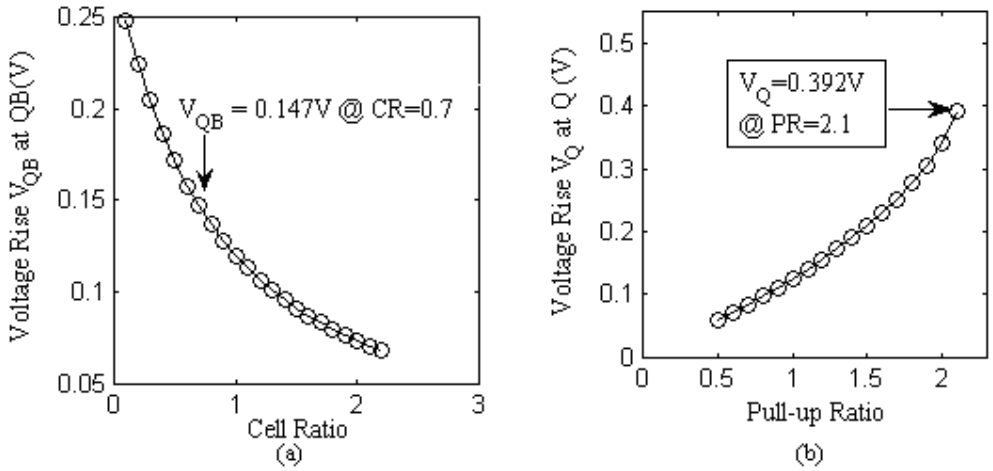

Fig. 3(a): Voltage ripple (V_{QB}) versus cell ratio while reading 6T SRAM cell. (b): Voltage ripple (V_Q) versus pull-up ratio while writing to 6T SRAM cell at 32 nm technology node.

4. 7T SRAM CELL AND DEVICE/TECHNOLOGY PARAMETERS

This paper analyzes design concepts addressing the realistic design challenges and issues such as hold power (H_{PWR}), static noise margin (SNM), read static noise margin (RSNM), write static noise margin (WSNM), read access time (T_{RA}), T_{RA} variability, read power (R_{PWR}), write access time (T_{WA}), and T_{WA} variability, write power (W_{PWR}) and W_{PWR} variability in nanoscale regime.

4.1 7T SRAM Cell

Authors in [16] proposed a 7T SRAM cell shown in Fig. 4 and reduced the activity factor α_{BL} for reduction of dynamic power while writing to a cell given by $P_{WRITE} = \alpha_{BL} \times C_{BL} \times V^2 F_{WRITE}$. But static power consumption in a SRAM cell is more critical than dynamic power consumption (during read and write operation due to bitline charging and discharging), since whole part of the cache remains idle most of the time except the row being read from or written to. Moreover, the 7T SRAM cell in [16] needs dual-V_t transistors requiring advanced technology and additional masking cost. In addition to that, its transistor sizing constraint for meeting its functionality poses additional area penalty.

Read/Write operation: Both BL and BLB are precharged high before and after each read/write operation. The write operation in 7T cell starts by turning off MN5. Complement of data to be written to node Q is applied to BLB and MN3 is turned on by asserting WL high, leaving MN4 off. BL and MN4 do not take part in write operation. During standby mode MN3 and MN4 are kept off applying WL and R low, MN5 is kept on asserting W high. Read operation of 7T cell is similar to that of 6T cell. BLB discharges through the critical read path consists of MN3, MN5 and MN1 during read operation with QB storing "0". BL discharges through the read path MN4 and MN2 during read operation with QB storing "1".

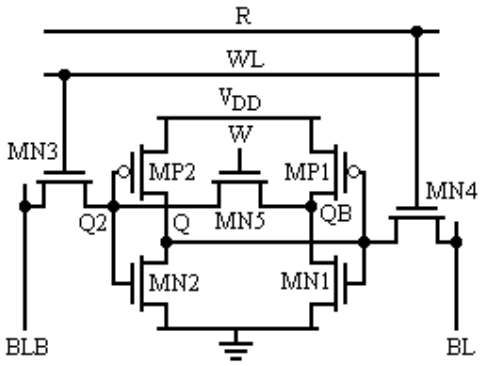

Fig. 4: 7T SRAM cell.

4.2 Device/Technology Parameters

Important device and technology parameters for the 6T and 7T SRAM cell are tabulated in Table 1. As MN1 ≥3 and MN2 ≥2 ensure stable read operation, the transistors in 7T SRAM cell are sized as shown in the Table 1. MN1 of 6T SRAM cell is upsized to make a fair comparison between 6T and 7T SRAM cell with an area penalty (defined as difference in cell area between 6T and 7T) of 11.1% in 7T compared to 6T SRAM cell. Table 2 presents comparison of cell area between 6T and 7T SRAM cell. It shows that the cell area of 7T is 10240 nm×nm whereas the cell area of 6T is 9216 nm×nm. The 11.1% area penalty is due to the functionality constraint of 7T SRAM cell. Other transistors used for the design are of minimum-sized. The simulation is run on HSPICE using 32 nm CMOS BPTM where $V_{tn0} \approx 0.63$ V and $V_{tp0} \approx -0.58$ V. The next Section presents a brief discussion on PVT variation and relates SRAM's various design metrics with it.

Table 1: Device/technology parameters.

Device/Parameter	**6T**		**7T**	
V_{tn0}	0.63 V		0.63 V	
V_{tp0}	-0.5808 V		-0.5808 V	
MP1	W = 32 nm	L = 32 nm	W = 32 nm	L = 32 nm
MP2	W = 32 nm	L = 32 nm	W = 32 nm	L = 32 nm
MN1	W = 64 nm	L = 64 nm	W = 96 nm	L = 32 nm
MN2	W = 32 nm	L = 32 nm	W = 64 nm	L = 32 nm
MN4	W = 32 nm	L = 32 nm	W = 32 nm	L = 32 nm
MN5	Absent		W = 32 nm	L = 32 nm

Table 2: Cell area comparison.

Parameter	Area (nm×nm)	% Area penalty
6T	9216	–
7T	10240	11.1

5. IMPACT OF PROCESS AND TEMPERATURE VARIATION

A large portion of the silicon area of many contemporary digital designs is dedicated to the storage of data and program instructions. More than half of the transistors in today's high-performance microprocessors are devoted to cache memories, and this ratio is expected to further increase. There is a prediction that memory modules typically realized with SRAM will occupy more than 90% of an SoC area in near future. High-performance work-stations and computers today contain several Giga bytes of semiconductor memory, a number that is continuously rising. Due to device scaling there are several design challenges for nanometer SRAM design. To reduce the power consumption, supply voltage has been scaled down which has consequently reduced the threshold voltage. Reduction of threshold voltage and ultra–thin gate oxide have increased subthreshold leakage and gate leakage current increasing standby power consumption. Besides this, read access time (T_{RA}) and write access time (T_{WA}) also get significantly affected. Intrinsic parameter fluctuation like random dopant fluctuation (RDF), line edge roughness (LER) and oxide thickness fluctuation further degrade the stability of SRAM cell. The intra-die V_t variation due to RDF results in failure of SRAM cell. The V_t shifts of the cell transistors due to RDF can be considered as independent Gaussian random variables with standard deviation given by [14, 17, 18]:

$$\sigma_{V_t} = \frac{qt_{ox}}{\varepsilon_{ox}} \sqrt{\frac{N_{SUB} W_{dm}}{3LW}} \tag{9}$$

where, t_{ox} is the oxide thickness, W_{dm} is the maximum width of depletion region, and N_{SUB} is the substrate doping concentration. In short-channel devices, a variation in channel length also induces a change in threshold voltage due to SCE (short-channel effect) [18]. T_{RA} and T_{WA} are crucial design criteria in high-performance microprocessor where SRAM cache is embedded. They are also crucial design metrics for designing FPGA where SRAM is embedded as look-up table. The distributions of T_{RA} and T_{WA} are even more problematic than their absolute values because meeting the design specification with variations in T_{RA} and T_{WA} is difficult for a designer. The spread in T_{RA} and T_{WA} are computed based on Central Limit Theorem [19]. As per the Central Limit Theorem, the distribution of a random variable (say, Y) which is the summation of a large number of independent random variables (say, X_1, ..., X_n) can be assumed to be Normal with mean and the standard deviation given by:

$$\mu_Y = \sum_{i=1}^{n} \mu_{Xi} \text{ and } \sigma_Y^2 = \sum_{i=1}^{n} \sigma_{Xi}^2 \tag{10}$$

If all the variables are identically distributed (i.e. all with equal mean μ_X and standard deviation σ_X) we further obtain:

$$\begin{aligned} &\mu_Y = N\mu_X \text{ and } \sigma_Y = \sqrt{N}\,\sigma_X \\ &\Rightarrow \frac{\sigma_Y}{\mu_Y} = \frac{1}{\sqrt{N}} \frac{\sigma_X}{\mu_X} \end{aligned} \tag{11}$$

From (11), it can be observed that, the spread (standard deviation/mean) of the variable Y is less than the spread in the variable X and the spread of Y reduces as more number of variables is added together. Monte Carlo simulation has been carried out to investigate the impact of the random variations of process parameters and temperature on the read access time (T_{RA}) and write access time (T_{WA}) which are presented in the next Section.

6. SIMULATION MEASUREMENTS AND COMPARISONS

This Section presents measurements of various design metrics which are measured during simulation on HSPICE using 32 nm CMOS BPTM [20]. Monte Carlo simulations are performed for the measurements. Monte Carlo simulation is a method for iteratively evaluating a design. The goal is to determine how random variation on process parameters, voltage and temperature affects the performance and reliability of a design. The arithmetic mean (μ) is the measure of central tendency that is found to fluctuate less than any other measure of central tendency if many samples are drawn from the same statistical data and standard deviation (σ) is a measure of dispersion (or variability) that states numerically the extent to which individual observations vary on the average.

6.1 Data Retention or Hold Power

The leakage current is the major contributor to the power consumption in the SRAM cell. The total leakage current in an SRAM cell mainly (excluding minor components) consists of the subthreshold leakage current (I_{sub}), the gate leakage current (I_{gate}) and the reverse-biased drain- and source-substrate junction band-to-band tunneling (BTBT) leakage current (I_{jn}) through different transistors as shown in Fig. 5 [21].

$$I_{sub} = I_{sub\,MN4} + I_{sub\,MN1} + I_{sub\,MP2}$$

$$I_{jn} = 2I_{jn\,MN3} + I_{jn\,MN4} + I_{jn\,MN1} + I_{jn\,MP2}$$

$$I_{gate} = I_{gd\,MN3} + I_{gs\,MN3} + I_{gd\,MN4} + I_{gd\,MP2} + I_{gd\,MN2} + I_{gs\,MN2} + I_{gd\,MP1} + I_{gs\,MP1} + I_{gd\,MN1}$$

$$I_{leak} = I_{sub} + I_{jn} + I_{gate}. \tag{12}$$

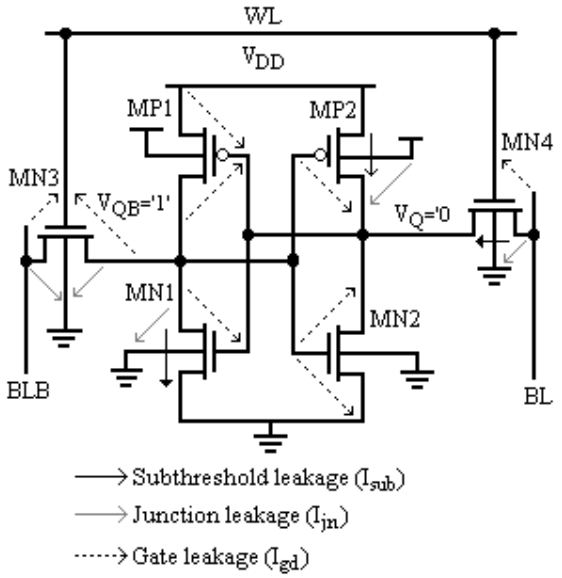

Fig. 5: Leakage components in standard 6T SRAM cell.

The above currents are dependent on stored value on the storage nodes Q and QB. These current equations are valid for V_{QB} = "1" and V_Q = "0". If the stored values on the nodes Q and QB are interchanged the current equations are required to be changed. The leakage power (H_{PWR}) or the data retention power or hold power consumed due to these leakage currents is measured at nominal voltage of V_{DD} = 1 V and at 0.9 V (−10% of V_{DD}) for both the designs. The measured results are reported in Table 3. The normalized values are presented in bracket. As can be observed from the Table 3, 7T SRAM cell consumes 57.3× and 30.7× higher hold power than that of 6T SRAM cell at V_{DD} = 1 V and at V_{DD} = 0.9 V with QB storing "1" respectively. The table also shows that the 7T cell consumes 2.1× at V_{DD} = 1 V and 1.76× at V_{DD} = 0.9 V higher hold power than that of 6T cell with QB storing "0" respectively. This is attributed to the extra transistor and cell area of 7T SRAM. The 7T SRAM cell has one transistor more, i.e. MN5 and its one cell occupies 11.1% extra area as compared to 6T SRAM cell. It is evident from Fig. 5 that the leakage increases due to increase in number of transistor and the area of the transistors involved in the SRAM cell.

Table 3: Hold power (H_{PWR}).

SRAM	**Hold Power while QB storing "1" (pW)**	**Hold Power while QB storing "0" (pW)**	**V_{DD} (Volt)**
6T	29.37(1)	29.37(1)	1
7T	1683(57.3)	61.94(2.1)	1
6T	19.73(1)	19.73(1)	0.9
7T	606.4(30.7)	34.66(1.76)	0.9

6.2 Static Noise Margin (SNM) Measurements

The static noise margin (SNM) of SRAM cell is defined as the minimum DC noise voltage necessary to flip the state of the cell. SNM of an SRAM is a widely-used design metric that measures the cell stability. Fig. 6 shows a conceptual test setup for measuring SNM. The measured results when plotted is called "butterfly curve". Fig. 7(a) and 7(b) plot “butterfly curve” of 6T and 7T SRAM cell respectively. The butterfly curve is obtained in the following way with the test circuit: 1) Word line (WL) is biased at ground and bit lines (BL, BLB) are biased at V_{DD}. 2) Voltage of N1 is swept from 0 V to V_{DD} while measuring voltage of QB. 3) Voltage of N2 is swept from 0 V to V_{DD} while measuring voltage of Q in the same way. 4) Measured voltages are plotted to obtain a butterfly curve. The side length of maximum square that can be fitted within the smaller wing of the butterfly curve represents the SNM of the cell. As can be seen in the plot, initially node QB remains stable, but as the noise source at node Q increases, QB starts falling, eventually flipping the cell. As can be seen in Fig. 7(a) and 7(b), the SNM of 6T SRAM cell is 150 mV where as the SNM of 7T SRAM cell is 240 mV, showing 60% improvement in 7T cell. To understand why this happens, consider the case when the value of noise voltage (V_N) increases from 0. This causes VTC (voltage transfer characteristic) for inverter 2 formed with MP2 and MN2 to move to the right and VTC^{-1} (inverse VTC) for inverter 1 formed with MP1 and MN1 in the figure to move downward. Once they both move by the SNM value, the curves meet at only two points. Any further noise flips the cell. It can be noted that, both the inverters of 7T have stronger NMOS transistors shifting its VTC to the left and pushing VTC^{-1} down.

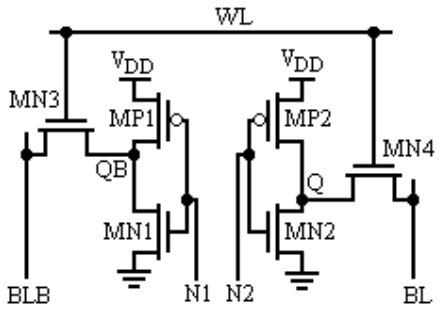

Fig. 6: Test setup for measuring SNM.

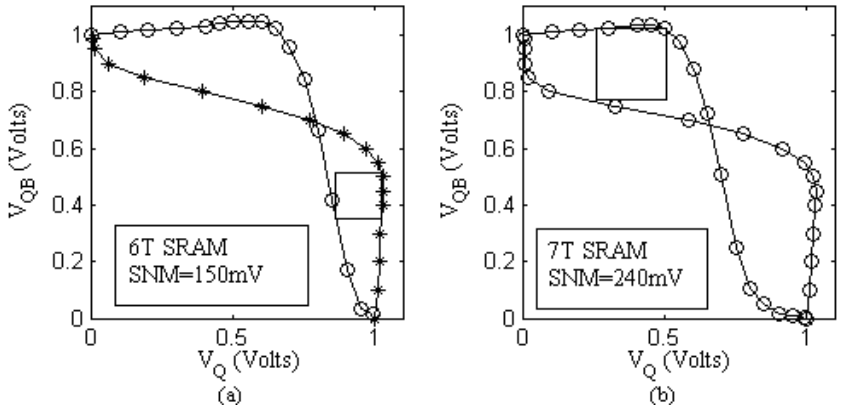

Fig. 7: (a) Static noise margin (SNM) of 6T and (b) SNM of 7T SRAM cell.

6.3 Read Static Noise Margin (RSNM) Measurements

The SRAM cell is most vulnerable to noise during read access since the "0" storage node rises to a voltage higher than ground due to a voltage division along the access transistor and inverter pull-down NMOS drivers between the precharged bitline and the ground terminal of the cell. The ratio of the widths of the pull-down transistor to the access transistor, commonly referred to as the cell ratio or β ratio, determines how high the "0" storage node rises during a read access. Smaller cell ratios translate into a higher voltage drop across the pull-down transistor, requiring a smaller noise voltage at the "0" storing node to trip the cell. Read static noise margin (RSNM) is a measure of how much noise voltage required at the node storing "0" to flip the state of an SRAM cell while reading. Therefore, RSNM is more critical design metric of SRAM cell than SNM. RSNM of both the design has been measured during simulation. Figure 8(a) and 8(b) plot the RSNM of 6T and 7T SRAM cell respectively. The plots show that the 7T outperforms 6T in terms of 71.4% improvement in RSNM. These butterfly curves are obtained with test setup shown in Fig. 6, and using the same measuring technique as done for SNM except biasing WL at V_{DD}.

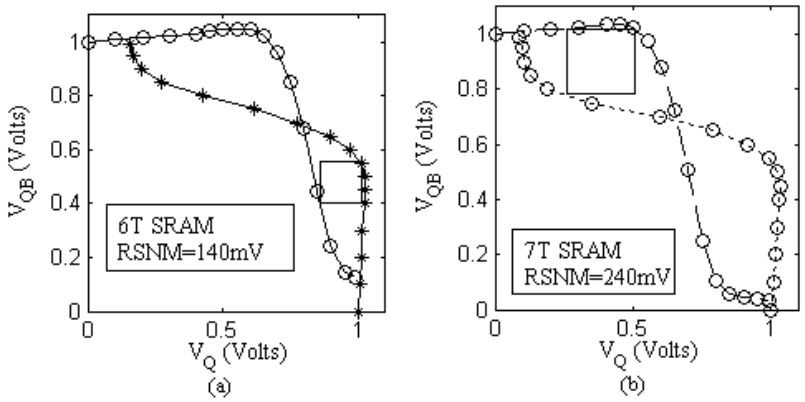

Fig. 8: (a) Read static noise margin (RSNM) of 6T and (b): RSNM of 7T SRAM cell.

6.4 Write Static Noise Margin (WSNM) Measurements

The write static noise margin (WSNM) is another SRAM cell's design metric, which implies the write ability of SRAM cell. It is a measure of ability of the cell to pull down the node storing "1" to a voltage less than the switching threshold voltage of the other inverter storing "0" so that flipping of the cell state occurs. WSNM is measured while writing "1". It is observed from simulation results that there is 50% improvement in WSNM in 7T SRAM cell.

6.5 Read Access Time and its Variability Measurements

The read access time (T_{RA}) measurements are taken with QB storing "0". The measured average T_{RA} are plotted in Fig. 9(a) and reported in Table 4. As evident from the Fig. 9(a) and Table 4, the read delay of 7T is increased by 13.1% and 16.7% at V_{DD} = 1 V and 0.9 V respectively compared to 6T SRAM cell. This is attributed to the fact that the read path of 7T cell consists of MN1, MN5 and MN3 that represents a critical read path with QB storing "0". This longer read path offers higher resistance and therefore lesser BLB discharge current while reading. Also to understand this fact, note that the V_{QB} developed during BLB discharge makes V_{BS5} negative, resulting in an increase in the threshold voltage (larger body effect) of MN5 thereby reducing discharge current. The spread of T_{RA} of both the SRAM cells are plotted in Fig. 9(b) and tabulated in Table 5. The Fig. 9(b) and Table 5 show that the spread of T_{RA} of 7T is 1.2× wider than that of 6T at V_{DD} = 1 V and 1.18× wider than that of 6T at V_{DD} = 0.9 V. It shows that 6T SRAM is more robust against process variations. This is attributed to the fact that MN1 of 6T is longer than that of 7T. Longer device is less sensitive to Drain-Induced Barrier Lowering (DIBL) and Short-Channel Effect (SCE). Therefore, 6T cell is less sensitive to PVT variation compared to 7T cell.

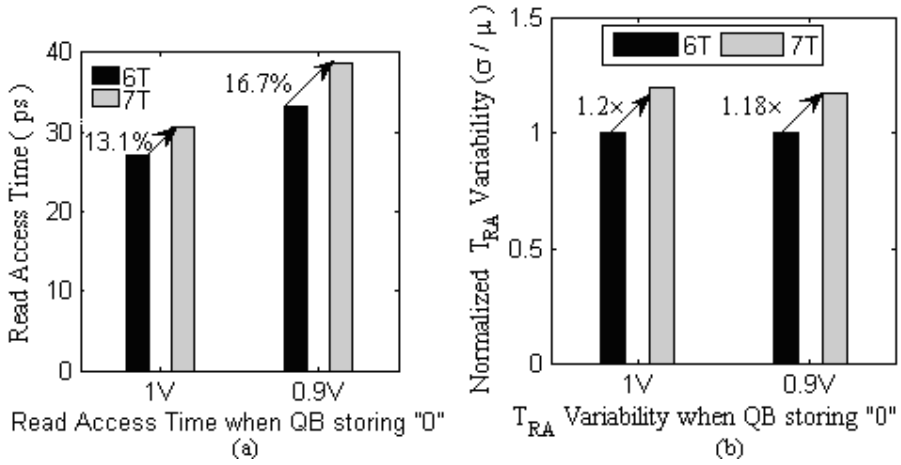

Fig. 9: (a) Read access time (T_{RA}). (b) Read access time variability.

Table 4: Average read delay.

SRAM	Average T_{RA} (μ) while QB storing "0" (ps)	V_{DD} (Volt)
6T	27.20	1
	33.25	0.9
7T	30.75	1
	38.79	0.9

Table 5: Read delay variability.

SRAM	T_{RA} Variability (σ/μ) while reading with QB storing "0"	V_{DD}(Volt)
6T	0.009(1)	1
7T	0.011(1.2)	
6T	0.011(1)	0.9
7T	0.013(1.18)	

6.6 Read Power Measurements

Power consumption during read operation is also an important parameter of SRAM cell as it contributes a considerable amount to total power. The read power is measured at supply of 1 V and 0.9 V. The measured values of average (μ) read power (R_{PWR}) and R_{PWR} variability (σ/μ) are tabulated in Table 6. The normalized values of variability are reported in bracket. The values show that the 7T cell offers saving in R_{PWR} (65.6% @ V_{DD} = 1 V and 71.4% @ V_{DD} = 0.9 V), while reading with QB storing "1". The normalized values of the R_{PWR} variability indicate that 6T cell is robust against PVT variation by 3.9× @ 1 V and 3.7× @ 0.9 V.

Table 6: Read power and its variability measurements.

SRAM	R_{PWR} (σ) while QB storing "1" (nW)	R_{PWR} (μ) while QB storing "1" (nW)	R_{PWR} Variability (σ/μ)	V_{DD} (Volt)
6T	1.263	95.99	0.013(1)	1
7T	1.445	32.98	0.044(3.9)	
6T	0.7898	79.07	0.010(1)	0.9
7T	0.8283	22.64	0.037(3.7)	

6.7 Write Access Time Measurements

The write access time (T_{WA}) is measured during simulation and plotted in Fig. 10(a), which shows that the 7T cell takes 16.6× @ 1 V and 41.7× @ 0.9 V longer time than 6T cell for writing "1" at QB. Fig. 10(b) plots the write delay variability while writing "1" at QB. It is evident from Fig. 10(b) that the 7T SRAM cell is more prone to PVT variation − 3.4× @ 1 V and 3× @ 0.9 V compared to 6T SRAM cell.

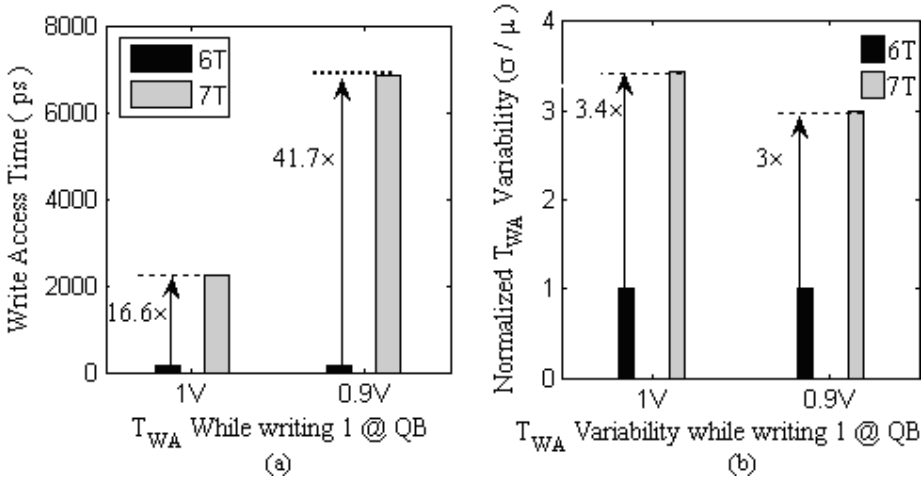

Fig. 10: (a) Write access time (T_{WA}). (b) Write access time variability.

6.8 Write Power Measurements

Power consumption during write operation is measured while writing "1" at QB. The measurement results are plotted in Fig. 11(a). It is clear from the Fig. 11(a) that the 7T cell offers 89% reduction in write power @ V_{DD} = 1 V and 93.6% reduction @ V_{DD} = 0.9 V.

Fig. 11(b) plots write power (W_{PWR}) variability while writing 1 @ QB. It is observed from this plot that 6T cell is more robust against PVT variation. In this plot, 7T cell shows 1.3× @ 1 V and 1.4× @ 0.9 V W_{PWR} variability.

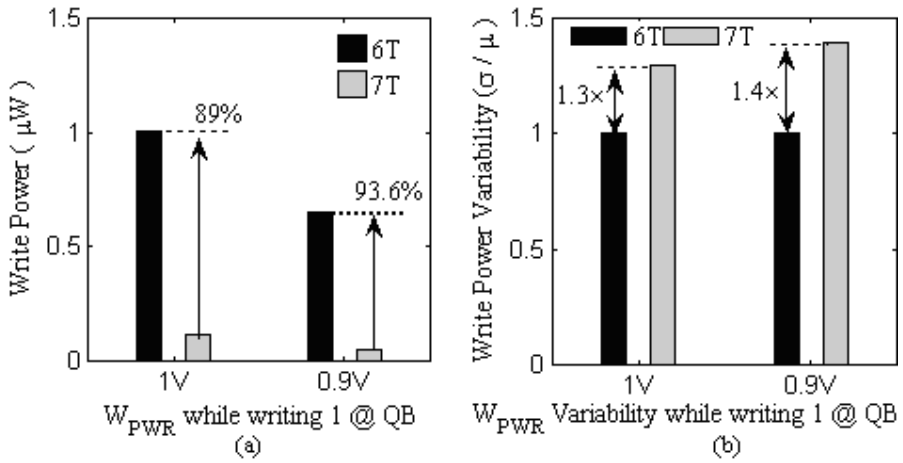

Fig. 11: (a) Write power and (b) Write power variability.

7. CONCLUSION

This paper has analyses the impact of process, voltage and temperature variations on read/write access time and read/write power of 6T and 7T SRAM cells. All the simulations are performed at the nominal voltage of V_{DD} = 1V with – 10% variations. The process parameters (±10%) as well as temperature (from 24°C to 134°C) are varied Normally using Gaussian function. Simulation measurements are taken for both the designs against $\pm 3\sigma$ variation of process parameters and temperature. The analysis shows that 6T SRAM cell is more robust against process variation in terms of most of the design parameters compared to 7T SRAM cell.

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