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A Low Voltage Delta-Sigma Fractional Frequency Divider for Multi-band WSN Frequency Synthesizers

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Abstract: A 1 V low voltage delta-sigma fractional-N frequency divider for multi-band (780/868/915 MHz and 2.4 GHz) WSN frequency synthesizers is presented. The frequency divider consists of a dual-modulus prescaler, a pulse-swallow counter and a delta-sigma modulator. The high-speed and low-voltage phase-switching dual-modulus prescaler is used in the frequency divider. Low threshold voltage transistors are applied to overcome low voltage supply and forward phase-switching technique is adopted to prevent glitches. The modified delta-sigma modulator with long output sequence length and less spurs is adopted to minimize the fractional spurs. The frequency divider is designed in 0.18 μm TSMC RF CMOS technology under 1 V supply instead of the standard 1.8 V supply. The total chip area is 1190 μm × 485 μm including I/O pads. The post simulation results show the frequency divider operates normally over a wide range of 1.3-5.0 GHz and the core circuit (without test buffers) consumes 2.3 mW. *Copyright © 2013 IFSA.*

Keywords: Low voltage, Fractional frequency divider, Delta-sigma modulator, Phase-switching prescaler, Wireless sensor networks.

1. Introduction

Wireless sensor networks (WSN) have attracted increasing attention and interest in wireless communication. ZigBee (IEEE 802.15.4) has been introduced into WSN because of low-cost, low power consumption, extended battery life, flexibility and autonomy. In WSN transceiver system, the frequency synthesizer based on phase-locked loop (PLL) structure generates the local oscillator signals for the transmitter and receiver [1, 2]. In the frequency synthesizer design, the frequency divider is the mixed signal block combining the analog and digital circuits [3]. Special consideration is needed when designing the low voltage and high-speed prescaler in the frequency divider because the prescaler works at the low supply voltage 1 V and the highest frequency of 5 GHz. As the load of voltage-controlled oscillator, the frequency divider should have small input capacitance. This paper presents the fractional-N frequency divider for dual-band ZigBee frequency synthesizers. In this paper, 1 V low voltage power supply is used instead of the typical 1.8 V for the standard 0.18 μm TSMC RF CMOS technology.

The paper is organized as follows. The architecture of the frequency synthesizer and the frequency divider are illustrated in Section 2. The circuit design is given in Section 3. Section 4 presents the layout design and post simulation results. The conclusion is shown in Section 5.

2. Architecture of Frequency Synthesizers

The architecture of the frequency synthesizer and the fractional-N frequency divider are illustrated in Fig. 1. The frequency synthesizer consists of voltage-

controlled oscillator (VCO), phase frequency detector (PFD), charge pump (CP), automatic frequency calibration (AFC), high-speed frequency dividers and programmable dividers. The fractional-N frequency divider is shown in the box in Fig. 1.

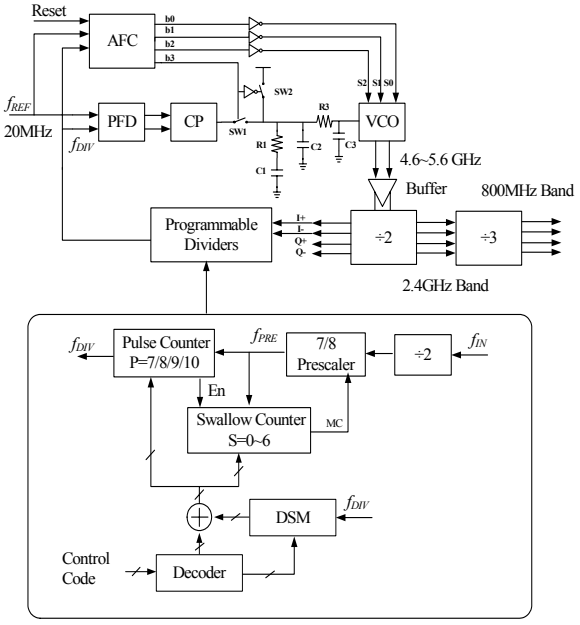

Fig. 1. Architecture of the frequency synthesizer and the fractional-N frequency divider.

The circuit is designed for low-Intermediate-Frequency (IF) transceiver with 2 MHz intermediate frequency [4]. According to specifications, ZigBee network operates in the 2.4 GHz industrial-scientific-medical (ISM) band and 780/868/915 MHz band. Since two bands obey the same specification, the frequency synthesizer can generate two groups of LO signals by using divider-by-3 for the transmitter and receiver [5]. IEEE 802.15.4 standard specifies operation in the unlicensed 2.4 GHz (worldwide), 915 MHz (Americas and Australia), 780 MHz (China) and 868 MHz (Europe) ISM bands. The center frequency of channels is as follows,

$$\begin{aligned}
&China\ band: && F_c = 780 + 2k\ MHz, && k = 0,...,3\\
& && F_c = 780 + 2(k-4)\ MHz, && k = 4,...,7\\
&Europe\ band: && F_c = 868.3 MHz, && k = 8\\
&Americas\ band: && F_c = 906 + 2(k-9) MHz, && k = 9,...,18\\
&2.4 GHz\ band: && F_c = 2405 + 5(l-11) MHz, && l = 11,...,26
\end{aligned} \quad (1)$$

From the specification, the frequency resolution of the frequency synthesizer is 100 kHz.

VCO operates at the frequency of approximately 5 GHz to generate in-phase and quadrature signals with divider-by-2. Using the high-speed divider-by-2 and divider-by-3, the synthesizer outputs the required frequencies. The frequency divider consists of pulse-swallow counter, dual-modulus prescaler (DMP), delta-sigma modulator (DSM) and the decoder. The DMP operates at the highest frequency of the frequency divider, which is approximately 2.4 GHz. DMP works under divide-by- N mode when the mode control input MC is high and divide-by-$(N+1)$ mode otherwise. Assume that the modulus of the pulse and swallow counter is P and S, respectively, then in each output cycle, the prescaler divide ratio is $N+1$ for S times, and N for the remaining $P-S$ times. Therefore, the total frequency divide ratio is:

$$M = (N+1)\cdot S + N\cdot(P-S) = P\cdot N + S \quad (2)$$

Note that P must be equal to or greater than S for continuous divide ratios. The lower boundary of continuous divide ratios of a pulse-swallow divider with a dual-modulus prescaler is $N\cdot(N-1)$. If the total divide ratio is not large, the modulus N of the prescaler needs to be reduced correspondingly. Since the pulse-swallow counter is realized by digital process, the maximum operating frequency is limited (about 300 MHz), especially under 1 V supply. In consideration of these conditions, the prescaler modulus $(N/N+1)$ is 7/8, and the programmable P and S counters are 4-bit and 3-bit, respectively. Before 7/8 dual-modulus prescaler, divider-by-2 is added to lower the operating frequency of pulse-swallow counters. Therefore, from the point of PLL output to the point of reference signal, the divide ratio is no longer continuous and the counting interval is two. This does not affect the total divide ratio because the frequency resolution of PLL is determined by DSM in the fractional-N frequency divider.

Assuming the input number of DSM is K with k-bit accuracy, the average output of DSM is $K/2^k$, which is a fractional number between 0 and 1. This offset $K/2^k$ is added to the input of pulse-swallow counters and the total divide ratio is $M+K/2^k$. The frequency resolution of PLL is therefore $f_{REF}/2^k$, where f_{REF} is the reference frequency. With 20MHz reference frequency and 20-bit Delta-Sigma modulator, the synthesizer achieves the resolution of $f_{REF}/2^{20} \approx 19Hz$, which meets the standard. The input number of pulse-swallow counter and DSM is given by the decoder.

3. Circuit Design

3.1. Dual-Modulus Prescaler

Two different structures are used to realize the high speed dual-modulus prescaler. The first architecture is using a synchronous divider and an asynchronous divider [6, 7]. Since the synchronous

divider, which usually consists of several full-speed D-flipflops, operates at the highest frequency, this architecture consumes more power and seriously increases the clock load. Another architecture that is proposed to exploit the full speed performance of the flip-flop is phase switching [8, 9]. The phase switching prescaler makes the most use of the D-flip-flop, since no additional logic is needed in the high frequency critical path. The dual-modulus function is realized using phase-select block to switch between different phase signals. In this paper, 1 V low voltage power supply is used instead of the typical 1.8 V supply. When the phase-switching prescaler works under low power supply, it suffers some problems at the high frequency. Low-voltage circuit techniques are adopted to solve these problems.

Fig. 2 depicts the block diagram of the phase-switching dual-modulus prescaler. The prescaler consists of full-speed divider-by-two, half-speed divider-by-two, phase-select block and asynchronous divider-by-2. The half-speed divider-by-2 generates four-way 90°-spaced signals for the phase-select block. When modulus control signal MC is logic zero, the phase-select block stops to work and one of the four-way signals is selected to the asynchronous divider-by-2. In this case, the total divide ratio is 8. When the modulus control input MC is logic one, the phase control block starts generating control pulses for the phase-select block. At every rising edge of the output signal f_{out}, the phase-select block selects one of four-way signals that lead its previous signal by 90°. As a result, the phase-select output Y leads by 90°, which means one clock leading of the prescaler input signal f_{in}. In this case, the total divide ratio is 7. If phase switching direction is backward, that is, the total divide ratio is 9 when MC is logic one, glitch may occur when improper phase-switch happens. The glitch-free method is proposed by reversing phase switching sequence and applied in this paper [10].

The full-speed divider-by-two is the frequency-limiting block in the architecture and the schematic is shown in Fig. 3. It consists of two latches connected in a master-slave configuration with feedback and each latch is realized by the source coupled logic (SCL) circuit [11]. The behavior of divider-by-two can be easily analyzed by using the method based on the static operation of the flip-flop. Due to its static nature, this architecture can work at higher frequency than dynamic flip-flop. M1 and M2 in Fig. 3 are the clock input pair transistors while M3 and M4 are the driving transistors, which read data from the previous latch. The latch transistors M5 and M6 keep the data constant in the latching period.

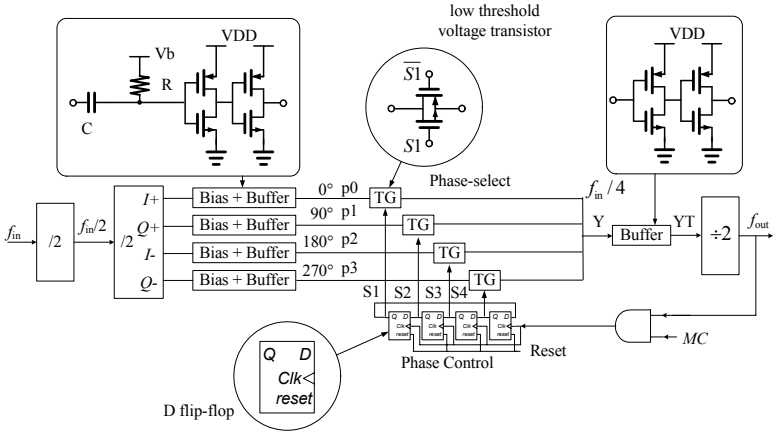

Fig. 2. Block diagram of the phase-switching dual-modulus prescaler.

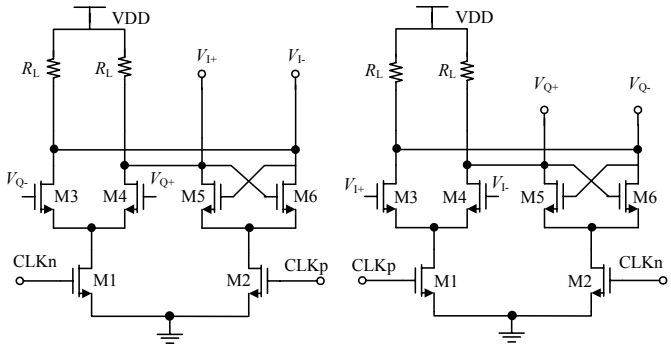

Fig. 3. High-speed frequency divider.

The phase-select block is implemented by using complementary transmission gate logic shown in Fig. 2. Using transmission gate as phase-select block has pros over the 4 to 1-Mux implemented by purely digital circuitry because the number of transistors is less and the working frequency is higher than digital circuitry (about 1 GHz). Since the circuit works under 1 V supply, the output of transmission gate may seriously distort with respect to the input signal. When the transmission gate is implemented by normal threshold voltage (about 500 mV-600 mV) transistors, the output signal can not drive the subsequent stage and asynchronous divider-by-2 doesn't operate correctly as a result. To overcome low voltage of 1 V supply, low threshold voltage transistors are applied in the traditional transmission gate. The effect is obvious that the difference between the input and the output is negligible.

Note that four-way 90°-spaced signals imply each signal has 50 % duty cycle. However, the output driving ability of the second divide-by-two divider is not strong enough when frequency is as high as 1 GHz. Hence, the duty cycle of the four-way signals is no longer 50 % duty cycle when parasitic capacitors and resistors from layout are introduced, especially under 1 V supply and ss (slow-slow) process. As a result, the output of phase-select block may be wrong and the divide-by-N divider fails to operate properly. The simple solution is adding buffers after the second divider to improve driving ability and thus the signal with fast rising and falling edges is obtained. The buffers are also realized by low threshold voltage transistors to ensure the correct operation of the phase-select block at the high frequency, low voltage supply and the worst process. The bias circuit before buffers is to overcome process and temperature variation.

3.2. Pulse-Swallow Counter

Fig. 4 shows the block diagram of the programmable frequency divider. The output of the decoder sets the initial numbers of pulse and swallows counters, while MC is set high and DMP works in divide-by-7 mode. After swallow-counter S counts down to zero, MC is set low and DMP divides by 8. If pulse counter is greater than 0, it continues counting down to zero. Once the pulse counter is equal to zero, swallow counter is reset and a new cycle begins. An inverter is inserted between pulse-swallow counter and the prescaler to remove glitch caused by the delay of MC. The modulus control signal MC, which is the output of pulse-swallow counter and the input of prescaler, lags the output signal f_{out} of prescaler. If the inverter is omitted, a glitch may occur when MC and f_{out} pass through AND gate. As a result, unwanted phase switching happens and the total divide ratio is wrong.

When DSM is disabled, the programmable frequency divider operates in integer mode and initial numbers of pulse and swallow counters keep constant. When DSM is enabled, the initial numbers of pulse and swallow counters, which are the sum of the decoder output and DSM output, change all the time. The instantaneous divide ratio is not constant while the mean value is equal to the required divide ratio.

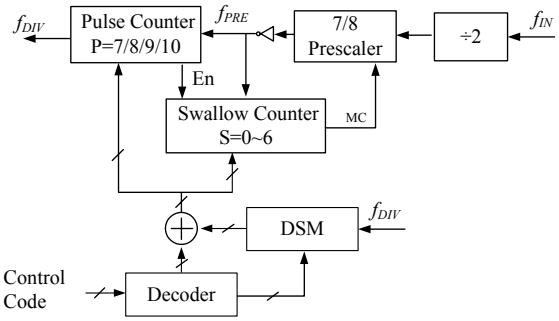

Fig. 4. Block diagram of the programmable frequency divider.

3.3. Delta-Sigma Modulator

In fractional-N frequency synthesizers, fractional multiples of the reference can be synthesized, allowing a higher reference frequency for a given frequency resolution, therefore, the loop bandwidth can be increased without deteriorating the spectral purity. However, fractional spurs become a problem in fractional-N frequency synthesizers. Several techniques are proposed to minimize fractional spurs and one of them is using ΣΔ modulators [12, 13]. The existence of pattern noise, which is caused by the quantization error, remains a serious problem in the ΣΔ fractional-N frequency synthesizers, where spectral purity is of utmost importance. Several improvements can be made to break the patterns in the ΣΔ modulator output. Moving to higher-order ΣΔ modulators is a first solution to remove the pattern noise. A second option to improve the prediction made by the modulator and further randomize its output is multi-bit quantization instead of single-bit. Another possibility is to add noise, namely dither, to the input signal.

DSM is usually implemented in digital circuit, hence, DSM is a finite state machine (FSM) because it is realized using finite precision arithmetic units and a finite amount of hardware. Without dithering, the DSM is a deterministic FSM with a unique rule for transitioning from each state to the next. In other words, DSM always produces a constant or a periodic output signal when the input is constant. In particular, the period of the signal depends on the input, the initial conditions, and the architecture of the DSM.

The traditional MASH (multi-stage noise-shaping) or cascade 1-1-1 ΣΔ modulator is shown in Fig. 5.

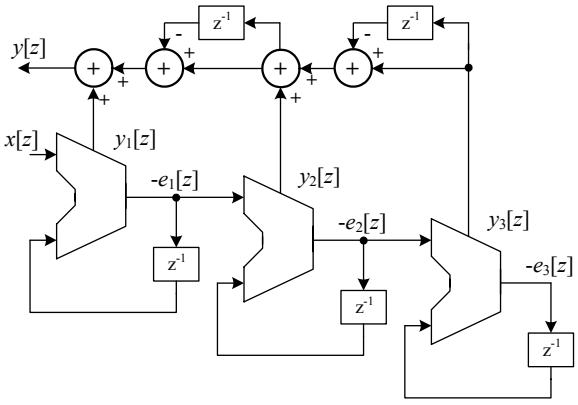

Fig. 5. Architecture of MASH 1-1-1 ΣΔ modulator.

The Z-domain expression can be written as,

$$\begin{cases} y_1(z) = x(z) + (1-z^{-1})e_1(z) \\ y_2(z) = -e_1(z) + (1-z^{-1})e_2(z) \\ y_3(z) = -e_2(z) + (1-z^{-1})e_3(z) \end{cases} \quad (3)$$

And the output is obtained,

$$\begin{aligned} y(z) &= y_1(z) + (1-z^{-1})y_2(z) + (1-z^{-1})^2 y_3(z) \\ &= x(z) + (1-z^{-1})^3 e_3(z) \end{aligned} \quad (4)$$

Then, we have noise transfer function of MASH 1-1-1 ΣΔ modulator,

$$NTF(z) = (1-z^{-1})^3 \quad (5)$$

From equation, the input signal $x(z)$ keeps the same in the output $y(z)$ and the quantization error is moved to high frequency. The order of noise shaping is increased by MASH 1-1-1.

In this paper, a modified MASH 1-1-1 is applied in the frequency synthesizer and the architecture is shown in **Error! Reference source not found.** [14].

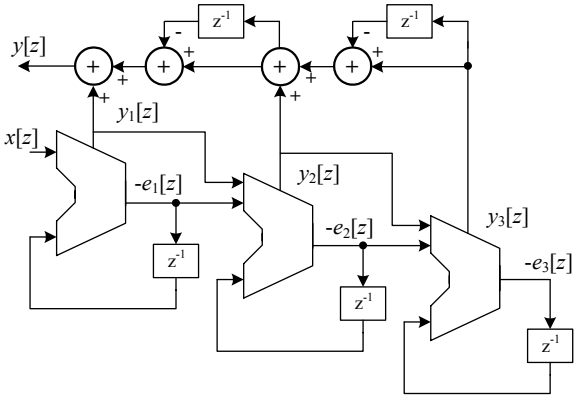

Fig. 6. Architecture of modified MASH 1-1-1 ΣΔ modulator.

The traditional MASH structure cascades a number of EFMs (error feedback modulator) by linking the quantization error signal of an EFM to the input of the next-stage EFM, while the modified MASH structure connects the output and the quantization error signal of an EFM with the input of the next-stage EFM. The modified MASH structure can increase the sequence length. The longer sequence length leads to the wider distribution of the quantization noise power and less spurs.

The input $x[n]$ is a k-bit integer value ranging from 0 to $M-1$, where $M = 2^k$. After calculation, we have signal transfer function (STF) and noise transfer function (NTF) of the modified MASH structure with three-order DSM.

$$\begin{aligned} STF(z) &= \frac{1}{M} + \sum_{n=2}^{3} \frac{1}{M^n}(1-z^{-1})^{n-1} \\ NTF(z) &= \frac{1}{M}(1-z^{-1})^3 \end{aligned} \quad (6)$$

The STF equation includes an all-pass filter and two high-pass filters. Since the input signal is constant, it is removed by high-pass filters and thus STF can be regarded as an all-pass filter. The quantization noise is shaped by high-pass filters, which is similar to the traditional DSM.

Error! Reference source not found. compares sequence length and input range of the traditional and modified MASH structure. The minimum sequence length of the traditional MASH structure is very short and thus some input numbers may cause serious spurs. The minimum sequence length of the modified MASH is considerably increased to $2M^2$.

Table 1. Comparison of MASH 1-1-1 Structures.

Architecture	Maximum Sequence Length	Minimum Sequence Length	Input Range
Traditional MASH	M	2	$0 \sim M-1$
Modified MASH	M^3	$2M^2$	$0 \sim M-1$

In this paper, 20-bit DSM with 3-bit output sequence is applied in the fractional-N frequency synthesizer and thus $M = 2^{20}$. Wide distribution of the quantization noise power is obtained when the sequence length is long. For input value of $M/2$ represented in 20 bits, the output spectra of the modified MASH and the theoretical NTF is plotted in 0.

The dashed line denotes the theoretical NTF curve, and the solid line represents the output spectra of the modified MASH. The modified MASH structure effectively removes spurs while keeping the noise-shaping property. The curves show that the spectra of the modified MASH are smooth,

and no noticeable spurs appear. This good property helps to minimize fractional spurs in the output of frequency synthesizers.

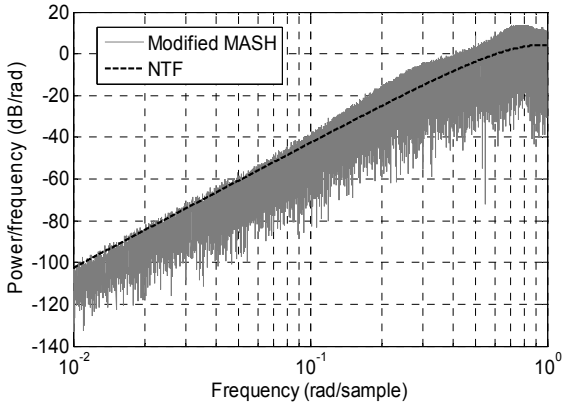

Fig. 7. Output spectra for an input value of $M / 2$.

4. Layout Design and Post Simulation Results

The fractional-N frequency divider is implemented in 0.18 μm TSMC RF CMOS technology. The supply voltage is 1V instead of standard 1.8 V to reduce the active power consumption and digital switching noise generation. Fig. 8 shows the layout of the fractional-N frequency divider. The total chip area occupies 1190 μm × 485 μm including I/O pads. To preserve the performance of high frequency circuits, layout design is critical because the parasitic resistance and capacitance will cause serious degradation. In consideration of symmetry of layout, differential structure is adopted in the high-speed divider-by-2. Common centroid technique is applied in the layout to improve the match between devices and some dummy devices are placed to overcome process variation.

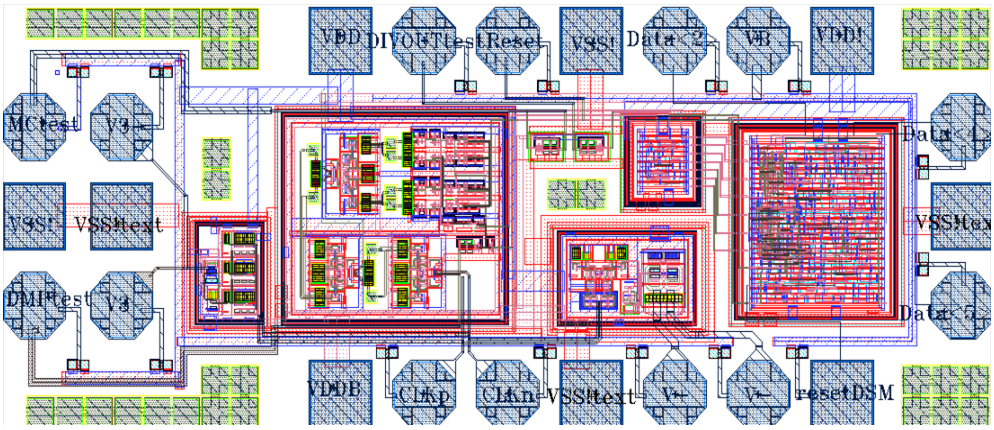

Fig. 8. Layout of the fractional-N frequency divider.

The pulse-swallow counter operates at lower frequency about 200 MHz and DSM works at about 20 MHz due to the low operating frequency, pulse-swallow counter and DSM can be implemented by digital process which is easier to design. Based on Artisan 0.18 μm standard cell library, Verilog HDL code describing the function is synthesized using Synopsys Design Complier. Then, auto place and route tool, Astro, is utilized to generate schematic and layout. It is worth mentioning that 0.18 μm standard cell library uses 1.8 V as the standard supply voltage, while 1 V is used in this paper. The verification of circuit function is necessary in transistor level to ensure the frequency divider functions normally. The fractional-N frequency divider is actually mixed signal circuit, therefore, guard rings in layout are adopted to isolate the digital and analog circuits.

The post simulation results show that the fractional-N frequency divider operates correctly from 1.3-5.0 GHz under 1 V supply and different PVT condition, and the power consumption of the core circuit (without test buffers) is about 2.3 mW, including analog and digital circuit. Fig. 9 shows the transient waveforms of the input and output of DMP. The 5 GHz input signal has amplitude of 150 mV. For the convenience of testing (load of 50 Ω), buffers are added to drive the load. From the waveform, DMP works correctly at the frequency well above the required frequency (about 2.4 GHz).

Fig. 10 shows waveforms of the input and output of fractional-N frequency divider. From top to bottom are DMP output signal, MC signal and divider output signal, which drive 50 Ω load. The frequency of the input signal is 2604.9 MHz, which equals 3×868.3 MHz. The input control code is 000100, which means the fractional divide ratio is 130.245. As the instantaneous divide ratio is not constant, each cycle of divider output signal has a different period. The calculated frequency of the divider output signal after sufficiently long time is 20 MHz. Therefore, the fractional-N frequency divider functions normally.

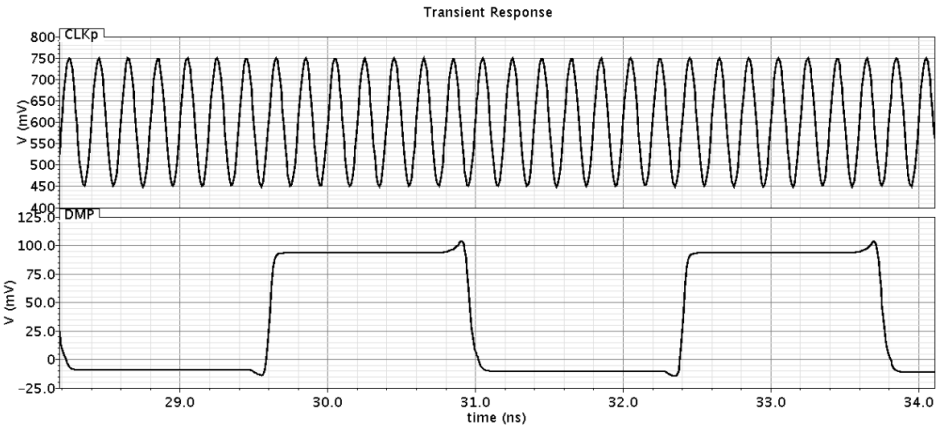

Fig. 9. Waveforms of the input and output of DMP.

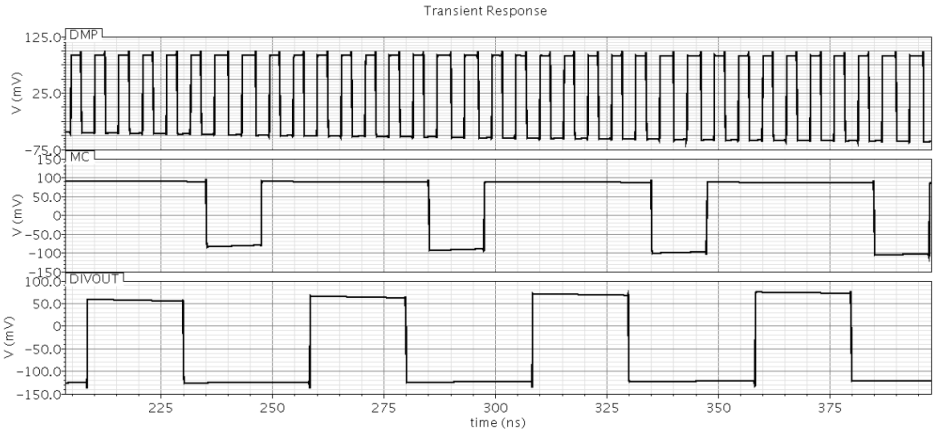

Fig. 10. Waveforms of the input and output of the fractional-N frequency divider.

5. Conclusions

In this paper, the design and performance of the high-speed, low-voltage CMOS delta-sigma fractional-N frequency divider for multi-band ZigBee frequency synthesizer is presented. The frequency divider consists of the dual modulus prescaler, the pulse-swallow counter and the delta-sigma modulator. The modified DSM with long output sequence length is adopted to minimize the fractional spurs. The frequency divider is designed and implemented in 0.18 μm TSMC RF CMOS technology under 1 V supply. Low voltage and mixed signal techniques are applied in the design. The frequency divider operates normally over a range of 1.3-5.0 GHz and the power consumption of the circuit is about 2.3 mW.

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