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Improved Efficiency and Voltage Gain Conversion Ratio using Inductor Model based modified Dickson Charge Pump

Gyan Prabhakar[1,*], Rabindra Kumar Singh[1] and Abhishek Vikram[2]

[1]*Dept. of Electronics Eng. Kamla Nehru Institute of Technology, Sultanpur, Dr. APJ Abdul Kalam Tech. Univ. Lucknow, U.P., India.*
[2]*Dept. of Electrical Eng. Motilal Nehru National Institute of Technology, Allahabad, UP, India.*

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Abstract

This paper proposes an inductor-based DC-DC conversion technique using the 5-stage Dickson charge pump that achieves efficiency up to 96%. The converter that the Dickson charge pump is built on is a novel series inductor and parallel capacitive construction, that is profitable for energy harvesting applications. In this paper, we have shown the use of an inductor in five stage Dickson charge pump to generate an output voltage of 8.76 V at 20 Ω resistive load with a 50 MHz external frequency. Least drop in voltage is at output capacitor that is used as an energy storage element. In the experiment, the integrated charge-up converter is based on LC tank features. This unique simulation study is done in the T-Spice 0.18µm CMOS process using an input voltage of 1.8 V, using high Vt and low oxide thickness Tox for reducing threshold voltage drop in latter stages.

Keywords: Inductor-capacitive Dickson charge pump, conventional Dickson charge pump, Power efficiency, R_{on} MOS resistance, Non-Over lapping Clock generator, Nonvolatile memories, integrated LC tank model

1. Introduction

The world of electronics is becoming dominated by mobile applications such as laptop computers and cellular phones. In such applications, reducing power consumption has increasingly become an important requirement for integrated circuits [1]. But with parallel circuit operation, higher throughput request builds pressure on clock rate and active current consumption. Charge pumps are a way of switching connection to control the connection of voltages to the capacitor [2]. At present, low power supply computer, SRAM, Input/output systems and several additional applications are widely used. Depending on these technologies, embedded systems often include high density flash drives on the same chip. Regardless of power fashions, Non-Volatile Memories, as well as Electrical Erasable PROMs, require maximum voltages ~ 4V-7V to enable hot electron injection and tunneling during writing and erasing actions. [3]. Capacitive load pumps based on the Dickson design structure [1] are widely used to increase the input on-chip voltage. The key constraints of such a methodology are: 1) the boosting phase 1 and 2 in each stage required in low voltage processing technologies that lead to the deterioration of energy efficiency and 2) the large area on chip needed by them [4,5].

This paper modified Dickson charge pump using LC tank based integrated architecture charge pump. After conducting the literature survey, we found that some architectural products have been produced for improving power efficiency. In previous papers on this topic, we have observed that circuit complexity increases to improve power efficiency. Efficiency has been shown to improve substantially, but it requires balancing a lot of parameters, that is a complex task - such as output power, delay, rise time etc. On the contrary, when the efficiency increases to an extent then the output voltage decreases due to the complex architecture. It is essential to have a better charge pump, regulating the balance current to the final output stage with the load [6].

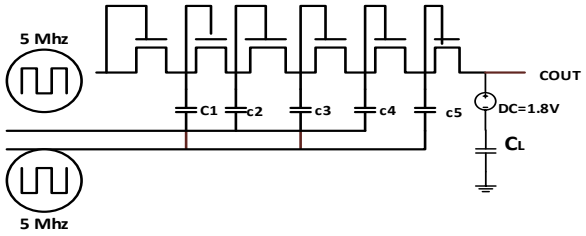

Fig. 1. The Dickson Charge Pump

In this paper, Inductor has been used to impress efficiency because the inductor produces a large current that is needed for the charge pump to work well. The related inclusive boost-up circuit behavior and efficiency analysis are presented in Section 2. In Section 3, the flow of model of integrated LC tank used in circuit simulations is introduced. In section 4, two phase Non-overlapping Clocking scheme Timing behavior circuit block it is important circuit block for charge pump circuit operation. Finally, in Section 5, measurement results at various load resistances are provided, and conclusions are discussed in Section 6.

2. Dickson Charge Pump Circuit Behavior and outcome Problems with Efficiency Analysis

The traditional charge pump invented by J.F. Dickson [7] is based on diode-connected NMOS transistor structure where

*E-mail address: gyanprabhakar@gmail.com
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the capacitive energy storage step circuit provided roughly a final voltage: V_{out}= (N+1) × (V_{dd}-V_t), where N is number of stages, V_{dd} is the input supply voltage, and V_t is the threshold voltage of the MOS transistor. It is to be noted that, as the voltage is increased by boost pump, body effect increases due to threshold voltage MOS transistors and each stage drops voltage by $V_{dd} - V_T$, thereby the power efficiency is reduced at the final stage. While the threshold voltage cannot be scaled as much the scaling of the supply voltage, the effect of the increase of the threshold voltage on the lowering of the output voltage becomes significant in the scaled V_{dd}. There after several attempts have been made to re-design the structure for decreasing the threshold voltage [8,9]. Actually, efficiency parameter depends on the current at each stage, which regulates the output level in each stage and leads to full charge transfer. A boost converter charge pump DC/DC depends on switching, instead of pass-transistor. The power efficiency η at the output is a measure of performance [8].

$$\eta = \frac{I_L \times V_{out}}{I_{power} \times V_{dd}} \times 100 = \frac{V_{out}}{(n+1)\times(V_{dd}-V_t)} \quad (1)$$

Where I_L is the output current; $V_{out\ is}$ the output voltage; I_{power} is the current delivered through V_{dd} to charge pump. $V_{dd} - V_t$ is the voltage gain per stage with threshold voltage drop V_t [9]. The current I_{power} can be written as

$$I_{power} = (n+1)\times I_{Load} + I_p \quad (2)$$

Where I_p current in parasitic capacitors, required to charge and discharge the capacitors.

$$I_p = n \times C_p \times f \times V_{dd} \quad (3)$$

n is the number of stage and C_p is the parasitic capacitance. C_p is relative to the boost capacitance itself by a factor α [10].

$$I_p = n \times \alpha \times C \times V_{dd} \times f \quad (4)$$

Thus, charge pump power efficiency can be written as

$$\eta = \frac{\frac{V_{out}}{V_{dd}}}{(N+1)\alpha \times \left(\frac{N^2}{N+1} - \frac{V_{out}}{V_{dd}}\right)} \times 100 \quad (5)$$

The α is a technology-dependent parameter and ranges from 0.1(for poly-poly capacitors) up to 0.3 like metal-metal capacitors) [11, 12].

2.1 Behavior of Inductor Model and MOS R_{on} Resistance

The main parameter in the design of charge pump is the current that should be delivered at regulation level. In this proposed charge pump the inductor behaves as a current source at t=∞ when the current starts flowing in the circuit, and the capacitor behaves as a voltage source when current is flowing in the circuit at $t=0^+$ as Fig 2 and Fig 3.

3. Inductor based modified Dickson, charge pump model

The NMOS transistor used in the charge pump behaves like a control switch, as the voltage from the inductor is higher than input voltage and the output current is much lower than the input. When the switch is ON and OFF very fast, the inductor magnetic field never collapses. Therefore, when the switch 2 is opened again, this causes a higher voltage on the inductor as it adds to the magnetic flux. In this circuit the inductor has a critical role, when the current is increasing, then it prevents it from decreasing and when the current is decreasing, it prevents it from increasing.

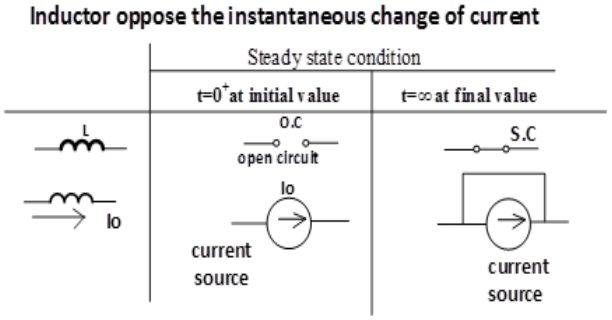

Fig 2. Inductor Behavior at $t=0^+$ and t= ∞

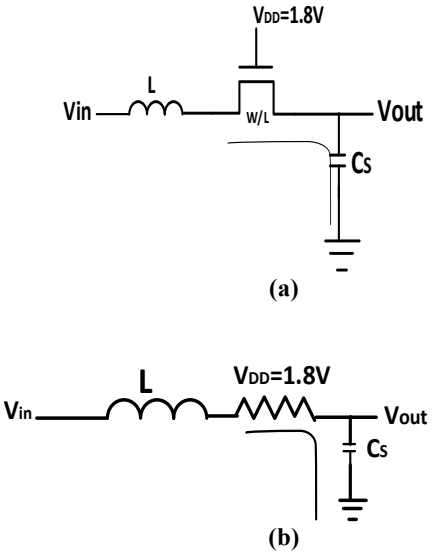

Fig 3. a) Inductor based Switch and b) inductive-resistive model.

$$R_n = \frac{V_{DD}}{\frac{K_P}{2}*\frac{W}{L}(V_{DD}-V_{THN})^2} \quad (6)$$

$$Req = \frac{L}{\mu Cox*(V_{DD}-V_{THN})^2*W} \quad (7)$$

There have been other attempts to design better charge pumps through structural modifications [13, 14]. The schematic of the basic operation of the first stage of the inductor-based Dickson charge pump is shown in figure (3). It is limited by the threshold voltages drop in the Dickson charge pump [15]. Alternatively, dc/dc converters based on inductive mechanism is widely used in power electronics, and in recent times, they have been integrated into CMOS standard processes [16]. The inductor techniques using diode generic circuit is shown in figure (4) by (Massimiliano Zucchelli and Luigi Colalongo, 2016).

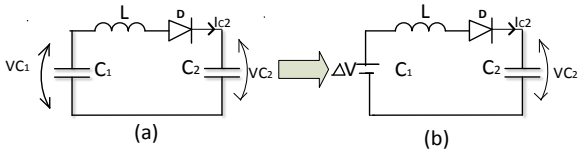

Fig. 4. Schematic of the basic operation of the first stage of the inductive-based Dickson charge pump.

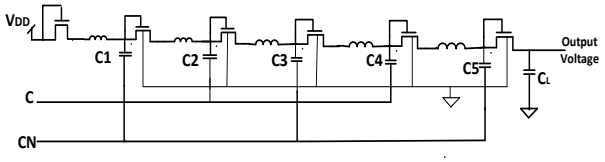

Fig. 5. Proposed Model of Inductor based Dickson Charge Pump.

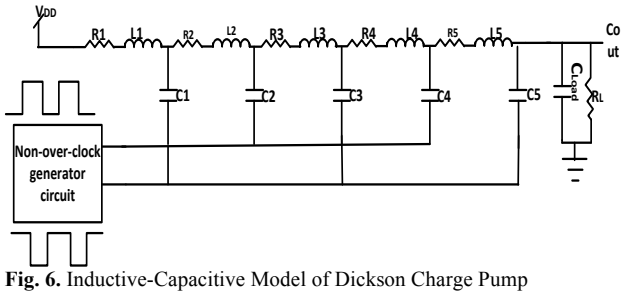

Fig. 6. Inductive-Capacitive Model of Dickson Charge Pump

The major limits of a completely integrated LC tank converter approach are the efficiency at low input voltage. The LC tank converters produce sufficient current to deliver to a clock signal which maintains the current level at each node [17]. The circuit diagram of the proposed inductor-based boost converter is shown in figure (5). The Charge Pump circuit receives a clock signal from the non-overlapping clock circuit. The value of L and C sets the desired frequency; the current can be adjusted through the value of inductor current. In this fashion, all parameters can be controlled to enhance the efficiency and reduce the ripple voltage [18].

$$f = \frac{1}{\sqrt{LC}} \tag{8}$$

The 5- Stage Modified inductor charge pump is a combination of the capacitors C_1-C_5 and inductor L_1-L_2 and C_{out} is output capacitors as shown in Fig (5). The modified LC tank converter can be well matched with low power in inductive-capacitive structural design and can be fabricated in standard low-voltage CMOS process [19].

As shown in Figure 3, a model LC tank DC converter is formed by a switch, an inductor, and a diode-attached MOS. The charge pumps up to boost approximately five times that can generate output voltage 8.5V from input 1.8V [20]. The energy of inductor used in charge pump is Inductor energy

$$E = \frac{1}{2}Li^2 \tag{9}$$

4. Non-overlapping Clocking scheme Timing behavior

Non-overlapping clocking scheme timing behavior is key circuit block for any charge pump circuit. The Charge Pump is never work without clock operation so it is required two phase non-over lapping clock circuit operation design through seven stage CMOS based ring oscillator circuit. The Ring Oscillator is not able to generate non-over lapping clock, therefore associated with using non-overlapping circuit using cross coupled CMOS based NAND gates. The overlapping clocking schemes consumes too much power which increases the dynamic power losses during switching operation. Non-overlapping circuit is reducing dynamic power operation during circuit switching operation. The ring oscillator with non-overlapping circuit output waveform shown in Fig (7). The Non-over clock circuit behavior shown in Fig (8).

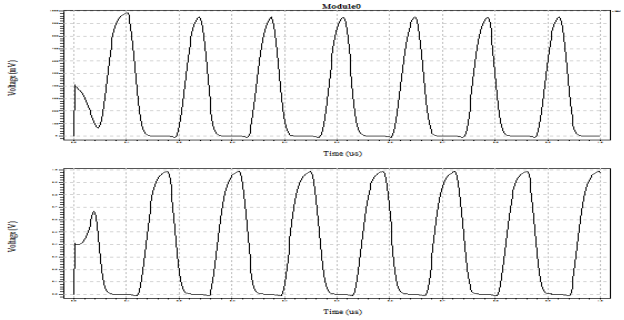

Fig. 7. Clock output voltage through Ring oscillator.

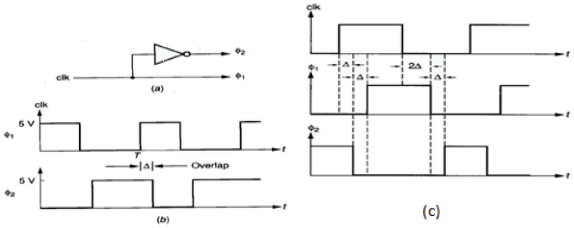

Fig. 8. (a) Generate two-phase clock using inverter, (b) Showing clock overlapping behavior (c) Ideal clock behavior of Non-over lapping circuit

Clocked DFF (Timing Circuit).

The timing circuit block in master slave fashion shown in Fig (9). It is providing smooth square wave and reduce the power loss during energy storage phase.

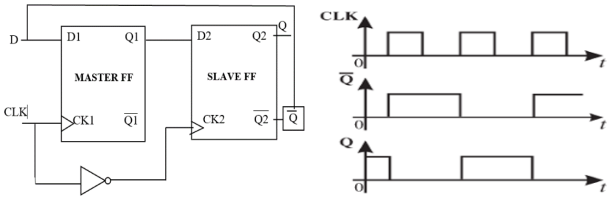

Fig. 9. Block of Master-Slave DFF

In Figure (9) is shown a clocked CMOS based DFF in master-slave fashion based on this circuit. It has a better pulse converter that is designed to reduce the power loss during the energy storage phase. When the NMOS control switch is ON the current flows from the input voltage source through the inductor, and the energy is stored in the inductor. The DFF produces a timing circuit for the proposed inductor-based Dickson charge pump. The main clock generator in the first phase is CMOS based ring oscillator through an odd number of stages. The seven-stage (n=7) ring inverter has been selected as a substitution. The 50% to 75% of the duty cycle is produced in the second stage [21]. Thus, a digital D-flip-flop (a master-slave type) and a NAND gate provide two output signals (Q and $\overline{Q}$) with 1/2 frequency. The NAND gate varies between CLK and $\overline{Q}$, with 75% duty cycle signals [22-24].

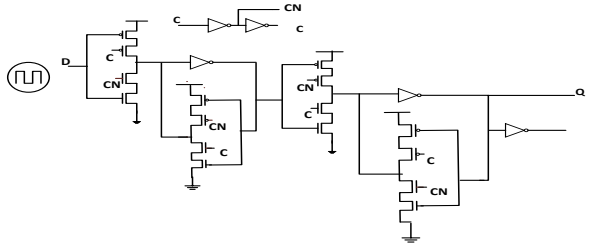

Fig. 9. Clocked CMOS based D-Flip Flop Master-Slave Fashion

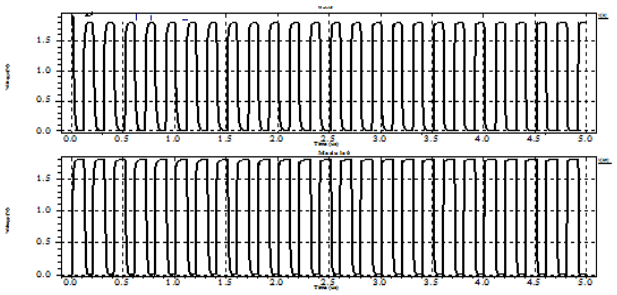

Fig. 10. Clock out voltage through clocked CMOS based D-Flip Flop Master-Slave DFF

5. Simulation Result Inductor and without inductor

The proposed inductor charge pump is simulated by using the T-Spice software in 0.18 µm CMOS technology. The voltage gain output per stage of the five-stage charge pump using an inductor and without inductor based on conventional charge pump circuit is shown in figure 5. It is observed that as the MOS resistance value is varied between 20Ω and 100Ω, it has an impact on the output voltage at L=100 µH and Supply voltage 1.8 V. The efficiency is largely improvised at different values of pumping MOS capacitors 6 pF - 20 pF with various load output resistance. In this paper Table 1 shows the Technology and Tools specification of parameters that have been used, Table 2 shows the values of parameters that are used during simulation.

Table 1. Tools & Technology Specification -Transient Analysis-Design Summary

Schematic	**Tanner schematic composer**
Simulation	Transient Analysis
Technology used	180 nm NMOS Level 49 Technology (MOSIS)
V_t	High V_t 0.49
Minimum Channel Length L_{min}	180 nm CMOS
T_{ox}	4.6 nm (NMOS) & (PMOS)
$K_n\mu*C_{ox}$	292 µA / V²
$K_p\mu*C_{ox}$	1455 µA / V²
Power Supply V_{DD}	1.8 V
C_{ox}	8.46 fF/ (µm) ²

Table 2. Charge pump specifications

Specification	**Name**	**Value**
Steady output Voltage (V)	V_{OUT}	6.5 V
Pumping Capacitor (pF)	C_1 to C_5	6 pF, 20 pF
Output Load capacitance in (pF)	C_L	1pF. 10 pF
Output Load Resistance in (kΩ)	R_L/R_{out}	250,500,750,1000
Output voltage ramp time (µs)	T_{RAMP}	10 µs
Pump power supply voltage (V)	V_{DD}	1.8V
Average pump current consumption (µA)	I_{PUMP}	6 µA
Rise/fall time (ns)	t_{rise} and t_{fall}	2.60ns/1.23ns

In Figure 11, output voltage V_{out} variation with MOS R_{on} resistance is shown. In this graph, we observe that by increasing the value of inductor to five times, the value of the output increases to 1 volt. Thus, there is an effect of inductor value on the output voltage. In this graph, R_{on} is the drain to source resistance that is actually decided by W and L of the MOS transistor, and both are technology dependent parameters. The MOS R_{on} resistance value is derived from W/L ratio.

The low value of MOS resistance can transfer the maximum charge and receive maximum voltage thereby reducing power consumption. As a result, the efficiency increases. Because of the low value of R_{on} resistance, the maximum current is delivered to the final stage, which improves the voltage gain and efficiency.

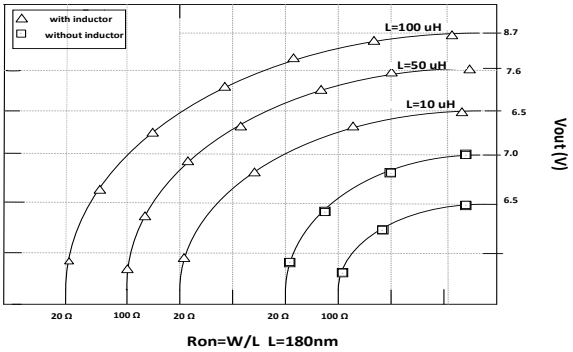

Fig. 11. T- Spice simulation comparison results of output voltage variation vs. efficiency vs MOS Ron resistance for conventional charge pump without inductor and proposed using inductor Dickson charge pump

Case-1 Inductor (L) and MOS resistance (Ron) play an important role in this simulation result. When R_{on} =20 Ω and L=10 µH then output voltage reaches 6.5 V. While when R_{on} =20 Ω and L=100 µH then output voltage reaches to maximum 8.7 V. When L=50 µH and R_{on}= 100 Ω, Vout=7.6 V. The inductor and the MOS resistance are the key parameters of inductor based Dickson charge pump design. It proves to be helpful in increasing the voltage gain and power efficiency.

Case-2 Without inductor when R_{on}= 20 Ω, output reaches 7.0 V. Then on further increasing the value of MOS resistance, the output voltage decreases significantly.

Table 3. Output Voltage measured with and without Inductor

	Inductor (L) in µH	**MOS Resistance (Ron) in Ω**	**Output Voltage (Vout) in V**
With Inductor	10	20	6.5
	50	100	7.6
	100	20	8.7
Without Inductor	--	20	7.0
	--	100	6.5

Using inductor value L=100µH - figures 12 and 13 show simulation result of efficiency analysis of 5 stage and 3 stage Dickson charge pump circuit under the various output load resistance (R_L) 250 kΩ - 1000 kΩ, pumping capacitors 6 pF and Figure 13 at 20 pF. The efficiency achieved is up to 96 % on load resistance value of 250 kΩ, but efficiency is decreased up to 55% on load resistance value 1000 kΩ using 5 stage charge pump. When using 3 stage charge pump at the same load value, the efficiency is observed going up to 60 % and maintains above 50% at 1000 kΩ load resistance. Similar explanation follows for the figure 13.

The figures 14 and 15 show simulation result of the relation between output voltage and efficiency with capacitors value 6 pF at N= 5 stage, and N=3 stage charge pump circuit under the various output load resistance (R_L) 250 kΩ - 1000 kΩ. It is observed that the efficiency increases as the output voltage is decreases and power increases. It means that when we want to achieve more efficiency for better charge pump work, then output voltage has to be compromised of 5 stages charge pump to produce the best efficiency in the range 96% to 55%. For N=3 stage charge pump efficiency ranges between 60% to 50%.

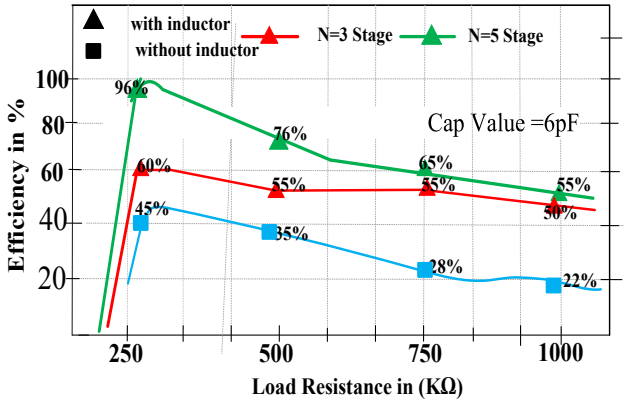

Fig. 12 Efficiency vs Load resistance at 6 pF

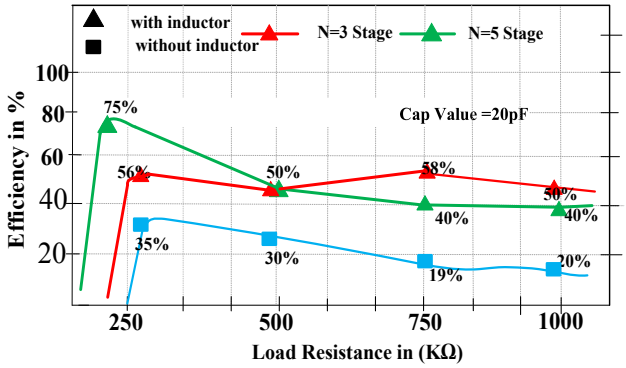

Fig. 13 Efficiency vs Load resistance at 20 pF

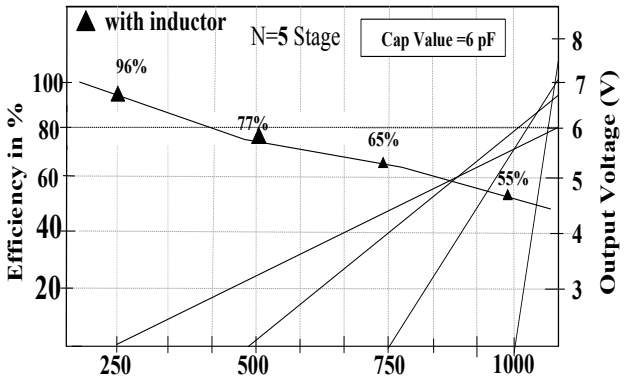

Fig. 14 Relation between Efficiency and output voltage at output load resistance at 6 pf, N=5 Stage.

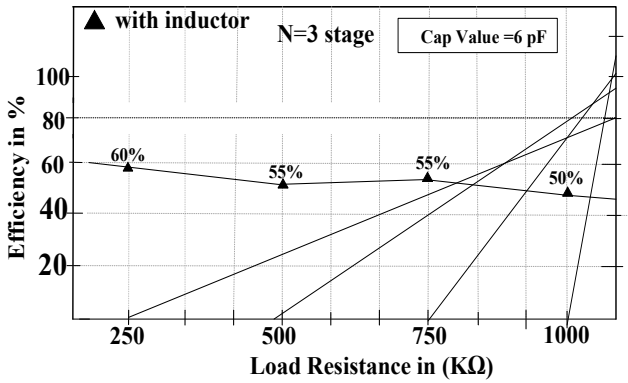

Fig. 15 Relation between Efficiency and output voltage at output load resistance at 6 pf, N=3 Stage

The figures 16 and 17 show simulation results for 20 pf capacitor value and follows similar description as for figures 14 and 15, for the relation between output voltage and efficiency.

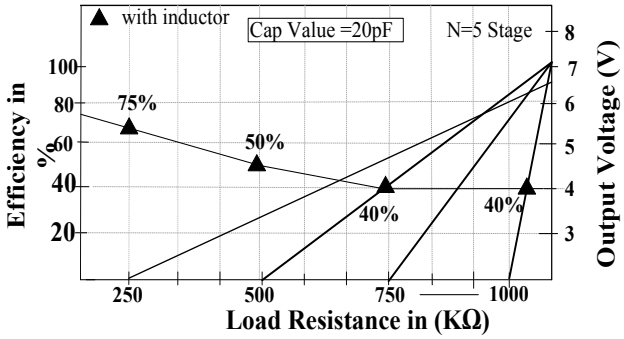

Fig. 16 Relation between Efficiency and output voltage at output load resistance at 20 pf.

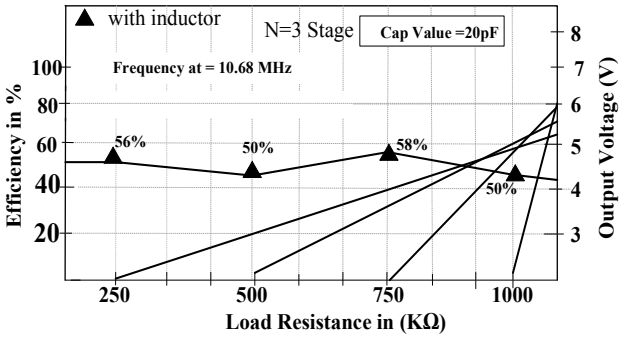

Fig. 17 Relation between Efficiency and output voltage, N=5 Stage at output load resistance at 20 pf, N=3 Stage.

The figures 18 and 19 show simulation result of output power with capacitor value 6 pF and 20 pF of 5 stage and 3 stage charge pump circuit under the different output load resistance (R_L) 250 kΩ to 1000 kΩ. It is observed that the output power decreases with increasing load resistance.

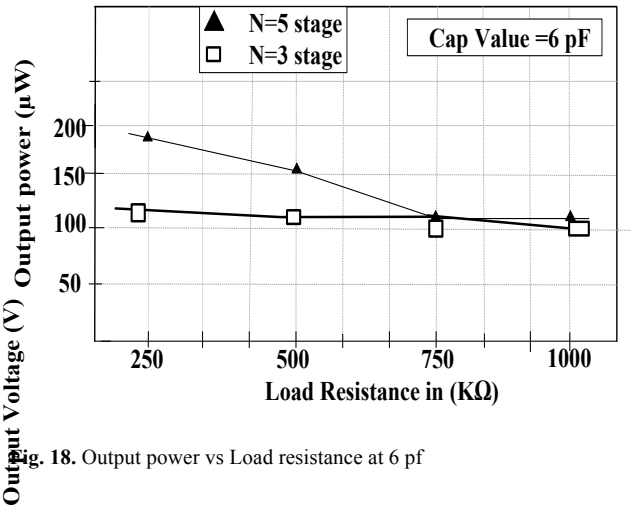

Fig. 18. Output power vs Load resistance at 6 pf

The figures 20 and 21 show simulation result of the output current with capacitor values 6 pF, and 20 pF for 5 stage and 3 stage charge pump circuit under the different output load resistance (R_L) 250 kΩ to1000 kΩ. The output current is observed to decrease with higher resistance values.

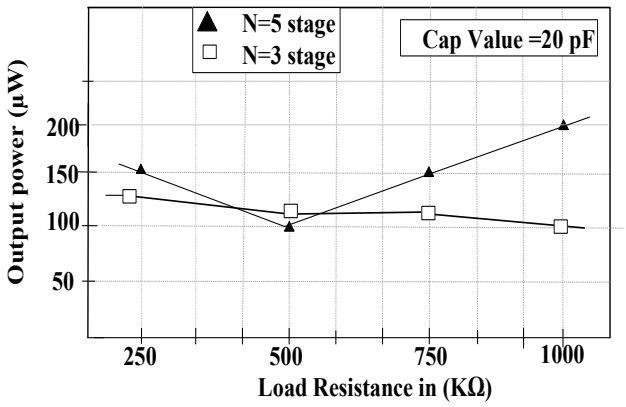

Fig. 19. Output power vs Load resistance at 20 pf

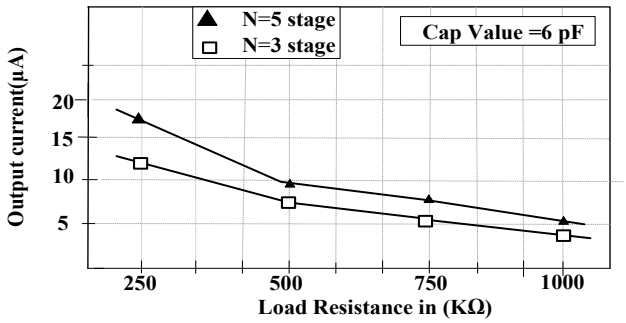

Fig. 20. Output current vs Load resistance at 6 pf

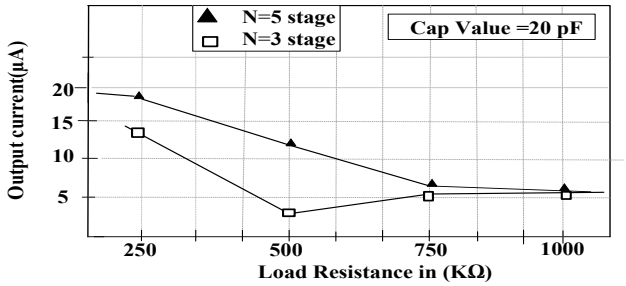

Fig. 21. Output current vs Load resistance at 20 pf

Figure 22 shows simulation result of Output voltage vs N=3 and N=5 stage of charge pump circuit at 6 pf. It clear shows an increase in output voltage value with increasing number of stages.

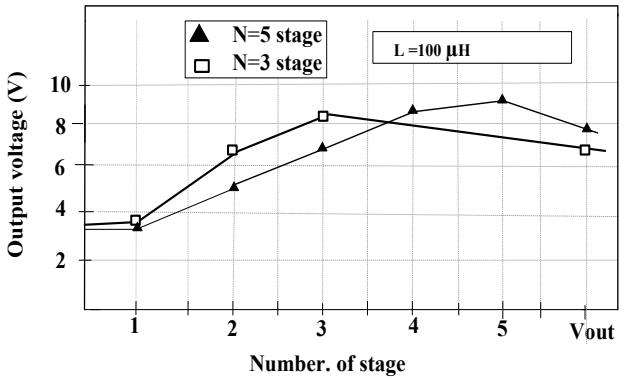

Fig. 22. Output voltage vs No. of stage at 6 pf

Table 4. Simulation Result Analysis - Performance Summary at 6 pF.

Result at, L= 100µH at frequency 32.49 MHz						Result at, L= 100µH at frequency 19.49 MHz			
C1 to C5=6 pF N=5						C1 to C3=6 pF N=3			
Load output resistance R_L(KΩ)	250	500	750	1000		250	500	750	1000
output voltage (V)	6	6.8	7.1	7.5		5.0	5.5	5.9	6.0
Efficiency Ƞ (%)	96	77	65	55		60	55	55	50
output power (µw)	193	154	110	110		118	110	110	100
output current (µA)	18	10	7.0	5.5		13	7.1	6	4.5

Table 5. Simulation Result Analysis- Performance Summary at 20 pF.

Result at, L= 100µH at frequency 17.75 MHz						Result at, L= 100µH at frequency 10.68 MHz			
Pumping Capacitor C_1 to C_5=20 pF N=5						Pumping Capacitor C_1 to C_3=20 pF, N=3			
Load output resistance R_L(KΩ)	250	500	750	1000		250	500	750	1000
output voltage (V)	6.5	7.0	7.1	7.1		5.2	5.5	5.8	5.9
Efficiency Ƞ (%)	75	50	40	40		56	50	58	50
output power (µw)	150	100	150	200		125	110	111	105
output current (µA)	18	12	7	5.5		14	3.5	5.3	5.3

Table 6. Simulation Result Analysis-Stage output voltage Summary as 3 and 5 stages.

Charge pump in each (N=5) stage	**1rst**	**2nd**	**3rd**	**4th**	**5th**
Pumping voltage (using inductor)	3.5	5.3	6.3	8.2	9.1
Pumping voltage (without inductor)	3.0	4.1	5.1	6.1	7.5
Charge pump in each (N=3) stage	1st	2nd	3rd	Vout	
Pumping voltage (using inductor)	3.6	6.3	8.1	7.26	

Table 7. Result Comparison with various inductor-based charge pump.

Parameters	**2016 (12)**	**2009 (6)**	**2017 (13)**	**2004 (5)**	**This Work**	
Process (µm)	0.18	0.18	0.18	0.18	0.18	0.18
Min Vin(V)	1.8	0.2	0.11	1.8	1.8	1.8
Vout (Load Resistance)	3.4	1.2	1.5	6.0	7.3	6.8
No. of stage	3	2	3	5	3	5
Max. Efficiency	47%	40.26%	46.5%	65%	60%	77%

6. Conclusions

Inductor based modified Dickson charge pump has been modeled and simulated using 0.18µm CMOS process. We applied five stage inductor-capacitors architecture to boost-up efficiency and conversion ratio up to 96% at load output resistance 250 kΩ. The efficiency was tested at various load resistance up to 1000 kΩ and pumping capacitors 6 pF and 20 pF and using L=100µH. The efficiency range was observed to vary from 65% to 96%. The output voltage up to 6.5 V to 8.5 V was achieved. Simulation results have been performed using 3 stage and 5 stage charge pumps. It was observed that for N=3 stage charge pump, the efficiency

varies 50% to 60%. In contrast, N=5 stage charge pump efficiency varies from 55% to 96% with respect to the load resistance. The Main theme of this paper, MOS resistance R_{on} (Drain to source resistance) is designed at 20 Ω and 100 Ω, because of which pumping current is the regulate at each stage up to regulation level and get the higher output voltage and higher efficiency. By using the the T-Spice software in 180 nm CMOS technology, the simulation results of the charge pump circuit for 1.8 V input voltage show that the output voltage and the conversion ratio of the proposed charge pump are 7.5 V and 77.3%, respectively. In comparison with the other charge pump circuits, the designed charge pump circuit has a higher voltage conversion ratio.

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