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A New Kind of Sub-pixel Interpolation Filtering Algorithm and Hardware Structural Design

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Abstract: Considering the problems of high complexity of sub-pixel interpolation operation and large visitor volume of storage in H.264/AVC standard, a kind of sub-pixel interpolation operation is put forward with changeable filter coefficient and unchangeable coefficient sum. According to the video image, filter coefficient can be confirmed. Based on the algorithm, a kind of 1/4 pixel precision interpolative hardware structural design. It is indicated by the performance analysis and filter structure that the structure is able to calculate pixel interpolation at different positions in a certain clock period with the characteristics of small area and fast speed. It is indicated by the result of experiment that compared with H.264 standard, new algorithm is able to reduce 18 % space complexity, improve noise ratio of peak, reduce bit rate and improve the performance of coding.

Keywords: H.264, Sub-pixel, Filter, Hardware structure.

1. Introduction

H.264 to improve the precision of motion compensation. It is indicated by the experiment [1, 3] that high-precision motion is able to improve compression efficiency of video coding. With the improved performance of motion prediction, some problems such as large calculating amount and frequent memory operation also emerge. Order of filter determines the reading amount of the reference data. On the premise that the accuracy of predication is guaranteed, reducing the space complexity and visitor volume of storage of interpolation is the present issue of study.

2. Principle of Sub-pixel Interpolation in H.264/AVC [2]

2.1. 1/2 Pixel Interpolation Operation

H.264/AVC defines the 6-order filter with the coefficient of (1, -5, 20, 20, -5, 1). 6×6 pixel piece is shown in Fig. 1. 'M' to 'U' is the integer pixel.

Sample point value of 1/2 pixel ss, aa, b, s, dd, vv; tt, bb, h, m, cc and uu is obtained by the horizontal and vertical 6-order filtering interpolation calculation of the sample point closed to the integer pixel. Calculation process of b and h is shown as following:

b=round((P-5C+20D+20E-5F+Q)/32)

h= round((M-5A+20D+20H-5K+T)/32)

Sample point value of 1/2 pixel j is obtained by the horizontal and vertical (the results are equal) 6-rank filtering interpolation calculation of the adjacent 1/2 pixel. Calculation process of j is shown as following:

j=round((tt-5bb+20h+20m-5cc+uu)/32)

or

j=round((ss-5aa+20b+20s-5dd+vv)/32)

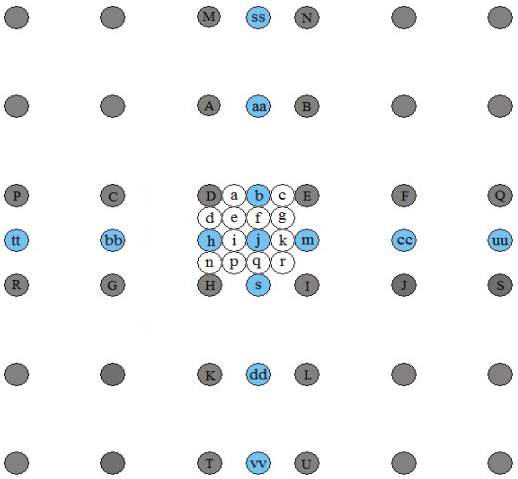


Fig. 1. The location of the Integer pixel and fractional pixel.

2.2. 1/4 Pixel Interpolation Operation

When 1/2 pixel is obtained, the sample point value of 1/4 pixel is obtained by bilinear filter interpolation.

Value of a, c; d, n; e, g, p and r at 1/4 pixel position can be obtained by the horizontal, vertical and diagonal bilinear interpolation calculation of two nearest integer pixel and 1/2 pixel. Calculating process of a, d and e is shown as following:

a= (D+b+1)/2

d= (D+h+1)/2

e= (D+j+1)/2

The value of f, i, k and q at the 1/4 pixel position is obtained by the horizontal and vertical calculation of the average value of two nearest 1/2 pixel. The calculating process of f and i are shown as following:

f= (b+j+1)/2

i= (h+j+1)/2

3. Improvement of Sub-pixel Interpolation Operation Principle

3.1. 1/2 Pixel Interpolation Operation

For the improvement of 1/2 pixel interpolation operation, two integer filters F1 and F2 with 4-order coefficients (a0, a1, a2, a3)/2n and (b0, b1, b2, b3)/2m are adopted in this paper. Filter meets the following conditions:

1) a0, a1, a2, a3 and b0, b1, b2, b3. All of the filters are integer;

2) a0+a1+a2+a3=2n, b0+b1+b2+b3=2m, m=n≥4;

3) a0=b3, a1=b2, a2=b1, a3=b0.

In Fig. 1, 1/2 pixel at aa, b, s, dd; bb, h, m, cc position is obtained by the interpolation calculation of nearest horizontal and vertical integer pixel applying filter F1 and F2. Calculation process of b and h is shown as following:

b=(a0×C+a1×D+a2×E+a3×F+2n-1)/2n

h=(b0×A+b1×D+b2×H+b3×K+2m-1)/ 2m

Sample point value of 1/2 pixel j is obtained by the horizontal interpolation calculation of adjacent 1/2 pixel applying 4-order filter F1. The calculating process of j is shown as following:

j=(a0×bb+a1×h+a2×m+a3×cc+ 2n-1)/2n

3.2. 1/4 Pixel Interpolation Operation

For 1/4 pixel interpolation operation, bilinear filter is adopted to conduct interpolation. Detailed arithmetic can be consulted above.

4. Realization of Hardware Structure

Sub-pixel interpolation filtering requires expansion of reference macro block. Order of filter decides the reading amount of reference data. When the size of macro block is M×N, the reading amount of the reference data is (M+3)×(N+3). For example, to conduct interpolation for a 8×8 reference block, 4-order filter is adopted. An integer pixel point is expanded on the left and above the 8×8 block and two integer pixel points are expanded on the right and below the block. It means that 11×11 reference data is read. It is shown in Fig. 2 that the value of 1/2 pixel with improved arithmetic can be obtained by the interpolation of horizontal 4-order filter and vertical 4-order filter. Interpolation process of 1/4 pixel is obtained by the selectable bilinear interpolation filtering of motion vector (X_Frac, Y_Frac) provided by entropy decoding unit. Block diagram of overall hardware structure is shown in Fig. 3.

3 operators are used to conduct 1/2 pixel interpolation filtering. The first and third operator, the second operator is the finite impulse response (FIR) filtering with 4 taps with the weight coefficients (a0 a1 a2 a3) and (b0 b1 b2 b3) respectively. 1/2 pixel interpolation filtering structure is shown in Fig. 4. The operation process of 1/2 pixel interpolation by the first operator is shown in Fig. 5. And operation process of 1/2 pixel interpolation by the second operator is shown in Fig. 6.

When the data storage unit is (M+3)×(N+3), input cache unit includes (M+3) line registers, which is input according to the data storage unit of pixel storage. (N+3) pixel constitute the data line. And data items of different lines are stored in the line register.

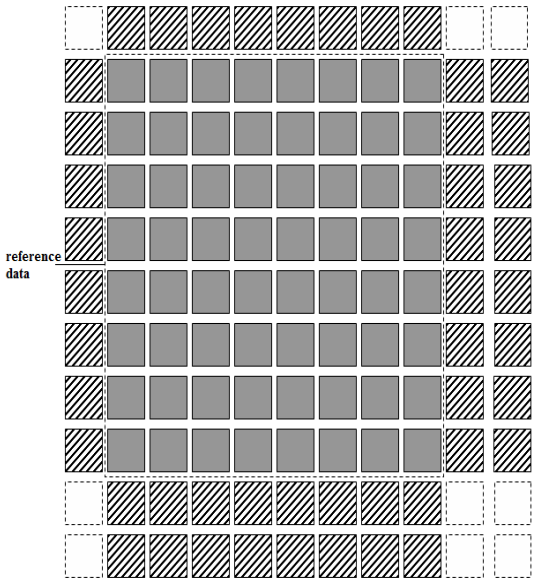


Fig. 2. Pixel to be Consulted at Sub-pixel Interpolation.

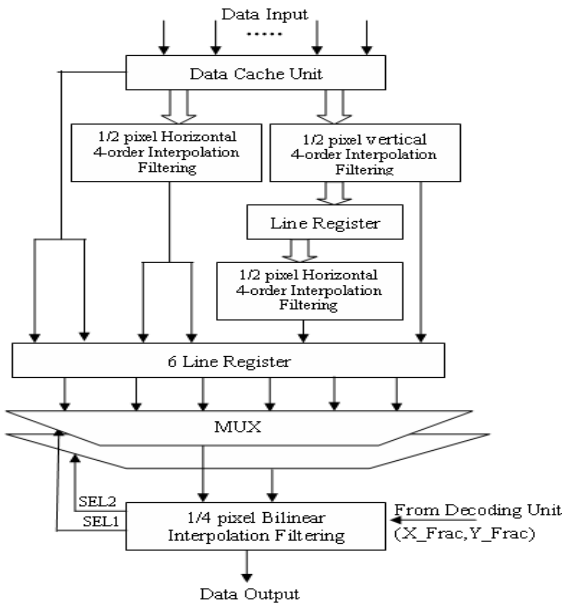


Fig. 3. Structure of Sub-pixel Interpolation Process.

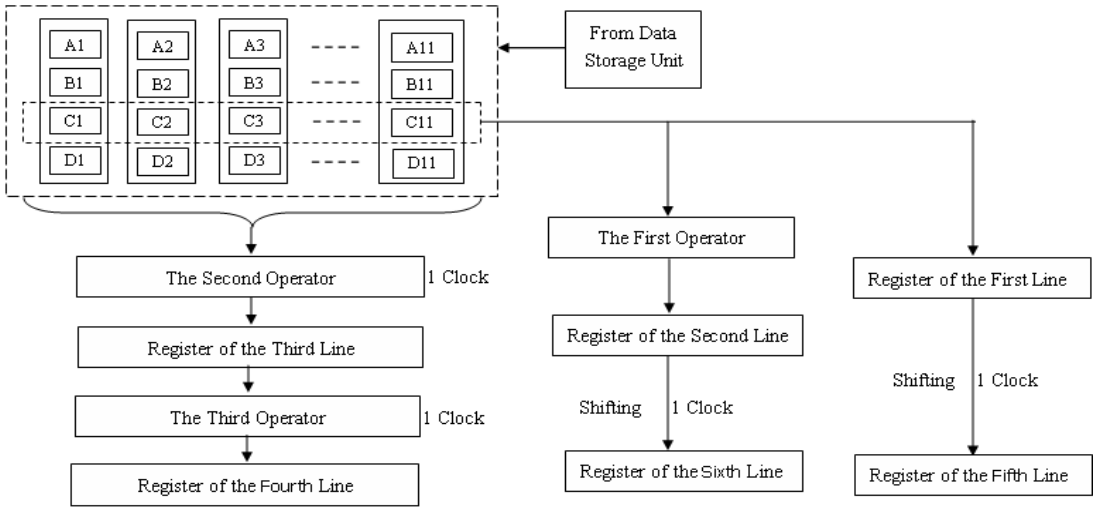
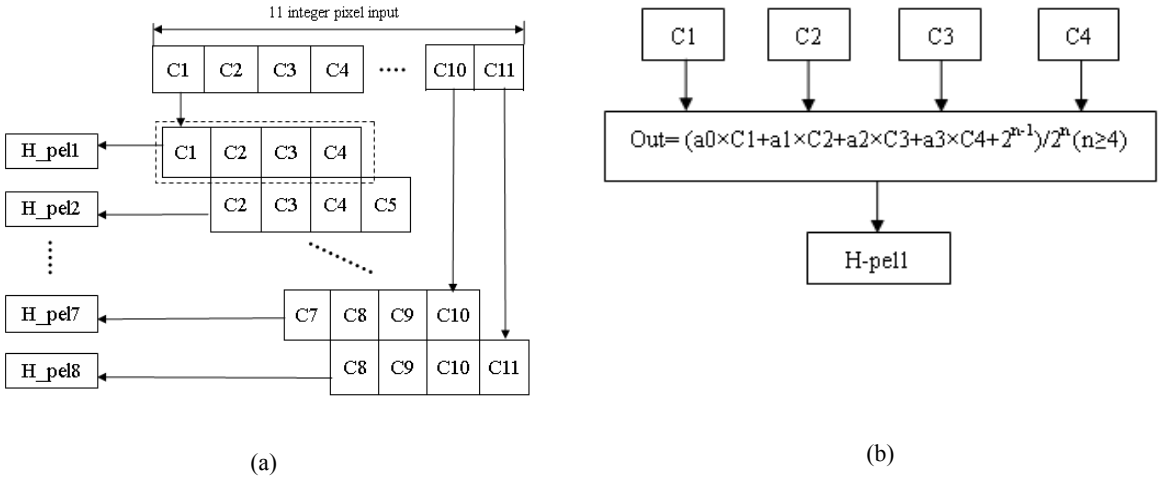


Fig. 4. Structure of 1/2 Pixel Interpolation Filtering.



(a) (b)

Fig. 5. Operation Process of 1/2 Pixel Interpolation by the First Operator.

It is seen from Fig. 4 and Fig. 5 that fourth line data items are input the input buffer (time by the first clock). And then 11 pixel values C1, C2...and C11 (correspond to 11 "D") in the third line of the input buffer are stored in one of line register of output buffer. Meanwhile, a shifted pixel arranging 4 integer pixel values (for example, C1, C2, C3 and C4) is used by the first operator to pixel and eight 1/2 pixel interpolation operations are conducted in the horizontal direction. And interpolation results H_pel1...H_pe18 are stored in second line register.

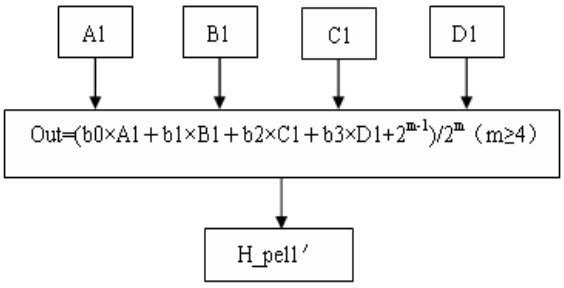


Fig. 6. Operation Process of 1/2 Pixel Interpolation by the Second Operator.

A1, B1, C1, D1, C1, C2, C3, C4 is the input data item.

It is known from the analysis Fig. 4 and Fig. 6 that when the first operator conducts 1/2 pixel interpolation filtering, the second operator conducts 11 vertical 1/2 pixel interpolations to pixel "h". The obtained interpolation result is stored in the third line register. In the second clock, interpolation is conducted by the third operator on pixel "j" according to the 11 operation results output by second operation. Eight pixel values obtained by interpolation are stored in the fourth line register of output buffer. During the timing of the second clock, 11 "D" data items and 8 "b" data items of the first and the second line register in the timing of the first clock are respectively transmitted to the fifth and sixth line register (corresponding to 11 "D" and 8 "b").

Therefore, except the initial 3 clock delays, the interpolation structure designed in this paper in every clock period is going to conduct a series of 1/2 pixel interpolation operation on a line of line data. The result obtained by interpolation is stored in the line register in the output buffer.

According to the motion vector provided by entropy decoding unit (X_Frac, Y_Frac), 1/4 pixel interpolation unit generates selection signal SEL1 and SEL2. 2 lines of line data output are chosen from 6 lines of line data (D, b, h, j, b', D') provided by output data buffer unit. Bilinear filtering is used to conduct 1/4 pixel interpolation. Interpolation operation is shown in Fig. 7.

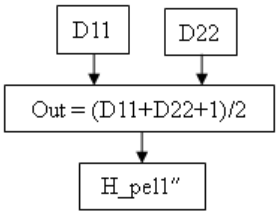


Fig. 7. Operation Process of 1/2 Pixel Interpolation D11, D22 is the input data item.

5. Analysis on the Algorithm Complexity

Interpolation comparison is conducted on the 4×4 block data from the perspective of space and algorithm complexity. Comparison of complexity between using improved algorithm and H.264 interpolation is listed in Table 1.

It can be seen from the table that 9×9 reference data is required in the 6-order filter in H.264 standard, while using 4-order filter put forward by this paper requires 7×7 reference data. 66/8 lines reference frame data are required in H.264 standard, while 54/8 lines reference frame data are required in the improved algorithm. Improved algorithm is able to reduce 18 % of space complexity. The computation complexity of the two is approximate.

Table 1. Comparison between Complexity of Improved Algorithm and H.264 Interpolation Method.

Interpolation Position	Reference Data Amount (Line×List)		Addition		Right Shift	
	H.264	Improved Algorithm	H.264	Improved Algorithm	H.264	Improved Algorithm
0,0(D)	4×4	4×4	0	0	0	0
2,0(b)	9×4	7×4	8	5	4	2
0,2(h)	4×9	4×7	8	5	4	2
2,2(j)	9×9	7×7	42	25	7	10
1,0(a)	4×9	4×7	58	56	29	23
0,1(d)	9×4	7×4	16	27	8	11
2,1(f)	9×9	7×7	18	27	9	11
1,2(i)	9×9	7×7	58	56	9	23
1,1(e)	9×9	7×7	14	16	3	7

6. Structural Comparison of 1/2 Pixel Interpolation Filter

Structural comparison 4-tap FIR and 6-tap FIR is shown in Fig. 8. It can be seen that structure of 4-tap FIR is easier to be realized by the 6-tap FIR. It is indicated by the experiment that [10] circuit area of the former and delay of key route are 36.2 % and 16.0 % less than those of the later.

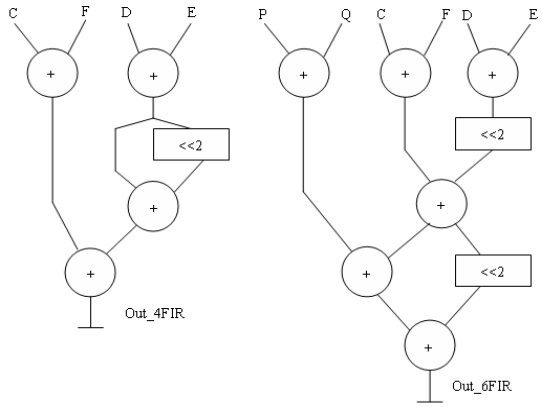


Fig. 8. Structural Comparison 4-tap FIR and 6-tap FIR.

7. Performance Analyses

Time of conducting macro block interpolation under the pipeline framework is analyzed in this paper. When the macro block is 4×4, the time of processing one macro block is 352 clock period. When the macro block is 8×8, time of processing one macro block is 152 clock period. When the macro block is 16×16, time of processing one macro block is 70 clock period. Therefore, interpolation operation of high-definition image can be accomplished in 676 clock period by the hardware structure designed in this paper.

Interpolation structure designed in this paper separates 1/2 pixel interpolation and 1/4 pixel interpolation to process 1/2 pixel interpolation and 1/4 pixel interpolation step by step. 1/4 pixel interpolation is chosen according to motion vector, and the data stored in the register is shifted downwards in the unit of line to conduct 1/2 pixel interpolation. Therefore, the calculation can be processed faster. Relevant different operations concerning interpolation can be conducted at the same time when the register is shifted, thus the operation time is reduced. The register is able to support small or big son macro block and pixel is shifted in one direction, thus the structure of interpolation circuit can be simplified. Under this circumstance, 1/2 pixel interpolation can be applied to all the big or small blocks.

8. Experimental Simulation Comparison

New algorithm is embedded in the H.264 standard and simulation comparison is conducted with the reference of software JM12.1. Four video sequences are adopted, namely Container, Foreman, News and Tenis. Each sequence consists of 30 CIF frames, which coded 100 frames respectively. Full research is adopted in the motion estimation, with the search radius of 16. Five reference frames are selected. Entropy coding is CABAC, of which structure is IBBPBBPBBP. Quantization parameters (QP) are 16, 24, 32 and 40. Comparison of image quality between improved algorithm and H.264 standard is shown in Table 2. By adjusting quantization parameters, test is conducted on the order coding Container, Foreman, News and Tenis (Frame frequency is 30 Hz). Comparison of code rate-signal to noise ration before and after the calculation is shown in Fig. 9. It can be seen from Table 2 and Fig. 9 that compared with the sub-pixel interpolation operation in H.264 standard, peak signal of noise ratio (PSNR) of new interpolation operation is obviously increased and at the same time, Bit-rate is obviously decreased.

9. Conclusions

Theoretical process of reference block being interpolation in the inter-frame test of H.264/AVC is introduced in this thesis. Considering the issues of high complexity of sub-pixel interpolation operation and large visitor volume of storage in H.264/AVC standard, a kind of sub-pixel interpolation operation with changeable filter coefficient and unchangeable is raised. 6-ordre filter is simplified to 4-order filter in H.264/AVC. It is indicted by the experimental result that, comparing the algorithm and H.264, the complexity of calculation is appropriate, and space complexity is decreased by 18 %, and coding performance is increased. Meanwhile, high degree of parallelism hardware structural design based on pipeline organization is proposed, which takes consideration of the balance of processing speed and area. This structure is able to reduce bandwidth and improve handling capacity, reaching the requirement of standard definition and high definition of processing.

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Table 2. The compare in image quality between the improved algorithm and algorithm in H.264 standards.

Sequence	Format	□PSNR(dB)				□Bit-rate			
		QP=16	QP=24	QP=32	QP=40	QP=16	QP=24	QP=32	QP=40
Container	CIF	0.37	0.42	0.42	0.27	-5.48 %	-6.64 %	-4.12 %	-3.21 %
Foreman	CIF	0.36	0.49	0.20	0.46	-8.29 %	-3.91 %	-2.71 %	-4.29 %
News	CIF	0.17	0.66	0.27	0.32	-8.19 %	-3.42 %	-3.54 %	-3.82 %
Tenis	CIF	0.35	0.79	0.54	0.27	-7.87 %	-3.82 %	-2.67 %	-5.26 %

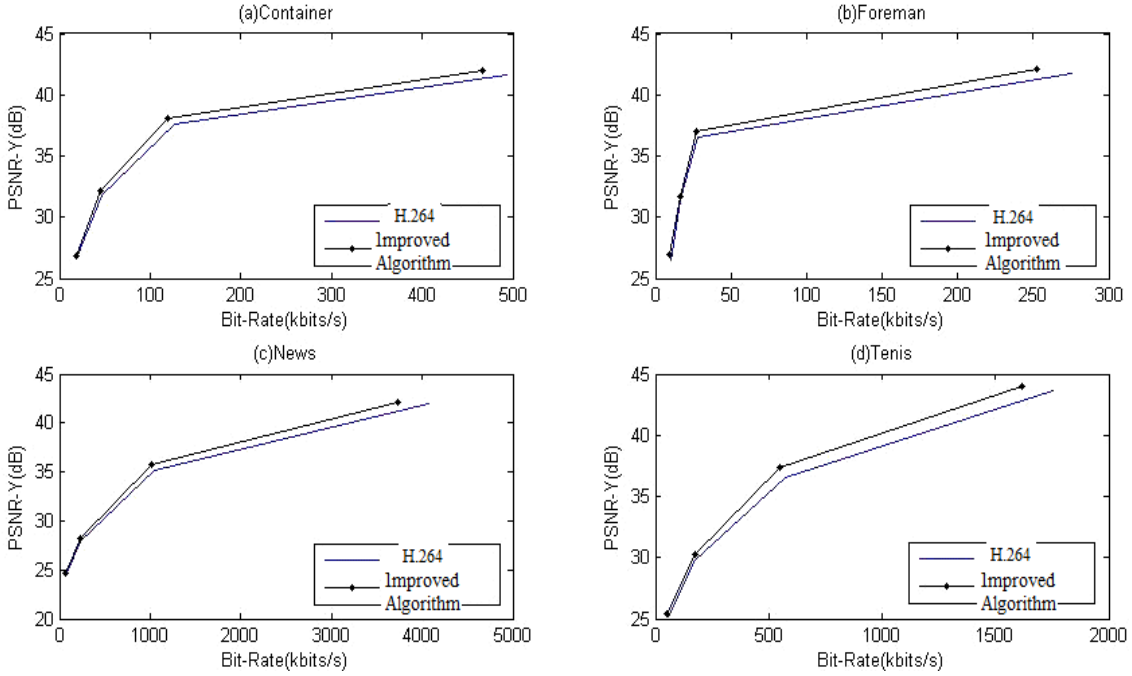

Fig. 9. The relation of the Bit-rate—PSNR-Y in before and after improved algorithm.

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