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A New Topology for Z-Source Inverter Based on Switched-Inductor and Boost Z-Source Inverter

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ABSTRACT
In this paper, a new topology for boost Z-source inverterbased on switched-inductor cell is proposed. The operating modes of the proposed inverter are analyzed and also a suitable control method to generate the trigger signals of the inverter is presented. Having a common earth between the input source and inverter and capability to generate a higher voltage gain by using lower amounts of the duty cycles are some advantages of the proposed Z-source inverter. Comparison of the proposed inverter with conventional Z-source inverters is presented from different points of the view. Finally, the accuracy performance of the proposed inverter is reconfirmed through the simulation results in EMTDC/PSCAD software program.

KEYWORDS: Z-source inverter, Shoot-through, Switched boost inverter, Switched-inductor cell.

1. INTRODUCTION

Nowadays, considering the renewable energy source, the power conversion from dc to ac is very important [1]. It is possible to increase or decrease the magnitude of output voltage of Z-source inverter by using shoot-through (ST) state [2]. As a result, the output voltage of the Z-source inverter can be lower or higher than the input voltage. In addition, the Z-source inverter presents a good resistance in the face to electromagnetic interference (EMI). This fact makes the Z-source inverter suitable in different applications such as power renewable systems, adjustable speed drivers systems, UPS [3-5]. However, the X-shape impedance network that is used in the Z-source inverter increases its size and total cost. Therefore, this inverter is not suitable in low power applications in which the size, weight and cost are the main parameters. In recent years, in order to solve the problems of the conventional Z-source inverters, various topologies of Z-source inverter have been presented [6-13]. Some of the studies on Z-source inverter are on the applications, modeling, control and modulation methods and the others are concentrating on presenting new topologies. One of these topologies is switched boost inverter [14]. This inverter consists of the advantages of the conventional Z-source inverter such as ST state, good resistance in face to electromagnetic interference in addition to use lower passive elements in its impedance network and common earth between the input and output of the inverter, but its voltage gain is lower than the conventional Z-source inverter. Its low voltage gain makes it unsuitable in low duty cycle applications. In [15], in order to decrease the nominal value of passive elements in the conventional Z-source inverters and to have continuity in the source current, the quasi Z-source inverter (QZSI) has been represented. One of the main problems of the QZSI is its voltage gain that is same conventional Z-source inverters. To improve the voltage gain, another topology called novel switched-inductor quasi-Z-source (SL-QZSI) has been reported in [16]. This topology has various disadvantages such as higher capacitors' voltage stress in comparison with the conventional ZSI and SBI.

In this paper, a new boost Z-source inverter based on switched-inductor cell is proposed. The main aim of this inverter is increasing the boost

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factor of the switched boost inverter. This inverter has also higher boost factor in comparison with the conventional Z-source inverters and is able to generate a higher voltage gain in lower amounts of duty cycles (D_{ST}). Therefore, the proposed Z-source inverter is suitable in low power and household applications. This inverter consists of the advantages of the switched boost inverter and conventional Z-source inverter. In addition, in order to increase the voltage gain, it is possible to develop the proposed Z-source inverter by using a higher number of switched-inductors.

At the following, first the proposed topology is presented. Then, its operation in different modes is investigated. After this, a modified control method is proposed to generate the required trigger signals for switches. Moreover, the proposed topology is developed by using a higher number of switched-inductors. To obvious the advantages and disadvantages of the proposed topology, this inverter is compared to some conventional Z-source inverters. Finally, the correct operation of the proposed topology is reconfirmed by using the simulation results in EMTDC/PSCAD software.

2. PROPOSED BOOST Z-SOURCE INVERTER

The proposed boost Z-source inverter is shown in Fig. 1. This inverter includes of an active switch (S), two diodes (D_a and D_b), one capacitor (C) and a switched-inductor cell ,which is connected between the input voltage source (V_i) and inverter. The switched-inductor cell consists of two inductors L_1, L_2 and three diodes of D_1, $D_2$and D_3. Different combinations of these elements to construct switched-inductor cell have been represented in [17-19]. In addition, a low pass LC filter at the end of the inverter is used to filter the high order harmonics of the output. The ST state in the H-bridge of the proposed boost Z-source inverter is also used same as the conventional Z-source inverters to increase the input voltage. It should be noted that the proposed topology can work on both three-phase and single-phase mode. Single-phase mode is shown in Fig. 1.

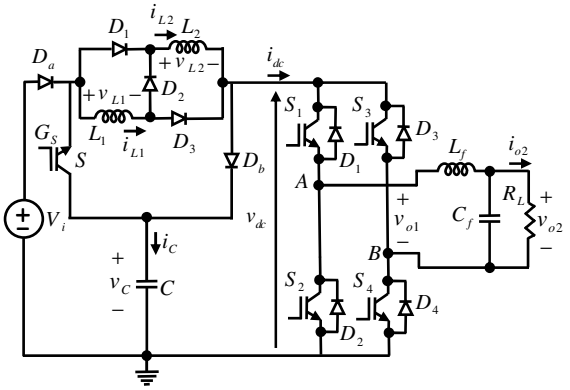


Fig. 1. The proposed boost Z-source inverter

2.1. Operating of the proposed inverter in continuous current mode (CCM)

The proposed inverter includes of two main operating modes; ST and non-ST states same as the conventional Z-source inverter that is shown in Fig. 2. In order to investigate the correct performance of the proposed topology in steady state, it is assumed that the ST state operates for time interval of $D_{ST}T_s$. In this time interval, the switch S and diodes $D_1$and $D_3$are turned on. D_{ST} is equal the ratio of time turned the switch S (T_{on}) to period switching (T_s) and with the name of converter duty ratio is known. For this time interval as shown in Fig. 2(a) the inductors of L_1 and L_2 are connected in parallel and the inverter acts as a short circuit. In addition, as V_C>V_i, the diodes of D_2, D_a and D_b are turned off and the capacitor of C is discharged to the inductors L_1 and L_2 by using switch S and inverter. Thus, the sum of the inductors current is equal to the discharge current of the capacitor. In the time interval of S, the proposed topology is in non-ST state. Therefore, the switch S and diodes D_1 and D_3 from switched-inductor current are turned off and the diode D_2 is turned on. This state is shown in Fig. 2(b). In this time interval, the inductors of L_1 and L_2 are connected in series and the inverter acts as a current source. In this condition, the inverter is supplied by the input voltage source (V_i) and inductors L_1 and L_2, while the capacitor C is supplied by the diodes of D_a and D_b. In addition, as the inductors are connected in series, their current are equal to each other and is the sum of the capacitor charge current and inverter input current.

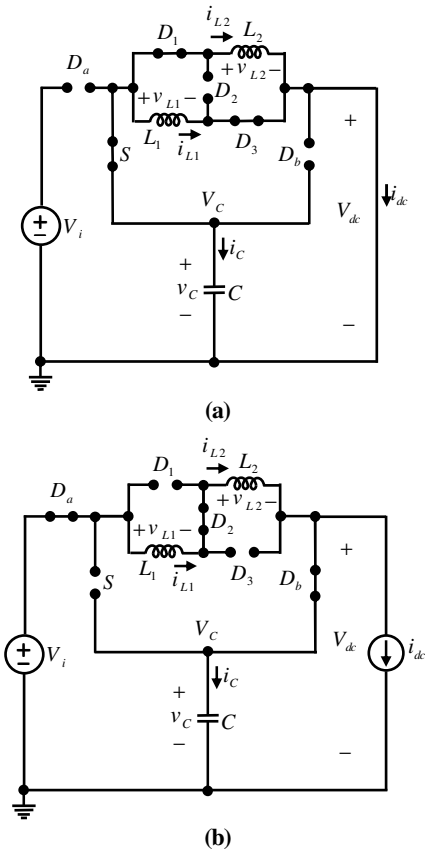


Fig. 2. The equivalent circuits of the proposed topology in different operating modes, **(a)** in the time interval of $D_{ST}T_s$, **(b)** in the time interval of$(1- D_{ST})T_s$

Firstly, it is assumed that the inductors of L_1 and L_2 have same inductances as follows:

$$L_1 = L_2 = L \tag{1}$$

According to Eq. (1), the current and voltage of these inductors in all operating modes are same. Therefore, we have:

$$v_{L1} = v_{L2} = v_L \tag{2}$$

$$i_{L1} = i_{L2} = i_L \tag{3}$$

v_L and i_L show the voltage and current of the inductors, respectively.

Considering Eqs.(1) to (3) and by applying KVL and KCL to the obtained equivalent circuits as shown in Figs. 2(a) and 2(b), it is resulted that:

$$v_L = \begin{cases} v_C & for\ \ 0 \le t < D_{ST}T_s \\ \dfrac{V_i - v_C}{2} & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{4}$$

$$i_C = \begin{cases} -2i_L & for\ \ 0 \le t < D_{ST}T_s \\ i_L - i_{dc} & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{5}$$

$$v_{dc} = \begin{cases} 0 & for\ \ 0 \le t < D_{ST}T_s \\ v_C & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{6}$$

where, v_C and i_C denote the voltage and current of the capacitor, respectively, and v_{dc} is the inverter input voltage. By neglecting the voltage and current ripples, these are rewritten as follows:

$$v_L = \begin{cases} V_C & for\ \ 0 \le t < D_{ST}T_s \\ \dfrac{V_i - V_C}{2} & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{7}$$

$$i_C = \begin{cases} -2I_L & for\ \ 0 \le t < D_{ST}T_s \\ I_L - I_{dc} & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{8}$$

$$v_{dc} = \begin{cases} 0 & for\ \ 0 \le t < D_{ST}T_s \\ V_C & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{9}$$

where, V_C and I_L are the average values of the v_C and i_L, respectively and I_{dc} is the inverter current in the time interval of $(1-D_{ST})T_s$.

Figure 3 shows the voltage and current waveforms of the proposed topology in steady state in CCM. In the time interval of $0 \le t < D_{ST}T_s$ the inductors voltage is a positive value and equal to V_C therefore, based on Fig. 3 and by considering the equations of the inductors voltage and current we have:

$$v_L = V_C \qquad for \quad 0 < t < D_{ST}T_s \tag{10}$$

$$i_L = \frac{1}{L}\int_0^t v_L\, dt + i_L\,|_{t=0} \tag{11}$$

According to Eqs. (10) and (11), the current of the inductors is linearly increased with the ratio of V_C/L. Therefore, we have:

$$i_L = \frac{V_C}{L}t + I_{LV} \tag{12}$$

In the time interval of $D_{ST}T_s \le t < T_s$ and based on the Fig. 3, the voltage of the inductors is a negative constant value that is equal to$(V_i-V_C)/2$. In other words:

$$v_L = \frac{V_i - V_C}{2} \qquad for \quad D_{ST}T_s < t < T_s \tag{13}$$

According to Eqs. (11) and (13), the current of the inductors is linearly decreased with the ratio of $\dfrac{V_i - V_C}{2L} < 0$ .In other words:

$$i_L = \frac{V_i - V_C}{2L}t + I_{LP} \tag{14}$$

In order to calculate the voltage gain of the proposed topology, the voltage balance law is used. According to this law, the average value of the inductor voltage in steady state is equal to zero in a period. Therefore:

$$\int_0^{T_s} v_L(t)\,dt = 0 \tag{15}$$

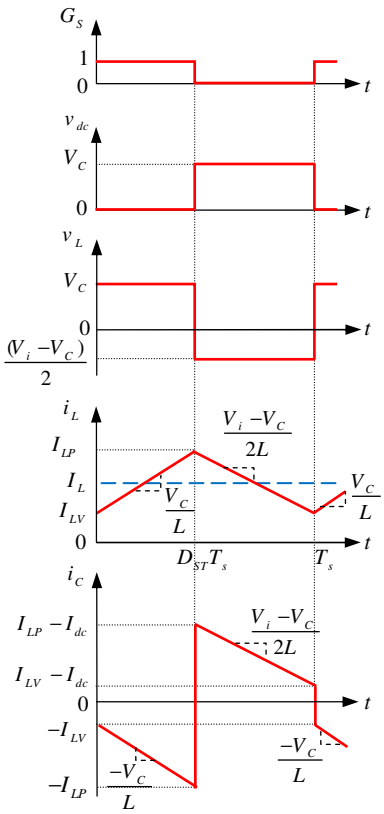


Fig. 3. The steady state waveforms of proposed Z-source inverter in CCM

By replacing the value of v_L from Eq. (7) into Eq.(15), we have:

$$\int_0^{D_{ST}T_s} V_C\,dt + \int_{D_{ST}T_s}^{T_s} \frac{(V_i - V_C)}{2}\,dt = 0 \tag{16}$$

By simplicity Eq. (16), it is resulted that:

$$\frac{V_C}{V_i} = \frac{1-D_{ST}}{1-3D_{ST}} \tag{17}$$

The variation curve of V_C/V_i versus D_{ST} is shown in Fig. 4. As shown in this figure, when, $D_{ST} = 0$, the value of V_C/V_i is equal to one and when D_{ST} is close to 0.333 this value is increased to the higher value. It is important to note that the value of duty cycle in ST state in the proposed Z-source inverter cannot be higher than 0.333.

According to current balance law, the average current of a capacitor is equal to zero in steady state. Thus, the following equation can be written:

$$\int_0^{T_s} i_C\,dt = 0 \tag{18}$$

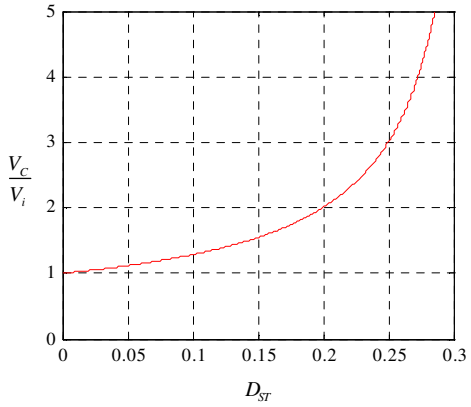


Fig. 4. Variation curve of V_C/V_i versus D_{ST} in the proposed Z-source inverter

By replacing i_C from Eq. (8) into Eq. (18), the above equation can be rewritten as follow:

$$\int_0^{D_{ST}T_s} -2I_L\,dt + \int_{D_{ST}T_s}^{T_s} (I_L - I_{dc})\,dt = 0 \tag{19}$$

Considering Eq. (19), the relation between the averages value of the inductors current and input current of the inverter in the non-ST state is equal to:

$$\frac{I_L}{I_{dc}} = \frac{1-D_{ST}}{1-3D_{ST}} \tag{20}$$

The average value of dc link V_{dc} is equal to:

$$V_{dc} = \frac{1}{T_s}\int_0^{T_s} v_{dc}\,dt \tag{21}$$

By replacing v_{dc} from Eq. (9) into Eq. (21), we have:

$$V_{dc} = \frac{1}{T_s}\int_0^{D_{ST}T_s} 0\,dt + \frac{1}{T_s}\int_{D_{ST}T_s}^{T_s} V_C\,dt = (1-D_{ST})' \tag{22}$$

2.2. Operating of the proposed inverter in boundary condition and calculation the minimum inductance in CCM

The inverter's waveforms in the boundary condition that the inductor current is reached to zero value are shown in Fig. 5.

According to Eqs. (17) and (20), the values of V_C/V_i and I_L/I_{dc} for the proposed boost Z-source

inverter are equal to $(1\text{-}D_{ST})/(1\text{-}3D_{ST})$. In the proposed topology, the value of input current from the voltage source is equal to zero because the diode of D_a is turned off in the time interval of $0 \le t \le D_{ST}T_s$. This current value in the second operating mode is equal to the inductors current. Thus, it is resulted that:

$$I_L = I_i \tag{23}$$

In Eq. (23), I_i is the input current from source side in the time interval of $(1\text{-}D_{ST})T_s$. By replacing Eq. (23) into Eq. (20) we have:

$$\frac{I_{dc}}{I_i} = \frac{1-3D_{ST}}{1-D_{ST}} \tag{24}$$

By replacing V_C from Eq. (22) into Eq. (17), it can be written:

$$\frac{V_{dc}}{V_i} = \frac{(1-D_{ST})^2}{1-3D_{ST}} \tag{25}$$

As the inductors are same, it is only required to calculate the current value of one of them. Based on the Fig. 5 it is obtained that:

$$I_{LP} = i_{LB1}\Big|_{t=D_{ST}T_s} = 0 + \frac{1}{L}\int_0^{D_{ST}T_s} V_C\, dt = \frac{V_C}{L} D_{ST}T_s \tag{26}$$

In Eq. (26), i_{LB1} is the inductor current of L_1 in boundary condition and I_{LP} is the maximum value of the inductors current. In boundary condition, I_{LP} is equal to the value of inductors current variations. In order to calculate the average current of the inductor (L_1) in the boundary condition, it is resulted that:

$$I_{LB} = \frac{\int_0^{T_s} i_{LB1}\, dt}{T_s} = \frac{\frac{1}{2} I_{LP}\, T_s}{T_s} = \frac{1}{2} I_{LP} \tag{27}$$

In Eq. (27), I_{LB} is the average current value of each inductor on boundary operation mode.By replacing I_{LP} from Eq. (26) into Eq. (27), the following equation is obtained:

$$I_{LB} = \frac{V_C T_s}{2L} D_{ST} = \frac{V_C}{2Lf_s} D_{ST} \tag{28}$$

By replacing V_C from Eq. (22) into Eq. (28) we have:

$$I_{LB} = \left(\frac{V_{dc}}{2Lf_s}\right)\frac{D_{ST}}{1-D_{ST}} \tag{29}$$

According to Eq. (25), in the boundary condition, we have:

$$I_{LB} = I_{iB} \tag{30}$$

where, I_{iB} is the input current to the impedance source network in the time interval of $(1\text{-}D_{ST})T_s$ in boundary operating mode.

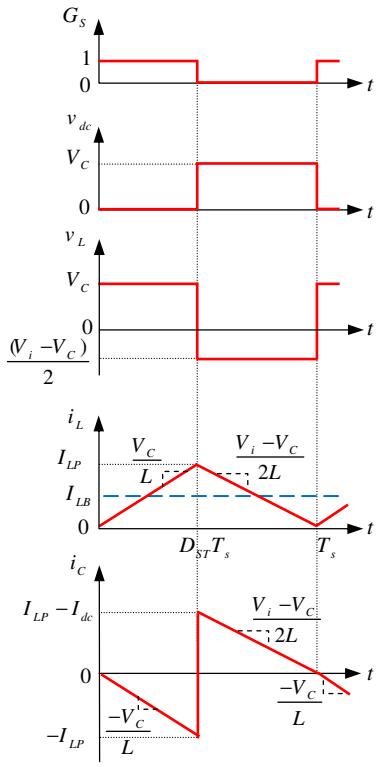


Fig. 5. Steady state waveforms of the proposed inverter in boundary operating

By replacing the value of I_{LB} from Eq. (29) into Eq. (30) the following equation is obtained:

$$I_{iB} = \left(\frac{V_{dc}}{2Lf_s}\right)\frac{D_{ST}}{1-D_{ST}} \tag{31}$$

According to Eq. (24), in the boundary condition, we have:

$$\frac{I_{dcB}}{I_{iB}} = \frac{1-3D_{ST}}{1-D_{ST}} \tag{32}$$

where, I_{dcB} is the drawn current by the inverter in the time interval of $(1\text{-}D_{ST})T_s$ and in the boundary operating mode. By replacing the value of I_{iB} from Eq. (31) into Eq. (32), the following equation is obtained:

$$I_{dcB} = \left(\frac{V_{dc}}{2Lf_s}\right)\frac{D_{ST}(1-3D_{ST})}{(1-D_{ST})^2} \tag{33}$$

In order to calculate the maximum value of I_{dcB}, the following equation can be used:

$$\frac{dI_{dcB}}{dD_{ST}} = 0 \tag{34}$$

According to Eq. (34), the value of D_{ST} is obtained as follows:

$$D_{ST} = 0.2 \tag{35}$$

By replacing the value of D_{ST} from Eq. (35) into Eq. (33) we have:

$$I_{dcB}\,|_{D_{ST}=0.2} = I_{dcB,\max} = 0.125\frac{V_{dc}}{Lf_S} \tag{36}$$

By replacing the value of $I_{dcB,\max}$ from Eq. (36) into Eq. (33) it is obtained that:

$$I_{dcB} = 4I_{dcB,\max}\frac{D_{ST}(1-3D_{ST})}{(1-D_{ST})^2} \tag{37}$$

Figure 6 shows the normalized current of I_{dcB} versus D_{ST}. In this condition, considering the value of $I_{dcB,\max}$, it is possible to calculate the minimum value of inductor to operate in boundary condition. By using Eq. (36) it is obtained that:

$$L_{\min} = 0.125\frac{V_{dc}}{I_{dcB,\max}f_s} = 0.125\frac{R_{L\max}}{f_s} \tag{38}$$

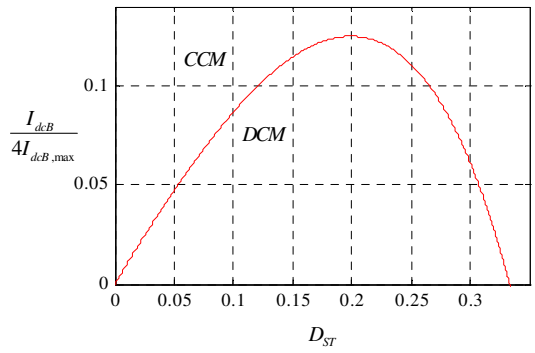


Fig. 6. Normalized curve of the inverter's drawn current versus D_{ST} in the boundary condition

3. DEVELOPED PROPOSED BOOST Z-SOURCE INVERTER

Developed Z-source network can be achieved by using several switched inductor cells as shown in Fig. 7. In this topology, all of the inductors of cell are equal(L_1=L_2=⋯=L_{n-1}=L_n=L). In the following, the operation of this inverter is analyzed.

In the time interval of $D_{ST}T_s$, the proposed topology is considered in ST state by turning on the upper and downer switches of the Inverter. In ST state, the switch of S is turned on and diodes of D_a and D_b are turned off. In addition, the diodes of $D_{1,2}$, $D_{2,2}$, ⋯,$D_{n-1,2}$ and $D_{n,2}$ are turned off while the diodes of $D_{1,1}$, $D_{1,3}$, $D_{2,1}$, $D_{2,3}$,⋯, $D_{n-1,1}$, $D_{n-1,3}$, $D_{n,1}$ and $D_{n,3}$ are turned on. In this condition, the inductors of L_1, L_2, ⋯,L_{n-1} and L_n are connected in parallel. The equivalent circuit of this state is shown in Fig. 8(a). By applying KVL and KCL to this circuit, it is resulted that:

$$v_{L1} = v_{L2} = \cdots = v_{Ln-1} = v_{Ln} = V_C \tag{39}$$

$$i_{L1} + i_{L2} + \cdots + i_{Ln-1} + i_{Ln} = -i_C \tag{40}$$

In the time interval of (1-D_{ST})T_s, the proposed topology is considered in non-ST state. In this state, the switch of S is turned off and diodes of D_a and D_b are turned on. In addition, the diodes of $D_{1,2}$, $D_{2,2}$, ⋯,$D_{n-1,2}$ and $D_{n,2}$ are turned on while the diodes of $D_{1,1}$, $D_{1,3}$, $D_{2,1}$, $D_{2,3}$,⋯, $D_{n-1,1}$, $D_{n-1,3}$,$D_{n,1}$ and $D_{n,3}$ are turned off. In this condition, the inductors of L_1, L_2, ⋯,L_{n-1} and L_n are connected series and transfer energy from dc voltage source to the main circuit. The equivalent circuit of this state is shown in Fig. 8(b). The voltage of the inductors L_1, L_2, ⋯,L_{n-1} and L_n are shown by v_{L1}, v_{L2}, ⋯,v_{Ln-1} and v_{Ln} respectively. By applying KVL and KCL to this circuit, it is resulted that:

$$v_{L1} + v_{L2} + \cdots + v_{Ln-1} + v_{Ln} + v_{dc} = V_i - V_C \tag{41}$$

$$i_{L1} = i_{L2} = \cdots = i_{Ln-1} = i_{Ln} = i_C + i_{dc} \tag{42}$$

As the voltage and current of the inductors are equal to each other, in the above equations v_L and i_L are considered as the voltage and current of the inductors, respectively. Thus, we have:

$$v_L = \begin{cases} v_C & for\ \ 0 \le t < D_{ST}T_s \\ \dfrac{V_i - v_C}{n} & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{43}$$

$$i_C = \begin{cases} -ni_L & for\ \ 0 \le t < D_{ST}T_s \\ i_L - i_{dc} & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{44}$$

$$v_{dc} = \begin{cases} 0 & for\ \ 0 \le t < D_{ST}T_s \\ v_C & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{45}$$

Neglecting the voltage and current ripples, the above equation is rewritten as follows:

$$v_L = \begin{cases} V_C & for\ \ 0 \le t < D_{ST}T_s \\ \dfrac{V_i - V_C}{n} & for\ \ D_{ST}T_s \le t < T_s \end{cases} \tag{46}$$

$$i_C = \begin{cases} -nI_L & for\ \ 0 \le t < D_{ST}T_s \\ I_L - I_{dc} & for\ \ D_{ST}T_s \le t < T_s \end{cases} \quad (47)$$

$$v_{dc} = \begin{cases} 0 & for\ \ 0 \le t < D_{ST}T_s \\ V_C & for\ \ D_{ST}T_s \le t < T_s \end{cases} \quad (48)$$

By replacing the value of v_L from Eq. (46) into Eq.(15), it is obtained:

$$I_{dcB}\ |_{D_{ST}=0.2} = I_{dcB,\max} = 0.125\frac{V_{dc}}{Lf_S} \quad (49)$$

By simplicity Eq. (49), the relation between capacitor voltage and input voltage is:

$$\frac{V_C}{V_i} = \frac{1-D_{ST}}{1-(n+1)D_{ST}} \quad (50)$$

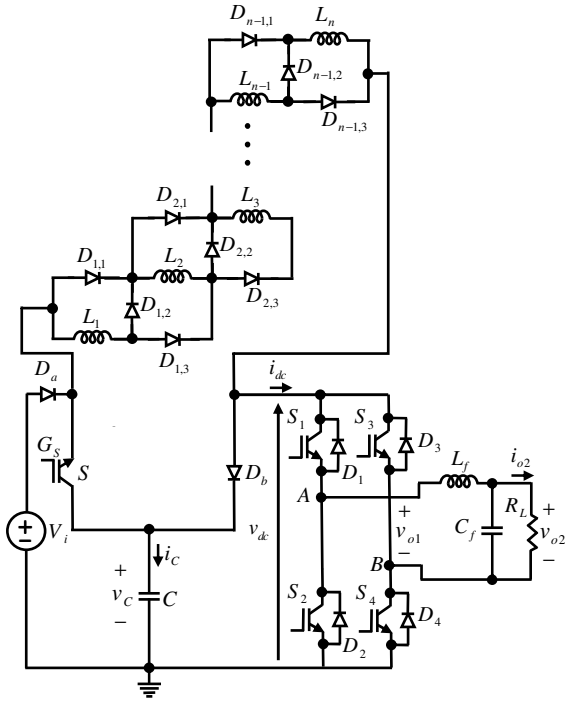


Fig. 7. Developed proposed Z-source inverter with $n-1$ switched cells

According to Eq. (50), when D_{ST}=0 the value of V_C/V_i is equal to one and when D_{ST} is close to 1/(n+1) this value is increased to the higher value. It is important to note that the value of duty cycle in ST state of the developed Z-source inverter cannot be higher than 1/(n+1).

By replacing, the value of i_C from Eq. (47) into Eq. (18) it is resulted that:

$$\int_0^{D_{ST}T_s} -nI_L\,dt + \int_{D_{ST}T_s}^{T_s} (I_L - I_{dc})\,dt = 0 \quad (51)$$

where, the relation between the average values of the inductors current and input current of the inverter in the non-ST state is:

$$\frac{I_L}{I_{dc}} = \frac{1-D_{ST}}{1-(n+1)D_{ST}} \quad (52)$$

By replacing v_{dc} from Eq. (48) into Eq. (21), the average voltage of dc link (V_{dc}) is given by:

$$V_{dc} = \frac{1}{T_s}\int_0^{D_{ST}T_s} 0\,dt + \frac{1}{T_s}\int_{D_{ST}T_s}^{T_s} V_C\,dt = (1-D_{ST})V_C \quad (53)$$

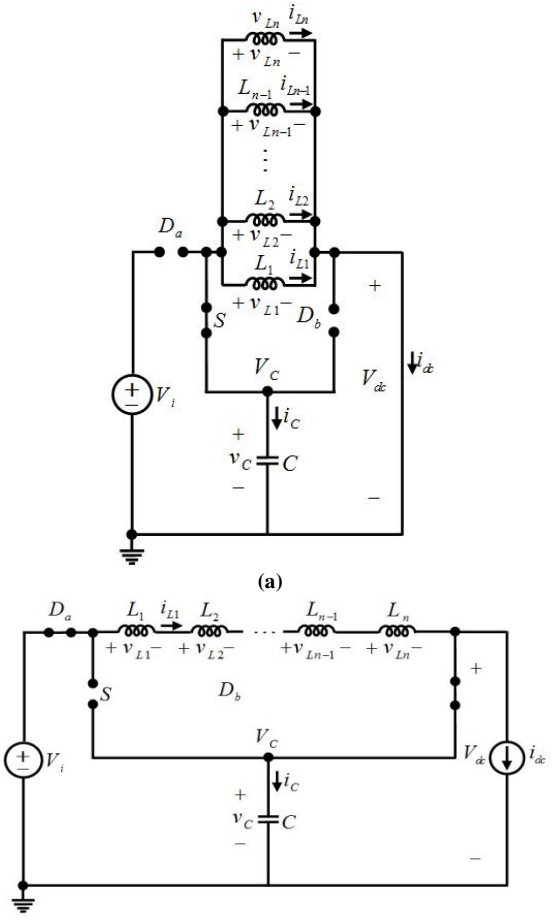


Fig. 8. The equivalent circuits of the developed inverter in different operating modes, **(a)** in the time interval of D_{ST}T$_s$, **(b)** in the time interval of (1- D_{ST})T$_s$

4. POWER LOSSES

In order to calculate the losses of proposed inverter the following assumptions are considered:

- The diodes are considered by an ideal switch in series with a resistor (R_D) representing the forward resistance and a voltage source (V_D) representing the forward voltage drop.

- The power electronic switches are considered by an ideal switch in series with a resistor (R_T) representing the forward resistance and a voltage source (V_T) representing the forward voltage drop.
- The equivalent series resistors of inductors and capacitors are considered.
- The inductors and diodes are all the same.

To obtain the converter power losses, the losses of each element must be calculated. Referring to Fig.7, by applying KCL to the input node of the proposed inverter the current through the switch S can be written as follows:

$$i_S = \begin{cases} nI_L & for\ \ 0 \le t \le D_{ST}T_s \\ 0 & for\ \ D_{ST}T_s \le t \le T_s \end{cases} \tag{54}$$

Using the above equation, the root mean square (RMS) value of the current through the switch S can be obtained as follows:

$$I_{S(RMS)} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_S^2 dt} = \sqrt{D_{ST}}\, nI_L \tag{55}$$

Hence, the ohmic power loss of switch the S is given by:

$$P_{RS} = I_{S(RMS)}^2 R_S = D_{ST}(nI_L)^2 R_S \tag{56}$$

Using the Eq. (54), the average value of current through the switch S is as follows:

$$I_S = D_{ST}\, nI_L \tag{57}$$

The power loss associated with the forward voltage drop V_T is:

$$P_{VT} = V_T I_S = D_{ST}\, nV_T I_L \tag{58}$$

Using the Eqs. (56) and (58), the conduction power losses of switch S are obtained as follows:

$$P_{C,S} = P_{RS} + P_{VT} = D_{ST}\, nI_L \left(nI_L R_S + V_T\right) \tag{59}$$

To obtain the switching power losses of switch, the energy losses during the turn-on and turn-off period of switch must be calculated. For this calculation, the linear approximation of the voltage and current during switching period is used. Using this approximation, the energy losses during the turn-on period of the switch can be obtained as follows:

$$\begin{aligned} E_{on,S} &= \int_0^{t_{on,S}} v_S(t) i_S(t)\, dt \\ &= \int_0^{t_{on,S}} [(V_C - V_i)(1 - \frac{t}{t_{on,S}})(nI_L \frac{t}{t_{on,S}})dt \end{aligned} \tag{60}$$

where, $v_s(t)$ is the voltage across the switch S and $i_s(t)$ is the current through the switch S.

Using the above equation, the turn-on loss of the switch can be calculated as follows:

$$E_{on,S} = n(V_C - V_i) I_L \frac{t_{on,S}}{6} \tag{61}$$

Also, the energy losses during the turn-off period of the switch can be obtained as follows:

$$\begin{aligned} E_{off,S} &= \int_0^{t_{off,S}} v_S(t) i_S(t)\, dt \\ &= \int_0^{t_{off,S}} \left((V_C - V_i)\frac{t}{t_{off,S}}\right)\left[nI_L\left(1 - \frac{t}{t_{off,S}}\right)\right]dt \end{aligned} \tag{62}$$

Using the above equation, the turn-off loss of the switch is given by:

$$E_{off,S} = n(V_C - V_i) I_L \frac{t_{off,S}}{6} \tag{63}$$

From Eqs. (59), (61) and (63), the power losses of the switch are as follows:

$$\begin{aligned} P_S &= nI_L D_{ST}\left(nI_L R_S + V_T\right) \\ &\quad + nI_L \frac{(V_C - V_i)}{6}(t_{on,S} + t_{off,S}) \end{aligned} \tag{64}$$

The current through the diode D_a is:

$$i_{Da} = \begin{cases} 0 & for\ \ 0 \le t \le D_{ST}T_s \\ I_L & for\ \ D_{ST}T_s \le t \le T_s \end{cases} \tag{65}$$

The RMS value of the current through this diode is

$$I_{\_} = \sqrt{1 - D_{\_}}\, I \tag{66}$$

Hence, the ohmic power loss of diode D_a is given by:

$$P_{RDa} = I_{Da(RMS)}^2 R_D = (1 - D_{ST}) I_L^2 R_D \tag{67}$$

The average value of current through the diode D_a is:

$$I_{Da} = (1 - D_{ST}) I_L \tag{68}$$

Thus, the power loss associated with the forward voltage drop V_D will be equal to:

$$P_{VDa} = V_D I_{Da} = (1 - D_{ST}) V_D I_L \tag{69}$$

Using the Eqs. (67) and (69), the conduction losses of diode D_a are calculated as follows:

$$P_{C,Da} = P_{RDa} + P_{VDa} = (1 - D_{ST}) I_L (I_L R_D + V_D) \tag{70}$$

To obtain the switching power losses of diode, the energy losses during the turn-on and turn-off time intervals of diode must be calculated. For this calculation, the linear approximation of the voltage and current during switching period is used. Using this approximation, the energy losses during the turn-on and turn-off time intervals of diode D_a can be obtained as follows:

$$E_{on,Da} = \int_0^{t_{on,D}} v_{Da}(t) i_{Da}(t)\,dt = (V_C - V_i) I_L \frac{t_{on,D}}{6} \tag{71}$$

$$E_{off,Da} = \int_0^{t_{off,D}} v_{Da}(t) i_{Da}(t)\,dt = (V_C - V_i) I_L \frac{t_{off,D}}{6} \tag{72}$$

From Eqs. (70), (71) and (72), power losses of diode D_a are obtained as follows:

$$P_{Da} = I_L (1 - D_{ST})(I_L R_D + V_D) + I_L \frac{(V_C - V_i)}{6}(t_{on,D} + t_{off,D}) \tag{73}$$

The current through the diode D_b is equal to:

$$i_{Db} = \begin{cases} 0 & for\ \ 0 \le t \le D_{ST} T_s \\ I_L - I_{dc} & for\ \ D_{ST} T_s \le t \le T_s \end{cases} \tag{74}$$

where, I_{dc} is the average value of input current in time interval $D_{ST} T_s \le t \le T_s$.

The RMS value of the current through this diode is:

$$I_{Db(RMS)} = \sqrt{1 - D_{ST}}\,(I_L - I_{dc}) \tag{75}$$

Hence, the ohmic power loss of diode D_b is obtained as follows:

$$P_{RDb} = I_{Db(RMS)}^2 R_D = (1 - D_{ST})(I_L - I_{dc})^2 R_D \tag{76}$$

The average value of current through diode D_b is:

$$I_{Db} = (1 - D_{ST})(I_L - I_{dc}) \tag{77}$$

Thus, the power loss associated with the forward voltage drop V_D is:

$$P_{VDb} = V_D I_{Db} = (1 - D_{ST}) V_D (I_L - I_{dc}) \tag{78}$$

Using the Eqs. (76) and (78), the conduction losses of diode D_b are calculated as follows:

$$P_{C,Db} = (1 - D_{ST})(I_L - I_{dc})\left((I_L - I_{dc}) R_D + V_D\right) \tag{79}$$

Using the linear approximation of the voltage and current during switching period, the energy losses during the turn-on and turn-off time intervals of diode D_b can be obtained as follows:

$$E_{on,Db} = \int_0^{t_{on,D}} v_{Db}(t) i_{Db}(t)\,dt = (V_C - V_i)(I_L - I_{dc}) \frac{t_{on,D}}{6} \tag{80}$$

$$E_{off,Db} = \int_0^{t_{off,D}} v_{Db}(t) i_{Db}(t)\,dt = (V_C - V_i)(I_L - I_{dc}) \frac{t_{off,D}}{6} \tag{81}$$

From the Eqs. (79), (80) and (81), the power losses of diode D_b are obtained as follows:

$$P_{Db} = (I_L - I_{dc})(1 - D_{ST})\left((I_L - I_{dc}) R_D + V_D\right) + (I_L - I_{dc}) \frac{(V_C - V_i)}{6}(t_{on,D} + t_{off,D}) \tag{82}$$

The current through capacitor C can be written as follows:

$$i_C = \begin{cases} -n I_L & for\ \ 0 \le t \le D_{ST} T_s \\ I_L - I_{dc} & for\ \ D_{ST} T_s \le t \le T_s \end{cases} \tag{83}$$

Using the above equation, the RMS value of current through capacitor C is calculated as follows:

$$I_{C(RMS)} = \sqrt{D_{ST} (n I_L)^2 + (1 - D_{ST})(I_L - I_{dc})^2} \tag{84}$$

Using the above equation, the ohmic power loss of the capacitor C is obtained as follows:

$$P_{rC} = I_{C(RMS)}^2 r_C = \left(D_{ST} (n I_L)^2 + (1 - D_{ST})(I_L - I_{dc})^2\right) r_C \tag{85}$$

In the following, the power losses of switched inductor cell are calculated. In general, this cell is included $3 \times (n-1)$ diodes and n inductors that diodes are divided into two groups. The first group of diodes $(D_{i,j}\ (i = 1 to\ n-1,\ j = 1,3))$ is turn on in shoot-through state and the second group of diodes $(D_{i,j}\ (i = 1\ \ to\ \ n-1,\ j = 2))$ is turn on in non-shoot-through state. The power losses of inductors are consisted of the core power losses and winding power losses. In PWM technique, the core power losses are ignored, but the winding power losses are very important.

The winding power loss of one inductor can be written as follows:

$$P_{rL1} = I_{L(RMS)}^2 r_L = I_L^2 r_L \tag{86}$$

Considering Eq. (86), the power losses of all inductors are obtained as follows:

$$P_{rL} = n\, I_L^2 r_L \tag{87}$$

The current through the diode $D_{11}$is:

$$i_{D11} = \begin{cases} 0 & for\ \ 0 \le t \le D_{ST} T_s \\ I_L - I_{dc} & for\ \ D_{ST} T_s \le t \le T_s \end{cases} \tag{88}$$

The RMS value of current through this diode is calculated as follows:

$$I_{D11(RMS)} = \sqrt{D_{ST}}\ I_L \tag{89}$$

Hence, the ohmic power loss of diode $D_{11}$is obtained as follows:

$$P_{RD11} = I_{D11(RMS)}^2 R_D = D_{ST}\ I_L^2 R_D \tag{90}$$

The average value of current through diode $D_{11}$is equal to:

$$I_{D11} = D_{ST}\ I_L \tag{91}$$

The power loss associated with the forward voltage drop V_D is given by:

$$P_{VD11} = V_D I_{D11} = D_{ST} V_D I_L \tag{92}$$

Using the Eqs. (90) and (92), the conduction losses of diode D_{11} are calculated as follows:

$$P_{C,D11} = P_{RD11} + P_{VD11} = D_{ST}\ I_L \left(I_L R_D + V_D\right) \tag{93}$$

Using the linear approximation of the voltage and current during switching period, the energy losses during the turn-on and turn-off time intervals of the diode D_{11} can be obtained as follows:

$$\begin{aligned} E_{on,D11} &= \int_0^{t_{on,D}} v_{D11}(t) i_{D11}(t)\, dt \\ &= \int_0^{t_{on,D}} \frac{(V_C - V_i)}{n}\left(1 - \frac{t}{t_{on,D}}\right) I_L \left(\frac{t}{t_{on,D}}\right) dt \\ &= \frac{(V_C - V_i) I_L}{n} \frac{t_{on,D}}{6} \end{aligned} \tag{94}$$

$$\begin{aligned} E_{off,D11} &= \int_0^{t_{off,D}} v_{D11}(t) i_{D11}(t)\, dt \\ &= \int_0^{t_{off,D}} \frac{(V_C - V_i)}{n}\left(\frac{t}{t_{off,D}}\right) I_L \left(1 - \frac{t}{t_{off,D}}\right) dt \\ &= \frac{(V_C - V_i) I_L}{n} \frac{t_{off,D}}{6} \end{aligned} \tag{95}$$

From the Eqs. (93), (94) and (95), the power losses of the diode D_{11} is obtained as follows:

$$\begin{aligned} P_{D11} &= I_L D_{ST} \left(I_L R_D + V_D\right) \\ &\quad + I_L \frac{(V_C - V_i)}{6n} (t_{on,D} + t_{off,D}) \end{aligned} \tag{96}$$

Using the above equation, the total power losses of diodes $D_{i,j}$ $(i = 1\ to\ n-1,\ j = 1,3)$ are obtained as follows:

$$\begin{aligned} P_{D,G1} &= 2(n-1) P_{D11} \\ &= 2(n-1) I_L D_{ST} \left(I_L R_D + V_D\right) \\ &\quad + 2(n-1) I_L \frac{(V_C - V_i)}{6n} (t_{on,D} + t_{off,D}) \end{aligned} \tag{97}$$

The current through the diode D_{12} is:

$$i_{D12} = \begin{cases} 0 & for\ \ 0 \le t \le D_{ST} T_s \\ I_L & for\ \ D_{ST} T_s \le t \le T_s \end{cases} \tag{98}$$

The RMS value of the current through this diode is calculated as follows:

$$I_{D12(RMS)} = \sqrt{1 - D_{ST}}\ I_L \tag{99}$$

Hence, the ohmic power loss of the diode D_{12} is obtained as follows:

$$P_{RD12} = I_{D12(RMS)}^2 R_D = (1 - D_{ST})\, I_L^2 R_D \tag{100}$$

The average value of current through diode D_{12} is:

$$I_{D12} = (1 - D_{ST})\, I_L \tag{101}$$

The power loss associated with the forward voltage drop V_D is given by:

$$P_{VD12} = V_D I_{D12} = (1 - D_{ST}) V_D I_L \tag{102}$$

Using the Eqs. (100) and (102), the conduction losses of the diode D_{12} are calculated as follows:

$$\begin{aligned} P_{C,D12} &= P_{RD12} + P_{VD12} \\ &= (1 - D_{ST})\, I_L \left(I_L R_D + V_D\right) \end{aligned} \tag{103}$$

The energy losses during the turn-on and turn-off time intervals of diode D_{12} can be obtained as follows:

$$\begin{aligned} E_{on,D12} &= \int_0^{t_{on,D}} v_{D12}(t) i_{D12}(t)\, dt \\ &= \int_0^{t_{on,D}} V_C \left(1 - \frac{t}{t_{on,D}}\right) I_L \frac{t}{t_{on,D}} dt = V_C I_L \frac{t_{on,D}}{6} \end{aligned} \tag{104}$$

$$\begin{aligned} E_{off,D12} &= \int_0^{t_{off,D}} v_{D12}(t) i_{D12}(t)\, dt \\ &= \int_0^{t_{off,D}} V_C \left(\frac{t}{t_{on,D}}\right) I_L \left(1 - \frac{t}{t_{on,D}}\right) dt = V_C I_L \frac{t_{off,D}}{6} \end{aligned} \tag{105}$$

From the Eqs. (103), (104) and (105), the power losses of the diode $D_{12}$is given by:

$$\begin{aligned} P_{D12} &= I_L (1 - D_{ST}) \left(I_L R_D + V_D\right) \\ &\quad + I_L \frac{V_C}{6} (t_{on,D} + t_{off,D}) \end{aligned} \tag{106}$$

Using the above equation, the total power losses of diodes $D_{i,j}$ $(i = 1\ to\ n-1,\ j = 2)$ is given by:

$$\begin{aligned} P_{D,G2} &= (n-1) P_{D12} \\ &= (n-1) I_L (1 - D_{ST}) \left(I_L R_D + V_D\right) \\ &\quad + (n-1) I_L \frac{V_C}{6} (t_{on,D} + t_{off,D}) \end{aligned} \tag{107}$$

Finally, using the Eqs. (64), (73), (82), (85), (87), (97) and (107), the total power losses of the developed topology are calculated as follows:

$$P_{loss} = P_S + P_{Da1} + P_{Da2} + P_{rC} + P_{rL} + P_{D,G1} + P_{D,G2} \quad (108)$$

5. PRESENTED CONTROL METHOD

In Fig. 9, a modified PWM control method for the proposed inverter based on conventional triangle-sinusoidal PWM control method with the unipolar voltage switching is presented. In this method, the power switch of S has only two switching time intervals in each period. Here, the switching frequency is considered constant. Fig. 9(a) shows the total scheme of the control circuit to generate the PWM control signals of the converter by using the modified PWM control method. Fig. 9(d) shows the generated control signals in the half period (positive time interval) of the $v_m(t)$. As shown in this figure, the gate control signals for the switches S_1 and S_2 are generated by a comparison of the sinusoidal modulation signals of $v_m(t)$and $-v_m(t)$ that are shown in Fig. 9(b) with the triangle high frequency carrier signal of $v_{tri}(t)$ with the magnitude of V_P. The frequency of carrier signal (f_S) is selected in a way that $f_s >> f_o$. Therefore, the value of v_m is approximately assumed constant as shown in Fig. 9(d).

The signals of ST_1 and ST_2 are generated by comparing the voltage of $v_{tri}(t)$ with two constant voltages of V_{ST} and $-V_{ST}$ in the duty cycle of D_{ST}. The main aim of using these two signals is determining the required time for short circuit in the time interval of $D_{ST}T_S$. In this state, it is possible to obtain the control signals of the switches S_1 and S by using the following logical decisions:

If $V_{ST} > v_{tri}(t)$, therefore $ST_1 = 1$.

If $-V_{ST} < v_{tri}(t)$, therefore $ST_2 = 1$.

If $v_m(t) > v_{tri}(t)$, therefore $G_1 = 1$.

If $-v_m(t) < v_{tri}(t)$, therefore $G_4 = 1$.

According to the above conditions, signals of the G_2, G_3 and G_4 in the modified PWM control method are obtained as follows:

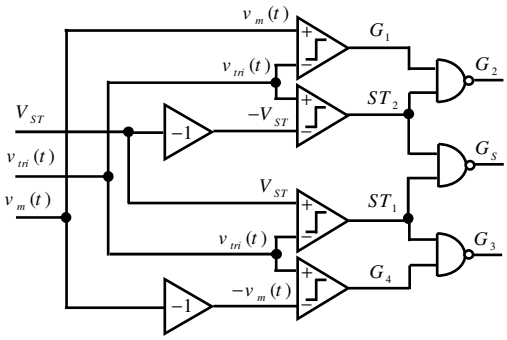
$$G_2 = \overline{G_1 \wedge ST_2} \quad (109)$$

$$G_3 = \overline{G_4 \wedge ST_1} \quad (110)$$

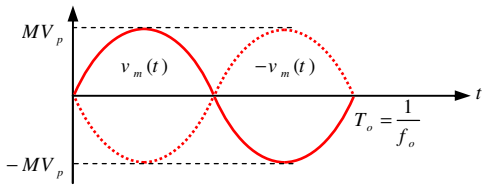
$$G_S = \overline{ST_1 \wedge ST_2} \quad (111)$$

where, "$\overline{\quad}$" means logically "NOT".

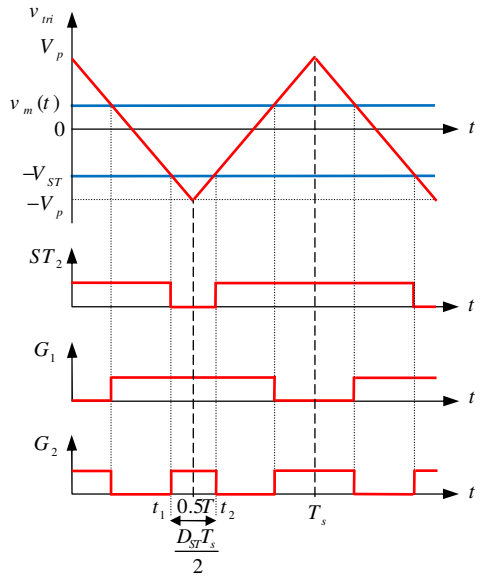
The voltage waveforms in input (V_{dc}) and output (v_{o1}) of the inverter are shown in Fig. 9(d). It is obvious that v_{o1}consists of nine time intervals in each period of T_s. Table 1 shows the on and off states of switches in the proposed boost Z-source inverter. It is obvious from Fig. 9(c) that the value of duty cycle D_{ST} can change based on different values of V_{ST}. As shown in Fig. 9(c), the slope of the line (a) in the time interval of $0 \le t < (T_s / 2)$ is given by:



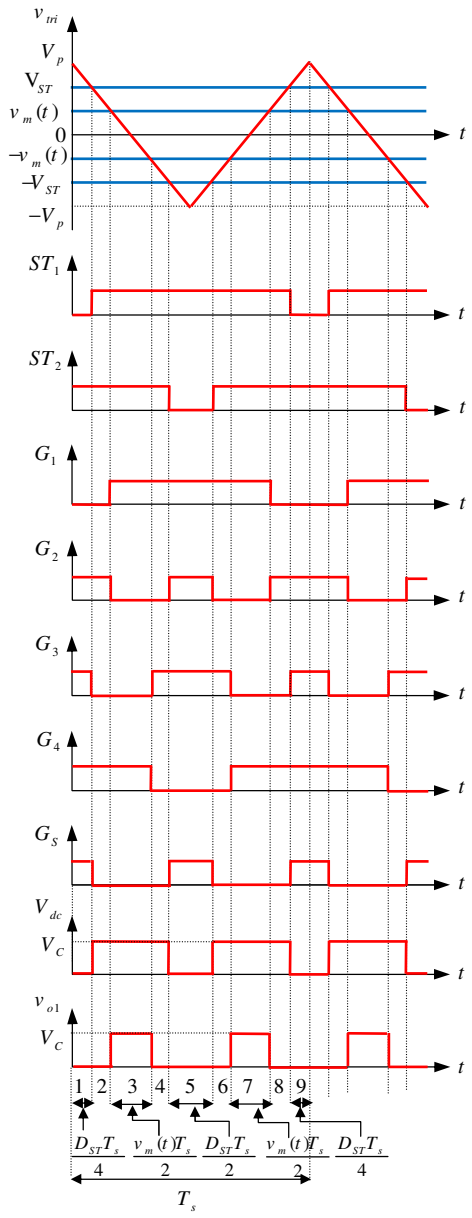
(a)



(b)



(c)



(d)

Fig. 9. (a) Control method; **(b)** sinusoidal modulation of the signals $v_m(t)$ and $-v_m(t)$; **(c)** the generation of shoot-through in the leg of the switches S_1 and S_2; **(d)** control signals of PWM for the proposed inverter in the half time interval of positive period of

$$a=\frac{-V_p-V_p}{(T_s/2)}=\frac{-V_p}{(T_s/4)} \tag{112}$$

By replacing Eq. (112) into line equation and by considering the coordinates of $\begin{vmatrix}0\\V_P\end{vmatrix}$, it is obtained that:

$$v_{tri}(t)-V_p=a(t-0)=\frac{-V_p}{(T_s/4)}t \tag{113}$$

By simplifying Eq. (113) we have:

$$v_{tri}(t)=\frac{-V_p}{(T_s/4)}t+V_p \tag{114}$$

Table 1. On and off states of switches in the proposed boost Z-source inverter

Number of time intervals	Turned on elements
(9) and (1)	S_1 , S_3 , S_4 and S
(8) and (2)	S_2 and S_4
(7) and (3)	S_1 and S_2 (S_3 and S_4 in the negative half of the period of $v_m(t)$)
(6) and (4)	S_1 and S_3
(5)	S_1 , S_3 , S_4 and S

By simplifying Eq. (114), the equation of $v_{tri}(t)$ in the time interval of $0\le t<(T_s/2)$ is calculated as follows:

$$v_{tri}(t)=\frac{-V_p}{T_s/4}(t-\frac{T_s}{4}) \tag{115}$$

According to Fig. 9(c), the line slope in the time interval of $(T_s/2)\le t<T_s$ is obtained as follows:

$$a=\frac{V_p-(-V_p)}{(T_s/2)}=\frac{V_p}{(T_s/4)} \tag{116}$$

By replacing Eq. (61) into line equation and by considering the coordinates of $\begin{vmatrix}T_s\\V_P\end{vmatrix}$, the following equation is obtained:

$$v_{tri}(t)-V_p=a(t-T_s)=\frac{V_p}{(T_s/4)}t-4V_p \tag{117}$$

By simplifying Eq. (117) we have:

$$v_{tri}(t)=\frac{V_p}{(T_s/4)}t-3V_p \tag{118}$$

By simplifying Eq. (118), the equation of $v_{tri}(t)$ in the time interval of $(T_s/2)\le t<T_s$ is:

$$v_{tri}(t)=\frac{V_p}{(T_s/4)}(t-\frac{3T_s}{4}) \tag{119}$$

Considering Eqs. (115) and (119) the following equation is obtained:

$$v_{tri}(t)=\begin{cases}\dfrac{-V_p}{(T_s/4)}(t-\dfrac{T_s}{4}) & for\ \ 0\le t<\dfrac{T_s}{2}\\[2ex] \dfrac{V_p}{(T_s/4)}(t-\dfrac{3T_s}{4}) & for\ \ \dfrac{T_s}{2}\le t<T_s\end{cases} \tag{120}$$

From Fig. 9(c), the below equations are resulted:

$$v_{tri}(t_1) = -V_{ST} \quad (121)$$

$$v_{tri}(t_2) = -V_{ST} \quad (122)$$

$$v_{tri}(t_1) = v_{tri}(t_2) \quad (123)$$

$$t_2 - t_1 = \frac{D_{ST}T_s}{2} \quad (124)$$

By replacing Eq. (121) into Eq. (120) in the time interval of $0 \le t < (T_s/2)$ it is resulted that:

$$-V_{ST} = \frac{-V_p}{(T_s/4)}(t_1 - \frac{T_s}{4}) \quad (125)$$

By simplifying Eq. (125) we have:

$$t_1 = \frac{T_s}{4}(1 + \frac{V_{ST}}{V_p}) \quad (126)$$

In addition, by replacing Eq. (122) into Eq. (120) in the time interval of $(T_s/2) \le t < T_s$, it is resulted that:

$$-V_{ST} = \frac{V_p}{(T_s/4)}(t_2 - \frac{3T_s}{4}) \quad (127)$$

By simplifying Eq. (127) we have:

$$t_2 = \frac{T_s}{4}(3 - \frac{V_{ST}}{V_p}) \quad (128)$$

Considering Eqs.(127), (128) and (124), we have:

$$\frac{D_{ST}T_s}{2} = \frac{T_s}{4}(3 - \frac{V_{ST}}{V_p}) - \frac{T_s}{4}(1 + \frac{V_{ST}}{V_p}) \quad (129)$$

By simplifying Eq. (129) we have:

$$D_{ST} = \frac{4T_s}{4T_s} - \frac{4T_s V_{ST}}{4T_s V_p} = 1 - \frac{V_{ST}}{V_p} \quad (130)$$

5.1. Investigation the effect of short circuit in the output voltage (v_{o1})

Figure 9(d) shows the input voltage (V_{dc}) and output voltage (v_{o1}) of the inverter. It is clear that the output voltage (v_{o1}) consists of three zero time intervals (whenv_{o1}=0) and two non-zero time intervals (when v_{o1}=V_C) in each period. In order to be certain that the time interval of ST state is not higher than the non-zero time interval of the inverter and it does not have interference with the time intervals of power v_{o1}, the value of D_{ST} has to be selected in a way that the total time interval of ST state does not more than an available total zero time interval in each duty cycle. In other word:

$$D_{ST}T_s < T_s - \max((v_m(t)T)_s / V_p) \quad (131)$$

By simplifying Eq. (131), we have:

$$D_{ST} < 1 - M \quad (132)$$

where, $M = \max(v_m(t)/V_p)$ is the inverter modulation index.

Considering Eqs. (130) and (132), the following result is obtained:

$$1 - \frac{V_{ST}}{V_p} < 1 - \mathrm{M} \quad (133)$$

By simplifying Eq. (133), we have:

$$V_{ST} > M\,V_p \quad (134)$$

If the value of V_{ST} is selected based on (134), the harmonic spectrum of $v_{o1}$is as same as voltage source inverter that is controlled by the conventional triangle-sinusoidal PWM with the unipolar voltage switching. In addition, the maximum fundamental component value of $v_{o1}$is obtained as follows:

$$(V_{o1,\max})_{fundamental} = V_{o2,\max} = MV_C = M(\frac{1 - D_{ST}}{1 - 3D_{ST}})V_i \quad (135)$$

6.COMPARISON OF THE PROPOSED TOPOLOGY

6.1. Comparison the voltage boost factor versus different duty cycles

Figure 10 compares the voltage boost factor of the proposed topology with the conventional topologies [2], [14-16]. The high boost factor in the proposed inverter makes it suitable in low power applications.

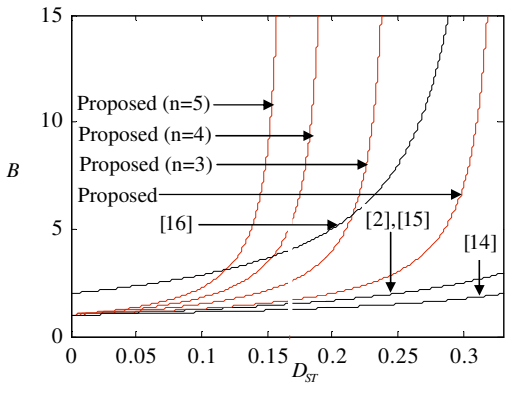


Fig. 10. Voltage ratio versus D_{ST}

6.2. Comparison the number of used devices

The number of used devices in the proposed inverter and conventional Z-source inverters regardless of the used elements in the H-bridge and output LC filter are compared in Table 2. It is obvious from this Table that in the proposed inverter three passive elements and six semiconductor switches are used. However, in the switched boost inverter (SBI) two passive elements, three semiconductor switches and in the Z-source and quasi-Z-source inverters four passive elements and one semiconductor are used. In the switched-inductor quasi-Z-source inverter (SL-QZSI) six passive elements and three semiconductor switches are used. According to Table 2, it seems that SBI needs a lower number of passive elements in comparison with the other topologies, but its low voltage boost factor in comparison with the proposed topology makes it unsuitable in most applications.

Table 2. Comparison the number of elements in the proposed inverter with the conventional Z-source inverters

Kind of devises	Number of devices				
	Proposed	SBI [14]	ZSI [2]	QZSI [15]	SL-QZSI [16]
Inductor	2	1	2	2	3
Capacitor	1	1	2	2	3
Switch	1	1	0	0	0
Diode	5	2	1	1	3

6.3. Comparison the value of ST tolerance

In the Z-source inverter, the value of drawn current from impedances network is limited when the ST state is made. As a result, the switches will not damage, but this state is impossible in the conventional voltage source inverter. In addition, in the proposed inverter the current is limited by using the inductors when the ST state is made and the switches will not damage. Therefore, the proposed inverter as same as ZSI and SBI are able to tolerance the ST state and have better immunity than the conventional voltage source inverter.

6.4. Comparison of capacitor voltage, dc link voltage and output power

In this section, the proposed boost Z-source inverter is compared with conventional topologies. Table 3 shows the used parameters to calculate the voltage and power of the inverters. Table 4 shows the results of the calculated output voltage and power for different topologies. According to the results obtained in Table 4 consider that under the same condition with V_i=64V and D_{ST}=0.3, maximum input voltage of inverter in the ZSI is 160V, in SBI is 112V and in the proposed topology is 448V. This leads to obtain a higher output power in proposed topology than the two other topologies.

Table 3. Parameters used for comparing the proposed inverter and conventional Z-source inverters

V_i	64V
M	0.5
D_{ST}	0.15
R_L	25 Ω

Table 4. The output voltage and power in the proposed inverter and conventional Z-source inverters

	B	$V_{dc,\max}$	$V_{o2,\max}$	$P_{o2}=V_{o2,\max}^2/R_L$
Proposed ($n=2$)	$\frac{1-D_{ST}}{1-3D_{ST}}$	$98.9V$	$49.45V$	$97.8W$
Proposed ($n=5$)	$\frac{1-D_{ST}}{1-6D_{ST}}$	$544V$	$272V$	$2959.6W$
SBI [14]	$\frac{1-D_{ST}}{1-2D_{ST}}$	$77.7V$	$38.85V$	$60.37W$
ZSI [2]	$\frac{1}{1-2D_{ST}}$	$91.4V$	$45.7V$	$83.54W$
QZSI [15]	$\frac{1}{1-2D_{ST}}$	$91.4V$	$45.7V$	$83.54W$
SL-QZSI [16]	$\frac{2}{1-3D_{ST}}$	$232.7V$	$116.4V$	$541.6W$

7.SIMULATION RESULTS

7.1. Ideal proposed boost Z-source inverter

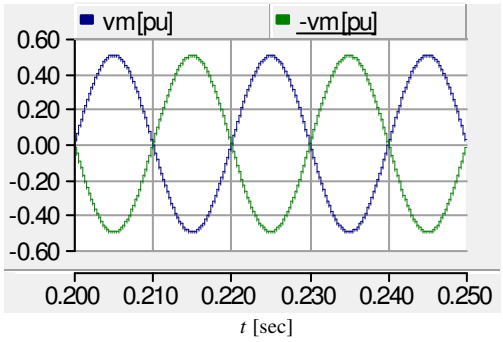
In order to verify the accuracy performance of the proposed inverter the simulation results by using EMTDC/PSCAD software are done. Table 5 shows the used parameters in the simulated inverter.

Table 5. The parameters used in the simulation

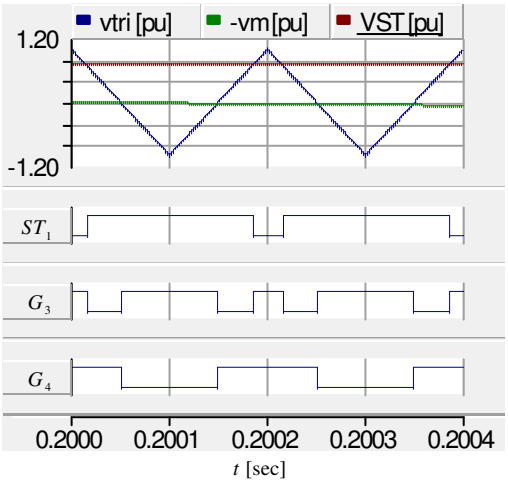
Parameter/Component	Value
Input voltage (V_i)	$64V$
Fundamental frequency (f_o)	$50\,Hz$
Switching frequency (f_s)	$5\,kHz$
Shoot-through duty cycle (D_{ST})	0.3
Modulation index (M)	0.5
Inductor (L)	$5\,mH$
Capacitor (C)	$470\,\mu F$
Inductance of output filter (L_f)	$4.6\,mH$
Capacitor of output voltage (C_f)	$10\,\mu F$
Load resistance (R_L)	25 Ω

In order to control the switches, the triangle-sinusoidal PWM control method that is shown in Fig. 9 is used. The magnitude of carrier signal (V_p) is considered equal to one. Therefore, to obtain the presented duty cycle in Table 5 (D_{ST}=0.3) and according to Eq. (130), the value of $|V_{ST}|$ is obtained 0.7 . In addition, based on the presented values of D_{ST} and Min Table 5, the enough condition to correct performance of the proposed inverter that is presented in Eq. (132) is made.

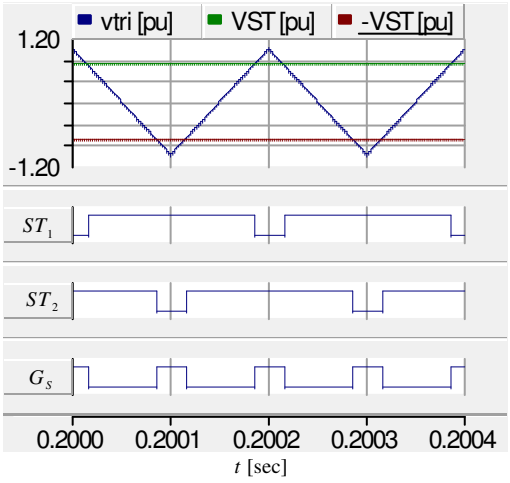
The short circuit signals are obtained by comparing two signals of V_{ST} and-V_{ST} with the carrier signal. The required signals for the switches $G_1$and $G_4$are obtained by comparing the sinusoidal modulation signals of $v_m(t)$ and -$v_m(t)$ with carrier signal. The gate signals of other switchesG_1, G_3 and G_S are obtained by using logical combinations ofG_1, G_4, *ST1* and *ST2*that are presented by Eq. (109) to (111). Figure 11 shows the sinusoidal modulation signals of $v_m(t)$ and -$v_m(t)$ and the PWM control signals that are generated by using the PWM control circuit as shown in Fig. 9(a).



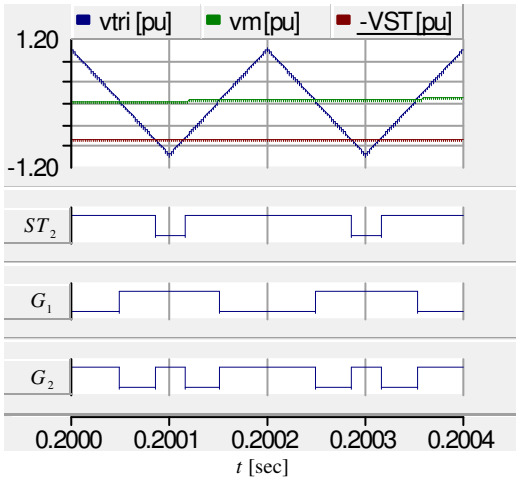
(a)



(b)



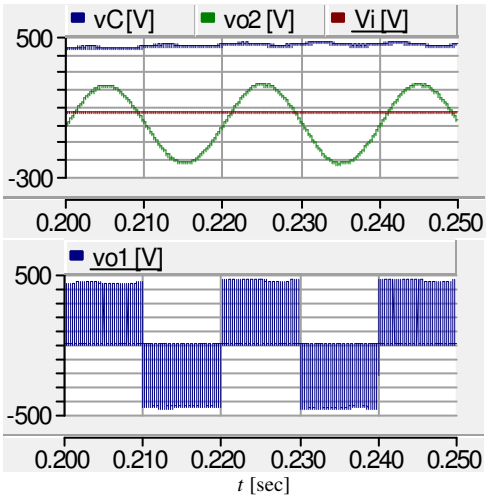
(c)



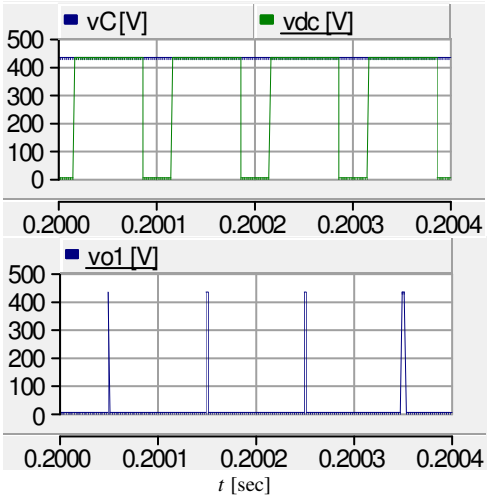
(d)

Fig. 11. Generation of PWM control signals for the proposed inverter, **(a)** the sinusoidal modulation signals of $v_m(t)$ and $-v_m(t)$, **(b)** generation of ST state in the switches S_1 and S_2 of the inverter, **(c)** generation of ST state in the switches S_3 and S_4 of the inverter, **(d)** generation of signal gate for switches S

Figure 12 shows the output and input voltage waveforms of the inverter. According to used values in Table 5 and based on Eq. (17), the capacitor voltage value at the duty cycle of D_{ST}=0.3isV_C=448V that is reconfirmed in Fig. 12. In addition, according to the presented equations in Table 4 and the presented value in Table 5, the maximum value of $V_{o2,\max}$ is $224V$ that is reconfirmed in Fig.12(a).



(a)



(b)

Fig. 12. Steady state performance of the proposed inverter, **(a)** input voltage (V_i), capacitor voltage (V_C), load voltage (V_{o2}) and the output voltage of inverter (V_{o1}), **(b)** capacitor voltage (V_C), input voltage of the inverter (V_{dc}) and the output voltage of inverter (V_{o1})

7.2. Power losses of the proposed boost Z-source inverter

Table 6 shows the selected values and parameters of the devices and other parameters in non-ideal simulation.

Since in the non-ideal conditions, voltage and current values do not follow from the equations obtained in the previous sections. So, under these conditions, it is essential to obtain some values from the simulation results. According to the values of Table 6, the average value of the capacitor voltage, average value of the one of inductors and average value of inverter input current in time interval $D_{ST}T_s \le t \le T_s$ have been shown in Fig. 13.

Table 6. The selected values and parameters in non-ideal proposed topology

Parameter/Component	Value
Input voltage (V_i)	$64V$
Fundamental frequency (f_o)	$50\,Hz$
Switching frequency (f_s)	$5\,kHz$
Shoot-through duty cycle (D_{ST})	0.3
Modulation index (M)	0.5
Inductor (L)	$5\,mH$
r_L	$0.5\,\Omega$
V_D	$0.7V$
R_D	$0.3\,\Omega$
V_T	$0.6V$
R_T	$0.2\,\Omega$
Capacitor (C)	$470\,\mu F$
r_C	$0.4\,\Omega$
Inductance of output filter (L_f)	$4.6\,mH$
Capacitor of output voltage (C_f)	$10\,\mu F$
Load resistance (R_L)	$25\,\Omega$
$t_{on}+t_{off}$	$1\,\mu s$
n	2

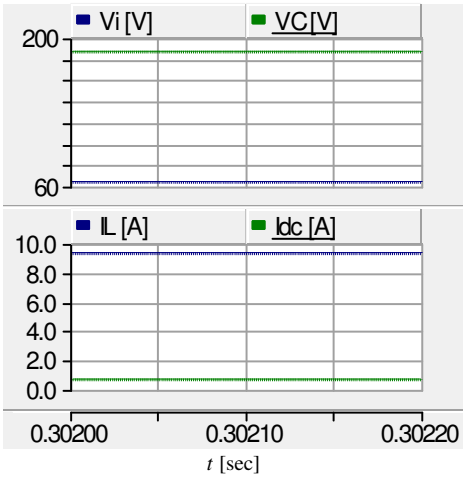


Fig. 13. The important waveforms in the time interval $D_{ST}T_s \le t \le T_s$

According to Fig. 13, the average values of capacitor voltage, inductor current and inverter input current is obtained 186V, 9.35A, respectively, and I_{dc}=0.66A. Under these conditions, the switching power losses are calculated as follows:

$$
\begin{aligned}
{}_{m-off} &= \frac{(t_{on}+t_{off})}{6T_s}(E_{on-off,S}+E_{on-off,Da} \\
&+E_{on-off,Db}+E_{on-off,DG1}+E_{on-off,DG2}) \\
&=6.135\,W
\end{aligned}
\tag{136}
$$

In order to determine the amount of switching power losses, the proposed topology can be simulated in non-load condition. Figure 14 shows the power losses of switches and diodes in non-load condition. It is important to note that the value obtained from Fig. 14 is very close to the calculated value from Eq. (136). Using Table 6 and relations of Eq. (59), (70), (79), (85), (87), (97), and (107), the conduction power losses of all elements in the proposed topology can be calculated as follows:

$$
\begin{aligned}
P_{C-loss} &= P_{C,S}+P_{C,Da1}+P_{C,Da2}+P_{rC} \\
&+P_{rL}+P_{C,G1}+P_{C,G2}=260.6W
\end{aligned}
\tag{137}
$$

Fig. 15 shows the conduction power losses values.

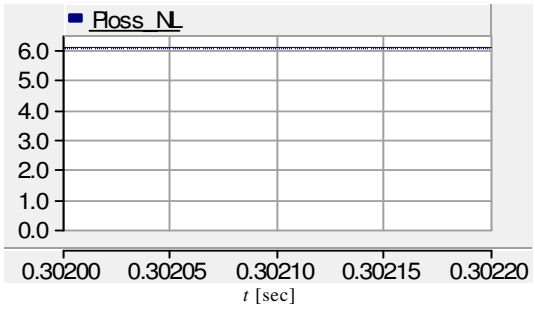


Fig. 14. The power losses of switches and diodes in non-load condition (Switching losses)

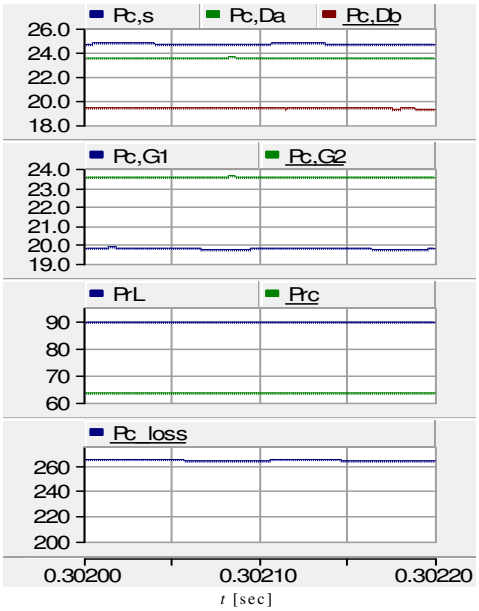


Fig. 15. Conduction power losses of elements

8.CONCLUSIONS

In this paper, a new boost Z-source inverter based on switches-inductor cell is proposed. In this topology, different operating modes are investigated and the waveforms of input and output parameters are also obtained. In addition to increase voltage gain, the developed topology of the proposed inverter is introduced. Then, the operation of the inverter in boundary condition is investigated and the value of critical inductance is also calculted. The proposed inverter is also compared with the conventional Z-source and boost Z-source inverters. The proposed inverter is able to generate a higher voltage gain by using a lower value of duty cycle in comparison with the other Z-source inverters.

For instance, based on the value of D_{ST}=0.3, the boost factor for the convnetionl Z-source inverter, switched boost inverter and the proposed inverter areB_{ZSI}=1.67, B_{SBI}=1.16, and$P_{roposed}$=1.16, respectively. The correct performance of the obtained analysis are reconfirmed by using EMTDC/PSCAD simulation results.

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