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Reduction the Number of Power Electronic Devices of a Cascaded Multilevel Inverter Based on New General Topology

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ABSTRACT
In this paper, a new cascaded multilevel inverter by capability of increasing the number of output voltage levels with reduced number of power switches is proposed. The proposed topology consists of series connection of a number of proposed basic multilevel units. In order to generate all voltage levels at the output, five different algorithms are proposed to determine the magnitude of DC voltage sources. Reduction of the used power switches and the variety of DC voltage sources magnitudes are two main advantages of the proposed topology. These results are obtained by comparison of the proposed inverter with the H-bridge cascaded multilevel inverter and one of recently presented topologies. The remarkable ability of the proposed topology with its algorithms in generating all voltage levels (even and odd) is verified through PSCAD/EMTDC simulation and experimental results of a 17-level inverter.

KEYWORDS: Multilevel inverters, Conventional cascaded multilevel inverter, Bidirectional switches.

1. INTRODUCTION

Recently, the multilevel inverters have received more and more attention in researches because of their capabilities in high power and medium voltage applications. High efficiency, high power quality, lower order harmonics, better electromagnetic interference, lower dv/dt stress on switches, and lower switching losses are some of the advantages of the multilevel inverters [1-7]. There are three main topologies for multilevel inverters: diode clamp multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter [2-4]. The cascaded multilevel inverters have received special attention due to the modularity and simplicity of the control. In addition, the ability of the cascaded inverters in generating higher number of levels with minimum number of semiconductor devices in comparison with other main topologies increases the trend to these types of inverters. In this inverter, the desired AC output waveform is synthesized from several steps of DC source as inputs [6-8]. The cascaded multilevel inverters are mainly classified into two groups: symmetric; with the equal magnitude of dc voltage source and asymmetric with different values of DC voltage sources, which leads to increasing the number of output voltage levels [8-10].

Up to now, different cascaded topologies have been presented in literatures. In [10-11], two different topologies for cascaded multilevel inverters have been presented that are known as symmetric ones. It has been also presented H-bridge cascaded multilevel inverter in [12]. Here, two different algorithms to determine the values of DC voltage sources have been represented that are known as symmetric and asymmetric ones. These symmetric topologies have the minimum variance of the value of the DC voltage sources that is the most important advantage of them. While, the higher number of switches and insulated gate bipolar transistors (IGBTs) are required for generation specific output voltage levels because of the low amplitude of the used DC voltage sources.

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Moreover, each switch requires a driver circuit. As a result, increasing in the installation space and total cost of the symmetric inverters are the most important disadvantages of them. Therefore, different asymmetric cascaded multilevel inverters have been suggested in [14-15]. In addition, different asymmetric H-bridge cascaded multilevel inverters have been also reported in [8-9] and [13]. The remarkable advantage of these topologies is the high number of generated output voltage levels with minimum number of used power electronic devices, but the high variety of the value of the DC voltage sources is their main disadvantage.

Although, all of the presented topologies in the literatures have their own advantages and disadvantages, but in this paper, a cascaded multilevel inverter based on the new basic unit is proposed. This inverter increases the number of output voltage level by using minimum number of power switches, driver circuit and IGBTs and less variety of the value of the DC voltage sources. Then, five different algorithms for generating all voltage levels are presented. In addition, the proposed topology with its algorithms is compared with the H-bridge cascaded multilevel inverter and the presented topology in [15] to investigate advantages of the proposed topology. Finally, the obtained results of PSCAD/EMTDC simulation and experimental prototype on a 17-level inverter reconfirm the correct performance of the proposed topology in generating all voltage levels.

2. PROPOSED TOPOLOGY

The basic multilevel unit is shown in Fig. 1. As Fig. 1 shows, the proposed basic unit consists of two DC voltage sources, one bidirectional switch (S_2) and two unidirectional ones (S_1 and S_3). It is important to note that each unidirectional switch consists of an IGBT with an anti-parallel diode and a driver circuit, however, the bidirectional ones include of two IGBTs with two anti-parallel diodes and a driver circuit if the switch with common emitter configuration is used. Therefore, the number of driver circuit for the bidirectional switches is as same as unidirectional ones in the proposed basic unit. The proposed basic unit is able to generate three voltage levels of V_1, 0 and V_1+V_2 at the output. According to Fig. 1, the switches (S_1, S_2) or (S_1, S_3) or (S_2, S_3) or (S_1, S_2, S_3) can't be turned on simultaneously, because a short circuit across the DC voltage sources would be produced. Table 1 shows the output voltage levels of the proposed basic unit based on different switching patterns. In this Table, 1 and 0 indicate the on and off states of the switches, respectively. It is obvious from Table 1 that the proposed unit is only able to generate positive levels at the output.

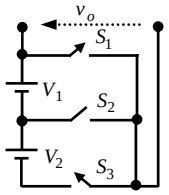

Fig.1. The proposed basic unit.

Table 1. The output voltageof the proposed basic unit based on different switching pattern.

State	S_1	S_2	S_3	v_o
1	0	1	0	V_1
2	0	0	1	V_1+V_2
3	1	0	0	0

A new cascaded multilevel inverter could be made by series connection of the n number of the basic unit shown in Fig. 1. This new proposed cascaded multilevel inverter is shown in Fig. 2. The output voltage of the proposed inverter is equal to adding the output voltage of each unit and can be written as follows:

$$v_o(t)=v_{o,1}(t)+v_{o,2}(t)+\cdots+v_{o,n}(t) \quad (1)$$

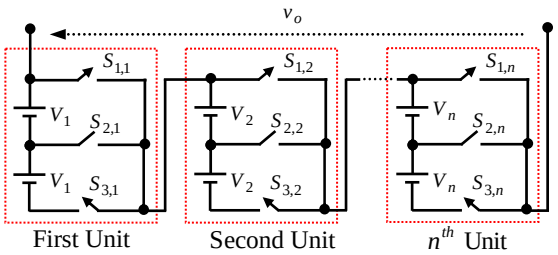

Fig. 2. Series connection of n number of basic unit.

As mentioned before, this inverter is only able to generate positive levels at the output so in order to generate all voltage levels (positive and negative), it is required to use of the H-bridge at the output. The completed cascaded multilevel inverter is shown in Fig. 3. As this figure indicates, T_1 to T_4 are the

unidirectional switches. The output voltage level will be positive and negative, if the switches T_1, T_2 and T_3, T_4 are turned on, respectively. In addition, by turning on the switches T_1 and T_3 or T_2 and T_4 the output voltage will be zero.

It is pointed out that the value of blocked voltage of power switches in each basic unit of the proposed topology is low that leads to use of power switches with low nominal voltage range. This is one of the main advantages of the proposed inverter. However, the used power switches in H-bridge, examine high value of blocked voltage because of cascading several basic units. This is the main disadvantage of the proposed inverter.

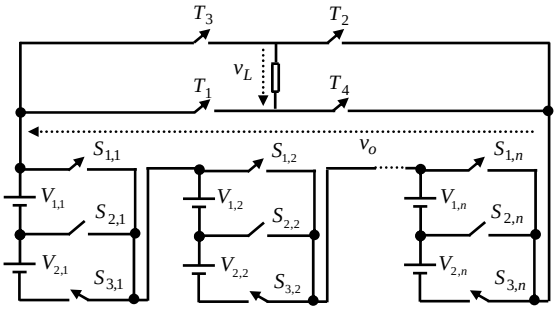

Fig. 3. The proposed cascaded multilevel inverter.

In the proposed cascaded multilevel inverter, the number of switches (N_{switch}), IGBTs (N_{IGBT}), driver circuits (N_{driver}) and dc voltage sources (N_{source}) are calculated as follows:

$$N_{switch} = 3n + 4 \quad (2)$$

$$N_{IGBT} = 4n + 4 \quad (3)$$

$$N_{driver} = 3n + 4 \quad (4)$$

$$N_{source} = 2n \quad (5)$$

At the following sub-sections in order to generate all voltage levels at the output, five different algorithms are proposed to determine the magnitude of the DC voltage sources.

2.1. First proposed algorithm (P_1)

In this sub-section, the amplitude of the DC voltage sources of the basic unit shown in Fig. 3 is considered as follows:

$$V_{1,j} = V_{2,j} = V_{dc} \qquad for \quad j = 1, 2, \cdots, n \quad (6)$$

This inverter is known as symmetric cascaded multilevel inverter. In this algorithm, the number of output voltage levels (N_{level}) and the maximum amplitude of the producible output voltage ($V_{o,\max}$) are respectively equal to:

$$N_{level} = 4n + 1 \quad (7)$$

$$V_{o,\max} = \sum_{j=1}^{n} V_j = (2n)\, V_{dc} \quad (8)$$

Although the number of used power electronic devices such as the number of the power switches, IGBTs and driver circuit have significant influence on the installation space and total cost of the inverter, but the variety of the magnitude of DC voltage sources is another important feature in determining this index. By reducing the variety of the value of the DC voltage sources, the total cost of the inverter decreases. Therefore, the variety of the values of the DC voltage sources ($N_{variety}$) in the proposed algorithm is calculated as follows:

$$N_{variety} = 1 \quad (9)$$

Considering (8), the low variety of the amount of the DC voltage sources is an advantage for the proposed algorithm.

2.2. Second proposed algorithm (P_2)

In the second proposed algorithm, the magnitudes of the DC voltage sources are determined as follows:

$$V_{1,1} = V_{2,1} = V_{dc} \quad (10)$$

$$V_{1,j} = V_{2,j} = 2V_{dc} \qquad for \quad j = 2, 3, \cdots, n \quad (11)$$

Considering this proposed algorithm, the number of output voltage levels, the maximum magnitude of the output voltage and the variety of the values of DC voltage sources are calculated as follows:

$$N_{level} = 8n - 3 \quad (12)$$

$$V_{o,\max} = (4n - 2)\, V_{dc} \quad (13)$$

$$N_{variety} = 2 \quad (14)$$

2.3. Third proposed algorithm (P_3)

In this sub-section, the values of the DC voltage sources are selected by below equations:

$$V_{1,1} = V_{2,1} = V_{dc} \quad (15)$$

$$V_{1,j} = V_{2,j} = 3V_{dc} \qquad for \quad j = 2, 3, \cdots, n \quad (16)$$

In this condition, the number of output voltage levels, the maximum magnitude of the output voltage and the variety of the values of DC voltage sources are written as follows:

$$N_{level} = 12n - 7 \quad (17)$$

$$N_{variety} = 2 \quad (18)$$

$$V_{o,\max} = (6n-4)\,V_{dc} \quad (19)$$

2.4. Fourth proposed algorithm (P_4)

In the fourth proposed algorithm, the magnitudes of the DC voltage sources of the proposed cascaded topology are selected as follows:

$$V_{1,1} = V_{2,1} = V_{dc} \quad (20)$$

$$V_{1,j} = V_{2,j} = 2^{j-1}V_{dc} \qquad for \quad j = 2, 3, \cdots, n \quad (21)$$

In the proposed algorithm, the number of output voltage levels, the maximum magnitude of the output voltage and the variety of the values of DC voltage sources are equal to:

$$N_{level} = 2^{n+2} - 3 \quad (22)$$

$$V_{o,\max} = (2^{n+1} - 2)\,V_{dc} \quad (23)$$

$$N_{variety} = n \quad (24)$$

2.5. Fifth proposed algorithm (P_5)

In this sub-section, the values of the DC voltage sources in the proposed cascaded multilevel inverter are written as follows:

$$V_{1,1} = V_{2,1} = V_{dc} \quad (25)$$

$$V_{1,j} = V_{2,j} = 3^{j-1}V_{dc} \qquad for \quad j = 2, 3, \cdots, n \quad (26)$$

Considering the fifth proposed algorithm, the number of output voltage levels, the maximum magnitude of the output voltage and the variety of the values of DC voltage sources are calculated as follows:

$$N_{level} = 2 \times 3^n - 1 \quad (27)$$

$$V_{o,\max} = (3^n - 1)\,V_{dc} \quad (28)$$

$$N_{variety} = n \quad (29)$$

3. COMPARING THE PROPOSED TOPOLOGY WITH THE CONVENTIONAL TOPOLOGIES

The most important aim of introducing the new cascaded multilevel inverter and its proposed algorithms is increasing the number of output voltage levels by using less number of power electronic devices such as switches, IGBTs, driver circuits and so on. In this section, the proposed cascaded multilevel inverter with its presented algorithms is compared with H-bridge multilevel inverter from the number of used power electronic devices point of view. This investigation is done to determine the advantages and disadvantages of the proposed topology.

The proposed topology and its algorithms considered as $P_1 - P_5$ in this investigation. In [12], the H-bridge cascaded multilevel inverter and two different algorithms have been presented. One of the represented algorithms in [12] cause the symmetric cascaded inverter and another presented algorithm leads to asymmetric one. In this comparison, these two different algorithms are considered as R_1 and R_2, respectively. Then, in order to increase the number of output voltage levels in the H-bridge cascaded multilevel inverter, another algorithm based on ternary method has been presented in [13]. This algorithm is considered by R_3 in this investigation. The main advantage of the presented algorithm in [13] is increasing the output voltage levels with minimum number of used H-bridges. However, the high variety of the value of DC voltage source for the presented algorithm in [13] leads to the introduction of two other algorithms in the literatures. These algorithms have been presented in [8-9] and are considered by $R_4 - R_5$ in this comparison. Moreover, the presented topology in [15] is considered by R_6. Figure 4 indicates the H-bridge cascaded multilevel inverter.

Figure 5 shows the comparison of the proposed topology and its algorithms with the H-bridge cascaded multilevel inverter with its different algorithms and the presented topology in [15] from the number of switches point of view. As shown in this figure, the number of required switch for the fifth proposed algorithm is lower than the number of switches in other presented algorithm in the literature. In addition, this algorithm has even better performance than other presented algorithms for the proposed topology.

As mentioned before, the number of switches in the proposed cascaded multilevel inverter is as same as the number of driver circuits in the proposed topology. As a result, this topology needs a less number of driver circuits than other presented algorithms in literature.

Because of using bidirectional switches in the proposed topology, which consist of two IGBT with two anti-parallel diodes, it is necessary to compare the number of required IGBTs in this topology with the H-bridge cascaded multilevel inverter and the presented topology in [15]. This comparison is shown in Fig. 6. As Fig. 6 shows, the proposed cascaded topology uses a lower number of IGBTs than other topologies except the algorithm that is indicated by R_3. From the viewpoint of required IGBTs number, the fifth proposed algorithm has also best performance between other proposed algorithms. Moreover, the number of diodes in the proposed inverter is lower than H-bridge cascaded inverter and the presented algorithm in [15]. The minimum number of required IGBTs, diodes and driver circuit in the proposed topology cause the reduction in the required installation space and total cost of the system.

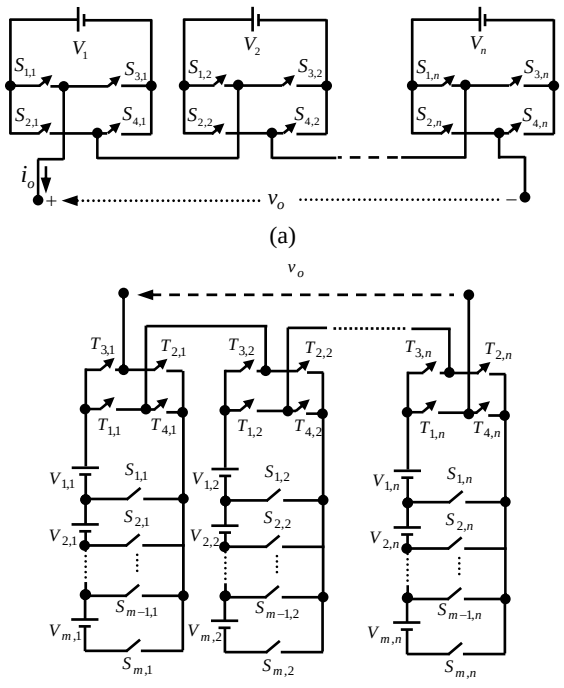

Fig. 4. The conventional cascaded multilevel inverter;(a) H-bridge cascaded inverter R_1 for $V_1 = V_2 = V_3 = \cdots = V_n = V_{dc}$, R_2 for $V_1 = V_{dc}$,$V_2 = 2V_{dc} \cdots$, $V_n = 2^{n-1}V_{dc}$, R_3 for $V_1 = V_{dc}$, $V_2 = 3V_{dc}$, $\cdots$,$V_n = 3^{n-1}V_{dc}$, R_4 for $V_1 = V_{dc}$, $V_2 = V_3 = \cdots = V_n = 2V_{dc}$, R_5 for $V_1 = V_{dc}$, $V_2 = V_3 = \cdots = V_n = 3V_{dc}$; (b) presented topology in [15].

Figure 7 compares the number of DC voltage sources in the proposed topology with the H-bridge cascaded multilevel inverter and the presented topology in [15]. As it is obvious, the number of used DC voltage sources in the proposed topology especially, by using the fifth algorithm, is less than other proposed algorithms and presented algorithms for the H-bridge cascaded inverter. However, this index in R_2 and R_3 is less than other proposed algorithms. This result is obtained from the differences between the topology of basic unit of the proposed cascaded inverter with the H-bridge cascaded inverter and the presented topology in [15]. In other word, there are two DC voltage sources in the proposed basic unit while one DC voltage source is required in each unit of the H-bridge cascaded inverter. However, this feature is considered as the main disadvantage of the proposed multilevel inverter, but because of increasing interest in using renewable energy sources such as solar cells, wind power and so on, this disadvantage could be easily eliminated.

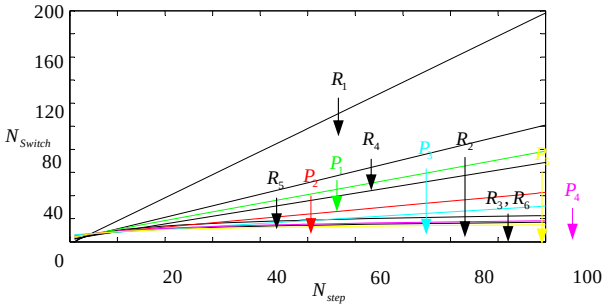

Fig. 5. Variation of N_{switch} versus N_{level}.

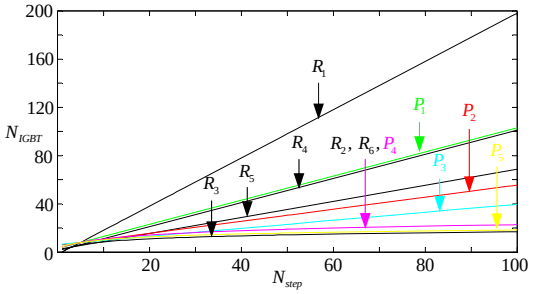

Fig. 6. Variation of N_{IGBT} versus N_{level}.

The variety of the value of the used DC voltage sources in the proposed topology with the H-bridge cascaded multilevel inverter and the presented topology in [15] is shown in Fig. 8. As Fig. 8 shows, this index in the proposed cascaded inverter is

lowerthan other presented topologies in the literature. In addition, it is important to note that the fifth algorithm has also the best performance from this point of view in comparison with other proposed algorithms.

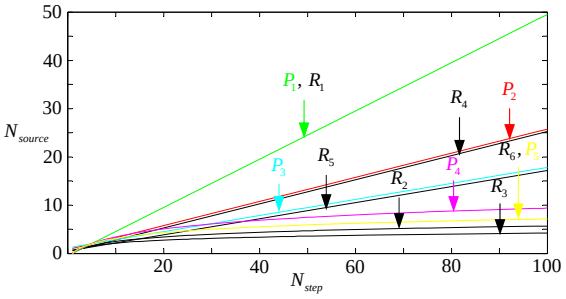

Fig. 7. Variation of N_{source} versus N_{level} .

Therefore, it is possible to consider that the proposed cascaded multilevel inverter with its new presented algorithms has better performance in comparison with the H-bridge cascaded multilevel inverter from the number of switches, driver circuits, IGBTs and diodes and the variety of the value of the DC voltage sources points of view. However, the number of required DC voltage source could be considered as the most important disadvantage of the proposed topology. This disadvantage is eliminated by using renewable energy sources.

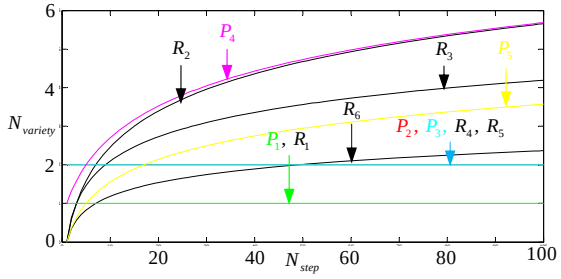

Fig. 8. Variationof $N_{variety}$ versus N_{level} .

4. SIMULATION AND EXPERIMENTAL RESULTS

The suitable performance of the proposed cascaded multilevel inverter in generating all voltage levels at the output is verified through simulation and experimental results. The simulation results are obtained by using EMTDC/PSCAD software program and the experimental results are obtained by using a laboratory prototype. These results are obtained from a 17-level inverter based on the proposed basic unit that is shown in Fig. 3. The proposed 17-level inverter is shown in Fig. 9. As it is obvious from Fig. 9, this inverter consists of two basic units, which are connected in series and the magnitude of its DC voltage sources are determined by using fifth proposed algorithms. Therefore, based on (25) and (26), the values of the used DC voltage sources are considered $V_{1,1}=V_{2,1}=25V$ and $V_{1,2}=V_{2,2}=75V$ in the first and the second unit, respectively. According to (27) and (28) this inverter is able to generate 17 levels (eight positive levels, eight negative levels and one zero level) with the maximum amplitude of 200 V at the output. It is important to note that the IGBTs used on the prototype are HGTP10N40CID (with an internal anti-parallel diode). The 89C52 microcontroller by ATMEL company has been used to generate all switching pattern. The load connected to the inverter is considered a resistive-inductive load with the values of $R=100\,\Omega$ and $L=55\,mH$. Moreover, the fundamental frequency control method is used in this inverter. This selection is based on low switching losses in comparison with the other control methods. This feature is because of low switching frequency in this control method.

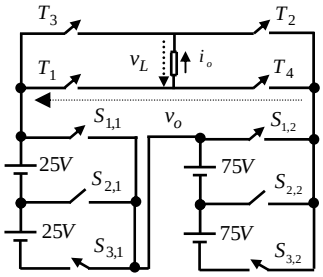

Fig. 9. The proposed cascaded 17-level inverter.

Figures 10(a) and 10(b) show the simulation and experimental output voltage waveforms (v_o) of the proposed topology, respectively. As it is obvious from Fig. 10(a), this inverter is only able to generate positive level at the output. Therefore, eight steps with the maximum amplitude of 200 V is generated at the output. In addition, Fig. 10(b) reconfirm the obtained results from simulation result. In order to have all voltage levels (positive and negative) at the output, the H-bridge is added to the proposed inverter. Figure 11 indicates the simulation and experimental current and voltage waveforms of the load, respectively. As shown in Fig. 11(a), this

inverter generates a step 17-level waveform the same as sinusoidal one with the maximum amplitude of 200 V and 1.96 A on the load, respectively. Moreover, comparing the voltage waveform with current waveform shows that the current waveform is closer to ideal sinusoidal one in addition to the existence of a phase shift between voltage and current waveforms. These features are due to resistive-inductive load feature, which behaves as a low-pass filter. The experimental results of current and voltage waveforms that is shown in Fig. 11(b) reconfirms the obtained results from simulation ones.

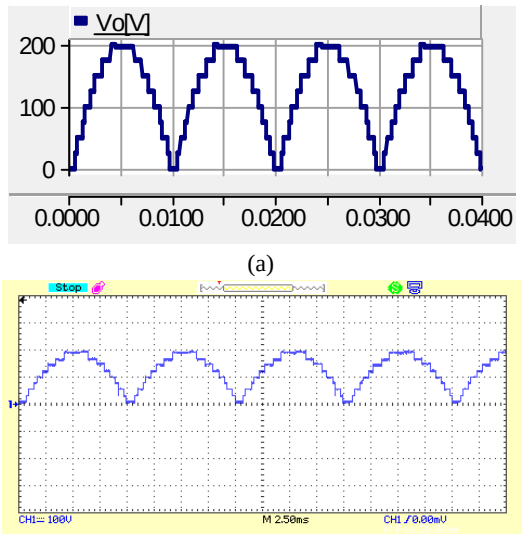

Fig. 10. The output voltage of the proposed inverter; (a) simulation result; (b) experimental result.

As mentioned before, this inverter consists of one bidirectional switch and two unidirectional ones from voltage point of view. In other word, although both of them conduct current in two directions, but the unidirectional switches block voltage in one direction while bidirectional one can block voltage in two directions. In order to investigate these facts, the voltage on switches of the first basic unit of the proposed cascaded inverter are shown in Fig. 12. Figure 12(a) and Fig. 12(e) show the voltage on switches $S_{1,1}$ and $S_{3,1}$ based on simulation results, respectively. As shown in these figures, the magnitudes of the blocked voltage on switches are either positive or zero, so there is not any negative amount on them. In addition, the amount of blocked voltage is equal to adding the magnitude of the used DC voltage sources in first basic unit. As a result, the existence of two unidirectional switches is reconfirmed in the proposed cascaded multilevel inverter. Figure 12(b) and Fig. 12(f) are obtained from experimental prototype. These figures also reconfirm the existence of two unidirectional power switches in the proposed topology. Fig. 12(c) indicates the blocked voltage on the switch $S_{2,1}$ is based on simulation results. As shown in this figure, there are positive and negative amount of voltages on it. This fact verifies that the switch $S_{2,1}$ is a bidirectional one. Fig. 12(d) is obtained from experimental prototype. This figure also reconfirms the existence of a unidirectional power switch in the proposed topology.

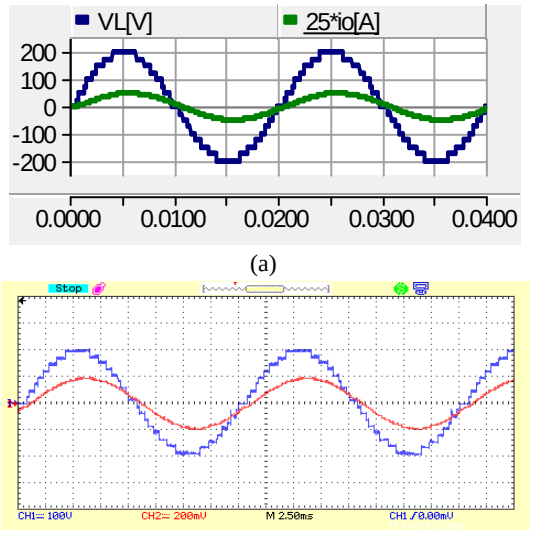

Fig. 11. Current and voltage waveforms of the load in the 17-level proposed inverter; (a) simulation result; (b) experimental result.

{R} In addition, the simulation results of the proposed topology in steady state operation by considering the load as high inductive one with the value of $L = 55\,mH$ are obtained. Figure 13 shows the simulation output voltage waveforms (v_o) of the proposed topology. As it is obvious from Fig. 13, this inverter is only able to generate positive level at the output. Therefore, eight steps with the maximum amplitude of 200 V is generated at the output. Fig. 14 indicates the simulation of current and voltage waveforms of the load. As shown in Fig. 14, this inverter generates a step 17-level waveform same as

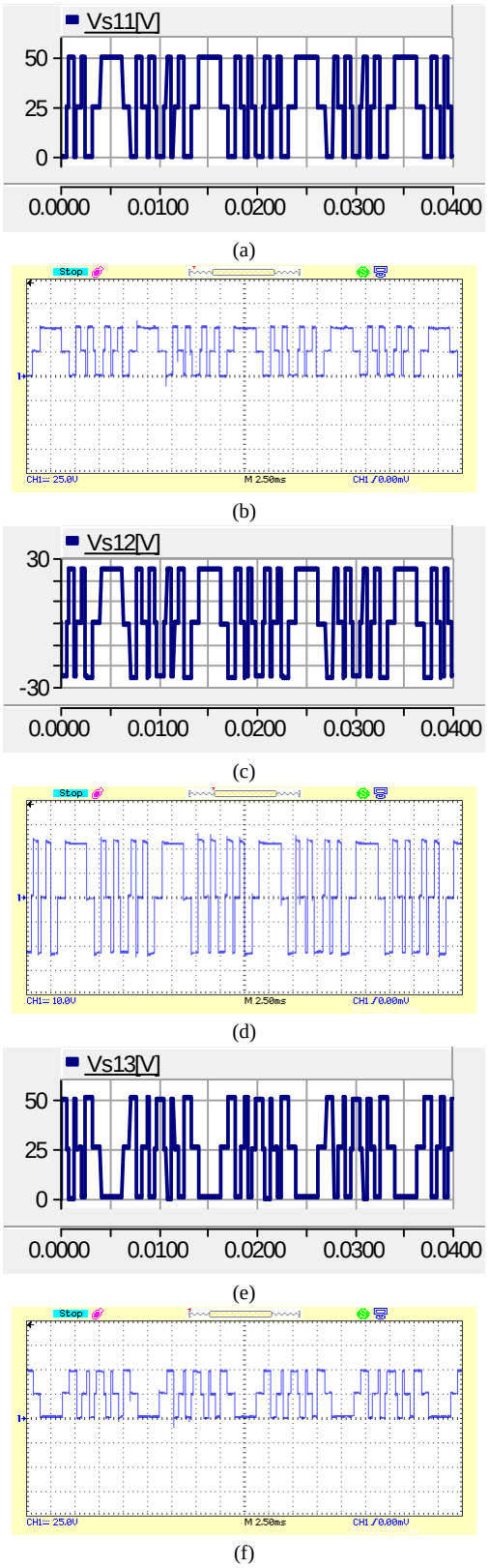

Fig. 12. The simulation results of the blocked voltage on the power switches in the first basic unit; (a) simulation result for $S_{1,1}$; (b) experimental result for $S_{1,1}$; (c) simulation result for $S_{2,1}$; (d) experimental result for $S_{2,1}$; (e) simulation result for $S_{3,1}$;(f) experimental result for $S_{3,1}$

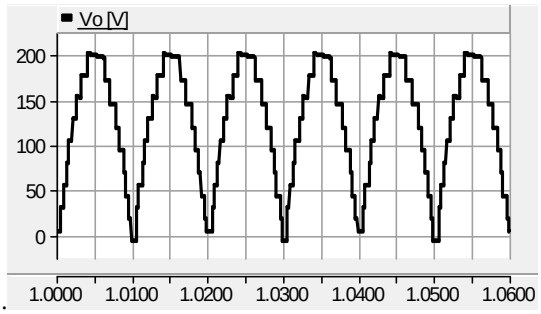

Fig. 13. The simulation output voltage of the proposed inverter.

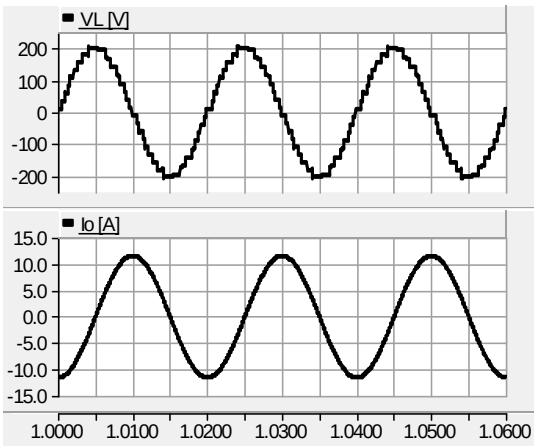

Fig. 14. Simulation result of current and voltage waveforms of the load in the 17-level proposed inverter.

sinusoidal one with the maximum amplitude of 200 V and 11.5 A on the load, respectively. Moreover, comparing the voltage and current waveforms shows that there is 90° a phase difference between voltage and current waveforms. As shown in these figures, the proposed inverter can operate correctly in high inductive loads.

Figure 15(a) and Fig. 15(c) show the voltage on switches $S_{1,1}$ and $S_{3,1}$ based on simulation results, respectively. As shown in these figures, the magnitudes of the blocked voltage on switches are equal to 0, 25 V and 50 V, so there isn't any negative amount on them. In addition, the amount of blocked voltage is equal to adding the magnitude of the used DC voltage sources in first basic unit. As a result, the existence of two unidirectional switches is reconfirmed in the proposed cascaded multilevel inverter. Figure 15(c) indicates the blocked voltage on the switch $S_{2,1}$ based on simulation results. As shown in this figure, there is the voltage from $-30V$ to $30V$ on it. Therefore, there are positive and

negative amount of voltages on it. This fact verifies that the switch $S_{2,1}$ is a bidirectional one.

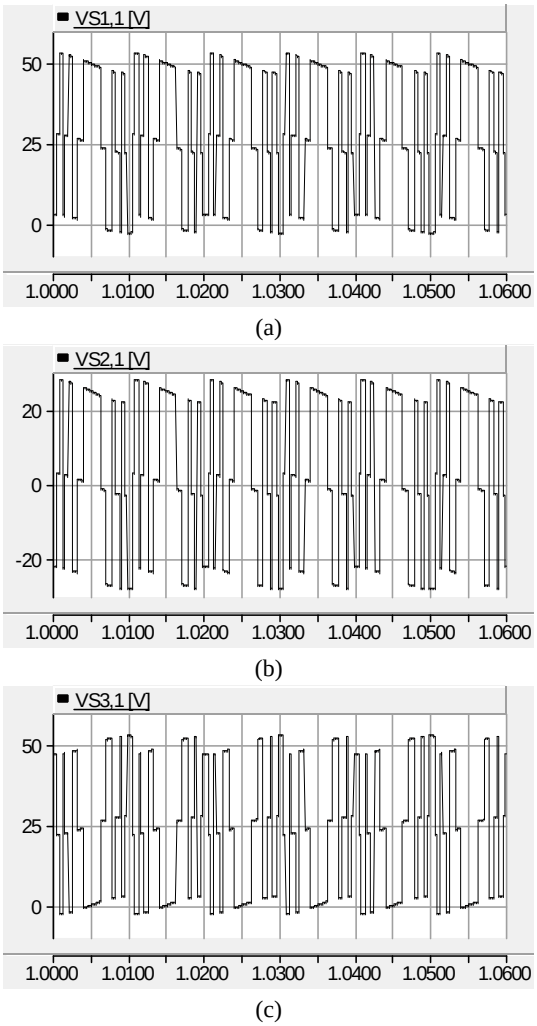

Fig. 15. The simulation results of the blocked voltage on the power switches in the first basic unit; (a) $S_{1,1}$; (b) $S_{2,1}$; (c) $S_{3,1}$.

5. CONCLUSION

In this paper, a cascaded multilevel inverter based on a new basic unit is proposed. The proposed unit is only able to generate positive levels at the output. Therefore, in order to generate all voltage levels (positive and negative) the H-bridge is added to the proposed topology. Then, fifth different algorithms to determine the magnitude of DC voltage sources are presented. Moreover, a comparison between the proposed topology with the H-bridge cascaded multilevel inverter and the presented inverter in [15] are done from the number of power electronic devices point of view. The most significant advantages of the proposed topology are that the number of switches, driver circuits and IGBTs and the variety of the value of the DC voltage sources are lower than the H-bridge cascaded inverter. These features cause to reduce the installation space and total cost of the inverter. For instance, to generate 161 levels at the output, the proposed cascaded multilevel inverter based on the fifth proposed algorithm needs an inverter with four numbers of basic topologies, $N_{switch}=16$, $N_{IGBT}=20$, $N_{driver}=16$ and $N_{variety}=4$. This selection is based on the best performance in comparisons with other proposed algorithms. However, in order to generate the same steps at the output in the H-bridge cascaded inverter, based on the presented algorithm in [13] it is required five numbers of the H-bridges, $N_{switch}=N_{IGBT}=N_{Driver}=20$ and $N_{variety}=5$ whereas based on the presented algorithm in [12] it is needed eight numbers of the H-bridges, $N_{switch}=N_{IGBT}=N_{Driver}=32$ and $N_{variety}=8$. These algorithms are shown by R_3 and R_2 in comparisons and have the best performance between all of the presented algorithms for H-bridge cascaded inverters. As it is obvious, the proposed inverter needs less number of power electronic devices. The main disadvantage of the proposed cascaded inverter is the high number of required DC voltage sources. For instance, to generate 161 levels at the output the proposed inverter needs $N_{source}=8$ while the presented algorithm for the H-bridge inverter as R_3 requires $N_{source}=5$. Moreover, it is suggested to use renewable energy sources as necessity dc voltage sources in the proposed topology to overcome this problem. Finally, the simulation and experimental results reconfirm the capability of the proposed cascaded inverter in generating all voltage levels through a 17-level inverter.

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