



A non-linear analytic stress model for the analysis on the stress interaction between TSVs

Ming-Han Liao*, Ssu-Chieh Kao, and Sung-Jie Huang

Department of Mechanical Engineering, National Taiwan University, Taipei, Taiwan.

(Received 7 October 2013; Accepted 19 June 2014; Published on line 1 June 2015)

* Corresponding author email: mhliao@ntu.edu.tw

DOI: [10.5875/ausmt.v5i2.323](https://doi.org/10.5875/ausmt.v5i2.323)

Abstract: Thermo-elastic strain is induced by through silicon vias (TSV) due to the difference of thermal expansion coefficients between the copper (~ 18 ppm/ $^{\circ}\text{C}$) and silicon (~ 2.8 ppm/ $^{\circ}\text{C}$) when the structure is exposed to a thermal budget in the three dimensional integrated circuit (3DIC) process. These thermal expansion stresses are high enough to induce the delamination on the interfaces between the copper, silicon, and isolated dielectric. A compact analytic model for the strain field induced by different layouts of thermal copper filled TSVs with the linear superposition principle is found to result in large errors due to the strong stress interaction between TSVs. In this work, a nonlinear stress analytic model with different TSV layouts is demonstrated by the finite element method and Mohr's circle analysis. The stress characteristics are also measured by the atomic force microscope-raman technique at a nanometer level resolution. This nonlinear stress model for the strong interactions between TSVs results in an electron mobility change ~ 2 -6% smaller than that resulting from a model that only considers the linear stress superposition principle.

Keywords: Nonlinear analytic modeling; strain field; through silicon via (TSV)

Introduction

Device scaling beyond the 22-nm node encounters physical constraints and technological challenges. Three dimensional integrated circuits (3DICs) [1-4] can increase device density along the third dimension, whereas conventional devices scaling is restricted. The stacking of ICs with through silicon vias (TSVs) is a crucial technique for vertical interconnections, resulting in enhanced circuit performance and reduced system size. Since the filling materials of TSVs and silicon have different thermal expansion (CTE) coefficients, cooling from the process temperature to the device operation temperature leads to the development of a strain field around the TSVs. The thermo-elastic strains introduced by TSVs in the active area [5, 6] can affect the carrier mobility [7, 8]. Some previous studies have also shown that an appropriate strain field can further enhance device performance, whereas a keep-out zone [1, 4] should be identified in advance to minimize device performance variability. Therefore, the strain effect induced by TSVs should be

formulated and taken into consideration for chip design. Analytic modeling is of particular importance to provide a detailed understanding of the strain distribution for these 3DICs structures. To analytically resolve the strain field distribution problem, Pan [9] used an isotropic two-dimension Lamé solution and the linear superposition principle without considering the stress interaction between TSVs. This approach resulted in a larger error in the TSV vicinity with a specific circuit layout. This work uses the finite element method (FEM) and Mohr's circle analysis to demonstrate a nonlinear stress analytic model for different TSV layouts. The corresponding stress characteristics are also measured by the atomic force microscope (AFM)-raman technique with nanometer level resolution. Experimental results show that the nonlinear stress analytic model provides better accuracy near the vicinity of TSV.

Experiment

Our previous work used the 325 nm light of an argon laser is used for polarized AFM-raman experiments



[10, 11]. This light is focused through a microscope on the sample. Lasers are linearly polarized along the x direction and the spectrometer has a strong polarization dependence. As a result, the polarized laser light scans across the TSV structure and the active region can be achieved in the backscattering mode. The sample is mounted on an automated XY stage under the microscope such that raman spectra can be recorded at different positions along the line on the sample.

The FEM is used with a proprietary version of the ANSYS and FLOOPS software [8]. To assess stress behavior, a displacement boundary condition equal to the burgers vector is introduced between nodes at the dislocation cores. The stress fields from the stress simulation are mapped onto the build structure in the electrical simulation tool. All simulated drive current differences in this work are due to the stress. Stress impact on device mobility is captured using a model of related strained Si theory [12, 13].

Results and Discussions

We investigate the characteristics of stress to determine whether it follows the linear superposition principle among different TSV layouts, the 2-D stress contour for two different TSV layouts. Figures 1(a) and (b) respectively illustrate the parallel and perpendicular layouts. The diameter of the TSVs is 10 μm . The pitch between the two TSVs is 15 μm . The TSVs are placed on a 50 x 50 μm silicon base as shown in the figure. The device (observation point) is denoted by the red square. For the parallel layout, we define a symmetry boundary condition along the y=0 line and the expansion in other directions is unbounded. For the perpendicular layout, we define a symmetry boundary condition along the x=0 line and the expansion in other directions is unbounded. The Cu of the TSVs is cooled from 400 $^{\circ}\text{C}$ to an ambient temperature of 25 $^{\circ}\text{C}$. Figures 1(a) and (b) respectively show the two dimensional simulated stress contour on the parallel and perpendicular TSV layouts. Cases A and B consider the effect of the two TSVs individually, and Case C shows the effect of both TSVs simultaneously. The thermo-elastic strain in the TSV is induced by the difference of CTEs between the copper (~18 ppm/ $^{\circ}\text{C}$) and silicon (~2.8 ppm/ $^{\circ}\text{C}$) when the structure is exposed to a thermal budget in the 3DIC process. When the distance of two TSVs is close to ~ 15 μm , the strong stress interactions between TSVs is observed by the

AFM-Raman spectra shown in Fig. 2. The Raman shift extends from 520 cm^{-1} to 516.6 cm^{-1} in the parallel TSVs layout (Fig.1(a)) resulting in a strong nonlinear stress effect. With the observation of the stress distribution on the parallel TSV layout and the perpendicular TSV layout shown in the Figs. 3(a) and (b), the stress for when the two TSVs are considered simultaneously is clearly less than the direct sum of the stresses induced by the two TSVs considered individually (i.e, the stress of Case C does not equal the sum of Case A and Case B). This indicates that the linear superposition principle cannot be directly used to analyze the stress in 3DIC when the two close TSVs have the strong stress interactions. In this work, a nonlinear stress analytic model with different TSV layouts is demonstrated using FEM and Mohr's circle analysis.

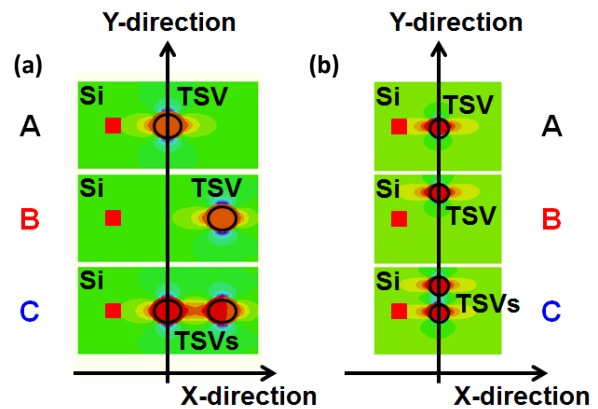


Fig. 1. Two dimensional simulated stress contour among different TSV layouts, including the parallel layout shown in Fig. 1(a) and perpendicular layout shown in Fig. 1(b).

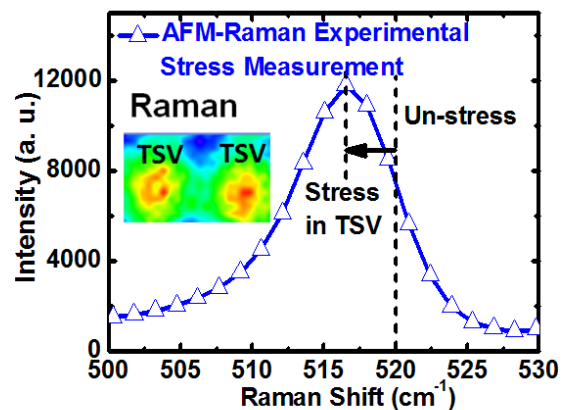


Fig. 2. Experimentally measured stress mapping by AFM-Raman in the parallel TSVs layout.

Figures 4(a) and (b) respectively show the Mohr's circle for the stress analysis on the parallel TSV layout and the perpendicular TSV layout. Firstly, it should be noted that the stress characteristics of case C are clearly not equal to the direct sum of cases A and B for both the parallel and perpendicular layout. The strong stress

Ming-Han Liao is associate professor of mechanical engineering at National Taiwan University, Taipei, Taiwan, R. O. C.

Ssu-Chieh Kao is an M.S. candidate at National Taiwan University.

Sung-Jie Huang is an M.S. at National Taiwan University, Taipei.



interaction between two close TSVs leads to the nonlinear stress effect and the linear superposition principle cannot be directly used for stress analysis. For both layouts, we may see a left-shift of the Mohr's circle for Case C compared with the linear superposition of the results of both TSVs considered individually, which will be referred to as Case A + Case B. The real normal stress of Case C is smaller than the normal stress obtained from applying the linear superposition principle on Case A and Case B. This is due to the stress interactions between the two close TSVs. The additional TSV located between the device area and the original TSV (shown in Fig. 5(a)) has an important influence on stress transmission. In addition to the normal stress, the maximum shear stress, which is the radius of the Mohr's circle, for both TSV layouts will require evaluation.

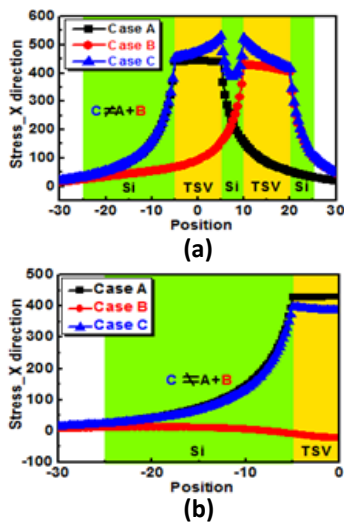


Fig. 3. Stress distribution among different TSV layouts, including the parallel layout shown in Fig. 3(a) and perpendicular layout shown in the Fig. 3(b).

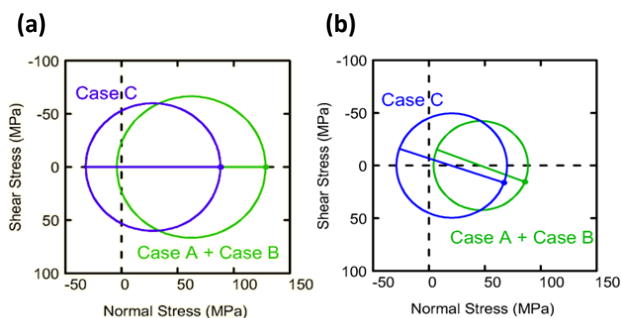


Fig. 4. Mohr's circles for the stress analysis on two different TSV layouts, including the parallel layout shown in Fig. 4(a) and the perpendicular layout shown in Fig. 4(b).

For the case of parallel TSV layout, as shown in Fig. 1(a), a smaller shear stress is observed in Fig. 4(a) for the real case (Case C) compared to the linear superposition of the two TSVs considered individually, depicted as Case A + Case B. We see a decrease in the radius for the

Mohr's Circle for Case C of the parallel TSV layout, implying a decrease of maximum shear stress.

The stress interaction between the two close TSVs, which reduces the aforementioned normal stress, will also reduce the maximum shear stress. For the parallel TSV layout, the stress from the right TSV is reduced as it is cut-off by the close TSV at its right. This phenomenon of stress cut-off is shown in Fig. 5(a). Since the location of the observation point (i.e., the device position) is in line with the two TSVs, the angular difference between the two major normal stresses is zero, which implies that the innate shear stress at the observation point (device position) is zero. This is demonstrated by the two critical points of the Mohr's circle being on the X-axis in the parallel TSV layout, as shown in Fig. 4(a).

For the case of the perpendicular TSV layout, as shown in Fig. 1(b), a larger shear stress is observed in Fig. 4(b) for the real case (case C) of the linear superposition of the two TSVs considered individually, depicted as Case A + Case B. The increased radius of the Mohr's Circle indicates an increase of maximum shear stress. However, in the real case (Case C) where both TSVs are present simultaneously, there is a shear stress component in addition to the normal stresses exerted at the observation point (device position). This shear stress component is absent from the direct summation result of Case A + Case B. Unlike the parallel TSV layout, the angle between the direction of the two major normal stresses is not zero, which induces an innate shear stress, as shown in Fig. 5(b). We prove this by noting that the critical points in Fig. 4(b) are not on the X-axis, implying the existence of a non-zero innate shear stress. This missing term of the innate shear stress from Case A + Case B will lead to it having a lower maximum shear stress and Mohr's circle radius compared to that of Case C, where the innate shear stress is considered.

Once the stress characteristics are understood, the change of carrier mobility is then investigated on these two different TSV layouts (Fig 6). The change of the electron mobility with the consideration of the nonlinear stress from the strong stress interactions between TSVs is ~2-6% smaller than when the linear stress superposition principle is considered in isolation. This indicates that the need to carefully design and manage the model of stress and device performance for modern complicated circuits and TSV layouts in 3DIC. The linear superposition cannot be used directly for the analysis of stress. The analytic nonlinear modeling is of particular importance to determine the details of the strain distribution for these 3DICs structures.

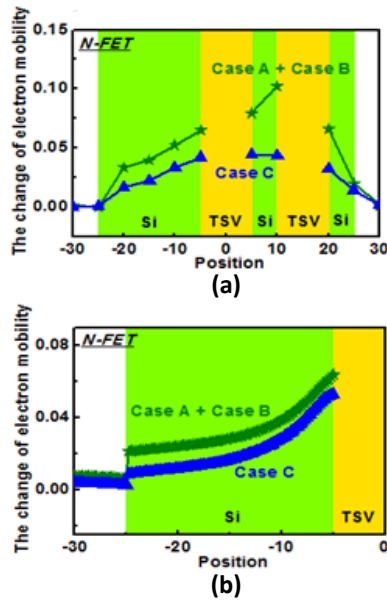


Fig. 5. Illustration of the stress interaction and its influence with different TSVs layouts.

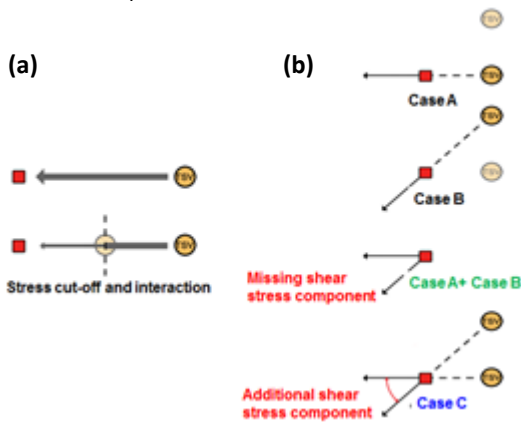


Fig. 6. Change of carrier mobility with different TSVs layouts considering of the nonlinear stress effect from the strong stress interaction and considering the linear stress superposition principle in isolation.

Conclusion

Based on the FEM results, the Mohr's circle stress analysis, and the actual stress measurements using the AFM-Raman technique for the different layouts of TSVs in the 3D circuit, the linear superposition principle without consideration of the stress interaction between TSVs is found to cause a larger error for the stress estimation in the vicinity of TSV. The change of the electron mobility with consideration of the nonlinear stress analytic model is ~2-6% smaller than that which considers the linear stress superposition principle in isolation. These experimental results indicate that the stress interaction among TSVs plays an important role in boosting device performance and in minimizing the variability device performance in future 3DICs. Analytic nonlinear

modeling is of particular importance to determine the details of the strain distribution for these 3DICs structures.

Acknowledgment

This work is supported by National Science Council (NSC), Taiwan, under the Grant Nos. 101-2628-E-002-018-MY3 and 103-2221-E-002-215-MY3, and Ministry of Economic Affairs (MEA), Taiwan, under the Grant No. 103-EC-17-A-01-S1-219. .

References

- [1] A. Mercha, G. Van der Plas, V. Moroz, I. De Wolf, P. Asimakopoulos, N. Minas, S. Domae, D. Perry, M. Choi, A. Redolfi, C. Okoro, Y. Yang, J. Van Olmen, S. Thangaraju, D. Sabuncuoglu Tezcan, P. Soussan, J. H. Cho, A. Yakovlev, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, and B. Swinnen, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-k / metal gate cmos performance," in proceeding of *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, Dec. 6-8, 2010, pp. 2.2.1-2.2.4. doi: [10.1109/IEDM.2010.5703278](https://doi.org/10.1109/IEDM.2010.5703278)
- [2] J.-C. Lin, W.-C. Chiou, K.-F. Yang, H.-B. Chang, Y.-C. Lin, E.-B. Liao, J.-P. Hung, Y.-L. Lin, P.-H. Tsai, Y.-C. Shih, T.-J. Wu, W.-J. Wu, F.-W. Tsai, Y.-H. Huang, T.-Y. Wang, C.-L. Yu, C.-H. Chang, M.-F. Chen, S.-Y. Hou, C.-H. Tung, S.-P. Jeng, and D. C. H. Yu, "High density 3d integration using cmos foundry technologies for 28 nm node and beyond," in proceeding of *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, Dec. 6-8, 2010, pp. 2.1.1-2.1.4. doi: [10.1109/IEDM.2010.5703277](https://doi.org/10.1109/IEDM.2010.5703277)
- [3] H. Chaabouni, M. Rousseau, P. Leduc, A. Farcy, R. El-Farhane, A. Thuair, G. Haur, A. Valentian, G. Billiot, M. Assous, F. De Crecy, J. Cluzel, A. Toffoli, D. Bouchu, L. Cadix, T. Lacrevez, P. Ancey, N. Sillon, and B. Flechet, "Investigation on tsv impact on 65nm cmos devices and circuits," in proceeding of *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, Dec. 6-8, 2010, pp. 35.31.31-35.31.34. doi: [10.1109/IEDM.2010.5703479](https://doi.org/10.1109/IEDM.2010.5703479)
- [4] G. Eneman, J. Cho, V. Moroz, D. Milojevic, M. Choi, K. De Meyer, A. Mercha, E. Beyne, T. Hoffmann, and G. Van der Plas, "An analytical compact model for estimation of stress in multiple through-silicon via configurations," in proceeding of *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, March 14-18,

- 2011, pp. 1-2.
doi: [10.1109/DATE.2011.5763088](https://doi.org/10.1109/DATE.2011.5763088)
- [5] C. S. Selvanayagam, J.-H. Lau, X. Zhang, S. K. W. Seah, K. Vaidyanathan, and T.-C. Chai, "Nonlinear thermal stress/strain analyses of copper filled tsv (through silicon via) and their flip-chip microbumps," *Advanced Packaging, IEEE Transactions on*, vol. 32, no. 4, pp. 720-728, 2009.
doi: [10.1109/TADVP.2009.2021661](https://doi.org/10.1109/TADVP.2009.2021661)
- [6] K.-H. Lu, X. Zhang, S.-K. Ryu, J. Im, R. Huang, and P.-S. Ho, "Thermo-mechanical reliability of 3-d ics containing through silicon vias," in proceeding of *The 59th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, May 26-29, 2009, pp. 630-634.
doi: [10.1109/ECTC.2009.5074079](https://doi.org/10.1109/ECTC.2009.5074079)
- [7] M.-H. Liao, C.-C. Hua, C.-L. Cheng, Y. Chen, and K.-S. Chieh, "Additional nitrogen ion-implantation treatment in sti to relax the intrinsic compressive stress for n-mosfets," *IEEE Transactions on Electron Devices*, vol. 59, no. 8, pp. 2033-2036, 2012.
doi: [10.1109/TED.2012.2198824](https://doi.org/10.1109/TED.2012.2198824)
- [8] M.-H. Liao, M.-Y. Yu, G.-H. Liu, C.-H. Chen, and T.-K. Hsu, "The demonstration of nonlinear analytic model for the strain field induced by thermal copper filled TSVs (through silicon via)," *AIP Advances*, vol. 3, no. 8, p. 082123, 2013.
doi: [10.1063/1.4706565](https://doi.org/10.1063/1.4706565)
- [9] D.-Z. Pan, S.-K. Lim, K. Athikulwongse, M. Jung, J. Mitra, J. Pak, M. Pathak, and J.-S. Yang, "Design for manufacturability and reliability for tsv-based 3d ics," in proceeding of *Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific*, Sydney, NSW, Jan. 30- Feb. 2, 2012, pp. 750-755.
doi: [10.1109/ASPAC.2012.6165055](https://doi.org/10.1109/ASPAC.2012.6165055)
- [10] M.-H. Liao, C.-H. Chen, L.-C. Chang, C. Yang, and S.-C. Kao, "The relaxation of intrinsic compressive stress in complementary metal-oxide-semiconductor transistors by additional n ion implantation treatment with atomic force microscope-raman stress extraction," *Journal of Applied Physics*, vol. 111, no. 9, pp. 094511-094511-094514, 2012.
doi: [10.1063/1.4714558](https://doi.org/10.1063/1.4714558)
- [11] M.-H. Liao, "Local stress determination in shallow trench insulator structures with one-side and two-sides pad-sin layer by polarized micro-raman spectroscopy extraction and mechanical modelization," *Journal of Applied Physics*, vol. 105, no. 9, pp. 093511-093511-093514, 2009.
doi: [10.1063/1.3116531](https://doi.org/10.1063/1.3116531)
- [12] M.-H. Liao, "Optimal stress design in p-mosfet with superior performance," *IEEE Transactions on Electron Devices*, vol. 55, no. 12, pp. 3615-3618, 2008.
doi: [10.1109/TED.2008.2006921](https://doi.org/10.1109/TED.2008.2006921)
- [13] M.-H. Liao, L. Yeh, T.-L. Lee, C.-W. Liu, and M.-S. Liang, "Superior n-mosfet performance by optimal stress design," *IEEE Electron Device Letters*, vol. 29, no. 4, pp. 402-404, 2008.
doi: [10.1109/LED.2008.918420](https://doi.org/10.1109/LED.2008.918420)

