

RF CMOS Oscillators Design for autonomous Connected Objects

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Abstract. Voltage controlled oscillator (VCO) is an integral part of IoT wireless transceiver components. In this paper, VCOs operating around 2.4 GHz have been designed in CMOS technology. The relation between their components and specifications is studied for their performance optimization. Ultra-low power, less than 270 μ W, has been obtained, while performing a frequency tuning range of about 10% between 2.1 and 2.4 GHz. Investigations on phase noise performance have been also achieved.

1 Introduction

The Internet of Things (IoT) has been in the spotlight for the past decade and has greatly impacted our economy, society and daily life. Objects are becoming intelligent and wirelessly interoperable due to the development of identification, sensor and communication technologies [1]. Today, many connected objects are deployed to enhance health monitoring, transport, wearables, digital life and digital industry. Recent studies estimate that as of now, there are 25 billion connected devices, and by 2020 it would reach 50 billion devices [2].

Key requirement for IoT is the ability to place wireless sensor terminals in all kinds of locations to collect desired data. This global deployment of IoT must bring challenges to each IoT sensor terminal mainly of low-power, low-cost and miniaturization.

The wireless transceiver is an important part of IoT terminals. It achieves transmission and reception of the data using radiofrequency (RF) connectivity, as shown in Figure 1.

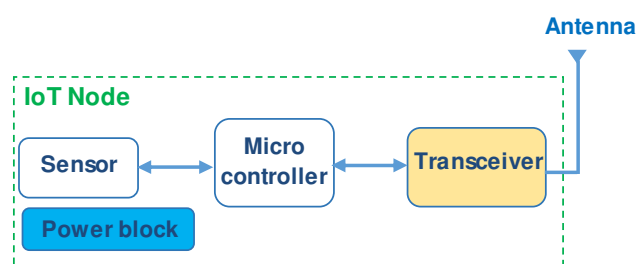


Fig. 1. IoT node topology

RF voltage controlled oscillator (VCO) is one of the main components of the transceiver. VCOs can be divided into two main categories: Inductor (L)-capacitor (C) VCO and ring VCO. Ring oscillators are characterized by a wide tuning range and low area occupation.

However, they usually end up with unacceptable phase noise for most wireless applications. Using an LC oscillator improves the phase noise, while consuming much power because of the current required to sustain the tank oscillation. The phase-noise of an LC-oscillator is correlated with the quality factor of the inductor. The higher the quality factor, the lower is the phase noise, but the bigger is the inductor size increasing the circuit cost that is a brake for the deployment of the IoT.

Many approaches have been used in the literature to reduce the power consumption of oscillators for ultra-low-power applications. A straightforward strategy was to use a high-Q tank like the FBAR as proposed by Wang et al., causing an extra cost [3]. Alternative techniques consist of sharing the bias current [4] or reducing the voltage supply which induces the use of MOS transistors operating in the subthreshold region.

In this work, different ultra-low-power 2.4 GHz LC VCOs are designed and implemented in 130nm CMOS technology: one using the current-reused technique and the other biased in the subthreshold region with adaptive body biasing technique. At such a low bias level, the measured phase noise of the VCO can be influenced by the environment making difficult the characterization of its intrinsic noise contribution. The noise characteristics of these RF VCOs are investigated in order to reduce the lowest consumption that can be achieved. Measured power consumption is less than 270 μ W for both circuits making them suitable for ultra-low power applications.

This paper is organized as follows. Section 2 investigates the design approach of RF LC-VCOs taking into account the design trade-offs. Section 3 describes both ultra-low-power VCO topologies. The obtained results are presented and discussed in section 4. Section 5 draws conclusions.

2 RF LC-VCO design approach

The progress in technology development has led to more challenging integrated circuits design. In the case of RF circuits, analog signals with wide dynamic range at high frequencies must be processed. The VCO, a critical element in the RF front-end, has many design challenges to accomplish the required specifications, at low power consumption and low phase noise.

The trade-off between oscillation frequency, power consumption, area and phase noise are particularly demanding when aiming a fully integrated solution. The trade-offs involved in the design of such circuits can be summarized in Fig. 2(a). Most of the commonly used RF oscillators are based on LC topology. It can be modelled as shown in Fig. 2(b). It consists of LC resonator, also referred as LC tank, and an active circuit used to compensate tank losses [5].

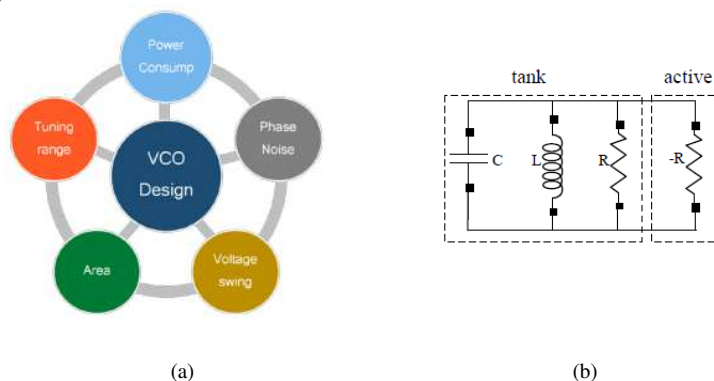


Figure 2. (a) VCO design trade-offs. (b) Simple model of an LC-VCO.

To maintain oscillation, the negative resistance (Gn) provided by the active circuit should be higher than the passive element loss Gp of the resonator circuit. The condition of oscillation can be defined as follows

$$Gp \leq |Gn| \tag{1}$$

In order to optimize RF oscillator design, it is necessary to consider the relation between its components and its design constraints. The design approach is based first on the study of the relation components/constraints and then on a physical and technological analysis of each component. The main goal is to guarantee good VCO design compromises essentially in terms of phase noise and power consumption. Figure 3 depicts the impact of the physical parameters of the LC-VCO elements (spiral inductor, varactor and active circuit) on its performances. Hence, it facilitates their choice depending on the different constraints of the desired application. If drastic constraints on power consumption and phase noise are considered, optimizing each element composing the VCO is mandatory, in particular the spiral inductor that contributes to area occupation.

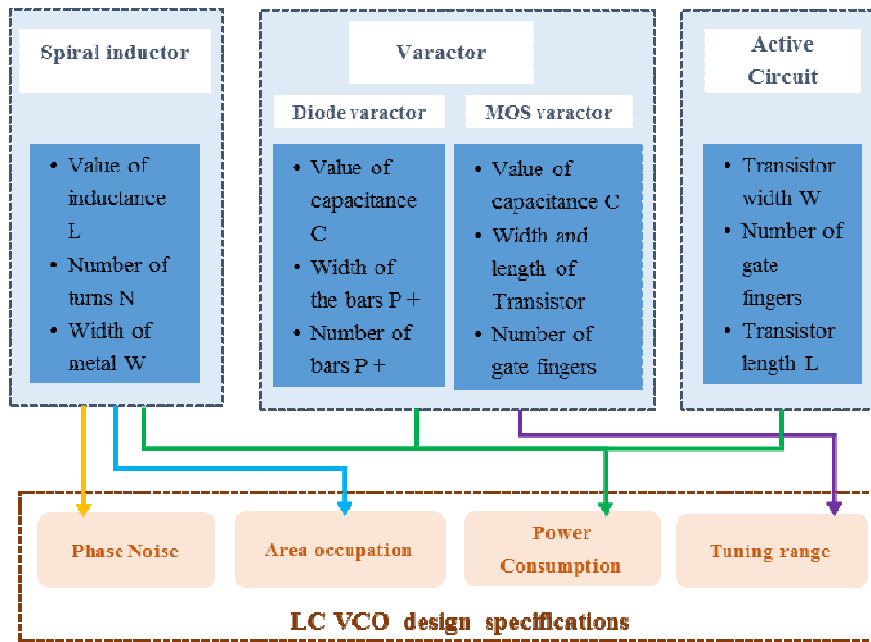


Figure 3. Impact of the VCO's components on its performance

Regarding the implementation of a low power and low phase noise LC-VCO, the design method deals with sizing the inductor components of the LC tank. Firstly, an optimal inductor value with minimal series resistance and maximal quality factor should be chosen at the desired operating frequency. In fact, using a high inductor value causes reduction of the resistive losses, and then a reduction of the VCO power consumption. Note that the inductance value is limited by its self-resonance frequency, which should be higher than the oscillation frequency. Secondly, after fixing the inductance value, the optimization variables that characterize the inductor geometry (number of turns N and turn width W) have to be selected.

Furthermore, varactor (C_{var}) is used to tune the oscillation frequency by the control voltage V_{ctrl} . A good varactor is characterized by a high-Q and a maximal ratio C_{max}/C_{min} leading to a wide tuning range. The series resistance of varactor has an imperious effect on overall tank quality factor. In this regard, the diode varactor gives a better compromise between tuning range and Q than the MOS varactor.

Afterwards, the focus goes to the active part of the VCO. An optimal sizing of MOS transistors contributes to a noise reduction. In fact, the transistor noise is directly related to the grid resistance R_g , then it should be decreased. Sizing the MOS with a maximal number of fingers causes a reduction of R_g . Thus, multi-fingers transistors have been used in this work to decrease the noise.

3 Circuits description

There are several topologies of LC-VCOs. The most popular one is the NMOS cross-coupled structure, shown in Figure 4(a). It is suited to be used with a supply voltage below the threshold voltage, so that the dc-power consumption will be decreased resulting in low power VCO designs.

Another common LC-VCO topology is based on CMOS cross-coupled, as depicted in Fig. 4(b). It uses two MOS pairs operating at the triode region. These MOS switching transistors are connected to generate the sufficient negative resistance for tank loss compensation. In order to reduce the current draw, both PMOS and NMOS switches are closed in the positive half cycle of the output. In this period, the DC current flows in the tank and load the capacitance of MOS varactor. In the next half cycle, the MOS switches are opened and the tank discharges [5].

Nevertheless, this technique suffers from imbalance of differential outputs voltage swing in terms of amplitude and phase. These asymmetries, caused by the difference of transconductances and parasitic capacitances of PMOS and NMOS transistors [6-7], resulting on power level mismatch of the differential output ports.

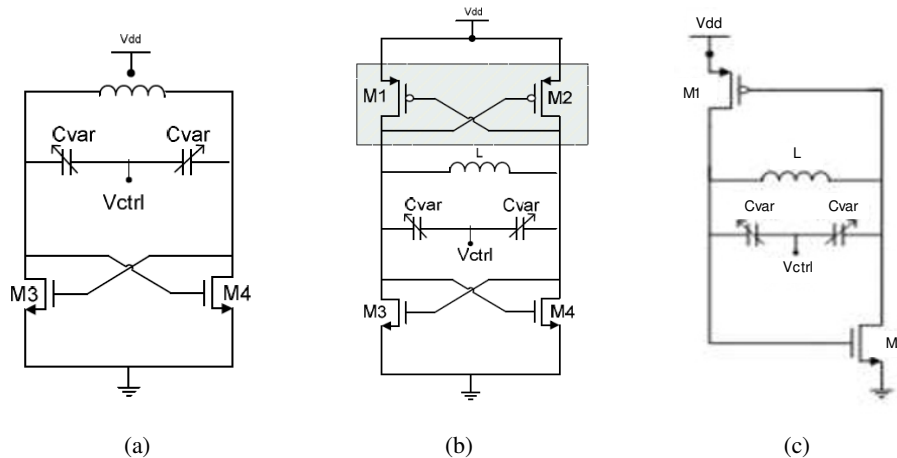


Figure 4. Schematics of LC-VCOs using the (a) NMOS cross-coupled, (b) CMOS cross-coupled and (c) current-reused topologies.

3.1 Current-reused VCO

The current-reused LC-VCO topology is used to reduce power consumption. Its operation mode is quite similar to the traditional cross-coupled CMOS LC-VCO in the first half period. However, in the second half period, the current-reused VCO is not required to provide current. Therefore, the power consumption is the half of the traditional and also phase noise is improved. The current-reused LC-VCO shown in Figure 4(c) has been designed using the optimization approach given in Figure 3 to reduce phase noise and power consumption. This structure can solve the asymmetry problem of differential output voltage swing.

In the first step, the resonator is set to optimize the quality factor of inductor Q_L and varactor Q_C because it often determines the phase noise of the oscillator. The total loaded quality factor at the resonant frequency can be expressed as

$$Q_{\text{tank}} = \frac{1}{\frac{1}{Q_L} + \frac{1}{Q_C}} \approx \frac{R_p}{\omega_0 L} \quad (2)$$

where ω_0 is the resonant frequency and R_p presents the parallel resistance of the LC tank, modelling the total losses of the tank.

In order to satisfy the condition of oscillation given in (1) and to ensure the desired operating frequency with low power performances, an optimization of the resonator loss should be achieved. This loss is defined as

$$G_p = \frac{1}{R_p} = \frac{1}{Q_{\text{tank}} \omega_0 L} = \frac{C \omega_0}{Q_{\text{tank}}} \quad (3)$$

The next step of the optimization approach concerns the transistors sizing. By using a large size of PMOS transistor, the drawing current can be increased, which limits the power consumption. Further study of relation between PMOS and NMOS transconductances g_{mp} and g_{mn} respectively gives

$$g_{mn} = \sqrt{\frac{3}{A}} g_{mp} \quad (4)$$

where A is the ratio between transistors widths ($W_p = A \cdot W_n$). It can be noted that when A increases, the NMOS transconductance g_{mn} is decreased. Thus, it is possible to adjust the transistors sizes in order to ensure the minimum negative resistance by using this expression.

3.2 Sub-threshold VCO

Implementing ultra-low power analog circuits creates a need for reducing the supply voltage and employing transistors biased in subthreshold region. The subthreshold regime, also known as weak inversion, exhibits higher transconductance G_m for a given bias current and comparable noise performance than the super-threshold one. In the subthreshold region, the gate source voltage V_{gs} is slightly above the threshold voltage V_{th} of the transistor and the concentration of carriers is very low but not negligible [8].

Using subthreshold MOS devices to implement analog circuits is allowed in low phase noise and low power VCO. However, it presents a high sensitivity to process, voltage and temperature (PVT) variations because CMOS has exponential property in subthreshold region. In order to overcome the PVT effects, VCOs must be designed for worst-case

conditions. Another solution is to use the adaptive body-biasing technique [9]. The principle consists to detect the VCO output amplitude and to feed it back to the body bias of the negative transconductance cell G_n . Then depending on VCO amplitude, the body-bias of G_n can be adjusted automatically in order to maintain a constant transconductance over PVT variations. The amplitude detector used in a cross-coupled LC-VCO is depicted in Figure 5.

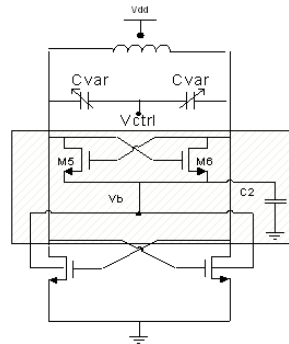


Figure 5. LC-VCO design using the adaptive body-biasing technique

It detects the minimum output voltages (V_{out+} and V_{out-}) and stores the obtained source voltage V_b into the capacitors C_2 . Therefore, when the VCO output amplitude decreases, V_b increases. The increased V_b lowers the threshold voltage of the negative transconductance cell and increases the transconductance G_n , thereby increasing the amplitude of the VCO output.

4 RF LC-VCO implementation and results

4.1 Implementation

LC-VCOs working around 2.4 GHz have been realized in 130nm CMOS process. Considering the proposed design approach, these circuits have been designed with main challenges of low power consumption and low phase noise. The first VCO is based on the current-reused topology, shown in Figure 4(c). It is followed by a 2-stage-buffer for experimentation constraints.

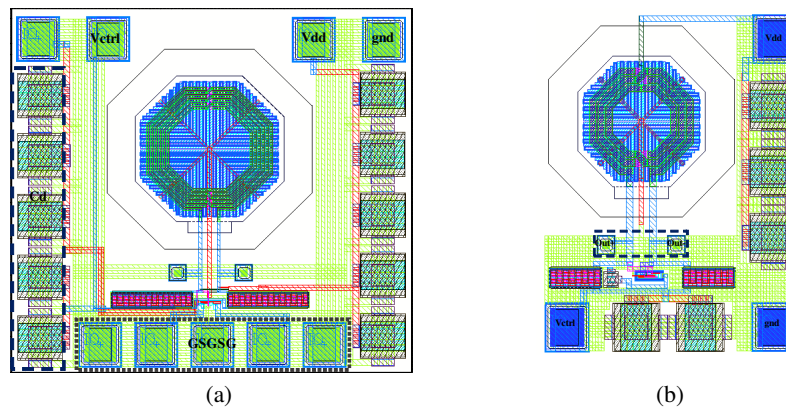


Figure 6. Implemented (a) current-reused and (b) NMOS subthreshold VCOs

Whereas, the second VCO is biased on the subthreshold region and uses the NMOS cross-coupled structure with adaptive body-biasing, shown in Figure 5, to allow good immunity to PVT variations.

Figure 6 depicts the layouts of both implemented LC-VCOs. The occupied surfaces are $(690 \times 630) \mu\text{m}^2$ and $(560 \times 426) \mu\text{m}^2$ with PADs for current-reused and NMOS subthreshold VCOs respectively.

4.2 Results

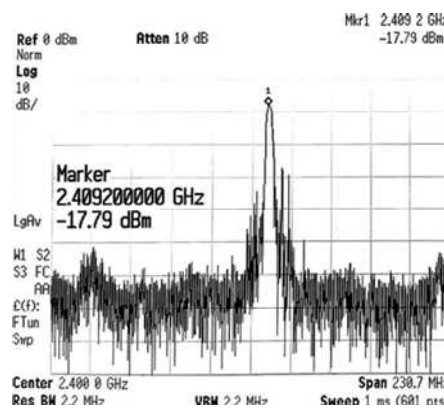
The measurement setup of on-chip RF circuits is very complex, especially if noise requirements are stringent (case of RF oscillators). The used probe station is shown in Figure 7. First, DC and RF probing are positioned into the PADs on the wafer. Then, they are connected with RF cables to the spectrum analyzer. Special care must be taken to the 50Ω probing calibration to meet measuring instruments needs. Besides, resolution bandwidth (RBW) of the spectrum analyzer should be calibrated, since it can be important versus the noise bandwidth. Noise floor of the setup measurement need to be calibrated as well.



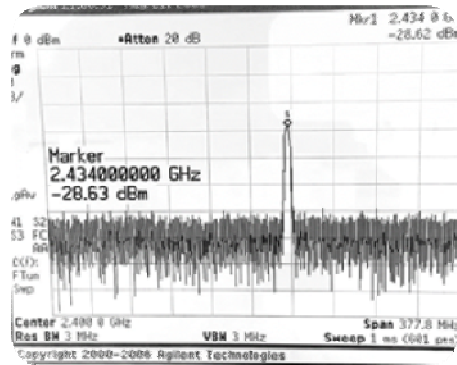
Figure 7. On-chip measurement station

Measurements have been done at nominal operating conditions : room temperature with noise and interferences are all around the measuring station, that will probably degrade the noise floor characteristic of the VCO.

The obtained output frequency spectrums are depicted in Figure 8. The current-reused VCO, biased with a voltage supply and a control voltage of 1V, achieves an oscillation frequency of 2.409 GHz, while the subthreshold VCO, biased at 0.6V, oscillates at 2.434 GHz.



(a)



(b)

Figure 8. Output spectrums of the (a) current-reused and (b) subthreshold LC-VCOs

Concerning the power consumption, it is as low as $262\mu\text{W}$ for the current-reused VCO and $168\mu\text{W}$ for the subthreshold VCO. These values are constant while changing control voltage, V_{ctrl} .

The phase noise has been measured using the spectrum analyzer. The profile of the current-reused VCO is depicted in Figure 9. It shows -102.16 dBc/Hz at 1MHz offset from the carrier for $V_{ctrl} = 1\text{V}$. However, post-layout simulations present a phase noise of -114.7 dBc/Hz at 1MHz offset. The same performance is observed with the subthreshold VCO. Note that the phase noise exhibits a degradation that was predictable due to the measurement conditions in a noisy environment around the test station. Indeed, a noise measurement of RF circuit is usually done with faraday chamber (which is not our case).

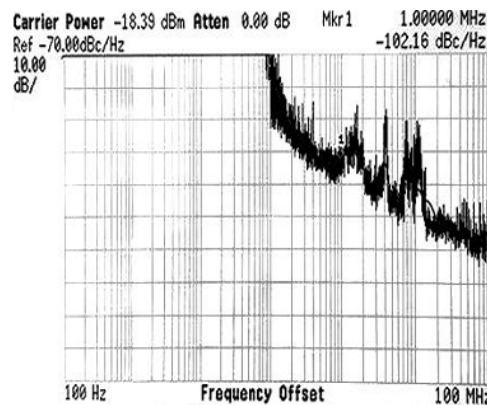


Figure 9. VCO's phase noise profile.

LSSB facilities with well-known noise characteristics and calibrated environment are a good opportunity to perform VCO phase noise measurement as a future work. One must point out the VCO's intrinsic noise floor characterization in order to investigate the phase noise profiles in different environments.

5 Conclusion

VCO is one of the key elements in RF transceivers. This work presents design trade-offs of RF VCOs and proposes a design approach associated to low-power LC-VCOs. Also, phase noise has been investigated. 2.4 GHz LC-VCOs have been implemented with full CMOS process. Measurement setup and obtained results in a nominal condition (a room environment with noise and interferences around the measuring station) have been presented. It was noted that the phase noise needs to be measured in a low-noise environment. Further VCO noise measurement will be done in LSBB facilities to address the more realistic phase noise.

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