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DESIGN AND SIMULATION OF HIGH PRECISION SECOND-ORDER SIGMA-DELTA MODULATOR FOR BLUETOOTH APPLICATIONS

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Abstract

A second-order sigma-delta modulator is presented in this paper which, according to the considered standards, is suitable for bluetooth applications. The oversampling ratio and signal bandwidth of the proposed modulator is 128 and 1 MHz, respectively. The Signal to Noise and Distortion Ratio (SNDR) of the proposed structure is achieved 74 dB, equivalent to 12-bit accuracy, which is desirable precision for the aforementioned application. Utilizing high-performance blocks to implement the system at the circuit level, the sigma-delta modulator has obtained an overall desirable performance more specifically in terms of minimizing the power consumption. The modulator is simulated in 180 nm CMOS TSMC technology at cadence software applying 1.8 V supply voltage. The power consumption is obtained as low as 1.9 mW very suitable for portable modern ultra-low power applications.

Keywords: Bluetooth application, High precision, Low power, Second-order, Sigma-delta modulator.

1. Introduction

With recent enormous developments of the technology, demand for smaller and more efficient circuit and system design has increased [1]. This is more especially applies for digital portable transceivers that use batteries as their power source, such as, Phones equipped with WLAN and bluetooth capabilities [1]. Bluetooth is one of the most successful short-range wireless communication technologies, which is utilized at numerous devices such as cell phones, headsets, headphones, game consoles and music players. According to Daoud et al. [2], Analog to Digital Convertor (ADC) is one of the most essential building blocks needed for data transmission utilized at digital transceivers. The ADC is used to produce the digital version of the analog input signals to be used at preprocessor core and final data transmission step [3], which is accomplished in digital domain due to its advantages versus analog domain [4].

Considering the sampling frequency, the analog to digital converters are designed and used either at a Nyquist rate or oversampling rate. Nyquist rate ADCs are suitable for high speed, medium/low precision applications and the hardware per bit correspondence must be met for them during circuit implementation [5]. On the other hand, for the oversampling ADCs the sampling frequency is very higher than the input signal frequency and the converters precision is increased as the sampling frequency increases. Hence, the oversampling ADCs are suitable for high precision low-frequency applications. In order to further increase the precision of the oversampling ADCs, out of band noise shaping of the quantization noise is preferred, which is accomplished by sigma-delta modulation techniques [6].

Sigma-delta modulators are the best choice where low frequency and high precision applications are considered. Obtaining higher precision with simple low-power structures is possible at sigma-delta ADCs in comparison with their other counterparts due to the oversampling and noise shaping technique [7, 8], which makes them attractive for short-range bluetooth applications as well [9]. Emerging bluetooth technologies require lower power consumption and simpler circuitry, which impose new restrictions on the modulator incorporated at sigma-delta ADC [10].

In this paper, a simple sigma-delta modulator is presented for Bluetooth applications. Utilizing low-power operational amplifiers and comparators, the proposed structure's total power consumption is the very low value of 1.9 mW.

This paper is organized as follows: In Section 2, the structure of the sigma-delta modulator system is investigated. The circuit level implementation of the modulator and its various blocks are described, in Section 3. Simulation results are provided in Section 4 and finally, Section 5 concludes the paper.

2. Modulator System-Level Structure

In order to design a modulator at system-level, first of all, the specifications required for the considered standard and application must be obtained and then the appropriate structure with proper coefficients are selected and designed to obtain the optimum performance of the modulator. To choose the system-level structure of the sigma-delta modulator, the type of structure and the blocks utilized inside must be considered. Accomplishing numerous system-level structure designs by trial and errors, it is realized that for bluetooth application the proper structure of the modulator is a second-order single-ring structure. Single loop structures are also

effective in maintaining the simplicity of the circuit and also reducing the power consumption of the modulator. For the proposed modulator, the capacitive switch structure has been also used because of the performance sensitivity of the continuous time structure to the latency of the analog circuits and the embedded extra loop.

The second-order single-ring sigma-delta modulator structure is shown in Fig. 1. This structure is less sensitive and has low noise due to the distortion of the operational amplifier. According to Farahani and Ismail [11], including an input feed-forward path in a single sigma-delta modulator is a method for reducing the limitations of the analog blocks utilized in the proposed modulator. This path is shown in Fig. 1 with a dashed line.

It is shown in Fig. 1 that the sigma-delta modulator has two distinct entry one for the input signal and another for quantization noise. The Signal and Noise Transfer Functions (NTF) can hence, be calculated as Eqs. (1) and (2).

$$STF(z) \equiv \frac{Y(z)}{X(z)} = \frac{1 + a_1 a_2 a_3 \left(\frac{z^{-2}}{(1-z^{-1})^2} \right) + a_1 a_4 \left(\frac{z^{-1}}{(1-z^{-1})} \right)}{1 + a_1 a_2 a_3 \left(\frac{z^{-2}}{(1-z^{-1})^2} \right) + a_1 a_4 \left(\frac{z^{-1}}{(1-z^{-1})} \right)} = 1 \quad (1)$$

$$NTF(z) \equiv \frac{Y(z)}{E(z)} = (1-z^{-1})^2 \quad (2)$$

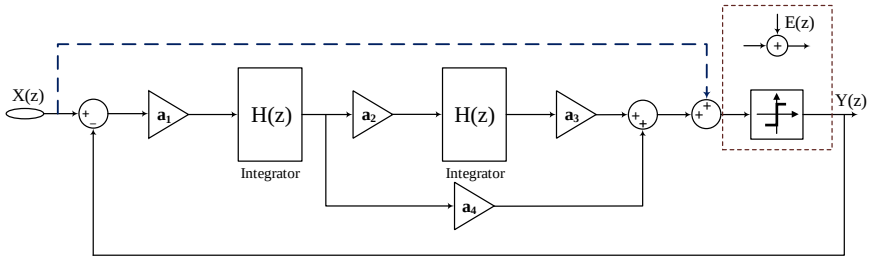

Fig. 1. Block diagram of the second-order single loop sigma-delta modulator.

The unity size Signal Transfer Function (STF) actually means that the STF is equal to one for all frequency ranges. An interesting feature of the unity size STF structure is that for ideal conditions, the integrators do not have any effect on the input signal and only affect the quantizer error. In addition, this method is applicable to any OSR value, which makes the structure particularly suited to reduce the sensitivity of a modular circuit implementation for broadband applications.

To simulate the structure of Fig. 1, a single-bit quantizer is used due to its inherent linearity and simplicity. This eliminates utilizing the dynamic elements matching circuit, which consequently reduces both power consumption and the capacitive loads of the operational amplifiers. But it should be considered that for modulators in which, the use of multi-bit quantizers is necessary, their non-linearity must be noise-shaped so that they have little impact on the performance of the sigma-delta modulator.

The system-level structure of the modulator is simulated with an oversampling rate of 128 MHz and signal bandwidth of 1 MHz in MATLAB Simulink. Gain coefficients can be obtained by calculating modulator signal and noise transfer functions. The optimum coefficients for system level implementation can be either found by re-simulation or by analytical calculations. The coefficients a_1, a_2, a_3 and a_4 are achieved by analytical calculations as follows:

The output relation versus input and noise of sigma-delta modulator is calculated as Eq. (3).

$$Y(z)=\left[X(z)\left(a_1\frac{z^{-1}}{(1-z^{-1})}\right)-Y(z)\left(a_1\frac{z^{-1}}{(1-z^{-1})}\right)\right]\left[a_2a_3\frac{z^{-1}}{(1-z^{-1})}+a_4\right]+X(z)+E(z) \quad (3)$$

Calculating the STF and NTF as is given by Eq. (4) and comparing with Eqs. (1) and (2) the relationship between the coefficients can be written as Eq. (5):

$$NTF(z)=\frac{(1-z^{-1})^2}{(1+(a_1a_4-2)z^{-1}+(1+a_1a_2a_3-a_1a_4)z^{-2}}\ ,\ STF(z)=1 \quad (4)$$

$$\begin{aligned} &a_1a_4-2=0\rightarrow a_1a_4=2\\ &1+a_1a_2a_3-a_1a_4=0\rightarrow a_1a_2a_3=1 \end{aligned} \quad (5)$$

There are numerous values, which can apply to the Eq. (5). The optimum parameters can be achieved by try and error to obtain the desired performance. According to the results obtained from the system level analysis, the optimum coefficients are achieved for a_1, a_2 = 0.25 and for a_3, a_4 = 8 by MATLAB.

3. Circuit Level Design of the Modulator

The proposed circuit level modulator is shown in Fig. 2, which is a switch capacitor structure that implemented with a supply voltage of 1.8 V. The circuit level realization of the sigma-delta modulator includes amplifiers and comparators as the basic blocks incorporated in integrators and quantizers, respectively. The circuits used to implement the proposed modulators will be described.

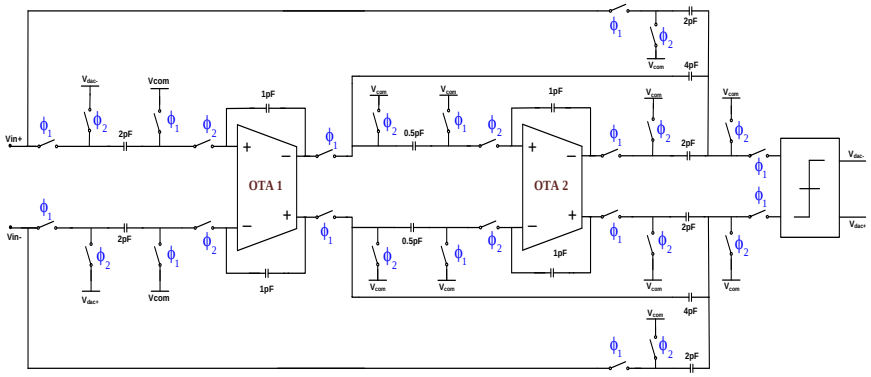

Fig. 2. Second order sigma-delta modulator implementation.

3.1. Operational amplifier

The most critical block of the sigma-delta modulator is the first integrator, in which the amplifier plays an essential role [11]. To evaluate the performance of the operational amplifiers utilized in switch capacitor circuits, various parameters such as gain, unity gain frequency, phase margin and slew rate should be considered. Undesirable parameters impose severe limitations on the modulator performance.

The small low-frequency gain of the amplifier affects the accuracy of the discrete time transfer function coefficients. The unity gain frequency and the phase margin also give an insight into the settling behaviour and performance of the amplifier. The limited slew rate can restrict the upper speed of the clock in a capacitive circuit.

There are various structures for operational amplifiers in order to achieve the desired performance in the sigma-delta converter, but in this paper, an operating amplifier with a recycling folded cascode structure has been used [12] as shown in Fig. 3. Table 1 shows the parameters obtained from the simulation of the amplifier by cadence for 180 nm technology. The operational amplifier frequency response gain is shown in Fig. 4.

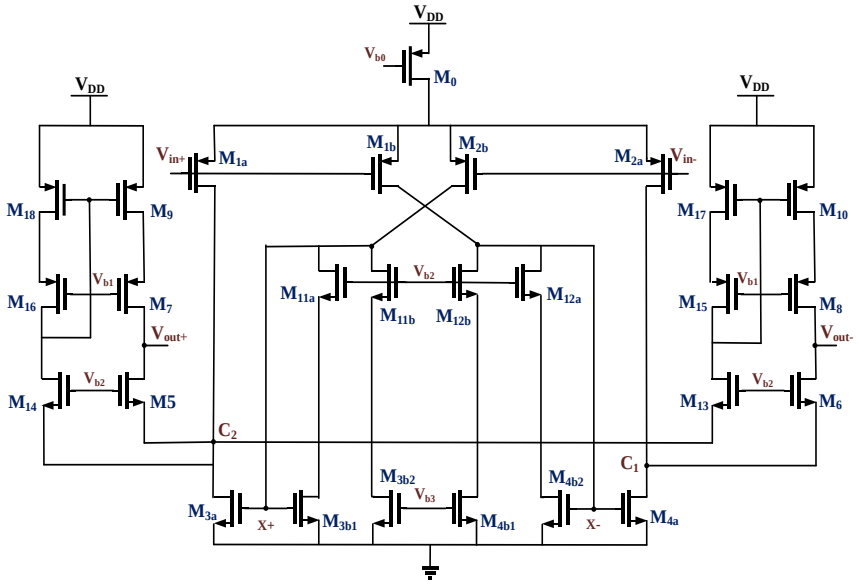

Fig. 3. Fully differential IRFC OTA.

Table 1. Specifications of the Operational Trans-Conductance Amplifier (OTA).

DC gain	40 dB
Phase margin	50 deg.
Gain Bandwidth (GBW)	147 MHz
Power consumption	967.34 µw
Slew rate	27 V/µs

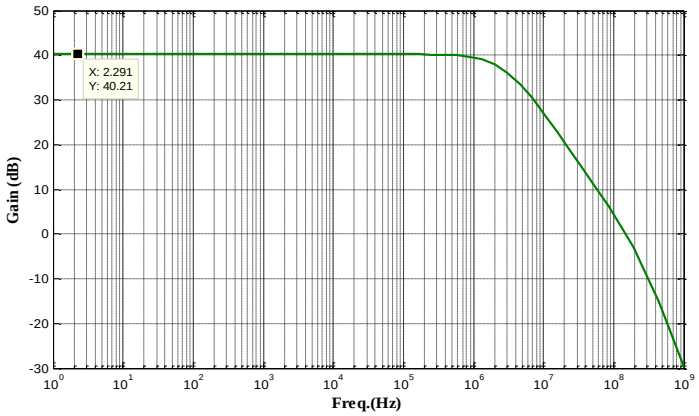

Fig. 4. The operational amplifier frequency response gain.

3.2. Comparator

Based on research by Yao et al. [13], the sigma-delta single bit quantizer is a comparator, which is implemented with an SR Latch. The comparator used to create the quantizer is shown in Fig. 5. Since the sigma-delta modulator has a very high accuracy, hence, the quantizer and consequently the comparator circuit can be designed simply due to the noise shaping nature of the sigma-delta modulator. Since the comparator has a dynamic operation, therefore a slow clock can cause a leakage current to flow through its branches. To solve this problem, one can use low power and high threshold voltage, V_T, transistors. This quantizer is simulated utilizing 180 nm technology and achieves power consumption of 14.4 µW.

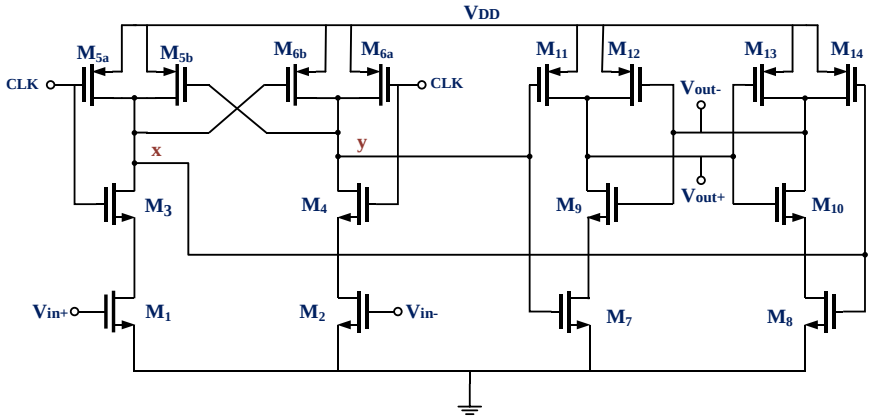

Fig. 5. Dynamic comparator and SR-latch.

The comparator, which is a high-speed positive feedback structure, operates in response to the applied clock pulse. For zero CLK nodes, '*x*' and '*y*' are set to VDD, i.e., the upper supply voltage value. When the CLK is set to logical one, i.e., VDD, the input signals Vin+ and Vin- are compared and the branch (M1, M3 at one side and M2, M4 on the other side) with higher input voltage draw more current and sets the corresponding node '*x*' or '*y*' to zero while the other one becomes VDD.

4. Simulation Results

The system-level sigma-delta modulator is simulated at Matlab Simulink considering sampling frequency of 256 MHz and signal bandwidth of 1 MHz. Circuit level implementations are evaluated by simulating at Cadence software utilizing 180 nm technology and applying 1.8 V supply voltage. Input signal amplitude of the modulator is considered 0.5 V with the frequency of 500 KHz.

With appropriate selection of the optimum coefficients for the modulator, the Signal to Noise and Distortion (SNDR) is simulated to be equal with 74.18 dB, which is equivalent to the 12.02-bit precision as is shown at Fig. 6. For the proposed sigma-delta modulator, the output noise power diagram is obtained using the SIMSIDES utility as shown in Fig. 7, which confirms the correct functionality of the modulator.

In order to evaluate the circuit performance, the time domain output signal for bluetooth application is extracted and is shown in Fig. 8 for one period of the input signal.

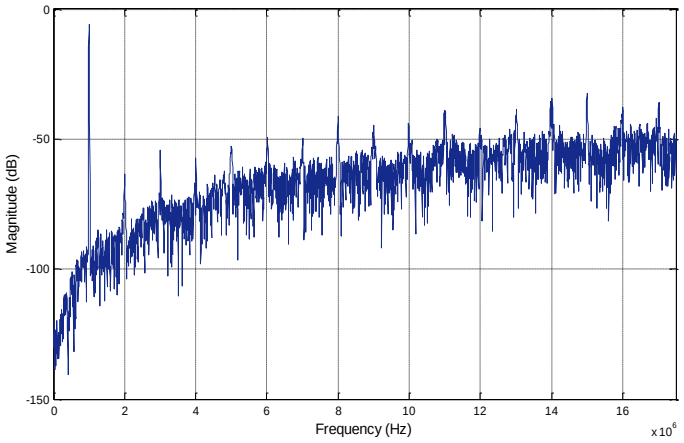

Fig. 6. Measured output spectrum of the sigma-delta modulator.

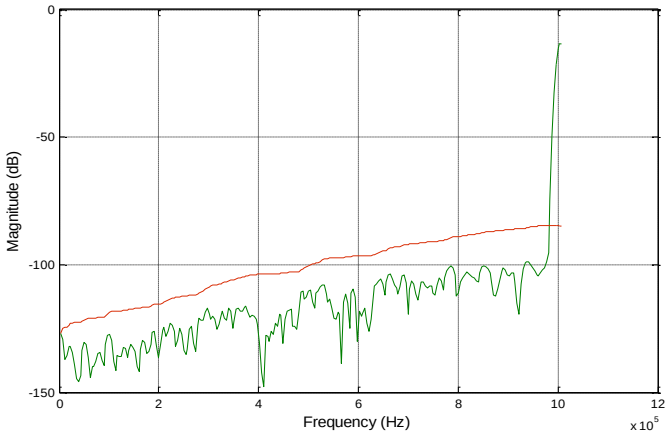

Fig. 7. Measured output power integrated noise.

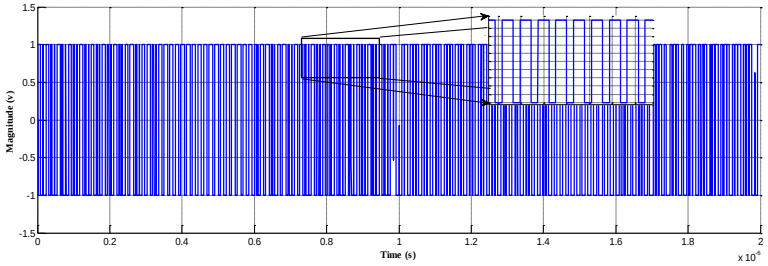

Fig. 8. The time domain output signal for bluetooth application.

Table 2 shows the specifications obtained for the second order modulator and compares the proposed structure with some other artworks. The figure of merit (FoM) of Eq. (6) is considered to compare different structures.

$$\text{FOM} = \frac{P_{total}}{2 \times 2^{ENOB} \times BW} \tag{6}$$

where P_{total} is the overall power consumption, *ENOB* is the effective number of bits, and *BW* is the bandwidth of the modulator. The FOM of the proposed modulator is smaller than other works and this proves its better functionality. In other words, the amount of energy dissipated at the proposed structure to determine each quantized level is less than other works.

Table 2. Performance summary and comparison with other works.

	Current work	[8]	[11]	[14]
Technology (nm)	180	180	180	130
BW (MHz)	1	1	1.5	1
OSR	128	24	-	20
Fs (MHz)	256	48	-	40
SNDR (dB)	74.18	49	53	71
Power (mw)	1.9	1.3	5	2.3
FOM (pJ/conv.)	0.23	4.57	2.83	0.5

5. Conclusion

In this paper, a sigma-delta modulator structure is presented with the appropriate double-code to be utilized in the bluetooth standard. In the system-level structure of the modulator, incorporating a forward path, the unity signal transfer function was obtained. Structures with unity STF have less distortion and hence, can increase the precision of the modulator. At circuit level implementation, optimum performance of the modulator is obtained due to the suitably designed high-performance blocks. The oversampling ratio and signal bandwidth of the proposed modulator was selected to be 128 and 1 MHz, respectively. The signal to noise and distortion ratio (SNDR) of the proposed structure was obtained equal with 74 dB, which presents 12-bit accuracy. The modulator was simulated in 180 nm CMOS TSMC technology at Cadence software applying 1.8 V supply voltage. The power consumption was obtained as low as 1.9 mW, which is very suitable for portable modern ultra-low power applications.

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