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AN EFFICIENT FULLY DIFFERENTIAL VOLTAGE COMPARATOR

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Abstract

With the compactness of the devices, the circuits are required with less delay, less area and less power consumption. An efficient fully digital-in-notion differential voltage comparator with the opamp-less approach is implemented in this paper. This comparator detects a small input voltage difference, i.e., resolution of this comparator is 8-bits and amplifies the output to either of the two different logic levels high or low, i.e., 1 or 0 respectively. Though dynamic latched comparators are quite attractive, they suffer from high power consumption and large offset voltages. In addition to the low power consumption, this comparator is extremely cost-effective as an analogue circuit has been designed digitally and fabricated in a digital process. The comparator is designed and implemented in the Cadence Virtuoso tool using SCL 180 nm Complementary Metal Oxide Semiconductor (CMOS) digital process at a supply of 1.8 V and a load capacitance of 1 pF.

Keywords: Differential circuit, Efficient, Low power, Offset, Voltage comparator.

1. Introduction

With the rapid growth of technology and shrinking the device size, low power is an important parameter in lightweight portable and battery operated devices. To get an enhanced battery life and performance, larger area and weight should be needed [1, 2]. A battery pack is required to store a large amount of energy and be charged in a short amount of time. Therefore, the solar cell can be used for large devices. To reduce the power dissipation either reduce the value of capacitance, which is partially depend on device size or reduce the supply voltage that debases the performance of the circuit. With the reduction in supply voltage, threshold voltage should be reduced. Moreover, as technology scales down it does not have more effect on dynamic power, but it has a great impact on static power dissipation. Therefore, power dissipation has become a critical design metric for a large number of CMOS circuits. As stated by Wicht et al. [3], the exploding market with new lightweight, portable devices, digital ICs have more advantageous than analogue ICs design. Digital IC design focuses on maximizing circuit density, logical correctness and placing circuits so that clock and timing signals are routed efficiently. Analog IC designs are more complex and costly than digital IC design to meet the similar performance constraints [4]. To make the world a digital platform, the analogue design can be re-constructed into digital form.

When the input voltage is compared with the reference voltage, the comparator provides an output logic level 0 or 1 based on the comparison. Typically, comparators are difficult to map out. In static comparator, offset is less, but power consumption is high and speed is low. Contrary to that, dynamic comparators have high input impedance, full-swing output, low power consumption and fast speed. Based on a study by Wicht [5], they are highly appealing for many applications such as flash analogue-to-digital converters (Flash ADCs), window detector, memory sense amplifiers (SAs), relaxation oscillator, level shifter and data receivers.

This paper is arranged as follows. Section 2 describes the different performance metrics of the comparator. Section 3 discusses the Proposed Fully Differential comparator. Simulation results are discussed in Section 4. Section 5 gives concluding remarks and the future scope.

2. Performance Metrics of Comparator

2.1. Power dissipation

According to Kang and Leblebici [6], power dissipation is a crucial design specification for the comparator. When Analog CMOS design circuits are compared with digital CMOS design circuits, Analog CMOS circuit will consume more power.

The total power dissipated in a digitally designed CMOS circuit is specified by the sum of dynamic (or switching) power dissipation (P_{dyn}), short-circuit power dissipation (P_{sh}) and leakage power dissipation (P_{leak}).

$$P_{total} = P_{dyn} + P_{sh} + P_{leak} \quad (1)$$

P_{dyn} is the power dissipated because of switching, which transpire when a node capacitance is charged or discharged, P_{sh} is the power dissipated due to the crowbar current (direct current path or short circuit current) that flows from a supply voltage V_{DD} to lower voltage, i.e., ground potential and P_{leak} is the power dissipated, even

when there is no switching. It plays an important factor in ultra-deep sub-micron technologies. But, it can be easily neglected in the present case of 180 nm technology. Thus, power dissipation, in our case, is mainly due to P_{dyn} and P_{sh}.

2.2. Propagation delay

The comparator basically compares two input signals and changes (trip) the output when one level exceeds other. But, the output cannot be changed at the same instance; there is some delay called propagation delay tells how fast the comparator changes its output according to the input. Delay is there because signal propagates through the internal circuitry. It defines the speed of the comparator. It also deteriorates the ADC performance. As stated by Allen and Holberg [7], propagation delay time is the average time of both rising edge and falling edge propagation delay. The rising propagation delay is given by 50% of rising edge of the input and 50 % of the transition edge of the output signal level and falling propagation delay is given by 50% of falling edge of the input and 50 % of the transition edge of the output signal level [7]. The propagation delay is given by:

$$T_{propagation\ delay} = \frac{T_{rise}+T_{fall}}{2} \quad (2)$$

where T_{rise} is the rising time and T_{fall} is the falling time. During clocked circuit, i.e., comparator's propagation delay can be calculated between the 50% transition points of the clock signal & output signal, i.e., difference of high level and low level (V_{OH}-V_{OL}).

2.3. Offset calculation

The input static offset of the comparator arises from a conflict in same devices. Therefore the comparator may give the random change in the output, i.e., the comparator output may be reversed. The output switches from one logic level to another as soon as the inputs difference becomes zero. If the output does not switch until the inputs difference reaches a value V_{os}, then this difference is termed as the offset voltage as shown in Fig. 1.

This offset voltage poses a problem for circuit designers as it varies randomly from circuit to circuit, and is hard to predict.

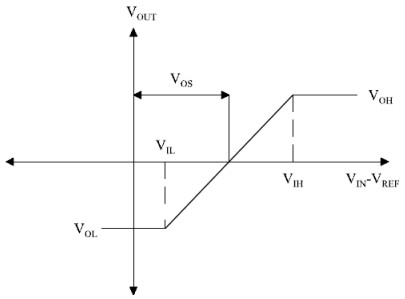


Fig. 1. Transfer curve of a comparator including input offset voltage [8].

2.4. Resolution

The smallest difference in the input voltage, which is identified by a comparator that gives logic 1 or 0 is called resolution. The restricting factors that affect the

resolution are noise and input offset voltage. The minimum resolution that an A/D can have is V_{LSB}. The comparator should be able to determine V_{LSB} that is $1/2^N$ for N bit ADC [7].

3. Proposed Fully MOS based Differential Comparator

A Fully Differential Voltage Comparator schematic is present in Fig. 2. It depends on the concept of the digital-based differential circuit [9], comprises of CMOS-based Inverter and NAND-NOR in the circuit. This comparator is designed, implemented and simulated in Cadence Virtuoso ADE-L using SCL 180 nm CMOS technology. The summer network comprises of the resistors with equal values, which forms a voltage divider. V_{sp} and V_{sn} are the intermediate nodes of the voltage divider and the signal is processed through that node to the outputs. The voltage divider consists of four Transmission gates that act as resistors, the capacitor (C_f) in the feedback block has been replaced by MOSCAP (MOSFET capacitor) [10, 11]. MOSCAPs require less area, offer more capacitance per unit area as compared to MIMCAP (metal insulator metal capacitor), MOMCAP (metal oxide metal capacitor). Summer provides the average of the feedback signal (V_f) and the external inputs (V_{INPUT_P} and V_{INPUT_N}), and such that $V_{sp} = \frac{V_{INPUT\_P}+V_f}{2}$ and $V_{sn} = \frac{V_{INPUT\_N}+V_f}{2}$. All inverters used in this circuit are symmetric such that their switching threshold voltage (V_{th})=$\frac{V_{DD}}{2}$ And Buffers are made up of two inverters, which are in series. These voltages (V_{sp} and V_{sn}) are passed from buffers to get O_P and O_N , which are the digital inputs of the circuit. Thus, O_P and O_N are compared and the correct output is obtained, eventually. The feedback block comprises of M13-M14 transistors, loaded by a capacitor C_f.

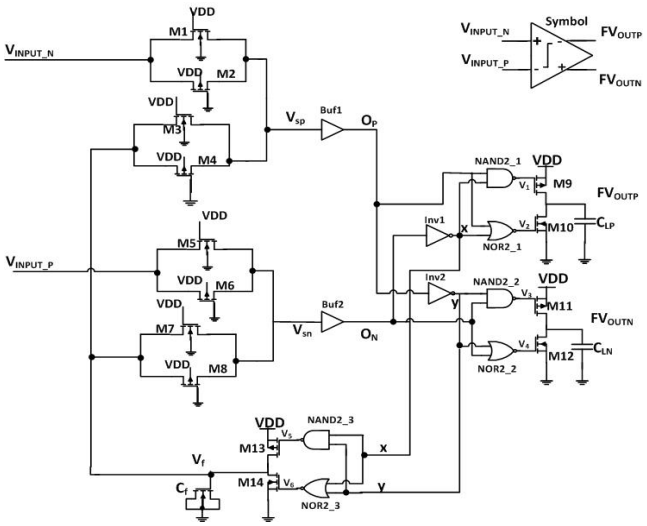


Fig. 2. A proposed digital-based differential NAND-NOR based comparator.

Thus, when the input voltages, V_{INPUT_P} and V_{INPUT_N} are less than V_{th}, then M13 transistor turns on to increase V_f and when both V_{INPUT_P} and V_{INPUT_N} are greater than V_{th}, then M10 transistor is turned on to decrease V_f. This is done to

obtain V_f in such a range that after adding up, it leads to distinguishable values of the digital inputs (O_P and O_N), of the circuit. In these two cases, the output transistors are off, until comparable digital inputs are obtained through a feedback mechanism. And as soon as valid digital inputs are obtained, correct outputs are provided by the output stage. In the case of different input voltages, V_f, the signal is not required, hence, feedback block is in off condition and the transistors present at the output stage (M9-M12) are on accordingly, to provide correct outputs.

Considering the case of differential inputs, let V_{INPUT_P} be higher than V_{INPUT_N} , once V_{sn} and V_{sp} cross the V_{th} of the buffers BUF1 and BUF2, respectively, O_P rises to logic '1' and O_P decreases to logic '0'. Thus, M9 transistor turns on and M10 transistor turns off. Therefore, FV_{OUTP} becomes '1' and FV_{OUTN} becomes '0'. Similarly, when V_{INPUT_P} decreases and V_{INPUT_N} rises, FV_{OUTP} becomes '0' and FV_{OUTN} becomes '1'.

As compared to by Crovetti [9], here, the two output signals FV_{OUTP} and FV_{OUTN} have been derived as fully differential circuits have certain benefits over single-ended circuits like, error subtraction, larger output swings, rejection of common-mode noise, a high closed-loop speed, etc. [12]. However, usually, all this is achieved at the cost of large power requirements [13, 14], which is quite low here. Another advantage of the proposed circuit is the use of universal NAND-NOR gates in the design.

4. Simulation Results

The schematic of proposed voltage comparator has been designed using Cadence Virtuoso and then implemented and simulated in ADE-L using SCL 180 nm CMOS digital process technology.

4.1. Transient response

To observe the transient response of the comparator, V_{INPUT_N} & V_{INPUT_P} were set at 0.9 V common mode level (V_{in_cm}) and at an amplitude (ΔV_{in}) of 0.2 V. The various intermediate voltages and final output voltages were observed as shown in Fig. 3. Thus, it is evident from Fig. 3 that in case of differential inputs V_f remains in the range of V_{th}.

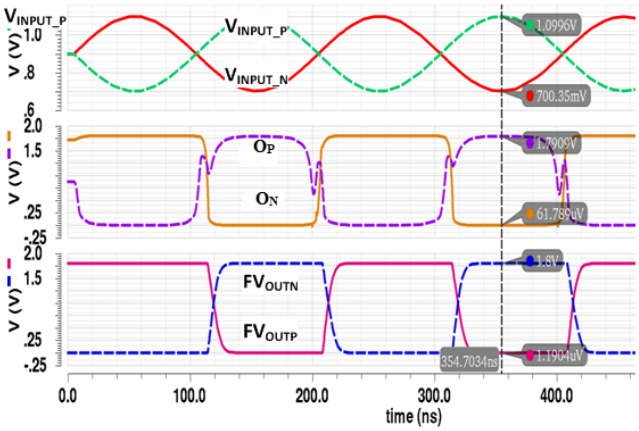


Fig. 3. Transient analysis of transmission-gate based comparator.

4.2. Delay analysis

The critical path from input to output can be observed in the path from V_{INPUT_P} to FV_{OUTN} and V_{INPUT_N} to FV_{OUTP} node or it can also be called as the worst-case delay. It includes the delay elements as follows: delay from input V_{INPUT_P} to V_{sp} The node is due to RC_{sp} value offered by the transmission gate where C_{sp} is the parasitic capacitance at V_{sp} node, which is mostly due to the capacitance present at the input side of buffer Buf1. Next, delay from V_{sp} to O_P node and the delay from O_P node to final output. Hence, the total delays from V_{INPUT_P} to FV_{OUTN} is approximately 10ns. A similar propagation delay analysis can be done for the path from V_{INPUT_N} to FV_{OUTP}. According to Wicht et al. [3], variation in propagation delay of the proposed comparator with change in differential input voltage (ΔV_{in}) can be observed in Fig. 4. Where V_{in_cm} is at 0.9 V. The delay is reducing with the increase in input voltage amplitude (V_P). The reason is less time consumption, by the feedback block, to bring digital inputs at two different logic levels. When the input voltage amplitude (ΔV_{in}) is 0.2 V, delay is 10.04 ns approximately.

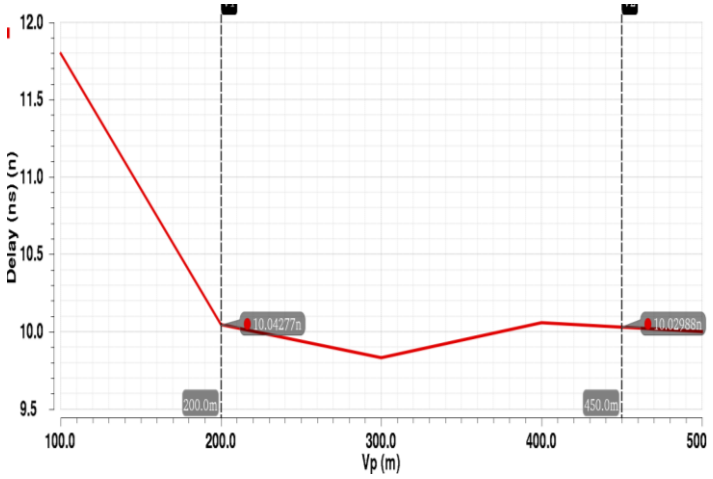


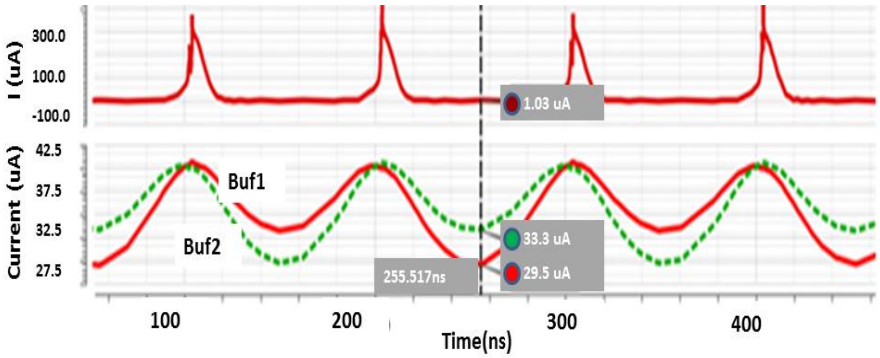
Fig. 4. Propagation delay response to changes in input amplitude.

4.3. Power measurement

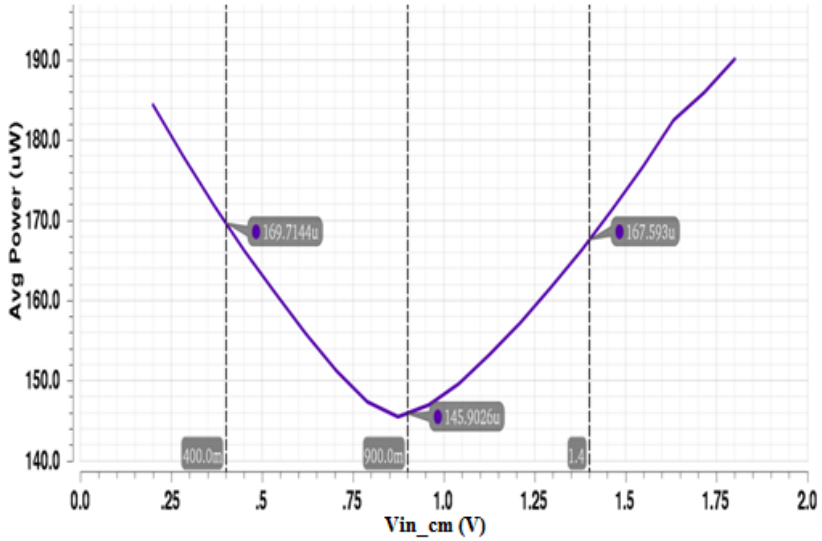
The current flowing through the Buf1 and Buf2 is shown in Fig. 5(a) and the current flow through the rest of the circuit be I. It is observed that 32 µA current is flowing through buffers all the time. While I can be observed during switching only. Almost all the circuit power is consumed by buffers because V_{sp} and V_{sn} are in the range of V_{th}, which turns on the transistors of buf1 and buf2 resulting static current through them. Hence, the circuit current is negligible, which proves that, the digital-based CMOS circuits consume very low power. Average power dissipated by the proposed comparator was measured to be 150.018 µW

Variation in average power dissipation with the change in common mode voltage (V_{in_cm}) can be observed in Fig. 5(b). The input voltage amplitude (ΔV_{in}) has been set at 400 mV. This shows that a minimal value is obtained near V_{in_cm} =

0.9 V and the average power increases whenever there is a variation in either side of this minimal.



(a) Various voltage and current waveforms.



(b) Variation of average power dissipation with input common mode voltage (V_{in_cm}).

Fig. 5. Power and current analysis of the proposed comparator.

4.4. DC analysis

From DC analysis of the proposed comparator as shown in Fig. 6 where V_{INPUT_N} is reference voltage and V_{INPUT_P} is the ramp signal, differential outputs FV_{OUTP} and FV_{OUTN} are obtained accordingly. With the reference to Fig. 7, the offset voltage was measured as 4.83 mV. Output voltage is supposed to reach 0.5 V_{DD} at the DC bias applied at the input. However, instead of switching at 0.5 V_{DD}, output switched at some other voltage, this difference is referred to be the offset voltage. Here too, 0.9 V was applied as DC bias to the input. Instead of switching at 0.9 V, FV_{OUTP} switched at 904.833 mV. This leads to an offset voltage of 4.833 mV and its ICMR fully supply range, i.e., is up to 1.8 V.

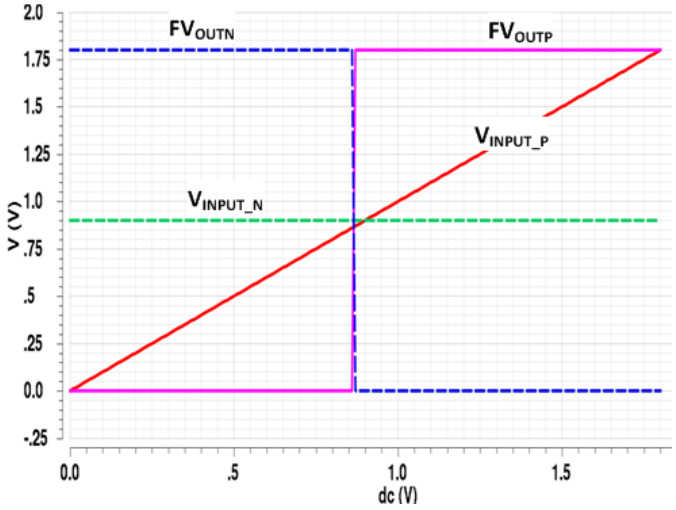


Fig. 6. DC analysis of transmission-gate based comparator.

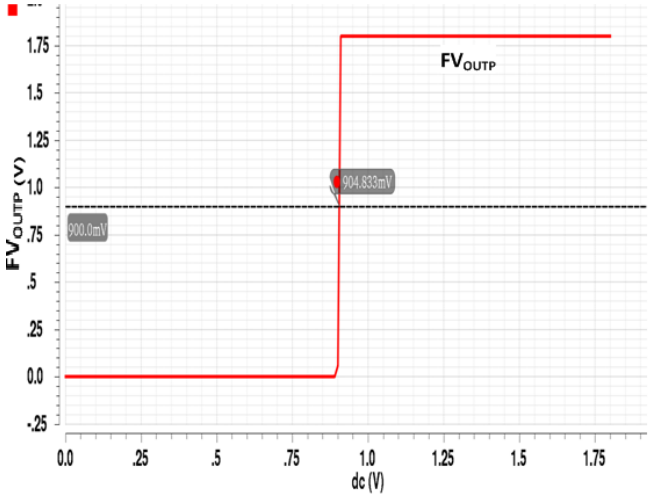


Fig. 7. Offset voltage of the transmission-gate based comparator.

A digital-in-concept implementation technique has been presented to design efficient fully differential voltage comparators. This is highly cost-effective as the digital-domain design is less tedious and time-consuming as compared to pure analogue implementations. The volunteered comparators are acceptable for SAR ADCs [15-17], pipelined ADCs [18], low-power ADCs [19], LED driver [20], etc.

Table 1 shows that the proposed comparators have better values of all the parameters. With the load capacitance of 1 pF, the comparator was simulated. In analogue comparator, with the scaling of supply voltage performance degrades. But this digital based comparator adds good trade-off between power dissipation and

delay, with the scaling technology, these digital comparators further design for low power application.

Table 1. Comparison of comparator characteristics.

Parameter	[21]	[22]	[23]	[24]	
Design methodology	**Analog**	**Switched capacitor used in clocked comparator**	**Dynamic dual tail comparator**	**Current mode**	**Fully digital**
CMOS technology (µm)	0.5	0.8	0.18	0.18	0.18
Supply voltage (V)	1	5	1.2	1.8	1.8
Offset voltage (mV)	-	77.3	7.8	-	4.83
Average power dissipation (µW)		800	329	158	150.014
Delay	4 µs	17.3 ns	550 ps	0.4 ns	10.0 4 ns

5. Conclusions

In this paper, an efficient of a fully differential voltage comparator with low power, low offset voltage and less delay is designed. This comparator based on digital NAND and NOR gates with some pass transistor. This concept is used for the reduction of power dissipation and offset voltage.

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Nomenclatures

FV_{out}	Final output
M	MOSFET
P_{dyn}	Dynamic power dissipation
P_{leak}	Leakage power dissipation
P_{sh}	Short-circuit power dissipation
T_{fall}	Falling time
T_{rise}	Rising time
V_f	Feedback signal
V_{in_cm}	Common mode level
V_{INPUT_N}	Positive input voltage (V)
V_{INPUT_P}	Negative input voltage (V)
V_{th}	Threshold voltage

Abbreviations

ADE	Analog Design Environments
CMOS	Complementary Metal Oxide Semiconductor
SCL	Semi-Conductor Laboratory

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