Analysis of BD MOS and DT MOS Current Mirrors in 130 nm CMOS Technology

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Abstract. *In this paper, an analysis of basic Current Mirror (CM) topologies was performed with a focus on comparison of conventional realization to Bulk-Driven (BD) and Dynamic-Threshold (DT) equivalents, in terms of main properties. These circuits were designed in 130 nm CMOS technology using the supply voltage of 0.6 V and laid out on a test-chip. Fabricated circuits were analyzed and their characteristics compared to the simulation results. The achieved results prove that these unconventional circuit design techniques are quite promising for contemporary ultra low-voltage analog Integrated Circuits (ICs).*

Keywords

Analog circuits, bulk-driven, current mirrors, dynamic-threshold, low-voltage circuits.

1. Introduction and Background

Nowadays, lot of research effort has been encouraged to develop design techniques for low-voltage analog ICs in standard CMOS process in order to avoid circuits to be the limiting factor of the power supply voltage downscaling. Design of low-voltage analog ICs is rather difficult challenge taking into account today's customer requirements and technology parameter fluctuations. Reducing the transistor channel length into sub-micron size as well as continuous shrinking of the gate-oxide thickness down to a few nanometers cause low breakdown voltages of MOS transistors [1]. The power supply voltage (V_{DD}) downscales in a similar fashion with the reduction of the transistor channel length L over the years, as can be observed in Fig. 1. Otherwise, the robustness and reliability of devices would deteriorate due to hot electron effect and time-dependent dielectric breakdown. However, unlike the shrinking of the power supply voltage, the threshold voltage V_{TH} reduces much less aggressively to maintain ON/OFF characteristics of MOS transistors [2]. It is known that better circuit performance can be achieved using BiCMOS technology however, at higher costs. Therefore, advanced design techniques for standard CMOS technology have been developed over the years to compete with BiCMOS technology and reduce the total IC fabrication costs.

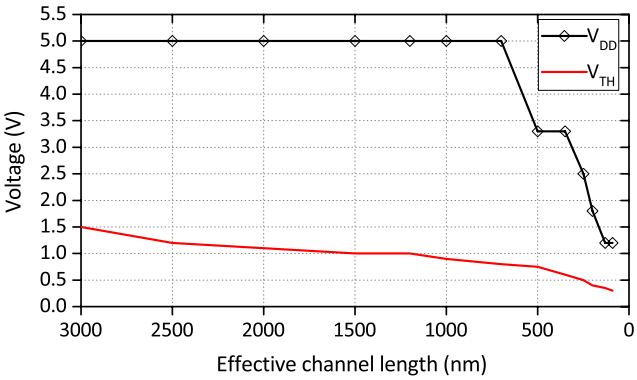


Fig. 1: V_{DD} and V_{TH} versus MOS transistor downscaling [2].

There are several design techniques that have been developed for low-voltage analog IC design [3]. The most used ones include:

- floating-gate MOS transistors,
- self-cascode topologies,
- level shifters,
- MOS transistor operating in sub-threshold region,
- BD MOS transistors,
- DT MOS transistors,

The most suitable design approaches for the selected 130 nm standard CMOS technology include techniques using MOS transistor operating in the sub-threshold region, BD, and DT MOS transistors.

In this paper, the BD MOS and the DT MOS transistors are analyzed and evaluated. Then, these design techniques are applied to basic IC building blocks and achieved results are compared.

2. BD MOS Transistor

In a MOS transistor, drain current I_D is usually controlled by the gate-source voltage V_{GS}. Bulk-source voltage V_{BS} can also affect this current, which is usually considered as a parasitic effect that may introduce undesired body transconductance g_{mb} [4]. Nevertheless, if a constant value of V_{GS} is kept as a bias voltage and the input signal is applied to the bulk terminal, a JFET-like transistor can be obtained [5]. Schematic diagram of a BD transistor is shown in Fig. 2. The main idea behind the BD design technique is in the structure of the MOSFET, where the bulk terminal is used as the signal input. In such a configuration, the transistor threshold voltage can be reduced with no modifications of the MOSFET structure or technology process.

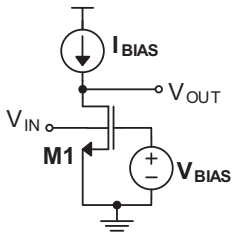


Fig. 2: BD MOS transistor.

Body transconductance g_{mb} is the second-order effect of a MOS transistor. It represents gain of a voltage-controlled current source, which is controlled by V_{BS} and situated between drain and source terminals in well-known MOS transistor equivalent circuit shown in Fig. 3. The body transconductance of the MOS device can be expressed by

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{-2\phi_F - V_{BS}}}, \tag{1}$$

where g_m is the transconductance of the conventional Gate-Driven (GD) MOS transistor in (S), γ is the body effect constant in $\left(\mathrm{V}^{1/2}\right)$, ϕ_F is the bulk Fermi potential in (V).

The body transconductance can be also expressed by the ratio η (Eq. (2)) which ranges from 0.2 to 0.4, depending on the V_{BS} value and specific process parameters [6].

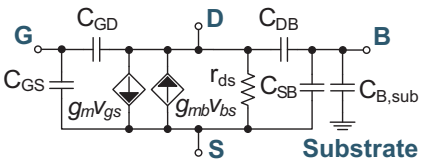


Fig. 3: Equivalent circuit of BD MOS transistor.

$$\eta = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{-2\phi_F - V_{BS}}} = n - 1 = \frac{C_{dep}}{C_{ox}}, \tag{2}$$

where C_{dep} is the capacitance of the depletion layer beneath the gate in (F), and C_{ox} is the capacitance of the oxide beneath the gate in (F).

Using g_{mb} transconductance instead of g_m decreases the overall device transconductance and increases the input capacitance, which is from 3 to 5 times larger than the input capacitance of a GD MOS transistor [7]. This can lead to lower Gain Band-Width (GBW) and worse frequency response $f_{t(BD)}$ in comparison to the transit frequency $f_{t(GD)}$ of a conventional GD MOS device. The transit frequency for the BD MOS transistor and the GD MOS device is expressed in Eq. (3) and Eq. (4), respectively.

$$f_{t(BD)} = \frac{g_{mb}}{2\pi(C_{SB} + C_{DB} + C_{B,sub})}, \tag{3}$$

$$f_{t(GD)} = \frac{g_m}{2\pi C_{GS}}, \tag{4}$$

where C_{SB}, C_{DB}, C_{GS} are capacitances between the MOS transistor terminals and $C_{B,sub}$ is the capacitance between the bulk and the substrate.

Moreover, the BD technique increases the thermal noise of MOS transistors and increases a risk in turning on parasitic bipolar transistors that might lead to latch-up [8]. A MOSFET driven through the well (bulk) increases the risk of turning on a parasitic diode between the source and bulk, as illustrated in general and simplified CMOS technology structure cross-sections without deep trench insulation (Fig. 4). In NMOS transistor, if the bulk-source voltage reaches a value greater than the built-in barrier potential of the PN junction, a leakage current starts flowing from the well to ground. The same principle can be applied for PMOS transistor. Thus, an action must be taken to prevent this effect – the supply voltage is limited to the value lower than the barrier potential of the PN junction between these terminals. Unfortunately, a sub-threshold current will still flow through this barrier [9]. Another effective technique to reduce the leakage current and the risk of triggering the latch-up effect is using the guarding rings created from N-wells and P-wells between individual transistors. Connecting N-wells to the positive supply voltage and P-wells to the negative supply voltage or ground creates reverse-polarized

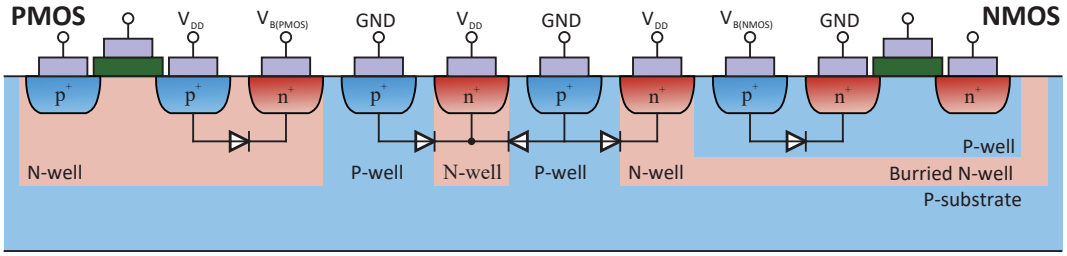


Fig. 4: Cross-section of a CMOS structure with parasitic devices.

diodes between NMOS and PMOS transistors, which effectively prevents the latch-up.

On the other hand, the main advantage of the BD technique is its compatibility with a standard CMOS process, since there is no need for modification of the structure or technology. Another benefit is improving the Input Common-Mode Range (ICMR) which can result in full rail-to-rail IMCR [10] topologies. At the same time, the BD technique decreases the need to overcome the threshold voltage at the input of a MOS transistor which increases the voltage swing in the signal path [11]. This can be expressed by the following formula

$$V_{TH} = V_{T0} + \gamma(\sqrt{|2\phi_F| - V_{BS}} - \sqrt{|2\phi_F|}), \quad (5)$$

where V_{T0} is the threshold voltage of a MOS transistor for $V_{BS} = 0$ V. Lowering the threshold voltage allows the decrease of the power supply voltage.

3. DT MOS Transistor

The DT design technique is similar to the BD technique in terms of the modulation of drain current by the bulk. However, instead of using the bulk alone as a signal input, DT MOS transistors have the bulk tight together with the gate terminal. As a result, voltages V_{BS} and V_{GS} are changed simultaneously ($V_{BS} = V_{GS}$) with the input signal swing and hence, the threshold voltage is changed dynamically, as can be noticed from Eq. (5). DT MOS transistor then requires lower current for its operation and has lower noise in comparison to the conventional GD MOS transistor [12]. The advantage of this technique is higher total transconductance g_{mbs} (Eq. (6)) and faster current transfer.

$$g_{mbs} = g_m + g_{mb} \quad (6)$$

The input capacitance and the maximum transit frequency change to value given by

$$f_{t(DT)} = \frac{g_m + g_{mb}}{2\pi C_{GD} + C_{GS} + C_{BS} + C_{BS}}. \quad (7)$$

Schematic diagram and small-signal equivalent circuits of the DT MOS transistor are depicted in Fig. 5.

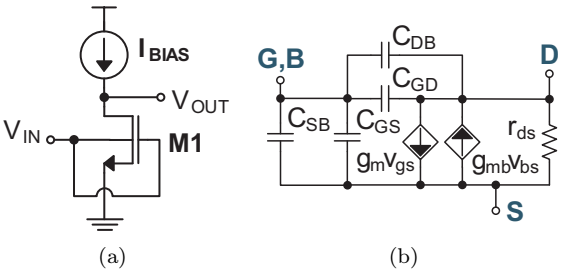


Fig. 5: DT MOS transistor: (a) schematic and (b) small-signal equivalent circuit.

4. Simulation Setup

In our research, three topologies of CMs designed using the above mentioned techniques are analyzed and compared in terms of the main parameters and features. Simulations of CM circuits were conducted for a standard 130 nm CMOS technology. Dimensions of transistors were $L = 2$ µm and $W = 6$ µm for a simple CM, and $W = 14$ µm for improved Wilson and cascode CMs. Different MOS transistor widths ensure the operation of all proposed BD CMs in the same range of operating currents around $I_{REF} = 10$ µA. Figure 6(a) and Fig. 6(b) show a simple CM designed using standard GD and BD techniques, respectively. In the BD CM, gates of both transistors are biased by the V_{BIAS} voltage of 300 mV. The minimum output voltage of a CM is the value of the output voltage representing the lower limit of the voltage headroom (the upper limit is the positive supply rail). In general, it is the point, where CM starts mirroring the input current to the output branch with a certain accuracy. The

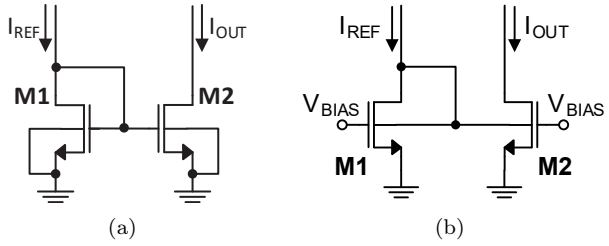


Fig. 6: Simple CM (a) standard GD and (b) BD version.

minimum output voltage $V_{MIN} = V_{DS,sat}$ of a simple CM does not depend on the threshold voltage V_{TH} or transconductance and thus, the output characteristics and the output resistance $r_{out} = r_{ds}$ of both version of a simple CM should be similar [13].

Using the BD technique, the improved Wilson and cascode CMs were designed. The improved Wilson CM and cascode CM in BD topology are depicted in Fig. 7(a) and Fig. 7(b), respectively. Since the minimum output voltage (Eq. (8)) of these CMs depends on the threshold voltage:

$$V_{MIN} = V_{TH} + 2V_{DS,sat}, \tag{8}$$

there will be differences in the output characteristics between GD and BD equivalents. The output resistance of the improved Wilson and cascode CMs [14] can be expressed as:

$$r_{out} = g_m r_{ds}^2. \tag{9}$$

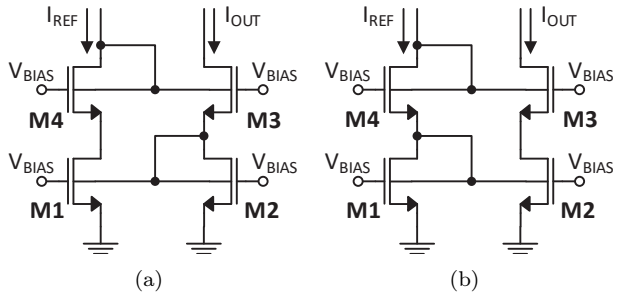


Fig. 7: BD CMs: (a) improved Wilson and (b) cascode.

DT equivalents of the mentioned CMs were designed and analyzed, too. Simple and cascode CMs are depicted in Fig. 8(a) and Fig. 8(b), respectively.

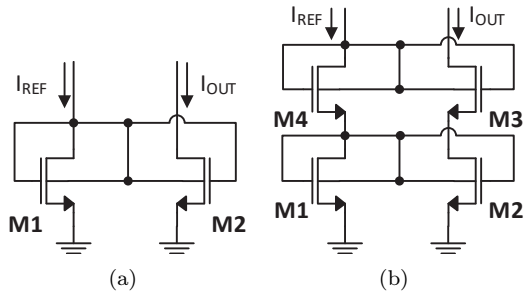
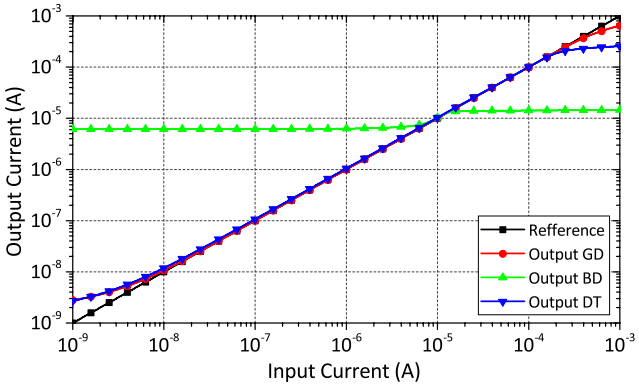
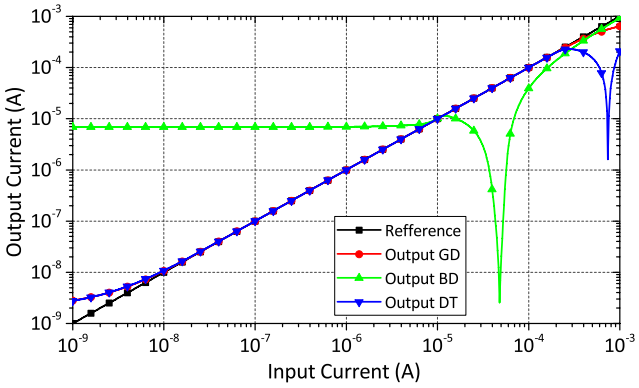


Fig. 8: DT CMs: (a) simple and (b) cascode.

Simulations of transfer characteristics show the big advantage of the DT CMs. From Fig. 9(a) and Fig. 9(b), one can observe that the DT CMs have the operation range similar to their standard GD equivalents, where a wide range of operating currents is achieved. On the other hand, BD CMs can operate accurately only in a narrow range of operating currents. For operation in a different range, sizing and biasing conditions have to be tuned. Other solution is to use other advanced topologies of BD CMs with the negative feedback for gate biasing [15]. The notches in Fig. 9(b) are caused by the ideal current source used in simulations, which open the bulk-drain diode in the CM output branch. Consequently, an input current can flow through this diode to the voltage source which supplies the output branch. Actually, in the linear scale, this current would have the negative value but because of the logarithmic scale, there are absolute values of currents.



(a) Transfer characteristics of simple CMs.



(b) Transfer characteristics of cascode CMs.

Fig. 9: Transfer characteristics of: (a) simple CMs and (b) cascode CMs.

5. Experimental Results

After simulations, the proposed CMs were laid out on an ASIC test chip. On the chip, there are overall 8 CM test structures including BD and DT topologies. Unfortunately, the number of probe pads for physical measurement on a probe station was the main limiting factor for the total number of CMs implemented on the chip. After considering the simulation results, we chose to implement the simple, the improved Wilson, and the cascode BD CMs as well as simple and cascode DT CMs. These structures were then fabricated, measured and characterized.

Simple GD and BD CMs have similar overlapping output characteristics, as already mentioned above. It means that the simple GD CM is suitable for design of low-voltage ICs but its drawback is in the low output resistance (in order of hundreds kΩ). Simulated and measured output characteristics are depicted in Fig. 10. Poor output resistance can be observed in the slope of the output characteristics for $V_{OUT} > V_{MIN}$, which is not fully horizontal as the reference current is. Measured characteristics show even lower output resistance with similar V_{MIN} compared to the simulation results.

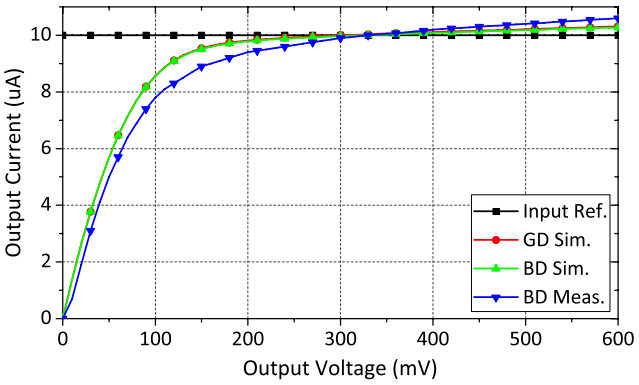


Fig. 10: Output characteristics of simple BD CM.

The improved Wilson CM can enhance the output impedance by introducing the negative serial feedback added to the circuit. From Fig. 11, one can observe that BD technique reduces the V_{MIN} voltage from 300 mV to approximately 120 mV, which is similar to the simple CM but with much higher output resistance (order of MΩ).

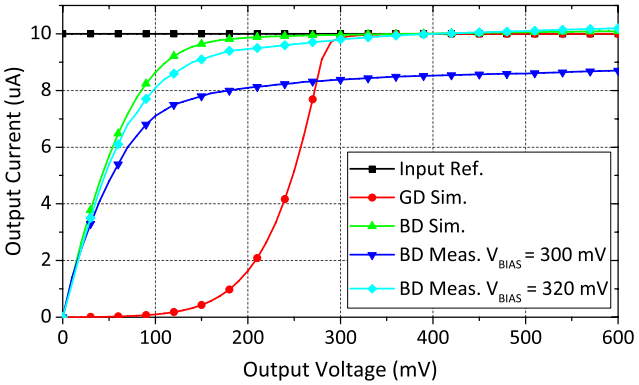


Fig. 11: Output characteristics of improved Wilson BD CM.

Similar situation is with the cascode BD CM (Fig. 12). The minimum output voltage is significantly reduced using BD technique to the value of 150 mV. Measurements of both topologies proved the simulated results with a small inaccuracy. Thus, DC biasing conditions had to be slightly modified from 300 mV to 320 mV to achieve the required CM accuracy.

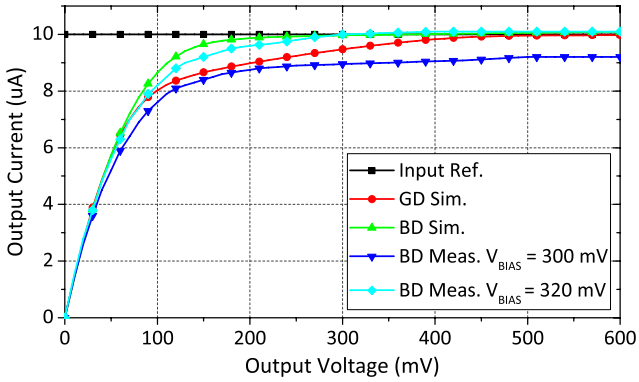


Fig. 12: Output characteristics of cascode BD CM.

DT CMs behave similar to their BD equivalents in terms of the output characteristics (Fig. 13). Their main advantage is that there is no need for gate biasing, so the designer does not need to look for a proper voltage source in the chip or external bias. Cascode DT CM exhibits the same performance as its BD equivalent (Fig. 14). The minimum output voltage is again reduced to the value of 150 mV.

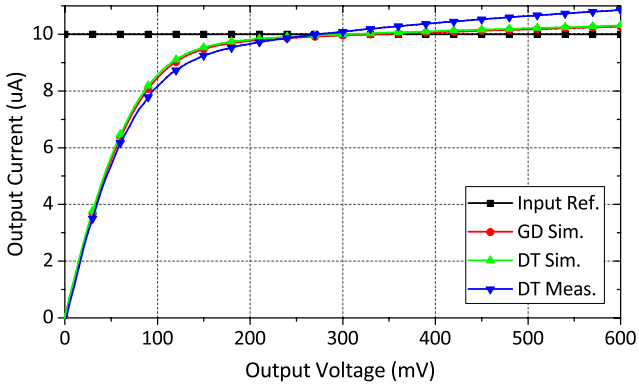


Fig. 13: Output characteristics of simple DT CM.

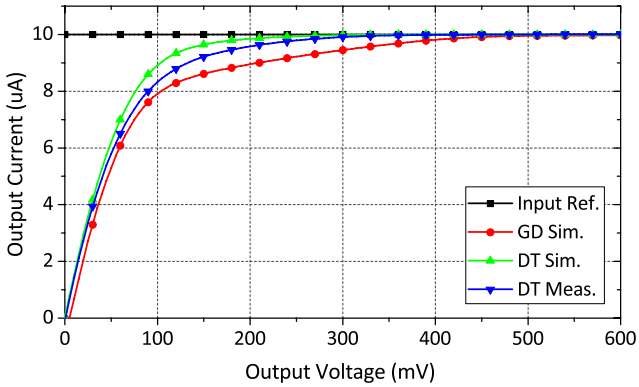


Fig. 14: Output characteristics of cascode DT CM.

Table 1 summarizes minimum output voltages V_{MIN} obtained by simulation and measurements of three CM topologies designed using three different techniques. The presented results prove the importance of the pro-

Tab. 1: Minimum output voltage of proposed CMs in (mV).

CM Topology	GD	BD			DT	
	sim.	sim.	meas. 300 mV	meas. 320 mV	sim.	meas.
simple	118	124	109	-	112	101
improved Wilson	286	131	97	137	264	-
cascode	372	131	127	162	96	98

Tab. 2: Output resistance of proposed CMs in (MΩ).

CM Topology	GD	BD			DT	
	sim.	sim.	meas. 300 mV	meas. 320 mV	sim.	meas.
simple	0.8	0.82	0.34	-	0.85	0.34
improved Wilson	2.17	1.18	1.17	1.01	2.62	-
cascode	2.21	1.18	1.2	1.05	2.83	1.82

posed design techniques for (ultra) low-voltage IC design.

Table 2 summarizes output resistances (r_{out}) of the proposed CM topologies obtained by simulation and measurements. The presented values are calculated from simulated and measured output characteristics, and the precision is strongly influenced by the number of digits of measurement equipment. The presented results show that the output resistance is lower for CM designed using the BD technique because of considering g_{mb} instead of g_m. On the other hand, the cascode and improved Wilson topologies have higher output resistance compared to the simple GD mirror. Output resistance of DT CMs is similar to their GD equivalents.

Furthermore, it has been figured out that the body diode of used device models is very badly modelled, which could be the reason of inaccuracy of simulations that do not represent the real behavior of MOS transistors with bulk used as the signal input.

6. Conclusion

Three different BD CM topologies were analyzed, fabricated, characterized and compared in a standard 130 nm CMOS technology. Simulation results show that the BD and DT techniques can reduce the minimum output voltage of the improved Wilson and the cascode CM down to 30% with respect to the GD equivalent topology. This techniques may eliminate limitations associated with the threshold voltage and thereby reduce the supply voltage value required by the circuit or system. Measurement evaluation of the prototyped chips uncovered that the accuracy of simulation models is lower when BD transistors are used. That is why DC biasing conditions had to be slightly modified during the measurements. The research carried out and the results presented in this paper have proven that the BD technique could be the approach to design low-voltage analog ICs usable mainly in battery-operated portable applications.

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Viera STOPJAKOVA received the M.Sc. degree and the Ph.D. degree in Electronics from Slovak University of Technology in Bratislava, Slovak Republic, in 1992 and 1997, respectively. Currently, she is a full-time professor at the Institute of Electronics and Photonics of the same university. She has been involved in several EU funded research projects under different funding schemes such as TEMPUS, ESPRIT, Copernicus, FP, H2020, etc. She has published over 200 papers in scientific journals and in proceedings of international conferences. She is a co-inventor of two US patents in the field of on-chip supply current testing. Her main research interests include ASIC design and test, on-chip testing, ultra low-voltage analog circuits, energy harvesting, smart sensors and biomedical monitoring.

Daniel ARBET received the M.Sc. degree and the Ph.D. degree in Electronics from Slovak University of Technology in Bratislava, Slovak Republic in 2009 and 2013, respectively. Since 2013 he has been a researcher at the Institute of Electronics and Photonics of Slovak University of Technology. He has published more than 50 scientific papers. His main research interests are ultra low-voltage and low-power analog design, on-chip parametric testing, analog BIST and test implementation.