A Form of List Viterbi Algorithm for Decoding Convolutional Codes

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Abstract

Viterbi algorithm is a maximum likelihood decoding algorithm. It is used to decode convolutional code in several wireless communication systems, including Wi-Fi. The standard Viterbi algorithm gives just one decoded output, which may be correct or incorrect. Incorrect packets are normally discarded thereby necessitating retransmission and hence resulting in considerable energy loss and delay. Some real-time applications such as Voice over Internet Protocol (VoIP) telephony do not tolerate excessive delay. This makes the conventional Viterbi decoding strategy sub-optimal. In this regard, a modified approach, which involves a form of List Viterbi for decoding the convolutional code is investigated. The technique employed combines the bit-error correction capabilities of both the Viterbi algorithm and the Cyclic Redundancy Check (CRC) procedures. It first uses a form of 'List Viterbi Algorithm' (LVA), which generates a list of possible decoded output candidates after the trellis search. The CRC check is then used to determine the presence of correct outcome. Results of experiments conducted using simulation shows considerable improvement in bit-error performance when compared to classical approach.

Keywords. Viterbi Algorithm, List Viterbi, Error Correction, Convolutional Codes, Cyclic Redundancy Check

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1. Introduction

The Viterbi algorithm was proposed by A. Viterbi in 1967 as a method of decoding the convolutional code. It is sometimes called trellis decoding because it uses a trellis to find a message with minimum "hamming distance" or "Euclidean distance". Aside from the field of communication, the Viterbi algorithm has been employed in various other applications such as speech recognition, speech synthesis, bioinformatics, keyword spotting and computational linguistics.

Over the years, the Viterbi algorithm has become widely known as the best algorithm to decode convolutional code in wireless communication systems (Lin and Costello 2004). The classical Viterbi decoding algorithm normally used decode incorrectly and the receiver discards the decoded output if it is corrupted and request for retransmission using Automatic Repeat Request (ARQ) (Wang and Luo 2018). Energy is considerably lost due to the frequent re-transmission and causes the delay in some real-time applications in communication systems.

Portable powered mobile communication devices are component of the nomadic computing system. They have limited battery life available to perform communications over a wireless channel. To improve spectral efficiency and achieve energy saving, energy efficient bit-error

control technique over the wireless link is needed. Therefore, error-detection and correction codes are normally employed to solve the bit-error problem (Gupta and Verma 2012).

The communication system such as cellular phones and cable modems use concatenated codes to perform error correction (Forney 1965). Concatenated codes are error correcting codes that use two or more simple codes before transmitting a signal. The concatenation increases the system performance. Convolutional codes and cyclic redundancy code (CRC) are concatenated together in many wireless communications system such as IS-95 system (Wang, Zhao, and Giannakis 2008). The conceptual block diagram of these two codes is depicted in Figure 1 below:

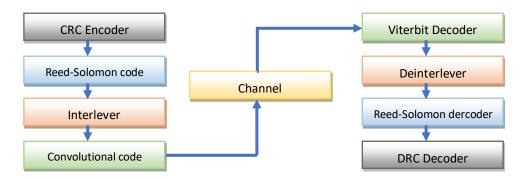


Figure 1: Example of concatenation of three codes: CRC code, Reed-Solomon code and convolutional encoder

Figure 1 shows three different concatenated codes which are CRC, Reed Solomon and Convolutional Code. It uses the CRC encoder for error detection as outside code, the Reed Solomon code as the middle code and finally the convolutional code as the inner code. The interleaver block between the Reed Solomon code and convolutional code helps to spread out any burst error if it occurs.

Error correction and detection decoder are formed by initial application of the "Viterbi Algorithm" to decode the convolutionally encoded message and then the application of the "CRC" to detect an error after decoding (Chen and Sundberg 2000). The classical "Viterbi decoder" tries to correct any bit-errors and produce just one decoded output-which may be correct or incorrect. It uses the outer CRC code to check for correctness of the output of the decoder. If the decoded sequence fails to pass CRC checks then the output of the Viterbi decoder is discarded and retransmission is requested. With this conventional method, which is also a feature of the IEEE 802.11 protocol, retransmissions add to traffic congestion, increase collision probability and introduce transmission delay. Hence, they decrease the performance of the network.

Several researches have employed the use of List Viterbi, Wei et al. (2013), Rota, Bergamaschi, and Guerra (2011), and Thomos et al. (2002). The early idea of the list decoding was proposed independently by Elias (1957) and Wozencraft (1957). It is an approach of decoding which the decoder generates a list of the codeword as a probable result. The approach is successful if one of the codewords in the list corresponds to the original message.

In another study, Sadowsky (1997) stated that list Viterbi algorithm has been applied for decoding turbo codes. Algorithms for generating a list of the maximum possible sequence through trellis has been proposed in Seshadri and Sundberg (1994) and Nill and Sundberg (1995). The list Viterbi algorithm can be either serial or parallel. A parallel list Viterbi generates best possible sequence simultaneously while the serial generates best possible sequence recursively based on the previous best paths (Chen and Sundberg 2000).

This paper aims to improve the bit-error performance of "convolutional coding" of CRC protected data by using a proposed form of "List Viterbi" algorithm. The paper presents a form of "List-Viterbi" decoder, which instead of just one output, it produces a list of eight possible different outputs sequences. It is then possible to use the CRCs to check all of the eight outputs to find a correctly decoded sequence. The technique provides better bit-error correction capability than the conventional "Viterbi algorithm".

The remaining part of the paper proceeds as follows: Section 2 highlights the Implementation of the proposed algorithm. The paper concludes in Section 3 and 4, which detail the results, discussion and conclusion.

2. Implementation of the Proposed Form of List Viterbi Algorithm

List Viterbi algorithm could be implemented using either the Register Exchange Mechanism or the TraceBack Mechanism (Gupta and Verma 2012). In the register exchange mechanism, each state is allocated a register that carries information bits for the survivor path up to the current state (Bahl et al. 1974). The register achieves this by maintaining a partly decoded output sequence along the path. Also, in the traceback mechanism, decoding is carried out by traversing the surviving paths from the last state to the first state. The decoded sequence is then obtained by choosing the potential input that influenced the reversed shift (last state to initial state).

Conceptually, the register exchange approach has advantages over the traceback mechanism as it reduces latency, hence it is faster (Ei-Dib and Elmasry 2002). However, the approach needs complex hardware or software than the traceback because the content of the register must be copied at each stage to the next stage, thereby resulting to higher energy consumption (Lin et al. 2005; Ranpara and Ha 1999; Singh, Vyas, and Raghuvanshi 2012).

For the purpose of this paper, the traceback mechanism is adopted due to its efficiency and the use of hard decoding compared to the register exchange approach. Notably, branch metric; path metric and traceback mechanism are the three major stages of performing decoding using conventional Viterbi. These stages are the same as the proposed form of LVA, except that the LVA produces a ranked ordered list of globally best candidates after the trellis search. The proposed idea for the form of a 'List Viterbi Algorithm' comes into effect only during the trace-back procedure whenever the two previous distances are the same. In this case, instead of one output, the proposed List Viterbi Algorithm is progressively randomised to generate up to eight solutions. In essence, the solutions are generated by making a randomised set of choices for the previous state when the previous distances are found to be the same. In this paper, 8 solutions are considered arbitrarily putt. Nonetheless, it is possible to have several solutions in the list by making various randomised choices.

The developed List Viterbi Algorithm was tested in two stages with a packet of twentymessage-bits as a test data. In the first stage a, CRC-8 was used to perform a test on the message-bits before transmission. In this case, bit-error was not introduced to the channel. The output received was exactly the same as expected due to the absence of bit error in the packet. The message-bits were then appended with check-bits, encoded with convolutional decoder and then transmitted. But, in the subsequent cases, different numbers of bit-errors were deliberately introduced into the channel to corrupt it.

3. Results and Discussion

Multiple sets of analysis with different numbers of bit-errors were carried out to examine the strength of the proposed method. One-bit error; two-bit errors; three-bit errors and four-bit errors were first used to test the error correction capability of the proposed algorithm. Table

1 presents the result of ten different tests when 4-bit errors were introduced into the channel. The table contains error-bit positions and Pass/Fail column. Error-bit positions indicate the bit positions where the errors were introduced; the Pass/Fail indicates if the proposed method was successful or not. The method is considered successful if at least one of the eight decoded output passes the CRC check after decoding. It fails if all the eight decoded output failed the CRC check.

S/N	Error bits positions	Pass/Fail
1	17 , 19 , 22, 26	Pass
2	2,4,8,10	Pass
3	9, 16, 20, 23	Pass
4	1,3,5,7	Pass
5	17 , 19 , 22, 24	Pass
6	14 , 17 , 19, 23	Pass
7	9,10,11,12	Pass
8	17,18,19,20	Pass
9	1,5,10,20	Pass
10	9,11,12,13	Pass

 Table 1: Test result after introducing four-bit errors at different positions using ten different tests

Table 1 shows that all the four-bit errors (in different positions) introduced at ten (10) different tests were successfully corrected. The finding suggests that this technique guarantee biterrors correction in any case if the number of bit errors does not exceed four (4) bit-errors. By any case, it means, even, if the errors are burst errors. However, as the number of bit-errors increased, the error-correcting capability of this technique decreases significantly.

S/N	Error bits positions	Pass/Fail
1	17,19,22,24,26	Pass
2	2,4,8,10,10	Pass
3	9 , 16, 20, 23,27	Pass
4	1,3,5,7,9	Pass
5	17 , 19 , 22, 24,26	Pass
6	14 , 17 , 19, 23,25	Fail
7	9,10,11,12,13	Fail
8	17 , 18 , 19, 20,21,	Fail
9	1 , 5 , 10, 20,15	Pass
10	9 , 11 , 12, 13,14	Fail

Table 2: Test result after introducing five-bit errors at different positions using ten different tests

Table 2 displayed a clear trend of decreasing performance of the technique as the bit-error increased. It shows results obtained after five (5) bit errors were introduced. Out of the ten test, six tests pass CRC checks while four (4) failed the CRC check. It was observed that bit-errors occurred in bursts for tests that failed the CRC check.

S/N	Error bits positions	Pass/Fail
1	17,19,22,24,26,27,1	Fail
2	2,4,8,10,10,20,27	Fail
3	9 , 16, 20, 23,27,1,5	Fail
4	1 , 3 , 5, 7,9,20,27	Fail
5	17 , 19 , 22, 24,26,3,1	Fail
6	14 , 17 , 19, 23,25,1,5	Fail
7	9 , 10 , 11, 12,13,14,15	Fail
8	17 , 18 , 19, 20,21,8,2	Fail
9	1 , 5 , 10, 20,15,25,27	Fail
10	9 , 11 , 12, 13,14,19,23	Fail

 Table 3: Test result after introducing seven-bit errors at different positions using ten different tests

From the results in Table 3, it is apparent that as the number bit error increases, there is a decrease in performance of the proposed technique. The table shows the results after sevenbit errors were introduced; the technique corrected only one instance of seven-bit-errors. This technique fails to correct any bit-error when eight-bit errors and above were introduced.

The most notable result emerging from the study shows that bit-errors occur in bursts for all the test that failed the CRC check. This result may be explained by the fact that Viterbi decoding algorithm produces burst errors when it chooses incorrect trellis paths during decoding (Heissler, Barsoum, and Condello 1999). The findings reported here suggest that Reed-Solomon code can correct burst errors. Hence, concatenation of convolutional code as inner code with Reed-Solomon code as outer coder should be used in the settings. Therefore, if the Viterbi decoding algorithm chooses a wrong trellis path and produces burst errors, it will be corrected by the Reed-Solomon code if the burst errors are within the error correction capability of the Reed-Solomon decode (Morris 1992).

4. Conclusion

The Viterbi algorithm is a conventional method for decoding the convolutional code. It produces a single output stream which ideally should be the original message. The receiver normally discards it if corrupted. This paper presented a modified form of List Viterbi Algorithm. The algorithm produces eight possible output streams at p>=1 for correct output. The result of the proposed form of List Viterbi Algorithm outperforms the standard Viterbi algorithm. The finding from the study suggests that the classical method of decoding used in Wi-Fi is not the best possible solution since the error correction capability of this technique depend on the length of the list of the algorithm produced. If the length of the list is large, the error correction capability increases whereas the performance of the technique decreases as number bit error increases.

Finally, as future work, the method of CRC for error correction proposed in Lyon (2010) can be combined with the proposed form of List-Viterbi decoding strategy to achieve even better results. If the proposed LVA fails to produce a correct output, there is still a possibility of using the CRC error correction facility to correct one or more remaining bit-errors. Also, a dualmode standard Viterbi algorithm that uses both maximum likelihood and burst error correction capability is presented in Miller, Deutsch, and Butman (1981) and Schlegel and Herro (1990). Hence, a dual-mode with the proposed algorithm can be used to achieve more error-bit correction especially burst error.

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