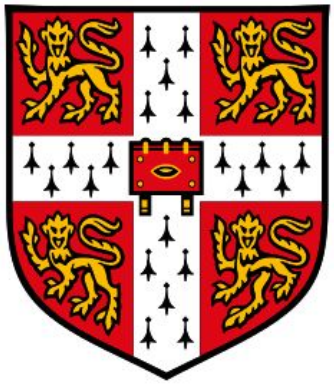
Multiservice Ethernet Digital Distributed Antenna Systems



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Multiservice Ethernet Digital Distributed Antenna Systems

Abstract

Lu Bai

Over 90% of wireless communications traffic occurs indoors and in-building wireless coverage is still one of the biggest obstacles for wireless users. As the growing demands on wireless capacity, coverage and connectivity have led to 4G and 5G standards, it has also become increasingly important to design and implement future-proof indoor wireless services in a cost effective manner. This thesis introduces a novel multi-service digital distributed antenna systems (DDAS) for indoor wireless coverage, which not only is able to transport multiple wireless carriers from different vendors and mobile operators, but also allows a converged architecture to integrate indoor wireless system with existing Ethernet infrastructures. The Cloud Radio Access Networks (C-RAN) has been suggested by major telecom vendors as the main architecture for last-mile coverage in 5G. However, the digital fronthaul interface defined in common public radio interface (CPRI), which is most widely adopted standard for C-RAN, requires very expensive infrastructures to be built due to the high data rate generated after digitisation. A solution has been introduced at the University of Cambridge previously to remove the digital redundancy by using a data compression technique which has shown 3-times higher transmission efficiency than CPRI. This thesis extends the concept to a more robust architecture allowing multiple wireless services to be transmitted simultaneously as well as being carried over standard Ethernet without losing the Quality of End-user Experience (QoE) and the Quality of Service (QoS) of in-building mobile network.

A two-channel DDAS system with data compression algorithm is experimentally demonstrated, showing wide RF dynamic range for both 4G LTE service and 3G WCDMA service simultaneously carried over a single fibre-based infrastructure. The system leads to the design and implementation of full-service DDAS system allowing 14 channels (all 2/3/4G service from three major mobile operators) to be carried over single 10Gbps network. Typically, the system using CPRI will need over 30Gbps network to be installed for wireless coverage.

Another key aspect covered in this thesis is the design and implementation of the multi-service DDAS over Ethernet (Eth-DDAS). Due to the stringent latency requirement in wireless

services, mitigation of delays and errors in frame ordering has become a key challenge for putting DDAS over Ethernet. To overcome these problems, a special Eth-DDAS frame structure is proposed in this thesis. After digitisation, digital signal bearing RF information is packetised onto Ethernet-compatible frames with additional timestamps and sequence numbers before transported via fibre to the receiver. Three latency scenarios are tested with different payload sizes of the proposed frame structure and real-time RF performance is measured to prove the capability of implementation of such system in real-life using commercial off-the-shelf (COTS) ADC/DAC and FPGAs.

Declaration of Originality

I, Lu Bai, declare that except where specific reference is made to the work of others, this thesis is my own work and that no part of this thesis has been submitted for other qualifications at any university or other institute of education. This dissertation includes nothing which is the outcome of work done in collaboration except where specifically indicated in the text.

This dissertation does not exceed 65.000 words and 150 figures.

Lu Bai

September 27th, 2018

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Finally, I would like to thank my parents, my sister and my brother for their encouragement and love.

Contents

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List of Acronyms

3GPP	Third Generation Partnership Project
3GPP2	Third Generation Partnership Project
ADC	Analogue to Digital Converter
AM	Amplitude modulation
AP	Access point
AT&T	American Telephone & Telegraph
AU	Antenna Unit
BBU	Baseband Unit
BS	Base station
BTS	Base Transceiver Station
CDMA	Code-Division Multiple Access
CPRI	Common Public Radio Interface
C-RAN	Centralised Radio Access Network or Cloud Radio Access Network
DAC	Digital to Analogue Converter
DAS	Distributed Antenna Systems
DDAS	Digital Distributed Antenna Systems
DDC	Digital down Converter
DUC	Digital up Converter
eNodeB	E-UTRAN Node B
EVM	Error Vector Magnitude
FM	Frequency modulation
FPGA	Field Programmable Gate Array

FMC	FPGA Mezzanine Card
GSM	Second generation mobile phone standard
HSMC	High Speed Mezzanine Card
IF	Intermediate Frequency
IoT	Internet of Things
IP	Internet Protocol
ITU	International Telecommunication Union
LAM	Local Area Network
LD	Laser Diode
LTE	Long Term Evolution
LSB	Least Significant Bit
MAC	Medium Access Control
MIMO	Multiple Input Multiple Output
MMF	Multimode Fibre
MSC	Mobile switching centre
MTS	Mobile Telephone Service
NASA	National Aeronautics and Space Administration
OBSAI	Open Base Station Architecture Initiatives
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
OSI	Open Source Interconnects
PAPR	Peak to Average Power Ratio
PD	Photodiode
POI	Point of interface
QAM	Quadrature Amplitude Modulation

QoE	Quality of End-user Experience
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
RE	Radio Equipment
REC	Radio Equipment Control
RF	Radio Frequency
RMS	Root-mean-square
RoF	Radio of Fibre
RoE	Radio over Ethernet
RRH	Remote Radio Head
RU	Remote Unit
SC-FDMA	Single-carrier Orthogonal Frequency Division Multiple Access
SDR	Software Defined Radio
SFP	Small Form Factor Pluggable
SMF	Single mode fibre
SNR	Signal to Noise Ratio
SQNR	Signal to Quantisation Noise Ratio
TCP	Transmission Control Protocol
TDMA	Time-Division Multiple Access
UDP	Transmission Control Protocol
UHF	Ultra-high frequency
VHF	Very high frequency
VSA	Vector Signal Analyser
VSG	Vector Signal Generator
WAN	Wide Area Networks

WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Chapter 1 Introduction

1.1 Historical Prospect of Modern Wireless Communications

The first radio transmission consisting of wireless telegraphy was made from a temporary station set up by Guglielmo Marconi in 1895 [1]. He is often credited as the inventor of the radio due to his pioneering work on long-distance radio transmission. Since then, radio technology has become increasingly important for people around the world. Radio stations broadcast in long-wave, medium-wave and short-wave bands, as well as very high frequency (VHF) and ultra-high frequency (UHF) [2]. Figure 1.1 indicates the significant stages in the development of wireless communication.

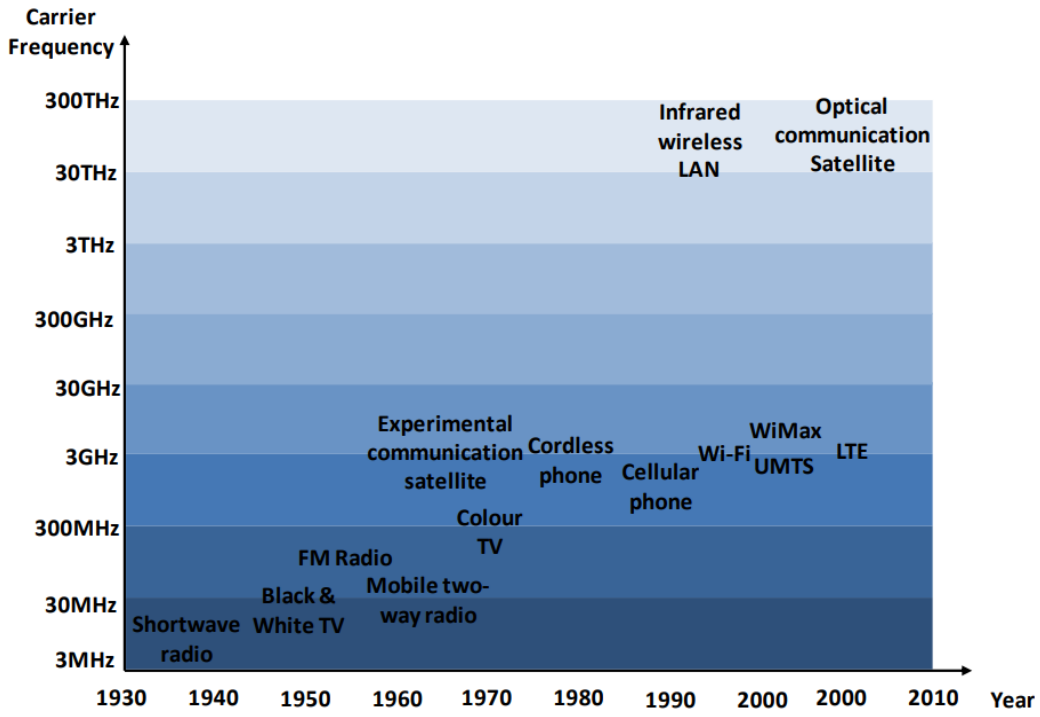


Figure 1.1: Milestone of wireless communication [1]

Amplitude modulation (AM) was developed as the first modulation technology for radio [3]. Before broadcasting was invented around 1920, all forms of radio were ‘one-to-one’, meaning that the messages were transmitted from one radio station to a single recipient [4]. To distinguish the activity between ‘one-to-one’ and ‘one-to-many’, the term ‘broadcasting’ – which was borrowed from the same term describing the agricultural method – was used to describe the communications between a single radio station and multiple recipients [4].

Frequency modulation (FM) broadcasting was developed in the 1950s [5], and before FM became widespread, AM broadcasting was the only commercially significant form of radio broadcasting.

In 1947, the American Telephone & Telegraph (AT&T) company, which is an American multinational telecommunications corporation, commercialised the Mobile Telephone Service (MTS) [6]. The MTS is a pre-cellular VHF radio system, although only three channels were initialised for all the users in the metropolitan area [7]. The first communication satellite was launched in 1960 by the National Aeronautics and Space Administration (NASA) [8]. Thereafter, communication satellites have played a significant role in communications around the world. Since the 1980s, commercial wireless networks for local area networks (LAN) and wide area networks (WAN) have been developed to allow general communications without wired infrastructure [9]. Although the cellular concept was initially proposed in Bell Laboratories in the 1970s [10], first generation (1G) cellular systems did not exist until the 1980s. Since then, modem mobile communications have been developed generation by generation [11], and Figure 1.2 shows the timeline of the evolution of modern mobile communications from the 1G to 5G, due to emerge in 2020.

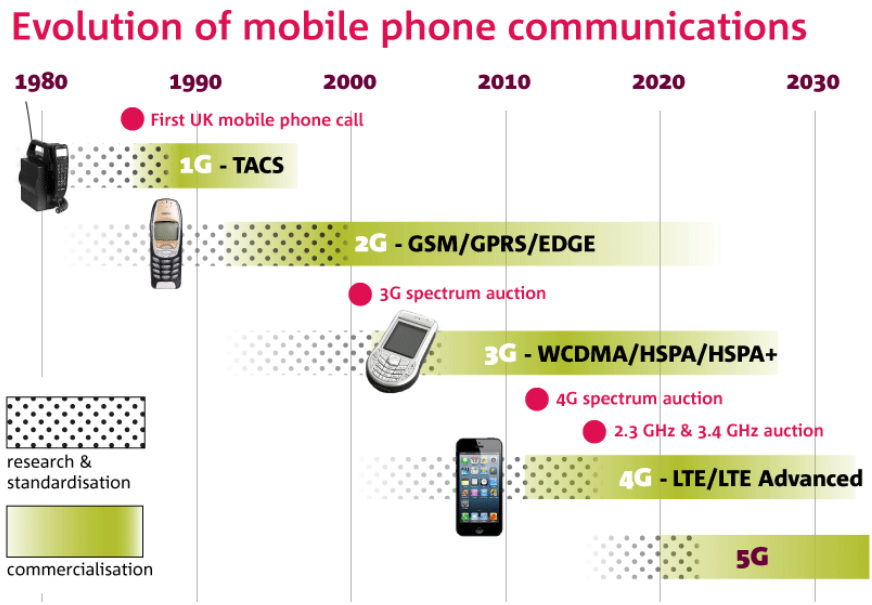


Figure 1.2: Evolution of modern wireless standards [12]

The 1G cellular system was built upon an analogue voice-only mobile network. It was not an effective method of transmitting information, with the very low capacity allowing for only one call to be carried on each frequency band. Using the advance mobile phone system (AMPS) for

1G, the voice quality was poor and the phone size was very large. Moreover, it only allowed for voice calls within one country [13].

For these reasons, 1G services did not become globally popular. The first commercial success in mobile networks was achieved after the second generation (2G) was launched in the early 1990s, and the quality of services increased immensely due to larger bandwidth provided, smaller jitter required and less latency caused. The system security is also improved by the invention of digitally encrypted voice calls [14].

The GSM (Global System for Mobile Communications) is the most widely used wireless standard in history. To date, most of the world's voice services are still being carried over GSM. It was firstly designed as a pan-European standard with a carrier frequency at 900MHz; currently 850-MHz and 1900-MHz are used in the Americas [15]. GSM uses Time-Division Multiple Access (TDMA) technology in which different timeslots are allocated for different users [16]. The biggest rival of GSM in the 2G network is the IS-95 standard which uses Code-Division Multiple Access (CDMA) technology, often referred to as the CDMA standard [17].

When comparing TDMA and CDMA, the main difference that can be observed is the way users share the same physical channels. As shown in Figure 1.3, TDMA divides the channel into sequential timeslots and each user can only use the channel for a short time. Alternatively, the CDMA technology separates them using the codes with the help of different spreading codes. As a result, the transmissions to each user are continuous [18].

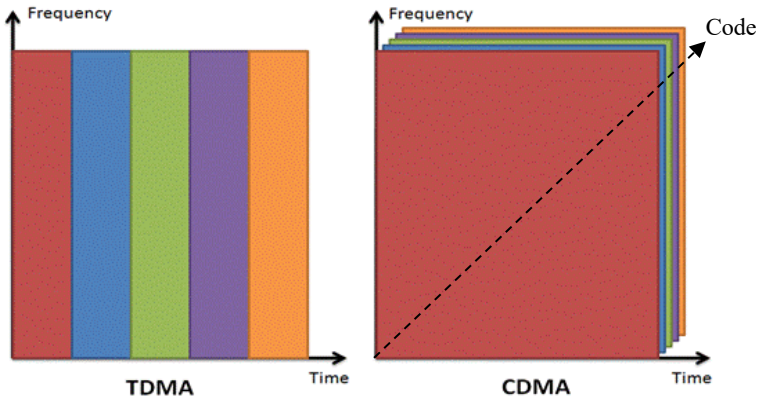


Figure 1.3: TDMA vs CDMA [18]

However, the concept of CDMA was not widely adopted until the emergence of 3G in the 2000s. There were two consortia for the development of 3G systems: the Third Generation Partnership Project (3GPP) and the Third Generation Partnership Project 2 (3GPP2) [19]. Within 3GPP,

Wide-Band Code Division Multiple Access (WCDMA) was the key technology [20]. However, the main technology of the 3GPP2 is the CDMA2000. Both of them utilise CDMA; the main difference between the 3GPP and the 3GPP2 is that the 3GPP uses this totally new approach for the air interface while the 3GPP2 is simply an enhancement of the old approach of IS-95 [21]. The reason for involving IS-95 is because of the limitation of the frequency bands. The frequency bands allocated for 3G systems had already been used by the IS-95 standard in North America; as a result, the aim of 3GPP2 is to improve the old IS-95 approach in order to achieve the requirements of the new generation system [22].

By using 3G networks, users can browse the Internet and download data with faster speeds than 2G networks. 3G services using packet-switched networks allow for the use of smartphones and tablets in which variety of apps provide users with more functionalities than simple texts and voices calls [23]. The speed of data transmission in 2G network is less than 50 kbits/s, while in 3G it can be more than 4 Mbits/s [24]. Although 3G system can provide users with a rich experience, 3G faced enormous challenges right after its launch due to the rapidly increasing user demand for capacity, coverage and seamless connectivity. Although 3G is still widely adopted in the world to date, the current role of the 3G primarily involves its use as a complementary alternative of 4G system in locations where coverage is not yet available. In several regions, 3G was very short lived and has been replace entirely by 4G, which is defined as the Long Term-Evolution (LTE) standard by 3GPP [25].

LTE supports the following different channel bandwidths: 1.4 MHz, 3MHz, 5MHz, 10MHz, 15 MHz and 20 MHz. For the downlink system, LTE uses the technology of Orthogonal Frequency Division Multiple Access (OFDMA). For the uplink system, LTE uses the Single-carrier Orthogonal Frequency Division Multiple Access (SC-FDMA) as the modulation method [25].

Orthogonal Frequency Division Multiplexing (OFDM) is a multiplexing technique in which the wideband carrier consists of numerous subcarriers. That is, a wideband carrier is transformed into many narrowband carriers when OFDM is employed. OFDMA is simply a variant of OFDM in which different OFDM subcarriers can be allocated to different users [26]. This characteristic of OFDMA allows several users to access system resources at the same time. However, one problem with OFDMA is that its peak-to-average power ratio (PAPR) is high [27].

It is possible for all subcarriers to use the maximum power level simultaneously, and as a result the combined carrier can have a very high power level. This can be handled at the base station transmitter, but for the user equipment, a high PAPR means inefficient power amplifier

performance and also short battery life [27]. Therefore, for the LTE uplink, SC-FDMA is employed. SC-FDMA is a hybrid scheme that combines the low PAPR of a single carrier system with many advantages of an OFDM system [28]. Figure 1.4 shows the difference between OFDMA and SC-FDMA.

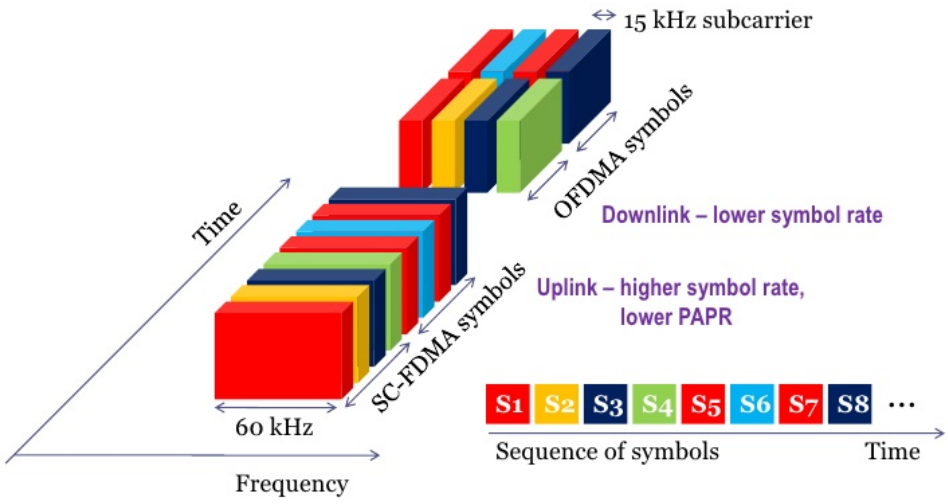


Figure 1.4: OFDMA vs SC-FDMA [29]

Although 4G systems have not been deployed fully around the globe, investigations beyond 4G have already been started. By 2020, industry analysts predict that more than 50 billion devices will be connected to mobile networks worldwide [30]. Furthermore, there will be all kinds of embedded devices that transmit and receive information to or from other devices and servers. This explosion of devices connected to the Internet has been named the Internet of Things (IoT) [31]. To satisfy the demands of all these devices, development of a new generation of mobile communication systems providing higher data rates, larger capacity, higher mobility, higher spectral efficiency and higher energy efficiency has begun.

5G is expected to be standardised by around 2020. Although it is too early to define the specifications of 5G, most researchers agree that compared with 4G, 5G's capacity should be improved 1000 times over, its spectral efficiency 10 times over, and its average cell throughput 25 times over 2014[32]. Network densification is considered as the fundamental strategy to achieve 5G; network densification is the process in which an operator massively increases the number of base stations in high demand areas [33]. By reusing the existing spectrum many times over, the capacity is radically increased.

In June 2015, three main 5G application scenarios were defined by the International Telecommunication Union (ITU) Radio Communication Sector (ITR-R) to guide the goals and

direction of 5G research: 1) Enhanced Mobile Broadband (eMBB); 2) Massive Machine Type Communication (mMTC), and; 3) Ultra Reliable & Low Latency Communication (uRLLC) [34]. Figure 1.5 shows these three usage scenarios.

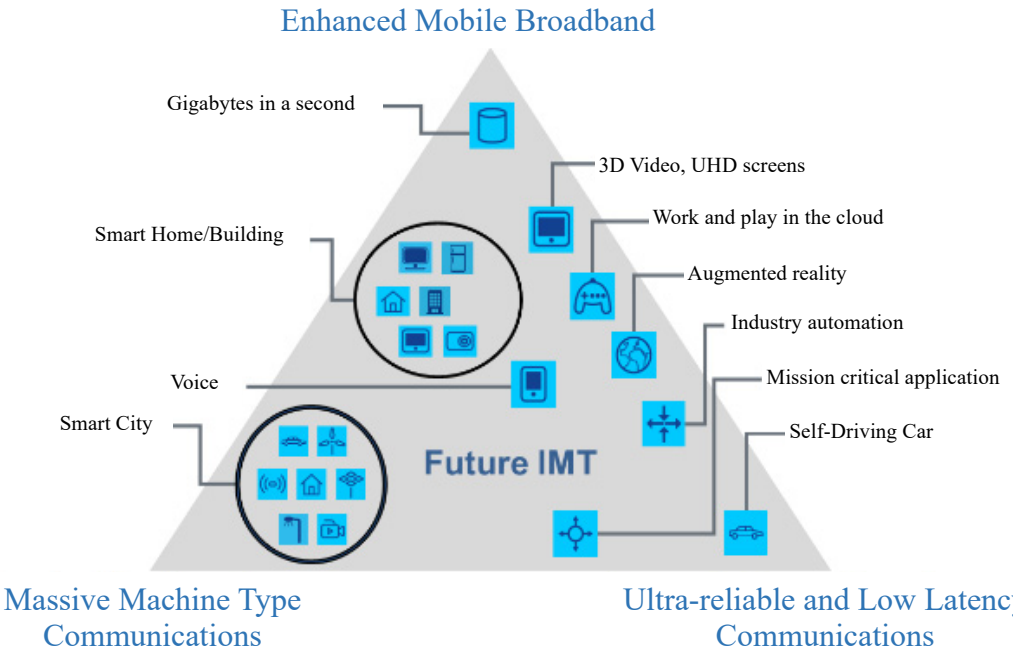


Figure 1.5: 5G usage scenarios [34]

Different 5G applications have different requirements. A self-driving car, for example, requires very low latency communications. However, a smart city needs to handle a great number of connections and applications; some applications, such as 3D video, require a high broadband speed though latency is less of an issue. Overall, the aim of 5G is to connect the entire world and achieve ubiquitous communications between anything, anyone, anywhere, anytime and anyhow [35].

1.2 The Need for In-building Wireless Coverage

Along with the dramatic increase in the number of mobile devices, mobile data has seen a rapid growth in recent years. Figure 1.6 shows the monthly worldwide mobile traffic from 2016 to 2021 provided by Cisco [36]. Mobile data is expected to reach 49 exabytes per month by 2021, which is a 7-fold increase over 2016.

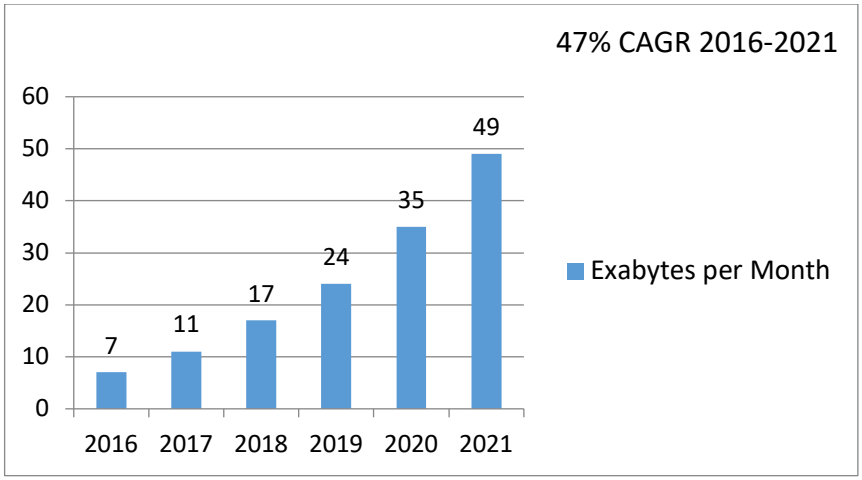


Figure 1.6: Cisco forecasts monthly mobile data from 2016 to 2021[36]

Smartphones contribute the majority of data as illustrated in Figure 1.7. By 2021, 86% data will be produced by smartphones, followed by machine-to-machine (M2M) connections (5%). The percentage of M2M connections will increase over the following years. By 2021, 4G will make up 53 percent of connections and 79 percent of total traffic [36].

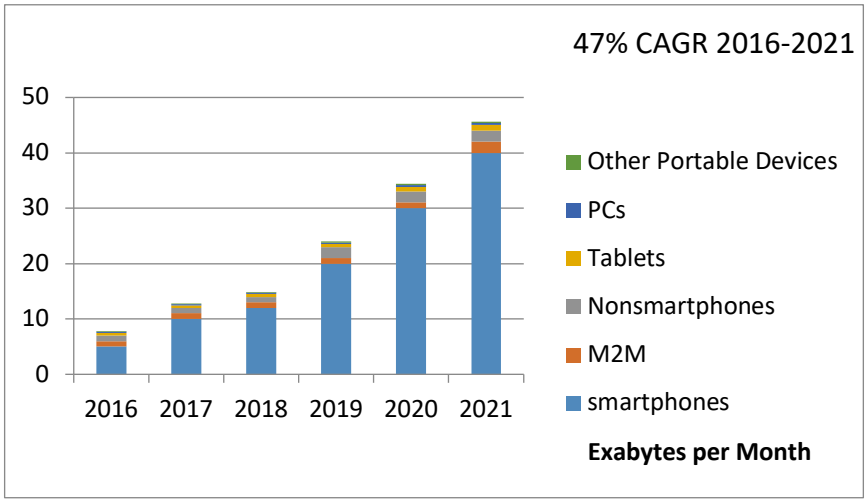


Figure 1.7: Global mobile traffic growth by device type [36]

However, studies estimate that 70% of cellular calls and 90% of data traffic originate from indoor locations [37]. If wireless communication for indoor mobile users relies on an outdoor base station, the penetration loss caused when the signals go through the building walls would be very high, and the situation would be even worse for areas deeper inside buildings. The ITU provides a model for indoor attenuation, which is formally expressed as[38]

$$L = 20\,log(f) + N\,log(d) + P_f(n) - 28 \qquad \text{Equation 1.1}$$

where,

- L = the total path loss (dB)
- f = the frequency of transmission (MHz)
- N = the distance power loss coefficient
- d = the distance (m)
- $P_f(n)$ = the floor loss penetration factor
- n = the number of floors between transmitter and receiver [38]

Equation 1.1 shows that as the frequency (f) increases, the total path loss (L) is also increased. However, in order to support high-speed mobile broadband, wireless services need to increase wireless carrier frequencies. In addition, the equation also indicates that the higher the number of floors between transmitter and receiver, the more total path loss occurs. The high attenuation through the building material seriously affects the Quality of End-user Experience (QoE) and the Quality of Service (QoS). QoE and QoS are the two major measurements to help providers improve their service. QoE describes how well the network operation is satisfying users' requirements and QoS provides many parameter requirements, such as the packet loss ratio and latency requirement [39]. To address these issues, an indoor wireless system is required.

1.3 Current Solutions for In-building Wireless Coverage

Many solutions have been investigated for wireless indoor systems, such as small cells (picocells and femtocells) and distributed antenna systems (DAS). These networks are deployed to provide coverage in targeted locations by moving radio emitters closer to users. Each of the various technologies has unique characteristics and capacities that make them most suitable for deployment in specific environments and for resolving particular coverage and capacity challenges. The main characteristics of small cells and DAS are introduced in the following sections.

- Small Cells (Picocells and Femtocells)

By increasing the power levels and the cell radii of the transmitters, wireless cells can be categorized as femtocells, picocells, microcells and macrocells [40]. Table 1 shows the typical cell radii and transmitter power levels for each cell type.

Cell Type	Typical Cell Radius	Power Amplifier (PA) Power: Range & (Typical Value)
Macro	>1 km	20 W – 160 W (40 W)
Micro	250 m – 1 km	2 W – 20 W (5W)
Pico	100 m – 300 m	250 mW – 2 W
Femto	10 m – 50 m	10 mW – 200 mW

Table 1.1: Different cell radii and Tx power levels [41]

Although the cell radii for each type of cell are different, the aggregate throughputs from cells are the same with identical conditions (such as the same channel bandwidth). Therefore, the total capacity of an area can be increased with the help of implementing more cells with small radii [41]. Macro-cells and micro-cells are usually used for rural areas where the user densities are extremely low but cellular service must nevertheless be provided. In this case, the cell radius must be as large as possible to minimise the total cell count [42]. In contrast, when user densities in indoor areas are extremely high, picocells and femtocells are used for indoor wireless systems to provide the required in-building capacity.

Picocells are usually found in academic campuses, hotels, airports and corporate offices. Picocells require professional installation and maintenance and they are generally owned by wireless service providers [43]. Picocells only support a few frequencies and only one wireless service provider per unit. An indoor picocell supply for a floor is shown in Figure 1.8.

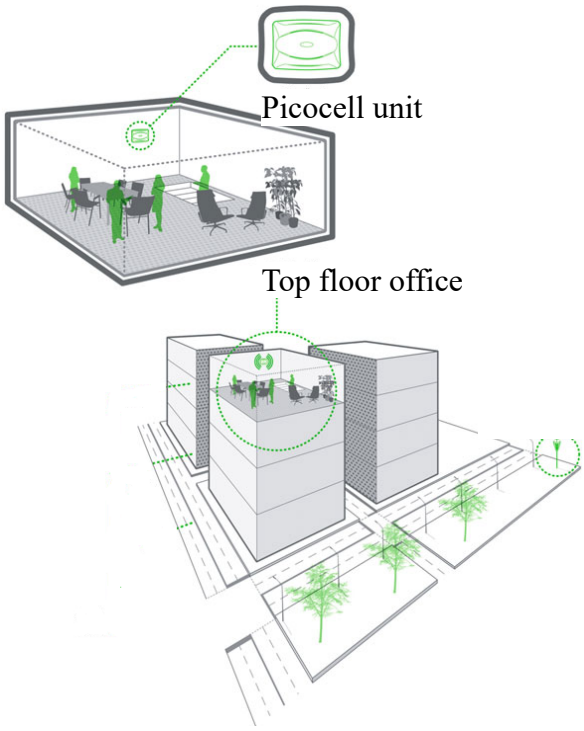


Figure 1.8: Indoor Picocells system [44]

A femtocell is usually deployed in homes or by small businesses as a cell service extender. It is connected through the existing broadband internet connection. Femtocells only support a single service provider. Therefore, separate femtocells are needed if different services are provided in an area [45]. Figure 1.9 illustrates the network architecture of femtocells.

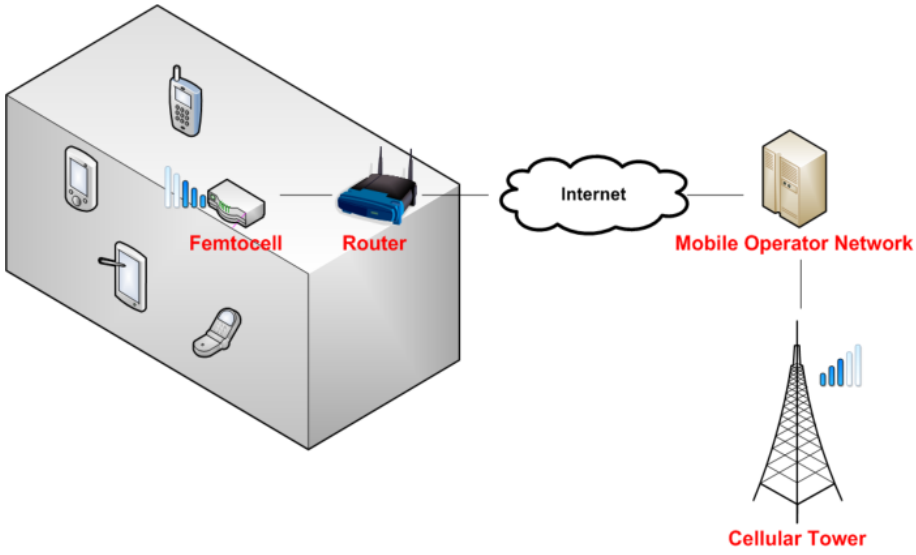


Figure 1.9: Indoor Femtocells system [46]

- Distributed Antenna System

The distributed antenna system (DAS) is a promising solution for indoor wireless coverage. The concept of DAS was first proposed by Saleh in [47]. Instead of using one pickup antenna exterior to the building, a dedicated base station is installed within the building. In this way, the capacity will not be shared with an external cell. A typical DAS system is shown in Figure 1.10.

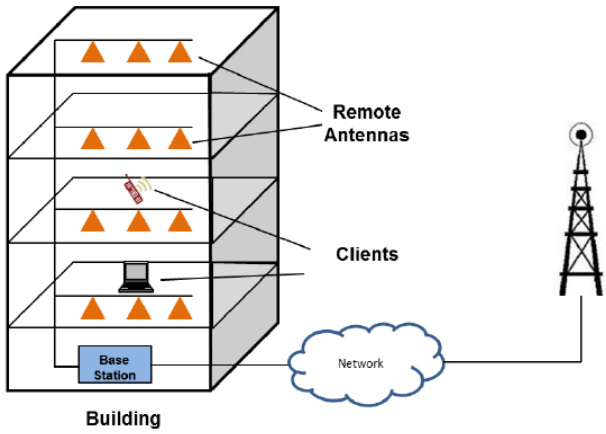


Figure 1.10: Dedicated indoor wireless system [48]

As shown in Figure 1.10, a typical DAS network usually consists of three primary components: 1) a number of remote antennas for the transmission and reception of a wireless service provider's RF signals; 2) a high capacity signal transport medium connecting each remote antenna back to the control centre; and 3) a base station located inside the building which can process or control the communications signals.

By distinguishing the methods used to deliver the signal to the remote antennas, the DAS system can be categorised into passive DAS, active DAS, hybrid DAS and digital DAS.

a) Passive DAS

In a passive DAS, signals are distributed to the remote antennas with the help of passive components. Figure 1.11 shows the architecture of a passive DAS.

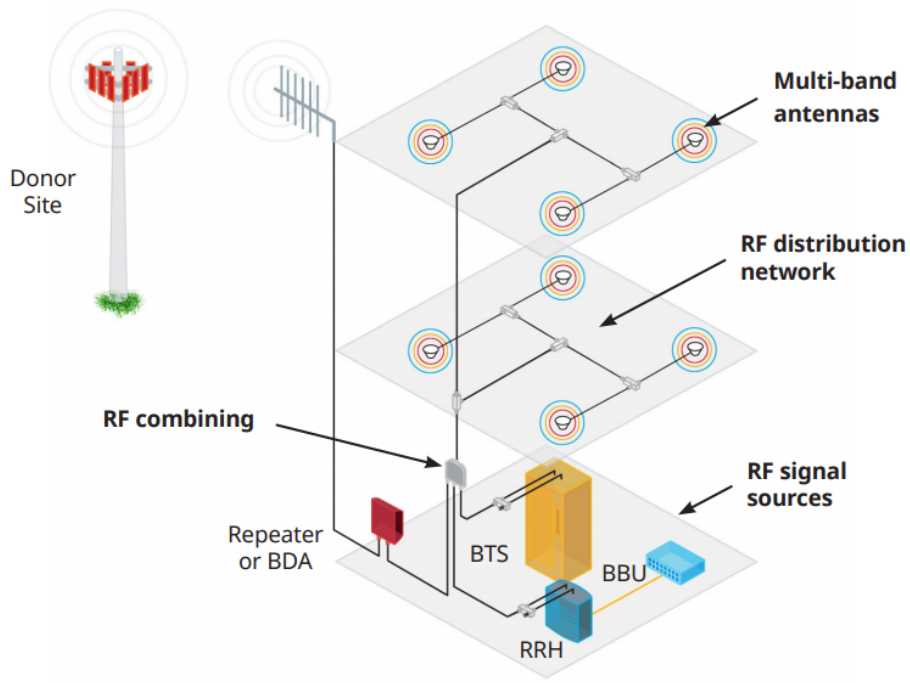


Figure 1.11: Passive DAS architecture [49]

The signal source of a passive DAS can be BTSs, eNode-Bs, Node-Bs and repeaters. RF combining is normally used to combine signals from different receive paths, and based on the coverage requirements, different types of antennas can be used in a passive DAS [50]. When using passive DAS, networks are simple to design and the passive components offer high reliability; passive DAS are usually selected as the solution for public safety applications where economic systems with high reliability solution are required. However, passive DAS networks are difficult to modify after the systems have been completely installed as the sectorisation is determined by system components and hard wiring capacity [51].

b) Active DAS

Compared with passive DAS, an active DAS can be modified after installation. In an active DAS, the sectorisation is determined by the optical connections and RF connections, which are all allocated in the head-end equipment room. By configuring the DAS head-end units, the system's performance can be easily modified. The following figure illustrates a common active DAS architecture.

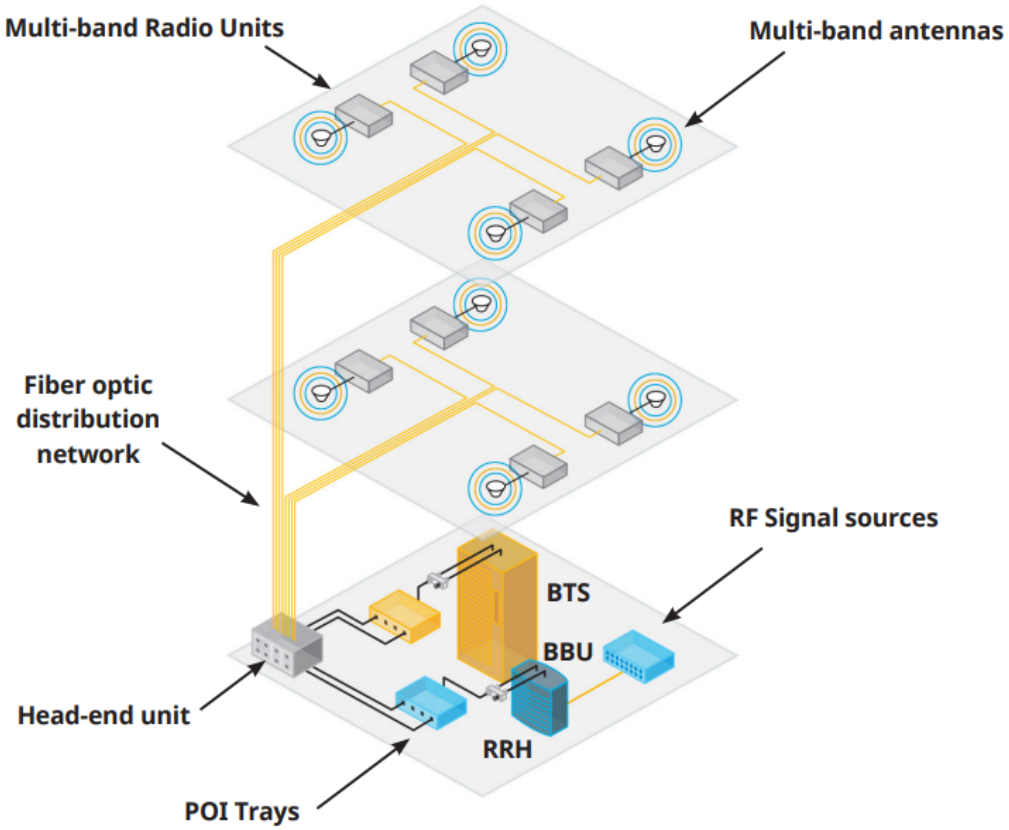


Figure 1.12: Active DAS architecture [49]

The point-of-interface (POI) tray installed between the signal source and the DAS head-end units is used to attenuate the signal before entering the hear-end unit. The head-end unit connects different ports from POIs, provides filters and amplifies the signal to satisfy the further conditions of each path [52]. Radio units are used to convert the optical signals from head-end units, and filters and amplifiers are provided by the radio units. Finally, the signals are re-broadcasted by the antennas.

c) Hybrid DAS

Although active DAS has many advantages, the active components used in the system lead to a much higher cost than when employing a passive DAS. To balance the performance and the cost, the hybrid DAS is deployed as shown in the figure below.

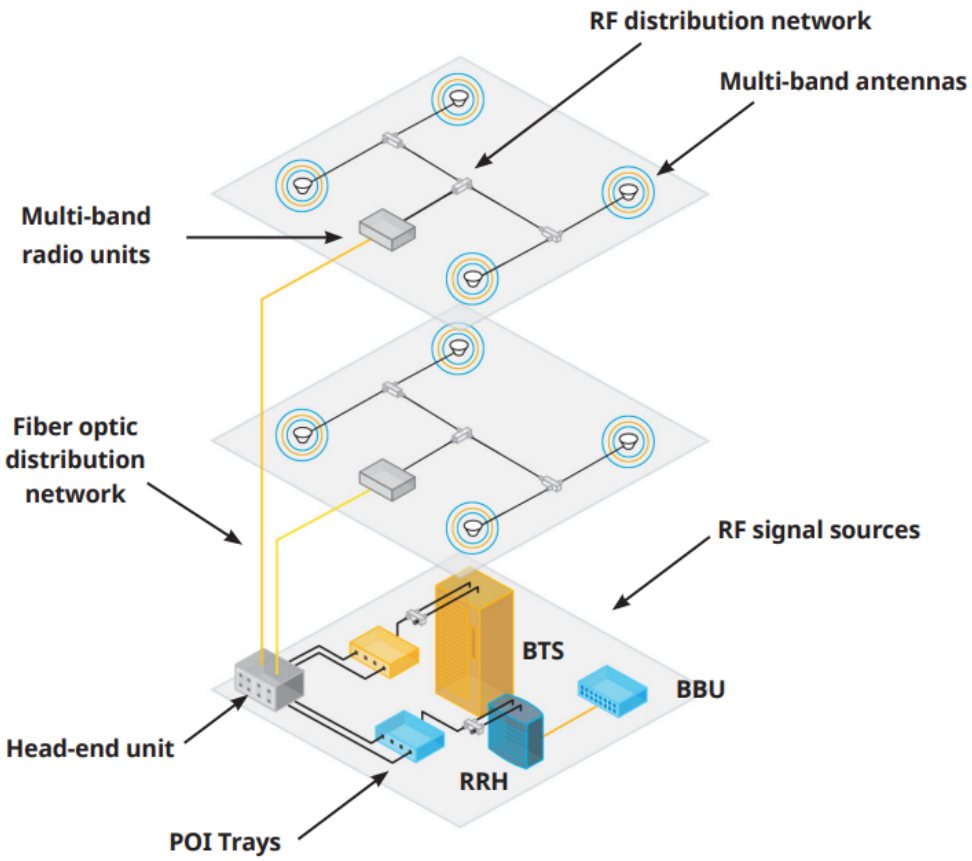


Figure 1.13: Hybrid DAS architecture [49]

In a hybrid DAS, a remote unit with high power is used to replace the remote units with lower power. In this way, the number of active components is reduced and fewer optical links are installed.

d) Digital DAS

The DAS systems introduced above are all analogue DAS. The architecture of a digital DAS is shown in figure1.14.

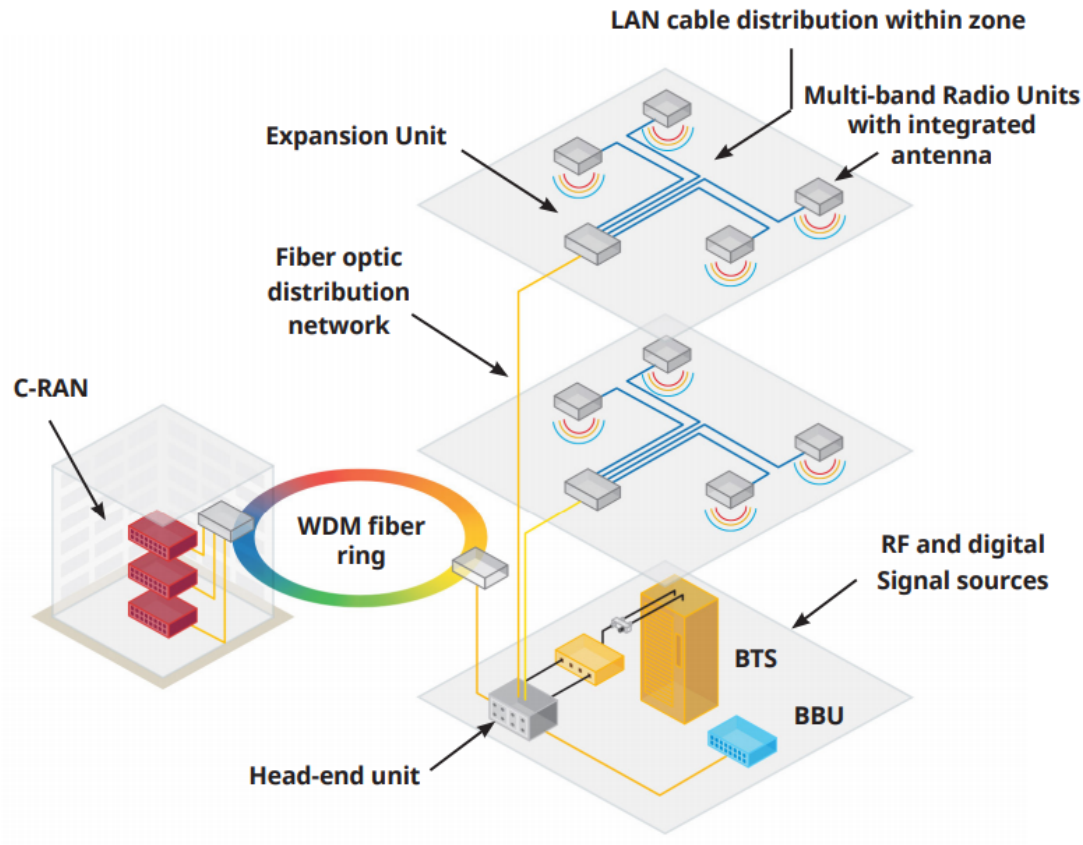


Figure 1.14: Digital DAS [49]

Compared with the analogue DAS, the signal between the head-end unit and the remote radio units is digital rather than analogue. The head-end unit converts the received signals from analogue to digital, and then transfers the digital signals to remote radio units. The remote radio units recover signals from digital to analogue. Apart from the same signal sources used to feed an analogue DAS, a centralised radio access network (C-RAN) also can be used as the signal source of a digital DAS.

The links used by DAS networks vary, and include optical fibre, coaxial cable, and twisted pair. Compared with other media, optical fibre is easier to install because of its characteristic thin diameter and light weight. Silica optical fibre has already been widely used for high-speed data communications. Some of the DAS networks use single mode fibre (SMF) and some of them use multi mode fibre (MMF) [53]. SMF has long been used as the solution for the successful transmission of RF signals over a long distance due to its low loss and dispersion. However, the use of small-core SMF increases the total cost and complexity of the system due to its difficulty with connectors. As a result, MMF is commonly preferred for indoor architectures with a moderate transmission distance as this has a lower handling cost [54].

Optical-fibre DAS is based on radio over fibre (RoF) technology which uses optical fibre links to distribute RF signals from the central unit to the remote antenna units. A traditional analogue RoF system is shown in Figure 1.14 (a); the system can directly transmit RF signals over optical fibre without demodulation. However, the RF performance of the analogue RoF system is highly dependent on the transmission distance and linearity of the analogue optical link. Thus, the digital RoF solution was proposed as shown in Figure 1.15 (b), which can achieve a fixed RF performance until the Error Vector Magnitude (EVM) exceeds the system required EVM limits , which will be discussed in more detail in Chapter 2.

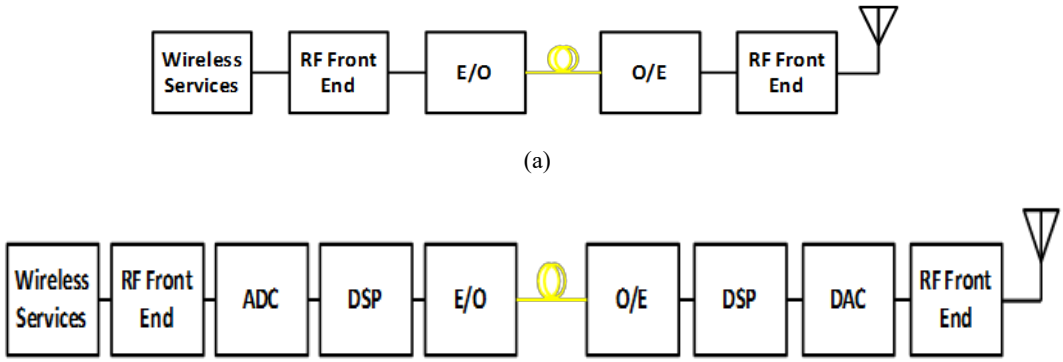


Figure 1.15: (a) Analogue RoF system (b) Digital RoF system [55]

When comparing small cells and DAS networks, it can be observed that small cell solutions are typically deployed to provide coverage or enhance capacity in a much smaller area with a single provider. However, when a multi-service system is required in a large building with a high density of users, a DAS network is a better solution than the small cell solutions in that it supports multiple wireless frequencies and technologies for two or more wireless service providers simultaneously.

The limitations of analogue RoF technology mentioned above also affect the performance of analogue DAS system. In addition, the noise of active devices implemented in the analogue DAS system, such as power amplifiers, also degrades the analogue signal quality. Although the structure of the analogue DAS is simpler than the digital DAS, causing the analogue DAS to incur a smaller cost, the analogue DAS system needs to be carefully designed to satisfy the system requirements. Compared with analogue DAS, although the digital DAS generates a large amount of data and more components need to be used, the high tolerance of digital DAS to transmission impairments makes it attractive. Moreover, the digital DAS system can be controlled and monitored by adding control bits to the system's internal data frame [56]. For

these reasons, the digital DAS is proposed to be a potential solution for in-building wireless systems.

1.4 Digital DAS over Ethernet

Digital DAS (DDAS) has been developed by many companies because it provides good RF performance, can be integrated with existing networks, and has a central remote control capability. A DDAS network for in-building wireless systems has been developed by Tongyun Li [55] in the Centre for Photonic Systems (CPS) of the University of Cambridge. The system contributes a data compression technology which improves the spectral efficiency of the CPRI approaches threefold. Due to the bandwidth limits of the current physical layer and its poor physical layer constraints, integrating the current DDAS system with an existing network with a reliable physical layer is becoming necessary. Since the Ethernet standard has been developed for many years and it is widely adopted worldwide, to integrate the current DDAS over Ethernet has been considered the solution for the above issues.

Applying Ethernet to the mobile communication fronthaul transport network has already been standardised as IEEE 1914.3--- Radio over Ethernet (RoE) [57]. The IEEE 1914.3 is an open standards draft effort to specify encapsulation formats and a transport protocol for the cellular radio fronthaul network. The aim of RoE standard is to define a native encapsulation header format for time sensitive radio data. Some technologies, such as sequence numbering and timestamping, have been developed to enable time synchronisation for RoE packets [58]. The CPRI defines the connection between Radio Equipment Control (REC) and Radio Equipment (RE) of radio base stations in legacy systems. Furthermore, eCPRI has been determined for next generation wireless technology as it connects eREC and eRE through fronthaul transport network, which is standardised by RoE [59].

1.5 Thesis Outline and Original Contributions

The aim of this thesis is to study and develop a reliable multi-service in-building digital distributed antenna system over Ethernet protocol (Eth-DDAS).

Chapter 2 reviews the current state of radio over fibre technology for distributed antenna systems. It also discusses the software-defined radio technology which constitutes the foundation of implementing the DDAS system. In this chapter, data conversion technology is also reviewed. In addition, the fundamentals of Ethernet protocol are discussed and the start-of-art performance of radio over Ethernet is presented.

Chapter 3 introduces the DDAS with data compression technology as previously investigated by Tongyun Li. A multi-service DDAS concept is demonstrated experimentally for the first time. Two services (LTE and WCDMA) are transmitted simultaneously over DDAS and the results are analysed. In addition, a full-service neutral host DDAS has been studied, designed and tested for the first time in collaboration with the Beijing Institute of Aerospace Control Devices (BIACD). The full-system is designed to meet the indoor wireless requirements of China Tower Ltd.

Original Contribution:

- *Demonstrated a multi-service DDAS for the first time.*
- *Studied a full-system DDAS in collaboration with BIACD.*

Chapter 4 theoretically and experimentally demonstrates the Ethernet layers implemented for DDAS. The architecture of the Eth-DDAS is introduced and the details of each module implemented using FPGA is also discussed. The system is tested and the results are subsequently analysed.

Original Contribution:

- *Proposed a DDAS toward Ethernet Protocols.*
- *Implemented the Eth-DDAS on FPGA.*
- *Three experimental setups are tested based on the Eth-DDAS.*

Chapter 5 extends the implementation in chapter 4 into a real-time solution. With the help of an ADC/DAC card, the Eth-DDAS is designed and tested with the RF signal.

Original Contribution:

- *Implemented an FMC interface between the ADC/DAC card and the FPGA.*
- *Combined the FMC interface with the system implemented in chapter 4.*
- *Demonstrated the Eth-DDAS with RF signal.*

Chapter 6 concludes the thesis and ideas for future work are discussed.

Chapter 2 Review of Radio over Fibre Technology

2.1 Review of Radio over Fibre Technology

2.1.1 Analogue Radio over Fibre Architecture

The radio over fibre (RoF) concept was first proposed in the early 1990s [60]. It is now used as an efficient networking technology worldwide for providing last-mile wireless coverage in a service agnostic manner. The RoF architecture allows one to deliver a radio frequency (RF) signal by modulating the signal onto an optical carrier and transporting it over optical fibre. Compared to other traditional transmission media such as coaxial cables, the use of optical fibre has many advantages. Firstly, the fibre is compact and light, easy to install, and is reliable. It solves installation problems in instances where the weight of communication media is important, such as optical airborne, and some maritime applications [61]. Secondly, the attenuation of fibre is much lower than for coaxial cable. Therefore, the signal can be transported much further without any amplification [62]. Thirdly, since fibre is electrically isolated, the equipment will not be damaged by lightning or other electric discharge [63]. Fourthly, another advantage of optical fibre over coaxial cable is its bandwidth. By using multiple wavelengths through a single fibre, bandwidth is greatly increased [64]. It is a cost-effective solution for converging wide band signals, without the need for complicated RF conversions.

The basic structure of an RoF wireless distribution system is shown in Figure 2.1.

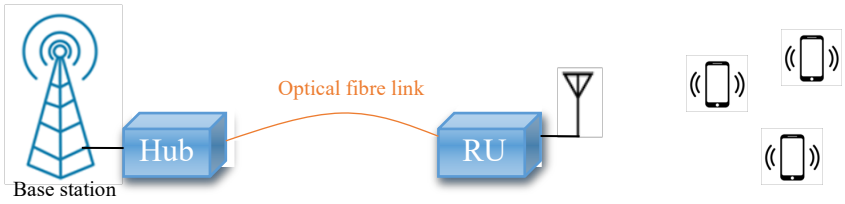


Figure 2.1: Structure of RoF wireless system.

As shown above, a typical RoF wireless distribution system generally consists of a base station (BS), a central hub, an optical fibre link, and a remote unit (RU). Depending on the signals transported over the fibre, the RoF system architecture falls into one of three main categories: direct analogue RF over fibre, intermediate frequency (IF) over fibre, and digital over fibre [65].

Compared with digital system, the main advantage of analogue system is it has infinite amount of signal resolution. Moreover, the analogue system is easier implemented because fewer components are needed. However, the primary disadvantage of the analogue system is the signal distortion and loss incurred and system noise added cannot be recovered.

Figure 2.2 indicates the architecture of direct analogue RF over fibre.

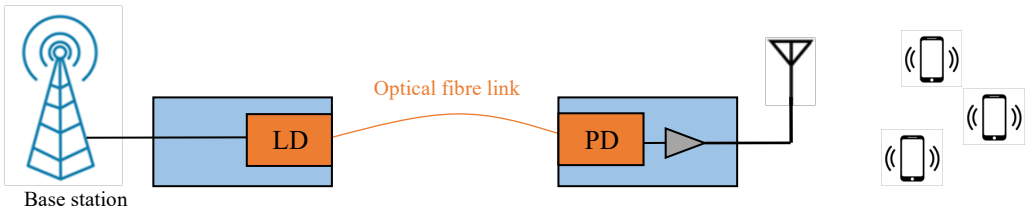


Figure 2.2: RF over fibre architecture.

In the direct analogue RoF system, the RF signal from the base station directly modulates the laser diode (LD) to create an optical carrier, which is then transported over the optical fibre to the remote unit (RU). At the RU, a photodiode is used to recover the signal back to its electrical form, which is subsequently amplified before being transmitted by an antenna [66]. Compared to the direct analogue RF over fibre system, the IF over fibre architecture requires a stage to perform conversion from RF to IF, prior to optical transmission. The IF over fibre architecture is shown in Figure 2.3.

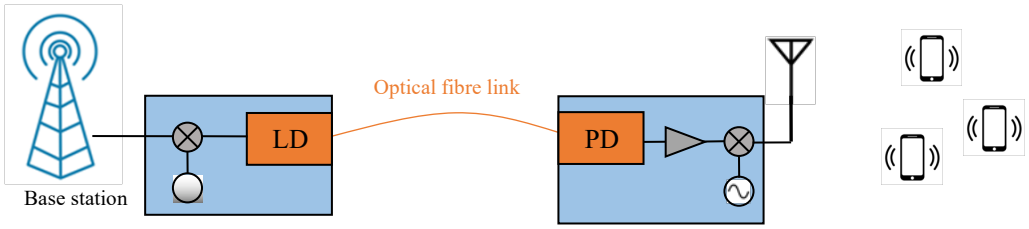


Figure 2.3: IF over fibre architecture.

The difference between RF over fibre and the IF over fibre is the signal frequency transmitted over the optical link [67]. As shown in Figure 2.3, a frequency conversion stage is added for the IF over fibre system. By reducing the signal frequency transmitted over the optical link, the effect of dispersion is also reduced [68]. Therefore, some cost-effective fibres (e.g. multimode fibre) can be used in these systems.

2.1.2 Digital RoF systems

The key advantage of the analogue RoF described above is its capability for carrying multiple wireless carriers onto a single fibre infrastructure, and using the simplest RU, composed only of E/O and O/E conversions for RF coverage. Compared to traditional BS architecture, this distributed antenna system (DAS) effects significant cost of coverage extension savings [69]. However, it also comes with the cost of high transmission losses, nonlinear distortion, and more importantly, difficulty integrating with existing digital infrastructures. As Cloud radio access networks (C-RAN) are proposed as the next generation RAN architecture for 5G [70], and has already been adopted by major telecom vendors [71],[72], a key debate has emerged about whether digital transmission will be essential for network convergence in the future. Small cells (described in the previous chapter) with both baseband and RF processing, housed in a single enclosure, are able to directly connect to the digital network through home broadband, due to its relatively low backhaul bandwidth requirement. However, these are primarily designed as single-service and single operator systems, though some neutral host smalls are recommended [73][74]. When wide-area coverage is required, the cost of deploying small cells becomes substantial. To reduce this cost, C-RAN architecture suggests a functional split in small cells by moving the RF functionalities to the remote radio unit (RRU), and centralising the baseband processing at the baseband unit (BBU), creating so-called wireless fronthaul. A digital fronthaul interface is defined in between to transport wideband digital RF signals over fibre. This digital RoF architecture is currently the most commonly adopted form of last-mile wireless coverage.

- Cloud Radio Access Networks (C-RAN)

A cloud radio access network (C-RAN) represents the new evolution of RAN architecture. C-RAN architecture offers increased performance, enhanced flexibility, and reduced cost in mobile fronthaul networks. Previously, the base station in a RAN network architecture comprised two elements: a remote radio head (RRH) and a baseband unit (BBU). These two elements are interconnected via the CPRI [75]. The BBU is connected to the mobile switching centre (MSC) for more control functions. The previous RAN network architecture is shown in Figure 2.4.

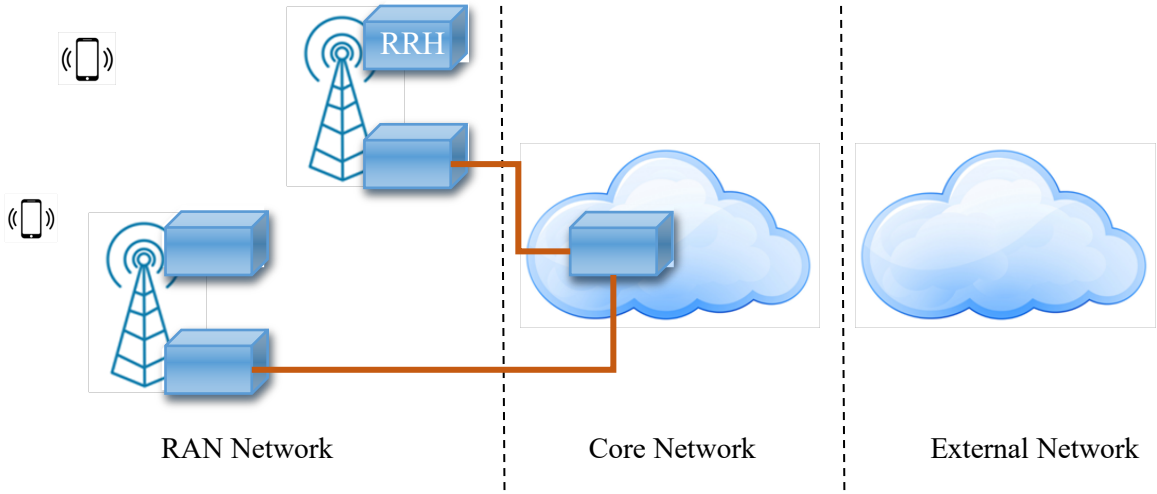


Figure 2.4: Previous RAN network architecture.

In C-RAN architecture, however, the BBU is reallocated from the individual cell to a centralised BBU centre, as shown in Figure 2.5. The BBU centre can be housed in a central office. Removing the BBU from the cell site can reduce the costs associated with space, heating, cooling, power, and test access. Moreover, the centralised topology simplifies networks [76].

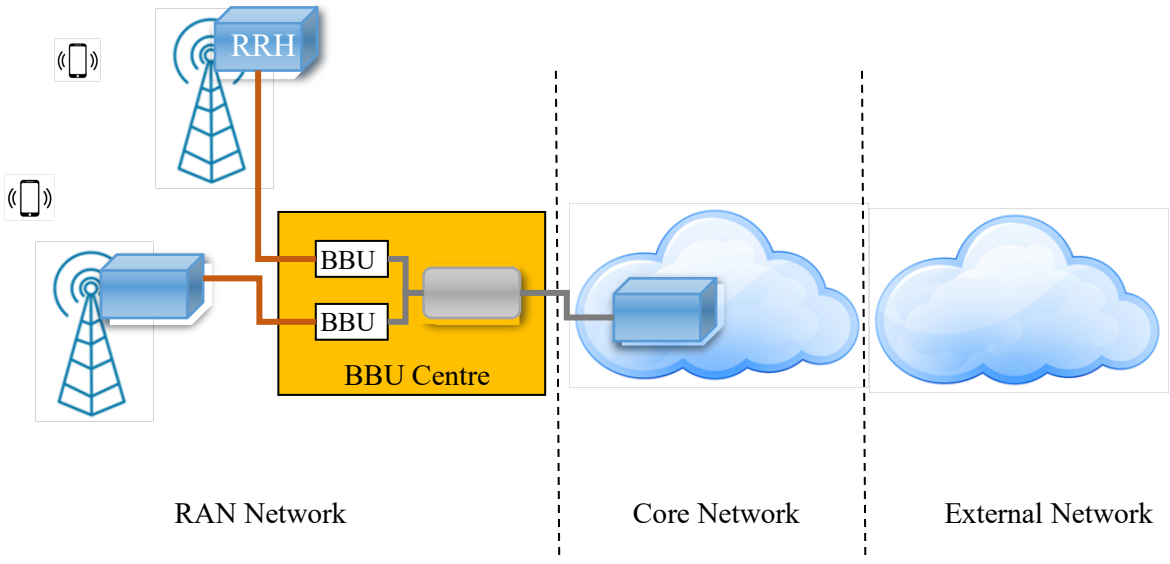


Figure 2.5: C-RAN network architecture.

Although the C-RAN architecture has many advantages, it also brings new challenges. The bit rate in a fronthaul network is very high. For example, a 20MHz bandwidth LTE sector with 2x2 multiple input multiple output (MIMO) requires an approximately 2.5 Gb/s data rate, and a typical three-sector cell requires a data rate of 7.5Gb/s [77]. The traditional RAN network infrastructure is designed to carry a much lower bit rate. To improve transport capacity, optical

fibre is implemented. However, this transport solution results in significant consumption of optical fibre links, particularly in the area where population density is large. As a result, installing a fronthaul network using existing infrastructure is proposed as the most economical solution. Due to the maturity of Ethernet and its wide adoption, using Ethernet as the fronthaul network for C-RAN is considered the best solution.

Compared to the analogue RoF system, the digital system uses an analogue-to-digital converter (ADC) to first convert the analogue signal to a digital signal. Then, the digitised signal is processed and transmitted over the optical fibre link. After the optical signal is recovered by the photodiode, the digital signal is converted to analogue signal using a digital-to-analogue converter (DAC). The analogue signal is recovered and emitted by the antenna. The basic architecture of digital RoF is shown in Figure 2.6. The digital RoF completely removes the impact of nonlinear distortion, noise, and losses caused during optical conversions and transmission. The system can be lossless until error free transmission is lost [78].

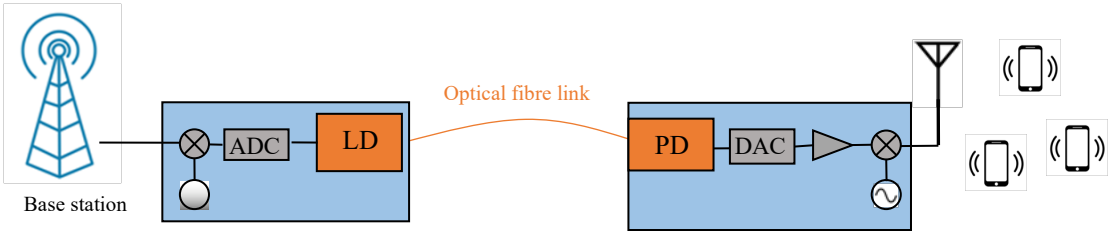


Figure 2.6: Digital signal over fibre architecture.

Traditional analogue RoF requires a dedicated infrastructure to be created, because the optoelectronic modules required in a RoF system have to be specifically designed to support a wideband analogue signal, and optimised for high carrier frequencies. Digital RoF systems, however, can utilise off-the-shelf digital transceiver modules, allowing for fast rollout and network deployment in a cost effective manner. There is a trend of converging all communication services onto a single network infrastructure, including mobile services, TV, and Ethernet data [79]. Digital RoF has become a promising candidate for enabling highly efficient network convergence. The current challenges of digital RoF arise from two aspects. Firstly, the bandwidth requirements for digital fronthaul are extremely high, and thus, an expensive infrastructure (typically over a 3G network) has to be created in neutral host scenarios. Secondly, no standard protocol has to date been fully developed for allowing digital fronthaul to be carried over an existing infrastructure such as Ethernet, without causing any latency issues. Recent development in radio over Ethernet (RoE) and eCPRI standards present a leap forward

towards fully converged networks. In this thesis, the two challenges noted here are addressed in a different to avoid loss of flexibility in existing digital networks.

2.2 Digital RoF Interfaces

In recent years, many researchers have studied digital DAS technology, and the digital DAS system is currently widely implemented worldwide. To standardise specifications, two standards have been released: the common public radio interface (CPRI) [80] and the open base station architecture initiatives (OBSAI) [81]. In addition, to satisfy the next generation fronthaul interface, eCPRI and radio over Ethernet are being studied.

2.2.1. CPRI

CPRI is an industry cooperation protocol used to standardise the specifications for the internal interface of radio base stations between the radio equipment (RE), which is located in the RRH, and the radio equipment control (REC), which is located in the BBU [82].

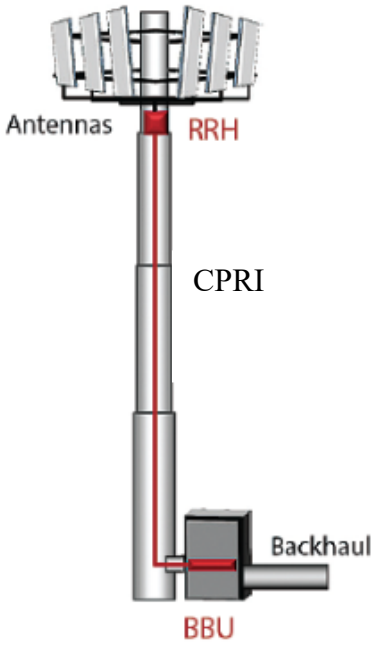


Figure 2.7: CPRI connection in a base station [83].

CPRI is defined with respect to different functions including control, transport, and connectivity. To provide the required functions, three information flows are transported over the interface: control and management plane data, user plane data, and synchronisation plane data. The following figure shows the system and interfaces of CPRI.

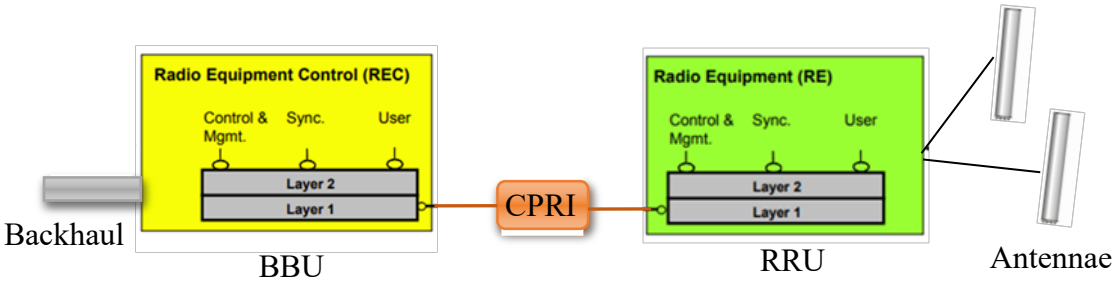


Figure 2.8: CPRI system and interface definition [80].

As shown in Figure 2.8, CPRI is used to define the interface between the REC and RE. The REC and the RE are defined by two layers. Layer one is the physical layer that supports both optical interfaces and electrical interfaces. This layer defines the optical and electrical characteristics. Layer two enables the scalability and flexibility of CPRI. The control and management plane data, the user plane data, and the synchronisation plane data are included in the second layer to support different applications, and to allow for the separate technological evolution of REC and RE [84]. The control plane is used for call processing. The management plane is used for administration, operation, and maintenance of the CPRI link. The user plane is used for transferring data between radio base station and the mobile station. The synchronisation data flow transfers timing information for the system [84].

From the CPRI specifications defined for quality of service, the maximum absolute round trip delay per link, excluding cable length, is 5µs [80]. The round trip delay includes the downlink delay and the uplink delay.

2.2.2 OBSAI

The aim of OBSAI is to create an open market for cellular base stations. As communication infrastructures need to provide sufficient capacity for mobile users, the deployment of a large number of base stations with sufficient capacity is a key challenge for cellular operators. Due to the basic modular architecture and the relatively detailed specifications of the base stations, with the help of the OBSAI open market, development costs can be reduced for new base station products [85].

Digital RoF systems also have limitations. The performance of the digital system is limited by the sampling bandwidth and resolution of ADCs and DACs. Thus, the selection of ADCs and DACs greatly influence system performance.

2.2.3 RoE and eCPRI

As noted in a previous section, C-RAN reallocates the BBUs from each cell to a centralised BBU centre, and Ethernet is proposed as the solution for installing the fronthaul network, as shown in figure below.

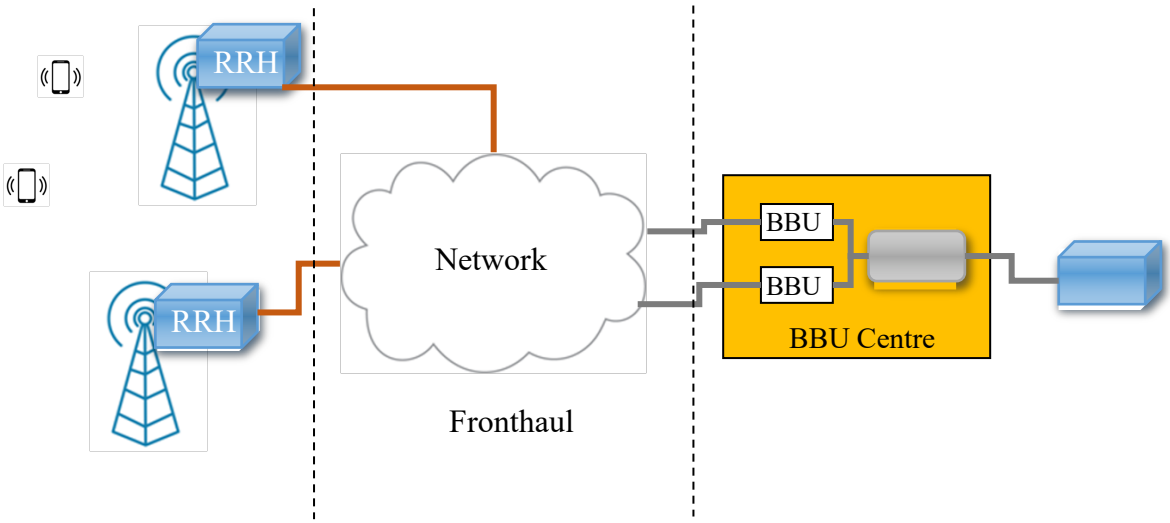


Figure 2.9: Next generation fronthaul interface.

As shown in Figure 2, 10, the eCPRI is used to connect the eREC and eRE. Similar to CPRI, eCPRI supports data transport, management and control mechanisms, and synchronisation. Additionally, eCPRI allows for radio data to be transported via a packet-based network, such as Ethernet [86].

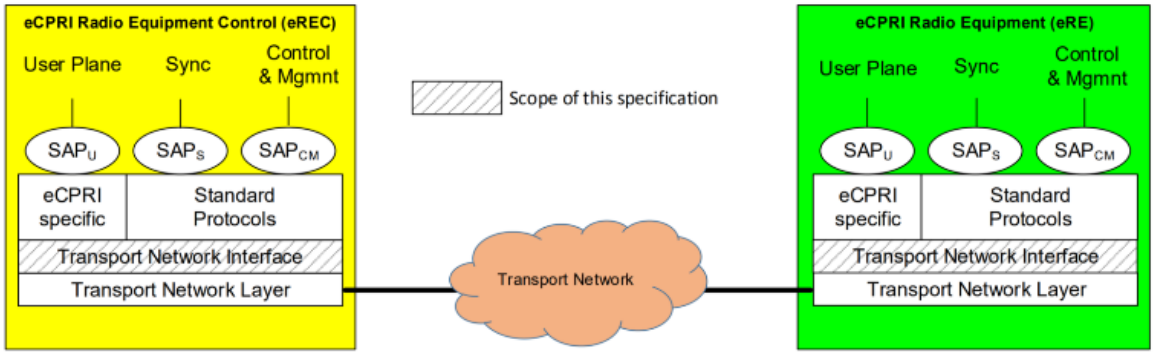


Figure 2.10: The eCPRI system and interface [87].

To map radio data over Ethernet, IEEE 1914.3- radio over Ethernet (RoE) is standardised but has not yet been published. The main aim of this standard is to specify encapsulations and mappings when radio data is transported via the fronthaul network. As radio data is time-sensitive, this protocol also supports time-synchronisation with the help of timestamping, or a

sequence number. From the specification draft, the basic format of RoE is presented in Figure 2.11.

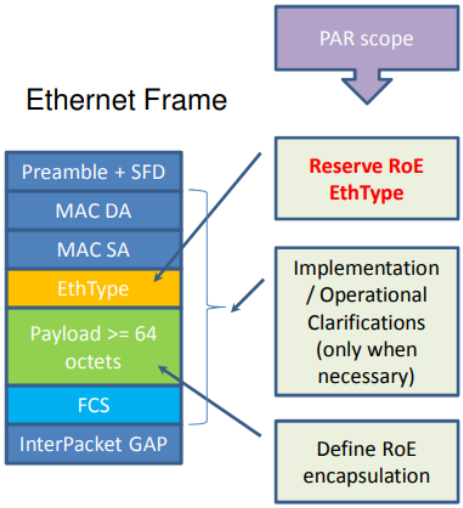


Figure 2.11: RoE format scope [88].

The Ethernet packet remains unchanged and the EthType field is replaced to define the RoE EthType, while the payload field of the Ethernet frame is used to define RoE encapsulation. The RoE encapsulations specify a RoE common header format, which is shown in Figure 2.12.

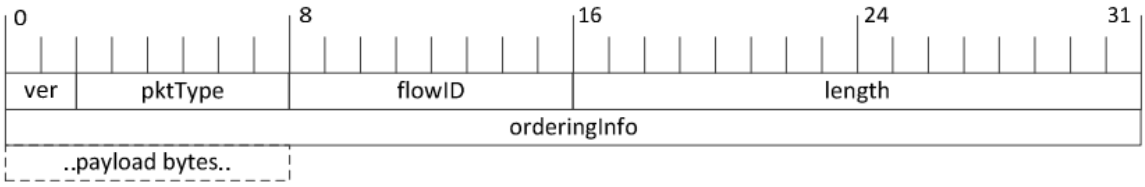


Figure 2.12: RoE common header format [88].

This common header is shared by all RoE packets. A timestamp or a sequence number is carried by this header; the type is decided by **pktType**; **flowID** is used to multiplex multiple flows between source and destination; **length** indicates the total length of the frame, excluding the length of the common header.

2.3 Technologies for Data Conversion

2.3.1 ADC Sampling

Sampling is a core aspect of analogue-to-digital conversion. In order to store a continuous analogue waveform as a digital form, the signal has to be discretised. This process is called 'sampling' [89]. Rather than storing the entire original wave, the amplitude of the wave at a particular time is recorded. One major consideration behind sampling is the sampling rate. The number of samples per second is called the 'sampling rate' or 'sampling frequency' [90]. If a signal is sampled at too low a sampling frequency, the output samples cannot accurately represent the original signal, and the reconstructed signal will have a lower frequency bandwidth. This problem is called 'aliasing' [91]. The use of the Nyquist theorem [92] can avoid aliasing a signal. This theorem simply defines that the minimum sampling rate (F_s) which must be at least double the maximum frequency of the signal (f_a).

$$\mathrm{F_s} > 2\mathrm{f_a} \tag{1}$$

Aliasing will occur if $F_s < 2f_a$.

Consider an analogue signal, *x(t),* and its digitised signal, *x[n]=x(nT$_s$)*. Here, $T_s = 1/F_s$ (F_s is the sampling frequency).

$$x_s(t) = x[n] = \sum_{n=-\infty}^{\infty} x(t)\delta(t - nT_s) \tag{2}$$

where $\delta(t - nT_s)$ is a periodic impulse signal.

By applying the Fourier transform to both sides of the equation:

$$X_s(f) = \frac{1}{T_s}\sum_{k=-\infty}^{\infty} X(f - \frac{k}{T_s}) \tag{3}$$

Since $T_s = 1/F_s$, equation (3) can be presented as:

$$X_s(f) = F_s \sum_{k=-\infty}^{\infty} X(f - kF_s) \tag{4}$$

Figure 2.13 shows the frequency domain representation of this scenario.

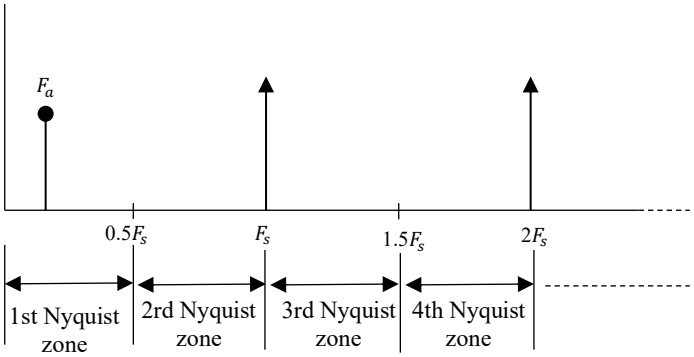


Figure 2.13: Nyquist zones.

As shown in Figure 2.13, the frequency spectrum from DC to half of the sampling frequency ($0.5F_s$) is defined as the Nyquist bandwidth. From equation (4), the range of k is from -∞ to ∞, and therefore, the frequency spectrum can be divided into an infinite number of Nyquist zones. The width of each Nyquist zone is $0.5F_s$. Sampling can introduce new frequencies and duplicate the spectrum of the original signal. In order to reconstruct the original signal, a low pass filter is used [93].

2.3.2 Quantisation

Quantisation refers to the process where an analogue input value is mapped to a discrete level, represented by a sequence of bits or a digital code. The number of discrete values for a code, or the quantisation level, is dictated by the input signal voltage reference and the resolution of the ADC [94]. Since the ADC uses a binary code, the number of levels in the ADC can be encoded to the n^{th} power.

$$\text{Number of quantisation levels} = 2^B \tag{5}$$

Here, B represents the resolution of the ADC.

For example, a 3-bit ADC can provide 8 (2^3) quantisation levels.

Resolution is an extremely significant parameter for an ADC. An ADC with a high resolution ensures minimal difference between an original signal and its sampled form. Figure 2.14 shows a signal prior to and following sampling.

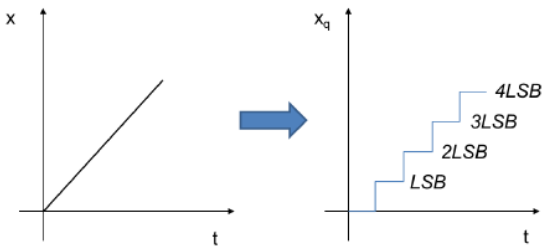


Figure 2.14: Signal before and after sampling.

The magnitude of the analogue signal difference between two consecutive levels, or the minimum change in signal voltage required to guarantee a change in the output code level, is known as the least significant bit (LSB) [95]. LSB is defined as:

$$\text{LSB} = \frac{V_{Ref}}{2^B} \tag{6}$$

Here, V_{Ref} represents the maximum voltage reference of an ADC. For example, a 3-bit ADC with a voltage reference of 5V, LSB = $\frac{5V}{8}$ = 0.625 V.

The difference between the original signal and the quantised signal is defined as the quantisation error or quantisation noise. Figure 2.15 shows an ideal quantized noise the green curve represents the original signal and the red curve describes the quantised signal. The difference between these two signals, ‘e’, is the quantisation noise.

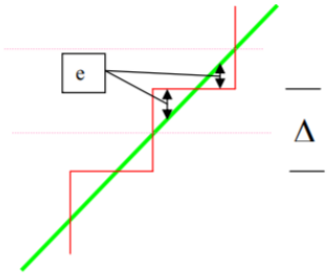


Figure 2.15: Quantisation error.

The maximum quantisation error is half the level step of a quantisation level:

$$-\frac{LSB}{2} \leq e_q(n) \leq \frac{LSB}{2} \tag{7}$$

The ideal quantisation noise can be written as a function of time, as shown in the figure below; this sawtooth waveform has a peak-to-peak amplitude of q, the size of an LSB.

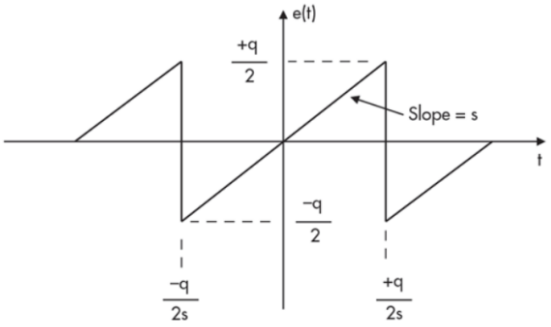


Figure 2.16: Quantisation noise sawtooth waveform [96].

From this sawtooth module with slope of s, the quantisation noise can be given by:

$$\mathrm{e(t)} = \mathrm{st}, \mathrm{t} \in (-\frac{q}{2s}, \frac{q}{2s}) \tag{8}$$

The mean-square value of e(t) is:

$$\overline{e^2(t)} = \frac{\int_{-q/2s}^{q/2s} (st)^2 dt}{\frac{q}{s}} \tag{9}$$

Simplifying this equation:

$$\overline{e^2(t)} = \frac{q^2}{12} \tag{10}$$

The root-mean-square (RMS) error is giving by:

$$\text{RMS quantisation noise} = \sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}} \tag{11}$$

As the signal-to-quantisation-noise ratio (SQNR) is widely used to measure the performance of an ADC, it is defined as:

$$\mathrm{SQNR} = \frac{P_{signal}}{P_{noise}} \text{ [96]} \tag{12}$$

Assuming a full-scale (FS) input sine wave:

$$\text{Input FS sine wave} = \mathrm{v}(t) = \frac{q*2^N}{2} \sin(2\pi f t) \tag{13}$$

The root-mean-square of this input signal is:

$$\text{RMS value of FS input} = \frac{\mathrm{q}*2^N}{2\sqrt{2}} \tag{14}$$

Therefore, the SQNR for an ideal N-bit converter is:

$$\text{SQNR} = 20\log_{10}\frac{\text{RMS value of FS input}}{\text{RMS quantisation noise}} \quad (15)$$

$$\text{SQNR} = 20\log_{10}\frac{\text{q} * 2^N/2\sqrt{2}}{q/\sqrt{12}} = 20\log_{10} 2^N + 20\log_{10}\sqrt{\frac{3}{2}}$$

$$\text{SQNR} = 6.02\text{N} + 1.76\ \text{dB}$$

The quantisation noise can be decreased by increasing the resolution of a converter.

2.3.3 ADC Dynamic Range

The dynamic range of an ADC is the ratio between the maximum input voltage and the minimum input voltage that the ADC can convert [97].

$$\text{Dynamic Range} = 20\log_{10}\frac{maximum\ input\ voltage}{minimum\ input\ voltage}\ (\text{dB}) \quad (16)$$

For example, consider a 12-bit ADC with full scale voltage of 5V. The minimum input voltage that this ADC can convert is $1.22mV$ and the dynamic range is 72.2 dB.

2.4 Software Defined Radio

Software defined radio (SDR) is a communication radio system that has been used for a number of years. Instead of using traditional hardware components, the software on a computer or embedded system is used to define the radio system [98].

As two A/D converters are needed when the analogue baseband real signal is translated to the analogue baseband complex signal, in order to reduce the number of analogue components, the analogue RF signal is down-converted to IF signal instead of baseband signal before the signal is digitised by the A/D converter as shown in Figure 2.17.

An SDR receiver block diagram is shown in Figure 2.17. Here, an analogue RF signal is applied to an RF tuner, which down-converts the RF signal to an analogue IF frequency. The A/D converter digitises the IF signal, creating digital signals. Then, the digitised signal is transmitted to Digital Down Conversion (DDC), which uses a two-step signal processing process. A

complex digital mixer and local oscillator are applied for the first stage. This converts the IF signal down to a complex baseband signal [99]. The second stage involves using a baseband complex digital FIR low-pass filter that matches the desired bandwidth of the received channel. All the signals outside of the bandwidth are removed. Since the low-pass filter output is band limited, an appropriate sampling rate is set according to the Nyquist limit. To reduce sample numbers, decimation is used, that is, keeping one out of every N samples and disregarding others [100]. N is the decimation factor and it is the ratio of the input sample rate to the decimated output sample rate. If the decimated output sample rate is kept above the Nyquist limit, no information is lost. Decimation has many benefits; for example, allowing the FPGA to process data more easily, because fewer samples with the same information are processed. Since the data can also be transmitted at a lower rate, a cheaper channel can also be used, or more channels can be transmitted within a particular channel bandwidth [101].

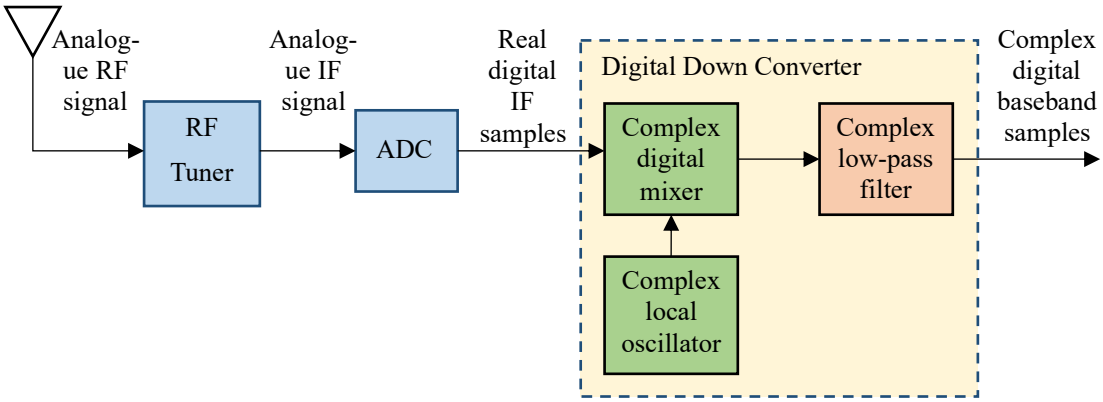


Figure 2.17: SDR receiver block diagram.

The block diagram of the SDR transmitter is shown in Figure 2.18. This is exactly the inverse signal processing scheme to the receiver. The Digital Up Converter (DUC) is used to translate these complex digital baseband samples to real IF samples, which are fed into a DAC converter, which converts the digital IF samples to an analogue IF signal. An RF up converter then translates the analogue IF signal to the RF signal [99].

The DUC again uses a two-step signal processing operation: the signal passing through an interpolation filter and a complex digital mixer. The digital mixer generates one output sample for each of its two input samples. The main function of this digital mixer is to translate baseband samples up to the IF frequency. As the mixer must deliver output samples at the DAC sample rate of F_s, the rate going into the mixer and the rate coming out of the mixer must equal F_s. As the input signal has a lower frequency of F_s/N (N is the decimation factor), and since the mixer requires a higher frequency, an interpolation filter is applied to increase the sampling rate of the

complex baseband input signal, in order to match the required rate for the mixer. The interpolation factor N is the ratio between the interpolated sample rate and the input sample rate [99].

After the complex digital baseband samples have been processed by the DUC, the signals are converted to real digital IF samples. Then, a DAC that has the same resolution as the ADC is used to convert the digital IF samples to the analogue IF signal. The final step is to translate the analogue IF signal to the analogue RF signal, using an RF up converter, which is generally implemented by a crystal oscillator or a PLL in order to produce the desired high frequency. Following this, the RF signal is broadcasted as the signal reception for users [102].

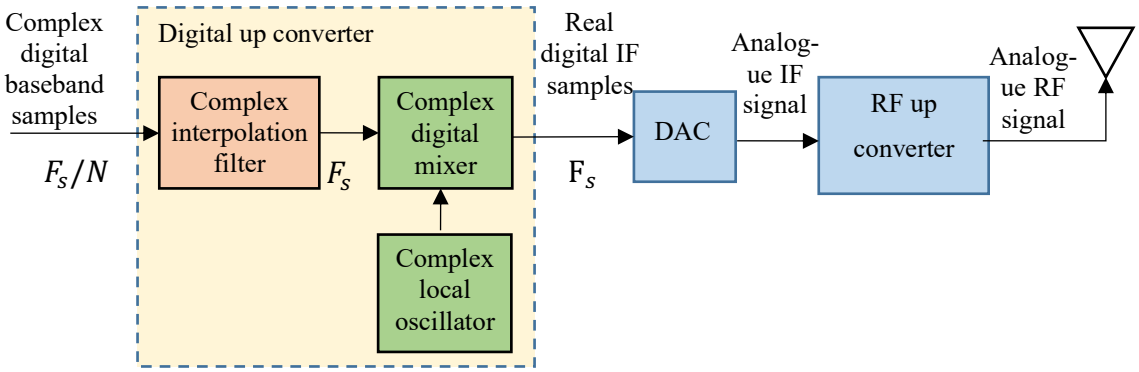


Figure 2.18: SDR transmitter block diagram.

2.5 Technologies for Networking Architecture

Before implementing the DDAS system over Ethernet, it is important to have an understanding of the network model and Ethernet. The open source interconnects (OSI) model and Ethernet family tree are reviewed in this section. More information about Ethernet is introduced in Chapter 4, as it is relevant to the experiment design.

2.5.1 OSI Model and TCP/IP Model

The open source interconnect (OSI) model is a conceptual stack of seven layers that can be used as a reference to assist an understanding of how networks operate. The seven layers are shown in the figure below.

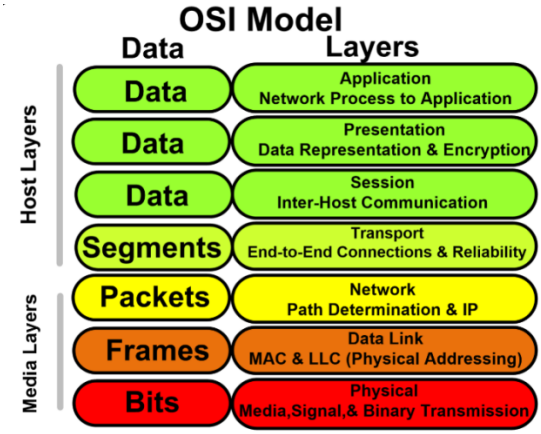


Figure 2.19: OSI model [103].

Layer one is the physical layer. The main function of this layer is to carry data across physical hardware, such as Ethernet cables. Layer two is the data link layer. The physical addresses, including the source and destination MAC addresses, are added to the data in this layer. Switches are operated at the data link layer [104]. The network layer handles IP addressing and routing. The source and destination IP addresses are added to the data. Routers are operated at this layer. The transport layer of the OSI model adds the transport protocols, such as TCP and UDP [105]. The router port number is also added at this layer. Layer five is the session layer. The key responsibility of this layer is to establish and terminate connections between devices. The presentation layer formats the data in a way that the receiving application can understand. This layer is also able to encrypt and decrypt data if needed [106]. Layer seven is the application layer and uses applications can communicate at this layer. Application specific protocols are also used at this layer, such as the simple mail transfer protocol (SMTP), which is the protocol for sending email [107].

The TCP/IP (transmission control protocol and internet protocol) model is one of the most popular models which maps onto the OSI model. TCP/IP is the standard for modern data communications across all networks. It provides a complete system for packetising, addressing, transmitting, routing and receiving data on a network [108]. The layers of the TCP/IP model are shown in Figure 2.20.

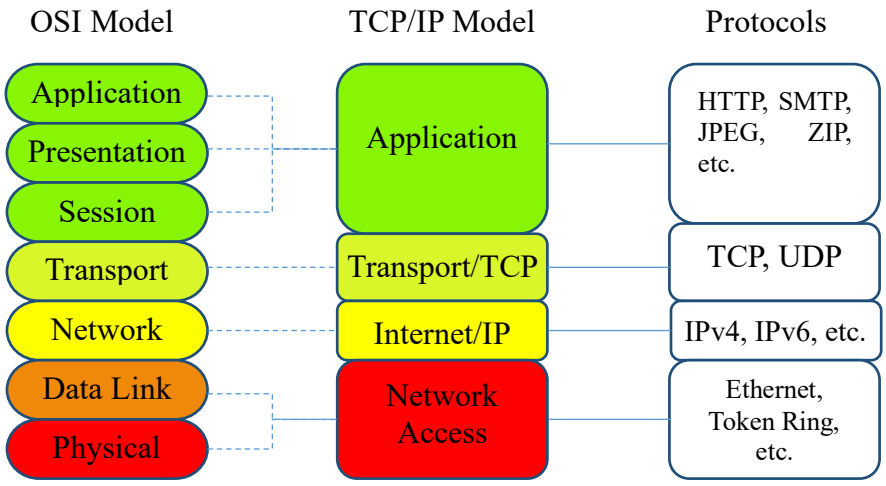


Figure 2.20: TCP/IP model [108].

The top three layers of the OSI model are implemented using the application layer in the TCP/IP model. Applications make requirements and allow a computer to communicate with other computers by performing tasks. The task of the application layer is to send files and information to the transport layer [109].

The transport layer, or TCP layer, defines how the data received from the application layer will be sent to the desired location. Since the received data is typically too large, the transport layer first breaks down the information into smaller parts called packets. The TCP provides reliable transmissions. If a packet is lost in transmission, the protocol responds that it has not arrived and requests that it be resent [110]. In contrast, the user datagram protocol (UDP) is an unreliable form of transmission. If a packet goes missing in transit, it is not resent. However, since UDP is faster, it is often used for low latency applications such as videos. Packets are sent individually to the network, and since the receiver needs to know the order of the packets. TCP, therefore, adds a header to each packet, containing instructions as to the order in which the packets should be reassembled [111].

Once the Internet layer, or IP layer, receives packets from the transport layer, the IP address is added to each packet. The IP address is the exact location on a specific network. The main function of the Internet layer is to address each packet with the proper source address and destination address, so that the packet knows where it came from and where it is going [112].

The network access layer is the central hub through which all information in the medium passes. Ethernet, Wi-Fi, and Token Ring are all technologies for network access. To locate the target, each network device has a unique number, a media access control (MAC) address, which is

provided by the manufacturer when the device is produced [113]. In order to communicate with the desired device, the source and destination MAC addresses are added to each frame at the network access layer.

2.5.2 Ethernet Technology

2.5.2.1 Ethernet Family

The Ethernet standard has been developed over many years. Ethernet equipment has always been designed to be cheap and quick to set up. Although it does not have Quality of Service functions of past telecommunication systems, it has been found that, provided the system capacity is sufficient, transmission is extremely reliable [114]. It has become the primary networking protocol for the local area network (LAN), and was first standardised as IEEE802.3 in 1983. Following decades of development, various Ethernet technologies with different ranges, speeds, and transmission media have been introduced. IEEE802.3 has since become a collection of Ethernet protocols and standards [115]. In this thesis, the NetFPGA-SUNE board is used as the developing board which supports 4 Small Form Factor Pluggable Plus (SFP+) modules. IEEE 802.3 10GBASE-R protocol is used as the standard for these 4 SFP+ modules. Here, 10G means the system supports data rate of 10 Gigabit per second, BASE stands for baseband and R indicates the physical layer encoding type is LAN PHY. 10 Gigabit Ethernet protocol was first published in 2002 in IEEE 802.3ae [116]. This release was published to support fibre optic medium. More details about how to use SFP+ modules on NetFPGA are introduced in Chapter 4.

2.6 Conclusion

Radio over fibre technology has been under development for many years. Due to the limitations of analogue RoF technology, digital RoF has been used to improve in-building DAS system performance, with the help of monitoring and controlling functions. With increasing mobile data, the current transport links of the in-building DAS system cannot provide sufficient bandwidth. As such, a new technology with an economical topology is required. As the widely-adopted Ethernet system has continued development, and as the technologies mature, implementing a built-in DAS system based on the Ethernet infrastructure is considered a solution to the issues. This thesis aims to implement a built-in digital DAS over Ethernet protocol.

Chapter 3 : Multi-service DDAS

As mentioned in Chapter 2, a key advantage of DDAS is the capability of transmitting multi-service multi-operator RF carriers over a single optical infrastructure. This neutral host DDAS allows infrastructure sharing among several service providers, and thus becomes a cost-effective and reliable architecture to deliver indoor wireless coverage, especially for large buildings. The traditional CPRI standard has defined a digital interface between baseband unit (BBU) and remote radio head (RRH) for last-mile wireless coverage. However, such an approach requires excessive digital bandwidth for relatively narrow band RF carriers, e.g. a single 20MHz LTE channel requires a 1.25Gbps link. Typically, there are 3-4 major mobile network operators (MNOs) in any given region. In a situation where all 2G/3G/4G services from the three MNOs are to be carried over a single digital fronthaul, current architecture (BBU+RRH) using CPRI is unsustainable; this is because of the rapid growth of bandwidth and increasing numbers of antennas for technologies such as using massive MIMO technology. To make the digital transmission more efficient, a novel compression technique has been introduced in [55] showing wide RF dynamic range with a compressed data rate of 400Mbps for a single LTE channel, which is 3 times more efficient than CPRI.

In this chapter, the multi-service DDAS concept is demonstrated experimentally for the first time. Two services are transmitted simultaneously over DDAS and the results are analysed. The DDAS architecture is explained in Section 3.1.1. The theory of the system is explained in Section 3.1.2. The system experimental setup and the test results are then described in Sections 3.1.3 and 3.1.4. To deeply understand the multi-service system, a full-service neutral host DDAS designed and built by Beijing Institute of Aerospace Control Devices (BIACD) explained and tested in Section 3.2. Section 3.3 provides the conclusion.

3.1 Novel Low Bit-rate Multi-service DDAS

3.1.1 System Architecture

A novel method for efficiently transmitting a digitised radio service over an optical link to provide wireless coverage has been previously investigated by Tongyun Li from the University of Cambridge [55]. The multi-service digital RoF system architecture is shown in Figure 3.1.

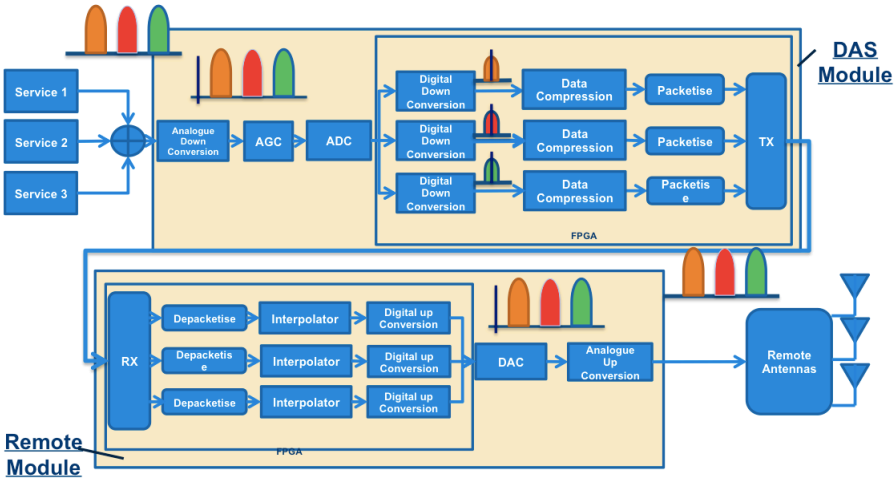


Figure 3.1: Multi-service digital DAS proposal [55]

This system includes a central DAS module and a remote module. Various wireless services generated by conventional access points or base stations are fed into the central DAS module. The signals are then converted to IF signals and processed with an automatic gain control (AGC). Before the signals are processed by the FPGA board, an analogue-to-digital converter is used to convert the analogue signal to digital signal. Then the digital signals are processed with the DAS module in four stages: digital down conversion (DDC), data compression, data packetisation and transmitter modulation.

The remote module, connected to the DAS module via an optical fibre or coaxial cable, recovers the received signals. After the processed signals are received by the receiver, the data is firstly depacketised, then recovered by the interpolator and digital up conversion (DUC) will be applied. The digital signals are then converted to analogue and up-converted to the original carrier frequency. At the far end of the link, the remote distributed antenna units receive the recovered analogue signals for signal transmission.

3.1.2 System Operation

The data processing implemented on the FPGA provides a data compression algorithm. By using the compression algorithm, the spectral efficiency is improved. Figure 3.2 illustrates the modules which are implemented on the FPGA of the multi-service DDAS.

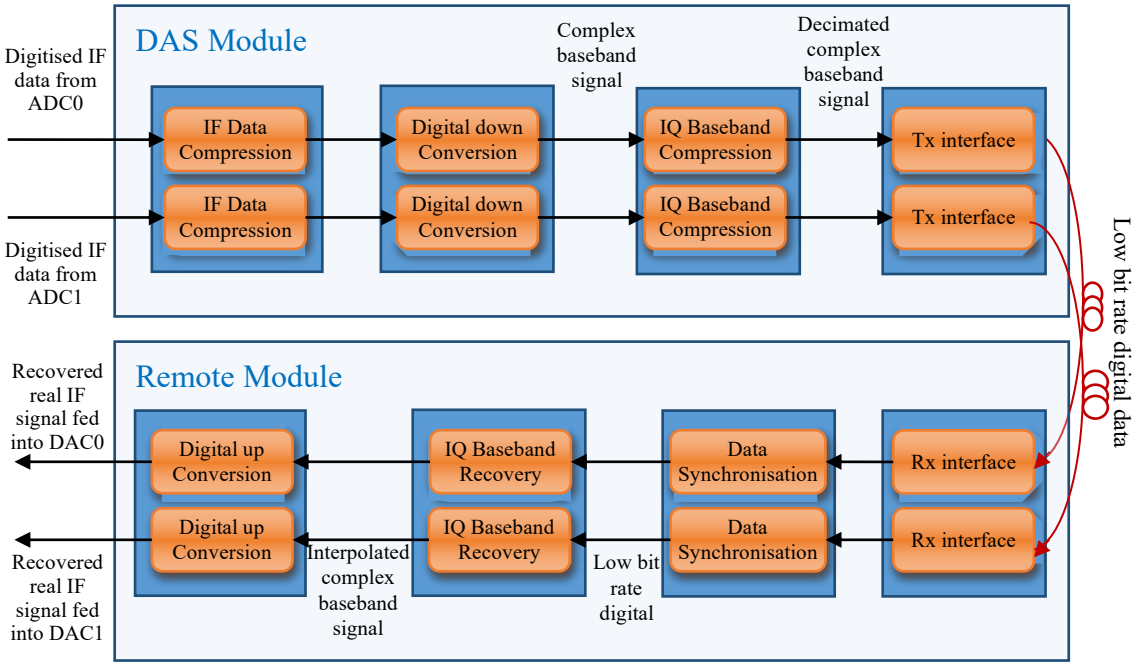


Figure 3.2: Block diagram of the multi-service DDAS on the FPGA

To explain the algorithm simply, a 20MHz bandwidth LTE channel is used as an example.

The IF LTE signal with the 20MHz bandwidth at a centre frequency of 31.25MHz (the centre frequency of the first Nyquist Zone) is used as the analogue input signal fed into the system. The IF signal is then digitised by the ADC and compressed from 14-bit to 8-bit by the IF Data Compression block. Digital down conversion is applied to convert the IF signal to baseband where spectral redundancy is removed by applying a finite impulse response (FIR) filter. By decreasing the sampling rate from 150MHz to 25MHz, the 8-bit IQ data stream is compressed again at baseband.

For the remote module, the received data is firstly recovered by changing the sampling rate from 25MHz to 150MHz. Then the restored data is processed by a matched FIR filter. Data up conversion then reassembles the signal into its original IF format. Then the reconstructed 14-bit signal is transmitted to the DAC for conversion to an analogue signal. After digital processing, the 14-bit data at sampling rate of 150MHz is compressed to 400Mbps (8*25Mbps*2).

By comparison, in CPRI the sampling rate for the LTE signal with a 20MHz bandwidth at baseband is 30.72MHz [80]. To transmit 16-bit resolution data for both in-phase and quadrature signals, a digital RoF link with at least 983.04Mbps (30.72M*16*2) is required. As the CPRI introduces control words and the system must meet dynamic range requirements, a 1.25Gbps

link has to be installed to transmit a 20MHz LTE signal. Hence, by using the data compression algorithm, the spectral efficiency is improved by a factor of three over the CPRI approaches.

3.1.3 Experimental Setup

In order to test the performance of the multi-service DDAS system, two services generated from vector signal generators are fed into the FPGA-based DDAS platform as shown in Figure 3.3. In the DAS module, LTE signals with three different bandwidths (10MHz, 15MHz and 20MHz) are generated by a signal generator and fed into channel 0 of the system as signal sources.

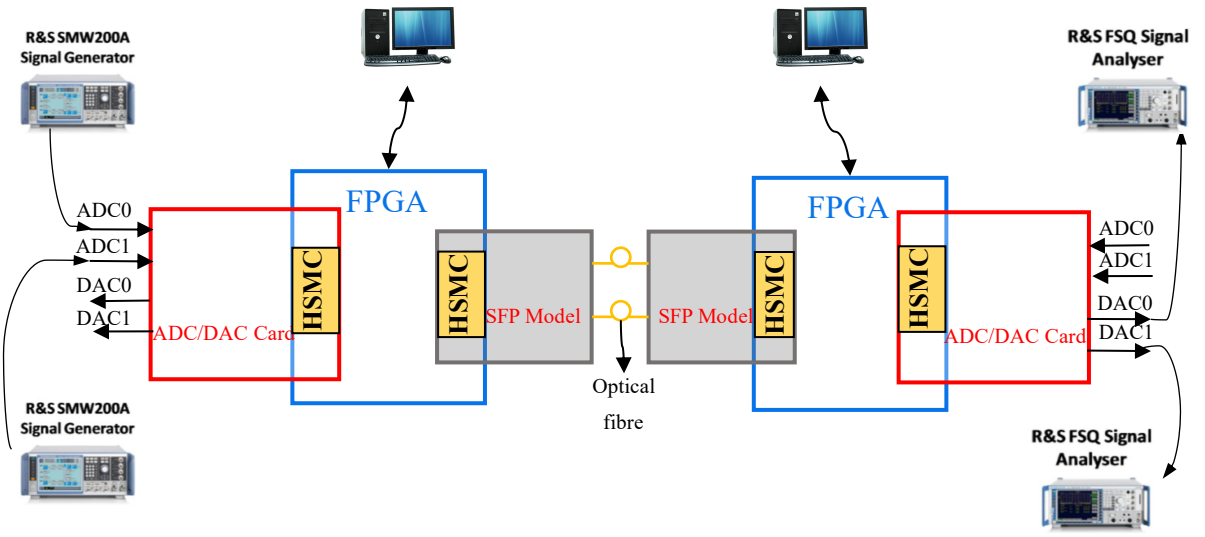


Figure 3.3: Experimental setup

As shown in Figure 3.3, two R&S SMW200A signal generators are used as signal sources for generating an LTE signal and a WCDMA signal. A Terasic data conversion card with two 14-bit ADC channels and two 14-bit DAC channels with a 150MHz sampling rate is connected to a Terasic DE4 FPGA [117] through a High-Speed Mezzanine Card (HSMC) connector. As the DE4 FPGA does not support Small Form Factor Pluggable (SFP) modules which are widely used as optical link interfaces, a Terasic SFP-HSMC board is connected to the FPGA to provide the SFP interfaces and 1.25Gbps optical SFP modules are installed in this system. Two-metre long single-mode optical fibres are used as the optical links between the centre module and the remote module. The system performance is tested and analysed by connecting the DAC output to R&S FSQ Signal Analysers. The FPGAs are programmed by using Altera Quartus. In this

experimental setup, channel 0 is used for transmitting an LTE signal and channel 1 transmits the WCDMA signal.

3.1.4 Experimental Results

To assess the performance of the system, the transmitted signal quality and the system dynamic range of channels 1 and 2 are tested. For channel 0, LTE signals with bandwidths of 10MHz, 15MHz and 20MHz respectively are fed into the system. The error vector magnitude (EVM) results with different input modulation formats (64QAM, 16QAM and QPSK) are tested.

In CPRI, the sampling rate for baseband 10MHz bandwidth LTE is 15.36MHz, for 15MHz bandwidth LTE it is 23.04MHz and 30.72MHz sampling rate for 20MHz bandwidth LTE [80].

- Test Results of Channel 0:

a) Channel 0 EVM performance of LTE signals with 64QAM modulation

Figure 3.4 indicates the EVM performance of channel 0 when the power of LTE input signal is varied from 0dBm to -60dBm. In LTE, 64QAM is defined as the highest order modulation format and the EVM requirement is 8%. This sets a key requirement on the experimental work.

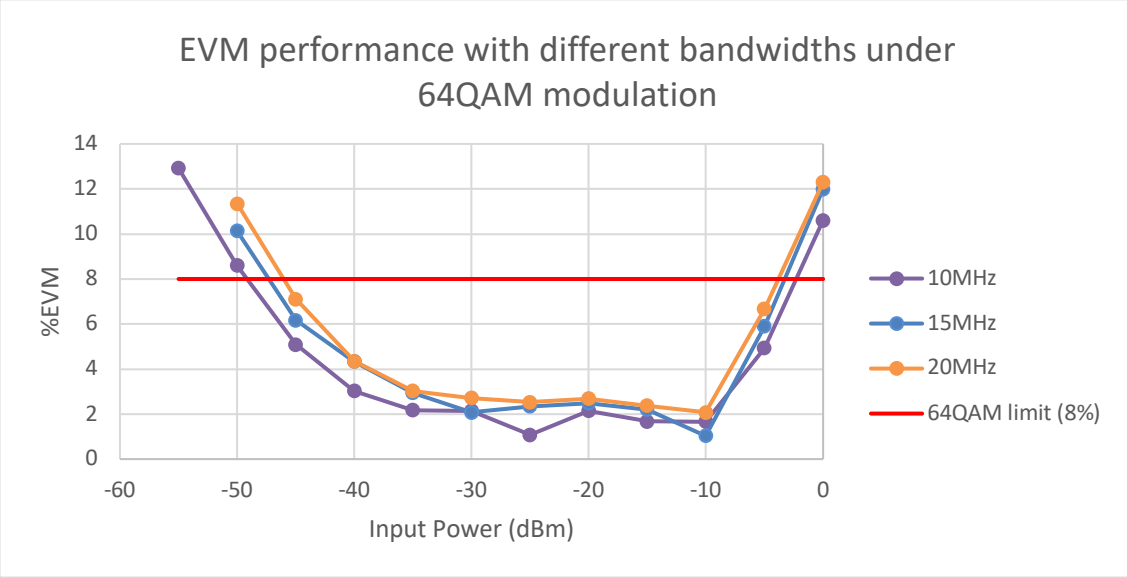


Figure 3.4 Channel 0 EVM performance with different bandwidths under 64QAM

From Figure 3.4, it can be seen that the curves of EVM performances v. input power represents a U-shape. The EVM is small in the middle and becomes larger when input power increases or decreases. This is because when the input power is very small, signals are corrupted by noise and the signals suffer distortion when input power becomes larger.

The yellow curve in Figure 3.4 indicates the EVM performance for the 20MHz bandwidth LTE when the input power varies from 0dBm to -50dBm. As the EVM requirement for 64QAM is 8%, the dynamic range of channel 0 for 20MHz bandwidth LTE is approximately 42dB, the dynamic range for 15MHz bandwidth is approximately 44dB and that for 10MHz is around 48dB. From this figure, it can also be found that decreasing the bandwidth of the input signal can increase the system dynamic range.

The following figures are the 64QAM constellation diagrams for 10MHz and 20MHz bandwidth LTE at input powers of -10dBm, -40dBm and -50dBm. Comparing the constellation diagrams of LTE signal with 10MHz bandwidth at different input powers, it is very easy to find that the transmission quality is very poor when the input power is -50dBm. The result is the same for the LTE signal with 20MHz bandwidth. Comparing the constellation diagrams with the same input power but different bandwidths, it can be found that the LTE signal with 10MHz bandwidth has a better transmission quality than the signal with 20MHz bandwidth.

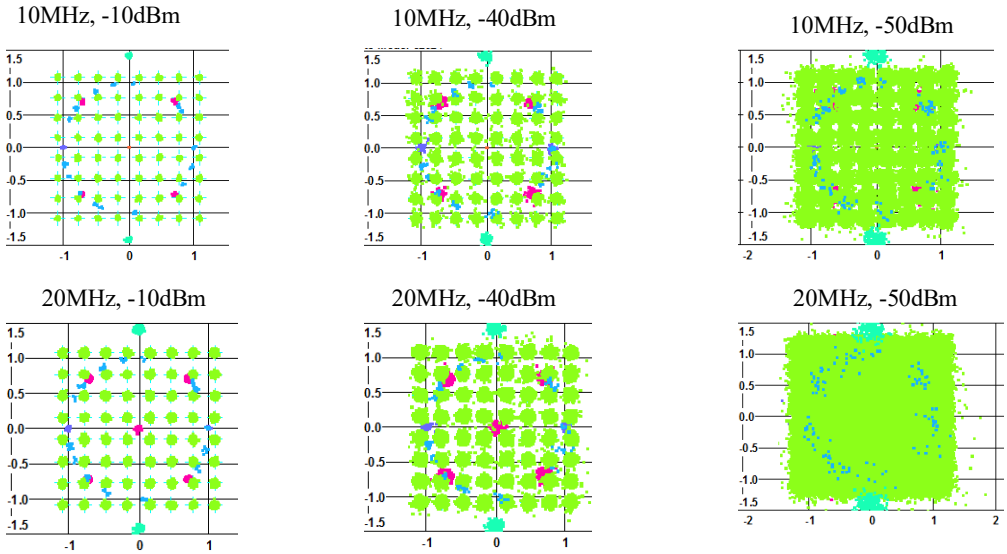


Figure 3.5 64QAM constellation diagrams for 10MHz and 20MHz bandwidth LTE

b) Channel 0 EVM performance of LTE signals with 16QAM modulation

Figure 3.6 is similar to Figure 3.4, except that the 3GPP EVM requirement is 12.5% when the modulation format is 16QAM.

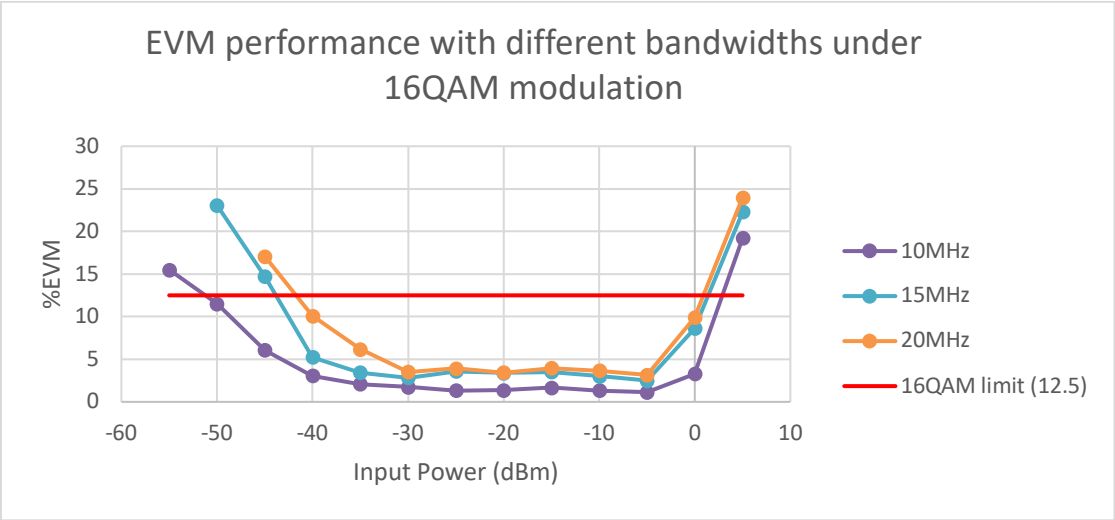


Figure 3.6 Channel 0 EVM performance with different bandwidths under 16QAM

The dynamic range of the 20MHz LTE is approximately 43dB, and the dynamic range for the LTE signal with 15MHz is approximately 45dB. The 10MHz bandwidth LTE has the best system dynamic range with the value of 53dB. The figures below are the constellation diagrams of the LTE signal with bandwidths of 10MHz and 20MHz at input powers of -10dBm, -40dBm and -50dBm. The transmission quality at input power of -10dBm has a better performance than that at input power of -40dBm and -50dBm when the same LTE signal is transmitted through the system. If two signals with different bandwidth of 10MHz and 20MHz are fed into the system at the same input power, the signal with 10MHz bandwidth has a better transmission quality than that of the 20MHz bandwidth LTE.

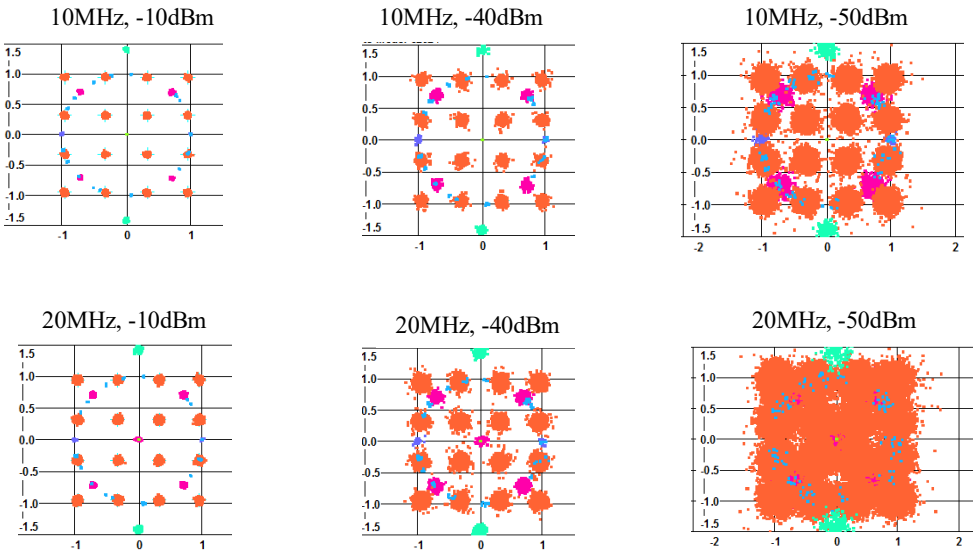


Figure 3.7 16QAM constellation diagrams for 10MHz and 20MHz bandwidth LTE

c) Channel 0 EVM performance of LTE signals with QPSK modulation

The final modulation format provided for LTE by the 3GPP is QPSK, for which the EVM requirement is less than 17.5% [84]. Figure 3.8 presents the test results when LTE signals with different bandwidth are fed into channel 0.

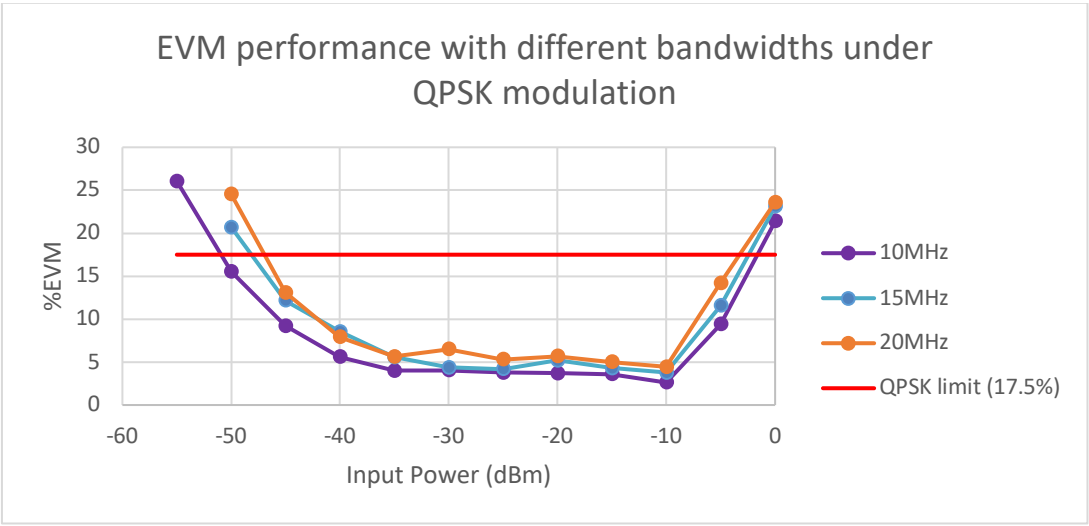


Figure 3.8: Channel 0 EVM performance with different bandwidths under QPSK

As shown in Figure 3.8, the dynamic range for 20MHz bandwidth LTE modulated by QPSK is approximately 43dB, while the 15MHz bandwidth yields approximately 45dB, and the 10MHz bandwidth provides the largest system dynamic range with the value of 49dB. The constellation diagrams shown in Figure 3.9 also indicate that the 10MHz bandwidth LTE has a better data

transmission quality than that of the 20MHz bandwidth LTE signal when the input power is the same.

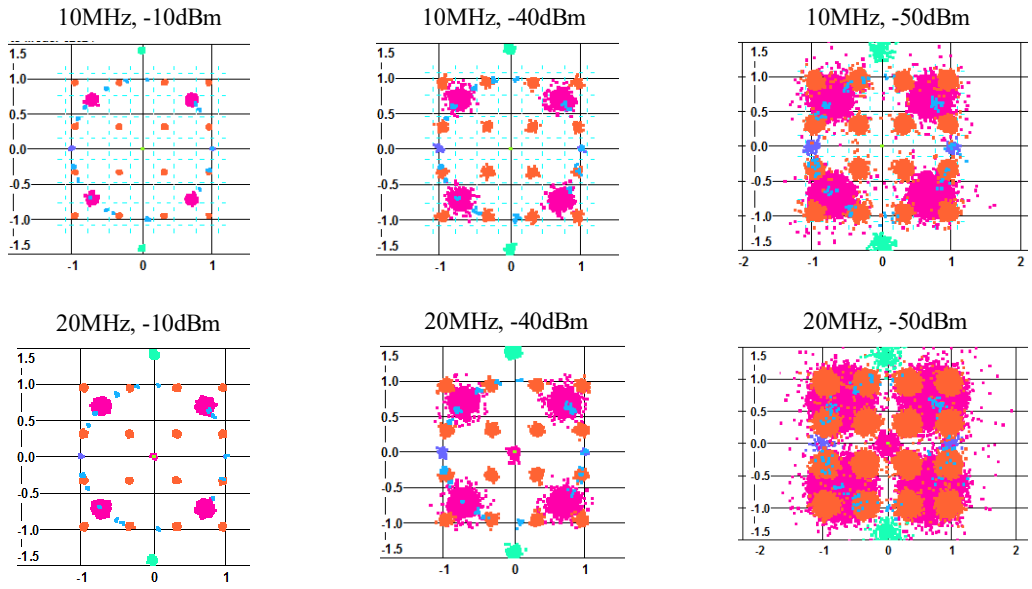


Figure 3.9 QPSK constellation diagrams for 10MHz and 20MHz bandwidth LTE

- Test Results for Channel 1:

For channel 1, a WCDMA signal is fed into the system. The single modulation format defined for WCDMA by 3GPP is QPSK with an EVM requirement of 17.5%. Figure 3.10 shows the EVM performance of channel 1 data transmission.

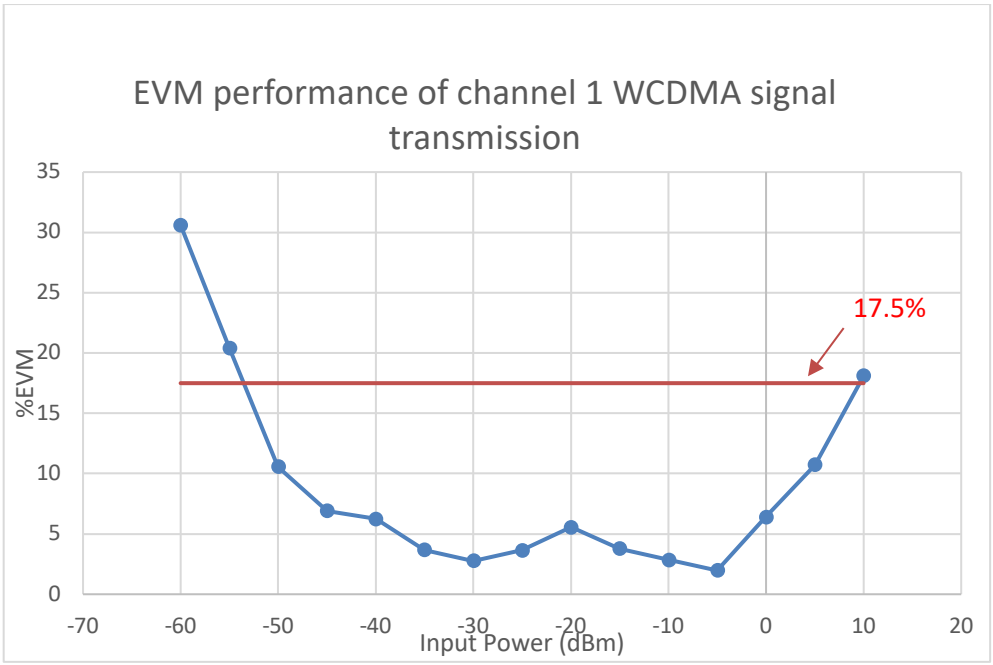


Figure 3.10: Channel 1 EVM performance

To ensure channel 1 is compatible with the QPSK standard of WCDMA, the input signal power range can vary from 9dBm to -53dBm. The dynamic range of channel 1 is approximately 62dB.

3.2 Full-service DDAS design

3.2.1 System Introduction

This section introduces the digital DAS architecture used for a specific application in large multi-storey buildings, this having taken advice of user requirements by China Tower Ltd. The system is built in collaboration with the Beijing Institute of Aerospace Control Devices (BIACD).

The architecture of the system is graphically illustrated in Figure 3.11. The system supports all three major wireless operators in China (China Mobile, China Unicom, and China Telecom), and is composed of the access unit (AU), the extended unit (EU) and the remote unit (RU). Typically, the distance between AU and EU is 5km, 1km from EU to cascaded EU and 300m from EU to RU.

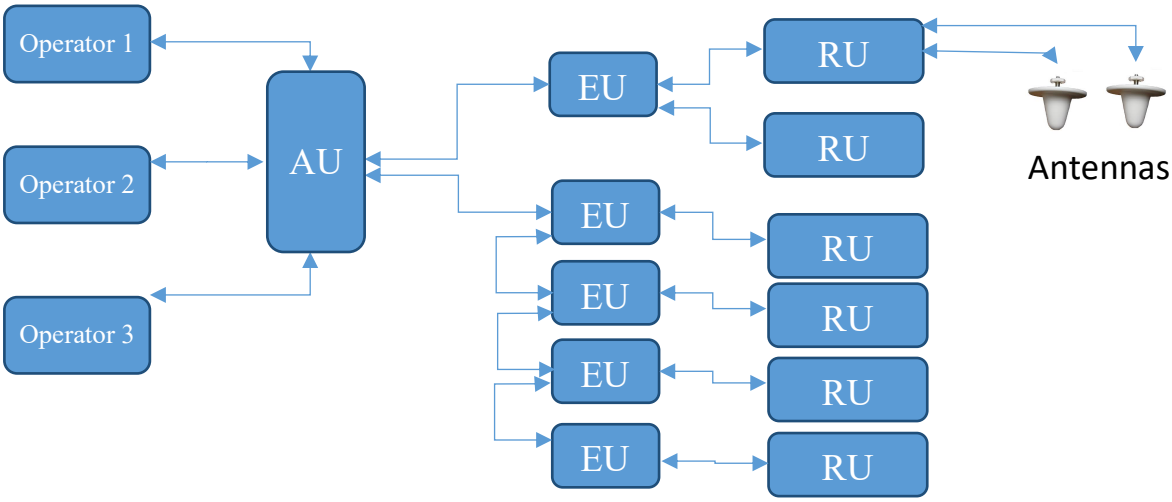


Figure 3.11 Full-service DDAS architecture for China Tower

The AU is at the heart of the system. As a receiver, the AU firstly couples different RF signals from the different service base stations. The RF analogue signal is then digitised and processed as required. The processed digital signal is converted to an optical signal and passed to the EUs through optical links. As a transmitter, the AU firstly converts the received optical signal from the EUs to a digital signal, then applies inverse data processing. Finally, the digital signal is converted to analogue RF and transmitted to the signal service base station.

Compared with the AU, the function of the EU is more straightforward. It is primarily used to distribute the optical signal to different areas. As the EU can be cascaded, as shown in the lower part of Figure 3.11, the use of EUs can provide more side branches.

The RU subsystem converts the received digital signals to the RF signal and provides wireless service to end-users. Meanwhile, the RU can also digitise the incoming RF signals from mobile users and pass them to the EU and the AU.

The AU can connect with four EUs and each EU can be cascaded up to four levels. Therefore, a total of 16 EUs can be installed. As each EU can connect with six RUs, a total of 96 RUs can be implemented.

3.2.2 Design and Considerations

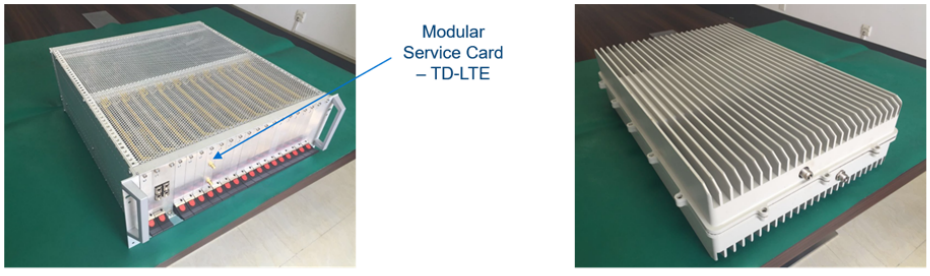
In this section, the China Tower optical distribution system technical requirements and the DDAS performances are introduced.

Table 3.1: China Tower optical distribution system technical requirements lists the main specifications imposed by China Tower, such as the EVM of the overall system, the maximum latency required, the dynamic range the system should provide, etc.

Main Specifications	Requirements
EVM	GSM: ≤ 6% WCDMA: ≤ 12.5% LTE: ≤ 8%
Latency	≤ 15μs
Gain	≤ 55dB
Input Power	Downlink: ≤ +5dBm Dynamic Range: ≥ 25dB
Transmission Power	
Topology	AU can be connected with at least 4 EUs. And AU to EU (≥ 5km). EU can be cascaded at least up to 4 levels. And EU to EU (≥ 1km). EU can be connected with 6 RUs. And EU to RU (≥ 300m).
Power Dissipation	
Operating Temperature	5℃~+40℃
Operating Humidity	15% to 85%

Table 3.1: China Tower optical distribution system technical requirements

To meet the technical requirements provided by China Tower, the DDAS with 14 channels are designed and tested. The products shown in Figure 3.12 are the Access Unit and the Remote Unit.



Access Unit　　Remote Unit

Figure 3.12: Access Unit and Remote Unit

As the centre of the system, the AU is implemented with multiple boards as shown in Figure 3.13.

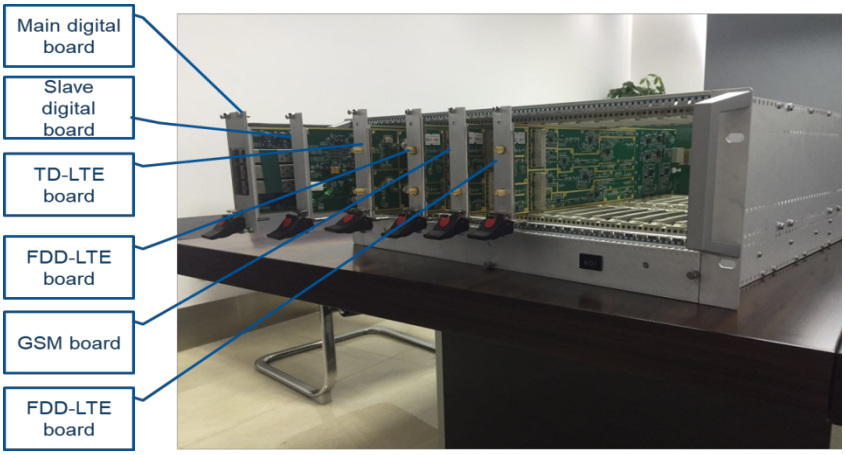


Figure 3.13: Access Unit with service cards

The boards are connected by a back card as shown in Figure 3.14 which allows each board to communicate with the others in the AU.

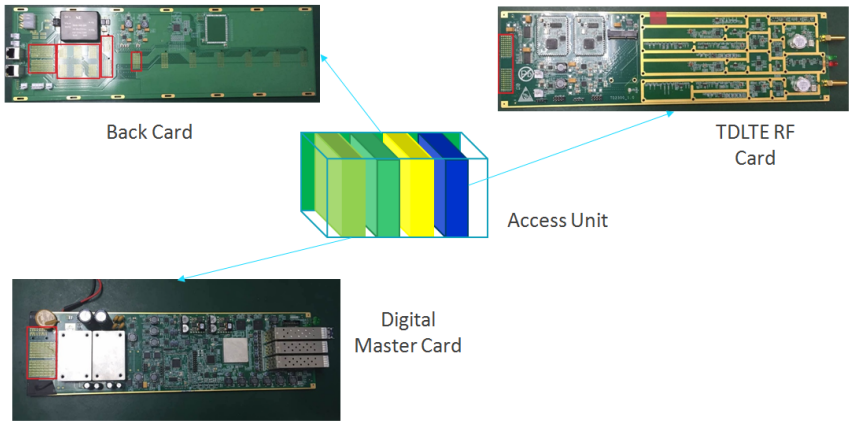


Figure 3.14: Access Unit connections between multiple boards

The function of the Remote Unit is also achieved by implementing multiple cards, such as the RU RF/digital card, the RU monitoring card and the RU TD-LTE card.

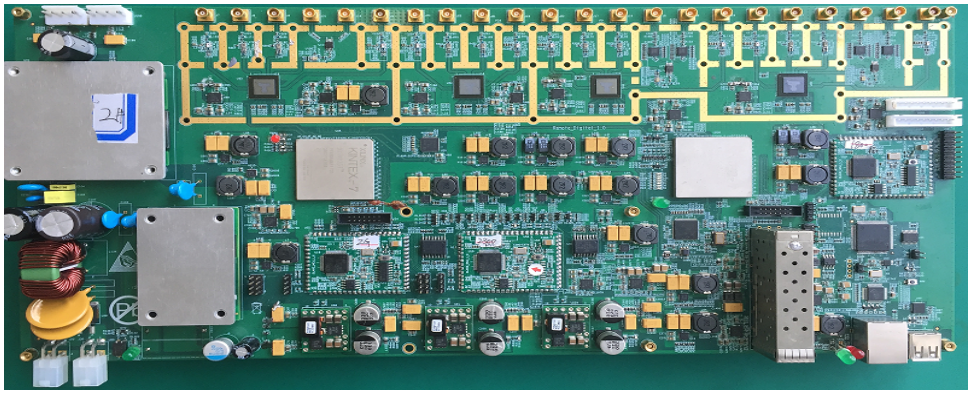


Figure 3.15: RU RF/digital card

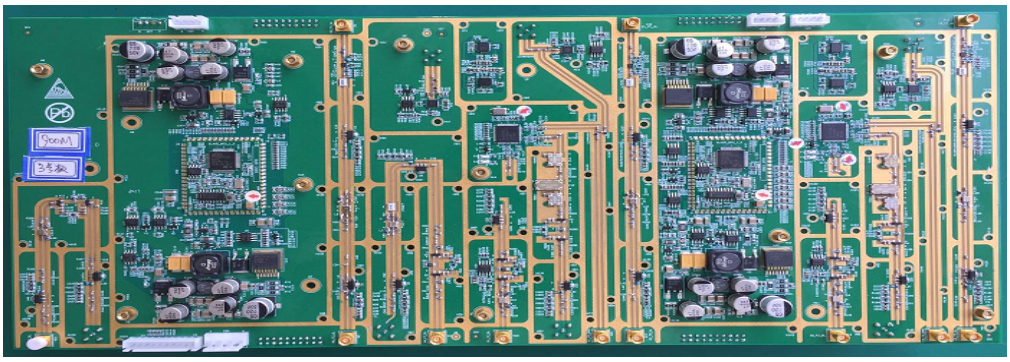


Figure 3.16: RU monitoring card

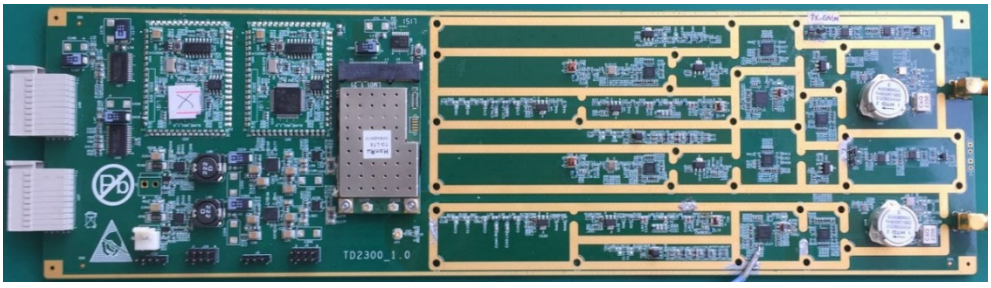


Figure 3.17: RU RF TD-LTE card

The system is tested, and the performance listed in Table 3.2.

Main Specifications	Performance
EVM	≤ 6%
Latency	≤ 7μs
Gain	≤ 55dB
Input Power	-30dBm ~ +5dBm
Transmission Power	2G:1W 3G/4G:2W
Topology	AU -> 4 EUs. AU to EU (≥ 5km). EU -> 4 levels. EU to EU (≥ 1km). EU -> 6 RUs. EU to RU (≥ 300m).
Power Dissipation	AU：250W EU：TBD RU：450W
Operating Temperature	5℃~+40℃
Operating Humidity	15% to 85%

Table 3.2: Measured system performance

The test results illustrated that the full-service DDAS system with 14 input channels meets the technical requirements provided by China Tower Ltd. The system can be used for multiple services with EVM values less than 6% and latency less than 7μs. Each Access Unit can feed four Extended Units, and six Remote Units can be connected with each Extended Unit. As each Extended Unit can be cascaded up to four levels, the full-service DDAS system supports up to 96 Remote Units.

3.3 Conclusion

In this chapter, two multi-service systems are tested. Firstly, a novel low-bandwidth multi-service DDAS is designed which can successfully transmit two channels simultaneously, one channel with LTE and the other channel for WCDM. By using the compression algorithm, the spectral efficiency is highly improved. For an LTE signal with 20MHz bandwidth, the spectral efficiency is improved by a factor of three over standard CPRI approaches.

Three different LTE modulation formats (64QAM, 16QAM and QPSK) were applied during tests of channel 0 transmission characteristics, each one with three different bandwidths (20MHz, 15MHz and 10MHz). From the testing results, it can be seen that the dynamic range of LTE signals becomes larger as the bandwidth gets narrower. On channel 1, a WCDMA signal is fed into the system with QPSK modulation. The dynamic range was approximately 62dB.

A full-service DDAS system with 14 channels is also introduced in this chapter. The system is designed for China Tower Ltd by the Beijing Institute of Aerospace Control Devices (BIACD). The full-service DDAS system has one AU, 16 EUs and up to 96 RUs. The transmission distance between AU and EU is 5km, 1km from EU to cascaded EU and 300m from EU to RU. During testing, the system performance met the technical requirements were provided by China Tower Ltd.

Chapter 4 Digital Distributed Antenna System over Ethernet

The DDAS system introduced in Chapter 3 indicates a highly efficient indoor wireless architecture, allowing infrastructure sharing among several RF services. This is an important step towards network convergence for all communication networks in buildings. Ethernet has been a standard networking protocol, primarily designed to transport digital data information for a local area network (LAN) or wide area network (WAN). Nowadays, Ethernet is used to deliver electric power to end devices, as defined in power over Ethernet (POE) standards. As Ethernet capacity grows and increases demand on fibre-based infrastructures, it is suggested that Ethernet can be used for carrying digital RoF data to the end user, effecting large scale reductions in the installation costs of indoor wireless infrastructures. However, the stringent synchronisation and latency requirements specified in RF standard serves as a bottleneck for maintaining quality of service (QoS) when utilising Ethernet protocols in these scenarios.

To overcome these problems, many solutions such as clock synchronisation and forward error correction have been considered [118]. However, technical challenges, caused by the coexistence of RF services and other higher layer services such as IPv4/6, Internet of Things (IoT) and others, may lead to loss of synchronisation, degradation of RF performance, and exceeding Ethernet capacity limits. These challenges are addressed in this chapter by introducing the Eth-DDAS architecture, a DDAS system over Ethernet solution that not only packetise DDAS data onto Ethernet frames, but also delivers a unique mechanism for maintaining frame order for RF packets over switched Ethernet networks.

Prior to implementing the DDAS over Ethernet, it is important to understand the architecture of the Ethernet sublayers, and the structure of the Ethernet frame. Ethernet technology is introduced in Section 4.1. The Eth-DDAS system architecture is introduced in Section 4.2. The method for Eth-DDAS system implementation is explained in Section 4.3, and the experimental setup and results are described in Section 4.4. Section 4.5 contributes a conclusion.

4.1 Ethernet Sublayers and Frame

4.1.1 Ethernet Sublayers

Ethernet standards set out the technology specifications for the network access layer of the TCI/IP model, focusing primarily on the data link layer and the physical layer. However, the

standard also defines the interfaces needed on different sublayers. The following figure describes the sublayers of the Ethernet.

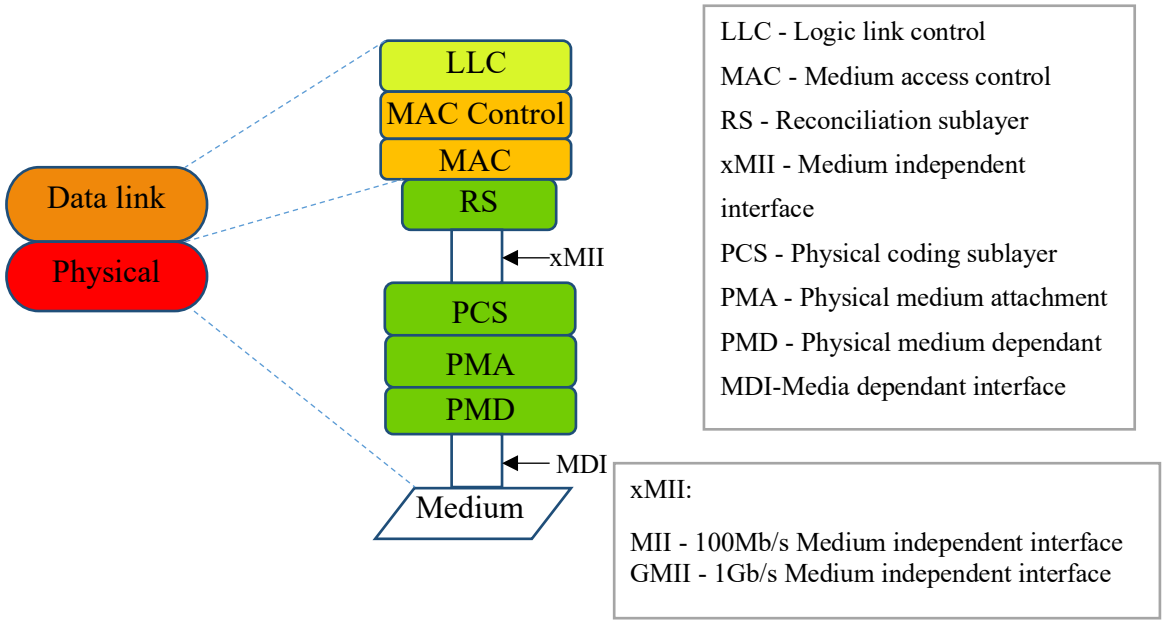


Figure 4.1: Ethernet sublayers.

The Ethernet separates the data link interface controls into two sublayers: the logic link control (LLC) sublayer and the medium access control (MAC) sublayer [119]. The LLC sublayer is used to communicate with the upper layers. Once the LLC receives IP packets from the Internet layer, control information such as frame synchronisation information is added to the packets. The reassembled packet is called a 'frame'. The LLC delivers frames to the destination node. Since the LLC is implemented by software and independent of the physical device, the function of LLC can be considered a link between the upper protocol layers and the physical equipment [120].

The MAC sublayer has two functions: data encapsulation and transmitting data into the transmission medium. For data encapsulation, the source and destination MAC addresses are added as a header to the frame, before it is transferred to the lower layer. In addition, a cyclic redundancy check (CRC) of the frame information is added as a trailer to the frame. When the frame is received by the receiver MAC layer, the receiver node creates a new CRC, based on the received frame information, and the newly created CRC is compared with the CRC in the frame to decide whether the received frame has been corrupted [121]. In addition to the data encapsulation, a full-duplex logical communication channel in a multipoint network is emulated by the MAC sublayer. This communication channel can provide broadcast, multicast, or unicast

services. If collisions occurred during the transmission, the MAC protocol can recover the lost frame.

The reconciliation sublayer (RS) is used to map commands and terminology in the MAC into an electric format that is appropriate for the lower physical layer. The medium independent interface (MII) is a standard connection between the MAC sublayer and the physical layer [122]. It is compliant with IEEE802.3 standards. Depending on the different Ethernet standards a system employs, various MII interface standards can be used to support the Ethernet standard speed. The MII is a 16-pin interface (two pins for collision and carrier indication, seven pins for data transmission, and seven pins for data reception) that supports the interface data rate up to 100Mb/s. The GMII is a 24 pins interface (two-pin for collision and carrier indication, 11 pins for data transmission and 11 pins for data reception) and the maximum interface data rate is 1Gb/s [123].

The physical layer mainly includes three sublayers: the physical coding (PCS) sublayer, the physical medium attachment (PMA) sublayer, and the physical medium dependent (PMD) sublayer. The PCS defines the coding schemes that are used. The coding schemes depend on Ethernet protocols and standards. For example, Manchester Phase Encoding (MPE) is used for a 10BaseT Ethernet system, which uses a coaxial cable to transport data, and 4B/5B coding is used for a 100BaseTX Ethernet system, which uses a CAT5e cable to transport data [124]. The PMA is used to define the standard that will be used for clock data recovery techniques. The physical property of the channel (both optics and electronics, if any) is defined by the PMD.

At the bottom of the physical layer, the medium dependent interface (MDI) is used to connect the PHY to the RJ45 connector [125]. This is a hardware connector between the electrical and physical devices. The MDI is implemented in a different manner, depending on the different media used in a system. For example, an eight pins MDI is used for twisted pair Ethernet, as shown in Figure 4.2 (a). However, for thick coaxial Ethernet, the MDI is implemented as a clamp, as shown in Figure 4.2 (b). The Ethernet device shown in Figure 4.2 (c) is an example for showing how the MDI is implemented in an Ethernet device.

(a) MDI (RJ45) (b) MDI for thick coaxial cable (c) Ethernet extender

Figure 4.2: Ethernet MDI interfaces [126].

4.1.2 Ethernet Frame

The IEEE 802.3 standard defines the structure of Ethernet frame, the details of which are graphically represented as in Figure 4.3.

Figure 4.3: Ethernet frame Figure

At the start of an Ethernet frame, seven-byte preambles are implemented. The function of the preamble bytes is to inform the receiver that a frame is starting, and allows the receiver to synchronise its clock with the incoming data. The seven-byte digits of the preamble are all the same: 10101010; the preamble is then followed by the start frame delimiter byte [123].

The start frame delimiter (SFD) is a single byte with the following form: 10101011. The SFD is a flag, which signifies that the content of the frame begins with the next byte, namely, the destination MAC address.

The destination MAC address identifies the desired receiver device, and the source MAC address identifies the source device.

The Ether-type field is used to define the protocol of the frame.

The minimum length of the payload data is 46 bytes; padding data is added if the length of the data does not meet this minimum requirement.

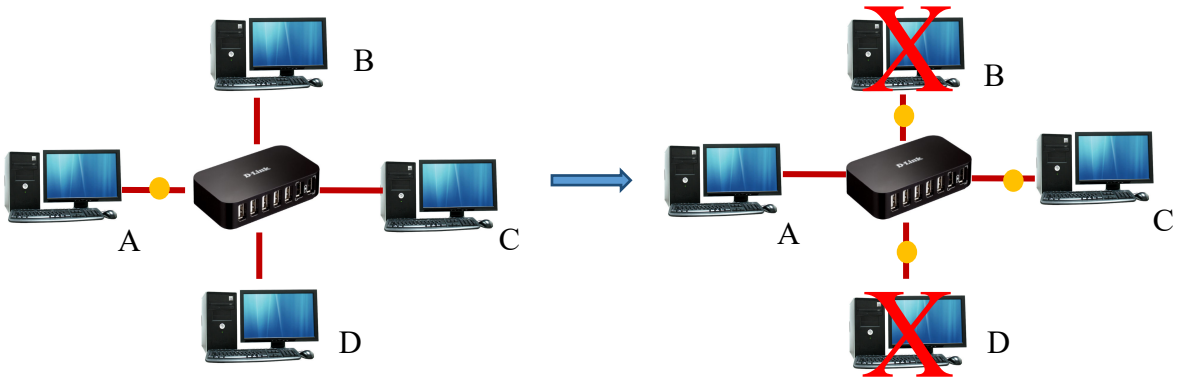
Finally, the frame ends with a frame check sequence (FCS), which is a 4-byte cyclic redundancy check (CRC).

4.1.3. Ethernet Device

To build an Ethernet system, specific hardware must be used. In this section, hubs, switches, and routers are introduced, as they are currently the most popular Ethernet devices on the market.

A hub is a layer one (physical layer) device, and has no knowledge of addresses. As the hub is implemented with multi-ports, the corresponding quantity of devices can be connected to the hub. Due to the hub having no ability to identify addresses, it broadcasts all data it receives. As a result, the hub wastes bandwidth by sending data to hosts unnecessarily, which can give rise to security issues, as anyone can receive the data and steal it [127]. As shown in Figure 4.4, if

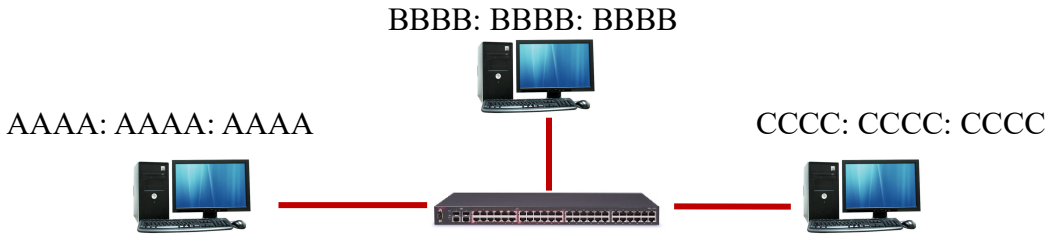
host A wishes to send data to host C, in practice, all the hosts connected to the hub receive the data. The standard requires hosts B and D to ignore the data after finding that the MAC address is not correct.



Host A sending data. All the hosts can receive data.

Figure 4.4: Data transmission using a hub.

Today, hubs have primarily been replaced by switches. A switch is a layer two (data link layer) device that needs MAC addresses [128]. A switch sets up a MAC address table, as shown in Figure 4.5, which lists each MAC address and the corresponding port it is connected to.



MAC Address	Port
AAAA: AAAA: AAAA BBBB: BBBB: BBBB CCCC: CCCC: CCCC	1 2 8

Figure 4.5: Data transmission though a switch and a MAC address table.

Since switches learn the MAC addresses of connected devices, sources do not need to send data to all other ports; thus, traffic is substantially reduced and the security of the system is improved.

In addition to a switch, Ethernet standards employ specific routers. A router is a layer three (network layer) device. It uses not only MAC addresses, but also IP addresses [129]. The function of the router is to connect the internal network to the outside network, as shown in Figure 4.6. A computer sends data to a switch firstly, then the data is sent to the router. After the router receives the data, the data is sent to the Internet using the router's IP address. A router can ensure that packets are passed to the correct Internet network destination correctly. In home Ethernet devices, a switch is generally built into a router.

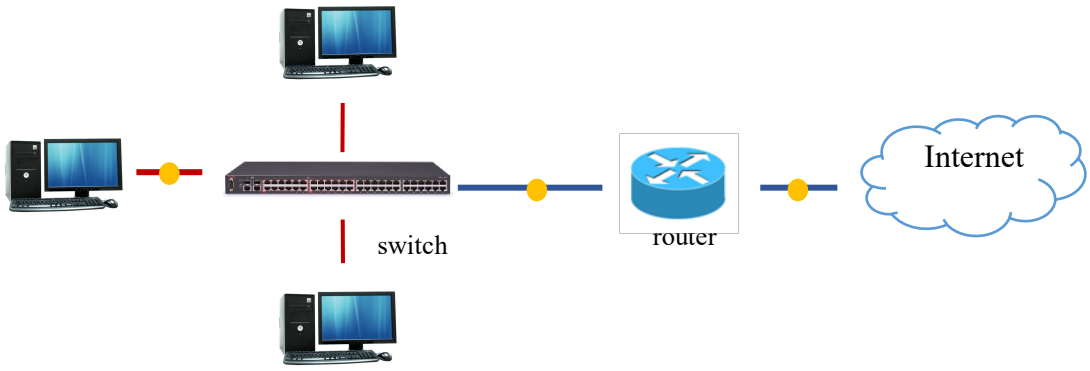


Figure 4.6: Router is used to connect to the Internet.

4.2 Eth-DDAS System Architecture

The system architecture of Eth-DDAS is graphically illustrated in Figure 4.7. It is designed as an embedded system that combines hardware and software. The system is designed to be reconfigurable through software programming. The software design is achieved by implementing a MicroBlaze microcontroller, as shown in Figure 4.7.

For the system hardware design, two paths are implemented: the data path and the control path. The function of the data path is to wrap the ADC/DAC signal into an Ethernet frame. The control path is used to monitor traffic logic, and to control submodules and peripheral modules within the FPGA.

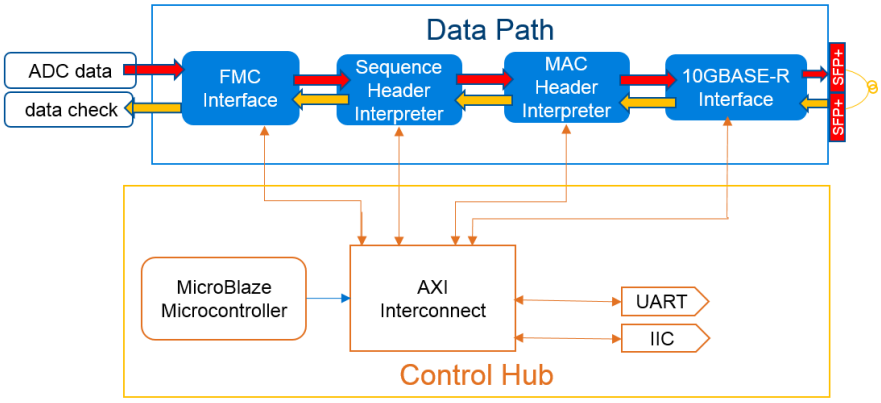


Figure 4.7: Eth-DDAS system architecture.

As shown in Figure 4.7, the data path includes four modules: the FPGA Mezzanine Card (FMC) interface, the RF header interpreter, the MAC header interpreter, and the 10G Ethernet interface. In this chapter, a block RAM (BRAM) is used to contain an LTE digital signal with a size of 14×2^{14} bits (for a signal with a bandwidth of 20 MHz, and a centre frequency of 30 MHz), which is designed to act as the system input source in front of the FMC interface module. The real time ADC signal is applied in Chapter 5. The FMC interface module is used to connect the ADC/DAC with the FPGA internal bus. Then, the reformed packets are added with a four-byte sequence header and a two-byte EtherType header, using the sequence header interpreter module. After adding the MAC source address and destination address headers using the MAC header interpreter module, packets are transmitted using a 10GBASE-R interface module. The packets are transmitted through the fibre link between the transmitter and the receiver. At the receiver, all the above added headers are removed. The recovered data is checked and compared with the original LTE data to test the performance of the system. Additional implementation details for these four modules are described in section 4.3. The frame structure of the Eth-DDAS designed for this project is illustrated in Figure 4.8. This design is based on the Ethernet frame structure introduced in section 4.3.2. This frame is implemented offline in the experiments described below.

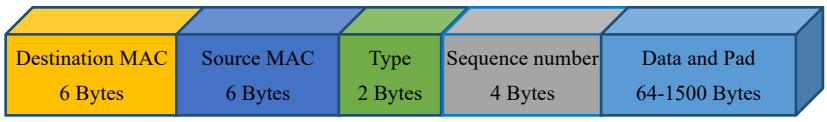


Figure 4.8: Eth-DDAS frame.

4.3 System Implementation

4.3.1 NetFPGA-SUME Board

The Eth-DDAS project is implemented using the NetFPGA-SUME, as it supports lower layer implementation down to the PMA layer. The NetFPGA-SUME is a new board that incorporates Xilinx's Vertex-7 690T FPGA, which is designed for networking infrastructure, as shown in Figure 4.9. It can be used as a multiport switch, a NIC, a test environment, and more. The NetFPGA-SUME supports 32 GTH transceivers and includes an eight-lane end-point PCI-E (Gen3×8), four SFP+ transceivers with a data rate of 10G/s, 18 GTH ports through an FMC-HPC, and two SATA-III ports. Two 4GB DDR3 SODIMMs and three 72Mbit QDRII+SRAMs are implemented as the combined memory for this board. The NetFPGA-SUME is configured and programmed by JTAG through a micro USB connector, or the Xilinx CPLD from the parallel flash. This board is developed as an open-source platform [130].

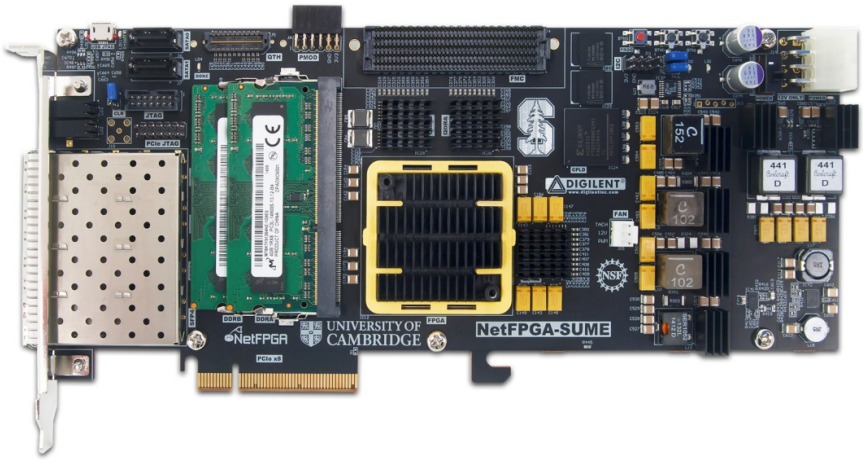


Figure 4.9: NetFPGA-SUME board [130].

4.3.2 AXI Protocol for Xilinx System Development

As the FPGA-SUME is implemented with Xilinx's Vertex-7 690T FPGA, and the Advanced eXtensible Interface (AXI) protocol was adopted by Xilinx for Intellectual Property (IP) cores when using a seven series FPGA [131], the project implemented in this chapter uses the AXI protocol as a bus interface.

The second version of AXI – AXI4, has three types: AXI4, AXI4-Lite, and AXI4-Stream. The AXI4 is used for high-performance memory mapped communication. AXI4-Lite is used for low-throughput, simple memory mapped requirements, and the AXI4-Stream is used when high

speed streaming data is transformed [132]. Generally speaking, the AXI protocol describes an interface between an AXI master and an AXI slave. The communications between the master and the slave can be divided into two categories: reading and writing.

For reading processing, a read address channel and a read data channel are implemented, as shown in Figure 4.10.

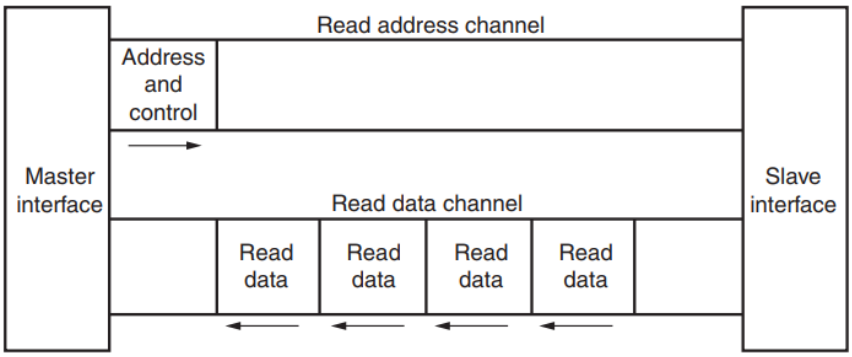


Figure 4.10: AXI4 reading channels [131].

When a master requires data reading from a slave, the required data address is first sent to the slave through the read address channel, then the slave sends the data to the master via the read data channel.

The writing process is more complex than the reading process, and a write response signal is required after the write data is received by the slave, as shown in Figure 4.11.

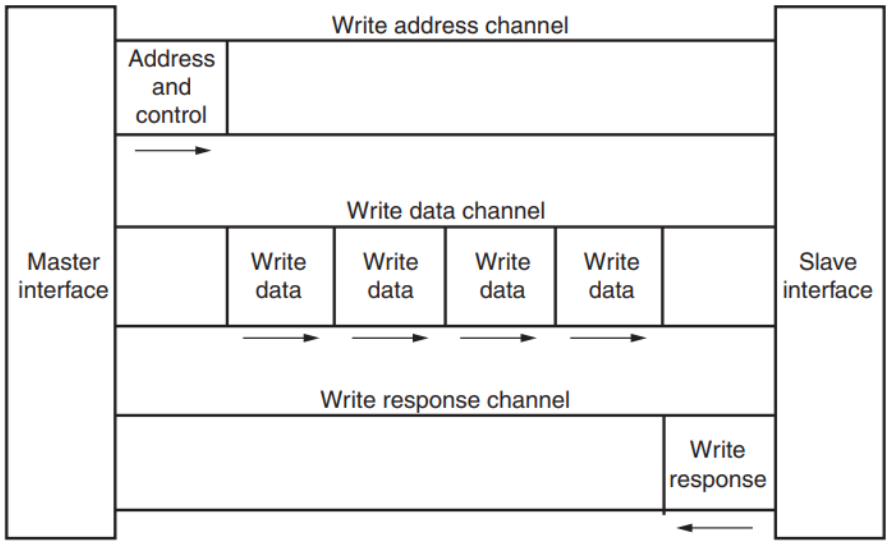


Figure 4.11: AXI4 writing channels [131].

For both reads and writes, the AXI4 supports burst of up to 256-bit data transfer cycles with a single address. This specification is important when the Eth-DDAS frame structure is designed; more details of the frame structure design is described in Section 4.3.2.

4.3.2 Design of System Modules

To implement the PMD layer, the FPGA GTH transceiver is used to drive the on-board SFP+ optical module. The transceiver fully supports the IEEE 802.3 10GBASE-R protocol. Xilinx Intellectual Property (IP) cores are used when MAC layer and PCS/PMA layer are implemented.

The following figure illustrates details of the modules implemented on NetFPGA-SUME; each of the modules is explained in this section.

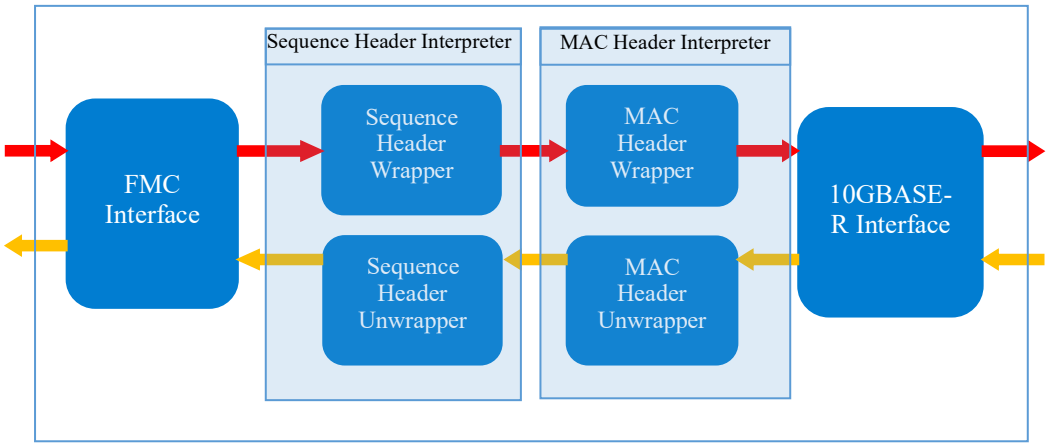


Figure 4.12: Hardware models.

FMC Interface Module

The main function of the FMC interface module is to connect the ADC/DAC to the FPGA internal bus, which includes bus width conversion and clock domain changing. For the purposes of traffic monitoring and latency measurement, a timestamp is tagged onto all packets. Meanwhile, a debug function is also implemented in this module to measure the total round-travel latency of frames, and to capture input/output data.

- Bus Width Conversion and Timestamp

Since the FPGA is designed to run with the AXI4 protocol, the bus width of which is 256-bit (as mentioned in section 4.1.4), 16 14-bit ADC data frames are cascaded and a 32-bit time-stamp is added to meet the internal bus width, as shown in Figure 4.13.

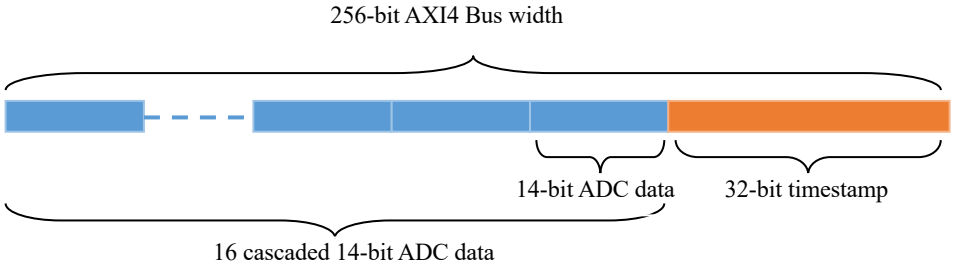


Figure 4.13: AXI4 256-bit internal bus.

The payload size of the Ethernet frame should be set between 46-byte and 1500-byte, as described in section 4.1.2.3. As the ADC digitised signal operates at 2.1 Gbps (14×150 MHz) and the SPF+ can run at 10 Gbps, there is significantly more room for headers. As the FPGA internal bus runs at a bus width of 256 bits (32 bytes), the minimum frame payload of Eth-DDAS is 64 bytes. The Eth-DDAS frame structure can therefore be adapted, as illustrated in Figure 4.14. The size of the payload can be configured using the register, which is controlled by the MicroBlaze unit.

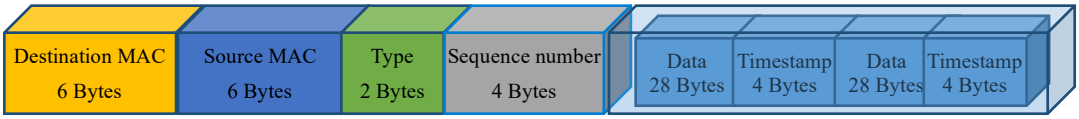


Figure 4.14: Eth-DDAS frame structure.

- Clock Domain Changing

A system is always designed with different clock domains according to its functions. In this system, there are three clock domains, as shown in Figure 4.15. As the ADC/DAC card is operated by a 150 MHz clock, the FMC interface receives data from ADC or sends data to DAC should be operated with the clock frequency of 150 MHz. The data processing modules on the FPGA are designed with a clock frequency of 180 MHz. The reason for using a clock frequency that is faster than the data input rate is to ensure every data packet received from ADC can be stored in the first-in first-out memory (FIFO), and processed by the FPGA. If the data processing progress speed is equal to or less than the data input rate, the FIFO will fill up, with ever more data arriving from the ADC. Since the 10GBASE-R interface module is designed with the Xilinx 10-Gigabit Ethernet MAC IP core – which requires running at 156.25 MHz – the 10GBASE-R Interface module should change clock domain from 180 MHz to 156.25 MHz.

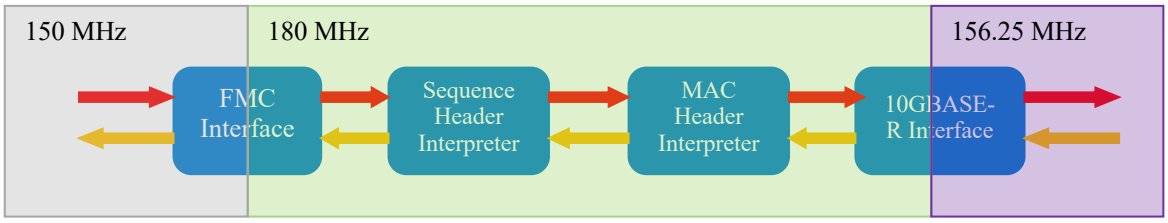


Figure 4.15: System clock domain.

The method for changing the clock domain is achieved using the Xilinx asynchronous FIFOs. The asynchronous FIFO is designed with two clock domains: a write clock domain and read clock domain. In the case of setting the asynchronous FIFO, used for receiving ADC data, the write clock domain is set to 150 MHz and the read clock domain is set to 180 MHz.

- Debug Function

The Xilinx design tool (Vivado) provides the debug function for monitoring the internal FPGA signals. By monitoring the first packet of the FMC interface module receives from ADC and the first packet of the FMC Interface Module sends to DAC, with the help of using a counter by recording the counter numbers when these two cases happen, the total round-travel latency of frames can be computed by ${}^{1}/_{180MHz} \times (Counter\ Number_{DAC} - Counter\ Number_{ADC})$. In addition, signals on any pins can be captured using the debug function.

Sequence Header Interpreter Module

The sequence number of each packet is generated by the sequence header interpreter module. Using a sequence number can improve system performance significantly. If every packet has the sequence information, packets can be ordered correctly when required, even when they travel though different switches or network paths and answer out of order. In this project, the sequence number was used to monitor current and previous packets. An error was reported if there was a mismatch with an enqueued packet.

MAC Header Interpreter Module

The MAC header interpreter module is used to add the EtherType header and the MAC address header (source MAC address and destination address). The default configuration for EtherType is 0x0800, which indicates that this is an IPv4 packet. The MAC address header and the EtherType header are readable and configurable by the MicroBlaze unit. A user can easily change the header information using MicroBlaze in order to meet network environments.

10GBASE-R Interface Module

The 10GBASE-R interface module is implemented based on the Xilinx AXIS 10G subsystem IP core, with additional logic contributed by the NetFPGA project [130]. The Xilinx 10G subsystem includes a configurable MAC IP core and PCS/PMA IP core. They are configured to meet the IEEE 802.3 10GBASE-R standard. The forward error correction (FEC) function is generally used for recovering corrupted data in the PCS/PMA module. Since the latency requirement is more restricted in this system, the FEC function is disabled. Moreover, for better timing, a reference SFP+ clock of 156.25 MHz is used, rather than 312.5 MHz.

4.4 Experimental Setup and Results

In order to determine the potential of the system, it is important to test the Eth-DDAS system latency and reliability of recovering a processed signal correctly. To determine the reliability, experiments are setup as represented in *Setup A* and *Setup* C, shown in Figure 4.16. To measure the system latency over a switch, experimental *Setup B* is designed.

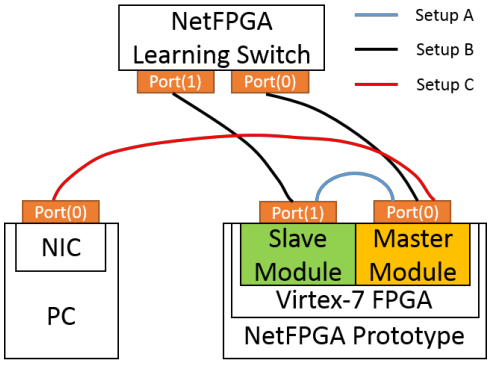


Figure 4.16: Experimental setup.

1) Setup A is self-loopback test.
2) Setup B is a test over a switch.
3) Setup C is a test that connects to the host PC directly.

4.4.1 Signal Recovery Overview

Experiments for *Setup A* and *Setup C* are carried out to test if the ADC digital signals are successfully received after propagating through the Ethernet link.

Self-loopback testing is conducted using *Setup A*. Here, Ethernet port 0 is set as the transmitter port (master port), and is connected to Ethernet port 1 (receiver port or slave port). By capturing the first packet that the FMC module receives from the ADC source, and the first packet that

the FMC module sends to the DAC side, it can be found that the identical waveform from the ADC input is observed at the DAC output as shown in Figure 4.17. The data is successfully recovered without significant distortion.

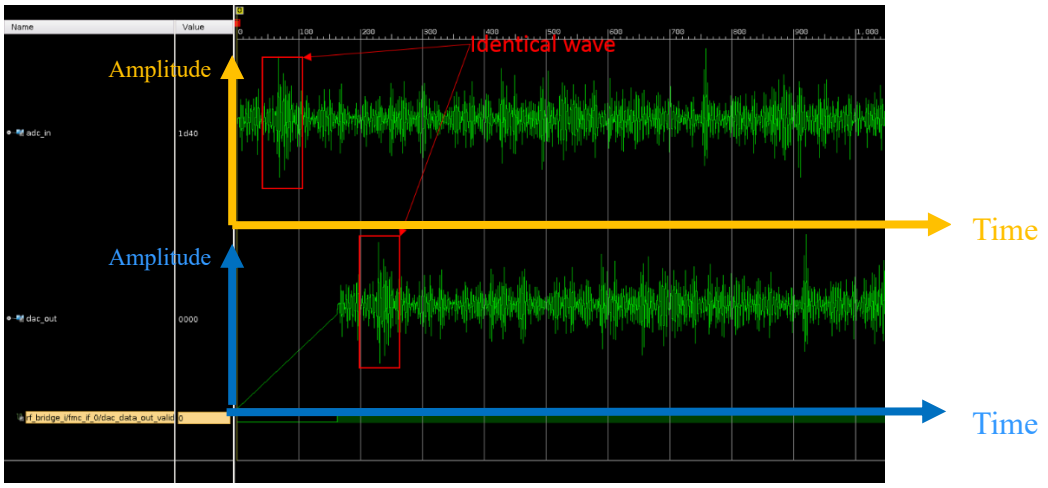


Figure 4.17: Identical waveform from ADC input and DAC output.

Secondly, it is very important to ensure the generated packets meet Ethernet standards, and can be transmitted through a third party device using the IEEE 802.3 10GBASE-R standard. As a result, experimental *Setup C* is established. A Solarflare SFC9020 10GbE NIC is employed as an endpoint receiver, as shown in Figure 4.16, and is connected to Ethernet port 0 (transmitter port). In this experiment, the source MAC address and destination MAC address are configured using MicroBlaze to 02:53:55:4d:45:00 and 02:53:55:4d:45:01, respectively. On the host PC side, a TCPDUMP session is employed to monitor the traffic. Figure 4.18 shows the first packet received by the host PC. The destination MAC address, source MAC address, and EtherType information are successfully added to the packet.

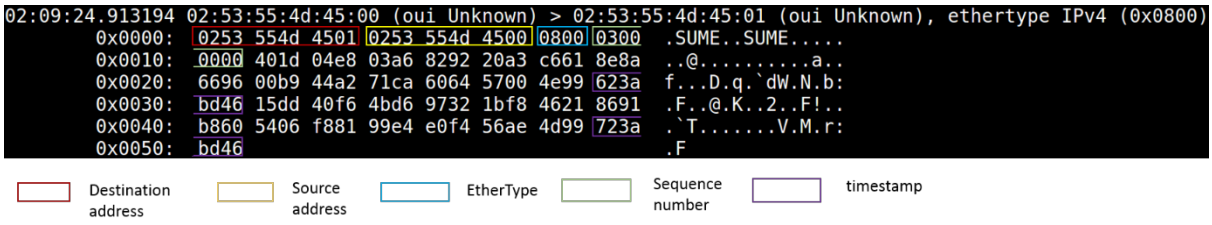


Figure 4.18: Packet captured by TCPDUMP.

4.4.2 Latency Measurement

The Eth-DDAS system latency is contributed from both fibre transmission and digital system processing. The OM2 fibre with LC connectors is used in this experiment, which introduces a latency of 5 ns/m [84]. Two 5m fibres are used in this experimental setup, which introduce a 50 ns latency. Digital processing is expected to introduce the majority of system latency.

In order to measure the system latency accurately, a first-out-first-in timestamp mechanism is implemented, as explained in Section 4.3. A timestamp is tagged at the first arrival frame from ADC and computed at the first arrival of the AXI4 stream data frame (FPGA internal bus). Meanwhile, the clock for computing the timestamp is an on-board MMCM-generated clock, which runs synchronously with the ADC module at 150 MHz. Such a clock offers a resolution of 6.67 ns. To compare the times of the same packet before sending and after arriving, latency can easily be computed, i.e. the difference between two time points.

A NetFPGA learning switch is also created for measuring cross-switch latency. The switch for the experiment is a reference switch from the NetFPGA-SUME project. It is a pure layer, two-learning switch with an internal lookup table that runs a round-robin algorithm for switching.

The latency of three loopbacks is measured: FMC loopback (*Setup C*), 10G loopback (*Setup A*), and switch loopback (*Setup B*). The latency of different payload sizes is measured as shown in Table 1.

Payload size	**FMC loopback**	**10G loopback**	**Switch loopback**
64 Bytes	346(±7) ns	1026(±7) ns	1846(±7) ns
512 Bytes	513(±7) ns	1253(±7) ns	2386(±7) ns

Table 3.3: Latency measurements for different payload sizes.

From the measurement results, it is found that the larger packets contribute high latency to the system as they need more clock cycles to process data. There is a trade-off between latency and the headers introduced to the system. Although a small-size packet can reduce packet latency, a greater proportion of header bits rather to data information are transported inside the system.

4.4.3 Error Frame

To test the system's reliability, the transmitted frames are captured and compared with the original LTE data dump stored in BRAM. A test program is designed to continuously push this dump data as the input data source. PC NIC is connected with Master Port 0, as shown in Figure 4.16 (*Setup C*). After the data is received by PC NIC, TCPDUMP is used to capture the data and store it into a file called 'Packet Capture'. The captured data is then recovered and compared with the original LTE data dump stored in BRAM. After running for more than 12 hours, a total number of 76578301 packets are captured, with 0 error frames received.

4.5 Conclusions

In this chapter, the design implemented for and the testing of the Eth-DDAS is reported. As the Eth-DDAS system combines the DDAS system and Ethernet protocol, the DDAS data is successfully carried over a standard Ethernet network. The experimental results show that the transmitted digitised RF signal is successfully recovered after processing, with 0 error frames received after running for more than 12 hours. Several latency scenarios are tested with different payload sizes. The 10G loopback with a payload size of 64 bytes contributes a latency of 1026 ns to the system, where a single Ethernet switch stage adds 820 ns to the latency. Increasing the size of the payload would introduce more latency, but the relative size of the headers decreased. This chapter thus demonstrates the feasibility of the Eth-DDAS architecture. To test the system in real-life implementations, a real-time Eth-DDAS system will be demonstrated in Chapter 5.

Chapter 5 Real-time Eth-DDAS System

Chapter 4 describes the implementation of the Eth-DDAS system using the NetFPGA platform. Digital RF data is first stored offline in the FPGA registers before Ethernet packetisation and processing. Regarding the performance of the system in real time, RF carriers generated from the vector signal generators (VSG) are first digitised by a dual-channel FMC142 ADC/DAC card with the FPGA mezzanine card (FMC) HPC connector for FPGA interfacing. The real-time testing platform is designed and implemented as shown in Figure 5.1. Compared with the system architecture introduced in Chapter 4, the FMC142_Connector module is able to take real RF inputs as a signal source and recover the signal back to its analogue domain at the reverse link. This is an essential step towards real-life implementation of the Eth-DDAS architecture and the RF performance can then be measured in real-time so that quality of services (QoS) of the cellular network can be assured.

The main functions of this module are:

1. Receive sampled ADC data from the FMC142 card.
2. Send DAC data to the FMC142 card.
3. Configure the FMC142 card through SPI interface.

To design the real-time system, a proper ADC/DAC card needs to be selected. The FMC142 card is first introduced in Section 5.1. To make sure the FMC142 card can work properly and the FMC142_Connector module is implemented successfully, a project ‘FMC142_Connctor Interface’ concentrating on the FMC142 interfaces and configurations is built and tested and the design details are described in Section 5.2. After the FMC142 interfaces and configurations are successfully implemented, the real-time Eth-DDAS system is then able to be built. The system performance is tested and the test results are introduced in Section 5.3. The system performance is compared and analysed in Section 5.4. Section 5.5 introduces the conclusions.

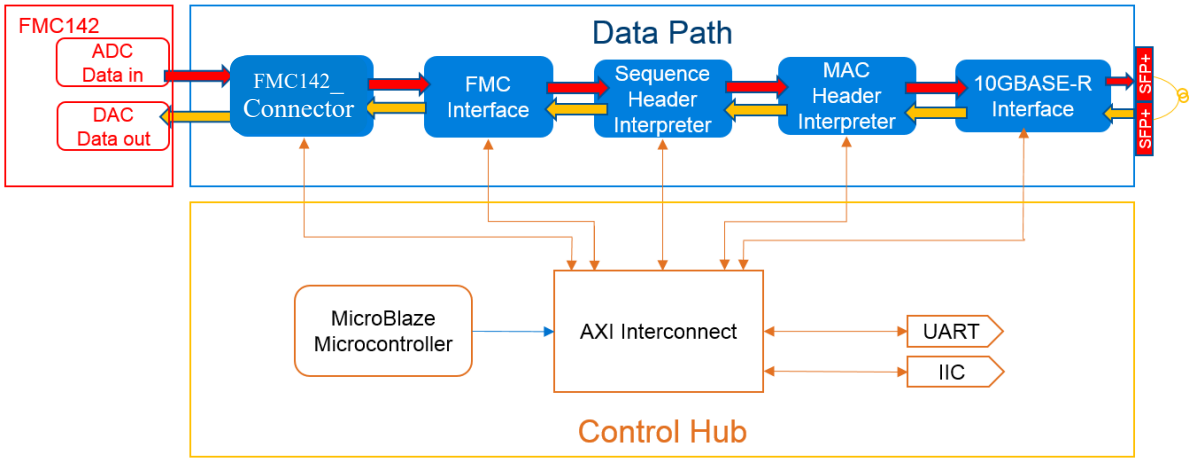


Figure 5.1: Real-time system architecture

5.1 ADC/DAC Card Selection

A lot of ADC/DAC products developed by third-party companies can be found on the market so selecting the proper ADC/DAC card for the design is not an easy task. First of all, cards that are implemented with both ADC and DAC will be considered. Second, the card should have multiple channels (≥ 2). Third, the sampling rate should be over 150 MHz and the resolution bit should be between 14 and 16 bits. Finally, the card should be compatible with an FPGA FMC connector. After considering these factors, three ADC/DAC cards are chosen as the appropriate options: FMC150, FMCDAQ2, and FMC142.

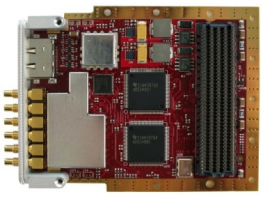
FMC150		Interface: LVDS FMC type: LPC			
ADC			DAC		
Channels	Sample Rate (MSPS)	Resolution (bits)	Channels	Sample Rate (MSPS)	Resolution (bits)
2	250	14	2	800	16

Table 5.1: FMC150 [133]

5.1 ADC/DAC Card Selection

FMCDAQ2		Interface: JESD204B FMC type: HPC			
ADC			DAC		
Channels	Sample Rate (MSPS)	Resolution (bits)	Channels	Sample Rate (MSPS)	Resolution (bits)
2	1000	14	2	2800	16

Table 5.2: FMCDAQ2 [134]

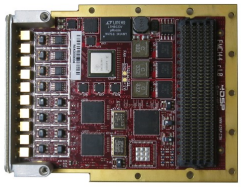
FMC142		Interface: JESD204B FMC type: HPC			
ADC			DAC		
Channels	Sample Rate (MSPS)	Resolution (bits)	Channels	Sample Rate (MSPS)	Resolution (bits)
2	370	16	2	2500	16

Table 5.3: FMC142 [135]

Comparing the interface of the FMC150 with that of FMCDAQ2 and FMC142, FMC150 uses the low-voltage differential signalling (LVDS) technology as the interface standard while FMCDAQ2 and FMC142 use the JESD204B interface standard. JESD204B is a new converter interface. With the increase in converter speed and resolution, a new interface with efficiency in terms of cost, size, and speed is required [136]. The benefits of JESD204B over LVDS include:

- Faster speed: JESD204B supports a data rate of 12.5 Gbps [136].
- Smaller package size: the pin count of JESD204B is lower than that of the LVDS interface.

- Lower cost: the design of the board is easier because of the number of trace routes for JESD204B is reduced.

Comparing the FMCDAQ2 and FMC142, although the FMCDAQ2 supports a higher sampling rate, the resolution bit of ADC and DAC is different. To simplify the FPGA programming, ADC and DAC with the same bit resolution bit is preferred. In addition, the sampling rate of the FMC142 is high enough for this application. As a result, the FMC142 card was selected as the ADC/DAC card for the real-time Eth-DDAS system.

- **ADC/DAC FMC142 Card**

FMC142 is an ADC/DAC FMC card with two channels of A/D and two channels of D/A [135]. The ADC device used for this card is ADC16DX370, which is a dual-channel ADC chip with a 16-bit resolution and a maximum 370 Msps sampling rate. DAC38J84 is implemented as the DAC chip for this card, which is a quad-channel chip with a 16-bit resolution and a maximum sampling rate of 2.5 Gsps [134]. The FMC142 card has 6 SSMC/MMCX connectors on the front panel: two analogue inputs, two digital outputs, one external clock, and one external trigger. The block diagram of the FMC142 is shown in Figure 5.2.

Apart from the ADC/DAC chip, an LMK04828B chip is used as the internal clock generator. In addition, an AMC7823 is implemented to monitor the temperature on the board as well as several power supply voltages [135]. The ADC and DAC data is transferred via JESD204B subclass 1-coded differential pairs that connect with the GBT pins on the FMC connector. Each ADC or DAC channel has two lanes of JESD204B. More details of each component on the FMC142 card are explained over the following section.

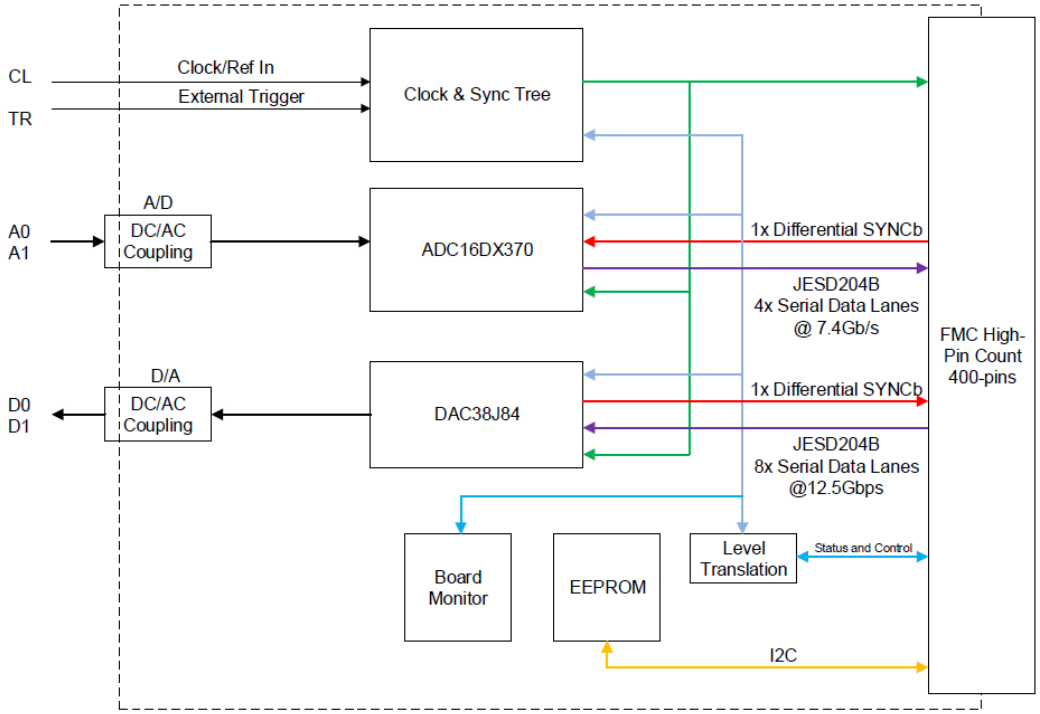


Figure 5.2: FMC142 block diagram [137]

ADC16DX370

The ADC chip implemented on the FMC142 card is the ADC16DX370. The ADC16DX370 device is a dual-channel analogue to digital converter with a 16-bit resolution and a sampling rate of 370 MSPS. The JESD204B subclass 1 interface is designed to output the digital signal and the ADC16DX370 is configured via an SPI interface [138].

DAC38J84

The DAC38J64 is implemented on the FMC142 card. The DAC38J64 device is a quad channel, low power with 16-bit resolution and 2.5 GSPS sampling rate digital to analogue converter. The digital signals sent to the DAC38J64 via the JESD204B interface and the device is configured through an SPI interface [139].

Clock Tree LMK04828B

The FMC142 card has three different clocking architectures [137]:

- Internal clock with internal reference (clock mode 1)
- Internal clock with external reference (clock mode 2)
- External clock (clock mode 3)

For this design, the internal clock with internal reference clock architecture is used as there is no need for an external clock or an external reference. The LMK04828B is implemented on the FMC142 card as the internal clock, which is a high-performance clock conditioner with JESD204B support. When the FMC142 card is configured to clock mode 1, an onboard 491.51MHz crystal oscillator is used as the internal reference [137]. Up to 7 SYSREF clock outputs are supported by the PLL and each output has its own clock divider. For this design, three pairs of clocks and SYSREF outputs are used and assigned to three devices: the FPGA over FMC connector, the onboard ADC, and DAC. In addition, two clocks from the LMK04828B are allocated to the gigabit transceivers over the HPC interface. The clocking architecture of this design is shown in Figure 5.3.

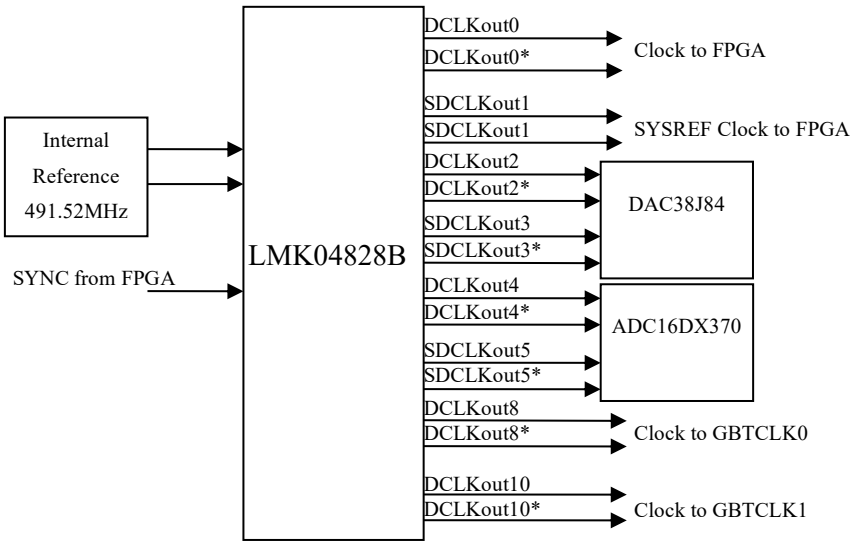


Figure 5.3: LMK04828 clock outputs

5.2 FMC142_Connector Interface Design

The FMC142 card connects the FPGA via a HPC connector and the connection is shown in Figure 5.4. The FPGA is configured through the UART port.

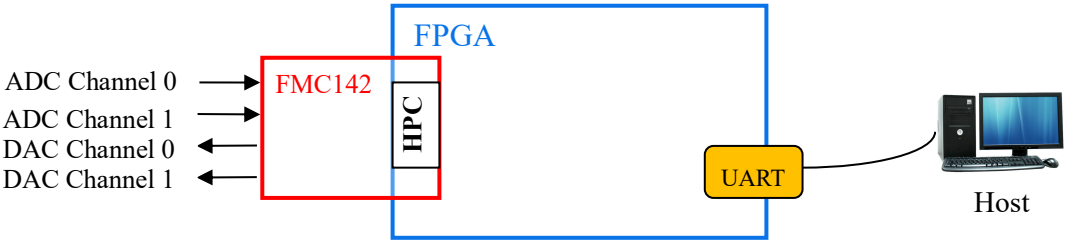


Figure 5.4: Hardware topology

5.2.1 FMC142_Connector Interface Hardware Design

To make sure the interface can work properly, project FMC142_Connector Interface only concentrates on the interface connections and the FMC142 card configurations are implemented. The block diagram of the project FMC142_Connector Interface is shown in Figure 5.5.

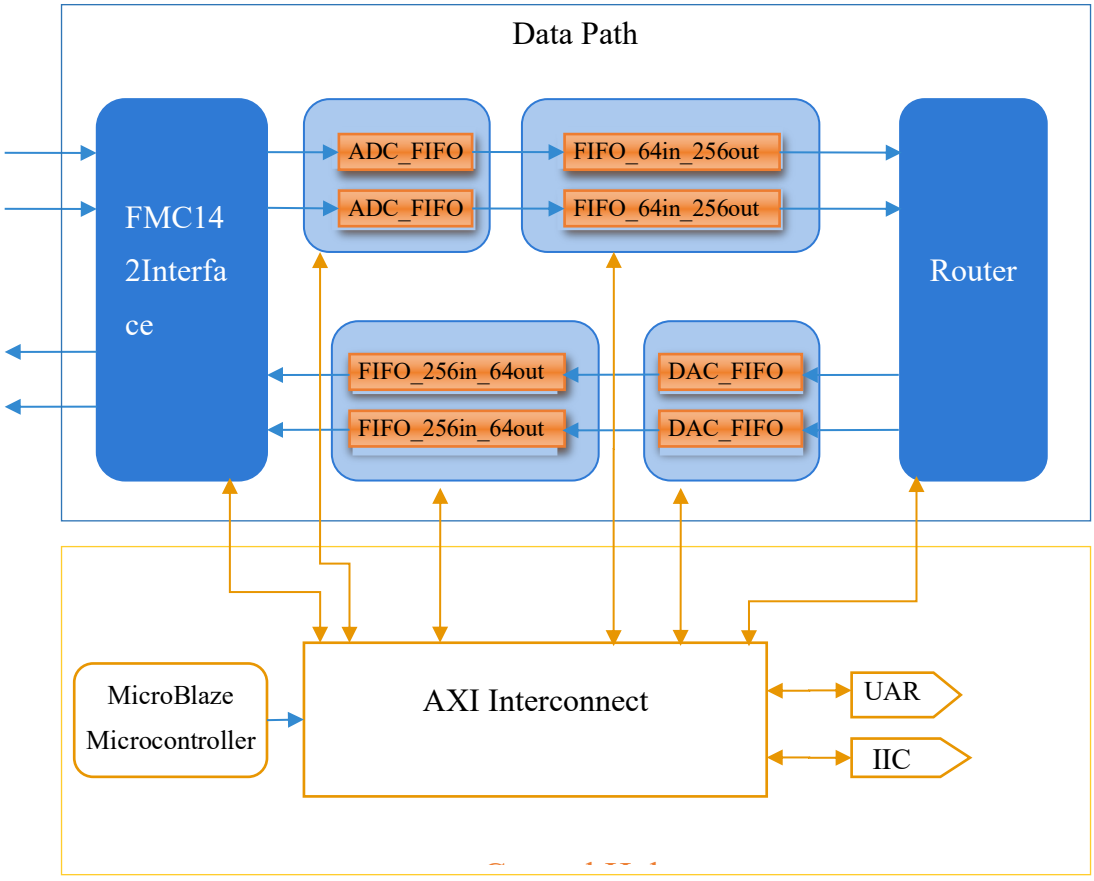


Figure 5.5: FMC142_Connector interface block diagram

e

module, the ADC_FIFO, the DAC_FIFO, the FIFO_64in_256out, the FIFO_256in_64out, and

the router. The FMC142_interface module receives sampled data from the ADC and then the sampled ADC data is captured by the ADC_FIFO, and clock domain of the ADC data is changed. As the onboard buses are configured with a data width of 256 bits, the FIFO_64in_256out module is implemented to convert the data bus width. A router is implemented to connect two ADC channels with two DAC channels. The DAC_FIFO module is used to transform the clock domain. Before the data is sent to the DAC via the FMC142_interface module, the FIFO_256in_64out module is implemented to convert the bus width from 256 bits to 64 bits.

To design the control hub, an AXI Interconnect is implemented to merge all the commands it received from the host to the relative modules. More details of each module are explained in the following sections.

Clock Design on the FPGA Board

The clock design for the FPGA modules is shown in Figure 5.6. There are three clocks for this design: *GBT_clk*, *axi_lite_clk,* and *axi_stream_clk*. As described in Section 5.1, the LMK04828B provides a GBT clock to drive the transceivers implemented on the FPGA via the HPC connector. This clock (*GBT_clk*) is synchronised with another clock generated by the LMK04828B. The *GBT_clk* is used as the transceiver reference clock.

The onboard clock is used as the clock source on the FPGA board. The clocking wizard IP core provided by Xilinx is used to configure the onboard clock source. Two clocks are generated: *axi_lite_clk* and *axi_stream_clk.* The *axi_lite_clk* is used for clocking the axi commands and it connects all the modules on the FPGA board. The *axi_stream_clk* is used for clocking the streamed data. Figure 5.6 indicates the clock domains of the data path of the FMC142_Connector interface.

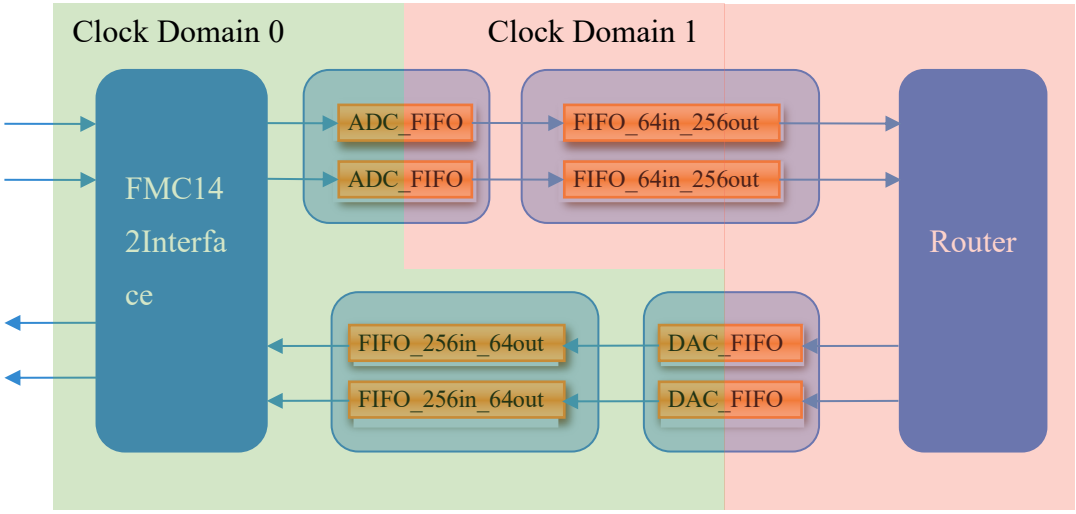


Figure 5.6: Clock domains

Clock domain 0 uses the *GBT_clk* to clock the data and *axi_stream_clk* is used as the clock for clock domain 1. In addition, the clock, *axi_lite_clk,* generated by the clocking wizard IP core clocks the command path of all the modules as shown in Figure 5.7.

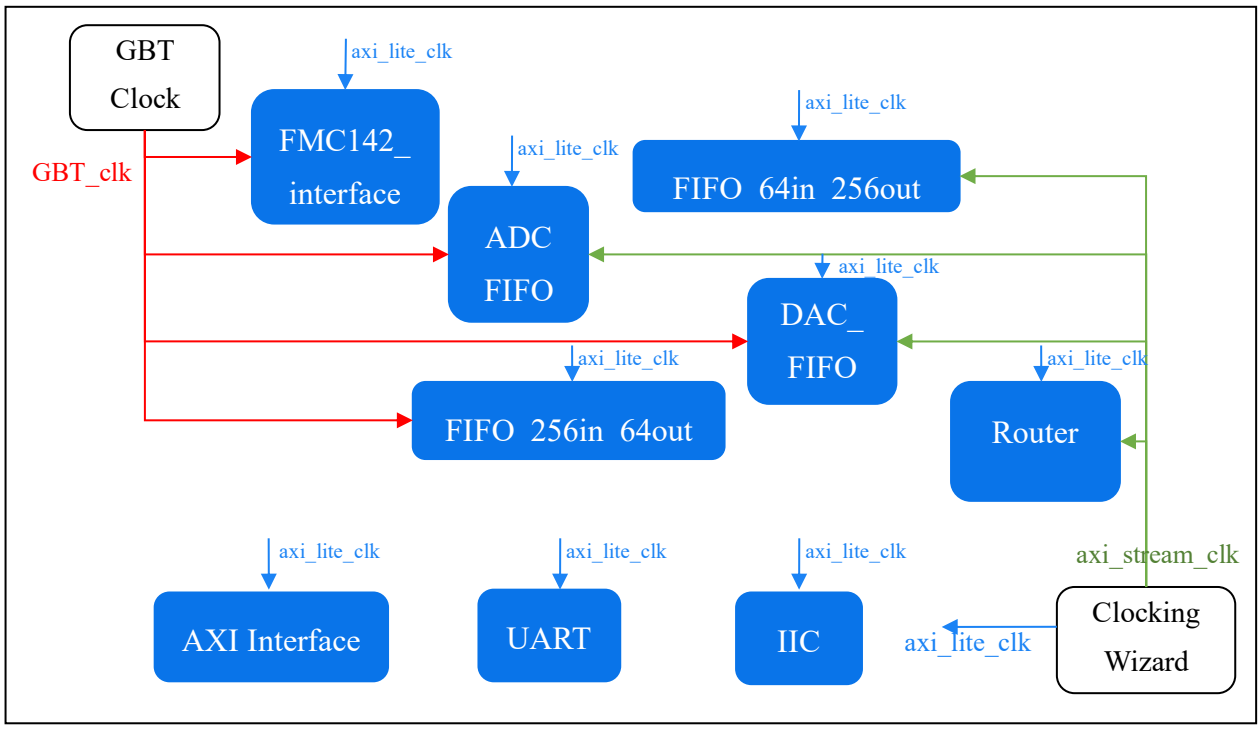


Figure 5.7: Clock for modules

FMC142_interface Module

The main function of this module is to connect the FPGA with the FMC142 card. This module has three main features:

- Receive data from ADC
- Transmit data to DAC
- Control the FMC142 card through SPI interface

To achieve these functions, the *FMC142_interface* module is implemented with three blocks: the Xilinx 7 Series FPGAs transceivers, the JESD204B core, and the SPI control block. The block diagram is shown in Figure 5.8.

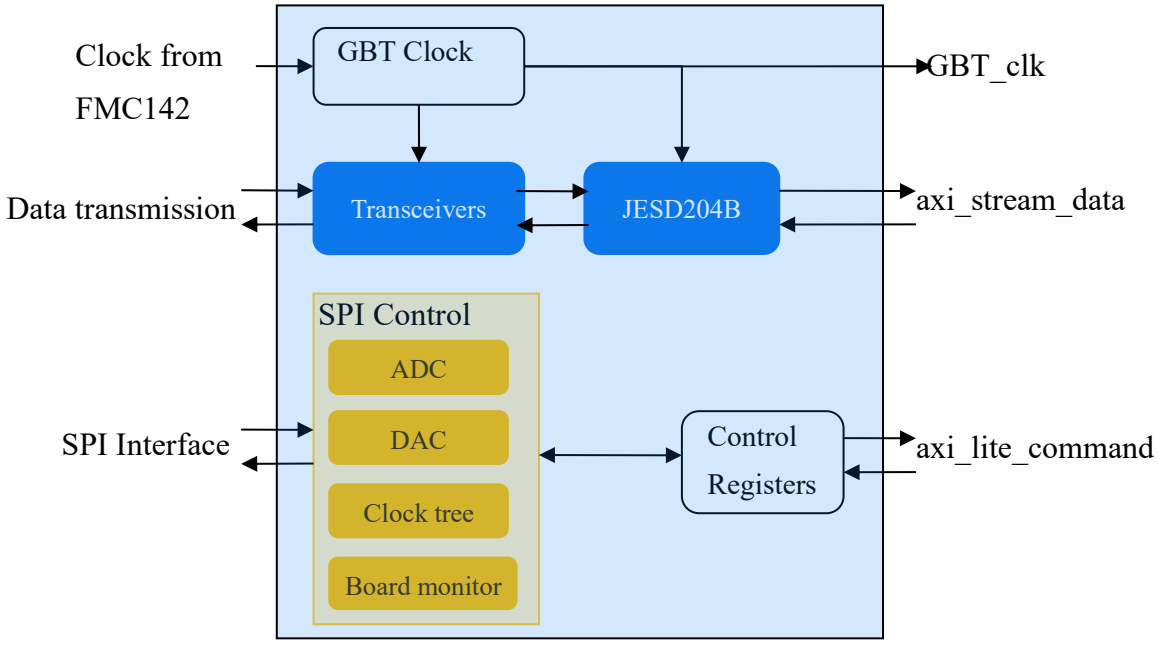


Figure 5.8: FMC142_interface module block diagram

- Transceiver IP Core and JESD204B IP Core

As the FMC142 card has two channels of ADC and the JESD204B supports a two-lane per link, thus, there is a four-lane for two channels of ADC. Although the number of lanes for dual-channel DAC38J84 JESD204B can be configured to be 8, 4, 2, or 1, by considering the link data rate matching, 4-lane JESD204B is used for DAC. Therefore, a total number of four transceivers are used to transmit and receive data. The transceiver block is implemented with the help of the 7 Series FPGAs Transceivers Wizard IP Core supported by Xilinx. By using this

wizard, the Xilinx 7 Series FPGA chip transceivers can be custom configured. The following table indicates the setting of key parameters:

Transceiver Parameters	TX	RX
Line Rate (Gbps)	1.5	1.5
Reference Clock (MHz)	37.5	37.5
External Data Width (Bits)	32	32
Encoding	8B/10B	8B/10B
Internal Data Width (Bits)	40	40

Table 5.4: Transceiver parameters setting

The transmitter line rate is determined by the sample rate of ADC (F_s) and the number of JESD204B lane settings. The total number of ADC output data is $F_s \times 16 \times \left(\frac{10}{8}\right) Mbps$. Therefore, the line rate is 20 times F_s when the JESD204B is configured as a 1-line interface and the line rate is ten times F_s if the JESD204B is configured as a 2-line interface. In this design, the ADC sampling rate is configured as 150 MHz and the 2-line JESD204B is used, thus the line rate of the transmitter is 1.5 Gbps. As the serial data will be converted to parallel data inside the transmitter and the reference clock is used to drive the transceiver block, so the reference clock is equal to $\frac{Line\ Rate}{Internal\ Data\ Width}$. In this case, the reference clock $= \frac{1.5\ G}{40} =$ 37.5 MHz.

The JESD204B IP core is used and the JESD204B parameters are configured as displayed in Table 5.5.

JESD204B Parameters	Description	ADC	DAC
M	Number of converters per device	2	2
L	Number of lanes per link	4	4
F	Number of octets per frame	1	1

Table 5.5: JESD204B parameters setting

By using the JESD204B IP core, the 2-line data output is combined together. As the external data width of the transceiver is configured to 32 bits as shown in Table 5.1, thus the data width of JESD204B output is 64 bits.

- SPI Controller

The SPI controller is used to configure and control the FMC142 card. All the devices on the FMC142 card are controlled by configuring their corresponding device registers. In this design, four SPI controllers are implemented as shown in Figure 5.8. The address offset of each SPI controller is indicated in Table 5.3.

Address Offset	SPI Controller	Device
0x00-0x03	ADC16DX370	ADC
0x04-0x07	DAC38J74	DAC
0x08-0x0B	LMK04828	Clock tree
0x0C-0x0F	AMC7823	Monitor

Table 5.6: SPI controllers

For each SPI controller, four registers are implemented. The function of each register is listed in Table 5.7.

Address Offset	Read	Write
0x00	BIT[31:0] SPI Address	BIT[31:0] SPI Address
0x01	N/A	BIT[31:0] SPI Write Data
0x02	Bit[1] Valid data Bit[0] Busy	Bit[1] Perform Read Bit[0] Perform Write
0x03	Bit[31:0] SPI Read Data	N/A

Table 5.7: Registers for SPI controller

The commands sent from the host are received and stored by the control registers block. For example, if the host sends an ADC SPI writing command, the first register allocated to ADC

will store the SPI address and the second register allocated to ADC will store the SPI data. When the SPI bus is ready, the address and the data will be sent to the ADC relative registers on the FMC142 card via the SPI interface.

ADC_FIFO

This ADC_FIFO is designed for two reasons:

- To store the streaming data sent from the *FMC142_interface* module for later use.
- To change the stream data clock domain from GBT_clock to *axi_stream_clock*.

The block diagram of ADC_FIFO is shown in Figure 5.9. The *s_axis_data* port receives the streaming data from the previous module, *FMC142_interface*, at the clock domain of the transceiver reference clock (37.5 MHz). Due to the axi stream, the clock is designed to 180 MHz, as discussed in the previous section, thus the clock domain of the stream data output *m_axis_data* is changed to 180 MHz.

A FIFO is implemented with a data width of 64 bits. The writing data clock (s_axis_clk) is configured to 37.5 MHz and the reading data clock (m_axis_clk) is configured to 180 MHz.

Figure 5.9: ADC_FIFO block diagram

FIFO_64in_256out

The project is designed to run with the AXI4 protocol and a bus width is 256 bits as described in Section 4.3.2. This module is used for converting the data width from 64 bits to 256 bits. To achieve this function, a FIFO with 64 bits of writing data width and 256 bits of reading data width is implemented as shown in Figure 5.10.

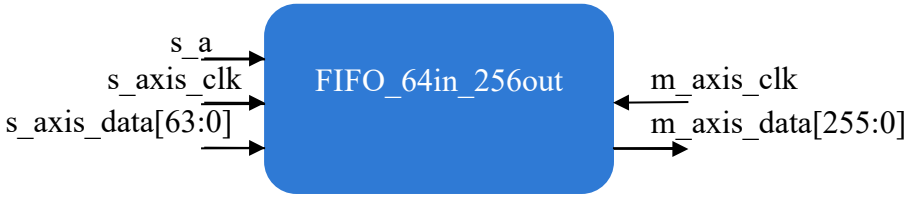


Figure 5.10: ADC_FIFO block diagram

Router

This IP core connects the two ADC channels and the two DAC channels. Data from one input can be routed to any output. By configuring the IP core register map, we can change the way data is routed. The block diagram of the router is shown in Figure 5.11.

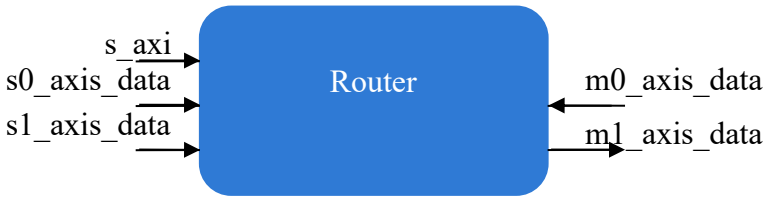


Figure 5.11: Router block diagram

The router has two input stream data ports and two output stream data ports. The *s_axi* is used to control the register map of this IP core and the details of the register map are shown in Table 5.8.

Address Offset	Register Function	Example Value	Description for example value
0x00	Route selection for m0	0x00000001	m0 connects to s1
0x01	Route selection for m1	0x00000000	m1 connects to s0

Table 5.8: Router register map

The first register is used for configuring the route for *m0_axis_data* and the second register is used for *m1_axis_data*. As the example shown in Table 5.5, the output *m0_axis_data* is routed to *s1_axis_data* when the first register is configured to 0x00000001. The input port *s0_axis_data* or *s1_axis_data* can connect to m0 and m1 at the same time, but the output can only connect one input.

The router is implemented by using the Xilinx AXI4-Stream Register Slice. Four Xilinx AXI4-Stream Register Slices are used, two for input and two for output. By changing the internal connection, the data route is changed.

DAC_FIFO

Due to the data sent to DAC via transceivers implemented in the *FMC142_interface* module and the clock of the *FMC142_interface* module operating at 37.5 MHz, the clock domain of the stream data needs to be changed. A FIFO is implemented to achieve this purpose with a writing data clock at 180 MHz and a reading data clock at 37.5 MHz.

Figure 5.12: DAC_FIFO block diagram

FIFO_256in_64out

This module has a revise function of the *FIFO_64in_256out* module and is used for converting the data width from 256 bits to 64 bits. A FIFO with 256 bits of writing data width and 64 bits of reading data width is implemented.

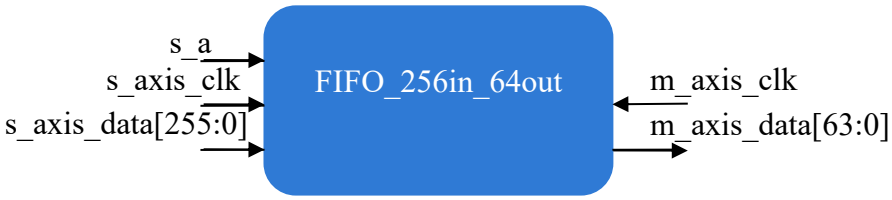


Figure 5.13: : FIFO 256-bit Input 64-bit Output

5.2.2 Software Design

The software design is achieved by using Xilinx Software Development Kit (Xilinx SDK). The main functions of the software design of this project include:

- Configuring the FMC142 card
- Configuring the parameters of hardware modules

The configuration of the FMC142 card is achieved via SPI interface. As mentioned in Section 5.2.1, four SPI controllers are implemented on the FPGA. By sending commands to the relative

registers, components (ADC16DX370, DAC38J74, LMK04828, and AMC7823) on the FMC142 card are configured. The design flow and key configurations are shown in Figure 5.14.

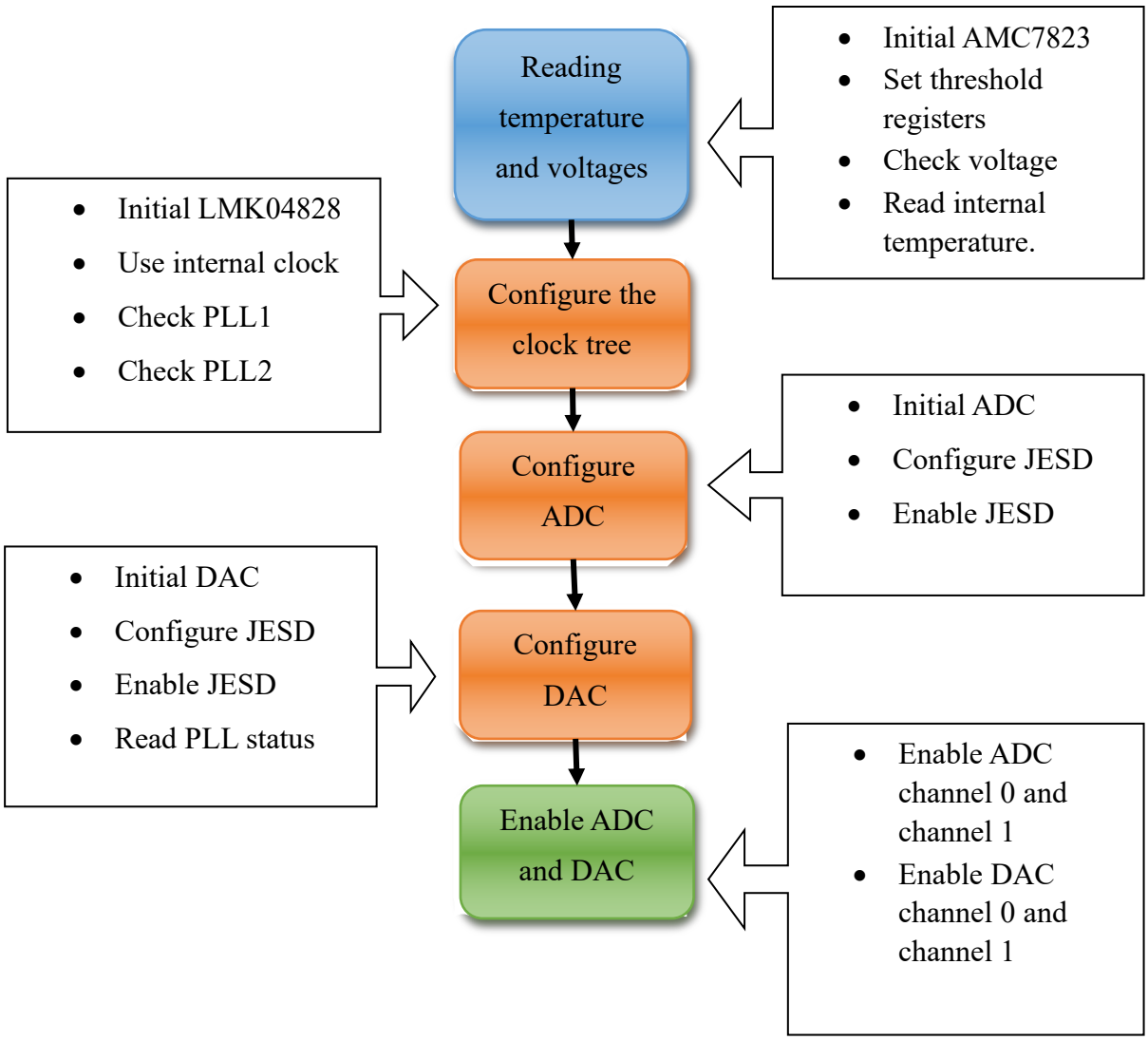


Figure 5.14: Software design flow

5.2.3 Experimental Setup

In order to test whether the FMC142_Connector interface can work properly, a data loopback experiment is set up, as shown in the Figure 5.15.

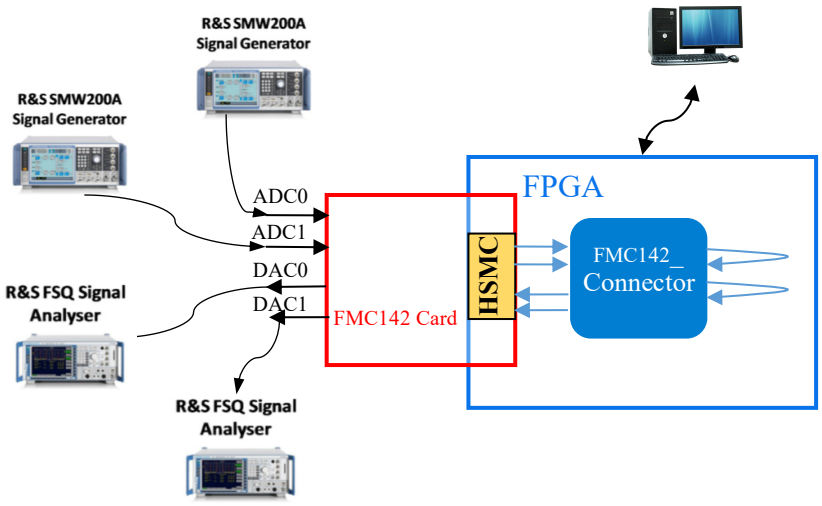


Figure 5.15: FMC142_Connector Interface Experimental Setup

As shown in Figure 5.15, an LTE signal and a WCDMA signal are generated by R&S SMW200A VSAs. The FMC142 card with 16-bit ADC channels and two 16-bit DAC channels at a sampling rate of 150 MHz are connected with FPGA through a HSMC connector. ADC channel 0 is connected to DAC channel 0 and ADC channel 1 is connected to DAC channel 1. Two R&S FSQ signal analysers are used to display and analyse the received analogue signals. In this experiment setup, the LTE signal is transmitted through ADC channel 0 and the WCDMA signal is transmitted through ADC channel 1.

5.2.4 Experiment Results

To assess the performance of the project FMC142_Connector Interface, the system dynamic range and the transmission signal quality are tested. For ADC channel 0, LTE signals with three different channel bandwidths (10 MHz, 15 MHz, and 20 MHz) are generated by the signal generator and fed into the system. The EVM results with modulation formats of 64QAM, 16QAM, and QPSK are tested. For ADC channel 1, the WCDMA signal is fed into the system. The EVM with 16QAM modulation format is tested.

- Test Results of ADC Channel 0

a) EVM performance with a modulation format of 64QAM for ADC Channel 0

Figure 5.16 indicates the EVM performance of channel 0 when the LTE signal is modulated with 64QAM. The signal input power is varied from -50 dBm to 0 dBm. The EVM requirement of 64QAM is 8%.

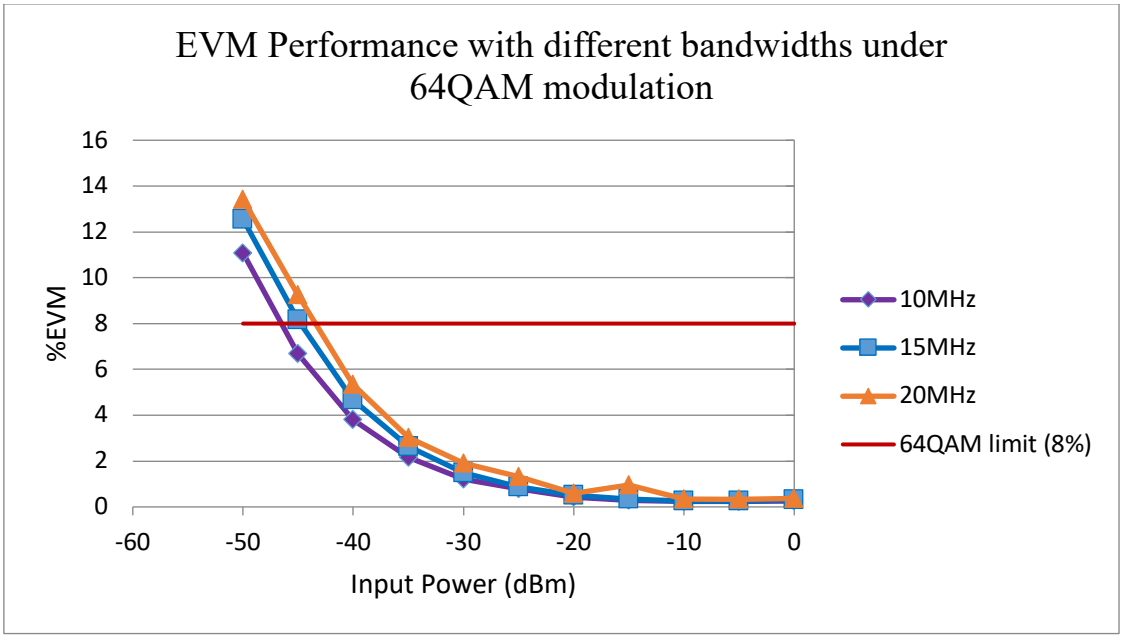


Figure 5.16: EVM performance of LTE signals under 64QAM

From the test results, it can be found the dynamic range of the system is power limited. The dynamic range calculation introduced in section 2.3.3 is for ideal system. In practice, the ADC dynamic range is smaller than the ideal value in order to ensure no damage to the equipment or clipping. When this system was tested, the maximum power was limited to 0 dBm and EVM could not be tested when the input power was larger than 0 dBm.

The EVM performance of a 20 MHz bandwidth LTE signal is illustrated by the orange curve in Figure 5.16. As the EVM requirement for 64QAM is limited at 8%, the dynamic range of channel 0 for a 20 MHz bandwidth LTE signal is approximately 43 dB. The dynamic range for a 15 MHz bandwidth LTE is wider than that of a 20 MHz bandwidth LTE, the value is 45 dB. The 10 MHz bandwidth LTE signal has the best performance of the dynamic range, which is around 47 dB.

Figure 5.17 shows the 64QAM constellation diagrams of the 10 MHz bandwidth LTE signal and 20 MHz bandwidth LTE signal at three different input powers (-10 dBm, -40 dBm, and -50 dBm).

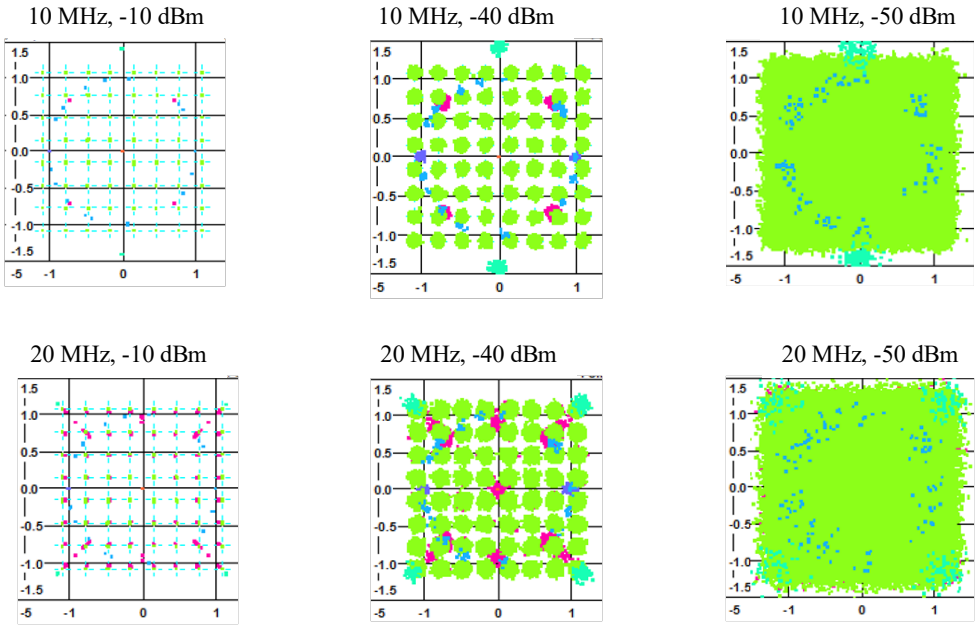


Figure 5.17: Constellation diagrams of LTE signals under 64QAM modulation

As shown in Figure 5.17, for both the 10 MHz bandwidth LTE signal and 20 MHz bandwidth LTE signal, the signal quality decreases as the input power decreases. Comparing the signal transmission quality with different bandwidths, but with the same input power, the 10 MHz bandwidth LTE signal shows better performance.

b) EVM performance with a modulation format of 16QAM for ADC channel 0

The EVM performance for channel 0 with a modulation format of 16QAM is tested with input power is varied from -50 dBm to 0 dBm. LTE signals with different channel bandwidths (10 MHz, 15 MHz, and 20 MHz) are fed into the system. The EVM performance requirement for 16QAM modulation format is 12.5%, as the red line shows in Figure 5.18.

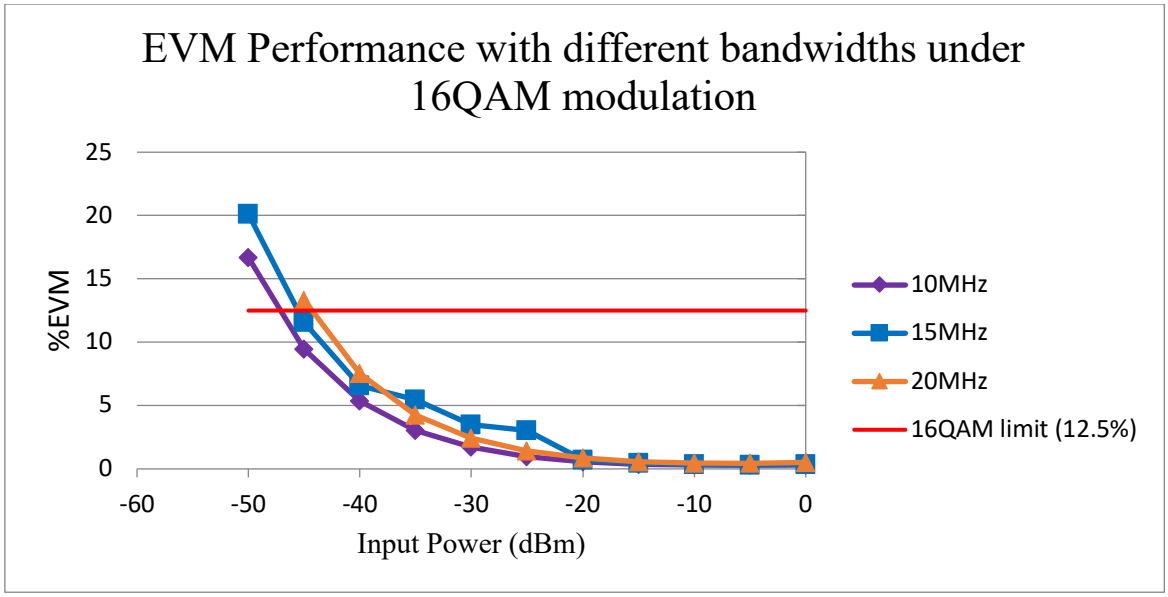


Figure 5.18: EVM Performance of LTE signals under 16QAM

As shown in Figure 5.18, the dynamic range of the 10 MHz bandwidth LTE signal is around 47 dB. The dynamic range of a 15 MHz bandwidth LTE signal is 45 dB, and the dynamic range of a 20 MHz bandwidth LTE signal is approximately 43 dB. From this figure, it can be found that the dynamic range of the system increases as the signal bandwidth decreases.

The following figures are the 16QAM constellation diagrams of the 10 MHz bandwidth LTE signals and 20 MHz bandwidth LTE signals with input powers of -10 dBm, -40 dBm, and -50 dBm.

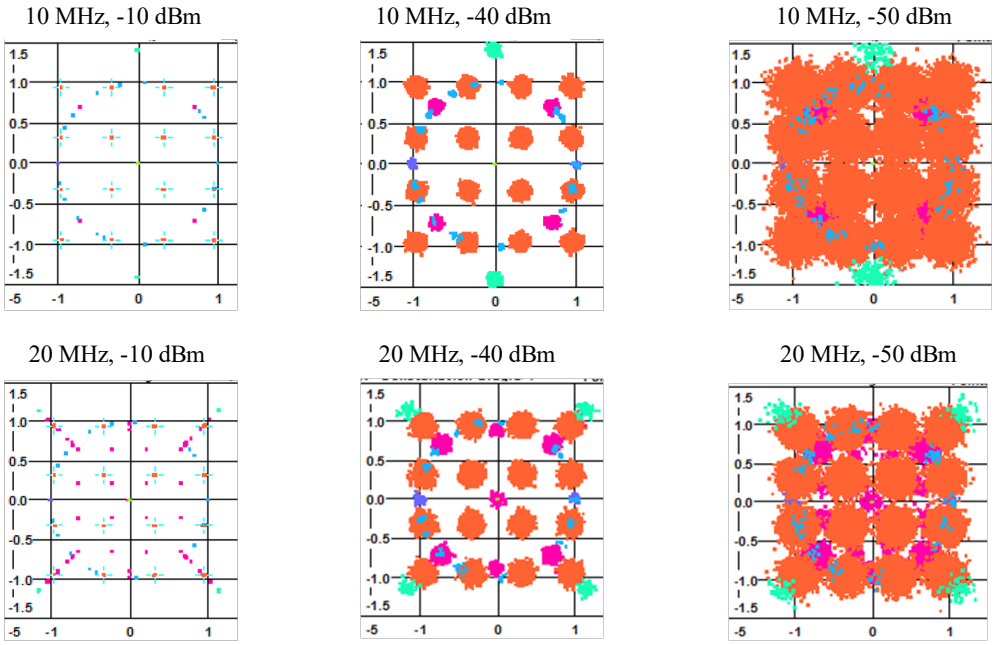


Figure 5.19: Constellation diagrams of LTE signals under 16QAM

bandwidth LTE signal has a better signal quality than that of the 20 MHz bandwidth LTE signal when the input power is the same. The signal quality is very poor when the input power is -50 dBm as the value of the EVM has already exceeded the 16QAM requirement.

c) EVM performance with a modulation format of QPSK for ADC channel 0

The EVM performance of channel 0 with modulation format of QPSK is tested. LTE signals with bandwidths of 10 MHz, 15 MHz, and 20 MHz are fed into the channel and the input power is varied from -50 dBm to 0 dBm. As the EVM request of QPSK is 17.5%, the dynamic range of the 20 MHz bandwidth LTE signal is around 43 dB. The 15 MHz bandwidth LTE signal has a better dynamic range with a value of 45 dB. The dynamic range of the 10 MHz bandwidth LTE signal is approximately 47 dB.

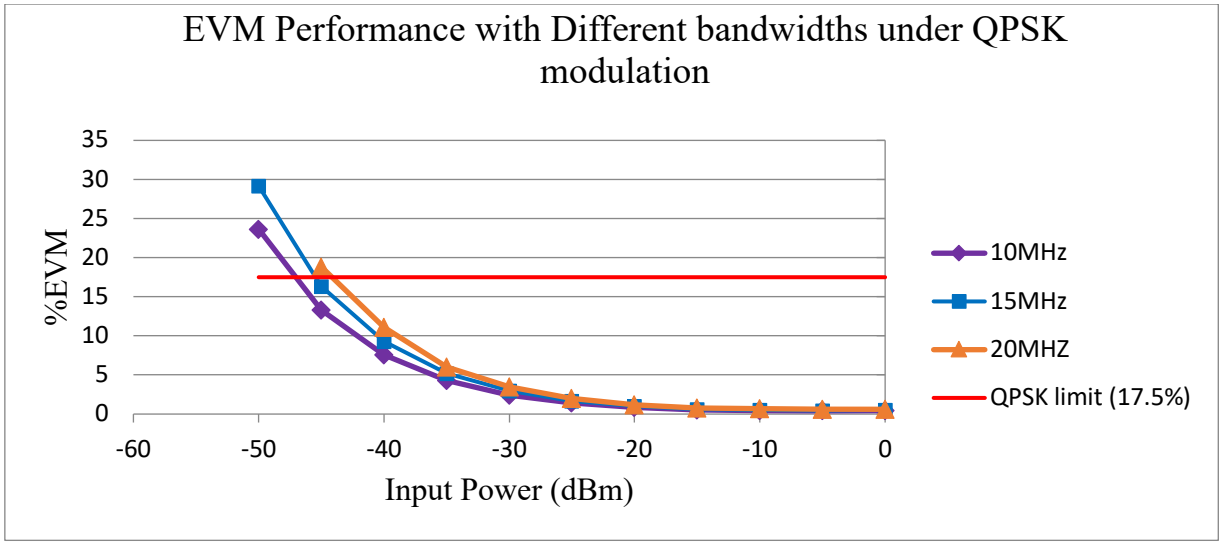


Figure 5.20: EVM performance of LTE signals under QPSK

The QPSK constellation diagrams shown in Figure 5.21 illustrates the signal transmission quality of the 10 MHz bandwidth and 20 MHz bandwidth LTE signals with input powers of -10 dBm, -40 dBm, and -50 dBm.

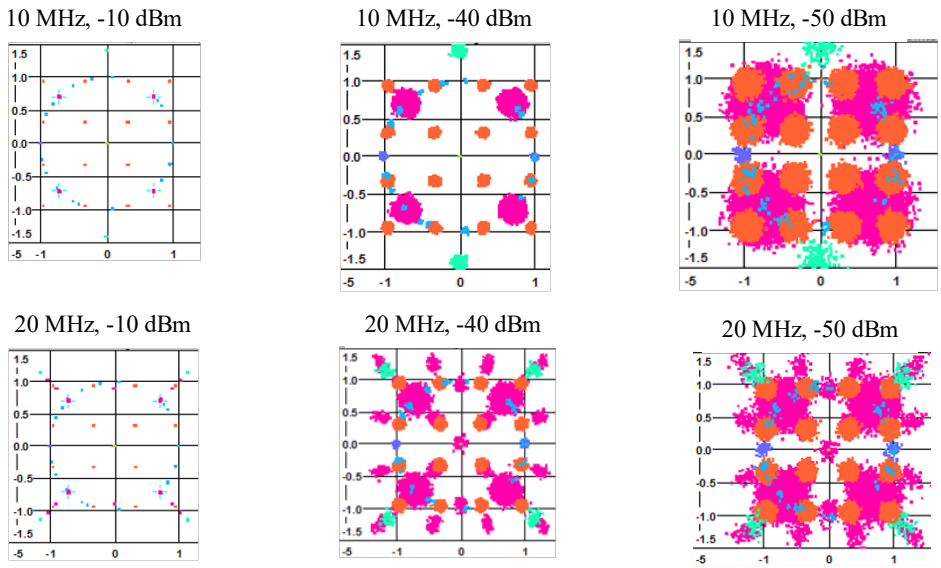


Figure 5.21: Constellation diagrams of LTE signals under QPSK

Figure 5.21 indicates that a signal with a narrow channel bandwidth has a better transmission quality than that of a signal with a wider bandwidth when the input power is the same. The

signal quality is very high when the input power is -10 dBm, but it reduces as the input power decreases.

- Test Results Channel 1

To test the performance of channel 1, a WCDMA signal is used as the input source. Figure 5.22 indicates the EVM test results.

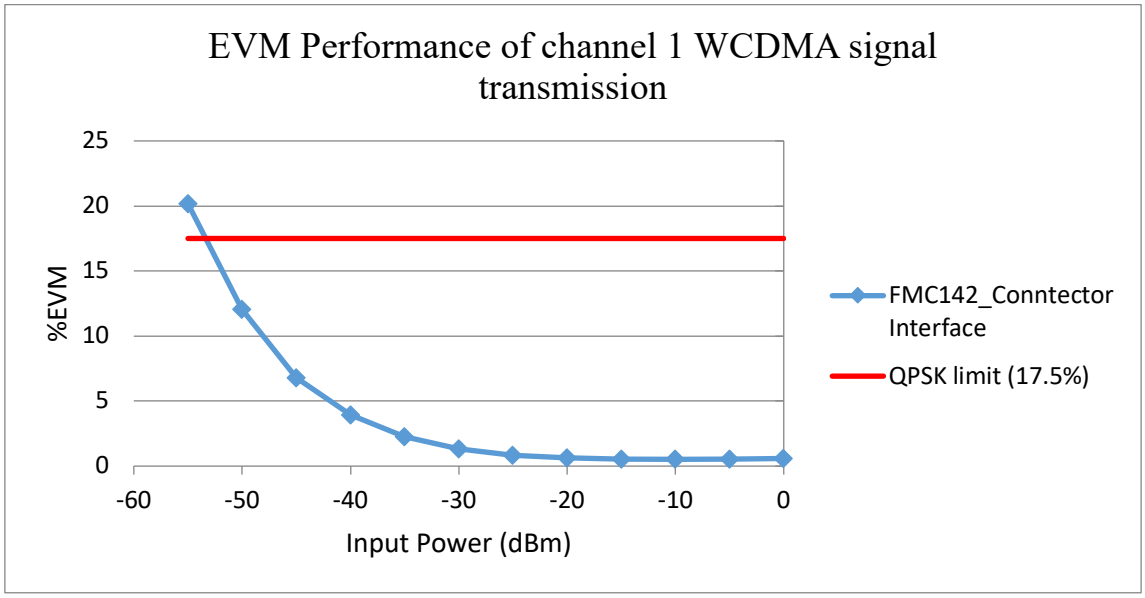


Figure 5.22: EVM performance of WCDMA signal

As shown in Figure 5.22, the WCDMA is modulated by QPSK and the EVM requirement is 17.5%. The dynamic range is approximately 53 dB.

5.2.5 Summary of FMC142 Performance

The project FMC142_Connector Interface is successfully implemented. All the components on the FMC142 card are configured and work as expected. The sampling rate of ADCs and DACs are configured to 150MHz and the transceivers on the FPGA work at a clock of 37.5MHz. All the parameters can be easily changed though the software design. The performance of channel 0 and channel 1 are tested by feeding an LTE signal and a WCDMA signal. The dynamic range and the signal transmission quality are measured and analysed.

5.3 RF Performance of Eth-DDAS

5.3.1 Experiment Setup

The last step to test the RF performance of the Eth-DDAS system is to combine the FMC142 interface module, introduced in Section 5.2, and the Eth-DDAS modules implemented on the FPGA, introduced in Chapter 4, together. The architecture of the real-time Eth-DDAS system has already been illustrated in Figure 5.1. The experiment setup is shown in Figure 5.23 below.

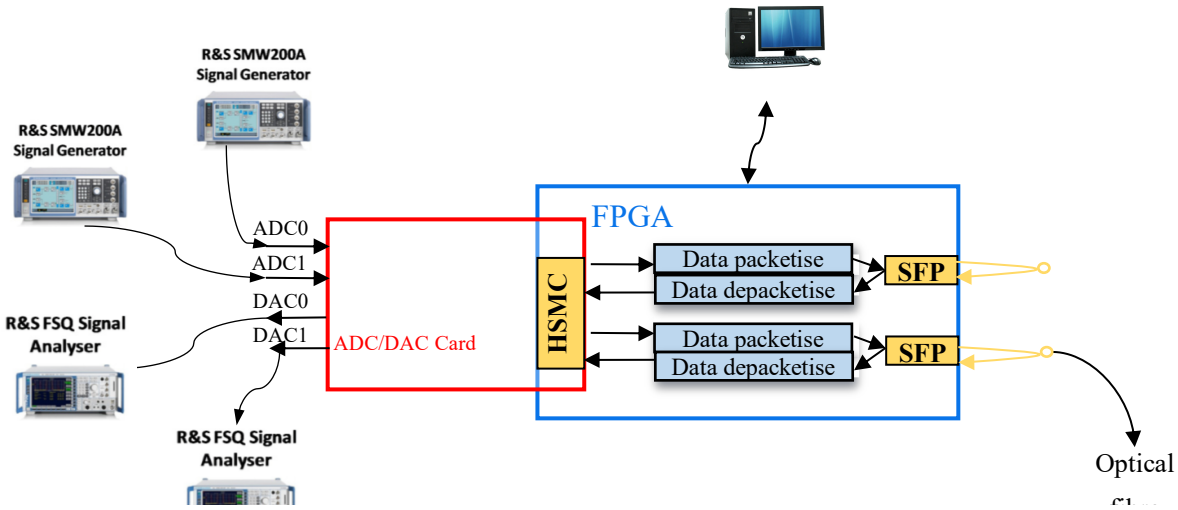


Figure 5.23: Real-time Eth-DDAS experiment setup with optical loopback

As shown in Figure 5.23, the performance of the system with two channels are tested and analysed. LTE signals with different bandwidths (10 MHz, 15 MHz, and 20 MHz) are fed into channel 0 and a WCDMA signal is fed into channel 1. Two onboard SFP^{+} connectors are used to transmit and receive signals and two 5m fibres are used to transmit signals.

5.3.2 Test Results

In order to compare the system performance between the real-time Eth-DDAS and the system FMC142_Connector interface, the same test methods are used in this section. Channel 0 is fed with LTE signals under 64QAM, 16QAM and QPSK modulation formats. Channel 1 is fed with a WCDMA under 16QAM modulation format. The dynamic range and the EVM performance of two channels are tested. The signal transmission quality is also analysed.

- Test Results of Channel 0

a) EVM performance with a modulation format of 64QAM for Channel 0

Figure 5.24 indicates the EVM performance of 10 MHz, 15 MHz and 20 MHz bandwidths LTE signals under a 64QAM modulation format. The input power varied from -50 dBm to 0 dBm.

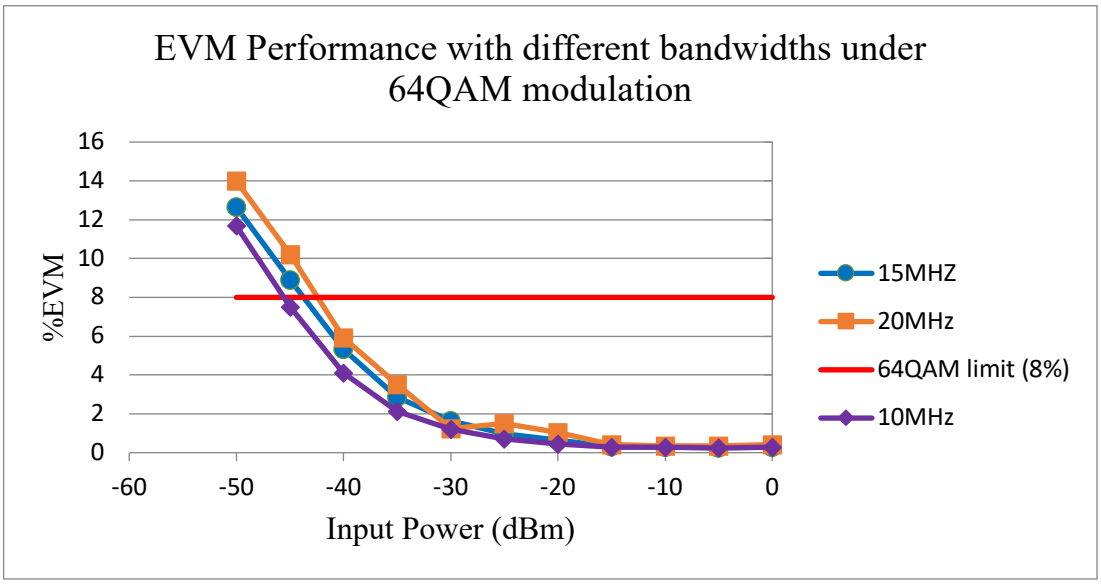


Figure 5.24: EVM performance of LTE signals under 64QAM

As shown in Figure 5.24, the dynamic range of a 20 MHz bandwidth LTE signal is approximately 42 dB. The dynamic range of 15 MHz and 10 MHz bandwidth LTE signals are around 43 dB and 46 dB.

b) EVM performance with a modulation format of 16QAM for Channel 0

The EVM performance of LTE signals under the 16QAM modulation format is also tested. The test results are illustrated in Figure 5.25.

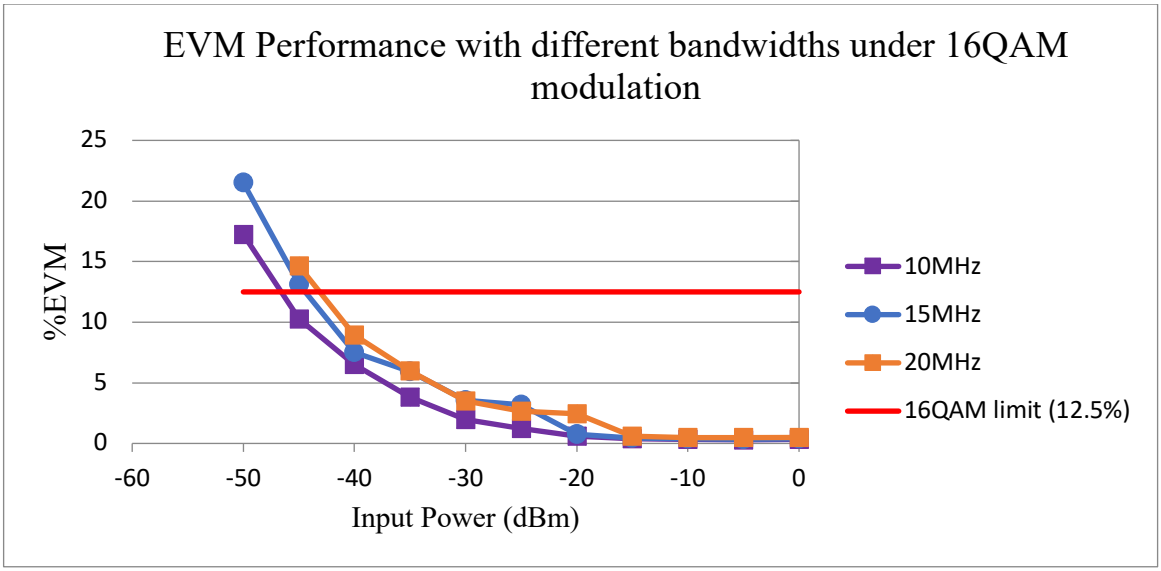


Figure 5.25: EVM performance of LTE signals under 16QAM

From Figure 5.25, the dynamic range of the 10 MHz bandwidth LTE signal is 46 dB. The dynamic range of the 15 MHz bandwidth LTE signal and 20 MHz bandwidth LTE signal are 44 dB and 42 dB.

c) EVM performance with a modulation format of QPSK for Channel 0

The following figure indicates the EVM performance of channel 0 when LTE signals are modulated with QPSK.

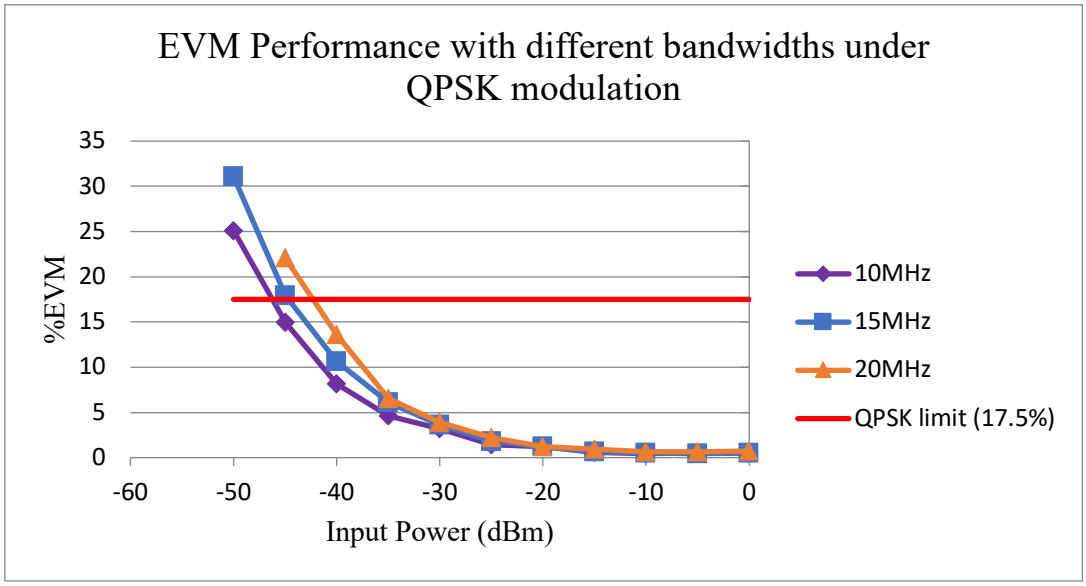
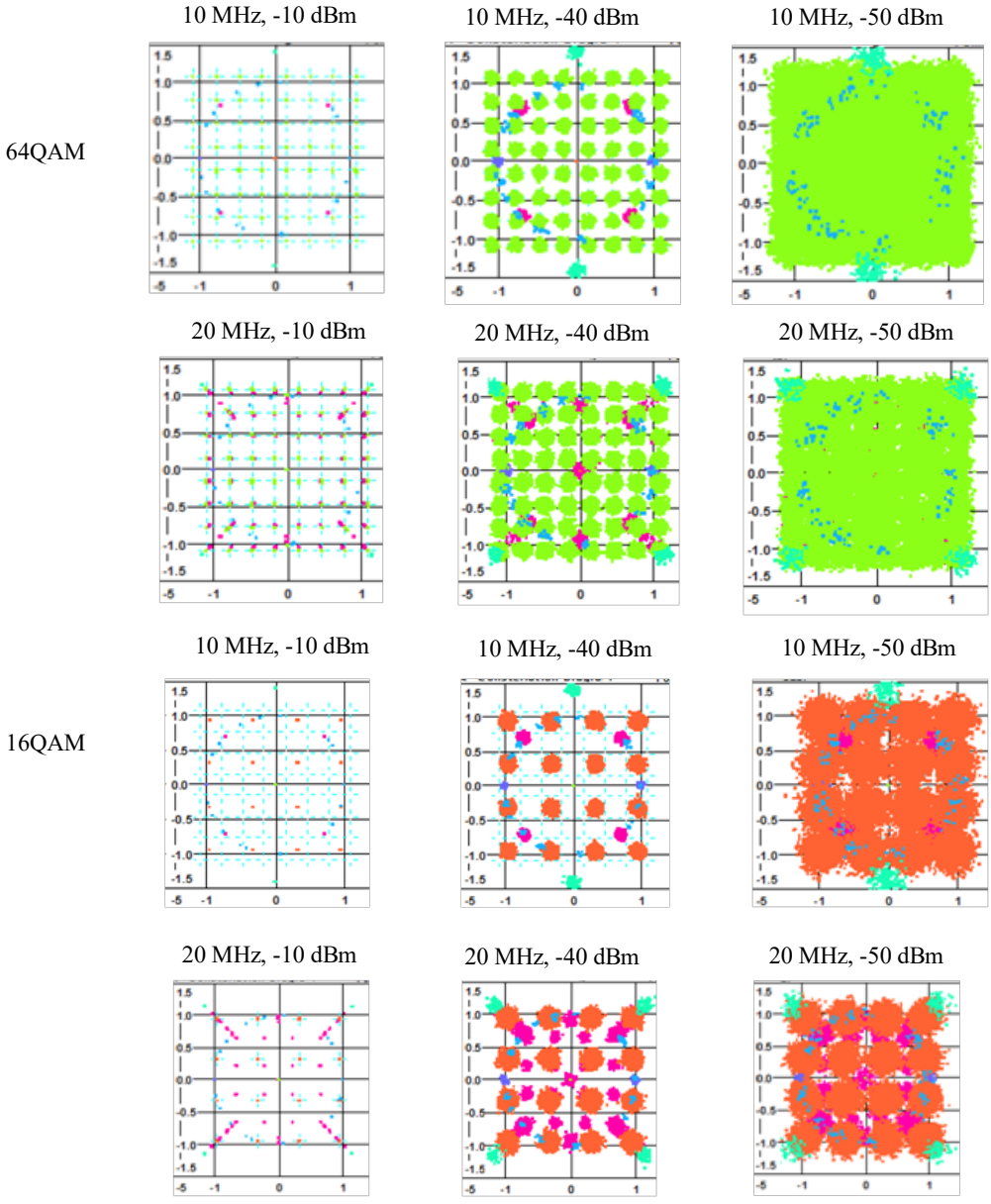


Figure 5.26: EVM performance of LTE signals under QPSK

Figure 5.26 shows that the dynamic range of the 20 MHz bandwidth LTE signal is 42 dB and the dynamic range of the 15 MHz and 10 MHz bandwidth LTE signals are 44 dB and 46 dB.

The constellation diagrams of 10 MHz and 20 MHz bandwidth LTE signals at input powers of -10 dBm, -40 dBm, and -50 dBm under 64QAM, 16QAM, and QPSK modulation formats are illustrated in Figure 5.27.



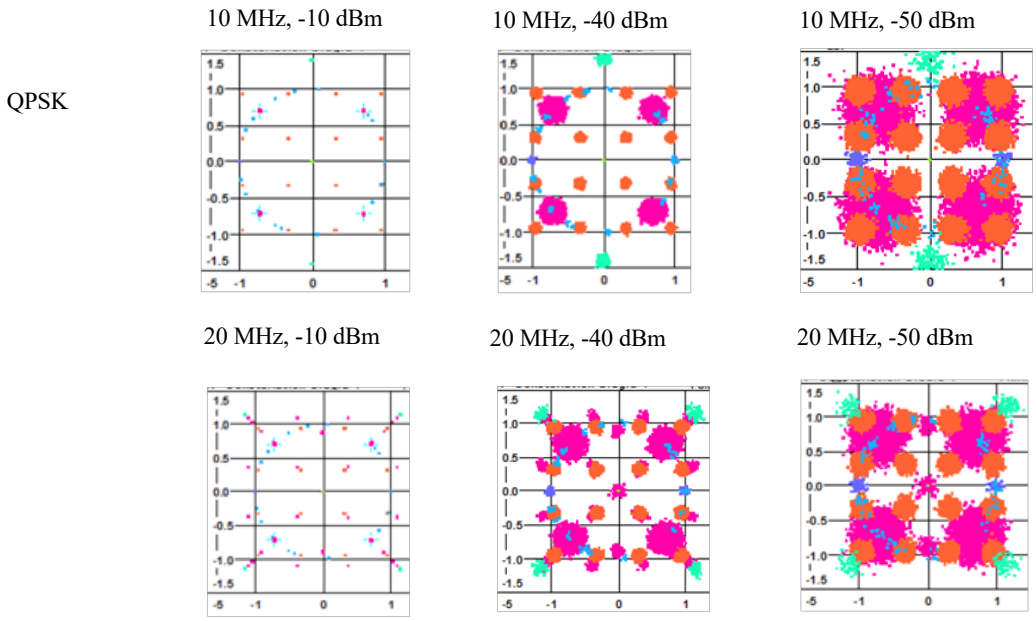


Figure 5.27: Constellation diagrams of LTE signals

The constellation diagrams show how the signal transmission quality becomes poor as the input power decreases and the 10 MHz bandwidth LTE signals have a better transmission quality than that of the 20 MHz bandwidth LTE signals.

- Test Results of Channel 1

A WCDMA signal is fed into channel 1 and the EVM performance is tested. Figure 5.28 shows the test results.

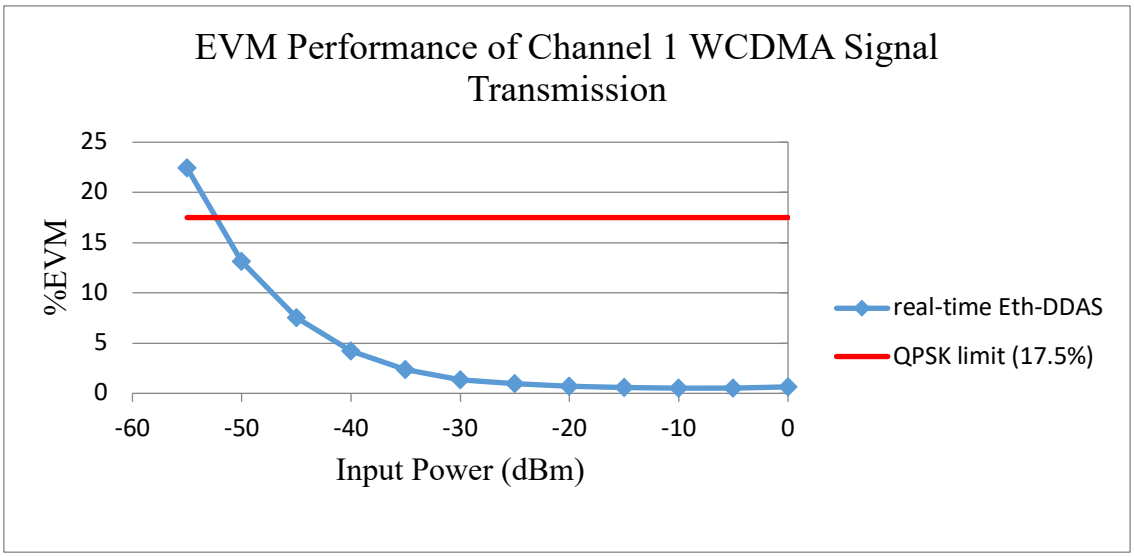


Figure 5.28: EVM performance of WCDMA Signal

The test results shown in Figure 5.28 indicate that the dynamic range of channel 1 is approximately 52 dB.

5.4 Comparison and Analysis

In Chapter 4, the signal source of the Eth-DDAS system is an LTE digital signal stored in a BRAM with 20 MHz bandwidth and a centre frequency of 30 MHz. By repeatedly feeding this LTE signal into the system over 12 hours, a total number of 76,578,301 packets are transmitted with 0 error frame received. For the real-time Eth-DDAS system, the test results show that the system EVM increases as the input power decreases. The dynamic range of a 20 MHz bandwidth LTE signal under 64QAM modulation format is 42 dB, the EVM exceeds the 64QAM requirement (8%) when the input power is less than 42 dBm.

The EVM performance of a real-time Eth-DDAS system and FMC142_Connector interface system are also compared. Figure 5.29 illustrates the difference when a 20 MHz bandwidth LTE signal under a 64QAM modulation format is used as the signal source for channel 0.

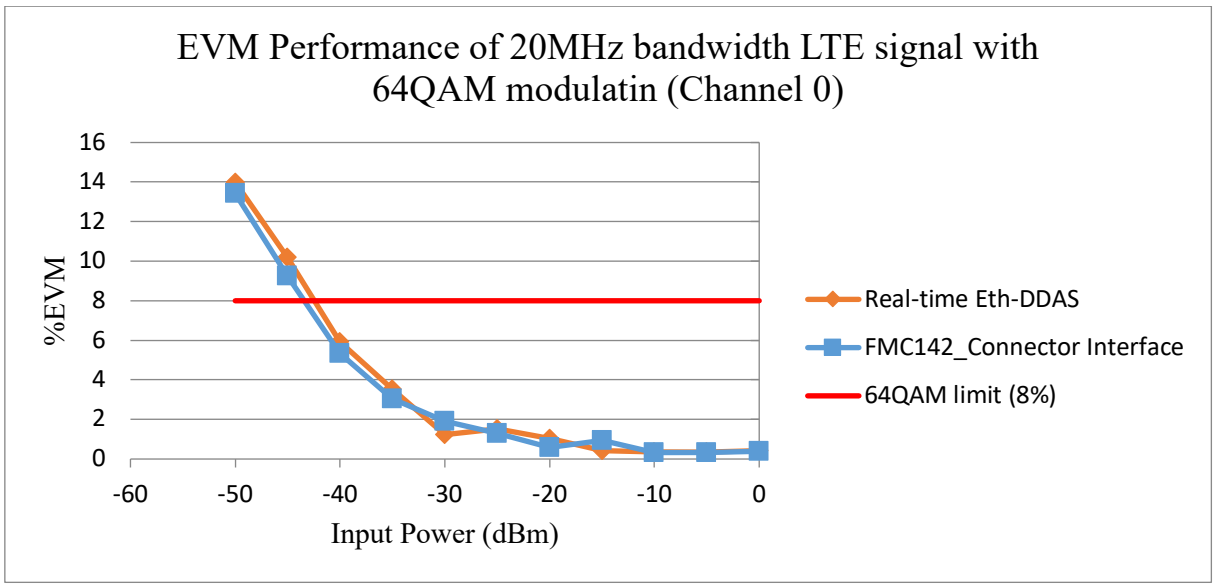


Figure 5.29: EVM performance of 20MHz LTE signal under 64QAM

As shown in Figure 5.29, the dynamic range of the real-time Eth-DDAS system is 42 dB and 43 dB for the FMC142_Connector interface system. There is a 1dB difference between the two systems.

The EVM performance of two systems is also compared when a 15 MHz bandwidth LTE signal under 16QAM modulation format is fed into channel 0. The results are shown in Figure 5.30.

The dynamic range of the real-time Eth-DDAS system is 45 dB and 46 dB for the FMC142_Connector interface system.

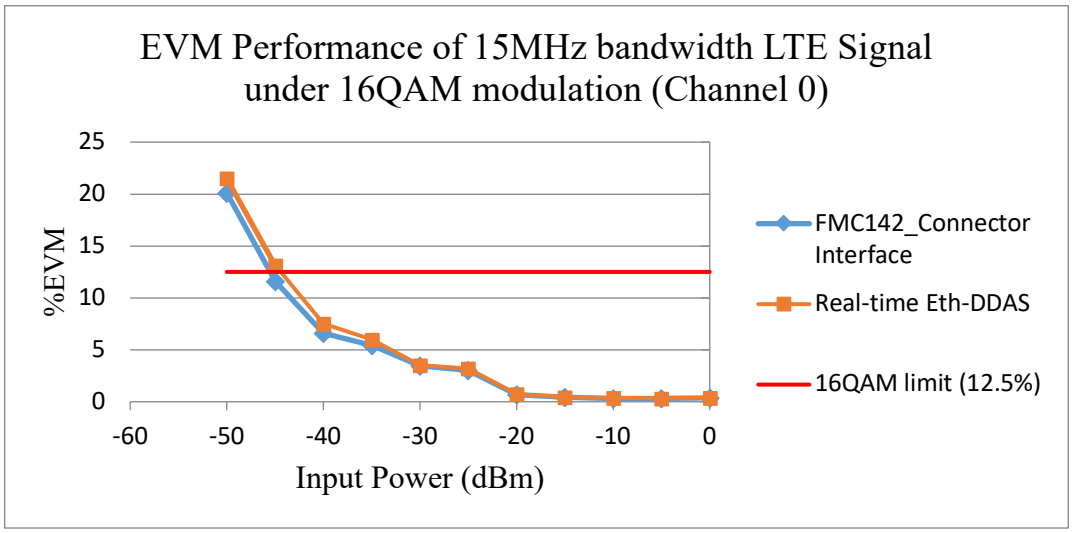


Figure 5.30: EVM performance of 15MHz LTE signal under 16QAM

The EVM performance of two systems is compared when a 10 MHz bandwidth LTE signal under QPSK modulation format is used as the input source of channel 0. As shown in Figure 5.31, the dynamic range of the FMC142_Connector interface system is 47 dB and 46 dB for the real-time Eth-DDAS system.

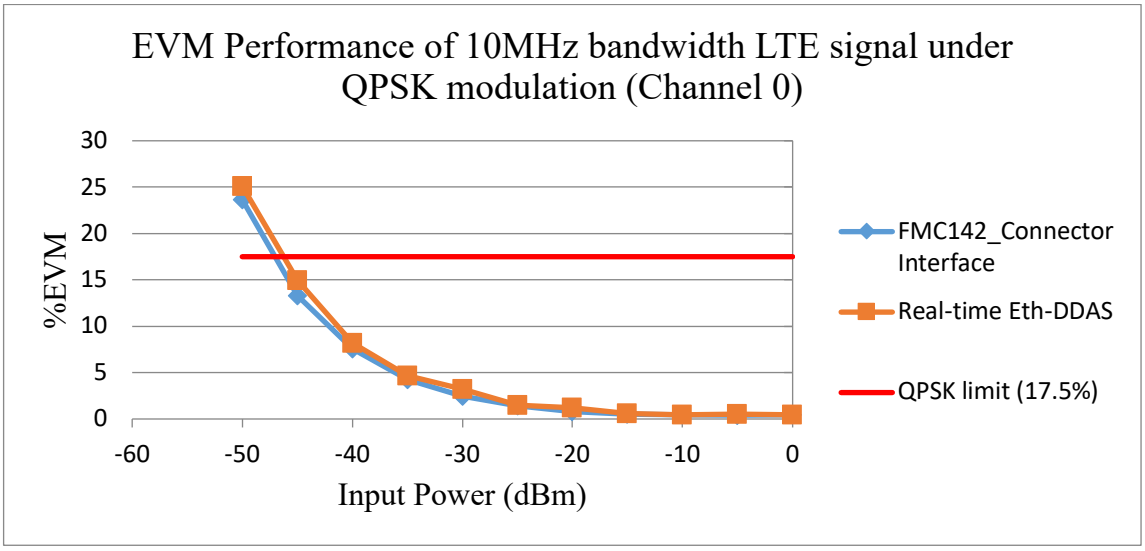


Figure 5.31: EVM performance of 10MHz LTE signal under QPSK

The EVM performance of channel 1 of two systems is compared and the results are shown in Figure 5.32. The dynamic range of the real-time Eth-DDAS system is 42 dB and the dynamic range of the FMC142_Connector interface system is 43 dB.

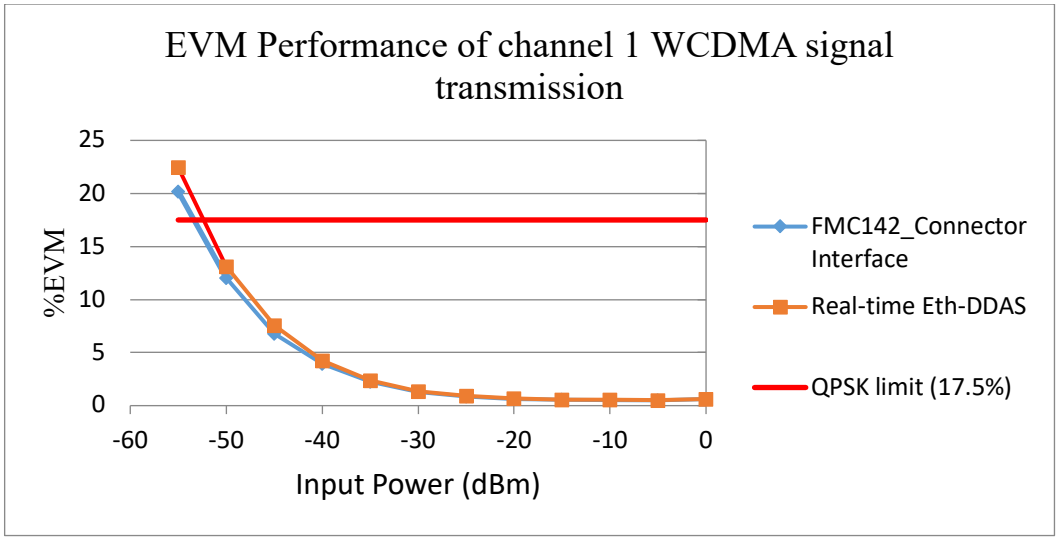


Figure 5.32: EVM performance of channel 1

By comparing the dynamic range of the real-time Eth-DDAS system with the FMC142_Connector interface system, it can be found that the dynamic range of two systems has a one dB difference. As the system becomes more complex, the components, such as SFP^{+} connectors and fibres, may introduce some errors, but the performance of the real-time Eth-DDAS system is mainly determined by the ADC/DAC card.

5.5 Conclusions

In this chapter, the real-time Eth-DDAS system is implemented and tested. Before building the full system, project FMC142_Connector interface is first implemented to make sure the FMC142 card is configured properly and the interface module between the FMC142 card the FPGA is implemented successfully. The performance of the real-time Eth-DDAS is tested. LTE signals with bandwidths of 10 MHz, 15 MHz, and 20 MHz under different modulation formats (64QAM, 16QAM, and QPSK) are fed into channel 0 and a WCDMA signal is used as the input source of channel 1. The dynamic range and the signal transmission quality is measured and analysed. For channel 0, the dynamic range of a 20 MHz bandwidth under a 64QAM modulation format is 42 dB. The signal transmission quality increases if a signal with a narrow bandwidth is transmitted. For channel 1, the dynamic range is around 52 dB due to the bandwidth of WCDMA, which is only 5 MHz.

5.5 Conclusions

Comparing the system performance of the real-time Eth-DDAS system with the system with a digital input source (introduced in Chapter 4), the dynamic range of the system is mainly determined by ADC/DAC card.

Chapter 6 Conclusions and Future Work

6.1 Overall Conclusions

6.1.1 Motivation

Mobile data is predicted to grow dramatically in the forthcoming years. Cisco forecasts that the quantity of monthly mobile data will reach 49 exabytes by 2021, which is seven times greater than that of 2016. However, more than 80% of data traffic is generated from buildings. In addition, there are normally between three and four major mobile network operators in a region, all of which provide multiple mobile services. In order to satisfy the Quality of Experience (QoE) and the Quality of Service (QoS) requirements, an in-building multi-service wireless mobile network with enough bandwidth and coverage is needed. Digital distributed antenna systems (DDAS) have become a key technolog when tackling this problem, especially for large buildings. As the optical fibre provides low-loss cabling, the fibre-based DDAS are able to obtain many benefits from it, especially when the DDAS are implemented within large buildings and over long distances. However, the current transport links for DDAS cannot provide enough bandwidth for the next generation of in-building wireless networks. Due to the fact that Ethernet is now widely used and has been developed over many years, use Ethernet infrastructure as the transport link for digital DAS is considered to be a reliable and cost-effective solution. To transport the required radio frequency (RF) signal over the Ethernet, the stringent latency requirement of the RF signal has become a bottleneck for the Eth-DDAS system.

To overcome these problems, a digital DAS over Ethernet (Eth-DDAS) system has been suggested in this thesis. The theory is that the system packetises the RF signal onto an Ethernet frame structure and provides a mechanism to help maintain the frame order. As a result, the system latency then meets the requirements provided by the Common Public Radio Interface (CPRI). Moreover, a multi-service DDAS system that uses a data compression algorithm and a 14-channel multi-service DDAS system have been demonstrated in this thesis to further explain the technology present in multi-service in-building DDAS.

6.1.1 Multi-service DDAS with a data compression algorithm

A multi-service digital DAS with a data compression algorithm has been demonstrated experimentally for the first time in this thesis. With the help of the data compression algorithm, the spectral efficiency has been shown to be improved by up to three times more than CPRI

when a single 20MHz bandwidth LTE signal is used as the input source. To test the EVM dynamic range of the system, LTE signals with different bandwidths are fed into channel 0 and a WCDMA signal is used as the input source of channel 1. The EVM dynamic range of channel 0 is 42dB when a 20MHz bandwidth LTE signal is fed into the system. Channel 1 offers an EVM dynamic range of 62dB.

In addition, a 14-channel multi-service system has also been introduced in this thesis. The system is designed in collaboration with the Beijing Institute of Aerospace Control Devices (BIACD) for China Tower Ltd. By demonstrating this multi-service system, it should hopefully become more straightforward to understand how to design a system that meets industrial requirements.

6.1.2 Multi-service Ethernet Digital DASs

The Eth-DDAS system is designed as an embedded system. The Net-FPGA SUME is used to implement the system hardware with the help of Xilinx Vivado. The system software is designed using the Xilinx Software Development Kit (Xlinx SDK). The FMC142 card is selected as the ADC/DAC convertor. It provides two channels of ADC/DAC with a 16-resolution bit, a 370MSPS sampling rate of ADC, and a 2500MSPS sampling rate of DAC.

Three functional blocks are implemented for the system hardware design: 1) a FMC142 interface; 2) data packetised and depacketised based on the Ethernet frame structure; 3) a SFP^+ module to transmit and receive signals.

The RF signal is digitised first, then the digital data is packetised as an Ethernet frame with a timestamp header, a sequence number header, and an IP header; source and destination MAC address headers are then added. The Ethernet frames are then sent through the SFP^+ connector over fibres. After the Ethernet frames are received, they are depacketised and recovered to form an analogue signal. The software is designed to control the Ethernet frame size and to configure parameters for each hardware module. In addition, the software is also used to control the FMC142 card.

In order to test the system performance, different RF signals are fed into Eth-DDAS. Channel 0 is tested with LTE signals with differing bandwidths. A 20 MHz bandwidth LTE signal under 64QAM modulation format is shown to offer an EVM dynamic range of 42dB. A 10MHz bandwidth LTE under 64QAM modulation format increases the EVM dynamic range to 46dB. Channel 1 is fed with a WCDMA signal; the EVM dynamic range is 52dB because the

bandwidth of WCDMA is 5MHz. The system latency is measured using three scenarios. A 1026 ns latency is contributed to the system with a loop test when the Ethernet payload size is 64 Bytes. An 820 ns latency is contributed by an Ethernet switch.

6.2 Future Work

While this thesis has contributed significant developments to the concept of multi-service Ethernet DDAS, more research is required into this area to achieve the ultimate deployment of the future Eth-DDAS. The future work includes the following elements.

6.2.1 Implementing the data compression algorithm onto Eth-DDAS

The data compression algorithm introduced in Chapter 3 has been shown to contribute a spectral efficiency that is three times greater than that of CPRI. If the data compression algorithm is to be integrated with the current Eth-DDAS, the upgraded Eth-DDAS would handle more signals over the same transport link. Due to the fact that the data compression algorithm's functional blocks are implemented on the Altera Quartus platform and the Eth-DDAS is implemented using a Xilinx Vivado platform, migrating the data compression algorithm blocks from Altera Quartus to Xilinx Vivado would be the first step for this work. The system architecture should be upgraded as shown in the figure below.

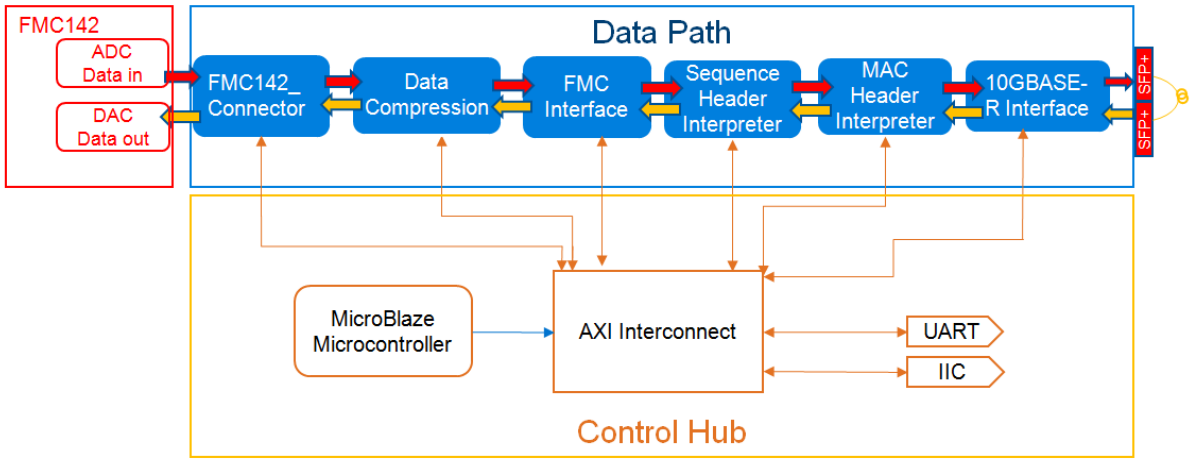


Figure 6.1: Eth-DDAS with data compression algorithm

6.2.2 DAS module and remote module separation

The current Eth-DDAS system is implemented on one FPGA. The transmitter and receiver of a channel are implemented with the same clock. In reality, the system's DAS module is normally

allocated in the base station, while the remote units are allocated at different places. The architecture is shown in the figure below:

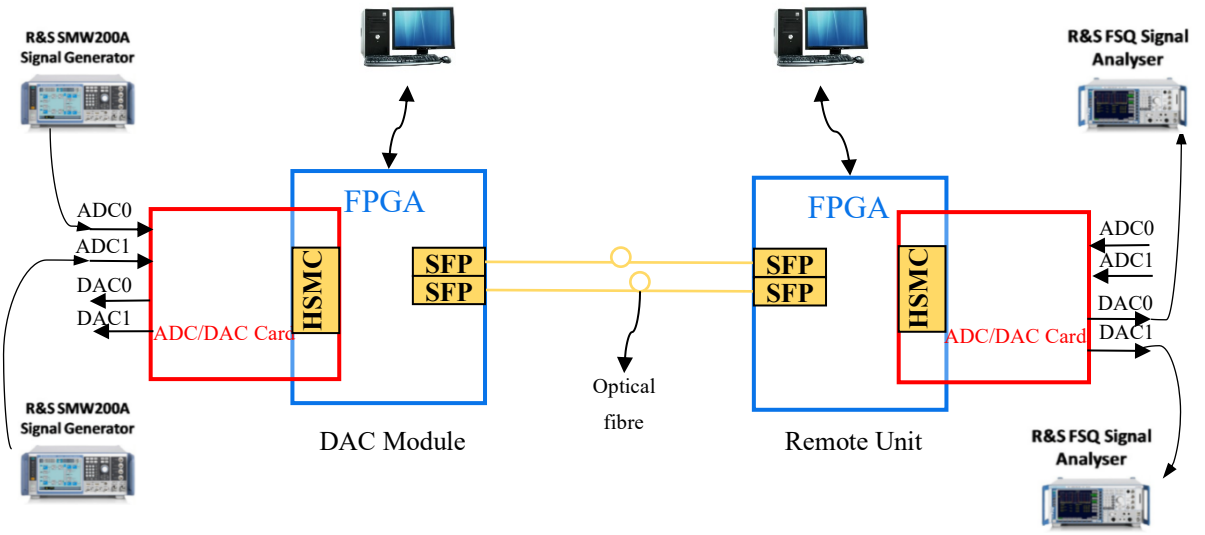


Figure 6.2: Experimental setup of the separated DAC Module and Remote Unit

on two FPGA boards. The challenge of this work is the synchronisation of the clocks on the two FPGA boards. A clock synchronisation mechanism should be designed to transport the time information.

6.2.3 Network congestion solution

The current Eth-DAS system does not have the network congestion problem as the bandwidth is wide enough. In the future, network congestion may occur as more data is transmitted into the system. A solution will be proposed to solve the network congestion problem. As the system is a real-time system, the packet latency requirement is strict. The packet must be dropped once the delay time beyond the latency limit and the dropped packet will be resend again.

6.2.4 Frame ordering with real Ethernet network

The real Ethernet network is complemented with many switches to transport frames. Currently the Eth-DDAS transports Ethernet frames with a 2m fibre; although an Ethernet switch has been implemented, as introduced in Chapter 4, it is only used to test the system latency. Figure 6.3 simply illustrates a network with four switches.

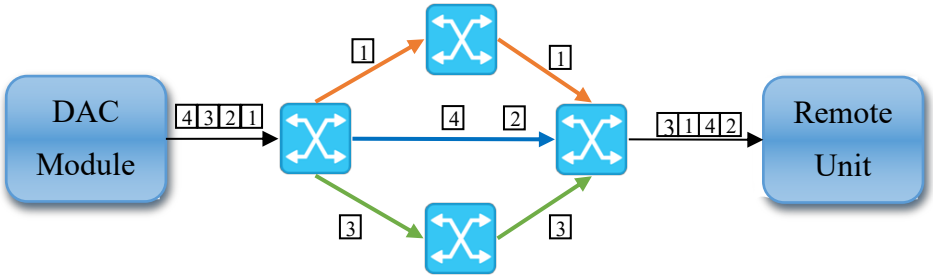


Figure 6.3: Network with multiple switches

As shown in Figure 6.3, the DAC Module sends four frames with ordering; however, due to the fact that frames are transported through different paths and that there are numerous switches in the paths, the Remote Unit received frames out of order. To overcome this problem, an ordering mechanism should be designed. The sequence number header has already been added to the current Eth-DDAS system; by reordering these sequence numbers, the Remote Unit receives the signal correctly.

6.2.4 Eth-DDAS System Integration with IP Network

In general, the technical aspect of the future work aims to develop a DDAS for the next generation of the in-building mobile network. To integrate the Eth-DDAS with the existing Ethernet infrastructure would make the new system economically feasible. Figure 6.4 illustrates an example of the next generation of in-building digital DAS mobile networks.

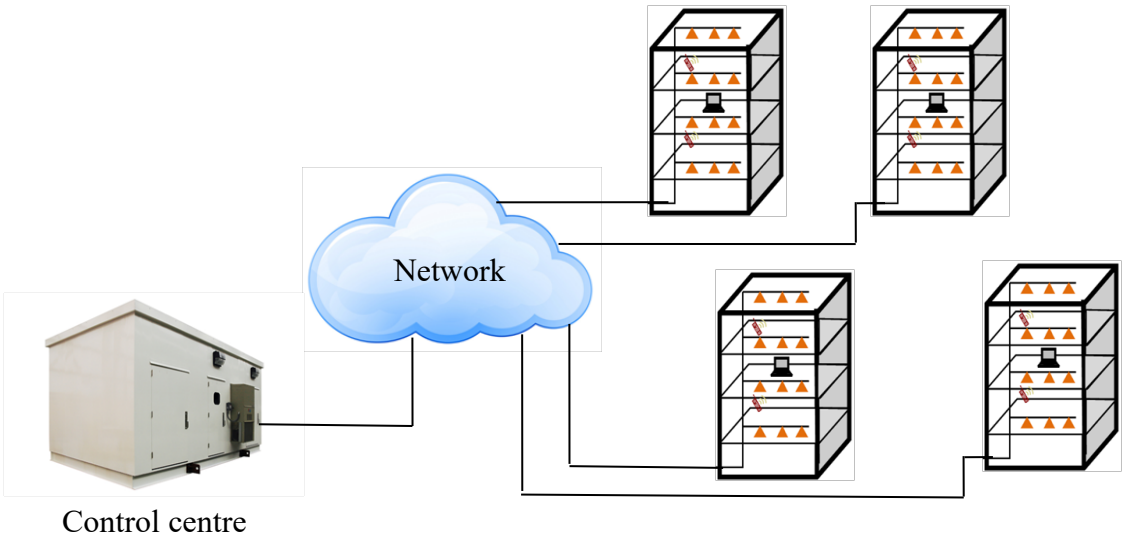


Figure 6.4: DDAS system integrated with IP network

6.2 Future Work

Similar to the CRAN architecture, the DAS Modules introduced in Chapter 3 will be centrally allocated in a control house. The RF signal is transported via the Ethernet network to the remote units allocated in buildings. By complying with the header information of each frame, all the frames should be transported to the correct addresses. By integrating DDAS with the existing network infrastructure, the cost of the system should be greatly reduced. The centralised control centre will also reduce energy consumption and lower the overall opex and capex.

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