Investigation of the Dual Implant Reverse-Conducting SuperJunction Insulated Gate Bipolar Transistor

E. M. Findlay, F. Udrea and M. Antoniou

***Abstract*—This letter presents the Dual Implant SuperJunction (SJ) trench Reverse-Conducting (RC) Insulated Gate Bipolar Transistor (IGBT) concept with two implanted SJ pillars in the drift region; one from the cathode side and another from the anode side. The proposed device is compatible with current manufacturing processes and enables a full SJ structure to be achieved in a 1.2kV device as alignment between the pillars is not required. Extensive Technology Computer Aided Design (TCAD) simulations have been performed and demonstrated that utilising this dual implantation technique can result in a 77% reduction in turn-off losses for a full SJ structure, compared to a conventional RC-IGBT. The results show that any snapback in the on-state waveform significantly increases the turn-off losses and only a deep SJ device (pillar gap < 10µm) warrants the additional processing expense.**

***Index Terms*— Insulated Gate Bipolar Transistor (IGBT), Reverse Conducting Insulated Gate Bipolar Transistor (RC-IGBT), SuperJunction (SJ), Body diode, Anti-parallel diode, Power devices, Power electronics**

I. Introduction

The RC-IGBT was first proposed in 1987 with a collector shorted, p-channel IGBT [1] building upon the concept in [2], where to integrate the diode structure within the IGBT n+ regions (anode shorts) are implanted into the p-collector region [3], [4]. It has several advantages: a reduction in the overall silicon area compared to a separate IGBT and diode solution; a reduction in module assembly, wafer processing and testing cost as well as improved reliability offered by a reduction in the number of bond wires; the RC-IGBT is more suitable for high junction temperature operation, and there is the possibility of optimising gate signals to allow better trade-off between the on-state voltage drop and the reverse recovery losses of the diode [5]. Yet despite these benefits, widespread use of the RC-IGBT within high voltage, hard switching applications are limited as the device suffers from an undesirable snapback in the current-voltage characteristics (MOSFET shorting effect) [5].

Several structures have been proposed to overcome this issue, with the majority focussing on the anode structure, but the Trench Field Stop SJ RC-IGBT (TFS-SJ-RC-IGBT) instead employs a SJ structure at the cathode and utilises traditional anode shorts to provide the reverse conduction path [6], [7]. For a TFS-SJ-RC-IGBT comparable with a CoolMOS structure, the switching losses of the proposed device are lower than a standard RC-IGBT but a snapback is present in the I-V characteristic [6], [7]. The diode reverse recovery characteristic was unaffected by the SJ structure [8]. It was demonstrated that extending the SJ pillars further into the drift region to approach a full SJ structure could completely remove the snapback, but this device is not currently manufacturable.

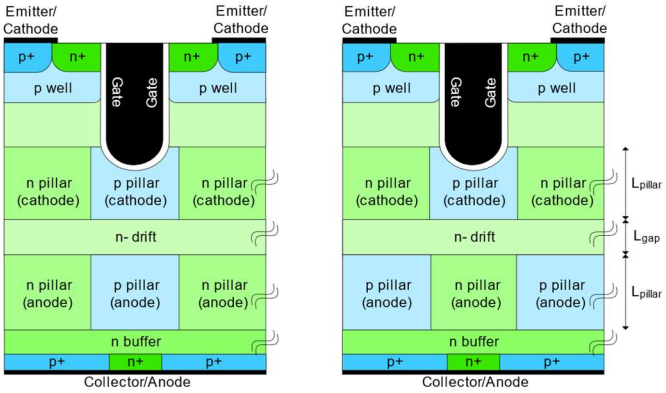

Fig. 1. Dual Implant SJ RC-IGBT structure (not to scale) (a) anode/cathode pillar with no offset, (b) anode/cathode pillar with full offset

More recent studies have focussed on the possibility of applying the SJ to the anode side [9], similar to the Alternating Buffer Reverse Conducting IGBT (AB RC-IGBT) concept [10]. In this alternative SJ device, it was shown that pillar location is independent of the features of the cathode, thus making processing simpler as there is no need for alignment [9]. It also decouples the anode design from the cathode enabling the designer to better control the saturation current and short circuit capability [9], and has the advantage over the AB RC-IGBT that the n/p pillars in the SJ device do not also need to be optimised for breakdown capability [5]. Similar improvements in snapback was reported for this anode SJ implantation, but, as for the cathode-side SJ device, to remove the snapback entirely the SJ implant had to extend through the entire drift region, which cannot be manufactured [9].

For the SJ devices, state of the art fabrication techniques

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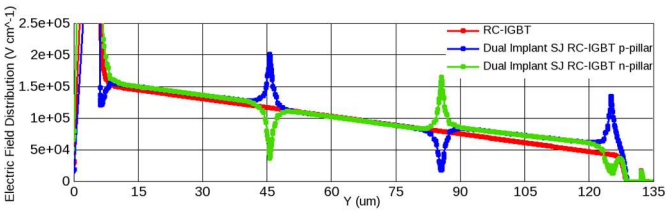

Fig. 2. Electric field distribution under blocking conditions (1.2kV) of the Trench RC-IGBT and Dual Implant Trench SJ RC-IGBT, thickness 135µm

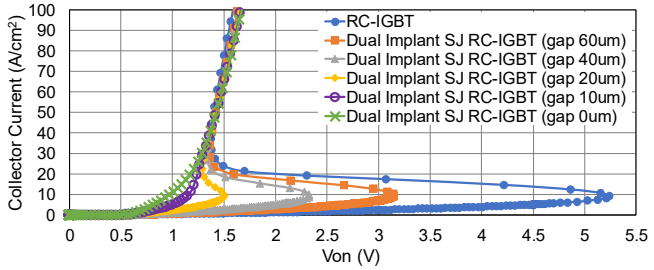

Fig. 3. On-state characteristics of Dual Implant SJ RC-IGBT, ambient temperature = 298K, SJ pillars have no offset between anode and cathode side

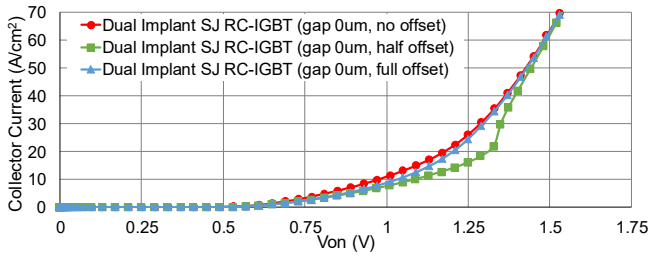

Fig. 4. On-state characteristics of Dual Implant Full SJ RC-IGBT with varying offset between anode and cathode SJ implants, ambient temperature = 298K

limits a pillar length to 65µm [11], so from a single deep SJ trench it is not possible to achieve a full SJ structure in the drift region of a 1.2kV IGBT. This study proposes applying two SJ implants, one from the cathode side and a second one from the anode side, and investigates the requirement for alignment of these pillars. This work builds upon the concepts and results as given in [7], [9], specifically for an RC-IGBT structure.

II. Device Structure and Fabrication Method

Fig. 1 is a schematic representation of the dual implant SJ RC-IGBT. It is based upon the standard RC-IGBT structure with anode shorts [5], but the drift region contains two regions of SJ pillars, one from the cathode side and a second from the anode side. The direct wafer bonding technique could be employed to manufacture this device. The SJ pillars can be formed either by using a trench and refill technique [11] or by other demonstrated techniques such as that reported in [12]. The proposed fabrication would require the front and backside wafers to be formed separately, with a SJ implant applied to both wafers. Additional wafer thickness is required to avoid damage during the SJ trench formation, which can later be removed prior to the wafer bonding. The n-buffer, p+ anode and remaining cathode and gate structures can be formed subsequently. The processing requirements for the backside are not as stringent as for the frontside since there are no cathode or gate structures. The two halves would be first bonded to glass carriers [13] and then etched to remove the excess wafer required for the SJ trench formation. The wafers are then bonded using a wafer bonding process as demonstrated in [13]–[16]. These studies have shown that the IGBT performance does not degrade using this technique. The results in section III demonstrate that there is no requirement for lateral alignment between these two wafers (frontside and backside).

Fig. 2 shows the electric field distributions under blocking conditions (1.2kV), for the standard RC-IGBT and Dual Implant SJ RC-IGBT with L_{gap}=40µm. The SJ pillars meet the condition for charge balance, such that the total charge in the n-doped and p-doped pillars are equal and deplete fully prior to device breakdown [17]. For both devices, breakdown occurs at the n+ injector layer at the cathode, but the presence of the SJ pillars alters the electric field distribution such that a larger voltage can be supported for a given device thickness. As a result, a SJ device can be made thinner for the same breakdown voltage to improve on-state performance, in line with previous studies [7], [9], [18].

Fig. 2 also shows three distinctive electric peaks in the drift region at 45µm, 85µm and 125µm which occur at the junctions between the superjunction pillars and the n-drift regions (n-buffer at 125µm). At all of these points the peak electric field is lower than the critical electric field and therefore does not affect the device operation. However, as reported in [9], this peak electric field at the p-pillar/n-buffer junction (125µm) meant the n-buffer doping had to be increased to prevent punch-through of the device. This increase in the buffer doping reduced the injection efficiency of the p+ anode which can be compensated for by increasing the p+ anode doping concentration.

III. Device On-State and Transient Performance

Application of the dual implanted SJ structure to the RC-IGBT supresses snapback in the forward direction while not affecting the reverse conduction. Fig. 3 shows the on-state characteristics where the cathode and anode SJ implants are aligned for varying L_{gap}. It was demonstrated in simulation that a deep SJ device (L_{gap}<10µm or L_{pillar}>54µm) either completely removes the snapback (L_{gap}<5µm) or it is very limited (L_{gap}=10µm). This is in line with the studies in [6], [7], however in this device the full SJ implantation (L_{pillar}) is 59µm; less than the 65µm limit imposed by current fabrication techniques.

Fig. 4 shows the effect of SJ pillar alignment in the x-direction, with the anode pillars misaligned fully (Fig. 1 (b)) and by 50%. The on-state characteristics show minimal variation; at 20A/cm^2 the on-state voltage varies by 0.03V between the half-offset and the fully aligned cells. This shows there is no requirement for alignment between the SJ pillars making this proposed device relatively easy to fabricate.

Overlapping of the SJ pillars (y-direction) was investigated. The on-state plots for varying amount of overlap (Fig. 5) shows minimal variation in the characteristic compared to the full SJ structure (Fig. 4) which is to be expected given the bipolar action of the IGBT. Fig. 5 shows the full offset device, but the result applies equally to the half offset and no offset cells.

With a 5µm overlap between pillars, for both full and half misalignment, the breakdown capabilities were unchanged. However, with full alignment between anode and cathode pillars the breakdown capabilities begin to degrade significantly. In the region where the pillars overlap, the SJ

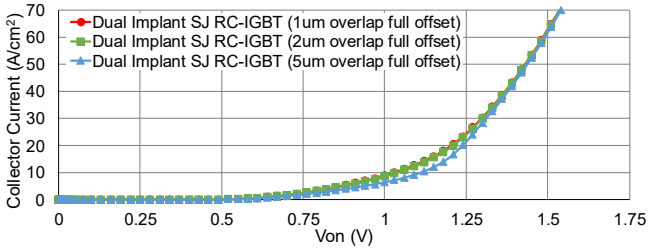

Fig. 5 On-state characteristics of Dual Implant SJ RC-IGBT with different amounts of overlap for full offset between anode and cathode SJ implants, ambient temperature = 298K

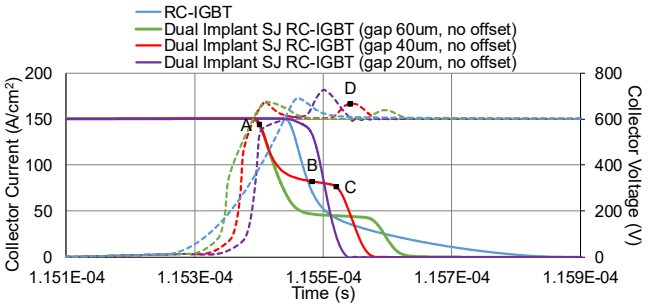

Fig. 6. Inductive load turn-off waveform for the Trench RC-IGBT and Trench Dual Implant SJ RC-IGBT with L_{gap}=60µm, 40µm and 20µm (no offset), ambient temperature = 298K. Dashed lines voltage; solid line current.

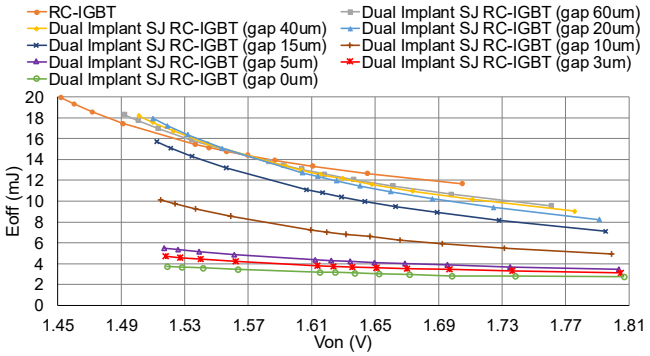

Fig. 7. Technology curves of Trench RC-IGBT and Dual Implant SJ RC-IGBT with varying L_{gap}, no offset, V_{on} at 100A/cm², ambient temperature 298K

charges add. For the fully misaligned cell, the charge from the p-doped pillars is cancelled out by the n-doped pillars resulting in a lowly doped region in the centre of the device (original n-drift doping concentration). For the no offset cell, SJ pillars are aligned and therefore in the overlapping region the pillar doping increases by a factor of two. Hence, under blocking conditions the overlapping area is unable to fully deplete as the conditions for charge balance are no longer met. With partial misalignment (half offset) the SJ pillars are able to compensate for the regions of charge imbalance, but with full alignment, a high electric field is produced in this highly doped central section of the drift region, resulting in premature breakdown. Therefore, to guarantee the performance of the device without the requirement for alignment between the SJ pillars, at most a 2µm overlap can occur, to ensure full drift layer depletion.

Fig. 6 shows the turn-off waveforms for the RC-IGBT and the dual implant SJ RC-IGBT with L_{gap} of 20µm, 40µm and 60µm. During turn-off, voltage is supported across the p-well/n-drift junction and the depletion extends down through the device (y-direction) towards the anode. The presence of the SJ structure induces a secondary lateral (x-direction) expansion of the depletion region which causes the higher breakdown capability (Fig. 2). In this dual implant device at the on-set of turn off (point A, Fig. 6) the cathode side SJ implant has already depleted to support the line voltage across the device, and Ic falls at a high dI/dt as the depletion region extends towards the anode through the lowly doped n-drift region. As the depletion region reaches the anode side SJ implant the collector current plateaus due to this secondary lateral expansion of the depletion region in the anode SJ pillars (point B, Fig. 6). This high voltage high current event could cause significant heating within the device; however, this plateau was eliminated for L_{gap}<20µm. Once the SJ pillars have been fully depleted, the collector current begins to fall rapidly (point C, Fig. 6) as the remaining excess charge is swept out of the device. This coincides with a small increase in collector voltage (point D, Fig. 6); Fig. 6 is an inductive load test and this second fast dI/dt event causes an increase in voltage across the inductor as seen in the waveform.

The device has been optimised for 600V operation, which constitutes the normal application range for a 1.2kV device. At this switching voltage the device shows good turn-off ruggedness (three times nominal current, 350A/cm²). Although the device is rugged up to 900V, at this switching voltage some unwanted oscillations are introduced due to the interaction between the depletion region and the highly doped buffer region, which also causes minimal tail current during turn-off. To address this issue, a simple re-optimisation of the n-buffer doping profile supresses this oscillation at 900V; achieving similar turn-off ruggedness without compromising the breakdown performance.

The technology curve given in Fig. 7 shows the advantage in removing the snapback; devices where L_{gap}<10µm exhibited negligible snapback and have significantly reduced turn-off losses. Compared to the traditional RC-IGBT, the full dual implant SJ RC-IGBT provides up to a 77% reduction in switching losses, and with L_{gap}=10µm a 39% reduction (V_{on} = 1.515V at 100A/cm²). The manufacturing requirements for the dual implant SJ RC-IGBT are therefore less restrictive, and a full SJ structure is not required to achieve significant improvements in performance; alleviating concerns regarding the overlapping of the anode and cathode SJ pillars during processing. To warrant the additional processing expense to implant the dual SJ structure, Fig. 7 shows that a deep SJ structure is required as there is little benefit in a partial implant.

IV. Conclusion

This letter presents the Dual Implant SJ RC-IGBT and describes how a full SJ structure can be manufactured within a 1.2kV device. Two separate SJ implants are applied to the device from both the anode and cathode sides and it has been demonstrated that there is no requirement for the pillars to be aligned. It has also been shown that for significant improvement in turn-off losses compared to a traditional RC-IGBT, a deep SJ device must be manufactured, with a maximum gap between the anode and cathode SJ pillars of 10µm such that there is negligible snapback in the on-state, and a maximum pillar overlap of 2µm to maintain breakdown capabilities. At most this Dual Implant SJ RC-IGBT achieved a 77% reduction in turn-off losses compared to the conventional RC-IGBT.

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