

Fault-tolerant magic state preparation with flag qubits

Christopher Chamberland^{1,2} and Andrew Cross¹

¹ IBM T. J. Watson Research Center, Yorktown Heights, NY, 10598, United States

² Institute for Quantum Computing and Department of Physics and Astronomy, University of Waterloo, Waterloo, Ontario, N2L 3G1, Canada

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Magic state distillation is one of the leading candidates for implementing universal fault-tolerant logical gates. However, the distillation circuits themselves are not fault-tolerant, so there is additional cost to first implement encoded Clifford gates with negligible error. In this paper we present a scheme to fault-tolerantly and directly prepare magic states using flag qubits. One of these schemes requires only three ancilla qubits, even with noisy Clifford gates. We compare the physical qubit and gate cost of our scheme to the magic state distillation protocol of Meier, Eastin, and Knill (MEK), which is efficient and uses a small stabilizer circuit. For low enough noise rates, we show that in some regimes the overhead can be improved by several orders of magnitude compared to the MEK scheme which uses Clifford operations encoded in the codes considered in this work.

1 Introduction

Certain algorithms can be implemented efficiently on quantum computers, whereas the best known classical algorithms require superpolynomial resources [1, 2]. At present, however, quantum devices are dramatically noisier than their classical counterparts. For all but the shortest depth quantum computations to succeed with high probability, operations will need to be performed with very low failure rates. Fault-tolerant quantum error correction provides one way to achieve the desired logical failure rates.

A straightforward way to implement fault-tolerant logical gates is to use transversal operations. However by the Eastin-Knill theorem, for any error correcting code, there will always be at least one gate in a universal gate set which cannot be implemented fault-tolerantly using transversal operations [3]. In recent years, many

proposals for fault-tolerant universal gate constructions have been introduced [4–9]. One of the earliest proposals, known as magic state distillation, uses resource states that, along with stabilizer operations, can simulate a non-Clifford operation [10, 11]. These resource states are called magic states since they can also be distilled using stabilizer operations. Despite considerable effort in alternative schemes, magic state distillation remains a leading candidate for universal fault-tolerant quantum computation.

Recently, very efficient distillation protocols have been developed which require substantially fewer resource states to achieve a desired target error rate of the magic state being distilled [12–15]. When studying magic state distillation protocols, it is often assumed that all Clifford operations can be implemented perfectly and that only the resource states can introduce errors into the protocol. However, with current quantum devices, two qubit gates are amongst the noisiest components of the circuits. In practice, Clifford gates with very low failure rates can be achieved by performing encoded versions of the gates in large enough error correcting codes, such that the failure rates of the Clifford operations are negligible compared to the non-Clifford components of the circuit. However the overhead cost associated with performing magic state distillation with encoded Clifford operations is often not considered (there are exceptions such as [16–19]). If the overhead cost of encoded Clifford operations is taken into account, it is not clear that magic state distillation schemes which minimize the resource state cost would achieve the lowest overhead when used in a quantum algorithm.

Recently, new schemes using flag qubits have been introduced to implement error correction protocols using the minimal number of ancilla qubits to measure the codes stabilizer generators [20–25]. The idea behind flag error correction is to use extra ancilla qubits which flag when $v \leq t$ faults result in a data qubit error of weight greater than v (here $t = \lfloor (d-1)/2 \rfloor$ where d is the distance of the code). The flag information can then be used in addition to the error syndrome to deduce the

Christopher Chamberland: christopher.chamberland@ibm.com

Andrew Cross: awcross@us.ibm.com

data qubit error.

In this paper, we propose a new scheme to fault-tolerantly prepare magic states which requires a minimal amount of extra ancilla qubits (in our case only one extra qubit). In particular, we consider a full circuit level noise model (which includes noisy Clifford operations) where gates can be applied between any pair of qubits. In this model, we compare the overhead cost of our scheme to a magic state distillation scheme introduced by Meier, Eastin and Knill (MEK), due to its efficiency and small circuit size [26]. Using the same encoded Clifford operations in both schemes, we show that in some regimes the qubit and gate overhead cost of our scheme can be smaller by several orders of magnitude as compared to the MEK scheme. We note that currently, state-of-the-art surface-code-based magic state distillation schemes are given in [27, 28]. Furthermore, an efficient state injection scheme using the surface code is given in [29]. The surface-code-based magic state distillation schemes have been shown to achieve logical error rates of 10^{-11} for physical error rates of 10^{-3} and can thus tolerate larger physical error rates than the scheme proposed in this work. On the other hand, in low noise rate regimes ($10^{-5} \leq p \leq 10^{-4}$), we show that the qubit and gate overhead cost of our scheme is lower compared to distance-three surface code implementations of magic state distillation. For larger distances, a more thorough analysis of surface code implementations of magic state distillation for error rates mentioned above is required to determine if our scheme has a smaller overhead. The scheme we numerically analyze in this work does require code concatenation for distances $d > 3$ and thus requires non-local connectivity[†]. However, the goal of this work is not solely to outperform the surface code, but instead to provide alternative magic state preparation schemes with low overhead. Indeed the proposed scheme in this work could be accessible to near term ion trap based architectures which could be amongst the first experiments to demonstrate the fault-tolerant implementation of logical non-Clifford gates.

We point out that a fault-tolerant magic state preparation scheme was previously considered by Aliferis, Gottesman and Preskill (AGP) in [30]. However, the scheme proposed by AGP requires the preparation and verification of large cat state ancillas to perform the logical measurements. Furthermore, Steane error correction, which requires a large number of extra ancilla qubits, was used for the error correction circuits. Our scheme does not require the preparation of large ancilla states, uses smaller error correction circuits, and has an improved threshold compared to the scheme proposed

[†]In addition we show how our scheme can be extended to higher distance color codes, but these are not numerically analyzed in this work.

by AGP.

The paper is structured as follows. In Section 2 we introduce the basic notation and noise model that we used throughout the remainder of the manuscript. In Section 3 we describe our scheme for fault-tolerantly preparing magic states. We provide both an error detecting and and correcting scheme. Proofs of fault-tolerance are given in Appendix A. In Section 4 we briefly review the MEK magic state distillation scheme and in Section 5 we compare the qubit and gate overhead costs of both schemes. Details of the overhead and numerical analysis are provided in Appendices C to E.

2 Basic notation and noise model

We define $\mathcal{P}_n^{(1)}$ to be the n -qubit Pauli group (i.e. n -fold tensor products of the identity I and the three Pauli matrices X , Y , and Z and all scalar multiples of them by ± 1 and $\pm i$). The Clifford group is defined by $\mathcal{P}_n^{(2)} = \{U : \forall P \in \mathcal{P}_n^{(1)}, UPU^\dagger \in \mathcal{P}_n^{(1)}\}$ and is generated by the single qubit Hadamard, $Y\left(\frac{\pi}{2}\right) = e^{-i\frac{\pi}{4}Y}$ gates

$$H = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}, \quad \text{and} \quad Y\left(\frac{\pi}{2}\right) = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & -1 \\ 1 & 1 \end{pmatrix}, \quad (1)$$

as well as $Z\left(\frac{\pi}{2}\right) = e^{-i\frac{\pi}{4}Z}$ and the two-qubit CNOT gate (which we write as C_X) with

$$C_X|a\rangle|b\rangle = |a\rangle|a \oplus b\rangle, \quad (2)$$

where $|a\rangle$ and $|b\rangle$ are computational basis states. In general, a controlled- U gate is

$$C_U = \frac{1}{2}(I + Z) \otimes I + \frac{1}{2}(I - Z) \otimes U. \quad (3)$$

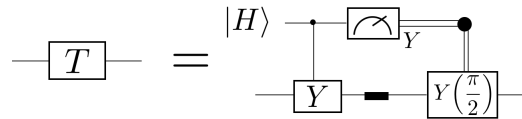


Figure 1: Circuit for simulating a T gate using an $|H\rangle$ state along with $Y\left(\frac{\pi}{2}\right)$ and C_Y gates and a measurement in the Y -basis. The $Y\left(\frac{\pi}{2}\right)$ gate is only applied if the measurement outcome is $+1$. The black rectangular box represents an idle location. The circuit for simulating T^\dagger is obtained by replacing $Y\left(\frac{\pi}{2}\right)$ with $Y\left(-\frac{\pi}{2}\right)$ and applying this gate if the measurement outcome is -1 .

The state

$$|H\rangle = \cos\frac{\pi}{8}|0\rangle + \sin\frac{\pi}{8}|1\rangle = T|0\rangle, \quad (4)$$

is the $+1$ eigenstate of the Hadamard operator and

$$T = e^{-i\frac{\pi Y}{8}} = \begin{pmatrix} \cos \frac{\pi}{8} & -\sin \frac{\pi}{8} \\ \sin \frac{\pi}{8} & \cos \frac{\pi}{8} \end{pmatrix} \quad (5)$$

does not belong to the Clifford group². We also write

$$|-H\rangle = Y|H\rangle \quad (6)$$

as the -1 eigenstate of the Hadamard operator.

The $|H\rangle$ state is an example of a magic state. Magic states can be distilled to produce reliable states from a larger number of noisy copies using only stabilizer operations [11]. The reliable magic states can be used, together with stabilizer operations, as resource states for universal quantum computation. In particular, as shown in Fig. 1, the $|H\rangle$ state, along with $Y\left(\frac{\pi}{2}\right)$, C_Y , and a measurement in the Y -basis, can be used to simulate a T gate. Note that some schemes choose to distill the state

$$|A_{\frac{\pi}{4}}\rangle \equiv \frac{1}{\sqrt{2}}(|0\rangle + e^{i\frac{\pi}{4}}|1\rangle) = e^{i\frac{\pi}{8}}HS^\dagger|H\rangle, \quad (7)$$

which is equivalent to the $|H\rangle$ state up to products of Clifford gates. For instance, see the $|A_{\frac{\pi}{4}}\rangle$ distillation scheme in [11].

Throughout this paper, we will use the following circuit-level noise model in all simulations:

1. With probability p , each single-qubit gate location is followed by a Pauli error drawn uniformly and independently from $\{X, Y, Z\}$.
2. With probability p , each two-qubit gate is followed by a two-qubit Pauli error drawn uniformly and independently from $\{I, X, Y, Z\}^{\otimes 2} \setminus \{I \otimes I\}$.
3. With probability $\frac{2p}{3}$, the preparation of the $|0\rangle$ state is replaced by $|1\rangle = X|0\rangle$. Similarly, with probability $\frac{2p}{3}$, the preparation of the $|+\rangle$ state is replaced by $|-\rangle = Z|+\rangle$.
4. With probability p , the preparation of the $|H\rangle$ state is replaced by $P|H\rangle$ where P is a Pauli error drawn uniformly and independently from $\{X, Y, Z\}$.
5. With probability $\frac{2p}{3}$, any single qubit measurement has its outcome flipped.
6. Lastly, with probability $p/100$, each idle gate location is followed by a Pauli error drawn uniformly and independently from $\{X, Y, Z\}$.

²Note that some references define the T gate as $T = \frac{e^{i\pi/4}}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ i & -i \end{pmatrix}$ which is a Clifford gate, while others define $T = \text{diag}(1, e^{i\pi/4})$ which is non-Clifford but Clifford-equivalent to the gate we have defined as T .

Our assumption of $p/100$ idle error is valid for systems whose gate errors are far from the limits set by coherence times. For example, trapped ion experiments have coherence times $T_2 = 2T_1$ on the order of $1 - 10$ seconds with gate times on the order of $10\mu s$. This suggests idle error probabilities of 10^{-5} to 10^{-6} , while two qubit gate infidelities are on the order of 10^{-3} to 10^{-4} [31, 32]. On the other hand, the assumption may not hold in systems such as superconducting qubits, whose gates currently achieve infidelities near the coherence limit [33]. Regardless, the concrete schemes we analyze all use the same underlying quantum code family and Clifford gate implementations, so we expect comparisons between them to be robust.

In the following sections, all Clifford gates and resource states will be encoded in the Steane code (see Section 3) which, paired with flag qubits, will allow us to obtain encoded magic states with low overhead. The code distance will be increased through code concatenation. Since the encoded version of the gates and states are implemented in a fault-tolerant way, the failure probability for each logical fault E of a gate G at a physical error rate p resulting from the malignant event $\text{mal}_E^{(1)}$ (where the superscript denotes the level of concatenation) can be upper bounded as

$$\Pr[\text{mal}_E^{(1)}|G, p] \leq \sum_{k=\lceil \frac{d}{2} \rceil}^{L_G} c(k)p^k \equiv \Gamma_G^{(1)}, \quad (8)$$

where $c(k)$ denotes the number of weight- k errors which can lead to a logical fault and L_G is the total number of circuit locations in the logical gate G . At the first concatenation level, we performed Monte-Carlo simulations with the above noise model to estimate the coefficients $c(k)$ for each logical gate and encoded states.

As was shown in [34–36], Eq. (8) can be generalized to the level- l concatenation level where each physical gate is replaced by its level- $(l-1)$ Rec³ (see [30] for more details). The error rate at the l -th concatenation level can be bounded as

$$\Pr[\text{mal}_E^{(l)}|G, p] \leq \sum_{k=\lceil \frac{d}{2} \rceil}^{L_G} c(k) \left(\Gamma_G^{(l-1)} \right)^k \equiv \Gamma_G^{(l)}. \quad (9)$$

In other words, to estimate the logical failure rate of a level- l gate, the probability of failure for all physical gates G in our level- l simulation will be replaced by

³Rectangles (Rec's) are encoded gates with trailing error correction units. Extended rectangles, which are encoded gates with leading and trailing error correction units, are abbreviated as exRec's.

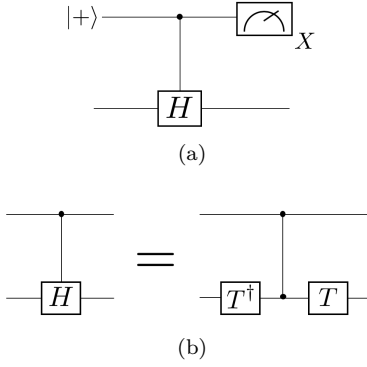


Figure 2: (a) Non-destructive measurement of the Hadamard operator. (b) The C_H gate can be decomposed into the gates T , C_Z and T^\dagger . As was shown in Fig. 1, the T gates can be simulated using only Clifford gates and an $|H\rangle$ resource state.

$\Pr[\text{mal}_E^{(l-1)}|G,p]$ obtained from a level- $(l-1)$ Monte-Carlo simulation. For the physical error rates we consider, higher order terms are found to be relatively small, so we only estimate the leading order terms. More details can be found in [34–36].

3 Preparing magic states in the Steane code

One way to measure the Hadamard operator using only Clifford gates and an $|H\rangle$ resource state is shown in Fig. 2. To obtain resource states with high-fidelity (which is required for universal quantum computation), one method is to encode them into an error detecting or error correcting code and perform several rounds of state-distillation. If the physical error rate is below some threshold (which depends on the codes and distillation routine), the error rate can be exponentially suppressed with the number of distillation rounds. Another, more direct method, is to fault-tolerantly prepare resource states in a large distance error correcting code. The distance is chosen to obtain the desired logical error suppression. In particular, in the presence of noisy Clifford gates, distillation routines require encoded Clifford operations which can substantially increase the qubit and gate overhead of the routine. We now show how to fault-tolerantly prepare an $|H\rangle$ state using the Steane code and flag-qubits in order to achieve a lower gate and qubit overhead. We will compare the overhead requirements of our methods with that of the Meier-Eastin-Knill (MEK) distillation routine [26]. A review of the MEK distillation routine is given in Section 4.

The Steane code is a $[[7, 1, 3]]$ CSS (Calderbank-Shor-Steane) code [37, 38] with stabilizer generators and logical operators given in Table 1. The Steane code has

$[[7, 1, 3]]$ Steane code	$[[4, 2, 2]]$ code
$g_1 = XIXIXIX$	$g_1 = XXXX$
$g_2 = IIIXXXX$	$g_2 = ZZZZ$
$g_3 = IXXIIXX$	
$g_4 = ZIZIZIZ$	
$g_5 = IIIZZZZ$	
$g_6 = IZZIIZZ$	
$\bar{X} = X^{\otimes 7}$	$\bar{X}_1 = XXII, \bar{X}_2 = XIIX$
$\bar{Z} = Z^{\otimes 7}$	$\bar{Z}_1 = ZIIZ, \bar{Z}_2 = ZZII$

Table 1: Stabilizer generators and logical operators of the $[[7, 1, 3]]$ Steane code and the $[[4, 2, 2]]$ error detecting code.

the property that all Clifford gates can be implemented transversally. In particular, the logical Hadamard operator is given by $\bar{H} = H^{\otimes 7}$. The fault-tolerant preparation of an encoded $|\bar{A}_{\pi/4}\rangle$ (see Eq. (7)) state has been previously analyzed in [30]. However, Steane error correction (not to confuse with the Steane code) was used for the EC units and cat states were fault-tolerantly prepared in order to measure $\bar{T}\bar{X}\bar{T}^\dagger$ ⁴. The high cost for preparing cat states and implementing Steane EC’s results in a large qubit overhead.

Instead of using Steane-EC circuits, in this work we consider an EC circuit recently introduced by Reichardt [25] for measuring the stabilizers of the Steane code with low circuit-depth and which requires only three ancilla qubits (see Fig. 3). The small qubit overhead is achieved with the use of flag qubits which can detect events where errors from a single fault spread to an X or Z error of weight greater than one on the data. The fault-tolerant properties of the circuit are discussed in Appendix A.1.

Flag-qubits can also be used to fault-tolerantly measure the logical Hadamard operator with only one extra ancilla qubit (and thus do not require the fault-tolerant preparation of cat states). In an error detection scheme, where the $|\bar{H}\rangle$ state is rejected if errors are detected, the circuit in Fig. 5a can be used to measure the logical Hadamard operator. If a fault results in an X or Z data qubit error of weight greater than one, the flag qubit (ancilla prepared in the $|0\rangle$ state) will be measured as -1 and the $|\bar{H}\rangle$ state will be rejected. The full error detecting scheme is shown in Fig. 5b⁵. Note that our scheme uses only 10-qubits and is shown to be fault-tolerant in Appendix A.2.

Error detection schemes have extra overhead arising

⁴Note that the T gates considered in this paper are Clifford-equivalent to the T gates considered in [30]

⁵In both Fig. 5a and Fig. 5b, the controlled Hadamard gates are implemented as shown in Fig. 2 and for concatenation levels greater than one, the T gates are implemented as in Fig. 1. See Appendix C for more details.

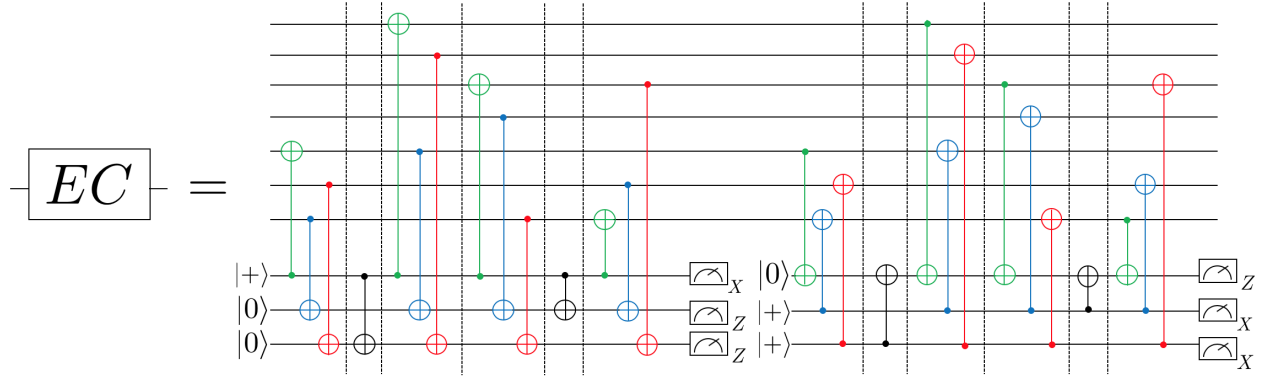


Figure 3: Fault-tolerant error correction circuit introduced by Reichardt [25] for measuring the stabilizers of the $[[7, 1, 3]]$ Steane code. The ancilla qubits act as flag qubits that flag if a single fault results in a data-qubit error of weight greater than one.

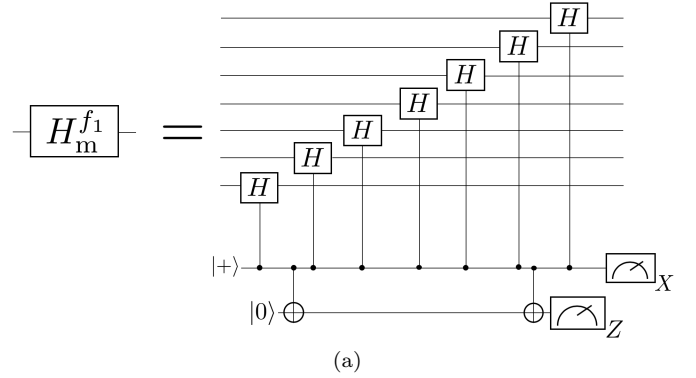
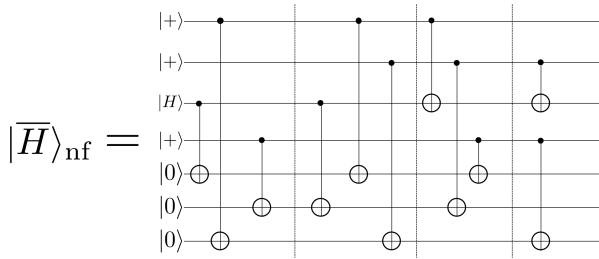


Figure 4: Non-fault-tolerant circuit for preparing a logical $|H\rangle$ state encoded in the $[[7, 1, 3]]$ Steane code. We label this circuit by $|\overline{H}\rangle_{\text{nf}}$. If there are no faults then $|\overline{H}\rangle_{\text{nf}} = T|0\rangle$.

from starting the process anew when a state is rejected (although they achieve much higher pseudo-thresholds). Alternatively, in Fig. 6 we show how the $|\overline{H}\rangle$ state can be fault-tolerantly prepared in an error correction scheme using three flag qubits. The details of the implementation and a proof of fault-tolerance is given in Appendix A.3. Due to the low pseudo-threshold of the error correction scheme, we will focus on the error detection scheme of Fig. 5 in the remainder of this manuscript.

The main motivation for concatenating the Steane code in order to increase the code distance is that finding flag circuits to measure high weight operators while maintaining error distinguishability is quite challenging [23]. However if a flag circuit satisfying the desired fault-tolerance criteria is found for a small code, the same circuit can be used at level- l where each gate is a level- $(l-1)$ gate. Additionally, if the data used in a quantum computation is encoded in the same code used to prepare the $|H\rangle$ state, the encoded $|H\rangle$ state does not need to be decoded and can be used to directly apply a logical T gate.

Lastly, we point out that following the 2-flag circuit construction of [23], it is possible to obtain a fault-

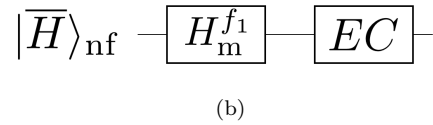


Figure 5: (a) Flag fault-tolerant circuit for measuring the the logical Hadamard operator of the $[[7, 1, 3]]$ Steane code in an error detection scheme. If a single fault results in a data qubit error of weight greater than one, the circuit will flag (the $|0\rangle$ state will be measured as -1) and the $|H\rangle$ state preparation scheme will begin anew. Note that the controlled Hadamard gates are implemented as shown in Fig. 2, where the T gates are implemented as in Fig. 1. (b) Full fault-tolerant error detection scheme for preparing an encoded $|H\rangle$ state. The EC circuit is given in Fig. 3 and the non-fault-tolerant circuit for preparing the encoded $|H\rangle$ state is given in Fig. 4.

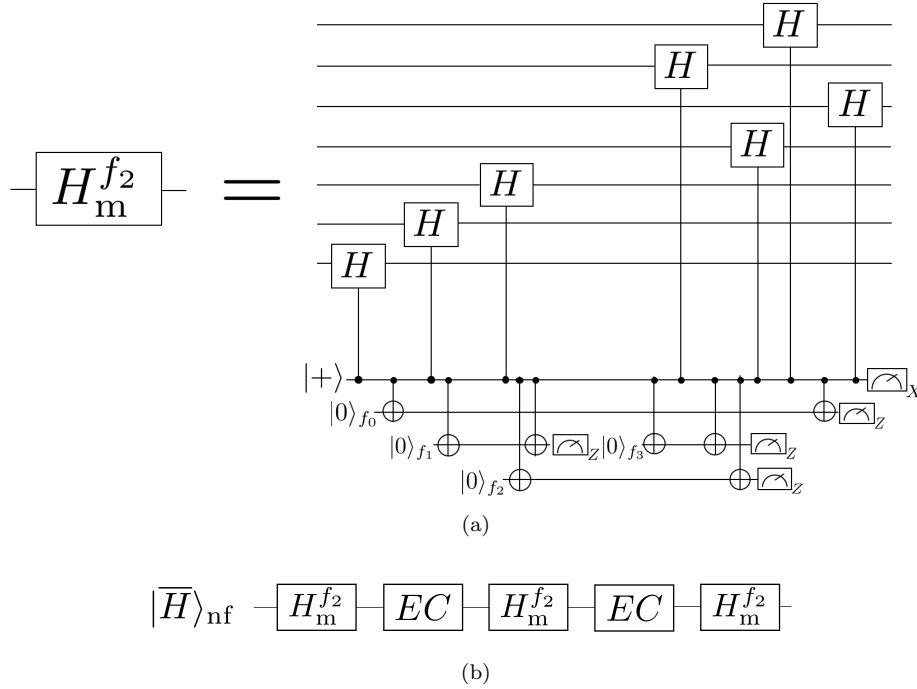


Figure 6: (a) Flag fault-tolerant circuit for measuring the the logical Hadamard operator of the $[[7, 1, 3]]$ Steane code. The extra flag qubits are used to localize errors occurring near the fourth controlled-Hadamard gate since these cannot be distinguished from errors occurring at the other controlled-Hadamard gates. Note that in order to distinguish errors from faults at other locations, the full six bit error syndrome must be considered. That is, we cannot correct X and Z errors separately as is usually done in CSS constructions. (b) Full fault-tolerant error correction scheme for preparing an encoded $|H\rangle$ state. The EC circuit is given in Fig. 3 and the non-fault-tolerant circuit for preparing the encoded $|H\rangle$ state is given in Fig. 4. If a flag occurs in the third $H_m^{f_2}$ measurement, an extra round of EC is performed.

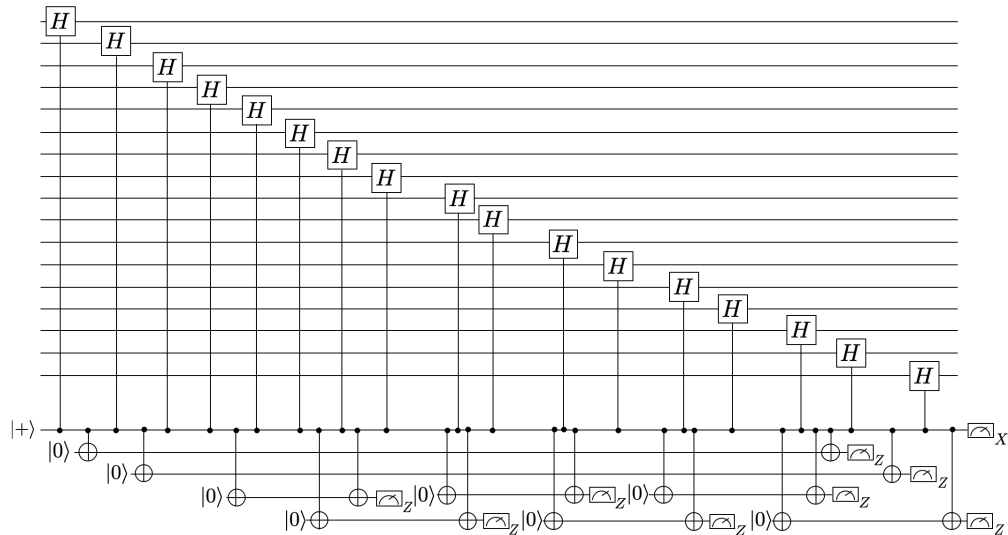


Figure 7: 2-flag circuit for measuring the logical Hadamard operator of the $[[17, 1, 5]]$ color code. This circuit can be used in an error detection scheme for fault-tolerantly preparing an $|H\rangle$ state encoded in the $[[17, 1, 5]]$ color code. If there are $v \leq 2$ faults which cause a data qubit error of weight greater than v , at least one of the flag qubits will flag and the $|H\rangle$ state will be rejected.

tolerant circuit to measure the logical Hadamard operator of the $[[17, 1, 5]]$ color code. The circuit is given in Fig. 7 and can be used in an error detection scheme analogous to that of Fig. 5. EC circuits for measuring the stabilizers of the $[[17, 1, 5]]$ color code were obtained in [23] and require at most four ancilla qubits. One could also measure the stabilizers using standard topological methods at the cost of requiring $\mathcal{O}(n)$ ancillas. This circuit could be useful if a higher distance is required prior to concatenation or if a hybrid state-preparation and magic state distillation scheme is used (see Section 5 for more details).

4 Meier-Eastin-Knill distillation circuits

In the MEK distillation protocol, $|H\rangle$ states are encoded in the $[[4, 2, 2]]$ error detecting code, whose stabilizer generators and logical operators are given in Table 1. For the $[[4, 2, 2]]$ code, the operator $H^{\otimes 4}$ is a valid encoded gate and performs the operation $\overline{H}_1 \overline{H}_2 \overline{\text{SWAP}}_{12}$ where $\overline{\text{SWAP}}_{12}$ swaps the two encoded qubits. The circuit in Fig. 8 performs an encoded measurement of $\overline{H}_1 \overline{H}_2$ on a pair of encoded $|H\rangle$ states and measures the stabilizers of the $[[4, 2, 2]]$ code (note that the circuit applies a Hadamard gate to one of the two encoded qubits). The routine accepts the pair of $|H\rangle$ states if both the $H^{\otimes 4}$ and syndrome measurements are trivial. More details can be found in [26].

Suppose that the desired output failure probability of the input resource states is $\mathcal{O}(p^{2^l})$. Note that a single fault in some of the two-qubit gates in Fig. 8 can result in multi-qubit errors on the data that go undetected⁶. Since all of the gates in Fig. 8 fail following the noise model described in Section 2, they must be encoded in another code (which we choose to be the level- l concatenated Steane code) in order to achieve the desired logical error rate in the output resource states. To provide a fair comparison between the overhead costs of our state preparation scheme with flag qubits and the MEK scheme, all exRec’s contain the EC unit of Fig. 3. These features will play an important role when evaluating the qubit and gate overhead of the MEK scheme.

Many magic state distillation protocols use a randomization called twirling [11] to diagonalize each magic state in a convenient basis. This greatly simplifies the analysis so that the acceptance probabilities and logical error rates can be found in closed form. However, twirling is not necessary in a physical implementation, since there is always another protocol without the randomization that uses the optimal choice of gates [39].

⁶This is due to the fact that magic state distillation circuits are fault-tolerant for noise models where errors are only introduced in resource states.

In our case, we observe that the logical error rates increase if we twirl, so we simply use the input states as they occur.

5 Resource overhead comparison

In this section we compare the overhead cost of our fault-tolerant magic state preparation scheme for preparing an encoded $|H\rangle$ state in the concatenated Steane code to the overhead cost of the MEK scheme for distilling $|H\rangle$ states (also encoded in the concatenated Steane code). In particular, we will compare the qubit and gate overhead cost of both schemes. In what follows, a level- l state or gate will always correspond to its encoded version in l concatenation levels of the Steane code.

For the MEK magic state distillation protocol, we consider two different approaches. In the first approach, physical $|H\rangle$ states are teleported into level-2 $|H\rangle$ states and a subsequent round of MEK (with level-2 Clifford gates) is applied to produce a state with a logical error rate well-approximated by the form $ap^2 + bp^4$ below the level-2 pseudo-threshold. The $\mathcal{O}(p^2)$ term is dominant at low error rates, and the $\mathcal{O}(p^4)$ term is dominant at error rates near the pseudo-threshold. To obtain further error suppression, we then teleport the distilled state into a level-3 state and perform a level-3 round of MEK to obtain a state with a logical error rate of the form $a'p^4 + b'p^8$. An additional round of MEK could be performed to obtain an $|H\rangle$ state with logical error rate $\mathcal{O}(p^8)$. However, for the physical error rates considered in this work ($p \in [10^{-5}, 10^{-4}]$), we found that there is no advantage in doing so.

In the second approach, we consider a hybrid scheme where a level-2 $|H\rangle$ state is first prepared using our fault-tolerant flag preparation scheme. The state is then teleported into a level-3 state and a round of MEK is performed resulting in an $|H\rangle$ state with logical error rate $\mathcal{O}(p^8)$. All teleportation schemes are performed using the methods described in Appendix B.

The qubit and gate overhead results for the magic state preparation scheme with flag qubits and the MEK schemes are shown in Figs. 9 to 11. Details of the analysis leading to the plots are given in Appendices C and D.

Comparing the results, it is clear that the qubit and gate overhead cost of the fault-tolerant $|H\rangle$ state preparation scheme of Fig. 5 is substantially smaller than schemes involving MEK. The primary reasons for this are due to the high pseudo-threshold of the error detection scheme as well as the small size of the circuits compared to the circuits used by MEK (where we used the teleportation scheme of Appendix B to inject states at a higher concatenation level). Further, note that the hybrid scheme (Fig. 11) has smaller qubit and gate over-

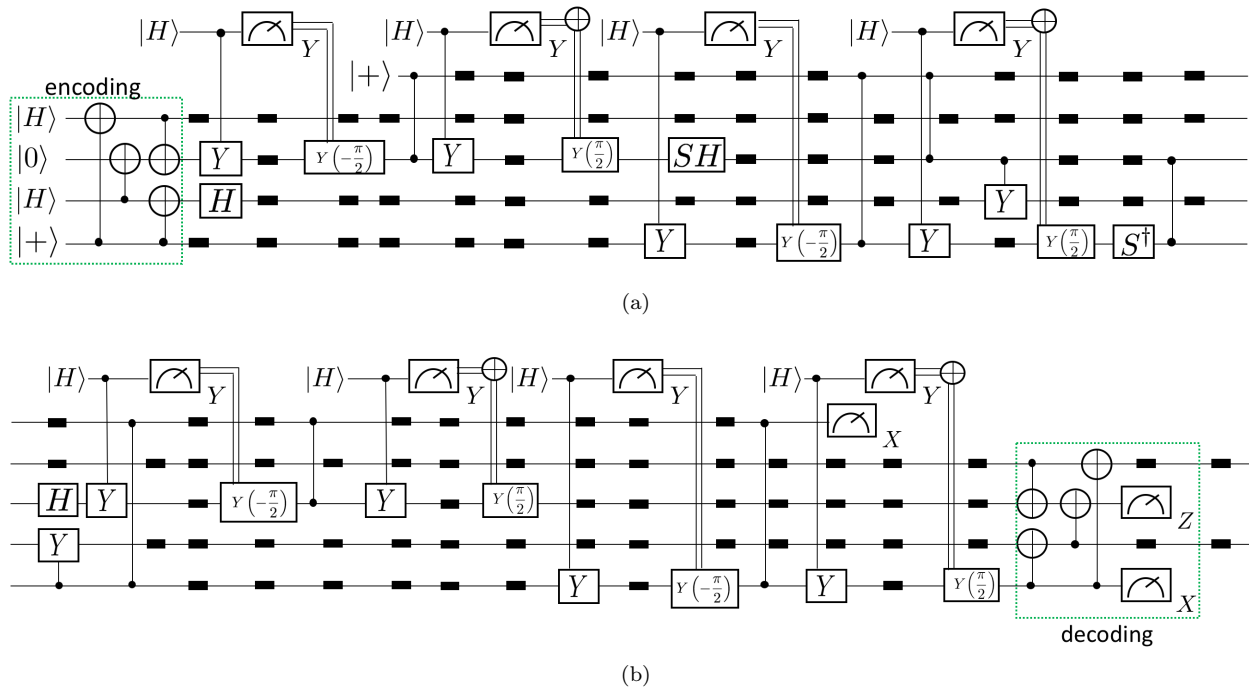


Figure 8: (a) First half of the MEK distillation circuit. (b) Second half of the MEK distillation circuit. The circuit is the same as given in [26] but has been written in detail to illustrate the idle qubit locations (filled rectangles). We reuse the $|H\rangle$ ancilla qubit instead of doing gates in parallel in order to minimize the overhead cost. A total of four C_H gates are required to measure the operator $\overline{H}_1 \overline{H}_2$.

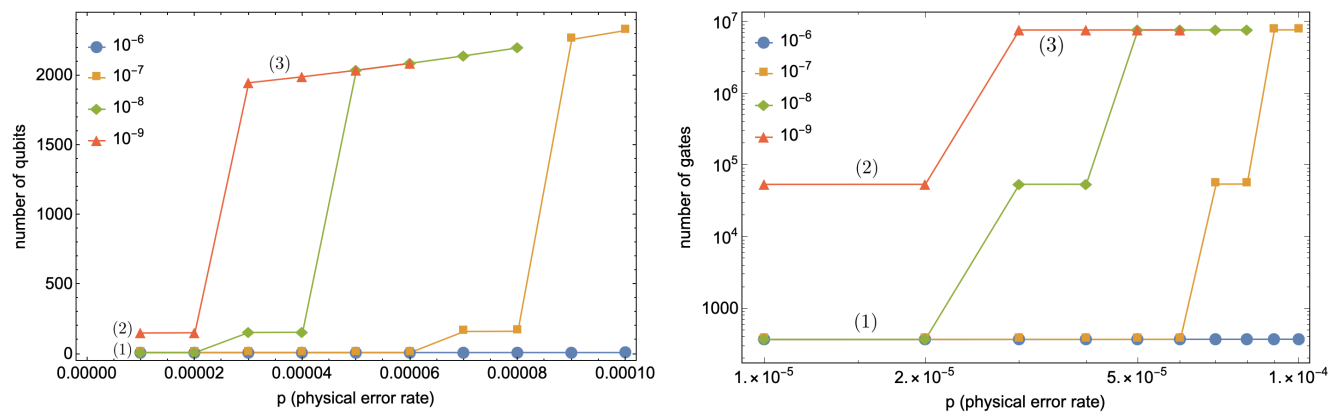


Figure 9: Qubit and gate overhead for our fault-tolerant magic state preparation scheme using flag qubits. We considering target logical failure rates ranging between 10^{-6} to 10^{-9} . The different jumps in the curves indicate that an additional concatenation level is required in order to achieve the desired logical failure rate. Note that the y axis of the qubit overhead plot is not displayed on a log scale. This is to show the increase in overhead cost due to the probability of rejecting a state when implementing the error detection scheme.

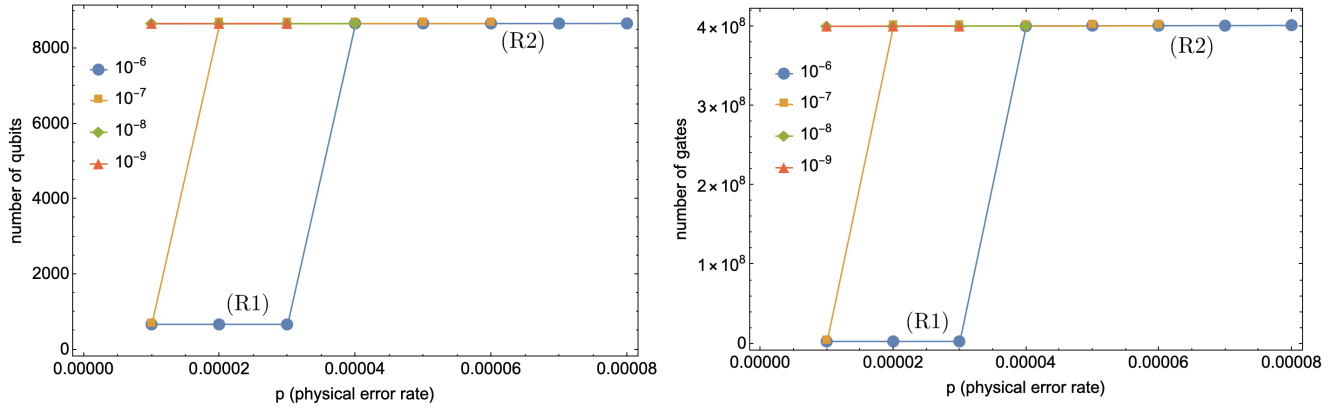


Figure 10: Qubit and gate overhead for the MEK protocol applied to level-2 and level-3 $|H\rangle$ states. In order to achieve the desired logical failure rate, we teleport a level-2 $|H\rangle$ state into a level-3 $|H\rangle$ state and apply one round of level-3 MEK. In a level- l simulation, all gates in the MEK circuit are encoded at level- l .

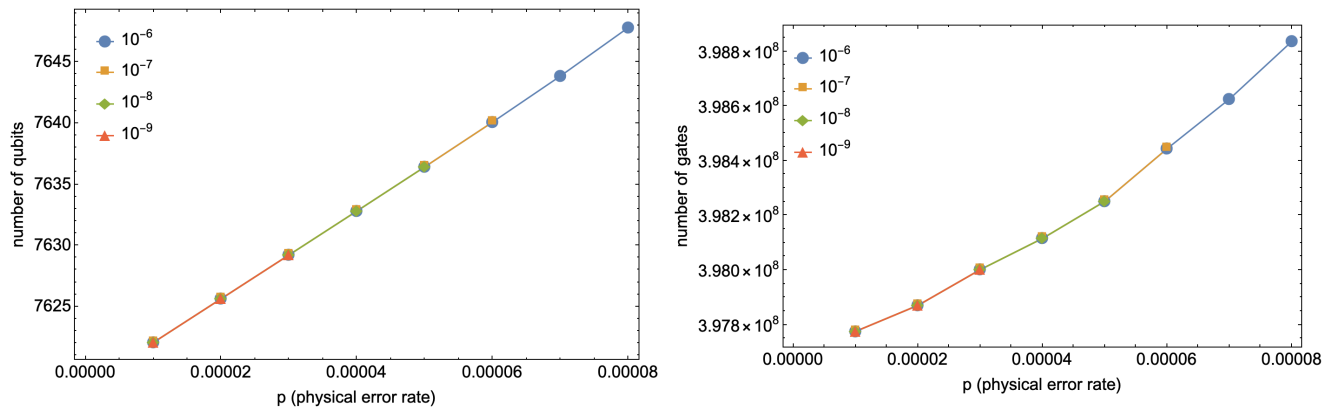


Figure 11: Qubit and gate overhead for the hybrid scheme. First a level-2 $|H\rangle$ state is fault-tolerantly prepared using the methods of Fig. 5. Afterwards the state is teleported to a level-3 state and a round of level-3 MEK is performed.

head costs compared to the full MEK scheme (Fig. 10), although the overhead is still much larger than the error detection scheme using flag qubits.

Lastly, we point out that due to the lower logical failure rates of the error detection scheme using flag qubits, three concatenation levels were sufficient to achieve logical failure rates of 10^{-9} for larger physical error rates compared to MEK (the same is true for other target logical failure rates). For example, suppose one wants to achieve a logical failure rate $p_L \leq 10^{-9}$. In our error detection scheme, one must use at least four concatenation levels for physical error rates $p > 6 \times 10^{-5}$. For the MEK scheme, one requires four concatenation levels for physical error rates $p > 4 \times 10^{-5}$. Hence for physical error rates $4 \times 10^{-5} \leq p \leq 6 \times 10^{-5}$, the error detection scheme will require fewer qubits by *several orders of magnitude* compared to MEK (see Figs. 9 and 10).

6 Conclusion

The high cost of universal fault-tolerant logic is a challenging and enduring problem. In this work, we propose an alternative to magic state distillation that is based on recently discovered flag fault-tolerance techniques. We have designed a flag-based magic state preparation scheme that reduces the number of qubits and operations to prepare a reliable magic state, and does so by orders of magnitude in some error regimes. Furthermore, the error-detection-based state preparation circuit at level-1 has a high pseudothreshold and uses a total of 10 qubits. The circuit accepts around 80% of the time and has logical error rates near 10^{-4} at physical error rates near 3×10^{-3} (see Table 4), making it an interesting candidate for experimental consideration.

The magic state preparation scheme relies on a transversal Hadamard operator and a flag circuit for measuring it fault-tolerantly. So that the operator's weight does not grow, we concatenate the code with itself to achieve some low logical error rate. The threshold is ultimately that of the concatenated Steane code in all of the schemes we analyze. It would be interesting to account for more realistic constraints on qubit connectivity, and to consider how to extend these techniques to families of higher distance (non-concatenated) codes, but we leave this to future work.

Another interesting application of our work is its use in state injection schemes [29, 40]. Using the fault-tolerant circuits for distance-three and five color codes in Figs. 5 and 7 (the w -flag circuits described in [23] could also be used for higher distance color codes), encoded magic states with logical failure rates of $\mathcal{O}(p^2)$ and $\mathcal{O}(p^3)$ can be produced. Lattice surgery techniques could then be performed to further distill the input magic states [40, 41]. We note that the state injection

scheme in [29] produces encoded magic states with logical failure rate $\mathcal{O}(p)$ and thus for low enough physical error rates, our approach could achieve lower logical failure rates.

If codes such as topological codes were used to perform the MEK protocol at high physical error rates, then magic state distillation might outperform the flag-based scheme, since a large number of concatenation levels would be necessary. However, the ideas we have presented may be broadly applicable to improve the pseudothreshold of magic state preparation circuits using codes other than the Steane code. In this direction, we have given a 2-flag circuit for fault-tolerantly measuring logical Hadamard of the 17-qubit color code. If lower logical error rates are needed, states could then be used in a hybrid approach that takes advantage of the topological code threshold. Lastly, one could use the w -flag circuit construction and EC circuits of [23] to fault-tolerantly prepare magic states for the family of color codes on a hexagonal lattice.

7 Acknowledgements

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A Proof of fault-tolerance for the magic state preparation schemes

In this appendix we provide proofs showing that our magic state preparation schemes for the $|H\rangle$ state are fault-tolerant. In what follows, a state-preparation scheme will be called fault-tolerant if the following two conditions are satisfied [42]

Definition 1. *Fault-tolerant state preparation*

For $t = \lfloor (d-1)/2 \rfloor$, a state-preparation protocol using a distance- d stabilizer code C is t -fault-tolerant if the following two conditions are satisfied:

1. If there are s faults during the state-preparation protocol with $s \leq t$, the resulting state differs from a codeword by an error of at most weight s .
2. If there are s faults during the state-preparation protocol with $s \leq t$, then ideally decoding the output state results in the same state that would be obtained from the fault-free state-preparation scheme.

In Definition 1, ideally decoding is equivalent to performing fault-free error correction. Now suppose $|\bar{\psi}\rangle$ is the encoded state to be prepared. If there are $s \leq t$ faults during a state-preparation protocol satisfying the criteria in Definition 1, then the output state will have the form $E|\bar{\psi}\rangle$ with $\text{wt}(E) \leq s$ (the output state will encode the correct state with no more than s errors).

For CSS codes, this definition can be applied independently to X and Z errors.

A.1 Error correction circuit

In this section we provide more details on the properties of the EC circuit of Fig. 3 which is used in all of our schemes.

The first half of the circuit measures the $XIXIXIX$ (green CNOT's), $IIIZZZZZ$ (blue CNOT's) and $IZZIIIZZ$ (red CNOT's) stabilizers of the Steane code. The second half of the circuit measures the remaining stabilizers. Given that the CNOT gates are not transversal, it is possible for a single fault to result in a weight-two X or Z data-qubit error. However the ancilla qubits also act as flag qubits which can be used to detect such events.

$$|\psi^{(2)}\rangle = \frac{1}{2} \left\{ \left(E_i^{(x)} E_j^{(z)} \bar{E}_i^{(x)} \bar{E}_j^{(z)} + E_i^{(z)} E_j^{(x)} \bar{E}_i^{(z)} \bar{E}_j^{(x)} \right) |\bar{H}\rangle |+\rangle + \left(E_i^{(x)} E_j^{(z)} \bar{E}_i^{(x)} \bar{E}_j^{(z)} - E_i^{(z)} E_j^{(x)} \bar{E}_i^{(z)} \bar{E}_j^{(x)} \right) |\bar{H}\rangle |-\rangle \right\}. \quad (11)$$

If $E_i^{(x)} \neq I$ or $E_j^{(z)} \neq I$, then the single-qubit error will

Let us assume that a single-fault occurs. For the first half of the EC circuit, the possible weight-two errors that can arise from a single fault are Z_4Z_6 , Z_3Z_7 , and X_3X_7 . In the case of Z_4Z_6 and Z_3Z_7 , the measurement in the X -basis will flag (with the two Z -basis measurements being $+1$), at which point the entire syndrome measurement is repeated. Since Z_4Z_6 and Z_3Z_7 are errors that have different syndromes than all other errors arising from a single fault leading to a $-++$ measurement outcome of the first three ancilla qubits, after the syndrome measurement is repeated these errors can be distinguished and corrected.

The same argument applies to the case where a single fault leads to the X_3X_7 data-qubit error. But this time the X_4 error has the same syndrome as X_3X_7 ($s(X_4) = s(X_3X_7) = 010000$). However, the faults causing an X_3X_4 error result in a $+--$ measurement outcome of the first three ancillas whereas X_4 results in $+-+$. Thus when the syndrome measurement is repeated and the flag outcomes are taken into account, the errors can be distinguished and corrected.

An analogous analysis can be applied to the second half of the EC circuit. See [25] for more details.

A.2 Fault-tolerance proof for the error detection scheme

Recall that the error detection scheme can be decomposed into three components as shown in Fig. 5b. Since $t = 1$ for the $[[7, 1, 3]]$ Steane code, we must show that if a single fault occurs in any of the three components, both criteria in Definition 1 will be satisfied.

Case 1: fault in $|\bar{H}\rangle_{\text{nf}}$ (see Fig. 4). Since the Steane code is a perfect CSS code and the $|\bar{H}\rangle_{\text{nf}}$ circuit is not fault-tolerant, the output state of the first component will have the form

$$|\psi^{(1)}\rangle = E_i^{(x)} E_j^{(z)} \bar{E}_i^{(x)} \bar{E}_j^{(z)} |\bar{H}\rangle, \quad (10)$$

where $E_i^{(x)} \in \{I, X_i\}$ and $E_j^{(z)} \in \{I, Z_j\}$ are single-qubit errors on qubits i and j and $\bar{E}_i^{(x)} \in \{I, \bar{X}\}$, $\bar{E}_j^{(z)} \in \{I, \bar{Z}\}$ are logical operators of the Steane code.

Now the output state of the second component of Fig. 5b, including the contribution from the first ancilla qubit (which will subsequently be measured in the X -basis), is given by

be detected by the subsequent EC and the state will be

rejected. Thus let us assume that $E_i^{(x)} = E_j^{(z)} = I$ so that

$$|\psi^{(2)}\rangle = \frac{1}{2} \left\{ \left(\bar{E}_i^{(x)} \bar{E}_j^{(z)} + \bar{E}_i^{(z)} \bar{E}_j^{(x)} \right) |\bar{H}\rangle |+\rangle + \left(\bar{E}_i^{(x)} \bar{E}_j^{(z)} - \bar{E}_i^{(z)} \bar{E}_j^{(x)} \right) |\bar{H}\rangle |-\rangle \right\}. \quad (12)$$

If $\bar{E}_i^{(x)} \bar{E}_j^{(z)} = \bar{Y}$, then $|\psi^{(2)}\rangle = |-\bar{H}\rangle |-\rangle$ and the ancilla measurement will be -1 resulting in rejection. Thus suppose that $\bar{E}_i^{(x)} \bar{E}_j^{(z)}$ is \bar{X} or \bar{Z} so that

$$|\psi^{(2)}\rangle = \frac{1}{\sqrt{2}} \left\{ |\bar{H}\rangle |+\rangle \mp i |-\bar{H}\rangle |-\rangle \right\}, \quad (13)$$

where we used the identities $H = \frac{1}{\sqrt{2}}(X + Z)$, $XHX = \frac{1}{\sqrt{2}}(X - Z)$ and $ZHZ = \frac{1}{\sqrt{2}}(Z - X)$. From Eq. (13), we see that $|\psi^{(2)}\rangle$ will be accepted with probability $1/2$ resulting in the state $|\bar{H}\rangle$. Thus if a single fault occurs in the first component of Fig. 5b, an accepted state will be $|\bar{H}\rangle$.

Case 2: fault in $H_m^{f_1}$ (see Fig. 5a). Since there are no faults in $|\bar{H}\rangle_{\text{nf}}$, the input to the circuit will be $|\bar{H}\rangle$. If the fault results in any measurement outcome to be -1 , the state will be rejected. Thus we only consider faults such that the measurement outcome of all ancilla's is $+1$. Since the circuit will flag if a single fault results in a data-qubit error of weight greater than one, the output state of the circuit will be $|\psi_{\text{out}}^{(2)}\rangle = E_i^{(x)} E_j^{(z)} |\bar{H}\rangle$ with $\text{wt}(E_i^{(x)}) \leq 1$ and $\text{wt}(E_j^{(z)}) \leq 1$. If $E_i^{(x)} E_j^{(z)}$ is non-trivial, it will be detected by the subsequent EC circuit and the state will be rejected. Hence an accepted state will be $|\bar{H}\rangle$.

Case 3: fault in the EC circuit (see Fig. 3). Since there are no faults in the first two components of Fig. 5b, the input state to the EC will be $|\psi^{(3)}\rangle = |\bar{H}\rangle$. If a fault causes a non-trivial measurement, the state will be rejected. Hence let us consider the case where a single fault results in an error which goes undetected. A single fault in the EC can result in a data-qubit error of the form $E_i^{(x)} E_j^{(z)}$ where $\text{wt}(E_i^{(x)}) \leq 1$ and $\text{wt}(E_j^{(z)}) \leq 1$ without any flags⁷. However, due to the fault-tolerant properties of the EC, a fault resulting in a data error with $\text{wt}(E_i^{(x)}) \geq 2$ or $\text{wt}(E_j^{(z)}) \geq 2$ will cause one of the flag qubits to flag. Hence if the state is accepted (all measurements are trivial), the output state of the EC will have the form

$$|\psi_{\text{out}}\rangle = E_i^{(x)} E_j^{(z)} |\bar{H}\rangle, \quad (14)$$

with $\text{wt}(E_i^{(x)}) \leq 1$ and $\text{wt}(E_j^{(z)}) \leq 1$. Since errors of the form $E = X_i Z_j$ are correctable by the Steane code,

⁷As an example, consider the error $Z \otimes X$ on the fourth black CNOT of Fig. 3 which results in the data-qubit error $X_6 Z_7$.

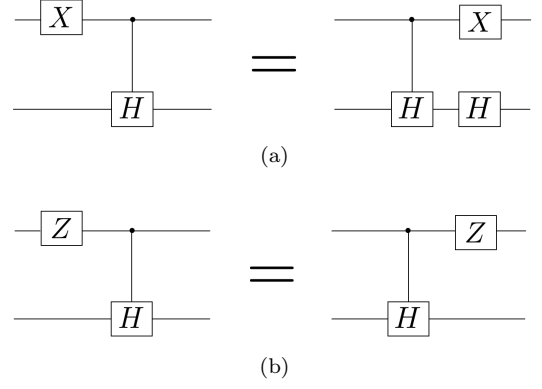


Figure 12: (a) Propagation of X errors through the control-qubit of a controlled-Hadamard gate. This induces a Hadamard error on the target qubit. (b) Propagation of a Z error through the control-qubit of a controlled-Hadamard gate.

fault-free error correction of an accepted state of the protocol in Fig. 5b will always result in the state $|\bar{H}\rangle$. We conclude that if there is at most one fault, both criteria in Definition 1 will be satisfied.

A.3 Fault-tolerance proof for the error correction scheme

A.3.1 Error distinguishability

Recall that for the error correction scheme, the circuit for measuring the logical Hadamard operator is given in Fig. 6a. The first thing to notice is that the controlled-Hadamard gates are implemented in a different order compared to the gates in Fig. 5a. If a fault occurs at one of the controlled-Hadamard gates resulting in an X or Y error on the control-qubit, the resulting data qubit error can be expressed as a product of Hadamard errors and Pauli errors (see Fig. 12). For the second to sixth controlled-Hadamard gates, all errors arising from a single fault at one of these locations which propagate to the data qubits (causing at least one of the flag qubits to flag) must be distinguishable (since $\bar{H} = H^{\otimes 7}$, a fault occurring at the first controlled-Hadamard gate will result in an X and Z data-qubit error of weight at most one). This is only possible if errors are corrected based on their full syndrome⁸ and with a carefully chosen ordering of the controlled-Hadamard gates. Performing a numerical search of all $7! = 5040$ permutations of the controlled-Hadamard gates, there was

⁸Instead of using a three-bit syndrome for correcting X errors and separately using the other three-bit syndrome to correct Z errors, one would use the full six-bit syndrome to correct the data errors. Note that we only correct using the full six-bit syndrome if there are flags. Otherwise, we perform the standard CSS correction of X and Z errors separately.

no permutation that allowed all possible errors (arising from a single fault) to be distinguished. However, ignoring a fault on the fourth controlled-Hadamard gate, a numerical search showed that the ordering found in Fig. 6a allows errors arising from a single fault to be distinguished. Consequently, we need to have the ability to isolate errors arising from a fault at the fourth controlled-Hadamard location. This can be achieved using the two extra flag qubits shown in Fig. 6a ($|0\rangle_{f_1}$ and $|0\rangle_{f_3}$ can be measured using the same qubit).

Suppose for example that an X error arises on the control-qubit of the fourth controlled-Hadamard gate resulting in the data qubit error $P_2 H_1 H_3 H_4$, where $P_2 \in \{I, X_2, Y_2, Z_2\}$. Then $|0\rangle_{f_0}$, $|0\rangle_{f_2}$ and $|0\rangle_{f_3}$ will flag. We could then apply $H_1 H_3 H_4$ to the data qubit and be left with the single-qubit Pauli P_2 . Of course, if a fault occurs on the first CNOT connecting $|0\rangle_{f_3}$ to the $|+\rangle$ state resulting in an $X \otimes X$ error, $|0\rangle_{f_3}$ will not flag but $|0\rangle_{f_2}$ will flag (in addition to $|0\rangle_{f_0}$). After applying $H_1 H_3 H_4$, the resulting data qubit error would be H_2 . Going through all possible cases of a single fault at one of the CNOT gates interacting the ancillas $|0\rangle_{f_1}$, $|0\rangle_{f_2}$ and $|0\rangle_{f_3}$ with the $|+\rangle$ state, we can guarantee error distinguishability by applying $H_1 H_3 H_4$ to the data if the following combinations of flag qubits flag:

1. $|0\rangle_{f_0}$ and $|0\rangle_{f_2}$ flag.
2. $|0\rangle_{f_0}$ and $|0\rangle_{f_3}$ flag.
3. $|0\rangle_{f_0}$, $|0\rangle_{f_2}$ and $|0\rangle_{f_3}$ flag.

Note that $|0\rangle_{f_0}$ would not flag if a single measurement error of the flag qubits $|0\rangle_{f_1}$, $|0\rangle_{f_2}$ or $|0\rangle_{f_3}$ occurred.

When following the circuit in Fig. 6b by an EC circuit, we will use a lookup-table containing all errors arising from a single fault resulting in a flag (which are all distinguishable) in order to correct.

A.3.2 Fault-tolerance proof

Given the above for applying Hadamard corrections to the data qubits depending on the flag outcomes (thus guaranteeing error distinguishability if a single fault occurs), we now show that our error correcting scheme shown in Fig. 6b satisfies both criteria in Definition 1. In what follows, $|\psi_{\text{final}}\rangle$ will correspond to the output state of the circuit in Fig. 6b. Also, the state at the output of the i 'th circuit in Fig. 6b will be labeled as $|\psi^{(i)}\rangle$. For instance, the state at the output of $|\overline{H}\rangle_{\text{nf}}$ will be $|\psi^{(1)}\rangle$.

Case 1: fault in $|\overline{H}\rangle_{\text{nf}}$.

The output of $|\overline{H}\rangle_{\text{nf}}$ is given by Eq. (10). To simplify the notation, let $\overline{E} = \widetilde{E}_i^{(x)} \widetilde{E}_j^{(z)}$, $\widetilde{E} = (\overline{H})\overline{E}(\overline{H})$, $E_p = E_i^{(x)} E_j^{(z)}$, and $\widetilde{E}_p = \overline{H} E_p \overline{H}$. With this notation, the

output to the first $H_m^{f_2}$ circuit (where we only write the first ancilla since the flag qubits have no effect) can be written as

$$|\psi^{(2)}\rangle = \frac{E_p \overline{E} + \widetilde{E}_p \widetilde{E}}{2} |\overline{H}\rangle|+\rangle + \frac{E_p \overline{E} - \widetilde{E}_p \widetilde{E}}{2} |\overline{H}\rangle|-\rangle \quad (15)$$

There are several cases to consider

1. $E_p = I$.

If $\overline{E} \in \{\overline{X}, \overline{Z}\}$,

$$|\psi^{(2)}\rangle = \frac{1}{2} |\overline{H}\rangle|+\rangle \pm \frac{1}{2} i |-\overline{H}\rangle|-\rangle. \quad (16)$$

Thus a ± 1 measurement outcome gives $|\pm \overline{H}\rangle$ and all three $H_m^{f_2}$ circuits will result in a ± 1 outcome. If $\overline{E} = \overline{Y}$, $|\psi^{(2)}\rangle = |-\overline{H}\rangle|-\rangle$ and all three $H_m^{f_2}$ measurement outcomes will be -1 .

For the case where all three measurement outcomes are -1 , applying \overline{Y} to $|\psi_{\text{final}}\rangle$, we will have $|\psi_{\text{final}}\rangle = |\overline{H}\rangle$.

2. $E_p = Y_i$.

In this case

$$|\psi^{(2)}\rangle = \frac{1}{2} Y_i (\overline{E} - \widetilde{E}) |\overline{H}\rangle|+\rangle + \frac{1}{2} Y_i (\overline{E} + \widetilde{E}) |\overline{H}\rangle|-\rangle. \quad (17)$$

If $\overline{E} \in \{\overline{X}, \overline{Z}\}$, $|\psi^{(2)}\rangle = \pm \frac{i}{\sqrt{2}} Y_i |-\overline{H}\rangle|+\rangle + \frac{1}{\sqrt{2}} Y_i |\overline{H}\rangle|-\rangle$. The Y_i error will be corrected by the following EC round. For a ± 1 measurement outcome, $|\psi^{(2)}\rangle = Y_i |\mp \overline{H}\rangle$ and the next two $H_m^{f_2}$ measurements will be ∓ 1 with $|\psi_{\text{final}}\rangle = |\mp \overline{H}\rangle$. Thus if the three $H_m^{f_2}$ measurement outcomes are $+-$, applying \overline{Y} to $|\psi_{\text{final}}\rangle$ will give $|\psi_{\text{final}}\rangle = |\overline{H}\rangle$. If the measurement outcome is $-++$, $|\psi_{\text{final}}\rangle = |\overline{H}\rangle$.

If $\overline{E} = \overline{Y}$, $|\psi^{(2)}\rangle = Y_i |-\overline{H}\rangle|+\rangle$ and Y_i will be corrected by the next EC. Hence the three $H_m^{f_2}$ measurement outcomes will be $+-$. Applying \overline{Y} to $|\psi_{\text{final}}\rangle$ will result in $|\psi_{\text{final}}\rangle = |\overline{H}\rangle$.

Lastly, if $\overline{E} = I$, $|\psi^{(2)}\rangle = Y_i |\overline{H}\rangle|-\rangle$. The Y_i error will be corrected by the next EC and the three $H_m^{f_2}$ measurements will be $-++$.

3. $E_p \in \{X_i, Z_j\}$.

If $\overline{E} = \overline{Y}$ then

$$|\psi^{(2)}\rangle = \pm \frac{1}{2} (X_i - Z_i) |-\overline{H}\rangle|+\rangle + \frac{1}{2} (X_i + Z_i) |-\overline{H}\rangle|-\rangle. \quad (18)$$

The three $H_m^{f_2}$ measurements will be $\pm - -$ with $|\psi_{\text{final}}\rangle = |-\bar{H}\rangle$. Applying \bar{Y} will give the correct state.

If $\bar{E} \in \{\bar{X}, \bar{Z}\}$, we have

$$|\psi^{(2)}\rangle = \frac{1}{2}(X_i\bar{Z} + Z_i\bar{X})|\bar{H}\rangle|+\rangle \pm \frac{1}{2}(Z_i\bar{X} - X_i\bar{Z})|\bar{H}\rangle|-\rangle, \quad (19)$$

or

$$|\psi^{(2)}\rangle = \frac{1}{2}(X_i\bar{X} + Z_i\bar{Z})|\bar{H}\rangle|+\rangle \pm \frac{1}{2}(X_i\bar{X} - Z_i\bar{Z})|\bar{H}\rangle|-\rangle. \quad (20)$$

Since in both Eqs. (19) and (20) the states are linear combinations of products of single-qubit Pauli's and logical operators, after the first EC circuit the output state will collapse to $|\psi^{(3)}\rangle = \bar{E}|\bar{H}\rangle$ where $\bar{E} \in \{\bar{X}, \bar{Z}\}$ (regardless of whether the first $H_m^{f_2}$ measurement outcome was ± 1). During the second $H_m^{f_2}$ measurement, the output state will become

$$|\psi^{(4)}\rangle = \frac{\bar{E} + \tilde{\bar{E}}}{2}|\bar{H}\rangle|+\rangle + \frac{\bar{E} - \tilde{\bar{E}}}{2}|\bar{H}\rangle|-\rangle = |\bar{H}\rangle|+\rangle \pm i|-\bar{H}\rangle|-\rangle \quad (21)$$

From Eq. (21) we conclude that the three $H_m^{f_2}$ measurement outcomes will either be $\pm + +$ with $|\psi_{\text{final}}\rangle = |\bar{H}\rangle$ or $\pm - -$ with $|\psi_{\text{final}}\rangle = |-\bar{H}\rangle$ (in which case we apply \bar{Y}).

4. $E_p = X_i Z_j$ with $i \neq j$.

E_p will be corrected in the next EC round. A similar calculation as the examples above show that the possible measurement outcomes of the three $H_m^{f_2}$ are $+++$, $-++$ and $+-$. If the last two measurements are -1 , then apply \bar{Y} to the data. In all cases (and after applying the necessary logical operations) $|\psi_{\text{final}}\rangle = |\bar{H}\rangle$.

Case 2: fault in the first $H_m^{f_2}$ circuit.

If the fault results in a data-qubit error of weight greater than one, as was shown in Appendix A.3.1, the possible errors can be distinguished when considering the full six-bit syndrome as well as applying $H_1 H_3 H_4$ or I to the data depending on the flag outcomes. Thus the output state of the first $H_m^{f_2}$ measurement can be expressed as $|\psi^{(2)}\rangle = E_f|\bar{H}\rangle|\pm\rangle$ where E_f will be corrected by the following EC. Hence the possible measurement outcomes of the three $H_m^{f_2}$ circuits are $\pm + +$ and the final output state will be $|\psi_{\text{final}}\rangle = |\bar{H}\rangle$.

Case 3: fault in the first EC.

The input state to the EC will be $|\bar{H}\rangle$. If a fault results in a data-qubit error of weight greater than one,

$H_m^{f_2}$ measurement outcomes	Logical gate correction
$+++$	I
$---$	\bar{Y}
$+-$	\bar{Y}
$-++$	I
$+-+$	I
$++-$	I

Table 2: Logical correction to apply at the end of the circuit in Fig. 6b given the three measurement outcomes of the $H_m^{f_2}$ circuit. The comparison between rows three and five of this table shows why three logical Hadamard measurements are required instead of two.

there will be a flag and the error will be corrected. The output of the EC will be $|\bar{H}\rangle$ and all three $H_m^{f_2}$ measurements will be $+1$ with $|\psi_{\text{final}}\rangle = |\bar{H}\rangle$.

If there are no flags, the output state of the EC can be written as $|\psi^{(3)}\rangle = E_p|\bar{H}\rangle$ where $E_p = E_i^{(x)} E_j^{(z)}$. The output state of the second $H_m^{f_2}$ measurement will be given by

$$|\psi^{(4)}\rangle = \frac{E_p + \tilde{E}_p}{2}|\bar{H}\rangle|+\rangle + \frac{E_p - \tilde{E}_p}{2}|\bar{H}\rangle|-\rangle. \quad (22)$$

Note that the error will be corrected in the next EC round. However the type of error can affect the $H_m^{f_2}$ measurement outcomes.

1. $E_p = Y_i$

In this case $|\psi^{(4)}\rangle = Y_i|\bar{H}\rangle|-\rangle$ and the second $H_m^{f_2}$ measurement will be -1 (with all three measurement outcomes being $+-$) and $|\psi_{\text{final}}\rangle = |\bar{H}\rangle$ ⁹.

2. $E_p \in \{X_i, Z_i\}$.

In this case $|\psi^{(4)}\rangle = \frac{X_i + Z_i}{2}|\bar{H}\rangle|+\rangle \pm \frac{X_i - Z_i}{2}|\bar{H}\rangle|-\rangle$. Thus the second $H_m^{f_2}$ measurement will be ± 1 and all three $H_m^{f_2}$ measurements will be $\pm \pm +$ with $|\psi_{\text{final}}\rangle = |\bar{H}\rangle$.

3. $E_p = X_i Z_j$ with $i \neq j$.

The analysis of this case is analogous to the case where $E_p = Y_i$.

Case 4: fault in the second $H_m^{f_2}$ circuit.

The analysis is identical to Case 2. The possible measurement outcomes of the $H_m^{f_2}$ circuits are $\pm \pm +$ with $|\psi_{\text{final}}\rangle = |\bar{H}\rangle$.

⁹This case shows why it is important to measure the logical Hadamard operator three times since if the first two measurement outcomes are $+-$, then the data qubit state can either be $|\bar{H}\rangle$ as in this case or $|-\bar{H}\rangle$ as shown in Case 1 (see the text following Eq. (21)).

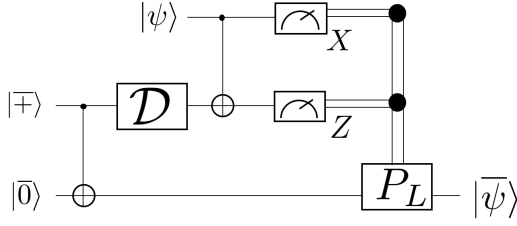


Figure 13: Circuit for teleporting the single-qubit state $|\psi\rangle$ into the codeblock. The operation \mathcal{D} is used to decode one of the code blocks, and P_L is a logical Pauli which is applied to complete the teleportation protocol.

Case 5: fault in the second EC circuit.

The analysis of this case is analogous to Case 3. The possibilities for the three $H_m^{f_2}$ measurement outcomes are $++\pm$ with $|\psi\rangle_{\text{final}} = E_p|\bar{H}\rangle$ where $E_p = E_i^{(x)}E_j^{(z)}$. Note however that E_p is a correctable error so both criteria in Definition 1 are still satisfied.

Case 6: fault in the third $H_m^{f_2}$ circuit.

The analysis is analogous to Case 4. However if there is a flag, an extra EC round should be performed following the third $H_m^{f_2}$ circuit. The three $H_m^{f_2}$ measurement outcomes will be $++\pm$ with $|\psi\rangle_{\text{final}} = E_p|\bar{H}\rangle$ where $E_p = E_i^{(x)}E_j^{(z)}$ as in Case 5.

A summary of the logical operations to apply to $|\psi\rangle_{\text{final}}$ based on the three $H_m^{f_2}$ measurement outcomes is given in Table 2.

B Teleporting into code blocks

In this section we review a general method introduced by Knill for preparing an encoded state $|\bar{\psi}\rangle$ from a physical qubit state $|\psi\rangle$ using teleportation [43].

The circuit used to implement the teleportation protocol is illustrated in Fig. 13. After preparing a logical Bell state, one of the code blocks is decoded. A CNOT is applied between $|\psi\rangle$ and the decoded state. After measuring both qubits in the X and Z basis, a logical Pauli operator is applied to the code block in order to complete the teleportation protocol.

In [44], Aliferis showed that the probability of a logical fault occurring during the teleportation protocol can be bounded by

$$p_L \leq 3p^{(k)} + p_{\text{dec}}^{(k)} + 4p. \quad (23)$$

Here we are assuming that the code block is encoded with k -levels of concatenation. Assuming a stochastic noise model where encoded gates fail with probability at most $p^{(k)}$, a fault in the encoded Bell state is upper bounded by $3p^{(k)}$. Since there are four locations in the physical part of the teleportation circuit, and with

$p^{(0)} = p$, the probability of this part is bounded by $4p$. Lastly, $p_{\text{dec}}^{(k)}$ is a bound on the probability of failure of the decoding circuit \mathcal{D} .

The level- k block is decoded recursively as follows. The level- k circuit comprises level- $(k-1)$ gates which, when applied to the code block, results in a level- $(k-1)$ encoded state. Then \mathcal{D} is applied again using level- $(k-2)$ gates and so on. Assuming that \mathcal{D} has D locations, we can bound $p_{\text{dec}}^{(k)}$ by

$$p_{\text{dec}}^{(k)} \leq D \sum_{j=0}^{k-1} p^{(j)}, \quad (24)$$

where $p^{(j)}$ is a bound on the failure probability of level- j gates.

In this paper, instead of using the bounds in Eqs. (23) and (24), we perform a direct simulation of the teleportation circuit using the methods in Section 2 in order to obtain smaller constant pre-factors (since not all fault locations will lead to a logical fault).

C Overhead analysis of the $|H\rangle$ state preparation scheme

In this section we provide a detailed description of the qubit and gate overhead analysis for preparing an encoded $|H\rangle$ state using our error detection scheme.

C.1 Qubit overhead analysis

We begin with a few definitions. Let $p_A^{H(l)}$ be the probability that an encoded $|H\rangle$ state at level- l passes the verification test of the circuit in Fig. 5b and let $n_T^{H(l)}$ be the total number of qubits used to prepare an encoded $|H\rangle$ state at level- l . At the first concatenation level, the largest component of the circuit in Fig. 5b is the EC, which requires 10 qubits in its implementation. Hence we have

$$\langle n_T^{H(1)}(p) \rangle = \frac{10}{p_A^{H(1)}(p)}, \quad (25)$$

for a physical error rate p of the depolarizing noise model.

At higher levels, a few considerations are necessary when considering different contributions to the qubit overhead. First, for the level- l circuit in Fig. 4, it is important to take into account the fault-tolerant preparation of the level- $(l-1)$ $|0\rangle$ and $|+\rangle$ states. The level- $(l-1)$ $|+\rangle$ state is obtained by first preparing the state $|+^{(l-2)}\rangle^{\otimes 7}$ (which is a $+1$ eigenstate of all the X -stabilizers), followed by measuring the Z -stabilizers

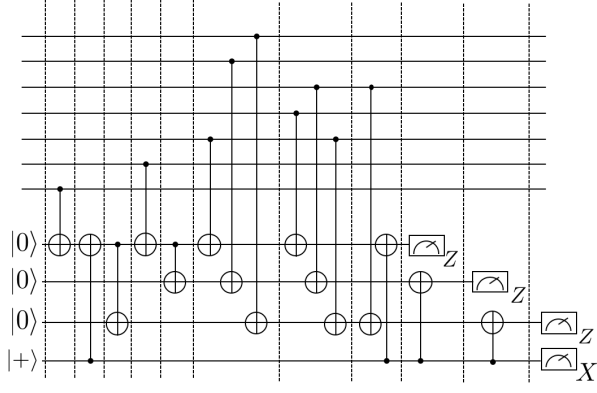


Figure 14: Flag fault-tolerant circuit for measuring the Z stabilizers of the $[[7, 1, 3]]$ Steane code obtained from [21]. The dashed vertical lines are used to separate different time steps.

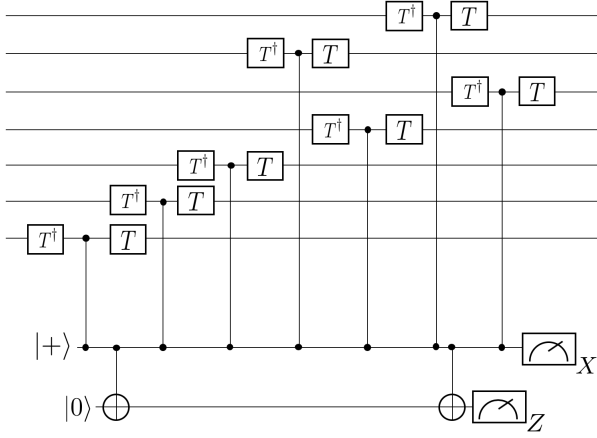


Figure 15: Circuit used to measure the logical Hadamard operator for concatenation levels $l \geq 2$. The T gates are implemented using the circuit in Fig. 1. At level- l , two level- $(l-1)$ $|H\rangle$ resource states are required for the entire circuit. We assume that the two resource states can be reused for each parallel implementation of T and T^\dagger .

using the circuit of Fig. 14 (which was shown to be fault-tolerant in [21]). Depending on the measurement and flag outcomes, it might be necessary to repeat the measurement of X or Z stabilizers without the flag qubit. Note that at the first level, the circuit in Fig. 14 requires 11 qubits instead of 10 since there needs to be at least one ancilla qubit prepared in the $|+\rangle$ state in order to detect errors of weight greater than two arising from a single fault. A similar protocol is used to fault-tolerantly prepare a level- $(l-1)$ $|0\rangle$ state.

Next, the details of the implementation of the controlled-Hadamard gates are considered as follows. Since the controlled-Hadamard gates are decomposed as shown in Fig. 2b with the level- $(l-1)$ T and T^\dagger gates implemented using level- $(l-1)$ $|H\rangle$ states as shown in

Fig. 1, at level $l \geq 2$, the logical Hadamard gate is measured using the circuit in Fig. 15. Due to the way in which we parallelize the the circuit in Fig. 15, only two level- $(l-1)$ resource states are required at each time step, apart from the first and last time step where we only need one resource state. In addition, a level- $(l-1)$ resource state is required for the circuit in Fig. 4.

In order to minimize the qubit overhead, we consider preparing in parallel $m_i^{(1)} \geq 1$ level- $(l-1)$ resource states at a time step where one resource state is required, and $m_i^{(2)} \geq 2$ level- $(l-1)$ resource states at a time step where two resource states are required. At a time step where one level- $(l-1)$ resource state is required, if none of the $m_i^{(1)}$ resource states pass the verification test, the protocol is aborted and begins anew. Similarly, at a time step where two resource states are required, we need at least two of the $m_i^{(2)}$ resource states to pass the verification test, otherwise, the protocol is aborted.

Let $p_{AP1}^{(l)}$ be the probability that at least one of the $m_1^{(l)}$ level- $(l-1)$ $|H\rangle$ states passes the verification test and $p_{AP2}^{(l)}$ be the probability that at least two of the $m_2^{(l)}$ level- $(l-1)$ $|H\rangle$ states pass the verification test. We have that

$$p_{AP1}^{(l)}(p) = \sum_{k=1}^{m_1^{(l)}} \binom{m_1^{(l)}}{k} (p_A^{H(l-1)}(p))^k (1 - p_A^{H(l-1)}(p))^{m_1^{(l)}-k}, \quad (26)$$

and

$$p_{AP2}^{(l)}(p) = \sum_{k=2}^{m_2^{(l)}} \binom{m_2^{(l)}}{k} (p_A^{H(l-1)}(p))^k (1 - p_A^{H(l-1)}(p))^{m_2^{(l)}-k}. \quad (27)$$

At each level, we set the values of $p_{AP1}^{(l)}(p)$ and $p_{AP2}^{(l)}(p)$ from $1 - 10^{-3}$ to $1 - 4 \times 10^{-2}$ in increments of 10^{-2} and obtain the corresponding values of $m_1^{(l)}$ and $m_2^{(l)}$ by solving Eqs. (26) and (27). The final values of $p_{AP1}^{(l)}(p)$ and $p_{AP2}^{(l)}(p)$ chosen to minimize $\langle n_T^{H(l)}(p) \rangle$ (see Eq. (28) below and Table 3). Now, the circuits for preparing level-1 $|0\rangle$ and $|+\rangle$ states require 11 qubits. Additionally, three extra $|0\rangle$ and $|+\rangle$ ancilla states are required, two in the circuit of Fig. 15 and three for the EC (we assume that the ancilla qubit's used to measure the Hadamard operator can be reused for the EC). Apart for the resource state used to prepare the circuit in Fig. 4, the qubits used in the resource states for implementing T and T^\dagger gates can be reused at each time step of the circuit in Fig. 15. Since there are three time steps where a single resource state is required and six

Acceptance probabilities for preparing $m_1^{(l)}$ and $m_2^{(l)}$ resource states
$p_{AP1}^{(2)}(p) \approx 0.999887 - 73.8p$
$p_{AP1}^{(2)}(p) \approx 0.99998 - 149p$
$p_{AP1}^{(2)}(p) \approx 0.999897 - 86.7p - 3.71 \times 10^5 p^2$
$p_{AP1}^{(2)}(p) \approx 0.99994 - 177p - 6.97 \times 10^5 p^2$

Table 3: List of the acceptance probabilities $p_{AP1}^{(l)}(p)$ and $p_{AP2}^{(l)}(p)$ at the second and third concatenation levels. The expressions were obtained by solving Eqs. (26) and (27) numerically for values of $p_{AP1}^{(l)}(p), p_{AP2}^{(l)}(p) \in [1 - 4 \times 10^{-2}, 1 - 10^{-3}]$ increasing in increments of 10^{-2} and choosing the pair of values which minimize the total average qubit overhead $\langle n_T^{H(l)}(p) \rangle$. We round the coefficients of p and p^2 to three digits.

times steps where two resource states are required, the average number of qubits required to implement our error detection scheme at level- l is given by

$$\langle n_T^{H(l)}(p) \rangle = \frac{(\lceil m_1^{(l)} \rceil + 2\lceil m_2^{(l)} \rceil) \langle n_T^{H(l-1)}(p) \rangle + 9(11^{l-1})}{p_A^{H(l)}(p) (p_{AP1}^{(l)}(p))^3 (p_{AP2}^{(l)}(p))^6}. \quad (28)$$

C.2 Gate overhead analysis

Since the circuit in Fig. 5b can be decomposed into three parts, the number of gates required to implement our error detection scheme at level- l can be written as¹⁰

$$n_{|H\rangle}^{(l)} = \frac{n_{H_{\text{nf}}}^{(l)} + n_{H_m^{f_1}}^{(l)} + n_{\text{ED}}^{(l)}}{p_A^{H(l)}(p)}, \quad (29)$$

where $n_{H_{\text{nf}}}^{(l)}$ is the number of gates used for preparing the state $|\overline{H}\rangle_{\text{nf}}$ at level- l , $n_{H_m^{f_1}}^{(l)}$ is the number of gates required to measure the logical Hadamard operator at level- l and $n_{\text{ED}}^{(l)}$ is the number of gates used in the EC circuit of Fig. 3 at level- l . We used ED instead of EC since the circuit is used in an error detection scheme. It will also be important to analyze the gate overhead of the circuit in Fig. 3 when used in an error correction scheme since all level- l ($l \geq 2$) Clifford gates in our circuits consist of extended rectangles where the EC's are used for error correction instead of error detection.

Performing a gate count of the level-1 circuits in Figs. 3, 4 and 15, we find that

¹⁰Note that in this section, all quantities $n_G^{(l)}$ should be written as $\langle n_G^{(l)} \rangle$ since we are computing average quantities. However, to avoid cluttering in the notation, we omit the brackets.

$$n_{H_{\text{nf}}}^{(1)} = 3(n_{|+\rangle}^{(0)} + n_{|0\rangle}^{(0)}) + n_{|H\rangle}^{(0)} + 11n_{\text{CNOT}}^{(0)} + 6n_{\text{idle}}^{(0)}, \quad (30)$$

$$n_{H_m^{f_1}}^{(1)} = 2n_{\text{CNOT}}^{(0)} + 7(n_{\text{CZ}}^{(0)} + n_T^{(0)} + n_{T^\dagger}^{(0)}) + n_{|+\rangle}^{(0)} + n_{|0\rangle}^{(0)} + 191n_{\text{idle}}^{(0)} + n_{X_m}^{(0)} + n_{Z_m}^{(0)}, \quad (31)$$

$$n_{\text{ED}}^{(1)} = n_{\text{EC1}}^{(1)} + \langle n_{\text{ED2}}^{(1)} \rangle n_{\text{EC2}}^{(1)}, \quad (32)$$

and

$$n_{\text{EC}}^{(1)} = \langle n_{\text{REC1}}^{(1)} \rangle n_{\text{EC1}}^{(1)} + \langle n_{\text{REC2}}^{(1)} \rangle n_{\text{EC2}}^{(1)}, \quad (33)$$

where $n_{Z_m}^{(l)} = n_{X_m}^{(l)} = 7^l$ are the number of Z and X -basis measurement locations.

In the above, for a gate $G \notin \{T, T^\dagger\}$, $n_G^{(l)} = 7^l$ since as we will show below, we will treat the EC's separately from the gates for $l \geq 2$. We split the EC circuit into the two components shown in Fig. 3, which we call EC1 and EC2. As we explained in Appendix A.1, depending on the syndrome measurement outcome, the full syndrome measurement can be repeated. Thus $\langle n_{\text{REC1}}^{(l)} \rangle$ and $\langle n_{\text{REC2}}^{(l)} \rangle$ corresponds to the average number of times that the circuits EC1 and EC2 are implemented at level- l . Similarly, $\langle n_{\text{ED2}}^{(l)} \rangle$ is the average number of times that EC2 is implemented when the EC circuit is used for error detection. These values were obtained through Monte-Carlo simulations with 10^6 trials (see Fig. 16).

Performing a gate count of the circuits EC1 and EC2, we have that

$$n_{\text{EC1}}^{(1)} = 46n_{\text{idle}}^{(0)} + 14n_{\text{CNOT}}^{(0)} + 2(n_{|0\rangle}^{(0)} + n_{Z_m}^{(0)}) + n_{|+\rangle}^{(0)} + n_{X_m}^{(0)} \quad (34)$$

and

$$n_{\text{EC2}}^{(1)} = 46n_{\text{idle}}^{(0)} + 14n_{\text{CNOT}}^{(0)} + 2(n_{|+\rangle}^{(0)} + n_{X_m}^{(0)}) + n_{|0\rangle}^{(0)} + n_{Z_m}^{(0)}. \quad (35)$$

Lastly, at concatenation levels $l \geq 2$, the $|0\rangle$ and $|+\rangle$ states are prepared fault-tolerantly using the circuit in Fig. 14 to measure the three Z stabilizers of the Steane code, and a similar circuit to measure the three X stabilizers (see the discussion in Appendix C.1). When preparing a logical $|\overline{+}\rangle$ state, if there is a flag in the circuit of Fig. 14, then there could be a Z error of weight greater than one. Thus one must measure the X stabilizers of the Steane code (without using a flag qubit) to correct the Z errors. If there are no flags but the Z stabilizer measurement outcome is nontrivial, then

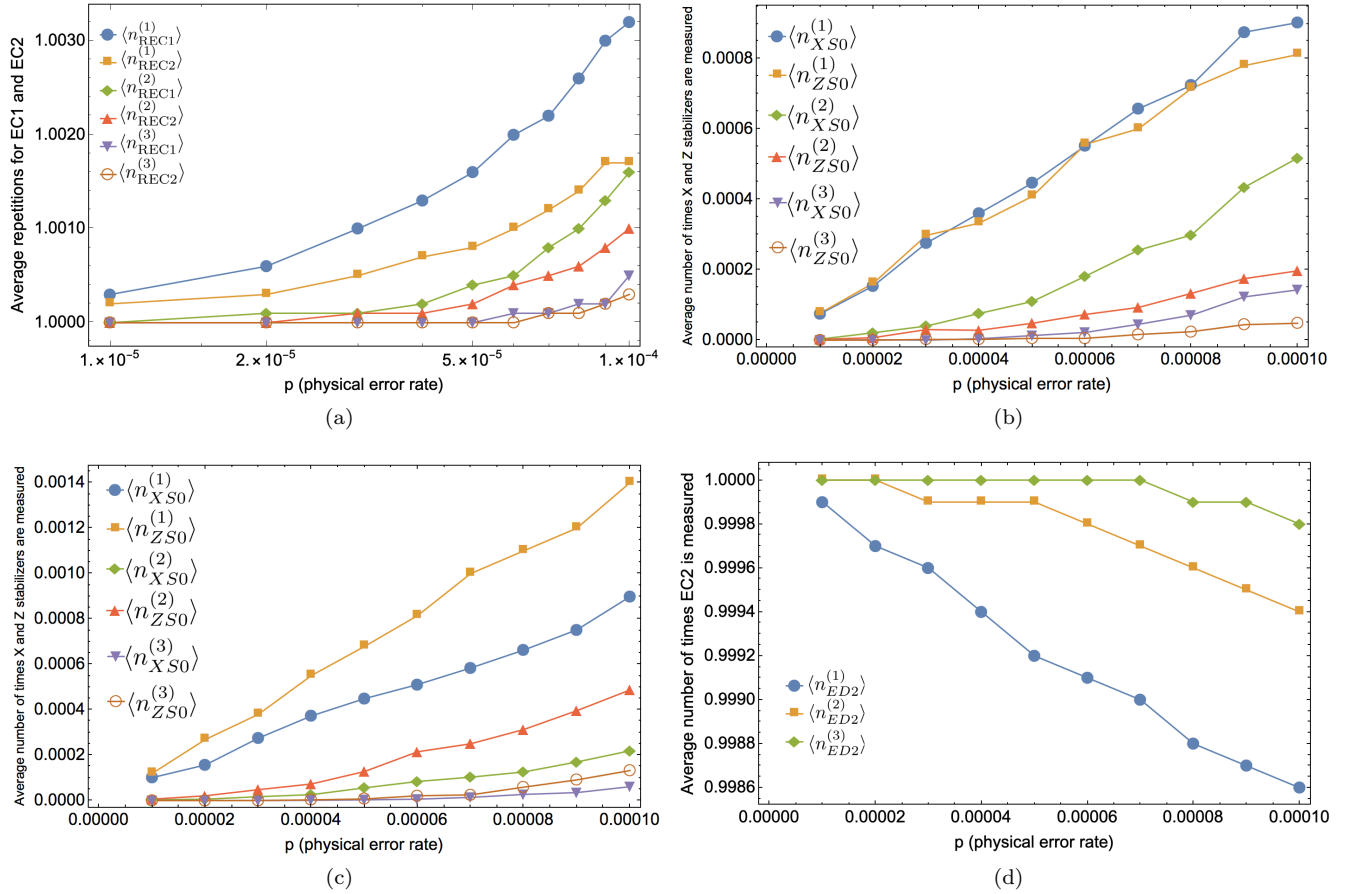


Figure 16: (a) Plot showing the values obtained for $\langle n_{\text{REC1}}^{(l)} \rangle$ and $\langle n_{\text{REC2}}^{(l)} \rangle$ at the first three concatenation levels of the Steane code. (b) Plots showing the values obtained for $\langle n_{X S0}^{(l)} \rangle$ and $\langle n_{Z S0}^{(l)} \rangle$ when preparing the $|0\rangle$ state at the first three concatenation levels. (c) Same as in (b) but for the $|+\rangle$ state. (d) Plot showing the values of $\langle n_{\text{ED2}}^{(l)} \rangle$ at the first three levels. All plots were obtained by performing a Monte-Carlo simulation with 10^6 trials.

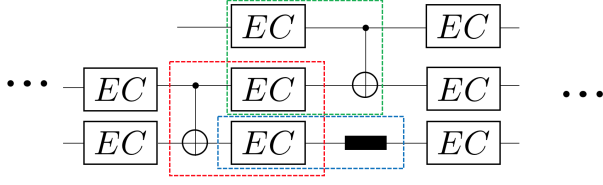


Figure 17: Circuit illustrating shared EC units between two logical CNOT gates and an idle qubit location. It is important not to double-count overlapping EC's when computing the gate overhead at concatenation levels $l \geq 2$.

one must repeat the Z syndrome measurement without the flag qubit. A similar analysis holds for preparing a logical $|\bar{0}\rangle$ state. Hence, as in Eqs. (32) and (33), we must also take into account the average number of times the non-flagged X and Z stabilizers are measured when counting the number of gates required to prepare level- l $|0\rangle$ and $|+\rangle$ states. The averages are obtained by performing a Monte-Carlo simulation (see Fig. 16). In what follows we define $n_{XS}^{(l)}$ and $n_{ZS}^{(l)}$ to be the number of locations in the level- l X and Z stabilizer measurement circuit without the flag qubits and $\langle n_{XS+|0}^{(l)} \rangle$ and $\langle n_{ZS+|0}^{(l)} \rangle$ to be the average number of times these circuits are used when preparing a level- l $|+ / 0\rangle$ state. Performing the level-1 gate count, we have that

$$n_{|+\rangle}^{(1)} = 73n_{\text{idle}}^{(0)} + 15n_{\text{CNOT}}^{(0)} + 8n_{|+\rangle}^{(0)} + 3(n_{|0\rangle}^{(0)} + n_{Zm}^{(0)}) + n_{Xm}^{(0)} + \langle n_{ZS+}^{(1)} \rangle n_{ZS}^{(1)} + \langle n_{XS+}^{(1)} \rangle n_{XS}^{(1)}, \quad (36)$$

and

$$n_{|0\rangle}^{(1)} = 73n_{\text{idle}}^{(0)} + 15n_{\text{CNOT}}^{(0)} + 8n_{|0\rangle}^{(0)} + 3(n_{|+\rangle}^{(0)} + n_{Xm}^{(0)}) + n_{Zm}^{(0)} + \langle n_{ZS0}^{(1)} \rangle n_{ZS}^{(1)} + \langle n_{XS0}^{(1)} \rangle n_{XS}^{(1)}, \quad (37)$$

with

$$n_{ZS}^{(1)} = 48n_{\text{idle}}^{(0)} + 11n_{\text{CNOT}}^{(0)} + 3(n_{|0\rangle}^{(0)} + n_{Zm}^{(0)}), \quad (38)$$

and

$$n_{XS}^{(1)} = 48n_{\text{idle}}^{(0)} + 11n_{\text{CNOT}}^{(0)} + 3(n_{|+\rangle}^{(0)} + n_{Xm}^{(0)}). \quad (39)$$

We now have all the tools to obtain the gate overhead at arbitrary concatenation levels. Recall that at concatenation levels $l \geq 2$, all physical gates G in the circuits of Fig. 5b are represented by extended rectangles, which consists of the logical gate G preceded and followed by EC units (in our case, the circuit in Fig. 3). More details on extended rectangles can be found in [30]. When computing the gate overhead of the error detection scheme (Eq. (29) with $l \geq 2$), we

must be careful not to double-count overlapping EC's since consecutive gates will share an EC (see Fig. 17 for an example).

Lastly, for $l \geq 2$, the T and T^\dagger gates are implemented as shown in Fig. 1. We thus see that the overhead for these gates can be computed recursively using

$$n_T^{(l)} = n_{T^\dagger}^{(l)} = n_{|H\rangle}^{(l-1)} + 3n_{\text{EC}}^{(l-1)} + 4(7^l). \quad (40)$$

With the above considerations and using Eq. (40), the gate overhead can be computed recursively using the following relations. First, the recursive relations for the EC unit are given by

$$n_{\text{EC}}^{(l)} = \langle n_{\text{REC1}}^{(l)} \rangle n_{\text{EC1}}^{(l)} + \langle n_{\text{REC2}}^{(l)} \rangle n_{\text{EC2}}^{(l)}, \quad (41)$$

where

$$n_{\text{EC1}}^{(l)} = 2n_{|0\rangle}^{(l-1)} + n_{|+\rangle}^{(l-1)} + 73n_{\text{EC}}^{(l-1)} + 63(7^l), \quad (42)$$

and

$$n_{\text{EC2}}^{(l)} = 2n_{|+\rangle}^{(l-1)} + n_{|0\rangle}^{(l-1)} + 66n_{\text{EC}}^{(l-1)} + 63(7^l). \quad (43)$$

Next, the recursive relations for the $|0\rangle$ and $|+\rangle$ states are

$$n_{|0\rangle}^{(l)} = 8n_{|0\rangle}^{(l-1)} + 3n_{|+\rangle}^{(l-1)} + 100n_{\text{EC}}^{(l-1)} + 92(7^l) + \langle n_{ZS0}^{(l)} \rangle n_{ZS}^{(l)} + \langle n_{XS0}^{(l)} \rangle n_{XS}^{(l)}, \quad (44)$$

$$n_{|+\rangle}^{(l)} = 8n_{|+\rangle}^{(l-1)} + 3n_{|0\rangle}^{(l-1)} + 100n_{\text{EC}}^{(l-1)} + 92(7^l) + \langle n_{ZS+}^{(l)} \rangle n_{ZS}^{(l)} + \langle n_{XS+}^{(l)} \rangle n_{XS}^{(l)}, \quad (45)$$

where

$$n_{ZS}^{(l)} = 3n_{|0\rangle}^{(l-1)} + 62(7^l) + 70n_{\text{EC}}^{(l-1)}, \quad (46)$$

and

$$n_{XS}^{(l)} = 3n_{|+\rangle}^{(l-1)} + 62(7^l) + 70n_{\text{EC}}^{(l-1)}. \quad (47)$$

Using Eqs. (41) to (47) and the results in Fig. 16, we can compute the following expressions

$$n_{H_{\text{nf}}}^{(l)} = 3(n_{|+\rangle}^{(l-1)} + n_{|0\rangle}^{(l-1)}) + n_{|H\rangle}^{(l-1)} + 28n_{\text{EC}}^{(l-1)} + 17(7^{l-1}), \quad (48)$$

$$n_{H_m^{f1}}^{(l)} = n_{|+\rangle}^{(l-1)} + n_{|0\rangle}^{(l-1)} + 202(7^l) + 14n_T^{(l)} + 129n_{\text{EC}}^{(l-1)}, \quad (49)$$

and

$$n_{\text{ED}}^{(l)} = n_{\text{EC1}}^{(l)} + \langle n_{\text{ED2}}^{(l)} \rangle n_{\text{EC2}}^{(l)}. \quad (50)$$

Note that $n_{\text{EC}}^0 = 0$ and $n_T^0 = n_{T^\dagger}^0 = n_{|H\rangle}^0 = n_{|0\rangle}^0 = n_{|+\rangle}^0 = 1$.

D Overhead analysis for the MEK scheme

In this section we provide a detailed description of the qubit and gate overhead analysis required to implement the MEK scheme.

D.1 Qubit overhead analysis

We first compute the overhead cost of teleporting a physical $|H\rangle$ state to a level-2 $|H\rangle$ state and then performing one round of level-2 MEK.

Let $n_{qij}^{(T)}$ be the qubit overhead cost of a level- i $|H\rangle$ state teleported to a level- j $|H\rangle$ state. From the teleportation of Fig. 13, a level-2 $|0\rangle$ and $|+\rangle$ state must be prepared, each requiring 11^2 qubits. We assume that these qubits can be reused when performing the logical gates and EC's that follow (since an EC requires only 10 qubits). Including the qubit for the physical $|H\rangle$ state, we have

$$n_{q02}^{(T)} = 2(11^2) + 1 = 243. \quad (51)$$

Next we define $n_{qMEK}^{(l)}$ to be the qubit overhead cost associated with performing a level- l round of MEK. We also define $a_{MEK}^{(l)}$ to be the probability that a pair of level- l $|H\rangle$ states are accepted in a level- l round of MEK. When implementing a level- l MEK circuit, we must prepare two level- l $|+\rangle$ states and one level- l $|0\rangle$ state. As was explained in Appendix C.1, we require two additional level- l $|H\rangle$ states in order to perform the C_H gates. Thus the level-2 MEK circuit qubit overhead with level-2 $|H\rangle$ states teleported from physical $|H\rangle$ states is given by

$$n_{qMEK}^{(2)}(p) = \frac{3(11^2) + 4(243)}{a_{MEK}^{(2)}(p)} = \frac{1335}{a_{MEK}^{(2)}(p)}. \quad (52)$$

Since the MEK circuit produces two distilled $|H\rangle$ states, when we compare the qubit overhead cost to our $|H\rangle$ state preparation error detection scheme, we will divide Eq. (52) by two. We note that several additional optimizations are possible. For instance, some of the qubits used for teleporting the $|H\rangle$ states that are used to perform the C_H gates could be reused. Additionally, the extra qubits used for preparing the level- l $|0\rangle$ and $|+\rangle$ states for the MEK circuit could also be reused in various parts of the protocol. However these additional optimizations are likely to strongly depend on the particular architecture that is being used and their associated constraints. Therefore, to be as general as possible, these will be omitted.

We now consider the overhead cost for performing a round of level-3 MEK. We first teleport the distilled level-2 $|H\rangle$ states to level-3 $|H\rangle$ states. We have that

$$\begin{aligned} n_{q23}^{(T)}(p) &= 2(11^3) + \frac{n_{qMEK}^{(2)}(p)}{2} \\ &= 2662 + \frac{1335}{2a_{MEK}^{(2)}(p)}. \end{aligned} \quad (53)$$

Using the level-3 $|H\rangle$ states, the qubit overhead for a level-3 MEK simulation is given by

$$n_{qMEK}^{(3)}(p) = \frac{3(11^3) + 4n_{q23}^{(T)}(p)}{a_{MEK}^{(3)}(p)}, \quad (54)$$

where we will divide Eq. (54) by two when comparing with the qubit overhead of our error detection scheme.

For the case when a level-2 $|H\rangle$ state is prepared using our error detection scheme, we must first teleport the level-2 $|H\rangle$ state to a level-3 $|H\rangle$ state. Defining $n_{2ED3}^{(T)}$ to be the overhead cost for the teleportation step, we have

$$n_{2ED3}^{(T)}(p) = 2(11^3) + \langle n_T^{H(2)}(p) \rangle, \quad (55)$$

where $\langle n_T^{H(2)}(p) \rangle$ is obtained from Eq. (28). Hence the overhead cost for performing a round of level-3 MEK is given by

$$n_{qMEKED}^{(3)}(p) = \frac{3(11^3) + 4n_{2ED3}^{(T)}(p)}{2a_{MEKED}^{(3)}(p)}, \quad (56)$$

where $a_{MEKED}^{(3)}$ is the acceptance probability for the level-3 MEK scheme when the level-2 $|H\rangle$ states (teleported to level-3) were obtained from our error detection scheme.

D.2 Gate overhead analysis

We now consider the gate overhead analysis for the various rounds of MEK considered in Appendix D.1.

Let $n_{gij}^{(T)}$ be the qubit overhead cost of a level- i $|H\rangle$ state teleported to a level- j $|H\rangle$ state. Two EC's must be performed after applying the logical CNOT gate. We must also take into account the gate cost for the decoding circuit. The decoding circuit requires the preparation of four $|+\rangle$ states and three $|0\rangle$ states. There are eight CNOT gates and the circuit requires a total of 16 EC's. Let $n_{ij}^{(D)}$ be the number of gates in the decoding circuit for level- i to level- j teleportation scheme. We have that

$$n_{02}^{(D)} = 4(n_{|+\rangle}^{(2)} + n_{|+\rangle}^{(1)}) + 3(n_{|0\rangle}^{(2)} + n_{|0\rangle}^{(1)}) + 16(n_{\text{EC}}^{(1)} + n_{\text{EC}}^{(2)}) + 8(7^2 + 7), \quad (57)$$

where $n_{\text{EC}}^{(l)}$, $n_{|0\rangle}^{(l)}$ and $n_{|+\rangle}^{(l)}$ are given by Eqs. (41), (44) and (45). We then have

$$n_{gij}^{(T)} = n_{|+\rangle}^{(2)} + n_{|0\rangle}^{(2)} + 2n_{\text{EC}}^{(2)} + n_{02}^{(D)} + 7^2 + 4. \quad (58)$$

The last term in Eq. (58) is due to the four physical operations of the decoding circuit.

Next we compute the gate overhead of the level-2 MEK scheme. The circuit has 48 logical gates, 177 EC's and requires the preparation of two level-2 $|+\rangle$ states and one level-2 $|0\rangle$ state. Defining $n_{\text{gMEK}}^{(l)}$ to be the gate overhead of a level- l MEK circuit, we have

$$n_{\text{gMEK}}^{(2)} = \frac{4n_{g02}^{(T)} + 2n_{|+\rangle}^{(2)} + n_{|0\rangle}^{(2)} + 48(7^2) + 177n_{\text{EC}}^{(2)}}{a_{\text{MEK}}^{(2)}(p)}. \quad (59)$$

Again when comparing the gate overhead of a level-2 MEK circuit to the gate overhead required to prepare a level-2 $|H\rangle$ state using our error detection scheme, we will divide Eq. (59) since an MEK circuit produces two distilled $|H\rangle$ states.

Following the same steps that lead to Eq. (59), it is straightforward to compute the gate overhead for a level-3 MEK circuit. Using

$$n_{23}^{(D)} = 4n_{|+\rangle}^{(3)} + 3n_{|0\rangle}^{(3)} + 16n_{\text{EC}}^{(3)} + 8(7^3), \quad (60)$$

and

$$n_{g23}^{(T)} = n_{|+\rangle}^{(3)} + n_{|0\rangle}^{(3)} + 2n_{\text{EC}}^{(3)} + 3n_{\text{EC}}^{(2)} + 7^3 + 7^2 + n_{23}^{(D)} + \frac{n_{\text{gMEK}}^{(2)}}{2}, \quad (61)$$

we get

$$n_{\text{gMEK}}^{(3)} = \frac{4n_{g23}^{(T)} + 2n_{|+\rangle}^{(3)} + n_{|0\rangle}^{(3)} + 48(7^3) + 177n_{\text{EC}}^{(3)}}{a_{\text{MEK}}^{(3)}(p)}. \quad (62)$$

The gate overhead for a level-3 MEK scheme where a level-2 $|H\rangle$ state was prepared from our error detection scheme is obtained as follows. First we compute the gate overhead to teleport the level-2 $|H\rangle$ state to a level-3 $|H\rangle$ state. It is given by

$$n_{g23\text{ED}}^{(T)}(p) = n_{|H\rangle}^{(2)} + n_{|+\rangle}^{(3)} + n_{|0\rangle}^{(3)} + 2n_{\text{EC}}^{(3)} + 3n_{\text{EC}}^{(2)} + 7^3 + 7^2 + n_{23}^{(D)}, \quad (63)$$

where $n_{|H\rangle}^{(2)}$ is obtained from Eq. (29). Using Eq. (63) we obtain

$$n_{\text{gMEKED}}^{(3)} = \frac{4n_{g23\text{ED}}^{(T)}(p) + 2n_{|+\rangle}^{(3)} + n_{|0\rangle}^{(3)} + 48(7^3) + 177n_{\text{EC}}^{(3)}}{a_{\text{MEKED}}^{(3)}(p)}, \quad (64)$$

where $a_{\text{MEKED}}^{(3)}$ is the acceptance probability of the level-3 MEK circuit when the level-2 $|H\rangle$ states (teleported to level-3) are obtained from our error detection scheme.

E State vector simulations

Here we describe how we simulate each $|H\rangle$ state preparation and MEK magic state distillation circuit. A common method for simulating fault-tolerant error-correction is to apply the Gottesman-Knill theorem to track how Pauli errors propagate through stabilizer circuits. However, unlike error-correction, circuits for magic state preparation and distillation contain non-Clifford gates that map Pauli errors outside the Pauli group, complicating the analysis. Since all of the circuits we consider act on relatively few qubits, we use the Qiskit state vector simulation [45] to accurately track error propagation through non-Clifford gates.

Each gate, preparation, idle and measurement location is subject to Pauli channel errors whose probabilities are functions of the physical error rate p that are determined by the noise model at level-1 and the logical error probabilities of fault-tolerant gates at level-2 and above (see Section 2). For each value of p , we run between 10^6 and 10^8 Monte-Carlo samples, where each sample draws an error at each fault location. The circuits are composed with an ideal decoder so that the output state is one or two physical qubits for state preparation or distillation, respectively. The output for each sample i is a pure state vector $|\psi_i\rangle$ and a measurement record m_i on which we post-select.

For simulations of $|H\rangle$ state preparation, we compute overlaps $\langle\psi_i|P|\psi_i\rangle$ for each Pauli P to determine the logical error class, since in this case the logical error is always of this form after ideal decoding. However, for the MEK distillation protocol there are additional failure modes. For example, the two output qubits can be in a maximally entangled state. This can be seen by placing Y errors on the fourth and seventh $|H\rangle$ states, which corresponds to failures of the first T gate and

third T^\dagger gate. Therefore, we solve for Pauli channel parameters using an estimate of the output density matrix $\tilde{\rho} \approx \sum_i |\psi_i\rangle\langle\psi_i|$. First, we compute the reduced state $\rho = \text{Tr}_2 \tilde{\rho}$ of one output qubit. Next, we model the output state as a Pauli channel applied to the state $\rho_H = |H\rangle\langle H|$,

$$\mathcal{E}(\rho_H) = (1 - p_x - p_z)\rho_H + p_x X \rho_H X + p_z Z \rho_H Z \quad (65)$$

$$= \frac{1}{2\sqrt{2}} \begin{pmatrix} 1 + \sqrt{2} - 2p_x & 1 - 2p_z \\ 1 - 2p_z & -1 + \sqrt{2} + 2p_x \end{pmatrix}. \quad (66)$$

For the parameter ranges we considered, we can solve for the Pauli channel parameters in terms of the matrix elements of ρ ,

$$p_x = \frac{1 + \sqrt{2} - 2\sqrt{2}\rho_{00}}{2} \quad (67)$$

$$p_z = \frac{1 - 2\sqrt{2}\rho_{01}}{2}. \quad (68)$$

We substitute these parameters back into the model and verify the density matrices are equal to machine precision.

The logical error probabilities and rejection probabilities are fit to functions of the physical error p . State preparation results are summarized in Table 4 and distillation results in Table 5. For the second round of distillation, the $\mathcal{O}(p^4)$ contribution to the logical error is too small to observe with 10^8 Monte-Carlo trials, so we do two such simulations. The first case uses ideal $|H\rangle$ states and noisy stabilizer operations, while the second case uses noisy $|H\rangle$ states and ideal stabilizer operations. We simulate the second case at higher physical error rates to estimate the coefficient of the $\mathcal{O}(p^4)$ term. Finally, we approximate the logical error rate and acceptance probability of the noisy circuit as a piecewise function (see the caption of Table 5).

Concatenation	Pr[accept]	Pr[mal _E ^(l) G, p]
$l = 1$	$(1 - p)^{75}$	$(9.95, 4.41, 7.87)p^2$
$l = 2$	$(1 - 3000p^2)^{200}$	$(1.26, 0.0627, 1.09) \times 10^9 p^4$
$l = 2^*$	$1 - 3.67p - 2.67 \times 10^3 p^2$	$(5.14, 0.33, 2.26) \times 10^4 p^4$
$l = 3$	$1 - 84.3p + 1.60 \times 10^6 p^2 - 9.41 \times 10^9 p^3$	$(1.23, 0.0555, 1.16) \times 10^{24} p^8$
$l = 3^*$	$1 - 84.3p + 1.60 \times 10^6 p^2 - 9.41 \times 10^9 p^3$	$(1.24, 0.0683, 1.17) \times 10^{24} p^8$

Table 4: State vector simulation results for $|H\rangle$ state preparation circuits using error-detection. The error probabilities (p_x, p_y, p_z) are given as functions of p for each error type $E \in \{X, Y, Z\}$. The entries marked with (*) use error-detection circuits for level-1 stabilizer operations (only in the $|H\rangle$ state preparation circuit). The acceptance probabilities are for the level- l circuit and do not include rejections at lower levels of concatenation. The expressions are all approximations computed using a standard non-linear fitting method, and coefficients are rounded to three digits. The level-3 expressions are valid for $p \leq 4 \times 10^{-4}$. We notice that both level-3 error polynomials are similar. This is due to the fact that errors arising from the level-2 $|H\rangle$ states have a much smaller contribution to the overall logical error rate compared to the Clifford operations.

Circuit	Pr[accept]	Pr[mal _E ^(l) G, p]
hybrid, $l = 3$	$1 - 3.45 \times 10^{20} p^6$	$(0.812, 1.68) \times 10^{26} p^8$
round-1, $l = 2$	$1 - 32.2p + 2.24 \times 10^4 p^2 - 2.37 \times 10^9 p^3$	$(150, 152)p^2 + (1.01, 2.00) \times 10^{11} p^4$
round-2, $l = 3$, ideal $ H\rangle$	$1 - 6.50 \times 10^{27} p^8$	$(1.43, 2.43) \times 10^{26} p^8$
round-2, $l = 3$, ideal stabilizer*	$1 - 1.47 \times 10^3 p^2$	$(1.97, 1.84) \times 10^5 p^4$
round-3, $l = 3$	$1 - 8.00 \times 10^{27} p^8$	$(2.00, 3.04) \times 10^{26} p^8$

Table 5: State vector simulation results for Meier-Eastin-Knill distillation circuits. The error probabilities (p_x, p_z) are given as functions of p for each error type $E \in \{X, Z\}$. The expressions are all approximations computed using a standard non-linear fitting method, and coefficients are rounded to three digits. The expressions are valid for $p \leq 2 \times 10^{-4}$, except for (*) which is valid for $p \leq 5 \times 10^{-3}$. For round-2, we combine the two results in the table into the following optimistic piecewise approximation: $\text{Pr}[\text{accept}] \approx 1 - \max(1.47 \times 10^3 p^2, 6.50 \times 10^{27} p^8)$ and $\text{Pr}[\text{mal}_E^{(l)}|G, p] \approx (1.97, 1.84) \times 10^5 p^4 + (1.43, 2.43) \times 10^{26} p^8$.