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Mitigation of The Influence of Parasitic Elements in Wide-Bandgap Power Converters

Mitigation of The Influence of Parasitic Elements in Wide-Bandgap Power Converters

By

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Abstract

This work undertakes a detailed investigation of the Mitigation of The Influence of Parasitic Elements in Wide-Bandgap Power Converters. It primarily considers techniques applied to Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in low voltage (<600 V) power converters.

It is shown that parasitic circuit elements have a broad range of negative impacts on the performance of Wide Band Gap (wide band gap) power converters. Analysis of an experimental set-up is performed to create an accurate simulation model which is then validated against experimental results. A parametric analysis of the parasitic Printed Circuit Board (PCB) elements is performed highlighting the sensitivity of the converter's performance to these.

State-of-the-art techniques for mitigating the influence of the parasitic elements are reviewed and a method for incorporating a small inductor into the converter output for mitigation of the load parasitics is proposed.

Considerable analysis is dedicated to the identification of the temporal source of frequency domain characteristics of power converter waveforms. The technique of successive differentials is demonstrated as a tool for analysing time domain waveforms and identifying key noise generating features.

The largest portion of this work proposes smoothed waveform transitions as an important technique in the mitigation of the influence of the parasitic elements of the converter. They are first defined, and a range of analytical tools considered. Following this they are shown to be able to provide significant performance improvements in terms of the interactions with parasitic elements of the converter.

Finally, methods for the practical realisation of waveform smoothing are explored, showing that the predicted performance improvements can be realised. Additional work is performed on the creation of gate drive systems with low complexity that realise the suggested performance improvements.

Dedicated to my parents and Meg

ACKNOWLEDGEMENTS

I would like to thank my primary supervisor Prof. Xibo Yuan for his continuing support throughout not only my PhD, but also my masters project. The technical discussion and focus on new areas of research has helped to shape my work into what it is now. I would also like to thank my secondary supervisors for their academic support.

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AUTHOR'S DECLARATION

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

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Glossary

Bandpower	A measure of the power contained within a specific frequency band of a signal
Co-device	In a phase leg of a converter made up of two devices the co-device refers the the other device in the leg
DC-link	The converters connection to a DC voltage supply
Galvanic isolation	A design technique that allows the transfer of signals but not current between two points by removing any direct conduction path
LCR meter	A device for measuring inductance, capacitance and resistance
Op-amp	Operational Amplifier
Scattering parameter	Parameters describing the behaviour of an electrical network under a steady state excitation (S-parameter)
Switching frequency	A measure of the frequency at which the switching transients occur
Switching loss	The energy that is dissipated during the turn-on or turn-off transient due to the device operating in the linear region

Switching speed	The switching speed (switching rate/switching time/transition time) refers to how fast the switching device transitions between the on and off states

List of Acronyms

AC	Alternating Current
AGC	Active Gate Control
ASIC	Application Specific Integrated Circuit
AWG	Arbitrary Waveform Generator
BJT	Bipolar Junction Transistor
CDCM	Continuous Derivative Control Method
CM	Common Mode
CMRR	Common Mode Rejection Ratio
CWT	Continuous Wavelet Transform
DC	Direct Current
DFT	Discrete Fourier Transform
DPT	Double Pulse Test
DUT	Device Under Test
EM	Electromagnetic
EMC	Electromagnetic Compliance
EMI	Electromagnetic Interference
EPC	Equivalent Parallel Capacitance
ESR	Equivalent Series Resistance
FEA	Finite Element Analysis
FFT	Fast Fourier Transform
FT	Fourier Transform
GaN	Gallium Nitride
GUI	Graphical User Interface

IGBT	Insulated-Gate Bipolar Transistor
JFET	Junction gate Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPS	Merged-PIN-Schottky diode
PCB	Printed Circuit Board
RRC	Reverse Recovery Current
SBD	Schottky Barrier Diode
Si	Silicon
SiC	Silicon Carbide
STFT	Short-Time Fourier Transform
VNA	Vector Network Analyser
wide band gap	Wide Band Gap
WT	Wavelet Transform

List of Functions

Dirac	The Dirac delta function
sinc()	$sinc(x) = \frac{sin(x)}{x}$

List of Symbols

C_{DS}	MOSFET output capacitance (equivalent to C_{OSS})
C_{OSS}	MOSFET output capacitance
C_{pp}	PCB pad-to-pad capacitance
D	Smoothness of a waveform
dI/dt	Rate of change of current
dV/dt	Rate of change of voltage
ϵ_{crit}	Material critical field strength
E_g	Band gap

μ	Electron mobility
I_D	MOSFET drain current
j	The square root of -1
ε_r	Relative permittivity
s	Complex frequency as used with the Laplace transform
V_{DS}	MOSFET drain source voltage
V_{GS}	MOSFET gate source voltage

MEMORANDUM

The accompanying thesis "Mitigation of The Influence of Parasitic Elements in Wide-Bandgap Power Converters" is based on work carried out by the author in the Department of Electrical and Electronic Engineering of the University of Bristol.

The main contributions claimed by the author are as follows:

- Development of a highly accurate simulation model for SiC MOSFETs based in the free-to-use LTspice simulation package
- A technique for designing an inductor for the purpose of mitigating the influence of the load capacitance on the converter performance
- A technique for analysing experimentally obtained power converter waveforms using exemplary waveform shapes for comparison to identify the temporal source of frequency domain characteristics
- A demonstration of a metric that can be effectively used to quantify both the smoothness and Electromagnetic Interference (EMI) generation capability of experimentally obtained waveforms
- A demonstration that the use of smoothed waveforms can mitigate the influence of many parasitic elements of a power converter
- A design of a predominantly passive waveform profiling gate drive circuit capable of achieving some of the advantages of a fully active linear gate driver with far lower complexity and cost

This research has resulted in, or contributed to, the following publications:

Conference Papers

- S. Walder and X. Yuan, "Effect of load parasitics on the losses and ringing in high switching speed SiC MOSFET based power converters," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 6161-6168.
- A. Charalambous, X. Yuan, N. McNeill, S. Walder, Q. Yan and C. Frederickson, "Controlling the output voltage frequency response of the auxiliary commutated pole inverter," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 3305-3310.
- S. Walder, X. Yuan, I. Laird and J. J. O. Dalton, "Identification of the temporal source of frequency domain characteristics of SiC MOSFET based power converter waveforms," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-8.
- S. Walder, X. Yuan, "Waveform Profiling as a Tool for Suppressing the Influence of Parasitic Elements," *9th International Conference on Power Electronics, Machines and Drives (PEMD 2018),* Manchester, 2018
- S. Walder, X. Yuan, Q. Yan,"SiC MOSFET Switching Waveform Profiling Through Passive Networks," *44th Annual Conference of IEEE Industrial Electronics Society, 2018. IECON 2018,* [in press, accepted: 18th July 2018].

CHAPTER 1

INTRODUCTION

This thesis describes the motivation for, approach to, and results of, the body of research undertaken by the author between 2014 and 2018. The work, under the title "Mitigation of The Influence of Parasitic Elements in Wide-Bandgap Power Converters" considers the influence of parasitic circuit elements on the performance of a power converter, and explores techniques for mitigating these effects.

1.1 Background

1.1.1 Power Conversion

In electronics, "power converter" refers to any circuit or system which transforms electrical energy from one form to another. Typical examples of power converter functions are conversion from Alternating Current (AC) to Direct Current (DC), changing voltage, or changing current. Historically, many power conversion applications have been achieved using passive systems - transformers for change in AC voltage and resistive voltage divides for DC voltage reduction. More recently, active circuits have been employed for these conversion applications.

Power converters are used in a huge range of applications; they are found in distribution grids, industrial drives, traction applications, and consumer applications to name a few. They

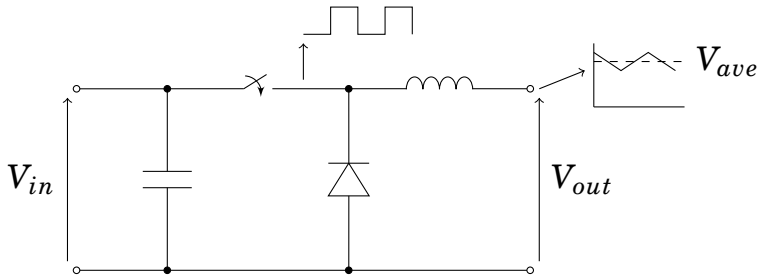

Figure 1.1: Model of a basic (Buck) power converter

handle the transfer of electrical power from milliwatts to megawatts and are critical to many technologies. With power converters handling so much electrical energy, their efficiency is extremely important - in many applications they reduce the power consumption significantly. Power converters are essential for integrating low carbon generation technologies into the grid and for ensuring that electrical energy is used efficiently.

Previously, power conversion has relied on transistors operating in their linear region - these would dissipate energy as they reduced the voltage to the required level. More modern power converters are of the switched-mode type. In these converters the fundamental operating principle is to reduce a voltage by turning on and off a supply at high frequency - this produces a rectangular voltage waveform which is then averaged. Figure 1.1 illustrates a basic switching mode converter - the switch creates a rectangular waveform, which is then averaged by the inductor and diode arrangement. The output voltage can then be regulated by varying the ratio of time the switch is on, or off.

Switched-mode converters achieve very high efficiencies and power densities. This is because the transistor implementing the switching device is operated in either the blocking state (off) or the conducting state (on) and only transiently in the linear region. With modern transistors having very high off-state resistance and low on-state resistance, most of the remaining loss is from the time spent transitioning between states. These very low losses have other system level benefits such as reduced heatsink volume, and reduced converter size. Operating the switch at high frequency also benefits the power density, as the size of the passive elements in the system can be greatly reduced.

A common switched-mode converter design is that of the three-phase inverter. In this design

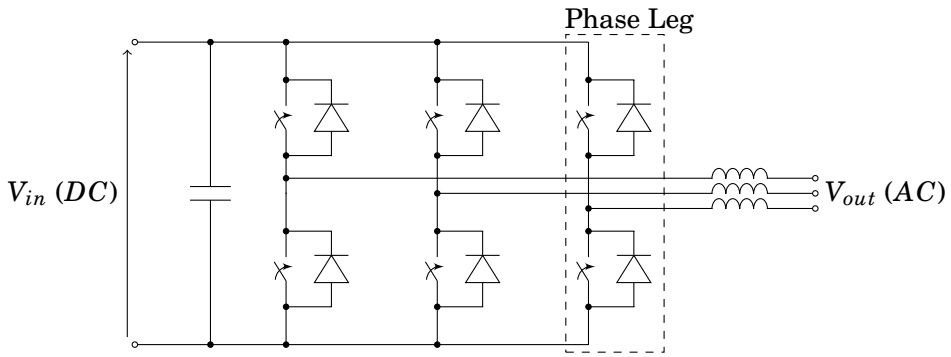

Figure 1.2: Model of a three phase converter

DC is switched so as to produce three phases of AC. This is a common converter as the DC supply can be created from rectified mains, and the output voltage and frequency can be varied, making it an ideal topology for driving an AC motor. Each phase is created using two switching devices, as this allows for current to be returned into the phase through the lower of the two devices. An example of such a converter is illustrated in fig. 1.2. As this is such a common converter topology, a single 'phase leg' (as labelled) of it will be used as the test circuit in this work.

1.1.2 Switching Devices

The circuits in figs. 1.1 and 1.2 have been illustrated using an ideal switch. In reality this is not a practical component to use and a semiconductor device will be used to implement this. With a view for maximising the efficiency, this semiconductor device should be like the perfect switch in that it should have an infinite off-state resistance, and zero on-state resistance. It should also be able to transition between these states instantaneously - though later this will be found not to be ideal from the perspective of EMI generation.

Presently there is a large range of semiconductor devices that could be used to implement the switching cell. These include:

- The MOSFET
- The Bipolar Junction Transistor (BJT)
- The Insulated-Gate Bipolar Transistor (IGBT)
- Thyristors

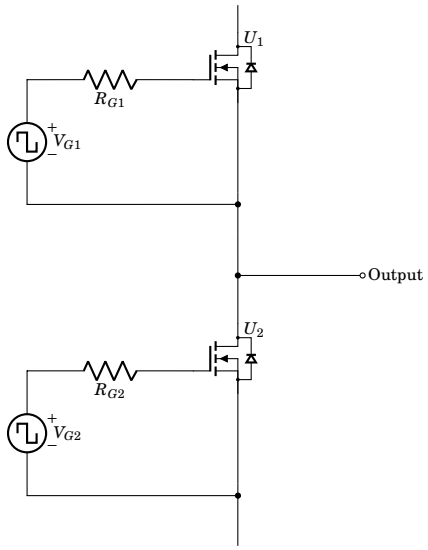

Figure 1.3: Illustration of the position of gate drivers in a typical half bridge

Each of these devices can be sourced in a variety of ratings, and more recently, many of these devices have also been produced in Wide Band Gap materials - a technology which is discussed in detail in section 2.1.

To operate these devices requires the application of a control signal. In the case of MOSFETs and IGBTs the gate terminal of the device is insulated from the conducting terminals - allowing control through application of a voltage signal. In the case of the other devices, control must be realised through application of a small current to the base terminal of the device.

Figure 1.3 illustrates the connection of a gate drive to each of the devices in a typical half bridge of a power converter. In this application an isolated DC supply is required to power the top device's gate driver as it must 'float' on the converters mid-point (the output node).

A typical MOSFET turn-on waveform is illustrated in fig. 1.4. The device starts supporting the full DC-link voltage prior to the gate signal being applied (t_0). When the gate signal is applied the converter current will first be commutated through the switching device before the voltage will begin to fall. This results in an overlap in non-zero voltage and current in the time period between t_0 and t_2 which causes switching loss in the device. Hence faster switching speeds will result in lower switching loss.

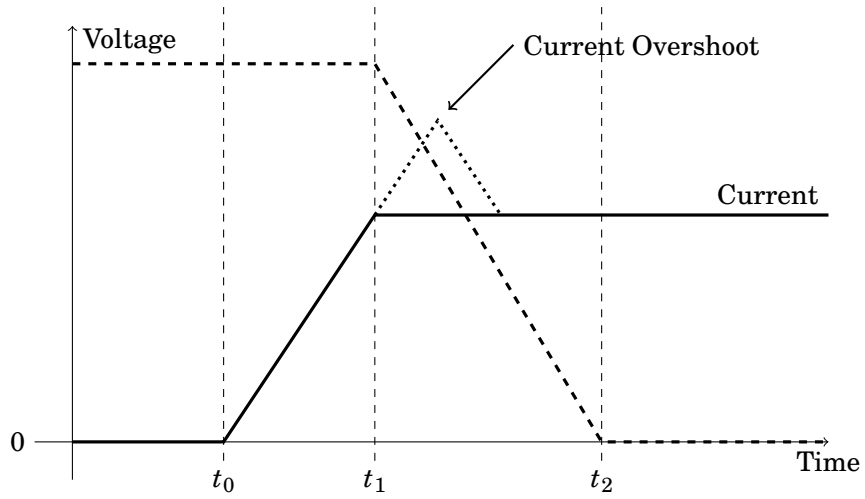

Figure 1.4: Typical shape of a MOSFET turn-on transient

In a practical implementation of a power converter there will typically be some current overshoot in the MOSFET switching transition. This is also illustrated in fig. 1.4 and will lead to additional switching losses as well as increased EMI generation.

Figure 1.5 illustrates the typical turn-off characteristics of the MOSFET. Here there is again a period of overlap during which both the current and voltage are non-zero which will result in switching loss. It is likely that in practice there will be current overshoot that goes below zero. This is often contributed by the Reverse Recovery Current (RRC) of the complimentary switching device and was the subject of the author's previous undergraduate work [1, 2].

The waveforms in a power converter can be approximated using a trapezoidal model. Such a model is illustrated in fig. 1.6. This waveform can be used to approximate the switching device voltage or current waveforms. It is defined by its amplitude (A), the rise time (t_r), the fall time (t_f), the period (T) and the duty ratio (τ). The switching speed refers to a transition and is defined as the time taken for a transition to rise (or fall) for 10 % to 90 % of its amplitude (A).

1.1.3 Wide Band Gap Semiconductors

Wide Band Gap semiconductor devices have been proposed by manufacturers as tool to deliver greater power converter performance than can be achieved with current Silicon (Si) technology. The properties of Wide Band Gap materials enables the manufacture of unipolar devices

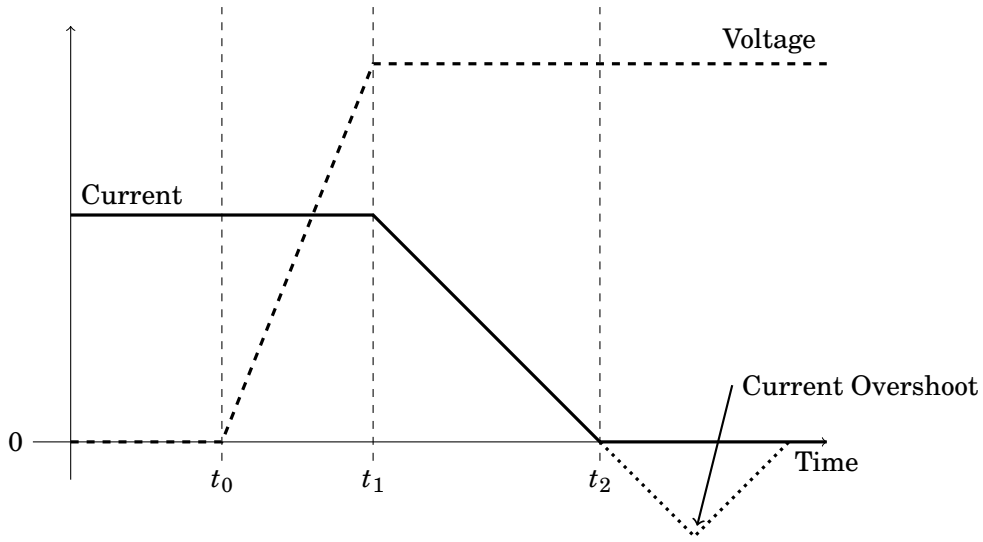

Figure 1.5: Typical shape of a MOSFET turn-off transition

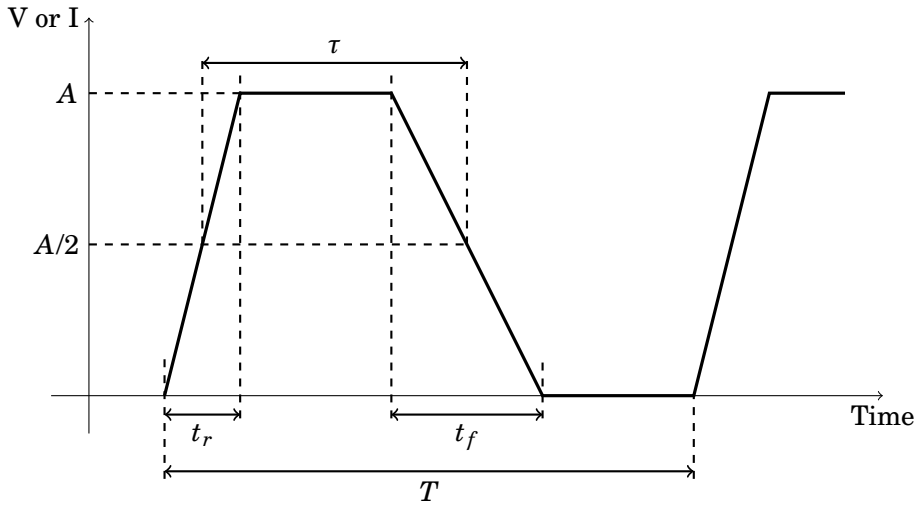

Figure 1.6: Typical power converter trapezoidal voltage or current waveform approximation. Reproduced from [1]

with higher voltage ratings than can be practically produced with Si. They also have higher carrier mobility, enabling faster switching transients which are desirable for low switching loss. In addition to this, Wide Band Gap materials an operate at higher temperatures. All of these benefits combined makes the Wide Band Gap semiconductor device suitable for increasing the performance of power converters in terms of efficiency and size.

Table 1.1 compares the material properties of Si, SiC, and Gallium Nitride (GaN) and shows

Table 1.1: Comparison of semiconductor material parameters at 300 K. Table reproduced from [3]

$Material$	$E_g\,(eV)$	$\epsilon_{crit}\,(kV/cm)$	$\mu\,(cm^2/Vs)$	ε_r
Si	1.11	370	1350	11.8
SiC (4H)	3.26	3180	700	9.7
GaN	3.44	5000	2000	5.35

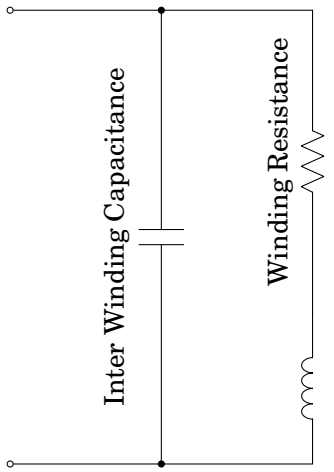

Figure 1.7: Inductor with typical parasitic elements

that Wide Band Gap materials have higher E_g, ϵ_{crit} and μ.

1.1.4 Parasitic Components

One of the focusses of this thesis is the interaction of the power converter with parasitic circuit elements. Parasitic elements are those element which are introduced unintentionally and that have a negative impact on the intended performance. An elementary example of this is the resistance of a wire - a wire will typically be introduced into a circuit with the intention of providing a zero impedance path for current to flow. However, that wire will have some amount of parasitic resistance, which will cause it to heat up with current flow. This is an undesired characteristic of the electrical connection. An example of an inductor with the most commonly associated parasitics is illustrated in fig. 1.7.

In power converters there are numerous electrical connections that will contribute parasitic elements as discussed above. In addition to this, the passive components, the load, and the

switching devices will contribute parasitic elements. As well as the resistance contributed parasitically, these elements will also contribute inductance and capacitance to the system. The high dV/dt and dI/dt transients that occur around the switching devices will interact with these to negatively influence the performance of the converter.

1.1.5 Electromagnetic Interference

A key focus of this work is the Electromagnetic (EM) performance of a power converter. A detailed understanding of its generation, control and reduction is required to allow analysis of the performance of different power converters. The main issue is noise - [4] writes that: *"Noise is any electrical signal present in a circuit other than the desired signal"*. As power converters deal with both large, rectangular shaped waveforms as well as small measurement signals and digital electronics, the potential for a signal to be coupled as noise from one point in the system to another is very high.

To understand the frequency domain content of a signal it can be processed using an algorithm to produce an amplitude vs. frequency plot. For sampled signals such as those in digital systems a common algorithm for performing this transformation is the Discrete Fourier Transform (DFT). This takes a sample of a time domain waveform and produces a representation of the frequency domain composition of that signal.

When performing spectral analysis with the DFT there exists a trade-off between time-domain and frequency-domain resolution. This is a variation of the uncertainty principle which implies that the product of the time- and frequency-domain uncertainty will be constant. One way of viewing this is to consider the time frequency space as illustrated in fig. 1.8. Here the area of the tiles will remain constant if the number of samples of the DFT remain constant. However, though the resolution in the time- or frequency-domain can be varied, it is not possible to increase the density of the tiles without changing the sample length.

It is possible to use the Wavelet Transform (WT) to provide an alternative trade-off between the frequency- and time-domain resolution. The time frequency space diagram for the WT is illustrated in fig. 1.9 showing a variation of the temporal localisation with frequency. Section 2.3.1 discusses existing literature on the application of the WT to the analysis of power converter

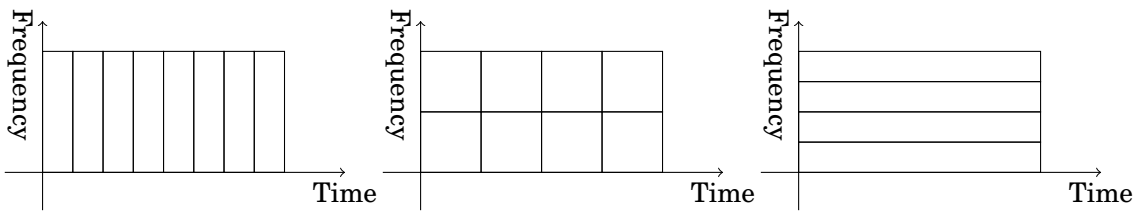

Figure 1.8: Time vs frequency domain localisation trade-off. A broad time domain sample produces high frequency domain resolution while a localised time domain sample produces low frequency domain resolution

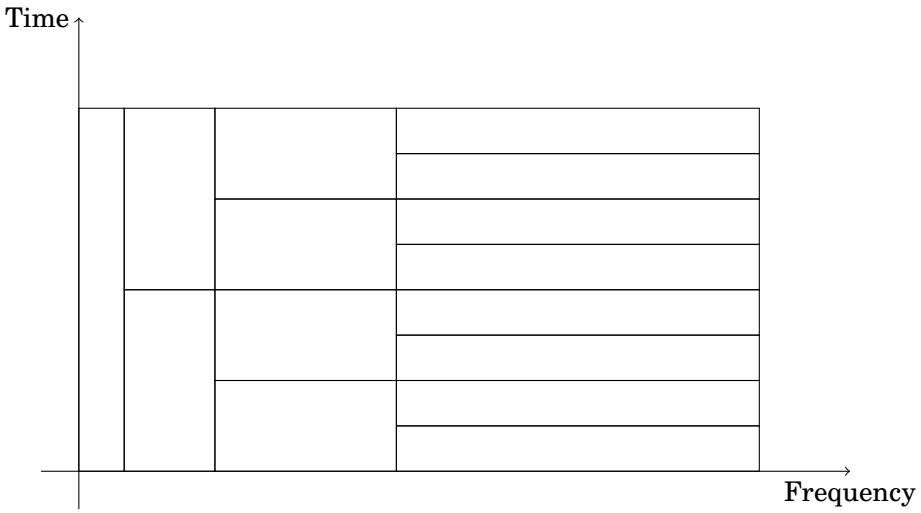

Figure 1.9: Time- vs frequency-domain localisation trade-off provided with the WT

waveforms.

The derivation of the DFT comes from the Fast Fourier Transform (FFT). The FFT is defined as a function of the infinite waveform whereas the DFT implicitly assumes a finite portion of this signal. This leads to spectral smearing. This is the spreading of a single frequency across many frequency bins in the output of the DFT and reduces the accuracy with which frequencies can be identified within a signal. This can be mitigated through the use of a windowing function. This weights the amplitudes of the sampled signal in the time domain to reduce spectral smearing at the expense of frequency domain amplitude inaccuracy. In this work a Hanning (raised cosine) window will be used in spectral analysis.

1.1.6 Design of EMI filters

For a practical converter to comply with regulations on the conducted and radiated EMI it produces the designer will be required to filter EMI using a passive filter. As the switching waveforms for a typical switched-mode power converter discussed in section 1.1.2 contain trapezoidal waveforms they will tend to require good filters.

[5] discusses the design of an EMI filter for a high power switched-mode converter. This design process requires measurements of the unfiltered converter to be taken prior to design of the EMI filter. Designers often must create a converter in this way before the process for filter design can begin, slowing down the development of a finished product. Once measurements are obtained an iterative process for designing the filter is undertaken which will try to stay within the limits of available, practical, and safe filtering components.

The complexity of producing an EMI filter design motivates reducing the generation of EMI at the source - the switching devices.

1.1.7 Previous Contributing Work

The work presented in this thesis builds on previous work by the author in which the the performance of the SiC MOSFET in hard switched converters was evaluated. The thesis, which was entitled *"Characterisation of Wide-Bandgap Devices in High Performance Power Electronics Converters"* explored the impact of the diode RRC on the EMI performance of the power converter. That work found that the improvement in the EMI performance of the power converter due to the removal of RRC with Wide Band Gap devices was offset by the increased emissions from the faster switching transients.

This masters thesis contributed to two publications:

- Conference paper: *"EMI generation characteristics of SiC diodes - influence of reverse recovery characteristics"* [1]
- Journal paper: *"EMI Generation Characteristics of SiC and Si Diodes - Influence of Reverse-Recovery Characteristics* [2]

Table 1.2: Influence of the gate resistance on the switching speed of the devices in the test setup

$R_G(\Omega)$	$dI/dt\ (A/\mu s)$	$dV/dt\ (kV/\mu s)$
100	248	4.9
51	387	8.4
24	593	15.6
12	866	23.7
6.2	1,250	29.8

1.2 Hardware

The investigations in this work will be based around a basic test set-up. The set-up has been selected to be representative of a simple converter and implements a single half bridge using SiC switching devices.

The experimental test set-up consists of a two layer PCB with DC-link decoupling capacitors, Cree C2M0080120D SiC MOSFETs, and gate drivers based around the Microchip TC4452VOA, driving the MOSFET gates from −5 V to 20 V. Use of a bench power supply allows the circuit to run at DC-link voltages up to 600 V with device currents up to 30 A. A programmable signal generator is used to provide the signals for switching the MOSFETs to perform either Double Pulse Tests (DPTs) or continuous tests. The assembled PCB is shown in fig. 1.10 with the top and bottom copper layouts in fig. 1.12 and fig. 1.13. The circuit diagram for this board is illustrated in fig. 1.11. The investigations in this section will make use of double pulse testing as well as zero current switching. A full description of this process and the parameters associated with it are discussed in appendix A.

An initial DPT was carried out with various gate resistances to establish that the switching characteristics were controlled and that the system exhibited classic waveform characteristics as described in section 1.1.1. Figure 1.14 shows some of these initial waveforms recorded from the top switching device. The gate resistor will be varied for many of the tests to control the switching speed. Table 1.2 details the switching speeds that are obtained with a range of gate resistance values.

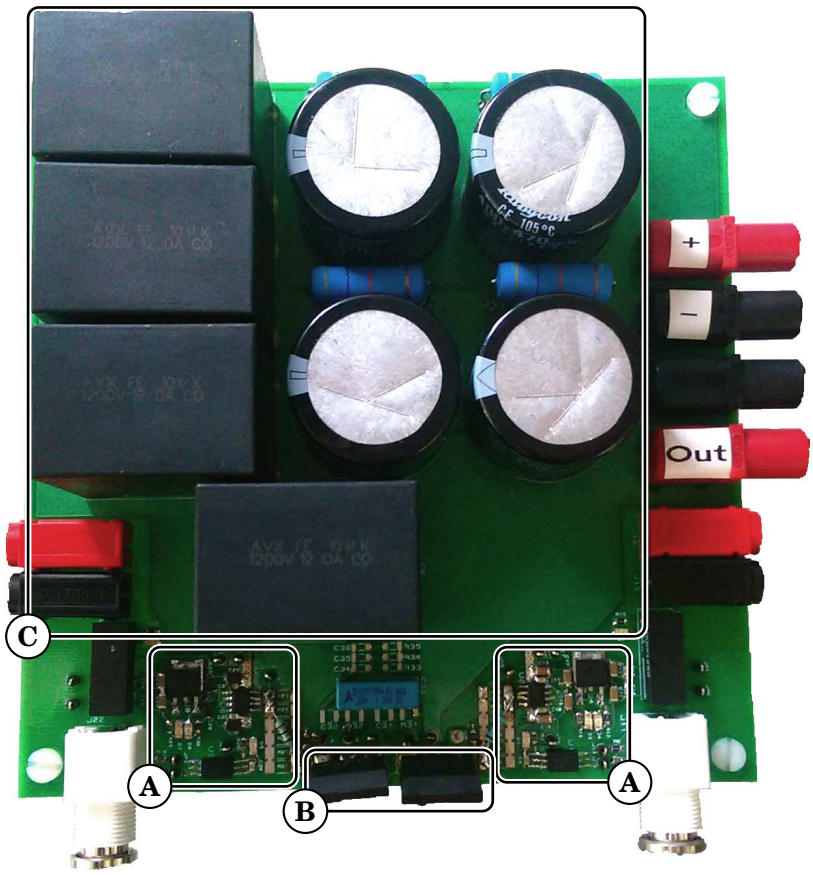

Figure 1.10: The test PCB used in this work. (A) - the device gate drivers, (B) - The Cree SiC MOSFETs, (C) - The DC-link capacitance

1.3 Objectives

Given the drive for high efficiency, high power density power converters, this work seeks to further the performance of these converters - particularly those utilising Wide Band Gap technology. In particular, this work aims to:

- Reduce the generation of EMI in power converters
- Create an accurate simulation model of a SiC MOSFET based power converter
- Investigate and propose techniques for mitigating the influence of parasitic elements

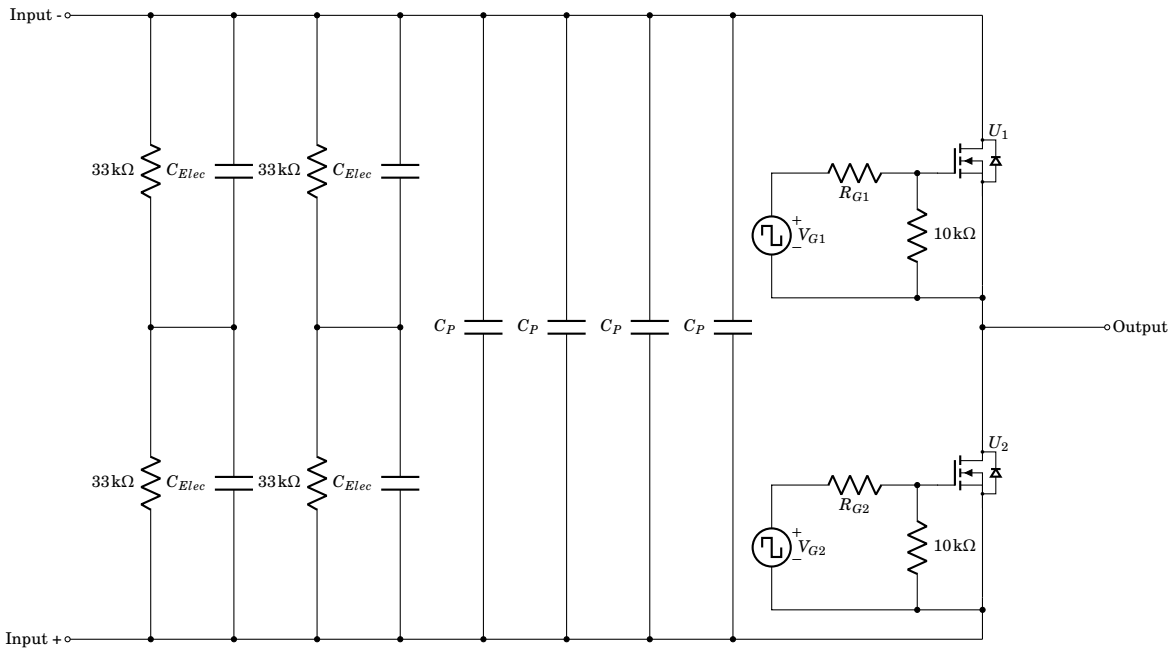

Figure 1.11: Circuit diagram of the test PCB. The capacitors C_P are plastic capacitors with a value of 10 µF and the capacitors labelled C_{Elec} are electrolytic capacitors with a value of 470 µF

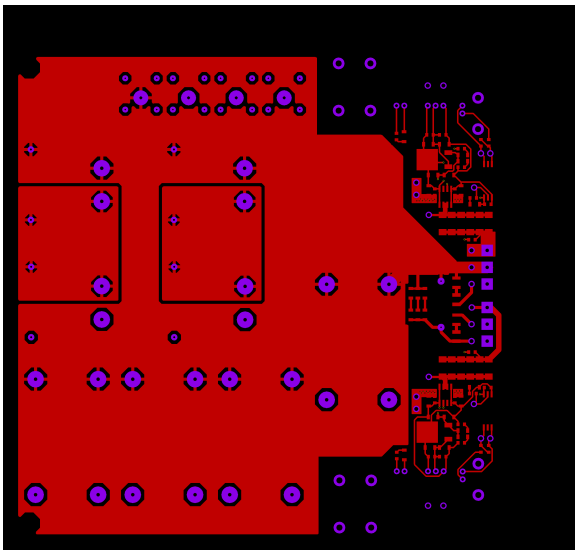

Figure 1.12: PCB top copper layout

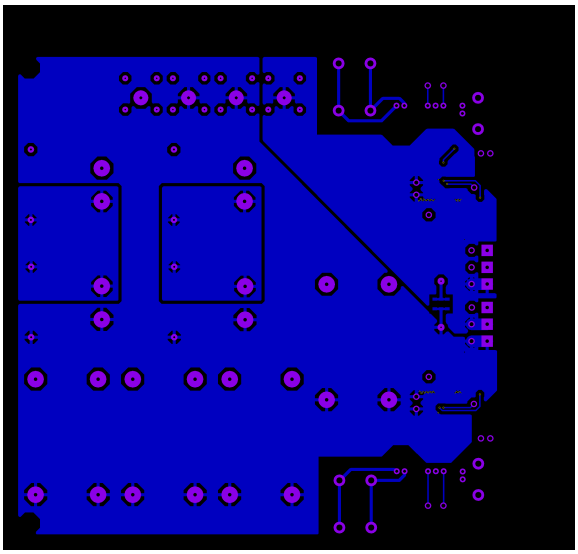

Figure 1.13: PCB bottom copper layout

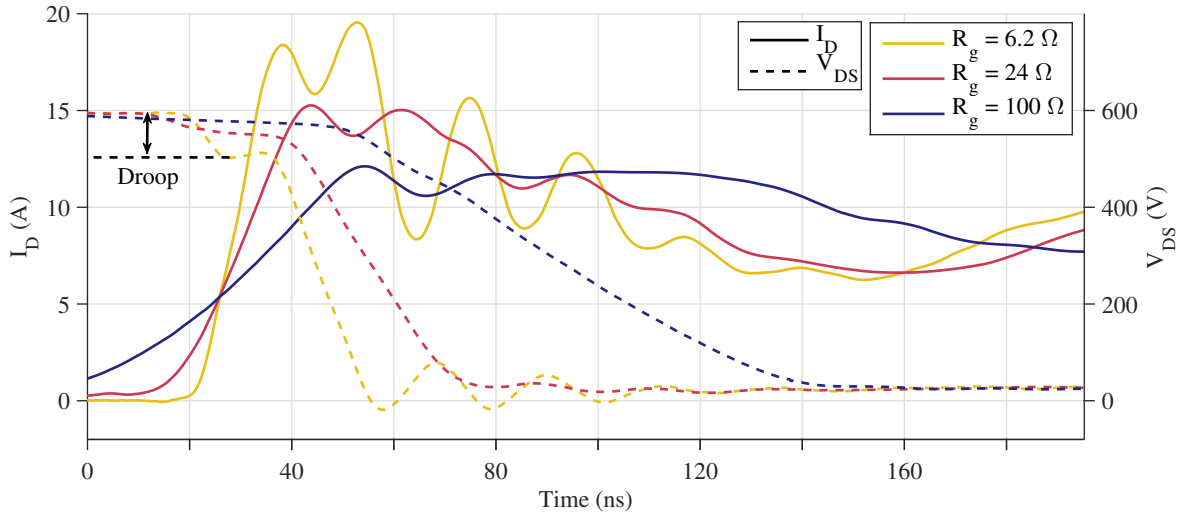

Figure 1.14: Initial DPT results from the experimental set-up with a DC-link voltage of 600 V

1.4 Thesis Structure

The technical content of this thesis is divided into chapters which are presented in sympathy with the chronological order in which the work was undertaken.

- **Chapter 2** reviews existing literature relating to the title of this work. A thorough review of EMI, Wide Band Gap, parasitics, and active gate driving are undertaken.
- **Chapter 3** investigates the manifestation of parasitic elements in power converters, and explores the influence they have on the performance. An experimental setup for use throughout this thesis is presented and a detailed study into the parasitic elements introduced by this is performed. A simulation system is set-up to demonstrate the accuracy of the parasitic extraction and used to propose methods of parasitic mitigation.
- **Chapter 4** discusses techniques for analysing the temporal waveforms of a power converter to determine the source of frequency domain artefacts. This is motivated by the observation of switching waveforms with uncharacteristically high rates of frequency domain roll-off. It goes on to discuss metrics for the EMI generation capability of power converters enabling performance comparisons.
- **Chapter 5 and chapter 6** discuss the removal of high frequency content from converter switching waveforms by smoothing of the transition shapes. The interaction of smoothed

waveforms with parasitic circuit elements is explored and simulation predictions are made. They then go on to present methods for applying these waveforms to a practical power converter and explore the performance enhancements that can be attained through their use.

- **Chapter 7** considers the performance enhancements achieved earlier in the work and seeks to find methods for simplifying the driver circuit while realising the same improvements. A passive gate driving network is proposed and a practical implementation is created and tested.

CHAPTER 2

LITERATURE REVIEW

Exploring mitigating techniques for the influence of parasitics on power converters presents a broad challenge - a detailed understanding of the operation of power converters and figures of merit for their performance will be required. This literature review investigates the state of the art in power conversion technology, applications of Wide Band Gap, and considers topics that will be critical for their analysis.

The review begins with a detailed exploration of EMI as the control and reduction of this is crucial to the performance of power converters. State-of-the-art techniques for modelling and analysing it, along with metrics for quantifying it will also be required. Existing works which have investigated parasitic element in power conversion are explored with a focus on their influence in Wide Band Gap based systems. The properties and applications of Wide Band Gap devices are explored with particular attention to the performance of the state-of-the-art converters. Methods for modelling and analysing these converters are reviewed as analysis will be crucial to understanding the interaction with parasitic elements. The technique of Active Gate Control (AGC) is reviewed in detail with a focus on its application to Wide Band Gap technologies. This technique is shown to be a powerful tool for influencing the performance of a power converter, and opportunities to apply it to the mitigation of the influence of parasitic elements are investigated.

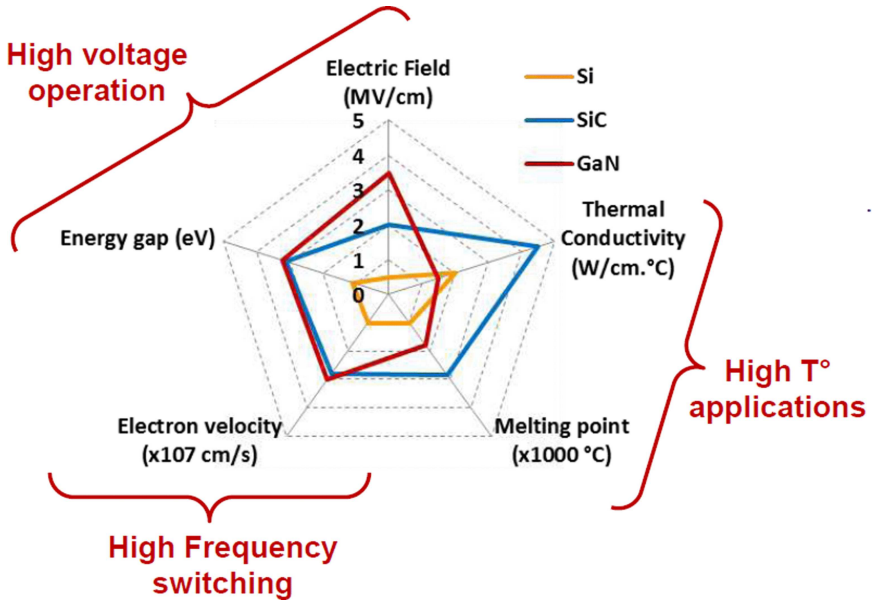

Figure 2.1: Summary of material properties for Silicon, Silicon Carbide and Gallium Nitride. Figure reproduced from [9]

Finally, shortcomings of the existing literature are identified and thus areas for further research are proposed.

2.1 Wide Bandgap Semiconductors

2.1.1 Overview

The primary technology of focus in this work is the Wide Band Gap semiconductor. In recent times wide bandgap semiconductors, specifically SiC and GaN, have shown the technological readiness to replace more conventional Si based technologies ([6, 7]) as well as push the boundaries of devices such as the MOSFET [8]. These new materials have a number of properties that allow for superior operation when compared with their silicon predecessors. Summarised in fig. 2.1, the key features of these new materials are the abilities to operate at higher temperatures, withstand higher voltages, and switch at very high frequencies.

The performance advantages of these devices looks set to greatly change the field of power electronics. With the increase in the switching frequency of a power converter, the smaller the energy storage and filtering elements become. As frequencies increase it enables the use of induc-

tors without any magnetic material [10]. Indeed the frequency of operation of power converters is predicted to rise, and converters with switching frequencies in excess of 20 MHz have already been presented [11–13]. The increase in operating temperature allows some simplification of the thermal design as well as operation in harsh environments.

A important opportunity available with Wide Band Gap devices is the possibility of making high voltage Schottky Barrier Diodes (SBDs). These can withstand higher voltages than traditional Si SBDs, and also have zero RRC. These devices can now be used in medium voltage converters where removal of the RRC can improve the switching loss as well as reduce the EM radiation produced by the converter [14, 15].

The work of [16] suggests that although the SiC SBD has no RRC, the diode recovery time and snappiness factor are not important for determining the EM performance. The cost of the SiC diode is also far greater, which makes evaluating the correct choice for a design more complex.

[15] shows more positive results from the use of SiC in a hard switched converter, finding that it has particular promise for converter designs operating at more than 100 kHz switching frequency. This is supported by [17] where the addition of a SiC SBD drastically improves the converter EMI performance, and [14] where use of the new technology surpasses the performance of Si devices. The authors previous work has also demonstrated strategies for modelling the influence of the RRC on the EMI, finding that significant benefits can arise through the use of the SiC SBD [1, 2].

Figure 2.2 shows experimental results from [14] comparing the reverse recovery characteristics of a traditional Si based diode and a SiC diode illustrating the stark difference in the RRC profile for the different technologies.

Though Wide Band Gap technology comes with a great number of advantages, a new set of challenges is also encountered in trying to utilise it effectively. Section 2.3 considers the characteristics of the temporal voltage and current waveforms in a power converter that contribute to the amplitude of the frequency spectra. The suggested increase in the switching speed and switching frequency will cause issues in terms of meeting EM design requirements [18].

In addition to the difficulty in meeting EMI requirements, the fast switching transients

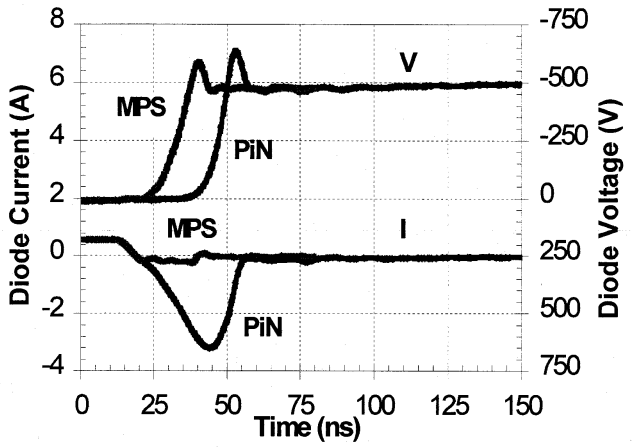

Figure 2.2: Experimental results comparing the RRC of a silicon PIN diode and a silicon carbide MPS diode in a hard switched converter at turn off. Reproduced from [14]

of Wide Band Gap switching devices will also interact with any circuit parasitics to a greater degree than previous devices. These interactions will cause greater current/voltage overshoots as well as increase the switching loss [19]. Both section 2.2 and chapter 3 will consider the interaction of the fast switching transients with the parasitic elements in more detail.

2.1.2 State of the Art

The use of Wide Band Gap semiconductors can enhance many aspects of the performance of power converters for all applications, and the degree to which this has already been achieved should be considered.

GaN transistor technology appears to be the technology that will drive the highest efficiency and highest switching frequency converters. The works of [13] and [12] demonstrate GaN based converters operating at 22 MHz and 250 MHz respectively - these exceptionally high frequencies enable the size of filtering components to be reduced as the energy storage requirement is inversely proportional to the switching frequency. [10] shows how at these high frequencies the filters can be reduced to PCB etched features. GaN is also pushing the envelope of power converter efficiency with [20] presenting a 97 % efficient GaN converter and [21] presenting a 99.3 % efficient design.

As the voltage rating of GaN devices is somewhat lower than that of SiC devices, a limitation

of GaN based converters could be the maximum power rating that can be achieved. Indeed this is one of the advantages of SiC devices. However, converters with medium power levels have already been demonstrated with GaN, such as the 2 kW converter presented in [22], and the 10 kW converter presented in [23].

SiC devices have higher voltage ratings than those of their competing GaN devices and are favoured for their robustness in some applications [24]. This makes them the preferable choice for higher power converters such as the 60 kW SiC converter presented in [25]. State of the art SiC converters do not demonstrate efficiencies as high as those in GaN converters, though they do achieve higher powers. High switching frequencies and very high efficiencies have been demonstrated such as the 96 % efficient, 2.4 kV SiC converter presented by [26], or the 95.91 % efficient, 100 kHz converter presented by [27]. [28] indicates that these performance statistics are not a significant improvement from Si devices which can achieve efficiencies of 96–97 %.

An important opportunity provided by Wide Band Gap technology is increasing the power density of power converters. The work of [29] presents the design and evaluation of a 99 % efficient SiC converter which achieves a power density of 12.1 kW/l over a benchmark for a similar Si converter of 4.1 kW/l.

Wide Band Gap semiconductors enable a wide range of ultra-high performance power converters, though challenges still exist leaving many opportunities for further work to improve on the current state of the art performance. Currently SiC the higher voltage and current ratings of SiC devices makes them the favourable candidate for higher voltage or power application while the high switching speed of GaN devices lend them to the very highest efficiency applications.

2.1.3 Simulation and Modelling

As with all new developments in power electronics, the need to perform accurate simulations of the devices operation is important. For researchers and designers to be able to quickly analyse varying scenarios they need to be able to utilise accurate and fast numerical and analytical models. As the switching speeds of these new devices have become so fast, the influence of circuit and load parasitics are far more pronounced than at previously obtainable switching speeds [30, 31]. This demands that simulation models be far more accurate than has previously

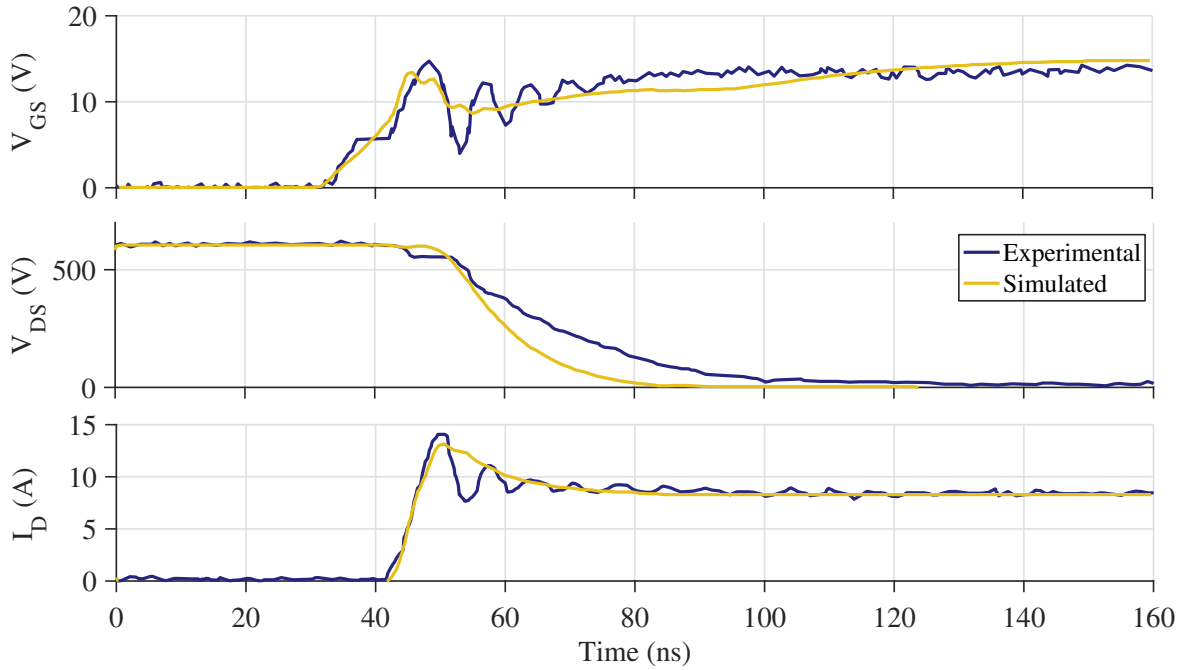

Figure 2.3: Comparison of experimental and simulation results of a SiC MOSFET turn-on transition. Reproduced from [35].

been required.

This demand has motivated a large amount of work on the development of models for the SiC MOSFET, ranging from those that work on developing such a model from fundamentals [32–34], to those which enhance and develop these and existing models further for increased performance [30, 35–38]. These simulations are becoming very accurate - fig. 2.3 illustrates the set of accurate simulation results achieved in [35]. Here the rise-time and overshoot of I_D is very close to the experimental result. The simulated V_{GS} waveform also matches well in terms of rise time, overshoot, and plateau level. The limitations are illustrated by the deviation between the results for the V_{DS} waveforms fall-time and matching of the ringing frequencies on both the I_D and V_{GS} waveforms.

2.2 Parasitic Elements of a Circuit

Parasitic elements of a circuit are those elements which are introduced unintentionally alongside intended components. A very common example of this is the resistance of a copper trace on

a PCB that would otherwise be considered a perfect conductor. Other common examples are the Equivalent Parallel Capacitance of an inductor which introduces a self resonant point, or the Equivalent Series Resistance (ESR) of a capacitor, which introduces losses. Every intentional component of a system will also contain every possible parasitic element to some degree, and though they can be neglected in many cases, in power electronics circuits, determining which elements can be neglected is a significant challenge.

As a power converter represents a system which can often contain all of: high voltages, high currents, high dV/dt, and high dI/dt, it is an environment in which parasitics will have a large effect. They have the potential to cause severe performance degradation, such as increased EM generation, current and voltage overshoots, and increased switching loss [39]. In section 2.1 the increased excitation of parasitic elements due to the adoption of Wide Band Gap devices was discussed - this increased interaction makes the investigation of parasitics more important. This section will explore in detail the various sources of parasitic elements and the effect that these have on the performance of the power converter.

2.2.1 Device Parasitics

The implementation of the switching cells in the power converter is an obvious source of a wide range of undesired parasitic elements. The most basic of these are the on- and off-state resistances - an ideal model of the switch would treat these as a perfect closed and open circuit, whereas the reality is that the device will have a finite on-state resistance leading to conduction losses.

The packaging of the switching device is well known to contribute parasitic elements. The leads of the switching device will contribute some parasitic inductance which will contribute to oscillation in the switching waveforms as well as voltage overshoots at the switching device. These lead parasitics are of particular interest when the switch is implemented with a module where long current paths are formed through the bond wires [40, 41].

An intrinsic parasitic element introduced by the fabrication of the active device is capacitances between each terminal. [42] proposes the model illustrated in fig. 2.4 which includes these capacitances and the inductances introduced by the package. Additionally the model in-

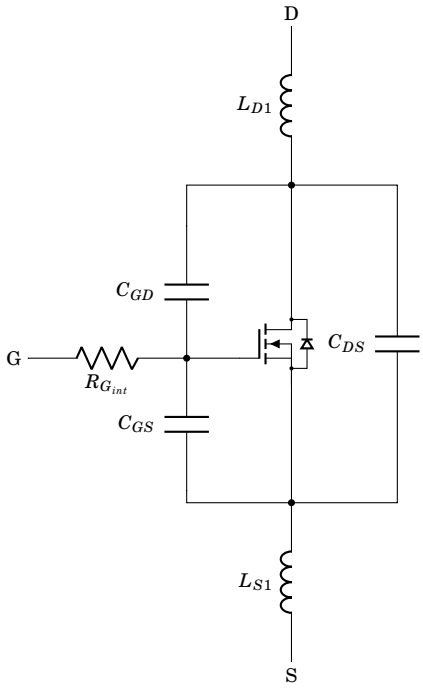

Figure 2.4: Equivalent model of a MOSFET as proposed in [42]

cludes the equivalent internal gate resistance. These capacitances can slow down the switching speed of the device, contribute to increased switching loss, increase ringing and oscillation during switching, and cause spurious turn-on of the device through drain to gate coupling [42, 43]. In many cases the capacitance C_{DS} (equivalently C_{OSS}) will be non-linear, contributing a large amount to switching loss and current overshoot at turn-on [44].

The RRC contributed by either the MOSFET body diode or the co-packaged diode in certain packages can also be considered a parasitic element. An ideal diode would turn off with the current waveform stopping once zero current is reached. In reality, the diode will have some negative current associated with recovery. The characteristics of the RRC have been studied in detail as it contributes to switching loss in the co-device and leads to increased EM generation [2, 45]

2.2.2 Interaction with Other Converter Parasitics

Having considered the parasitic contributions of the switching device, the next most local contribution will be the layout of the circuit, followed by the local components of the converter. The

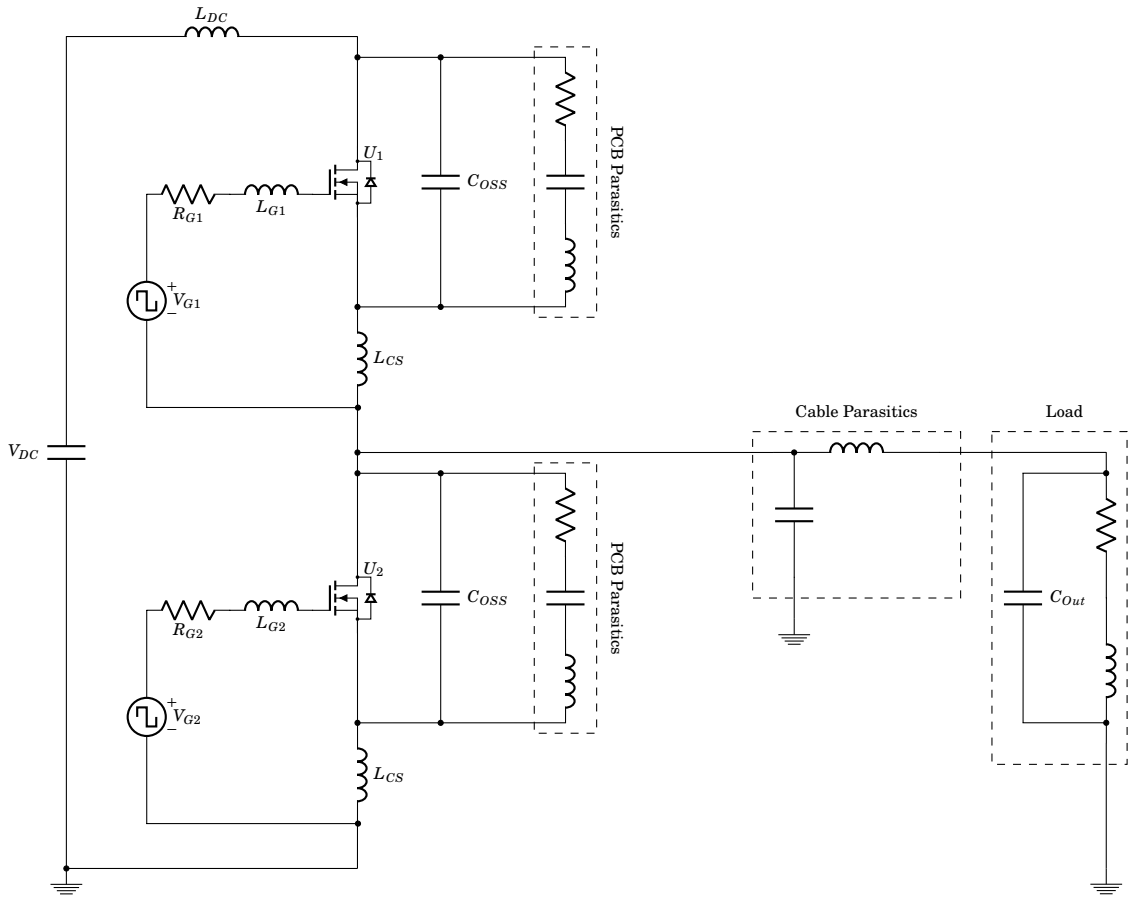

Figure 2.5: Illustration of typical parasitic elements in a single phase leg of a converter including L_{DC} - The DC-link inductance, C_{OSS} - The MOSFET output capacitance, L_{CS} - The common source inductance, the PCB parasitics, the cable parasitics and, C_{Out} - The load EPC

layout typically refers to the design of the PCB for most converters, though for higher power converters where no PCB is used this refers to the interconnection of the switching devices along with other passives.

The layout of the circuit can contribute the full range of parasitic elements, and these can present particular issues when trying to maximise the performance of Wide Band Gap devices. Figure 2.5 illustrates just a few of the parasitic elements of a typical phase leg.

It has been shown that elements such as the gate-loop inductance, switching-loop inductance and the common source inductance will adversely affect the converters efficiency and the EMI produced [46–48]. The influence of the parasitic inductance in the switching loop is particularly important as it has been shown that this can cause very serious ringing and over-voltage dur-

ing switching [49], several works have shown that the introduction of ferrite beads can reduce this ringing at the expense of increased damping [50, 51]. Indeed, for an accurate view of the converters switching characteristics a detailed understanding of all the layout elements must be obtained. The most accurate simulations of the systems performance are obtained when automated parameter extraction of the PCB is used [30, 52, 53].

[54] shows that it is possible to intentionally adjust the circuit parasitics throughout the converter to reach an optimum performance. This allows the irreducible parasitic elements to be mitigated without resorting to drastic minimisation techniques. The other approaches considered focus on minimisation of parasitics, so the technique presented by this work will be of particular importance when other minimisation techniques have been exhausted or are impractical.

Aside from the layout parasitics, the other components in the converter will present numerous significant parasitic elements that need to be carefully considered to maximises the performance of Wide Band Gap based converters. The passive elements of the system such as the DC-link capacitors can have a significant effect on the switching performance, causing voltage droop and increased switching loss [55]. The severity of the effect that these parasitics have on the performance is such that detailed design of each of the power components is warranted [56].

There are also more subtle parasitic effects that will be found when a careful model for EMI sources is constructed - the positioning of the heatsinks relative to the switching devices can be significant ([57]) and the common-mode capacitance of the gate-drive circuits can form paths for conducted EMI [58]. To maximise the performance of high switching speed converters the parasitic elements in the EMI filter must also be considered [59].

2.2.3 Interaction with Load Components

The load connected to the converter can have a very significant effect on its performance. For the case of a motor load, it is often found that they will have a significant Equivalent Parallel Capacitance (often in the range 0 pF to 1000 pF) which presents a bypass circuit for high frequency elements and can cause significant current overshoot in the switching devices [60–62]. Typically when converter technology is tested under lab conditions an optimised test inductor

will be used, whereas in a typical motor drive application the output will be far from this ideal case [63]. The capacitance of the load can lead to large current overshoot, which contributes to additional switching loss and increased EMI generation. It has been suggested that the inclusion of an auxiliary inductor could decouple the load to remove this effect [64].

In motor drive applications there there will often be a significant length of cable between the drive and the motor. The impedance of the output cable will introduce additional output capacitance to the converter, and create waves and reflections that will contribute to voltage overshoot at both the switching devices and the motor [65, 66]. These additional voltage overshoots will cause significant increases to the radiated and conducted EMI generated by the system and cause degradation of the motor winding insulation [67]. Some works have proposed models for helping predicting aspects of a system's performance under the influence of long cables [68].

With the exploration of converter parasitics detailed so far a typical phase leg of a converter is illustrated in fig. 2.6 with many of the common parasitic circuit elements that contribute to the converters performance. This illustration is not exhaustive.

2.2.4 Measurement Techniques

A particular problem when working with Wide Band Gap technologies comes in the measurement of their waveforms. It is very difficult to take any measurement from a system without changing the behaviour of the system, even if this is only in a small way it may still cause captured data to be misleading. Here, each of the common probes used to investigate a power converter are considered to establish their impact on the observed waveforms.

2.2.4.1 Voltage Measurement

When making medium voltage measurements there two typical probing options; high impedance passive probes, or differential probes. Each of these comes with its own relative merits and flaws - passive probes are cheap, but require a grounded connection which prohibits their use for measurement of floating signals. Differential probes overcome this problem, though they have a limited Common Mode Rejection Ratio (CMRR) which can cause unwanted noise in measurements, particularly for typical power electronics waveforms [69]. [70] discusses the impact that

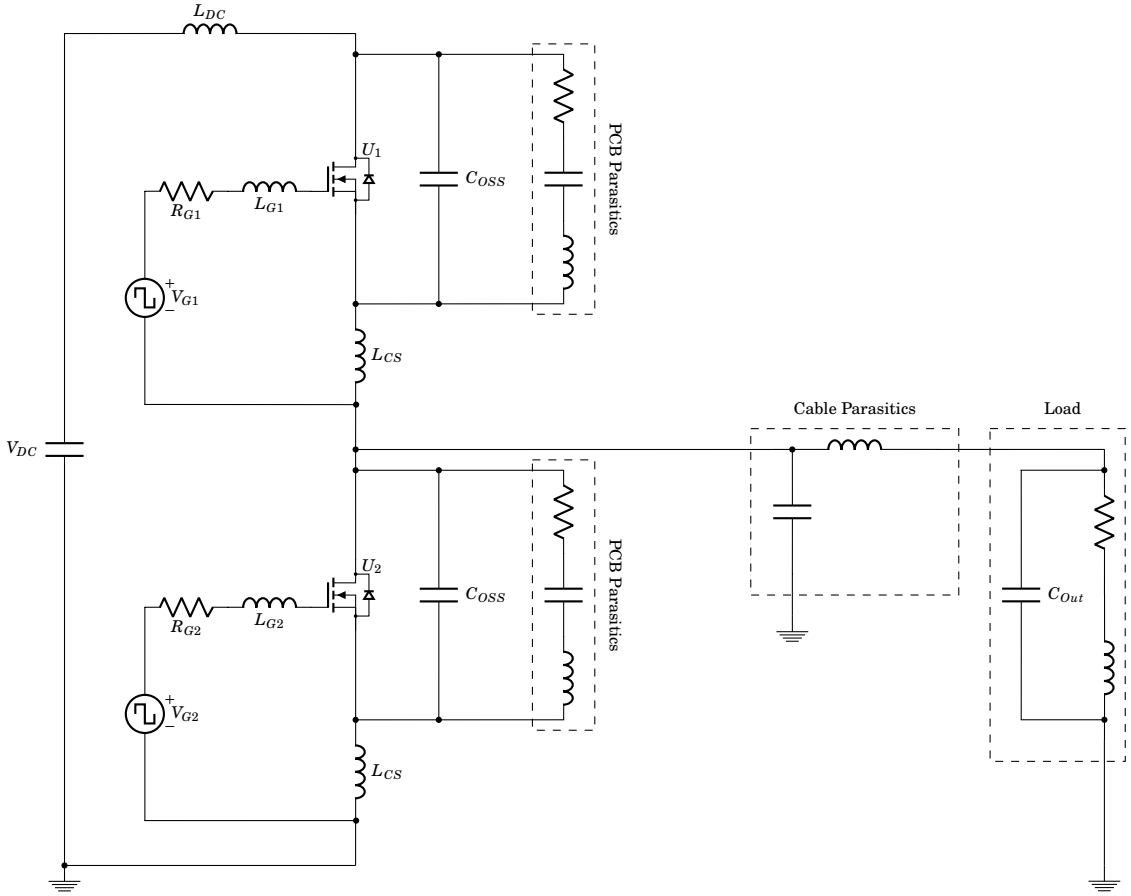

Figure 2.6: Illustration of typical parasitic elements in a single phase leg of a converter including L_{DC} - The DC-link inductance, C_{OSS} - The MOSFET output capacitance, L_{CS} - The common source inductance, the PCB parasitics, the cable parasitics and, C_{Out} - The load EPC

the long leads typically present on differential voltage probes can have on taking repeatable measurements, finding that their placement can make a significant different to the shape of the observed waveform.

Both differential and passive probes are non-ideal in operation. In theory the ideal probe has infinite impedance across all frequencies, whereas in practice the probe will add a load to the circuit under test. Of particular interest in power electronics applications is the probe tip capacitance - as the waveforms in power converters contain large dV/dt edges the current that can be admitted into a probe's tip capacitance may be significant when trying to take very precise measurements [71, 72].

The work of [73] has found that the speed of the measurement equipment employed in mea-

surement of Wide Band Gap switching devices can often hide the true characteristics. It is found that the equipment measuring the switching edge of interest should be 3.1 times faster than the signal it is measuring to ensure the error remains below 5 %. This has serious implications for the equipment used to take accurate measurements of these technologies.

2.2.4.2 Current Measurement

When considering taking accurate measurements of current waveforms there are several technologies that could be employed. These are hybrid current clamps, coaxial current shunt resistors, or Rogowski coil probes. Each of these methods has its specific advantages and disadvantages.

The hybrid current clamp is one of the most common techniques used for measuring current in power electronics applications. These are available in high bandwidths which extend from DC to around 100 MHz. They have low noise and are quick and easy to use. However, for very high switching speed applications the physical size of the probes can present issues as they call for space in the layout which can introduce unacceptable parasitic inductance. In addition to this added space requirement they have a non-linear insertion impedance as a function of frequency that must be taken into account [74]. An example of the insertion impedance of a typical probe is shown in fig. 2.7.

Another issue that can occur with this type of probe is noise induced by a high dV/dt being presented to the probe. Section 3.1.4 discusses this is detail.

A good alternative to the hybrid current clamp is the coaxial current shunt resistor [76]. These have exceptionally high bandwidths (> 1 GHz) and have a constant insertion impedance with frequency which makes them easy to model in simulation. However these are not good for making measurements of currents at points in the circuit where one of the terminals of the resistor will not be grounded, as a differential voltage probe is then required. The use of a differential probe to measure the floating current sense resistor will introduce the problems associated with differential probes discussed previously, as such high fidelity measurement precludes this option. The use of a shunt resistor require the circuit layout to be designed around its use which will increase the board space required.

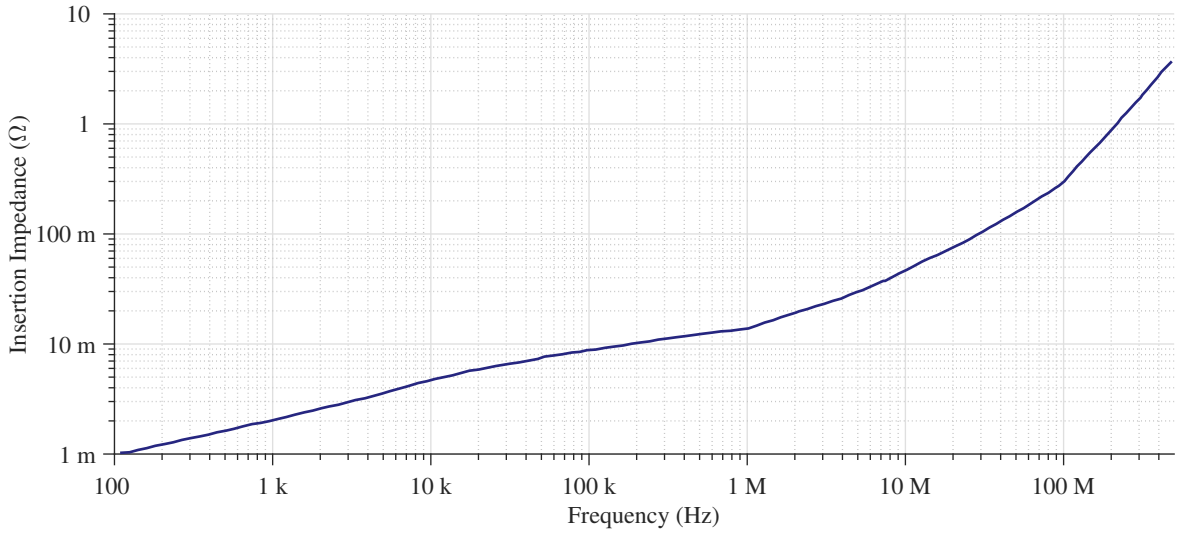

Figure 2.7: Insertion impedance of typical hybrid current clamp probe - Reproduced from [75]

A comparatively new technology for the measurement of current waveforms is the Rogowski coil. These are advantageous in power electronics applications due to their very small physical size which allows them to fit into existing circuit layouts. Additionally they have very low insertion impedance (10 pH [77]) which makes them suitable for measurement of sensitive circuits [78].

However, there are some significant drawbacks to the use of the Rogowski coil - the first is that they often have relatively high noise ([78]), particularly at low frequency, which can be a problem for making accurate measurements of the power dissipation in a switching device. Often their design restricts the accurate measurement of the low frequency current due to the reliance on an integrator, though some works have proposed the inclusion of a hall effect element to improve the low frequency bandwidth [79]. As with the hybrid current clamp probe, the Rogowski coil is subject to dV/dt induced noise, though it is possible to design a differential coil to remove this [80]. Presently however, commercially available Rogowski coils do not utilise this design.

The state of the art in Rogowski coil design is the PCB integrated differential probe [81] - these demonstrate the advantages of the very small physical size and insertion impedance of these probes, though significant PCB design work is required to realise this performance.

2.2.5 Methods of Parasitic Extraction

The parasitic elements of a Wide Band Gap power converter and its load are crucial to determining the performance. Effective modelling and prediction of the converter is then reliant on accurate calculation or measurement of the values of the parasitic elements - this is the field of parasitic extraction.

Section 2.1.3 showed simulation results for a hard switched SiC converter. These simulation results predict the operation of the circuit with reasonable accuracy. The results presented have been enabled through the use of parasitic extraction with 3D Finite Element Analysis (FEA) techniques. The works of [30, 82] use such techniques and have demonstrated simulation results that are faithful to experimental results. This demonstrated the simulation accuracy that can be obtained through use of these tools.

Accurate measurement of the passive elements that interact with the switching devices is also crucial. Typically this is approached with the use of an impedance analyser, though in power electronics applications the passive element may need to be biased to the voltage or current levels that they would experience in operation for accurate measurement. Often biasing to this level is out of range of typical impedance analysers, and special care must be taken - [83] shows how additional elements can be added to the test fixture of an analyser to provide high power drive.

The switching device itself must also be accurately understood and datasheet parameters for the device are often insufficient for this. Techniques for extraction of the device characteristics such as those discussed in [84] are required to avoid lengthy testing with traditional LCR meters. In the case where the switching device is a power module, the complicated interconnects require careful analysis through the use of innovative techniques such as the Scattering parameter analysis presented in [85] which requires the use of a Vector Network Analyser (VNA).

2.2.6 Mitigation

Given the wide range of negative effects that the parasitic elements of a power converter have on the performance there is a critical need for any technique that can improve the performance in the presence of these elements. Particular value can be attributed to techniques that do not

require complex and expensive circuitry or major modification to the design. [54] presents a technique which achieves this - instead of trying to minimize the parasitic elements they are intentionally manipulated to provide useful impacts. Specifically, the parasitic capacitance can be adjusted to provide snubbing and remove the need for discrete snubber components. This will contribute to reduced component count, converter mass, and converter volume.

The high value, non-linear C_{OSS} of super-junction devices presents a difficult element to overcome. The work of [86] has suggested a method through which drain current is injected into the device prior to turn on to pre-charge this capacitance without the associated losses during switching. This technique achieves a converter efficiency of >99 % despite the large C_{OSS} of the switching devices.

The parasitic elements found in the load and cable of the converter are addressed in many works. The works of [64, 66, 87] discuss decoupling of the load capacitance through the use of a small reactive element in the output connection of the converter. This is a simple and effective way of improving the converter performance.

As well as the mitigation methods discussed, some works propose design guidelines for enabling performance maximisation. [46, 53] have proposed guidelines on the layout of the PCB to minimise the parasitic elements. A particularly detailed set of guidelines is given in [42] where the trade-offs of each layout optimization are considered, and priority is assigned to the various parasitics. In particular:

- The gate-drain and drain-source capacitances should be kept low. This maximises the voltage slew rate
- The gate resistance should be kept low to help maximise the voltage slew rate
- The gate-source capacitance, stray inductances, and gate resistance should be kept low to maximise the current slew rate
- Trace lengths should be minimised and current loops kept small to minimise stray inductance which would otherwise cause device stress by voltage overshoot
- Separate turn-on and turn-off gate resistances should be used to provide a better optimisation between losses and voltage/current stress

2.3 Electromagnetic Interference

A converters EM performance will likely have to comply with certain regulations. These are limits on the emissions of a system that are imposed so as to reduce the chance of systems interfering with each other [88]. The requirement to comply with these regulation and controls motivates methods for prediction and control of the EMI produced by a converter and has resulted in a wide range of practical techniques. This section explores current literature on the subject of EMI.

In power electronics the switching devices are the most critical source of EMI. The fast switching transients, high voltages, and high currents mean that both high dV/dt and high dI/dt waveforms exist in the switching loop. As such most works focus on producing models of the interference caused by a trapezoidal approximation of these waveforms [89–91].

To control the level of EMI and meet regulations, a range of techniques exist. Often the methods employed to reduce the EM emissions are techniques such as shielding and the inclusion of filter elements, though these contribute significant cost and weight to any design. Alternatively, the noise can be suppressed at the point of generation [92]. The work of [93] discusses careful control of the gate resistance, coupled with the filter design, to realize substantial improvements, while [94] shows that two converters combined back-to-back can be controlled so as to eliminate the EM emissions.

It has been shown by [95] and others that the sharp edges of the temporal switching waveform will be significant contributors to the EM performance. A field of techniques exist in smoothing the transition waveforms for reduction of the EMI generation capability at the switching devices [96, 97].

Given that suppression of the EM noise at the source may not be sufficient or practical in many designs, there is a wide range of technology in the art of filter design for power electronics. The work of [98] shows a design which is able to measure the noise and actively inject a waveform to reduce this, achieving very low emissions. [99] controls the parasitic elements in the filter to achieve very high performance filters, and [100] investigates the influence of long motor cables to ensure the filter is able to control the voltage overshoots at the motor which are

known to reduce the life of the motor [60]. It was stated earlier that the addition of filters to the converter will increase the cost and weight, though [10] demonstrates a filter that is integrated in the PCB itself which can be applied to Wide Band Gap based converter designs significantly reducing the impact on the size and weight. This takes advantage of a very high switching frequency ($< 10\,\text{MHz}$) to use inductors and capacitors which are directly etched into the PCB.

2.3.1 Modelling and Analysis

Accurate models assist in the analysis of the waveforms from switching converters and can help to identify the temporal source of frequency domain characteristics. A wide range of methods exist for modelling, predicting and analysing the EM performance. These methods will now be considered in detail.

There are two typical ways of analysing the waveform of fig. 2.10; either numerical, or analytical methods. These assume that the waveforms in the physical implementation conform to the shapes illustrated in fig. 2.10. [101–103] present numerical methods for the analysis of the EMI in various power electronic systems, though they do not provide particular insight as to how features of the switching waveform will contribute to the emissions. [90, 91, 104–107] present analytical methods for analysing common waveforms and give more insight into how the features of the temporal waveform will influence the frequency domain representation of the waveforms. From the designer's perspective, an analytical model is more desirable as it will give some insight into which aspects of the temporal waveform are most critical. Other works discuss alternative methods of analysing these waveforms which offer other benefits such as very fast simulation times [104], and in [108] a graphical approach is discussed which allows the analysis of waveform shapes of greater complexity than that of the trapezoidal model.

Analysis techniques also exist which are not based around modelling of the power converters waveforms. These strategies typically seek to analyse existing data captured from a converter to help identify the source of noise. [109] demonstrates a strategy in which the time domain converter waveforms are repeatedly differentiated to reveal the high order characteristics, which are shown to be critical to determining the high frequency performance. An alternative to the DFT which provides time localisation of high frequency noise generation is the spectrogram -

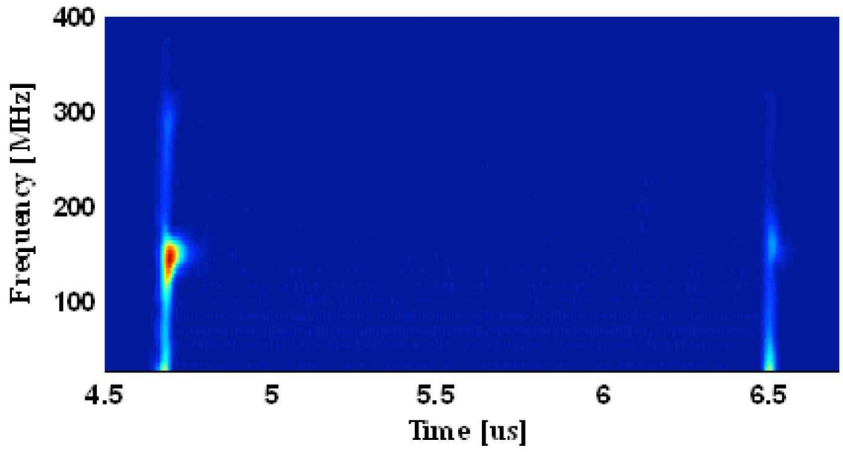

Figure 2.8: An example of a spectrogram for identifying the temporal source of frequency domain noise. Figure reproduced from [111]

this is applied to noise identification in power conversion by the works of [110, 111]. Applied well this technique can identify the temporal source of noise in a simple graphical way as illustrated in fig. 2.8.

An alternative to use of the Short-Time Fourier Transform (STFT) as relied on by methods producing spectrograms is the WT [112]. The WT is able to provide a better balance of the trade-off between frequency- and time-domain resolution determined by the uncertainty principle, making it a promising tool for the analysis of power converter switching waveforms.

The WT achieves this balance between frequency- and time-domain resolution by using a non-uniform bin size as a function of frequency. This varying bin size is illustrated by fig. 2.9. Adjustment of the wavelet size and shape allows the distribution of the bins to be varied. This enables better time localisation as there are more bins per unit time at higher frequencies, though it retains better low frequency accuracy by using fewer bins at low frequencies.

There is a broad range of works investigating specifically the application of the WT to EMI analysis in the field of power electronics [113–118].

Works such as [90] suggest models that take simple measurements of the characteristics of the temporal waveforms to make accurate predictions of the frequency domain envelope. A typical converter switching waveform approximation is shown in fig. 2.10. It is characterised by its fundamental period (T), the amplitude (A), the rise and fall times (t_r and t_f) and the duty

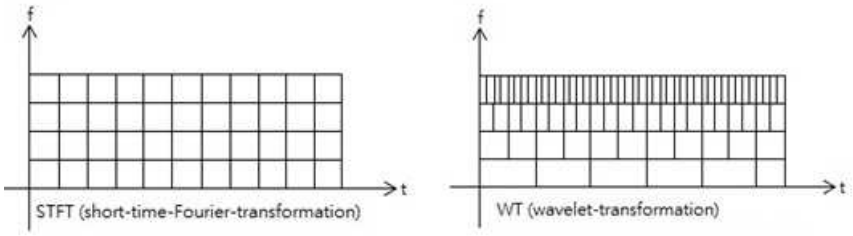

Figure 2.9: Comparison of STFT and WT reproduced from [119]

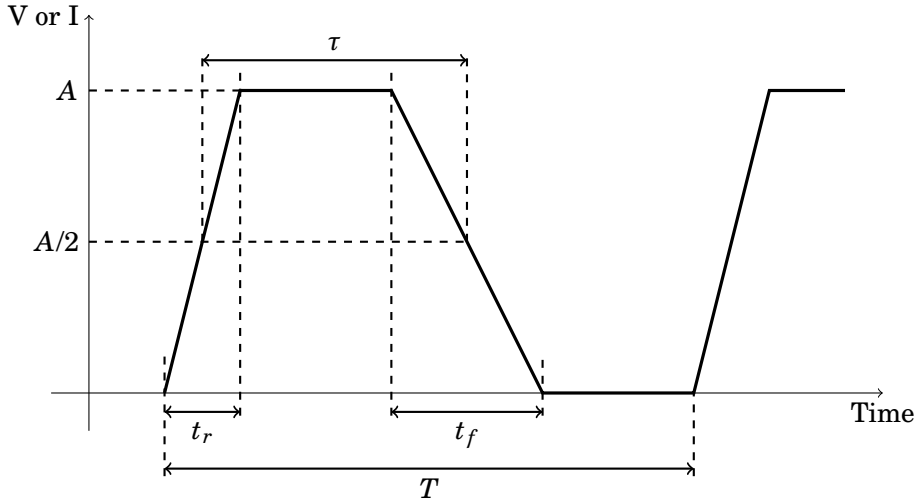

Figure 2.10: Typical power converter trapezoidal voltage or current waveform approximation. Reproduced from [1]

ratio $\left(d = \frac{\tau}{T}\right)$. The characteristics of these trapezoidal waveforms in the frequency domain have been widely reported [89, 90, 108, 120–122]. Figure 2.11 shows the form taken by the envelope for a few cases of converter waveforms.

The envelope shown in fig. 2.11 can be very quickly determined from the waveform parameters illustrated in fig. 2.10 by using eqs. (2.1) to (2.13) taken from [90] with K - harmonic number, f - the frequency and f_0 - the fundamental frequency ($frac1T$).

$$R = \frac{t_r}{T} \quad (2.1) \qquad F = \frac{t_f}{T} \quad (2.2)$$

$$d = \frac{\tau}{T} \quad (2.3) \qquad f = Kf_0 \quad (2.4)$$

$$\alpha = max(R,F) \quad (2.5) \qquad \beta = min(R,F) \quad (2.6)$$

$$K_{c1} = \frac{2}{\frac{\pi}{A}S(1)} \quad (2.7) \qquad K_{c2} = \frac{1}{\pi\alpha} \quad (2.8) \qquad K_{c3} = \frac{1}{\pi\beta} \quad (2.9)$$

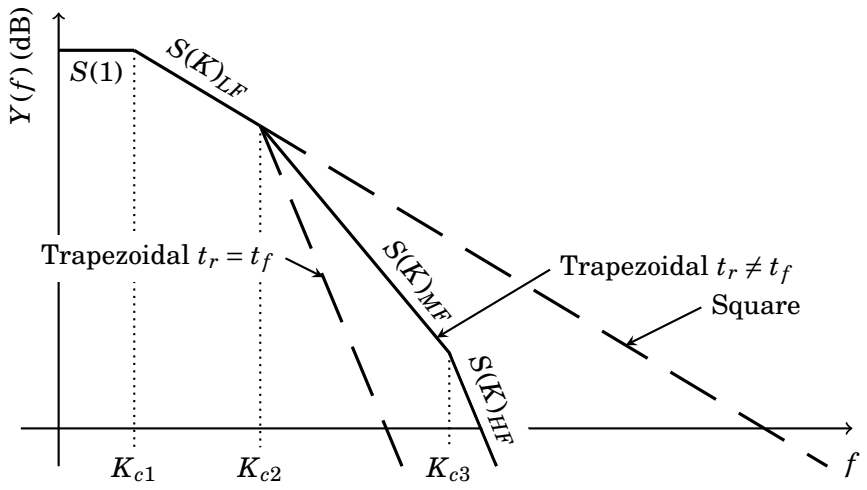

Figure 2.11: Spectral envelope of typical power electronics waveforms. Adapted from the works of [1, 89].

$$S(1) = \frac{A}{\pi}\sqrt{[sinc(\pi R) + sinc(\pi F)]^2 sin^2(\pi D) + [sinc(\pi R) - sinc(\pi F)]^2 cos^2(\pi D)} \tag{2.10}$$

$$S(K)_{LF} = \frac{2A}{\pi K} \quad (2.11) \quad S(K)_{MF} = \frac{A}{\pi K}\left(1 + \frac{1}{\pi K \alpha}\right) \quad (2.12) \quad S(K)_{HF} = \frac{A}{\pi^2 K^2}\left(\frac{1}{R} + \frac{1}{F}\right) \quad (2.13)$$

These equations show that any increase in either the amplitude (A), or speed of the rising or falling edges $\left(\frac{1}{t_r}, \frac{1}{t_f}\right)$ will lead to an increase in the amplitude of the envelope of the frequency spectrum. They also show that if it is possible to reduce the switching frequency $\left(\frac{1}{T}\right)$ then this will lead to considerable improvements in the EM performance of the converter, though this will likely be at the cost of switching loss.

A wide range of techniques have been explored that allow the EM performance of a power converter to be analysed, however, these methods do not lend themselves to easy comparison of several converters. As this work will explore a large number of variations in converter design a figure of merit is required. The work of [123] discusses such a metric for power converters and is based on the required filter breakpoint to hit an arbitrary performance target. Alternatively, [97] suggests the summing of the power in a particular frequency band as a metric. Later in this work, each of these metrics will be tested on actual power converter switching waveforms to evaluate their usefulness.

2.3.2 Trade Offs

A difficult issue to address in switching power electronics devices is the trade-off between switching loss and EM generation [124, 125]. As the device is pushed to minimise the switching transient length the switching loss is decreased. However, as the models discussed here have already shown, the faster and more frequent the transients of the voltage and current, the higher the EM generation of the waveform will be.

An interesting and important area of work is identifying techniques that mitigate this trade-off to enable converters to have both low switching loss and low EMI generation. Various approaches to this problem have been made - [126] suggests that mixing device technologies could enable an improvement upon this trade-off reducing the switching loss by 70 %. As using a mix of device technologies will not be practical in many applications, alternative approaches exist. [127] uses independent control of the turn-on and turn-off switching transients to optimise the switching loss and the EMI independently lowering the Common Mode (CM) EMI by 5 dB and increasing the efficiency by 1.21 %. The works of [97, 128] offer solutions that rely on manipulation of the gate waveforms. [128] simply uses careful control of the IGBT switching speed achieving 13 % reduction in switching loss, whereas [97] demonstrates the use of gate voltage profiling to influence the shape of the device waveforms for a 20 dB EMI reduction.

Though these techniques offer improvement in the trade-off, it is not clear which technique will be best suited to a particular application. All of these techniques will increase the complexity or cost of the full system which may not be acceptable in all applications.

2.4 Active Gate Driving

A technique that will be considered in some detail for the mitigation of the influence of parasitic elements is the use of AGC. This technique offers control of the performance of a converter and as such it will be considered in detail in this work.

Using the technique of AGC involves somehow controlling the transient shape of the voltage or current imposed upon a switching device so as to influence the switching transient. Typically this type of gate driving strategy is more complex than that of traditional drivers which simply

apply high-speed rising or falling edges via a preset gate resistance.

A very wide range of literature exists in the field of AGC with applications to many different switching device technologies, though is most well established for Si IGBTs - the work of [129] provides a summary of the state of the art for these devices. This technique has also been explored for application to the Si MOSFET as early as 1997 [130] and has been developed significantly since then. As the focus in this work will be on Wide Band Gap devices, applications of AGC to this will be the primary interest. As Wide Band Gap devices are beginning to reach maturity most of the variations of device have been investigated. The work of [131] has explored the application of AGC for non-insulating-gate Wide Band Gap devices and the work of [132] has taken a closer look at the SiC Junction gate Field-Effect Transistor (JFET). Insulated gate Wide Band Gap devices have also been widely investigated and the works of [133] and [134] show the application of AGC to both GaN devices and the SiC MOSFET.

The wide range of existing literature on AGC shows that this is a developed area in regards to mature technologies such as Si. The applicability of AGC to so many devices shows that it is a versatile technique, motivating further development of this within the scope of Wide Band Gap devices.

2.4.1 Advantages of Active Gate Driving

The use of AGC can be applied to many technologies, and the existing literature shows a wide range of performance improvements that can be made through this technique. Exploring the advantages of the use of AGC makes clear the motivation for the increased complexity that these drives will introduce.

A typical problem in power electronics discussed in section 2.3 is that of EMI generation in the converter. This is a problem which has previously been addressed with a range of techniques, though at the cost of a trade-off with the switching loss - a technique without this trade-off would be advantageous. The works of [134–136] discuss the application of AGC to SiC devices where the generation of EMI is reduced without compromising on the switching loss. Likewise, the works of [137–139] discuss similar advantages realised for GaN switching devices.

The losses in the switching devices are a primary source of inefficiency in a power converter,

Work	Technology	Switching Loss	Speed	Overshoot
[143]	SiC	5.3 %	Slower	Reduced
[144]	SiC	53.3 %	Unchanged	28.2 %
[145]	SiC	Unchanged	n/a	30 %
[146]	SiC	20 %	n/a	Reduced
[147]	SiC	Reduced	Faster	Reduced
[148]	SiC	n/a	Faster 29 %	Unchanged
[149]	SiC	30 %	n/a	25 %
[141]	GaN	33 %	n/a	n/a
[142]	GaN	0.5 %	Unchanged	Unchanged

Table 2.1: Comparison of the performance improvements obtained through the use of AGC in previous literature

and the reduction of this is critical to producing ultra-high performance converters. As such, AGC has been applied to the reduction of this loss by a wide range of work. The works of [140–142] have demonstrated the application of AGC to GaN switching devices, and other works have implemented switching loss improvement using this technique and SiC switching devices [143–149]. The improvements achieved by each of these works are compared in table 2.1.

Some existing work has looked more specifically at how the trade-off of the efficiency and EMI generation of the switching transients can be influenced by AGC, finding that there is a large scope for independent control of these two performance metrics [95]. However this is still a trade-off and does not solve the loss/EMI issue and finding better performing and simpler solutions is still required.

A novel application of the AGC technique is to control the switching loss such that the device thermal stress is reduced. In the work of [150] the dV/dt is controller to intentionally increase the device losses some of the time to keep the device at a constant temperature. This is an interesting example of a technique for extending the lifetime of these components as it does not simply focus on minimisation of switching loss or EMI and illustrates the wide range of performance enhancements AGC can realise.

Enabling the potential performance of Wide Band Gap technologies is a common focus of current works. Using AGC to achieve this is something which is explored in [151] - here the gate transitions are profiled to reduce the influence of the switching transient on the gate voltage of the co-device in a half bridge leg.

A more common application of AGC is the reduction of oscillation and overshoot. Both of these effects can contribute to an increase in the generated EMI from a converter. Additionally, the current overshoot will tend to contribute to increased switching loss and the voltage overshoot contributes to device stresses. Several works have considered AGC as a tool for suppressing these effects with [133] considering the application to GaN devices, and the works of [152] and [132] considering application to SiC devices.

The work of [153] explores the use of AGC for enabling the high performance of Wide Band Gap devices by providing improved short circuit protection. This is another example of a uncommon application of the AGC technique and the variety of control it allows.

The works presented here show that the technique of AGC can offer a very wide range of performance benefits and that these are even more broad when considering the application of the technique to Wide Band Gap switching devices. The switching loss, EMI generation, device stresses, and oscillation are all common performance metrics which can be improved with this technique. Additionally, the literature explored has demonstrated that thermal profile control, short circuit protection, and crosstalk suppression can also be provided.

2.4.2 Transition Shape Targets

A key part of using AGC is achieving a particular transient shape in one of the V_{GS}, V_{DS} or I_D waveforms. Various transient shapes have been proposed by previous works - some of these have been derived for specific performance enhancements, whereas some waveform shapes are arrived at through an iterative process. This section will consider the main categories of shapes that have been demonstrated in the literature and the techniques which lead to their definition.

The work of [97] identifies sharp corners in the waveform shape as a source of high frequency content using selective filters and defines a waveform by graphically removing sharp features. This is consistent with with the model equations discussed earlier in section 2.3.1. Considering that the sharp features are a source of high frequency content, works such as [109] have proposed successive differentiation of the converter switching waveform by the Continuous Derivative Control Method (CDCM) to identify, and subsequently remove, the high frequency content.

Extending the work on the successive derivative method, several works go on to define the

case where Dirac functions are first encountered in the 3^{rd} derivative as an 'S-shaped' waveform [154, 155]. The S-shaped transition is shown to reduce the EMI generation of the switching waveforms while maintaining the switching loss.

In general, the more differentials that can be taken of a waveform before encountering Dirac functions, the lower the high-frequency spectral content of that waveform will be. The rectangular approximation of a converter switching waveform can only be differentiated once before encountering Dirac functions, whereas the S-shaped waveform discussed can be differentiated thrice. This general rule motivates finding suitable switching waveform shapes which can be differentiated as many times as possible, and it is shown that by convolving a Gaussian pulse with a rectangular wave, a switching waveform that is infinitely differentiable is produced [156, 157]. Such a waveform shape will have very low high frequency spectral content. This is demonstrated for the case of a simulated model in [156] where it is found that the limitation is the implementation of a gate driver that can track the reference waveform.

The works discussed so far have derived waveform targets mathematically. An alternative approach taken in other works is to create an objective function and allow an algorithm to iteratively refine the waveform shape to achieve a high performance switching transient. The works of [158] and [159] present methods in which the waveform shape is optimised by an iterative process. The work of [159] shows a technique for achieving on-line optimisation as the control signal is modified between one switching transient and the next. These techniques are advantageous as they are robust to changing conditions such as voltage and current, whereas using a predefined excitation as discussed previously may not be optimal under all conditions.

The work of [160] arrives at the switching waveform by first choosing frequency domain coefficient values so as to reduce the amplitude of selected frequencies. Transferring these back into the time domain creates the temporal waveform target.

A wide range of possible methods for defining or arriving at a particular excitation to use with the method of AGC have been explored here. There are many options for the target waveform shape, and when verifying the design of a shape the CDCM can be used as a tool for identification of high frequency components.

2.4.3 Technical Approaches

In addition to the wide range of technical benefits and the variety of waveform shapes used in the technique of AGC, there is an equally broad array of approaches to the physical implementation and the control of the gate drives used. Each of these designs have advantages and drawbacks and are each individually suited to certain applications. This section will review the state of the art in implementation of AGC gate drive circuits as well as control strategies for these.

2.4.3.1 Hardware Implementation Strategies

Most often in the field of electronics electrical engineers are accustomed to observing voltage waveforms, and as such this is a natural place to start when discussing AGC designs. Many works have proposed AGC gate drive designs which apply a controlled voltage waveform to the gate of the switching device [97, 161]. It is most commonly used in application to IGBTs. This strategy is most useful in relatively low speed systems as the parasitic inductance in the gate path after the controlled point makes accurate control of the actual gate voltage difficult at higher speeds. However, there is scope for manipulating the techniques presented to achieve AGC.

The difficulty in controlling voltage sourced AGC systems at high switching speeds is due to the parasitic inductance in the gate path. Figure 2.12 illustrates the typical connection of a gate driver to the gate of a switching device - this will inevitably include some parasitic inductance. A voltage source AGC system will be aiming to control the voltage on the gate of the switching device (V_A), however, at high switching speed the voltage drop (V_{LG}) will obscure the actual gate voltage from the closest possible measurement point (V_M).

Overcoming the issue with the parasitic gate inductance is the work of [146] - here the parasitic inductance in the gate path is used as part of the gate charging circuit. However the main focus of [146] is not the profiling of the transitions shapes, but increasing the switching speed. This work could be adapted to the more general case of shaping a voltage waveform at the gate of the switching device.

An alternative to the voltage source driver is the current source driver. These have been presented for application to Wide Band Gap semiconductor devices with both insulating [162]

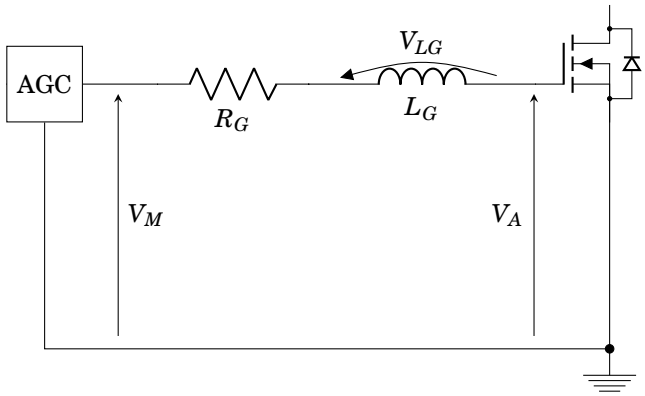

Figure 2.12: Active gate driver driving the gate of a device with parasitics in the connection

and non-insulating gates [131]. In the case of non-insulating-gate devices a current source driver is essential as a voltage-source drivers cannot typically sustain a high (>500 mA) output current. For the insulating-gate devices a current source driver will be able to overcome the changing dV/dt that occurs in voltage source drivers with a fixed gate resistance. Current source drivers are also effective at the higher switching speeds attainable by Wide Band Gap devices as the drivers can operate at high speeds - [162] demonstrates this with transient times of around 20 ns. They will also overcome the issue of measurement of the gate voltage by instead measuring the current into the gate. These drivers have been practically implemented in a number of ways including both traditional current source circuits and switched source designs [163].

A more complex technique for controlling the gate of the switching device is to use a variable impedance source to drive the gate. These will typically involve a network of switchable resistances with some fixed voltage supply. A very fast logic system is required to switch these resistances, so several works rely on the use of an Application Specific Integrated Circuit (ASIC) to perform this task [130, 145]. The work of [152] however, overcomes the need for a fast controller by calculating the switch timings in advance. Designs involving an ASIC typically implement the impedances on chip, whereas it is possible to implement these discretely as in [136, 152]. Controlled impedance drivers have the advantage of being able to operate at very high speeds (several GHz bandwidth), and presently are the only drivers that have been integrated.

The final drive design that will be considered is optically coupled designs. The work of [164] has demonstrated that it is possible to create Wide Band Gap semiconductor devices which are

controlled through exposure to light. They have also demonstrated in this work that the switching speed can be modulated through manipulation of the light intensity, though they do not specifically attempt to shape the waveform transitions. The works of [165] and [166] present optical gate drivers that have the advantage of exceptionally good isolation which is of value in the design of high voltage converters. [165] shows the output stage of the driver having switched resistances similar the that discussed previously. [166] has specifically shown that it is possible to modulate the switching transient of the device. This type of driver is very promising for allowing the use of AGC as well as providing fantastic galvanic isolation, though the switching speed achieved is only around 500 ns at present whereas SiC has typical transition times of several to tens of ns.

Considering the range of hardware implementation strategies discussed here, careful consideration should be given to the design of gate drivers for application of AGC to Wide Band Gap devices. Voltage source drivers are the most basic designs to create, though there are significant advantages to other techniques. Current source drivers function well at higher switching speeds which would make them a promising candidate in application to Wide Band Gap switching devices.

2.4.3.2 Control Strategies

Existing literature shows that the control strategy employed by an AGC system can take one of several forms. The particular strategies that can be used will be considered in this section.

Possibly the most common approach to AGC is to use an open-loop controller. Here the target drive profile is pre-determined by the designer and the driver simply applies this to the gate of the device. This type of control has the benefit of being very simple to implement, though it is not robust to changing conditions and so is only really useful in an experimental set-up under fixed operating conditions.

A more practically useful approach is a closed-loop design. Here a signal is measured and fed back into the system to ensure that the target profile is met. This kind of driver can compensate for changing conditions, though the complexity and circuit speed required is very high. An example of such a driver is presented in [135] and a photo of the physical implementation of this

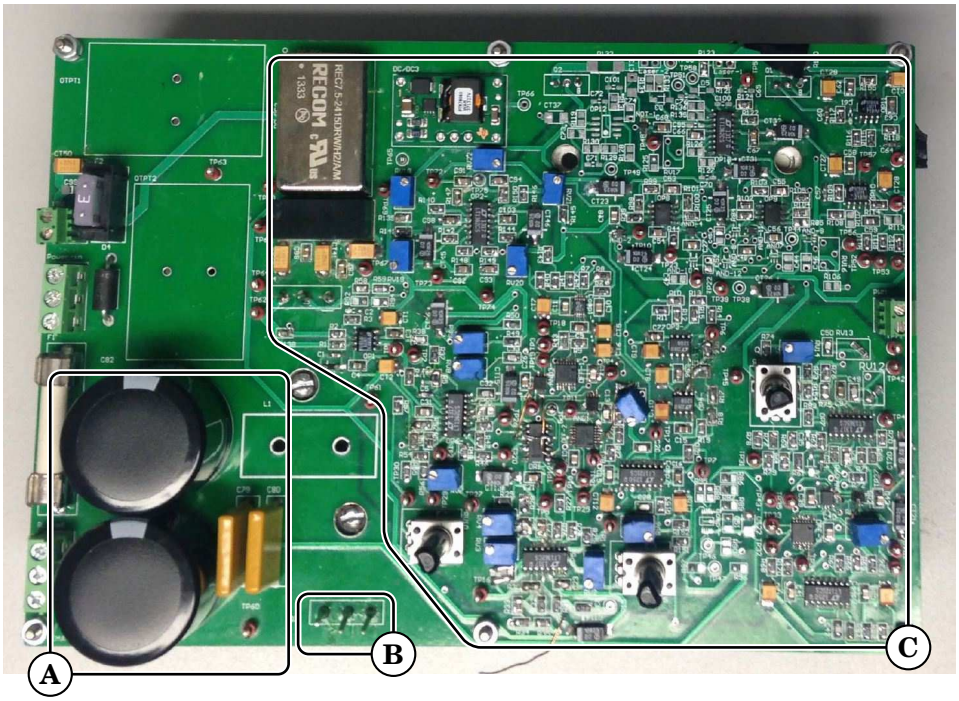

Figure 2.13: Photo of a closed-loop control gate driver implementation. (A) - The DC-link capacitance. (B) - The switching device. (C) - The active gate driver. Reproduced from [135]

driver is reproduced in fig. 2.13.

A compromise between the closed-loop and open-loop gate drive designs is presented in [159]. Here the loop is closed by altering the switching profile between transitions as opposed to during the transition. This design does not require a feedback network of such extremely high bandwidth, but still reaches a very good performance point in very few transients.

It is likely that any initial use of the AGC technique will use the open-loop control design as this is the most basic design to implement in an experimental set-up. Consideration of the closed- and semi-closed-loop designs that have been presented indicates that when creating a closed-loop gate drive, a high-speed feedback network may not actually be required.

2.4.4 Summary

AGC has been shown here to be able to control a wide range of performance metrics. These extend from the common performance metrics of EMI generation and switching loss (and their trade-off), to less common goals such as the thermal profile balancing of multiple switching

devices on a substrate.

Though the widest range of literature on AGC focusses on application to IGBTs, there are existing works showing that the technique can be applied to a wide range of switching device technologies, including Wide Band Gap devices and MOSFETs.

In addition to the variety of devices that AGC can be applied to, there is an equally wide variety of waveform shapes that can be used as the target of the shaping. There is no definitive 'best' waveform shape defined at present as each shape that has been defined offers different performance trade-offs. The designer of an AGC system must still choose a waveform shape based on the application.

Implementation of AGC drivers can take a number of forms and the existing literature has shown that similar performance goals can be achieved with any of the strategies considered. The physical implementation of an active gate driver will need to balance the needs of the control system and the tolerable design complexity to ensure that its performance is optimised.

The existing literature that has been considered in this section has shown that the technique of AGC has a wide range of application and utility in controlling switching devices. The wide range of control and the applicability to Wide Band Gap devices makes this a useful tool for consideration in the control of the influence of parasitic elements on the performance of a power converter.

2.5 Limitations of The Literature and Research Opportunities

2.5.1 Wide Band Gap Semiconductors

Wide band gap semiconductor technology is beginning to reach maturity and is being adopted into a wider range of designs. This technology has demonstrated that it can offer far superior performance to traditional Si based devices with the current state-of-the-art converters demonstrating ultra-high performance in a range of metrics. Detailed and accurate models of converters utilising Wide Band Gap devices have been demonstrated illustrating the requirement for attention to detail when using this technology.

The literature to date has presented works that seek to address the new challenges pre-

sented by Wide Band Gap semiconductor devices. However, these works are still limited, and research into methods for enabling ultra-high performance converters utilising these devices is still an area requiring further work.

2.5.2 Parasitic Circuit Elements

A review of parasitic elements of a power converter has been undertaken and has illustrated the extremely broad range of elements that must be considered in the context of Wide Band Gap devices. The issues with connection of power converters to loads via long cables or to loads with other significant parasitic elements has been discussed finding that there is significant art in the mitigation of these issues. The measurement of power converter switching waveforms in the presence of parasitics has also been considered, finding that the measurement process must take account of the sensitivity of the devices to the probe parasitics and interpretation of measured results must consider their influence on the observed waveforms.

The existing literature on parasitic elements shows in some details how aspects of the design of a power converter can contribute to parasitic elements with which the switching devices will interact. It has also been shown that with the adoption of Wide Band Gap semiconductor devices these parasitic elements become more crucial to determining the converter's performance. Further work is required in developing strategies for mitigating these effects as these are essential for enabling ultra-high performance power conversion.

2.5.3 Electromagnetic Interference

The high-speed switching transitions that are present in power electronic converters have been identified as a significant source of both radiated and conducted EMI. The review of literature in this area emphasises the importance of methods to control its generation and emission. There are a wide range of models that enable the analysis of the switching waveforms for prediction of the EMI and the difficulty in the classic trade-off between switching loss and EMI has been discussed.

At present, there is limited existing literature addressing the trade-off between switching loss and EMI generation as most techniques will mitigate only one issue as opposed to both

simultaneously. This topic is of key importance to enabling ultra-high performance power conversion with Wide Band Gap switching devices. In particular, methods for improving the performance in both of the metrics are lacking in present literature as both of these will need to be improved without compromise to the other.

A wide range of models for predicting the EMI generation of power converter switching waveforms have been presented. These models are primarily useful for analysis and prediction of trapezoidal or similar simplified waveform shapes. Some of the methods investigated consider the case of smoother waveform shapes, though few of the techniques presented can identify the temporal source of high frequency content.

A common task in the evaluation of a power converters performance is quantification of the spectral performance. The techniques for producing an EMI metric presented in the literature to date are not currently robust. This is in the sense that a spike at one particular frequency may effect the metric to a great degree. The development of a metric that allows the quick, easy, and robust comparison of the EMI performance of several converter designs is a key area of research that will be considered.

2.5.4 Active Gate Control

A review of AGC has illustrated the advantages of its use and the range of device technologies that it can be applied to. This review has also considered the range of target waveform shapes that have been presented in the existing literature and discussed the process by which these have been arrived at. The variety of hardware implementations presented in the literature so far gives many options for the design of an AGC system.

AGC has been shown to be a powerful tool in the field of power electronics. However, there is currently very limited work considering the application of this technique to the mitigation of the effects of parasitic elements. There is still a large scope for reviewing the capabilities of current AGC designs and evaluating the potential for parasitic mitigation.

CHAPTER 3

Analysis of the Performance of Power Converters Under the Influence of Parasitic Elements

It is well established that there is not such a thing as a perfect electrical component - it is inevitable that the physical implementation of any component will introduce unintended 'parasitic' elements. Resistors, capacitors, inductors, and wires all have properties of resistance, capacitance, and inductance, despite this not necessarily being part of their design. Section 2.2 has discussed the definition, manifestation, and mitigation of these elements in detail.

This chapter will explore the influence of parasitic elements on a hard switched SiC power converter by presenting a simulation model which can be used for sensitivity analysis. This simulation model will be developed through parasitic parameter extraction from the hardware set-up presented in section 1.2. The outcomes of the sensitivity analysis can then be used to propose parasitic mitigating strategies.

3.1 Extraction of System Parasitics

To enable effective work with the test system presented in section 1.2 it is important to understand the parasitic elements that are introduced through the design of the PCB and the choice of

components. Knowledge of these values will enable the creation of accurate simulation systems, elucidate the influence of probe configurations, and enable effective investigation of performance enhancing techniques.

As has been discussed in section 2.2, there are many aspects of a circuit which will introduce parasitics. The following sources will be investigated in detail:

- Device parasitics
- PCB parasitics
- Load and cable parasitics
- Probe parasitics and influences

Each source of parasitic components is investigated here to determine the contribution to the circuit switching performance. This will in turn allow more accurate simulation of the basic converter system, and investigation into mitigating techniques.

3.1.1 Device Parasitics

The first elements of the system that will be considered are the switching devices themselves. These will introduce significant parasitic elements into the system when they are transitioning, conducting, and when they are switched off.

While the switching device is switched on, it will present a fixed resistance in the current path. Information on this value is easily obtained from the device manufacturer's data-sheet [167]. In the case of the devices used in this work the channel resistance when turned on is 80 mΩ. In practice, the channel resistance of the switching device contributes to the on-state losses of the converter as well as damping the impulse response.

During the switching transition of the converter the presence of the co-device in the leg will present several readily observable influences on the device which is transitioning. Considering the turn-on of the top switching device with the lower switching device in the off state, a current overshoot will be observed. Referring to fig. 2.6 it is expected that a proportion of this current will be supplied to the Equivalent Parallel Capacitance of the load, some to the C_{OSS} of the

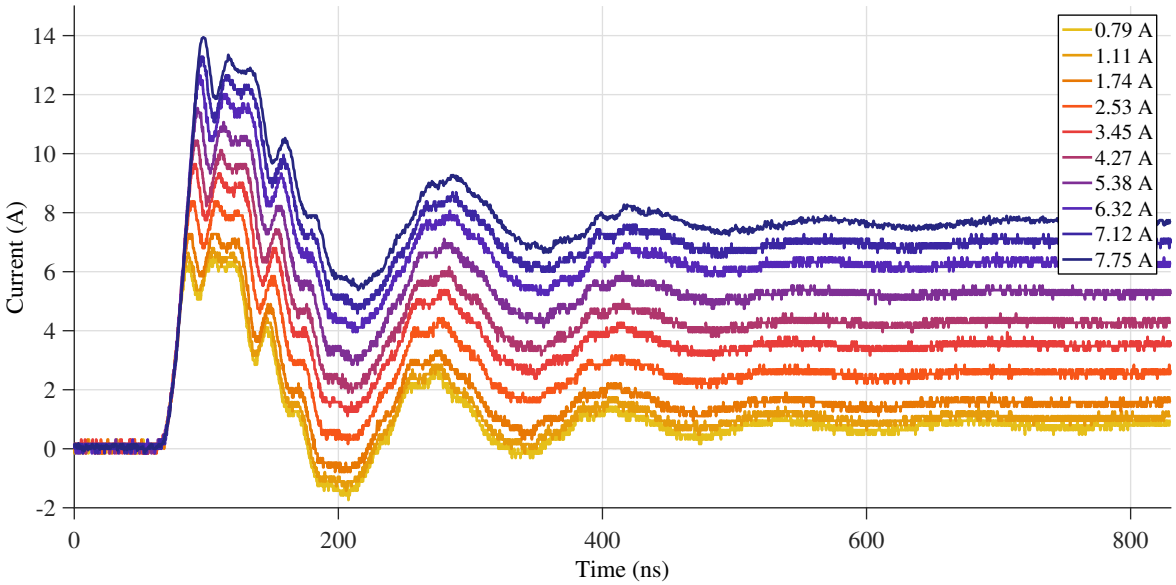

Figure 3.1: Top device turn-on current waveforms for varying output current level showing increased overshoot with increasing current level

lower switching device, some to the Equivalent Parallel Capacitance of the PCB, and some will be supplied to satisfy the RRC of the lower diode.

As the RRC should be proportional to the current in the diode before turn-off, this element can be eliminated by switching the top device on with no current being output by the converter (A full description of the zero current switching technique can be found in appendix A). Figure 3.1 shows how the current waveform for the top switching device varies with changing output current - as the output current is reduced the overshoot is reduced. The overshoot was measured and plotted against the commutating current in fig. 3.2 where the variation in the overshoot can be seen more clearly.

These results allow the estimation of the overshoot current due to elements other than the diode RRC. If the trend of fig. 3.2 is extended to $I_D = 0$ the overshoot can be estimated as 5.4 A. Noting the scale of the y-axis in this figure is very fine, it can be concluded that the effect of the RRC is relatively small, and that this overshoot is primarily caused by other elements. From the device data-sheet the C_{OSS} of the device is expected to be 80 pF. With R_G set to 24 Ω the switching speed is 15.6 kV/µs (table 1.2). Using $I = C\frac{dV}{dt}$ the expected current would be 0.96 A due to this capacitance. The results presented here and the data-sheet information will help to

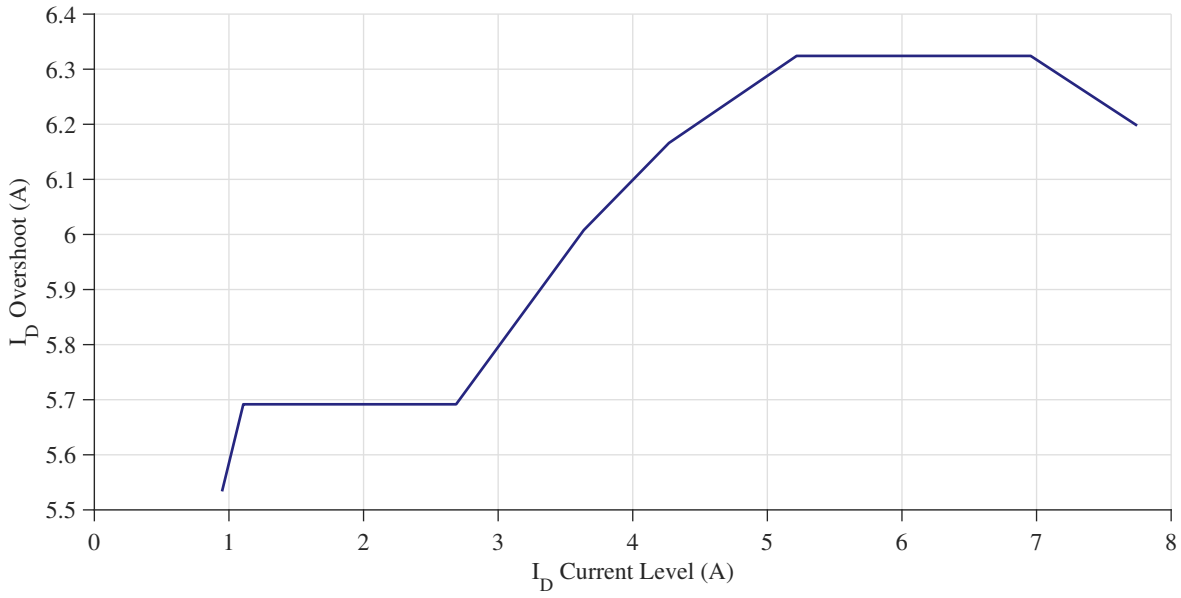

Figure 3.2: Illustration of current overshoot against output current for the top switching device, showing a trend for increasing overshoot with output current

identify which elements contribute to the overshoot.

During the transition period of the devices, the dynamic switching characteristics will be influenced by the reactive elements around the device. In particular, the stray inductances that are presented by the device packages and connections will alter the switching performance [46]. The legs of the device package will introduce inductance into the drain, source, and gate paths. The source inductance presents a challenging issue as this is common to the gate loop. To mitigate this, some manufacturers supply devices with a Kelvin connection for the gate to remove some of the common source inductance.

A Kelvin connection (or 4-port connection) is a measurement technique which decouples the drive and sense wires when measuring a component value. Figure 3.3 illustrates a Kelvin connection for measuring an impedance - here a current is applied to the main driving connections and the voltage drop across the impedance measured on the sense connections. This avoids any error due to voltage drop in the main drive connections as there will be close to zero current in the sense connections.

In the context of a MOSFET the same technique can be used to mitigate any voltage drop in the source connection. Figure 3.4 illustrates a MOSFET package with its parasitic elements.

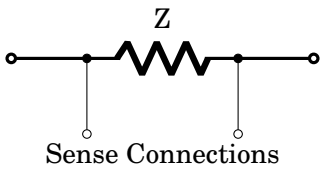

Figure 3.3: Illustration of Kelvin (or 4-port) connection for measuring and impedance

This also illustrates the placement of an additional source connection S_2. The second connection is used for connection of the gate driver while the first source connection is used for connection of the main switching circuit. In this way the main switching current is transferred via the first source connection where it will cause a voltage drop across L_{leg}. This voltage drop will not be seen at the gate drive source connection (S_2), mitigating the impact of the source inductance.

3.1.2 PCB Parasitics

The geometrical arrangement of conductors on the PCB will introduce several parasitic networks into the system - the adjacent layers will act as capacitance, and the length of the conductors will act as inductors. It is also found that the gaps between adjacent pads of a device footprint will contribute capacitance. These parasitic values are extracted by first measuring between the various terminals of the board with an impedance analyser while all the components are removed. The results of this are illustrated in fig. 3.5. Terminals (A) and (C) are the connections for the DC-link, and (B) is the converter midpoint. The resolution of the data presented in fig. 3.5 is limited by the frequency domain resolution of the analyser, though it still allows for the resonant frequencies to be determined to within 5 kHz.

An equivalent circuit is then assumed between each terminal. Based on the geometry (an open circuit between each node) a serial LCR network is assumed to exist between each of the terminals. A pattern-search algorithm was then used to adjust these 9 parameters (3 networks of 3 components) to achieve the closest possible approximation of the measured impedances between each terminal. The search was seeded with estimated component values and after 2135 iterations a local minimum point is found. Figure 3.6 illustrates the network that was assumed to be present between the terminals and the values that were found by the search. Figure 3.7 compares the measured impedances with the impedance of the estimated network.

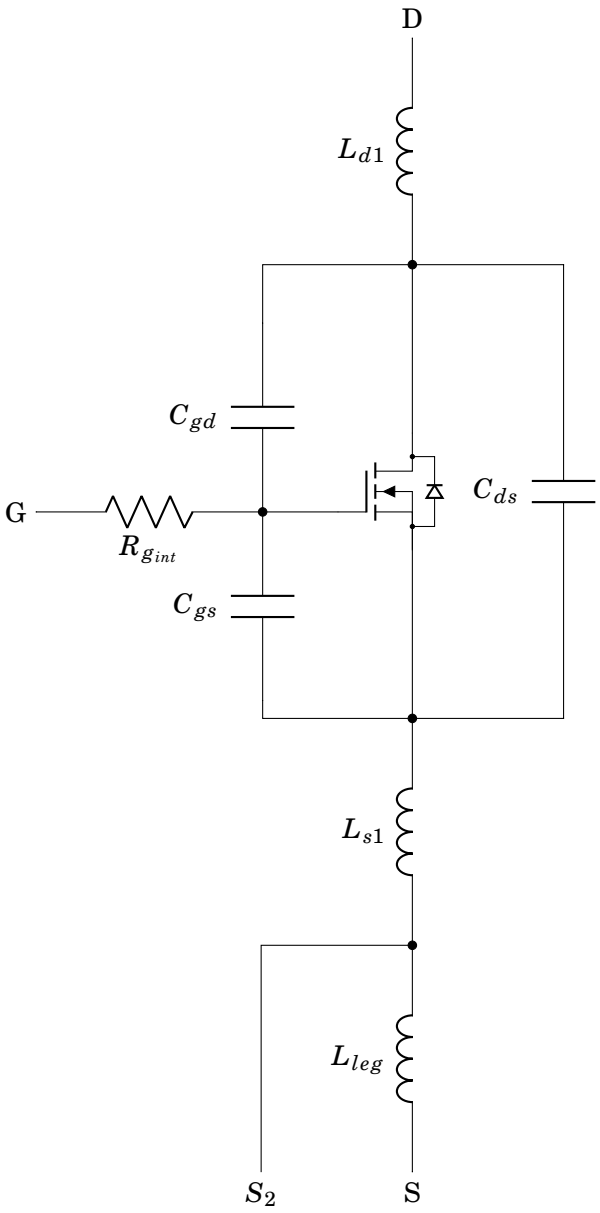

Figure 3.4: Illustration of a MOSFET with a Kelvin source connection

It is notable that in fig. 3.7 the measured impedances only show one resonance point, whereas the estimated impedances exbibit two. The form of the assumed network in fig. 3.6 dictates that there should be two resonant frequencies which does not align with observations. The fit of the assumed network is satisfactory in the locations and magnitudes of the resonance frequencies which allows this to be used in investigations, but further work could investigate other models for this network. Ideally, using 3D parameter extraction as discussed in [30] would produce a

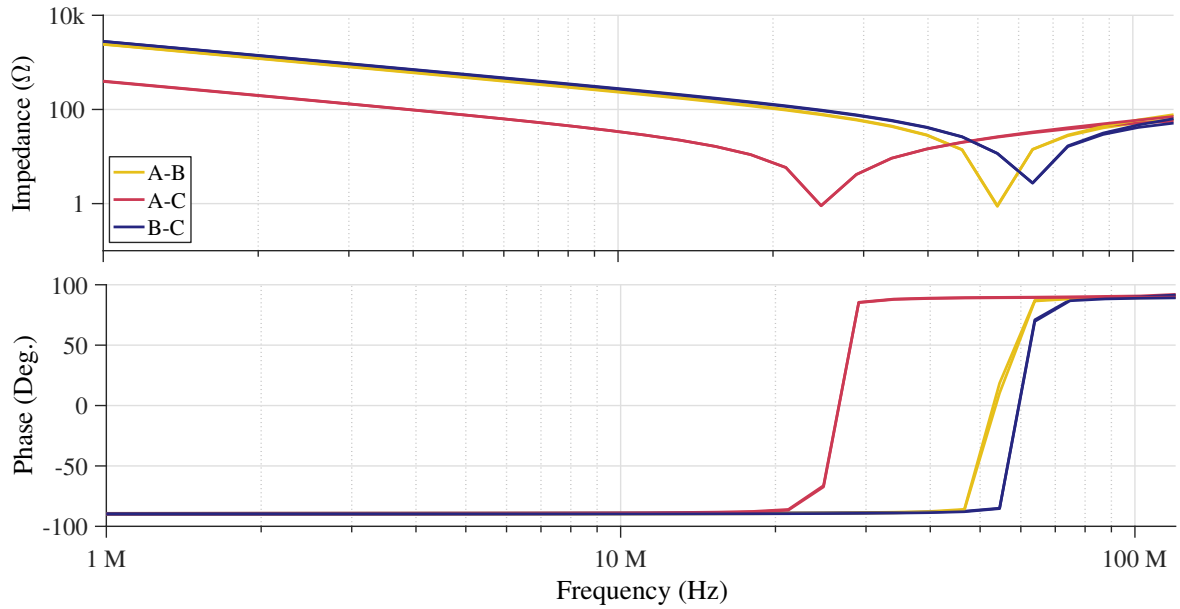

Figure 3.5: Measured impedance between the main PCB power terminals. Terminals (A) and (C) are the connections for the DC-link, and (B) is the converter midpoint. The resolution of the data is limited by the equipment used for capture, hence the unrealistic sharp edges in the phase response.

more accurate model, however, this requires specialised software, and the method used here produces a reasonable approximation.

Additionally, the inductance of the switching loop can be estimated by first observing the voltage 'droop' at the beginning of the switching transient during the current transition, an example of which is annotated in fig. 1.14. This inductance limits the rate-of-change of current during a switching transition and is comprised of all the inductances from the DC-link capacitance to the switching device, i.e. $L_{DC}+2\times L_{CS}$ from fig. 2.6. Measuring the initial device voltage droop at the beginning of a transition and the rate of change of current in the device, the DC-link inductance can be estimated. Table 3.1 presents these, and the estimated DC-link inductance for several values of R_G.

3.1.3 Load Parasitics

The load used in this work is a series RL load as would be presented by a motor load. The nominal values of the components are 10 Ω and 40 mH. However, another significant parasitic

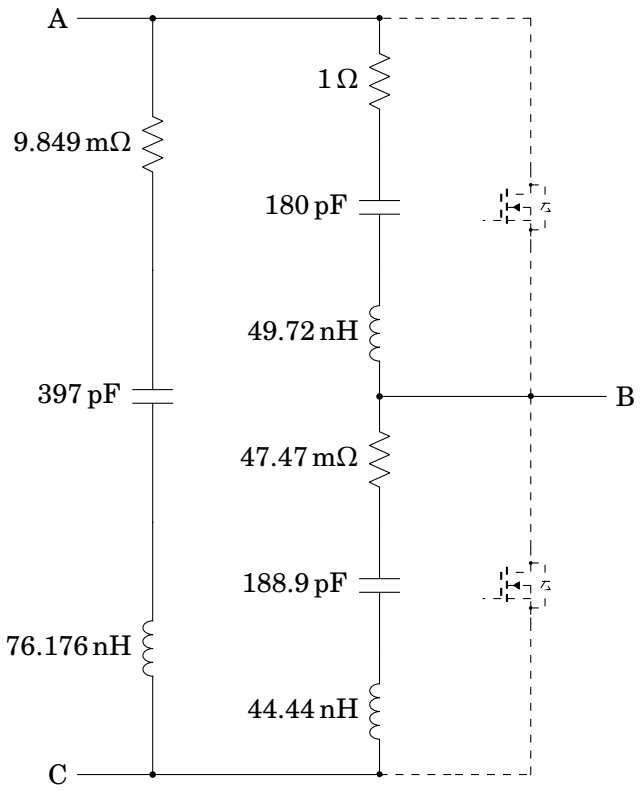

Figure 3.6: Illustration of the equivalent circuit presented between each of the main PCB power terminals. Dashed components are removed from the PCB for testing the PCB parasitics

Table 3.1: Measurement of voltage droop and dI/dt during switching for estimation of loop inductance

R_G (Ω)	Droop (V)	dI/dt ($A/\mu s$)	Approximate Inductance (nH)
100	26	248	104
51	33	387	85
24	44	593	74
12	62	866	72
6.2	92	1,250	74

element is the Equivalent Parallel Capacitance of the load. This is investigated using two methods - the first is connection of the load to an impedance analyser, and the second is to switch the top device with and without the load connected and observe the current waveform.

The investigations in this section will make use of double pulse testing as well as zero current switching. A full description of this process and the parameters associated with it are discussed in appendix A.

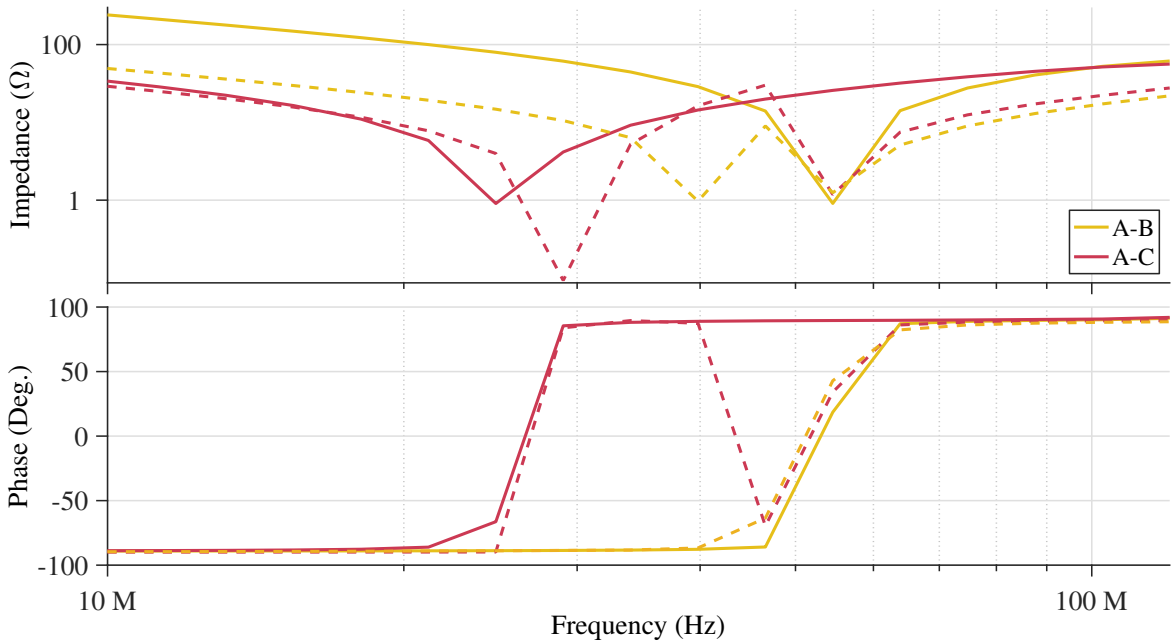

Figure 3.7: Comparison of the measured (solid line) terminal-to-terminal impedance with the estimated (dashed line) impedance from parameter extraction. Only the traces for the A-B and A-C branches are shown as the A-B and B-C branches have similar responses.

Figure 3.8 shows a reduction in the current in the top switching device when the load is removed from the system. This indicates that the load contributes a significant parasitic capacitance, which will lead to increased current overshoot in the switching device, and hence increased switching loss. It is also interesting to note the significant reduction in ringing after switching which results from removal of the load. This will have implications for the EM performance of the converter.

Figure 3.9 shows the load impedance as measured with an impedance analyser. Also illustrated is the response of the best-fit equivalent circuit. The equivalent circuit is an LCR network with series R and L, and a parallel C. The values of these components are $R = 11.2\,\Omega$, $C = 145\,\text{pF}$ and $L = 45.1\,\text{mH}$.

The difference in charge shown in fig. 3.8 between the load being connected and disconnected is 204 nC. With the 600 V DC-link voltage, this corresponds to a fixed capacitance of 340 pF - around twice that of that measured with the impedance analyser. This demonstrates a difficulty in measurement - as the impedance analyser is not able to bias the load to the same working

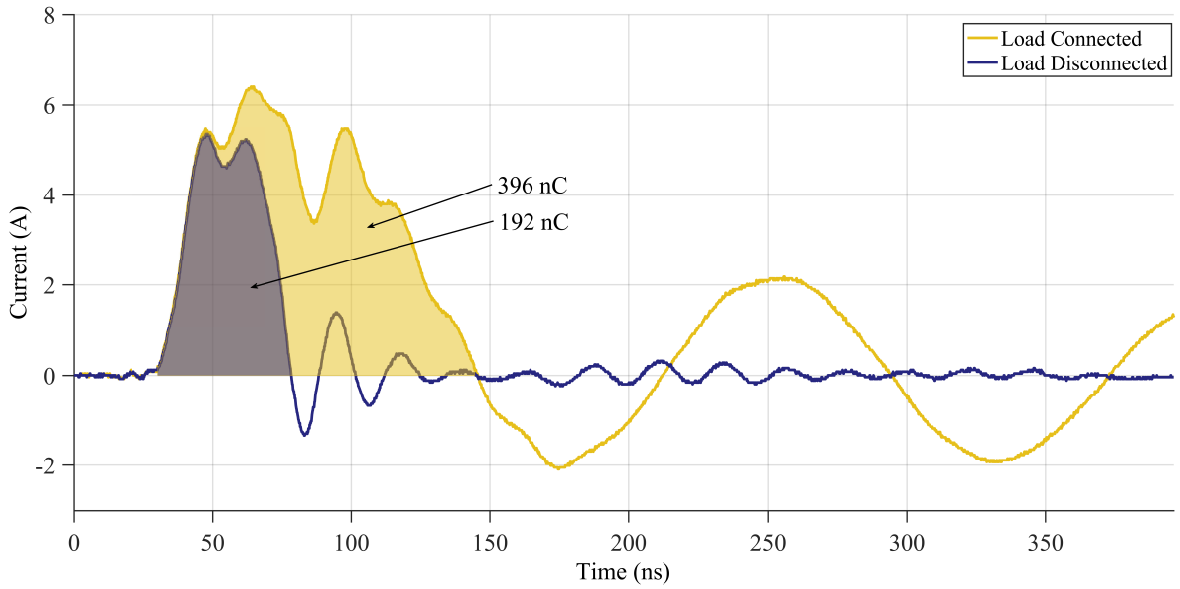

Figure 3.8: Measured current into the load under zero current switching conditions showing the increase in current when the load is connected

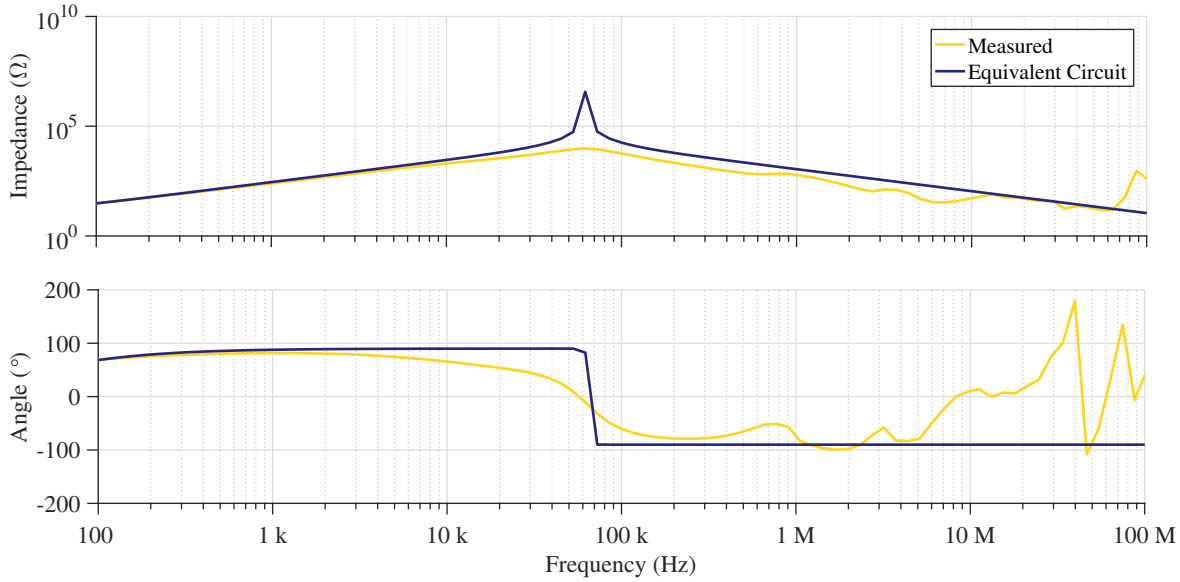

Figure 3.9: Load impedance as measured with an impedance analyser and the response of a fitted equivalent circuit.

voltage as the power converter it may not be able to accurately measure the working capacitance. To increase the accuracy of the capacitance measurement it is possible to create a test fixture for the impedance analyser which allows high biasing to be used. Creating such a fixture is

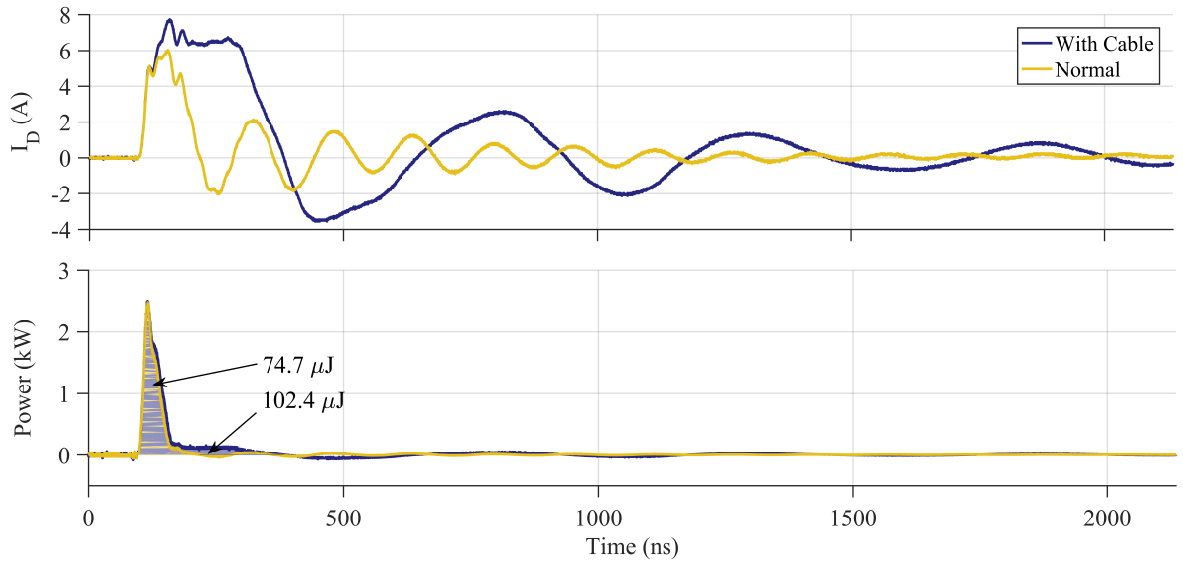

Figure 3.10: Comparison of the top switching device current overshoot and switching loss with and without a cable connected showing the large overshoot increase and the energy increase

not within the scope of this work provided that this limitation is is appreciated when analysing results derived from these measurements.

In addition to the parasitics presented by the load, the presence of a long cable connecting the converter and the load may introduce more. The arrangement of the conductors in the cable will contribute a distributed RLC system which will affect both the current overshoot at the converter, and the voltage overshoot at the load [65, 66]. This will lead to increased switching loss as well as degradation of the load windings. Figure 3.10 shows experimental results from the DPT test rig in which the load is connected either directly to the converter, or through a 2 m cable. This shows that the cable contributes to the device overshoot current, which will increase the switching loss.

3.1.4 Probe Parasitics

Here, the probes used to collect the temporal data for the experiments are put under scrutiny. There are three aspects that are of importance - the resilience of the current probe to dV/dt induced noise, the effect of the tip capacitance of the differential voltage probe, and the insertion impedance of the current probe.

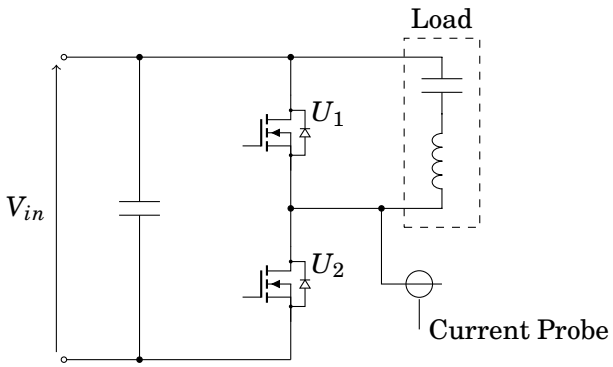

Figure 3.11: Illustration of the connection of the current clamp probe to a stub of wire

It is known from information presented in [75] that the current probe employed in these experiments will contribute an insertion impedance as shown in fig. 2.7. At low frequencies this impedance will not be significant in comparison to the other impedances presented around the circuit, though at higher frequencies the impedance is large, and this could attenuate high frequency content in the measured signal such as ringing.

To investigate the effect of dV/dt on the current probe, it was connected to a stub of wire at the midpoint of the converter as illustrated by fig. 3.11. This meant that it would have the same dV/dt incident upon it as when measuring I_D for the lower switching devices, but would not actually have any current flowing through it. Figure 3.12 shows the apparent current induced.

From these results a peak of 71.2 mA is observed, this is a false reading as no current could be flowing into the stub of wire and so this signal must be entirely induced by the dV/dt. This is an important result, as it indicates an inaccuracy that could occur when measuring the current into the switching devices.

To mitigate the influence of the dV/dt induced noise all following experimentation is set-up such that the current probe is connected to a node which does not have a high dV/dt present. For most of the DPTs in this work the set-up takes the form presented in fig. 3.13. Here the probe still measures the current through the top switching device but it is not exposed to the high dV/dt as the node it is connected to is also grounded.

The current flowing into the differential voltage probe connected to the midpoint of the circuit is also placed under scrutiny. This is investigated by connecting the current probe to one of

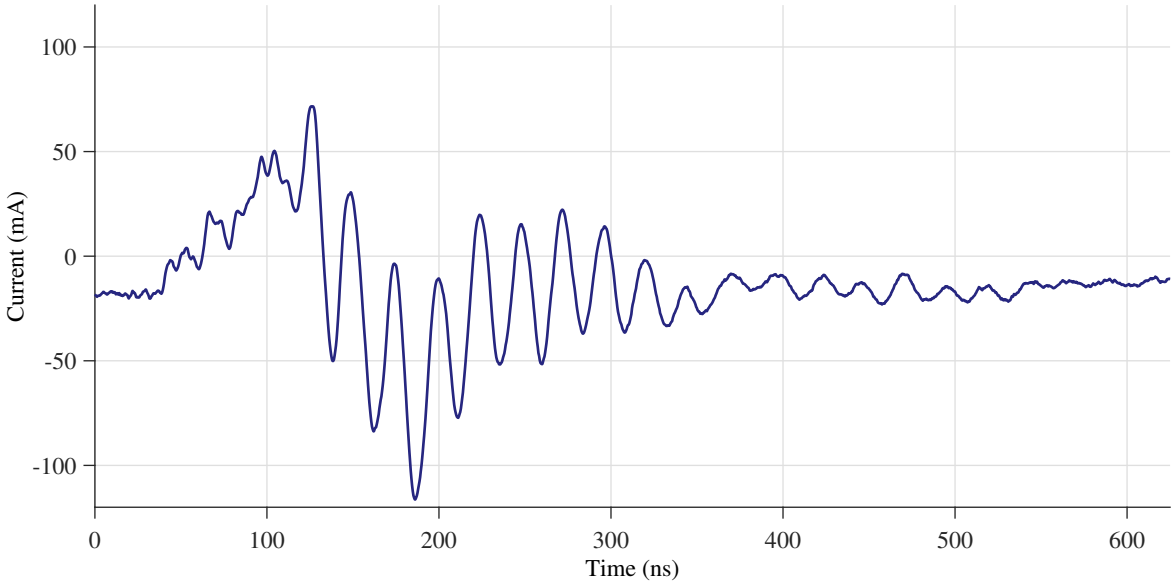

Figure 3.12: Measured current due to dV/dt induced noise. The ringing frequency is 41.2 MHz

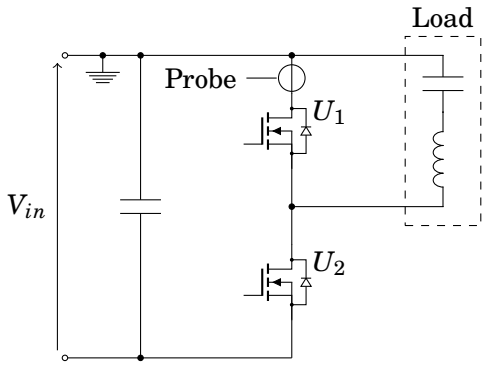

Figure 3.13: Illustration of the connection of the current clamp probe to a node in the circuit that is also grounded to prevent dV/dt induced noise

its test leads. The results of doing so are shown in fig. 3.14.

A peak of 527 mA is measured into the voltage probe. However, as the previous experiment showed a peak of 71.2 mA just due to the dV/dt induced noise there could be up-to 13 % error in this reading.

A model for the passive probe is produced based on the less detailed models presented in [71, 72, 168–170] with the component information presented by the manufacturer in [171]. Likewise, a model for the differential voltage probe is constructed using the provided manufacturers information [172]. These models are illustrated in fig. 3.15.

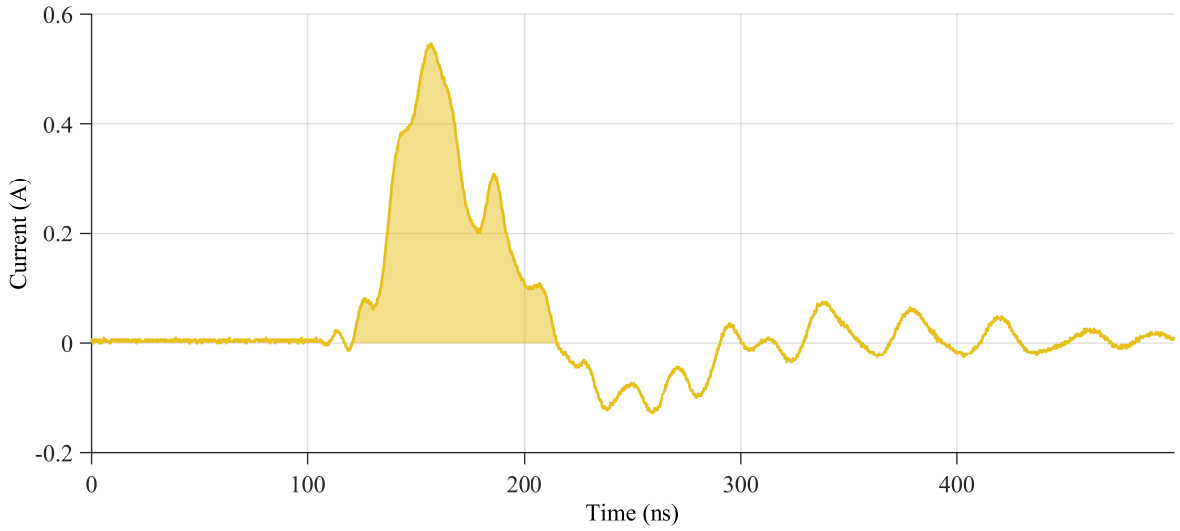

Figure 3.14: Measured current into one of the connections of the differential voltage probe

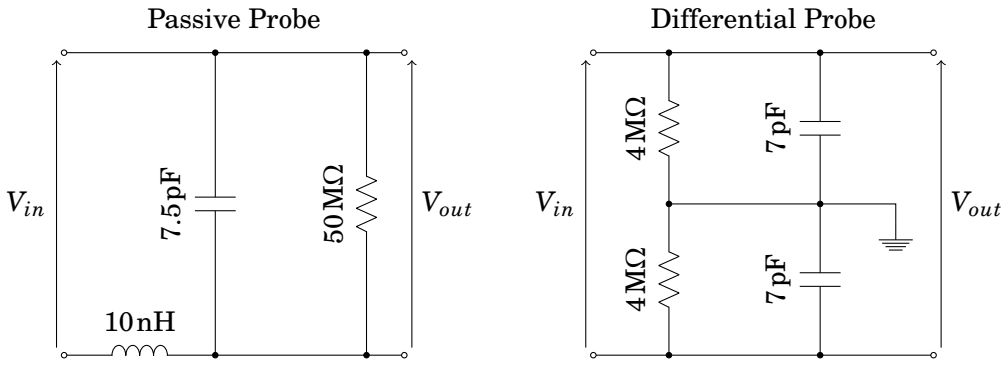

Figure 3.15: The equivalent circuit of each of the types of voltage probe used in this work. V_{in} is the voltage that the probe is connected to in circuit and V_{out} is the voltage that would actually be observed.

The results here demonstrate both the influence that the probes connected to the circuit can have, and the problems they can cause when analysis is performed on the data. These imperfections in measurement mean that a significant amount of current overshoot may be observed on waveforms despite only a small amount being present.

To mitigate the impact of the probes on the measurements the models for the probes will be incorporated into simulation models. When taking measurements current probes will be separated from high dV/dt nodes and passive voltage probes used instead of differential probes where possible. If higher fidelity measurements are required the differential Rogowski coil de-

sign discussed in [80] can be utilised.

3.2 Simulation

3.2.1 Design and Validation of Simulation Model

To investigate the elements that contribute to the current overshoot during turn-on in greater detail and to investigate the ringing after switching in a more thorough manner a simulation model is created. This will allow for investigation of the signal characteristics without introducing probes which influence the behaviour of the system. Use of a simulation model also enables the automated sweeping of component values, which helps to reveal their influence on the system.

For accurate time domain simulation of the system the model requires a high level of detail. The investigations presented in section 3.1 are used to inform the values of the parasitic elements included in the system. An impedance analyser was used to produce models for the following PCB components:

- The electrolytic DC-link capacitors
- The large plastic DC-link capacitors
- The small plastic DC-link capacitor
- The PCB traces
- The load elements
- The snubber inductor

The simulation model is based in the LTspiceIV simulation package. This is chosen because the device manufactures (CREE) supply a spice model for their devices in this format which has been investigated in [173]. This report finds that the device modes supplied by ROHM include the influence of the most parasitic elements, however these models are not readily available. As such the CREE device models are selected for use in this work. The full simulation model is shown in fig. 3.16.

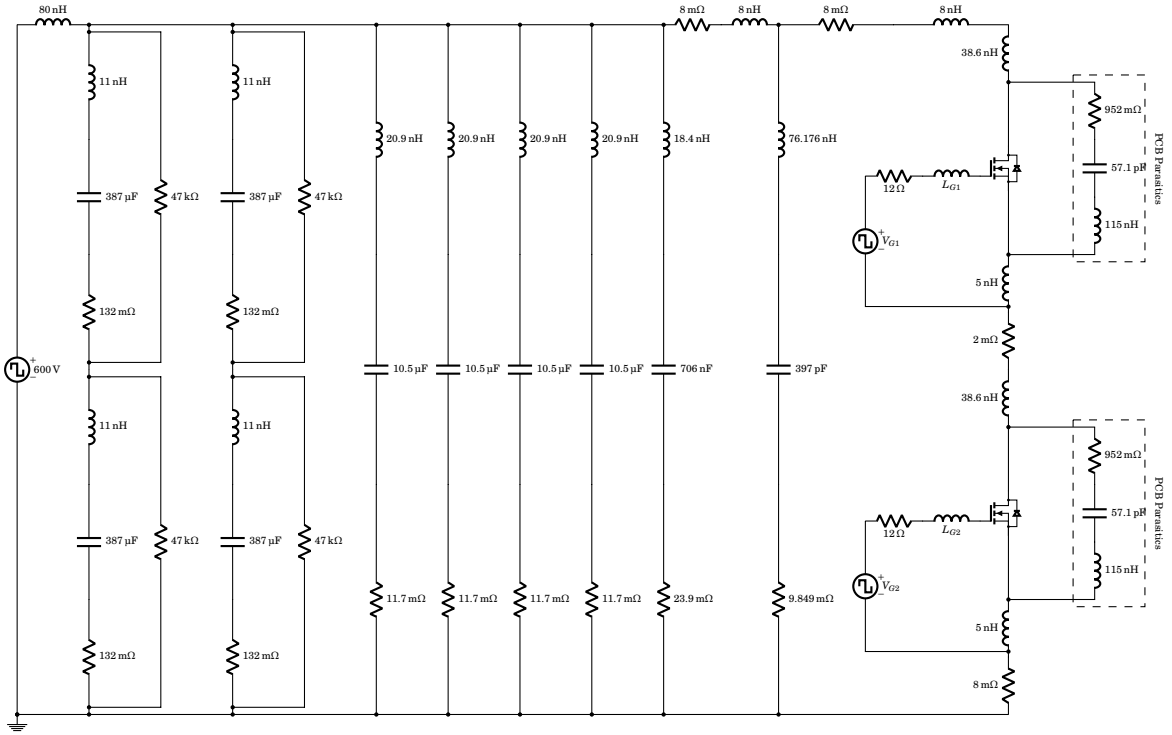

Figure 3.16: The simulation circuit set up in LTSpice showing the relative complexity required to achieve good agreement with the experimental system. Each of the components of the PCB has been measured with an impedance analyser and the equivalent circuit of that component is included. The PCB parasitics discussed in section 3.1.2 are also included.

To allow comparison with experimental results, the effect of the current and voltage probes on the circuit are also modelled. The models for the probes that were illustrated in fig. 3.15 are included in the simulation model when taking measurements.

Figure 3.17 compares the device current waveforms from the simulation setup with those from the experimental system. These results show that the simulation system is able to achieve a useful level of accuracy - the key characteristics of the waveform shapes are reproduced in the simulation system, though they are not quite faithful to those from the experimental system. The inaccuracy could likely be due to the mutual field couplings that will be present between elements such as the PCB traces - as each trace impedance was measured independently these mutual couplings are not accounted for. 3D analysis of the board layout as discussed in section 2.2.5 could be used to improve this accuracy.

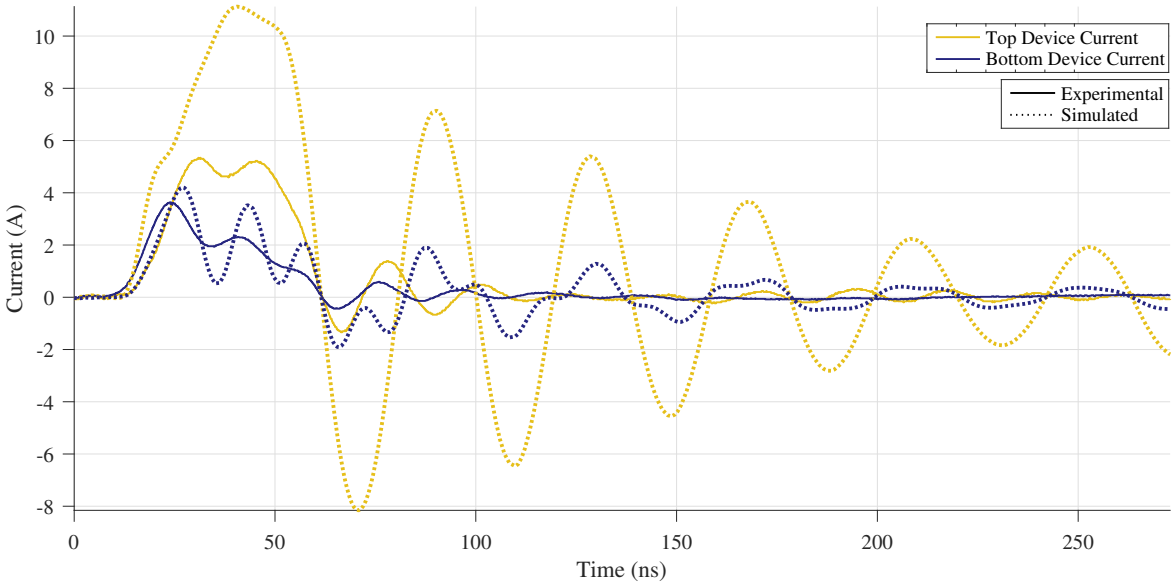

Figure 3.17: Comparison of the simulated and experimental results showing the inaccuracy in prediction of ringing frequency

This simulation model can now be used to test modifications to the circuit, and test the sensitivity of the system to variations in the parasitic elements.

3.2.2 Sensitivity Analysis

To provide a more detailed understanding of the influence the parasitic elements have on the switching waveforms for a converter a set of parametric sweeps was performed. In each test one parameter was scaled from its measured value and the set of switching waveforms captured. A zero current DPT test was performed with the top device ($U1$) switching and the current into the drain of each device at turn-on measured (I_{D1} top device, I_{D2} bottom device).

The parameters that were swept, and the ranges through which they were swept were as detailed in table 3.2. It was anticipated that the sensitivity to a change in the inductance would be greater, so a range of 0.5 to 2 was chosen for these, while capacitances were swept the larger range 0.1 to 10. The results of each of these parameter sweeps are included in figs. 3.18 to 3.23.

The comparison of the simulation and experimental results in fig. 3.17 shows the frequency of the simulation does not match that of the experimental results. To improve the match between the simulation and experiment the parasitic values in the simulation can be adjusted using

Table 3.2: Details of swept parameters and their sweep ranges

Parameter Symbol	Parameter Description	Sweep Range
C_{pp}	Capacitance between pads of the switching device footprint	$\times 0.1$ *to* $\times 10$
L_{D1}	Top device parasitic drain inductance	$\times 0.5$ *to* $\times 2$
L_{D2}	Bottom device parasitic drain inductance	$\times 0.5$ *to* $\times 2$
L_{S1}	Top device parasitic source inductance	$\times 0.5$ *to* $\times 2$
L_{S2}	Bottom device parasitic source inductance	$\times 0.5$ *to* $\times 2$
ESR	The ESR of the DC-link capacitors	$\times 0.1$ *to* $\times 10$

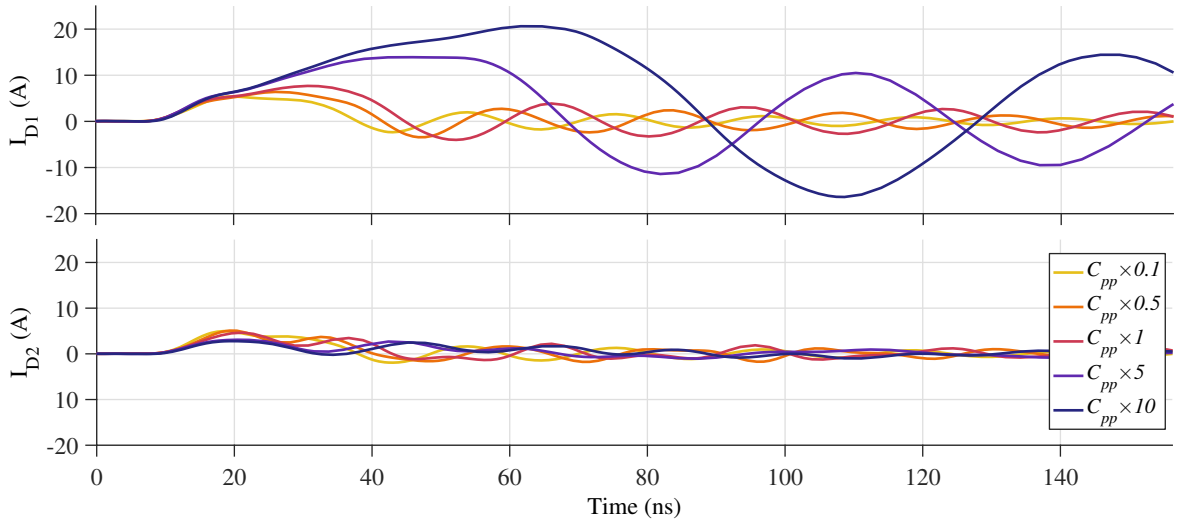

Figure 3.18: Variation in the switching device current waveforms for varying values of C_{pp}

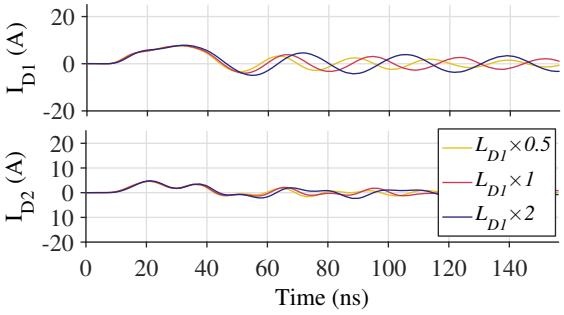

Figure 3.19: Variation in the switching device current waveforms for varying values of the top device drain inductance

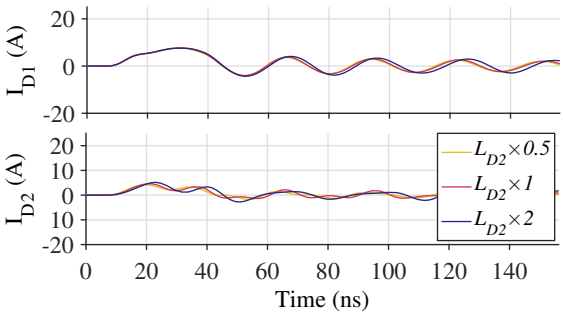

Figure 3.20: Variation in the switching device current waveforms for varying values of the bottom device drain inductance

knowledge of what impact each one will have from these parametric sweeps. It appears that the scaling of the top device drain inductance (L_{D1}, fig. 3.19) allows the frequency of the ringing in the top switching device to be modulated with minimal impact on the bottom device current

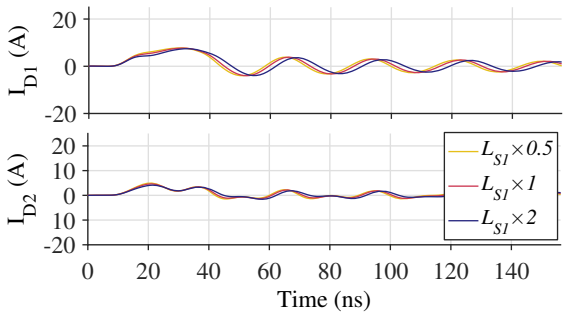

Figure 3.21: Variation in the switching device current waveforms for varying values of the top device source inductance

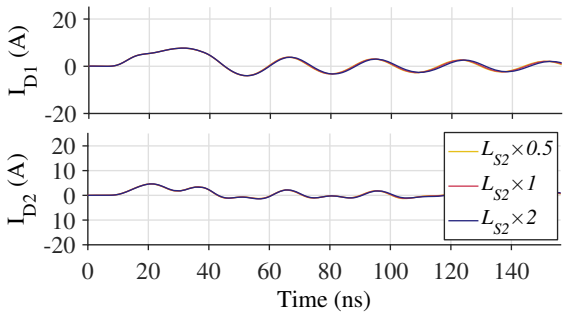

Figure 3.22: Variation in the switching device current waveforms for varying values of the bottom device source inductance. Note that changing this parameter in the range explored changes the waveforms very little, hence the difference is only very slight.

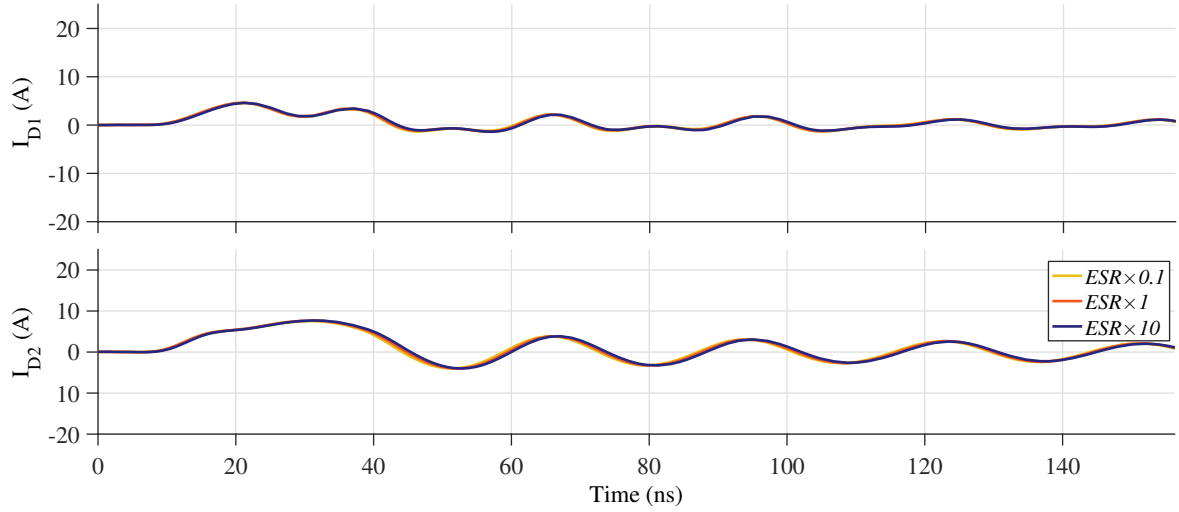

Figure 3.23: Variation in the switching device current waveforms for varying values of DC-link capacitance ESR

waveform. Similarly, the pad-to-pad capacitance (C_{pp}, fig. 3.18) can control the overshoot and ringing frequency of the top switching device current.

These parametric sweeps show that it is possible to achieve a wide range of change in the shape of the current waveforms for both the top and the bottom devices through relatively small changes in the values of the parasitic elements of the circuit. Effects of particular note are the increase in the device current overshoot with increasing capacitance between the device pins, and the minimal variation in the current waveform for changes in the ESR of the DC-link

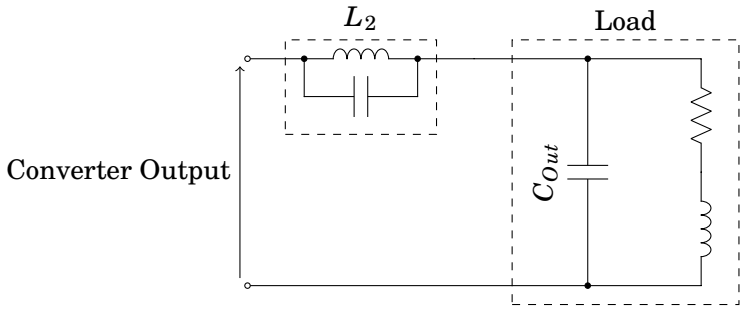

Figure 3.24: Series connection of a small inductor for controlling overshoot due to the load EPC. The load is illustrated including its inherent EPC, as is L_2

capacitance.

3.3 Mitigation

Typically, mitigation of the influence of the parasitic elements is approached by reducing the values of the parasitic elements themselves. This involves techniques such as the reduction of the switching loop area to reduce the parasitic inductance. One particular technique for controlling parasitic induced issues is to reduce the switching speed - this will reduce the current and voltage overshoots, though eliminates some of the benefits of utilising Wide Band Gap switching devices as the switching loss will be increased.

It is unavoidable that the capacitance associated with the load will have to be charged when a switching action occurs. However, this current will only contribute to switching loss significantly if it is supplied while the device is still in the process of switching. For converters with limited or no output filter the inclusion of a small value inductor with a low Equivalent Parallel Capacitance could reduce the inrush of current and as such reduce the switching loss. The reset of this inductor is provided during the off period where the voltage drop across the load resistance provides a reset voltage.

The inclusion of a small series inductor with the load is illustrated in fig. 3.24. The inductance L_2 is chosen to be a low Equivalent Parallel Capacitance type because this would form a bypass of the inductor for any high frequency current. Such an inductor is shown in fig. 3.25 - it has only a single layer winding to minimize the inter-winding capacitance.

Figure 3.25: A small, low EPC, inductor

3.3.1 Inductor Sizing

To calculate the sizing of the small inductor, information on the load and its parasitics are required. Additionally the following approximations are made to simplify the calculation:

1. The inductance of the output cable is insignificant with respect to the added inductance
2. The converter output voltage waveform is a ramp with a constant dV/dt
3. The output capacitance does not become charged significantly during the rise of the current
4. The load current does not increase appreciably in the period of current overshoot

These assumptions are all to the effect of assuming that during the period in which current overshoot occurs the small inductor will be the dominant element.

There are two parameters that must be calculated for this inductor - the inductance, and the acceptable Equivalent Parallel Capacitance. To calculate the inductance, approximate the expected current that will flow into the load capacitance based on the dV/dt at the midpoint of the converter using $I = C\frac{dV}{dt}$. This current is the overshoot current caused by the load capacitance and is what the added inductor will control. By specifying that the rise time of this current

should be somewhat longer than the voltage rise-time (in order that the overlap of the current and voltage of the top switching device is reduced) and also taking the voltage over the inductor to be constant during the transient, the inductance can be calculated using $V = L\frac{dI}{dt}$.

Having calculated the inductance for the snubber inductor a value for its Equivalent Parallel Capacitance can now be considered. If the Equivalent Parallel Capacitance was allowed to be too high then the high frequency components of the current waveform would bypass the inductance entirely and the performance of the inductor would be greatly diminished. To calculate this consider the overshoot current that was previously calculated. Defining the allowable current through the Equivalent Parallel Capacitance of the snubber inductor to be one tenth of the current that would have flown through the load inductance Equivalent Parallel Capacitance is a reasonable performance increase. The allowable capacitance can then be calculated using $I = C\frac{dV}{dt}$, or, as this is simply proportional, divide the load Equivalent Parallel Capacitance by 10.

As an example of these calculations, the specification for a snubber inductor for the converter under test will be presented. The fastest switching speed identified in the test setup will be used, table 1.2 shows this to be 29.8 kV/µs. Section 3.1.3 found the Equivalent Parallel Capacitance of the load to be 340 pF. Given these, the approximate overshoot current into the load would be expected to be 10.1 A.

The inductance is calculated using $L = V\frac{dt}{dI}$. It is assumed that the snubber inductor will support the full voltage during the transition ($V = 600\,\text{V}$). The change in current is the current overshoot calculated previously ($dI = 10.1\,\text{A}$) and the time is set to be slightly longer that the voltage fall time $dt = \frac{600\,\text{V}}{29.8\,\text{kV/µs}} \times 1.2 = 24.2\,\text{ns}$. This gives an inductance of 1.43 µH.

The allowable Equivalent Parallel Capacitance for this inductor will be set at 1/10 of the load's Equivalent Parallel Capacitance - that is 34.0 pF.

3.3.2 Experimental Verification

To verify the effectiveness of these calculations, the inductor in fig. 3.25 was constructed and DPTs were performed with and without it. In these tests a 5 m cable was included in series with the load and the DC-link voltage was 600 V. The waveforms presented in fig. 3.26 illustrate how

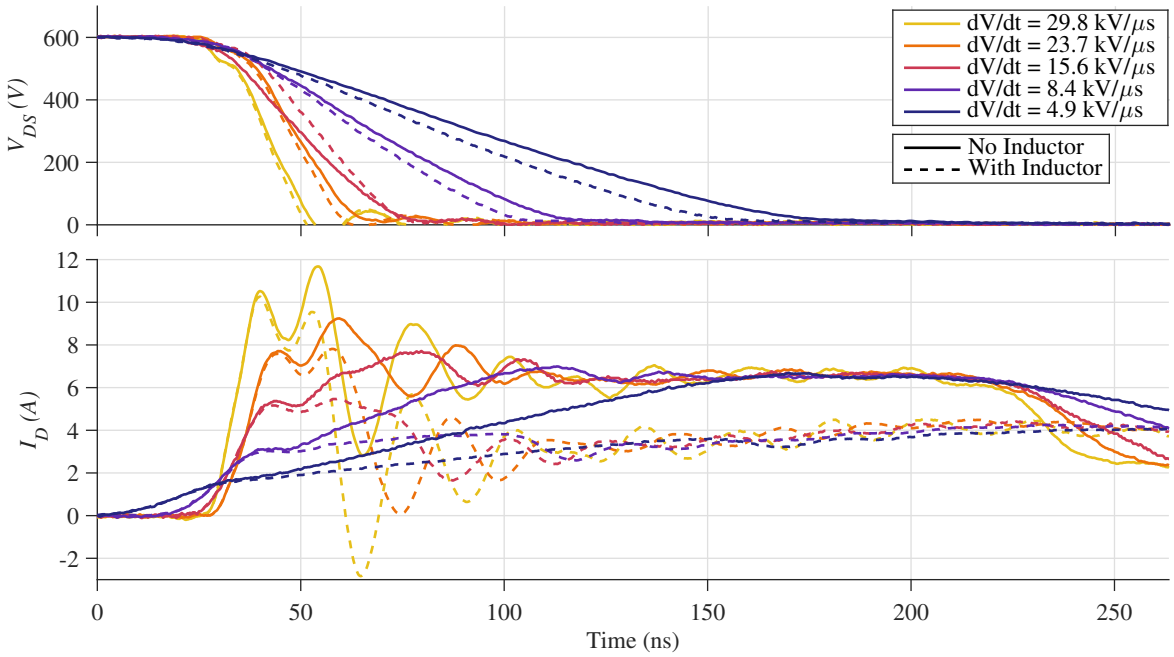

Figure 3.26: Top switching device current and voltage waveforms with and without the inclusion of the additional inductor

the top switching device current and voltage waveforms are influenced by the inclusion of the small inductor over a range of switching speeds - this shows current overshoot is reduced, and voltage transient is sped up.

The voltage and current waveforms are used to calculate the switching power during the switching transition which is presented in fig. 3.27. At each switching speed investigated the switching loss is reduced through inclusion of the small inductor.

Figure 3.28 shows the switching loss calculated at each switching speed with and without the inclusion of the small inductance. It shows that with increased switching speed the switching loss decreases as expected. It is also interesting to note that as the switching speed is increased, the reduction in energy from inclusion of a snubber inductor reduces quite dramatically. This is because the higher switching speeds are able to induce enough current through the Equivalent Parallel Capacitance of the additional inductor that its added impedance does not perform as well as desired.

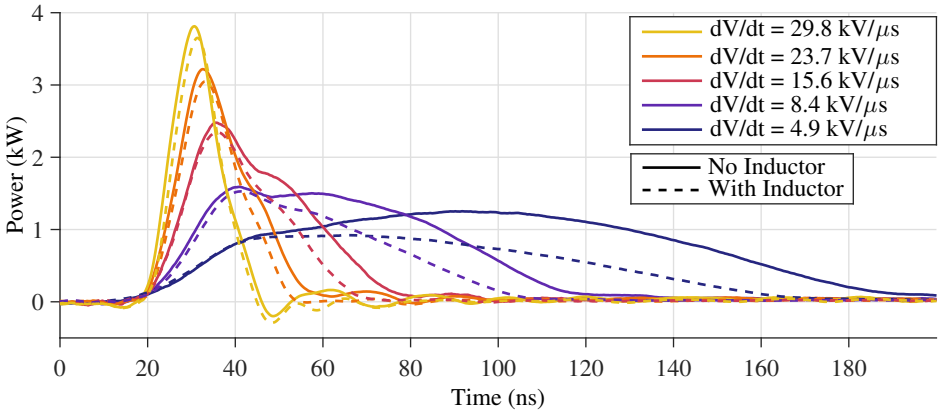

Figure 3.27: Top switching device turn-on power waveforms with and without the inclusion of the additional inductor

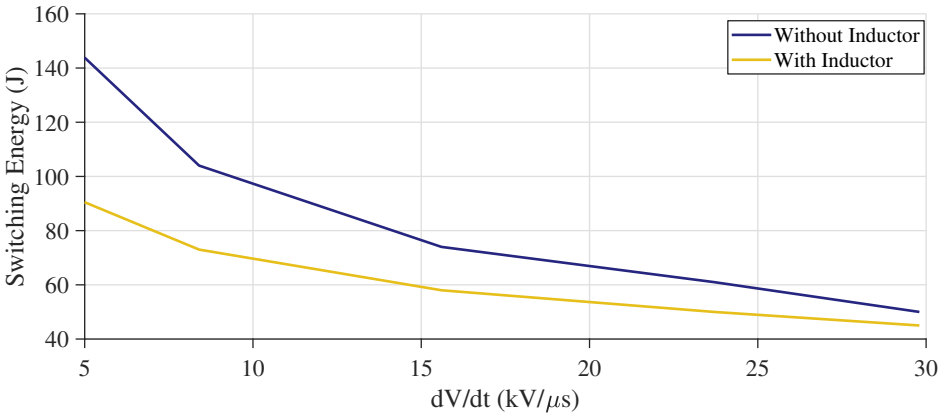

Figure 3.28: Reduction of the switching loss at various switching speeds with the inclusion of the additional inductor

3.4 Summary

The work presented in this chapter has investigated the impact of parasitics on Wide Band Gap based power converters. A hardware setup has been developed that supports DPTs and continuous switching experiments and parameter extraction has been undertaken on this experimental setup to determine the parasitic circuit elements it contains. This process used conventional parameter extraction techniques as well as relying on manufacturer supplied data in some cases.

The extraction techniques used were limited in accuracy contributing to the error in the simulation model accuracy. The impedance analyser measurements in section 3.1.3 were not taken with the same drive bias as the components will experience in actual use. It would be

possible to collect more accurate results using the biasing rig the manufacture supplies for the impedance analyser. At higher voltages some of the parasitic capacitances may increase. The deviation in the model impedance as shown in fig. 3.9 will also contribute to this inaccuracy. This shows that the impedance at the resonance frequency is higher in the model than what was measured. This could be improved through fitting of a more complex model.

The parameters extracted from the experimental setup have been used in the development of a high fidelity simulation model for the SiC power converter. Careful consideration of the parasitic influences on the hardware system have allowed this model to become sufficiently accurate for the testing of techniques for the mitigation of parasitic elements. The accuracy is now limited to that of the manufacturer supplied switching device model which is beyond the scope of this work.

The investigations here show that to create high performance converters utilising Wide Band Gap devices it is important to understand and control parasitic elements throughout the converter. A well designed converter with minimised PCB induced elements may still have very poor performance if the load connected to the converter is poor. Parasitic elements will contribute to the ringing after the switching transient, adding to the EMI generated by the converter, as well as increasing current and voltage overshoots at the switching device and the load. The impact of these features on the EMI will be analysed in section 4.2. Even relatively subtle parasitic such as the C_{pp} can have a significant impact on the performance of the converter when it is operating with high speed switching transitions.

Investigations with a detailed simulation setup have shown that variations in some of the parasitic elements can have a range of impact on the converter performance, in particular any inductance close to the switching device can alter the switching transient drastically. The simulation model was shown to replicate several of the key behaviours of the hardware based system that is used in this work with reasonable accuracy.

Finally, after analysis of the load parasitics, a simple method for reducing the current overshoot and switching loss at turn on has been proposed and tested. The method involves simply including a carefully designed inductor into the load connection to reduce the inrush current to the loads parasitic Equivalent Parallel Capacitance. A method for calculating the size of this

inductor has also been presented and validated using the hardware system.

CHAPTER 4

IDENTIFICATION OF THE TEMPORAL SOURCE OF FREQUENCY DOMAIN CHARACTERISTICS

When creating power converter systems in industry an important concern of the designer will be the EMI generation of the converter. This is essential in order to achieve Electromagnetic Compliance (EMC). To meet the criteria set out the designer needs to have an understanding of how the time domain features of the converter waveform influence the frequency domain performance. This chapter explores the various techniques that a designer may use to identify the temporal characteristics that produce certain frequency domain characteristics. This will include the proposal of a new method of analysis for the temporal waveforms along with the analysis of experimental results. The aim of this chapter is to explore tools which enable the identification of which time-domain characteristics result in specific frequency domain characteristics.

This chapter is inspired by the frequency domain characteristics observed in the experimental results presented in fig. 4.2 in which the spectra are seen to roll-off at a very high rate. It is not immediately apparent from the time domain waveform in fig. 4.1 why this roll-off should be present - understanding the temporal characteristics which manifest this would allow manipulation of the waveform to meet particular design goals.

Work in this chapter is closely supported by the author's publication "Identification of the

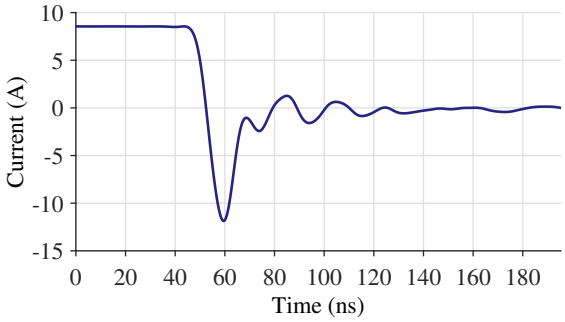

Figure 4.1: Experimental temporal current waveform from the top switching device during the device turn-off. This temporal waveform is found to have interesting frequency domain content. This data has been filtered to remove noise.

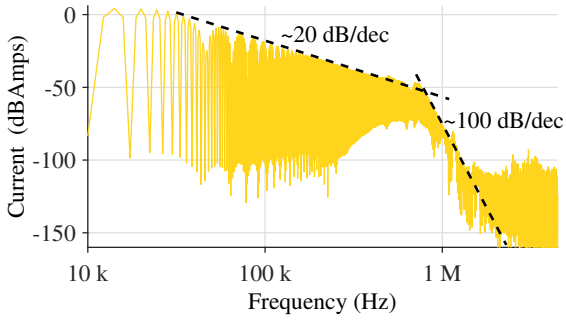

Figure 4.2: Frequency domain content of the temporal current waveform shown in fig. 4.1 illustrating a high frequency region with a 100 dB/dec roll-off. This is calculated as discussed in section 4.1.1.

temporal source of frequency domain characteristics of SiC MOSFET based power converter waveforms" [174].

4.1 Analysis Techniques

To predict the frequency domain content of a typical power converter switching waveform it is common to use the trapezoidal approximation of the switching waveform (fig. 2.10) discussed in section 2.3.1 for which many works report the spectral characteristics [89, 90, 108]. This model predicts a maximum rate of roll-off of the frequency domain content of –40 dB/dec, whereas it has been observed that practical waveforms can contain frequency domain roll-off rates of near –100 dB/dec. Hence analysing these practical waveforms requires a higher fidelity model.

Previous works have suggested techniques for modelling higher order frequency domain characteristics [96, 108, 154, 156], though these methods do not readily apply to experimentally obtained waveforms. Building on the ideas presented in these works this section will seek to explore methods for analysing the experimentally obtained waveforms to determine the temporal source of the high rates of roll-off.

4.1.1 The DFT

The most common method for analysing the spectral content of a signal is the FFT and its discretized dual, the DFT. The FFT takes an infinite waveform and represents it in the frequency domain. The infinite signal can be windowed to a short sample as is necessary in practical systems with finite memory though this will be at the expense of spectral smearing (as discussed in section 1.1.5).

The frequency domain spectra presented in this work will be calculated using the DFT with a Hanning window. Amplitude compensation will be used to compensate for the energy lost in the windowing process, giving better frequency domain amplitude accuracy. This computation is based around the Matlab *fft* function which is then wrapped to ensure a uniform sampling rate is used in the computation. The full listing for this function is included in appendix B.

4.1.2 Spectrograms

One technique for identifying the temporal location at which frequency domain content is generated is to use a spectrogram. In this technique the DFT is calculated for short segments of the signal (STFT) to create a dual frequency/time graph.

The voltage waveform for the top switching device from the hard switched converter (fig. 4.3) was chosen as a test signal to use for investigation. Figure 4.4 shows the waveform after having been processed with the STFT to produce a spectrogram of the signal. At this scale the spectrogram is dominated by the DC component during the periods where the device is switched off.

Figure 4.5 shows a closer zoom of fig. 4.4 focussing on the transient. The temporal waveform has been scaled and superimposed onto the axes to give a time domain reference. The sampling frequency of the original data capture was very high, which gives a good frequency domain range, though most of the frequency domain content is contained below 1 GHz so is not clearly visible in this graphic. A high spread of high frequency energy is shown to occur during the middle of the switching transient, though the limited time domain resolution means it is unclear where within the transition the high frequency content is generated.

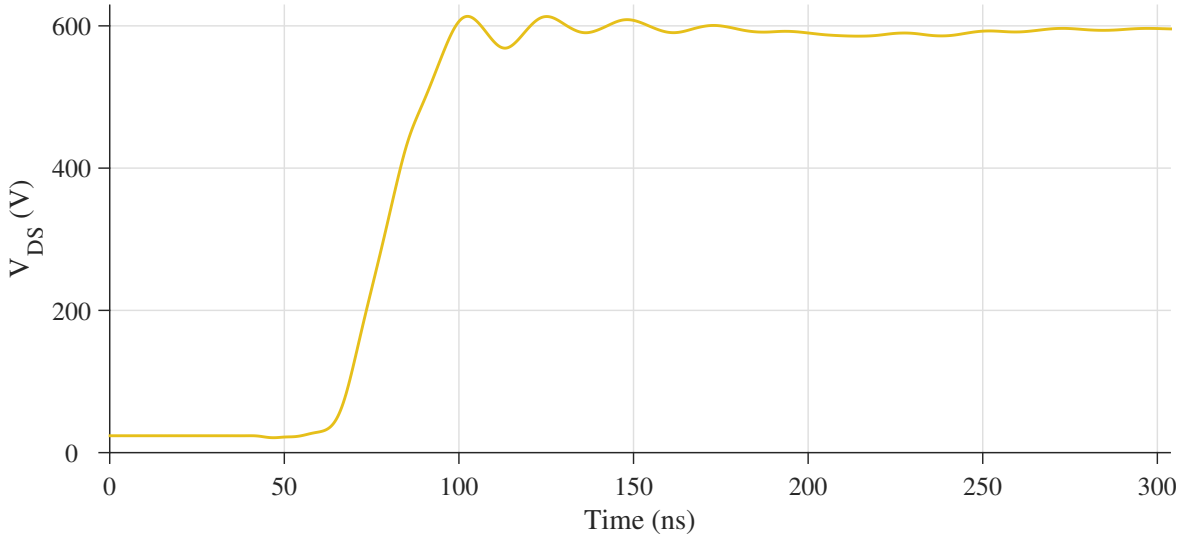

Figure 4.3: The top device turn-off voltage waveform selected for use in spectral analysis

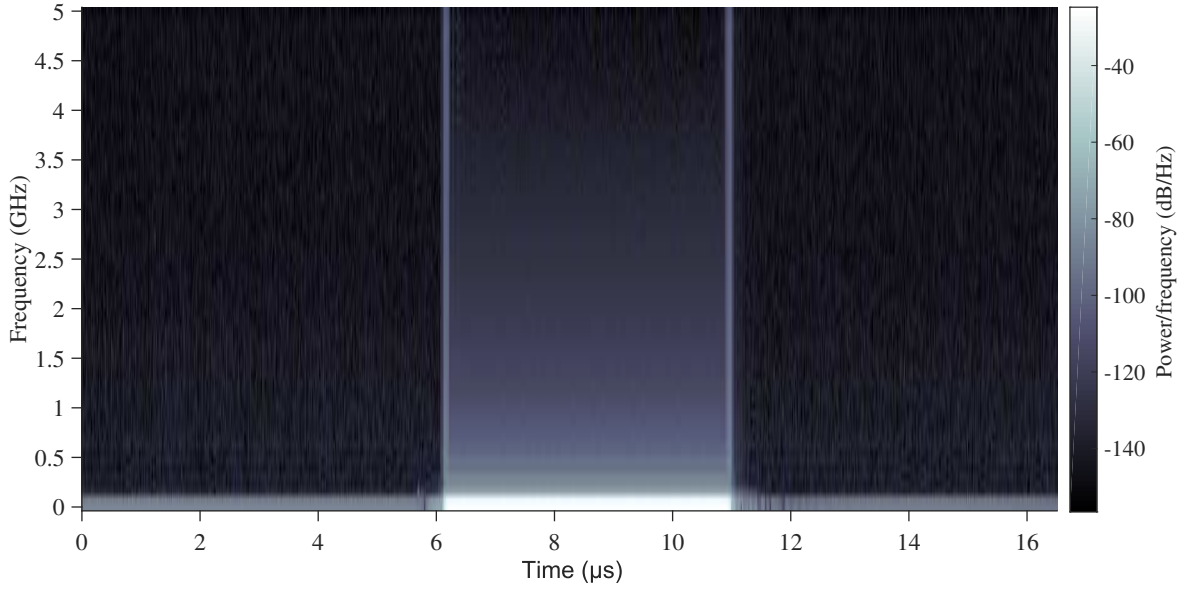

Figure 4.4: Spectrogram of the voltage waveform showing the device switching

Though the spectrograms presented here allow some localisation of the frequency domain content of the signal, the frequency domain resolution will be limited in comparison to taking the DFT of the full signal. This result is a direct product of the uncertainty principle which dictates that identification cannot be both time and frequency domain localised. This limits the utility of spectrograms as a tool for analysing power converter transient signals in this way.

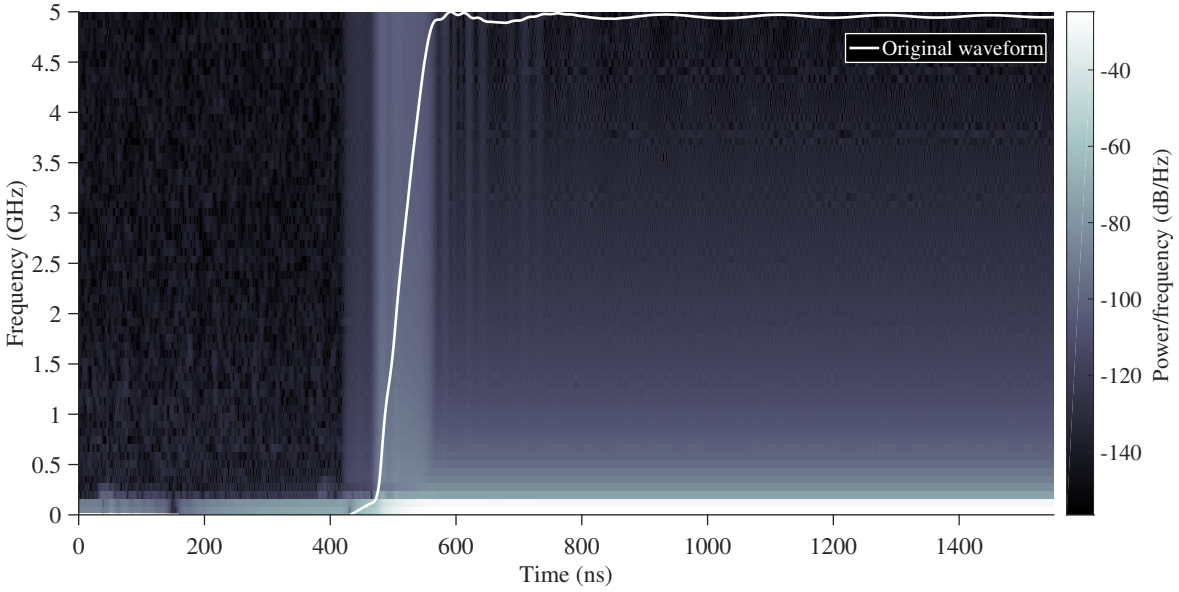

Figure 4.5: Spectrogram of the rising edge of the top device voltage waveform with an overlay of the time domain waveform scaled into the frame for reference to the time domain characteristics

4.1.3 Successive Differentiation

Previous works have demonstrated alternative models for the switching transients of power converter waveforms. [96] has presented a model that is one order higher than that discussed earlier - the 'S'-shaped waveform model. Both this work, and others, show that the introduction of further derivatives into the waveform shape will improve the spectral performance.

The proposal of the 'S'-shaped waveform is founded in the expansion coefficients for the Fourier Transform (FT) of the periodic waveform. Equation (4.1) shows the coefficient expansion for the rectangular waveform, eq. (4.2) shows those for the trapezoidal waveform and eq. (4.3) shows those for the 'S'-shaped case.

Each of the expressions introduces a further sinc() product to the system, which will contribute an additional –20 dB/dec roll-off to the spectral response. This pattern can be continued to produce waveforms with arbitrarily high rates of roll-off.

Rectangular waveform expansion coefficients:

$$c_n = \frac{A}{2} sinc\left(\frac{n\pi}{2}\right) \tag{4.1}$$

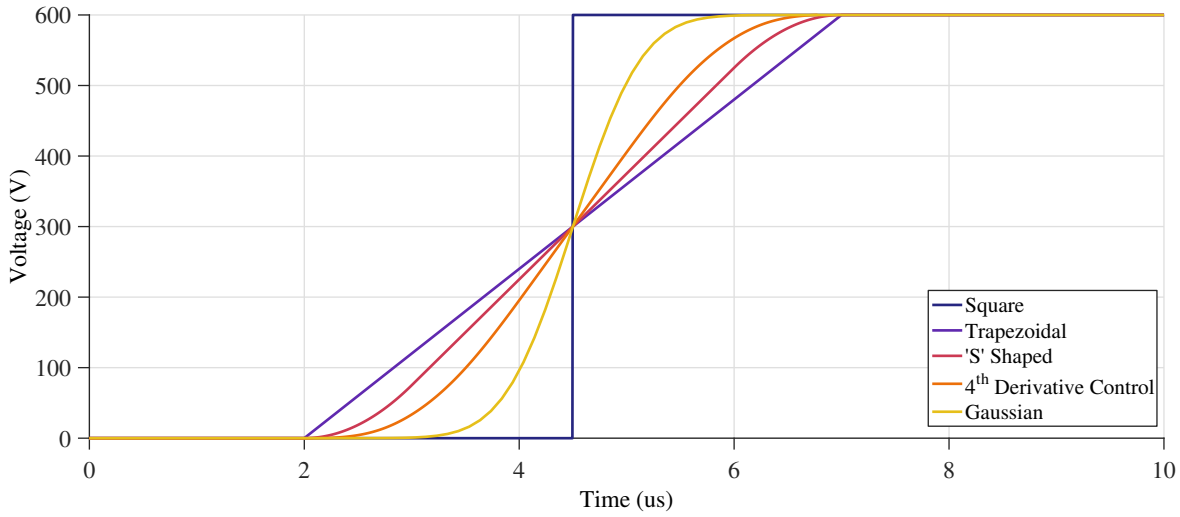

Figure 4.6: Illustration of possible transient shapes with the same transition period

Trapezoidal waveform expansion coefficients [90]:

$$c_n = A\frac{\tau}{T}sinc\left(n\omega_0\frac{\tau}{2}\right)sinc\left(n\omega_0\frac{\tau_r}{2}\right)e^{-jn\omega_0\frac{\tau+\tau_r}{2}} \tag{4.2}$$

For the 'S' shaped waveform [95]:

$$c_n = A\frac{\tau}{T}sinc\left(n\omega_0\frac{\tau}{2}\right)sinc\left(n\omega_0\frac{\tau_r-\tau_{r(dV/dt)}}{2}\right)sinc\left(n\omega_0\frac{\tau_{r(dV/dt)}}{2}\right)e^{-jn\omega_0\frac{\tau+\tau_r}{2}} \tag{4.3}$$

For all of eqs. (4.1) to (4.3) $sinc(x) = \frac{sin(x)}{x}$

Figure 4.6 presents synthesised time domain waveforms for several such extensions of this concept with their DFTs presented in fig. 4.7. These show how manipulation of the transition alone can produce the various rates of roll-off in the frequency domain.

Given that it is possible to create waveforms with any desired rate of roll-off simply through modification of the switching transient in this way, it is proposed that the temporal characteristics of the transient could be compared with these definitions to determine the temporal characteristics.

Each of the waveforms explored has a measurable level of 'smoothness'. Mathematically it is possible to define the smoothness of a given function in relation to the number of times that function can be differentiated before Dirac functions are encountered. This is defined as D for the work presented here. For the rectangular model of a power converter waveform with the

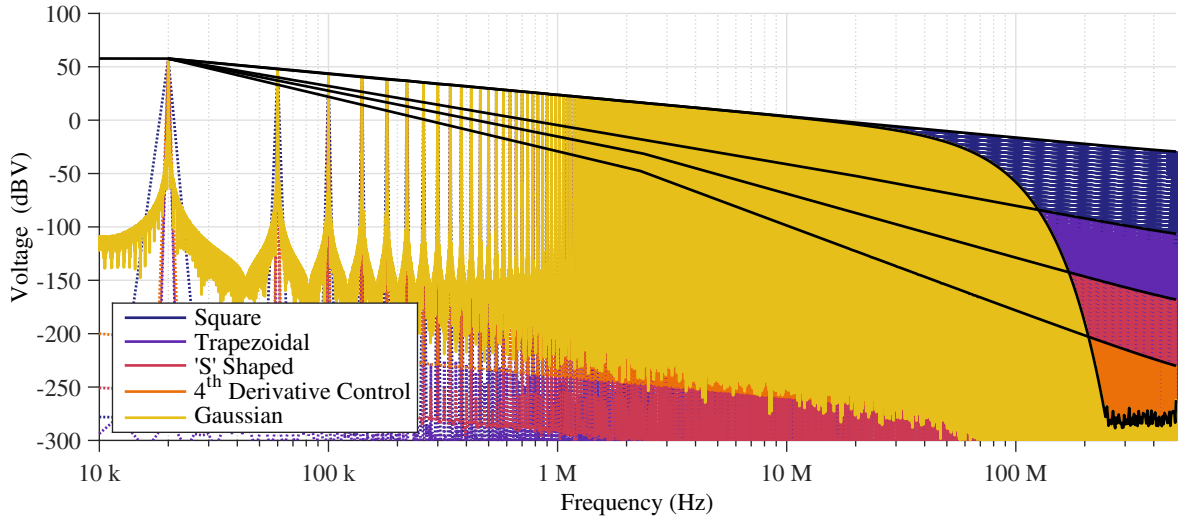

Figure 4.7: Spectral profile of the transient shapes shown in fig. 4.6 illustrating the various rates of roll-off of high frequency content. 100 cycles of the waveform are used along with the analysis technique discussed in section 4.1.1

expansion coefficients presented in eq. (4.1) the waveform can be differentiated just a single time before encountering Dirac functions.

Example waveforms and their differentials are presented in fig. 4.8 - each additional level of smoothness adds an additional differential prior to the appearance of Dirac functions.

Figure 4.8 shows that the characteristics of the waveform at the zeroth differential are difficult to distinguish, whereas the shapes observed in the higher order differentials are distinct in characteristic. It is proposed that the analysis of experimentally obtained waveforms could be performed by successive differentiation of the waveform followed by comparison with the known shapes. This could be a viable technique for identifying with greater time domain resolution, the temporal source of the frequency domain characteristics.

Figure 4.9 shows the proposed process applied to experimental data. The differentiation of the waveform at each step will amplify the noise on the signal, so it is important to use a smoothing function to clearly show the profile of the waveform at each level. The smoothing function used here is a 5 point moving average as this works well with uniformly distributed noise. The effect of this is demonstrated in fig. 4.10 - it is notable that the amplitude of the waveform can be significantly reduced during this smoothing operation, and this must be accounted for by using

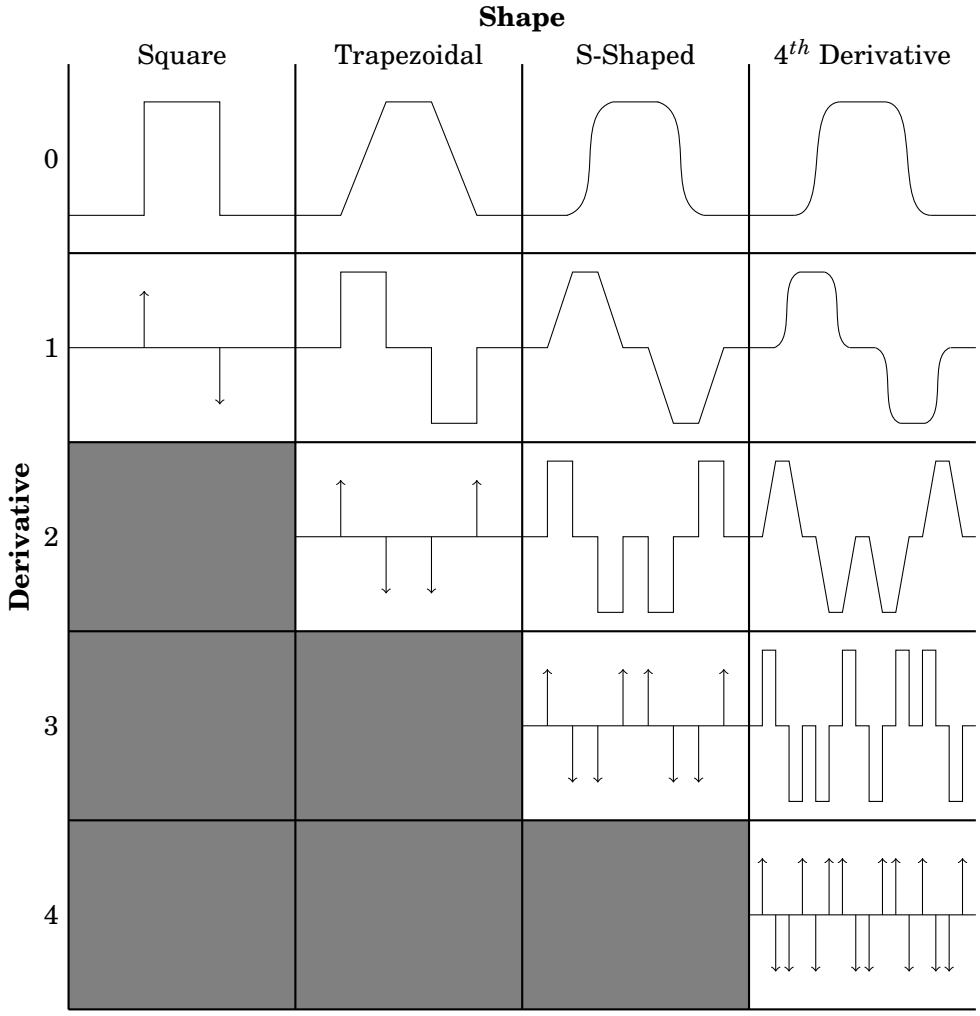

Figure 4.8: Illustration of the result of successively differentiating waveforms of increasing smoothness showing appearance of Dirac functions after increasing numbers of differentiations

the same number of filter iterations when comparing the differentials of several results.

Annotated on fig. 4.9 are the approximate equivalent shapes of each differential - as experimental data is naturally derived it will always be infinitely differentiable and never contains discontinuities, so the closest approximation must be considered. The shapes here suggest that this data is representative of a 3^{rd} or 4^{th} order system. The fourth differential shows clearly a higher amplitude at the beginning of the transient indicating that this will be a more significant contribution to the frequency domain content than the end of the transient.

The use of the successive differentials technique shows that it is possible to predict the characteristics of the frequency domain waveform, and importantly, can help to identify when,

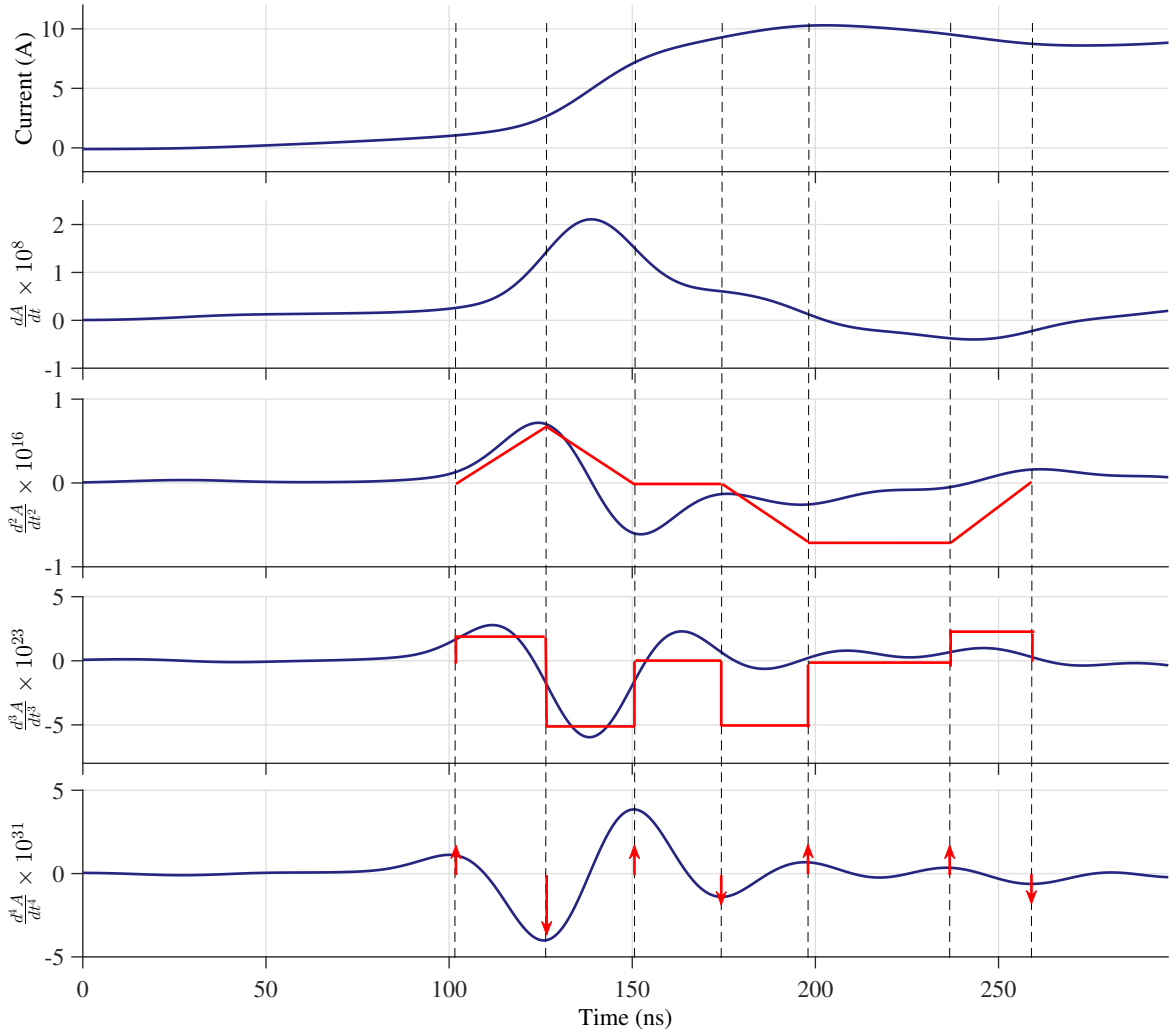

Figure 4.9: Demonstration of successive differentiation of a temporal waveform to identify the transition characteristics

within a switching transition, the most important characteristics are located.

4.2 Frequency Domain Impact of Temporal Characteristics

Some particular time domain features are well understood in terms of their contribution to the frequency domain performance. In this section two such influences are explored with the aim of contributing to a full analytical model of the frequency domain performance. The two artefacts that will be explored are the overshoot and ringing that occur at the switching transient. [120] shows that the the characteristics illustrated in fig. 4.11 can be expressed as a set of coefficients

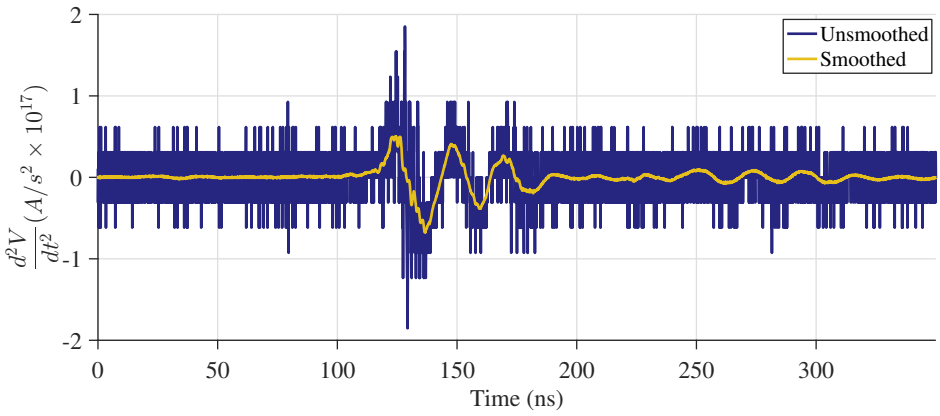

Figure 4.10: Illustration of the use of a smoothing function to help reveal the characteristics of the higher order differentials of time domain waveforms

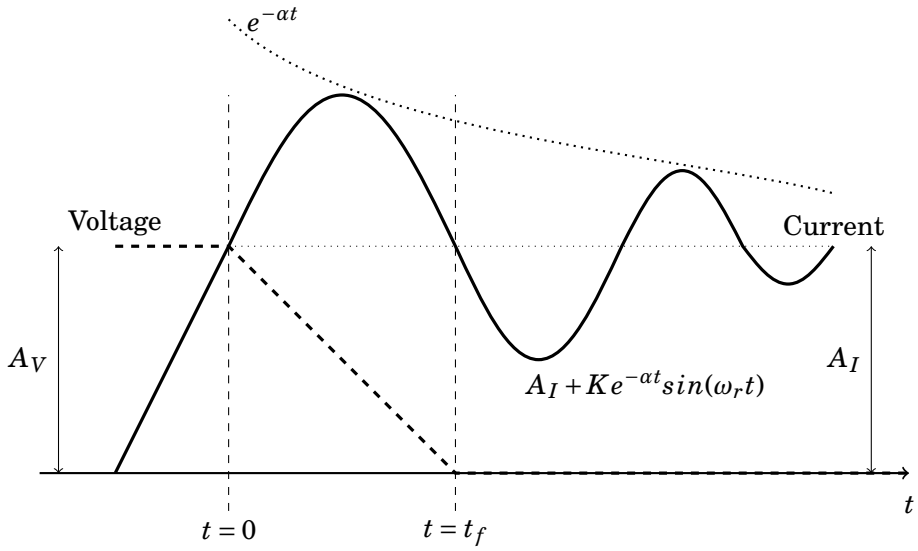

Figure 4.11: Parametrisation of the characteristics of a typical device transient waveform with overshoot and ringing

in the frequency domain given by eq. (4.4).

$$C_n = (fundamental) \times \left(\frac{p^2 + \left(2\alpha + \frac{K}{V_0}\omega_r\right)p + \alpha^2 + \omega_r^2}{p^2 + 2\alpha p + \alpha^2 + \omega_r^2} \right) \tag{4.4}$$

The frequency domain effect of the additional coefficients included with the model in eq. (4.4) is that of a bandpass function. This will create a spike in the spectra of a signal with ringing. The centre frequency of this function is given by $\omega = \sqrt{\alpha^2 + \omega_r^2}$.

Table 4.1: Parameters used to characterise the overshoot and ringing during the switching transient

Parameter Symbol	Parameter Description
A_I	The amplitude of the current
A_V	The amplitude of the voltage
$\frac{dI}{dt}$	The rate of change of current (assumed to be constant)
t_f	Voltage fall time
K	The magnitude of the current ringing/overshoot
α	Damping ratio of the ringing
ω_1	Frequency of the ringing
E	Switching losses
p	$jn\omega_0$

The impact of overshoot in the time domain on the frequency domain can be analysed in the same way [120]. This is because overshoot is ringing with a very high damping ratio.

Given the parametrisation defined by fig. 4.11 coupled with the definitions of table 4.1 an equation for the switching loss can be defined. This is computed taking the integral of the product of the voltage and current waveforms and leads to eq. (4.5).

$$E = (A_I K - \frac{dI}{dt} t_f K)\left(\int e^{-\alpha t} sin(\omega_1 t_f)\right) + A_I A_V t_f - \frac{1}{2}\frac{dI}{dt} t_f^2 A_V \tag{4.5}$$

The models presented so far now allow for investigation of the influence of ringing in the experimental system. Section 3.1.2 explored the extraction of the circuit inductance which can be used to estimate the frequency of ringing. These estimations repeated in fig. 4.12 along with the measured ringing frequency from the time domain data shown in fig. 4.13.

Comparing the predictions from the results in fig. 4.12 with the observed frequency peaks in fig. 4.14 shows that the estimation is not very accurate. This is because the estimation relies on an estimation of the switching loop inductance. The estimation of the switching loop inductance has been inferred through measurement of the voltage droop at the beginning of the switching transient - this is a small signal to measure so will be prone to noise. There may also be some voltage supported by the switching device if a small current is flowing which would skew the estimation. The accuracy of this estimation could be improved by simultaneously measuring both of the switching device voltages during switching to determine where in the loop the voltage droop is.

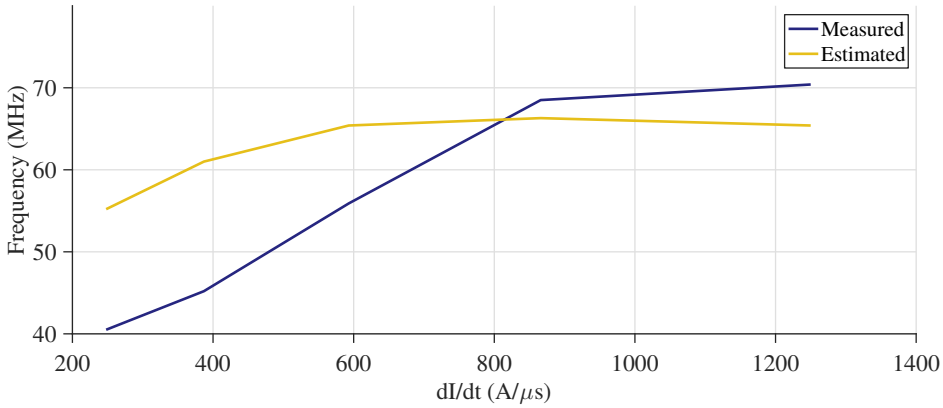

Figure 4.12: Comparison of calculated and measured current ringing frequency

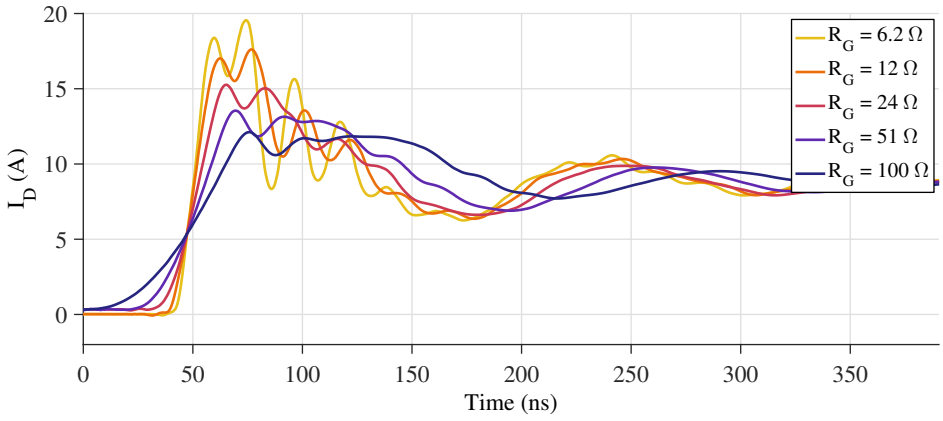

Figure 4.13: Experimental current waveforms from the top switching device with various gate resistances

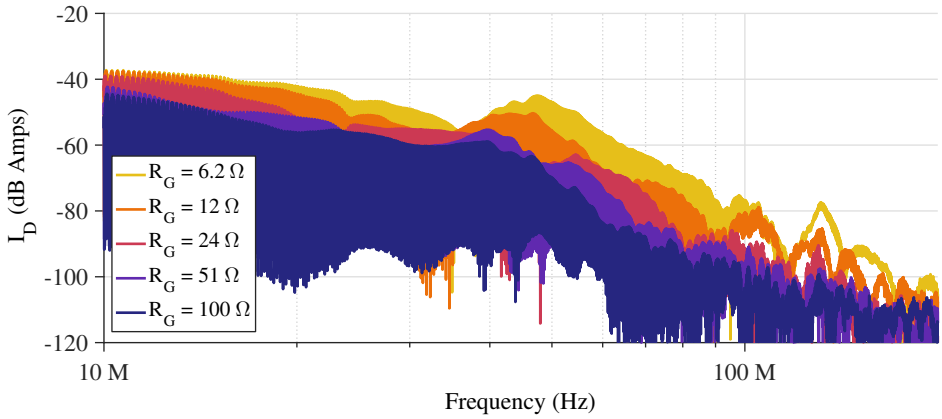

Figure 4.14: Spectra of the time domain waveforms shown in fig. 4.13

4.3 Performance Metrics

Having discussed ways of identifying the temporal characteristics which tend to cause frequency domain features there is now a need to quantify how 'good' a particular result is. This requires the use of metrics to compare any given waveform. Most such metrics come about trivially and naturally - an example of which is the switching loss - the physical meaning of this metric is instantly understandable and easy to compare. Also simple to compare are the switching speed and the converter's efficiency. However, there is one aspect for which a clear solution does not already exist: EMI.

To be able to compare the relative performance of different waveforms in the frequency domain it is common to plot the spectrum of the signals and visually inspect them. This does not lend itself to fast categorisation of which waveform is 'better'. To quantify the performance of the converters EMI generation capability several methods are explored. A good metric would take into account the need to fit within a particular EMC limit, as well as taking into account the effective cost (in terms of size/weight) of additional filter components required to correct the EMI performance.

[123] presents a technique for producing a metric for the EMI generation capability of power converter waveforms. In this technique an ideal filter with a roll-off of –20 dB/dec is introduced into the system. The break frequency required for this filter to lower the spectra of the test waveform below a particular standard is treated as the metric. In this work the EN5022 standard for EM radiation is used as the limit [175].

Figure 4.15 illustrates the spectra of the voltage waveform at the mid point of the converter for the case where the gate resistance is set to 100 Ω. Also illustrated on this figure is the limit of the EN5022-CB specification. The spectra of the midpoint of the converter has a much higher amplitude than the standard - this is because this is not the way in which the standard is intended to be applied. The low frequency content of the waveform now dominates the metric as this will be the part that the filter would meet first. This dominance of the low frequencies means that for this metric to be useful in application to this work the input waveform would first need to be filtered so as to reduce this dominance.

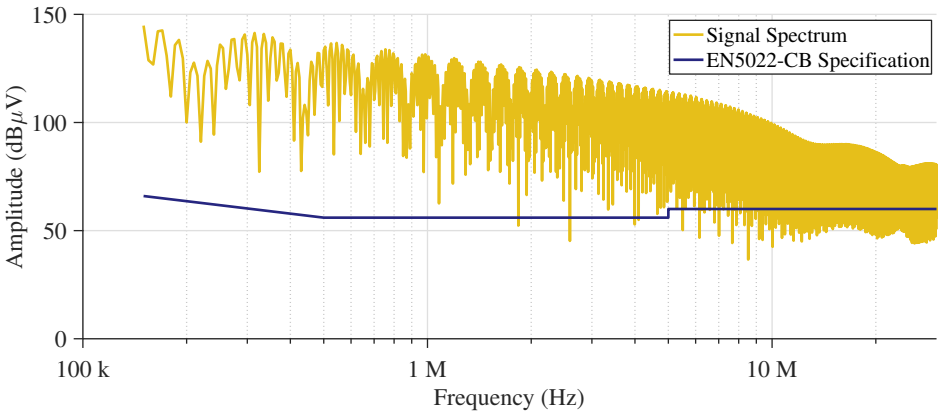

Figure 4.15: Comparison of the spectra of the voltage waveform at the switching node with the EN5022-CB specification with $R_G = 100\,\Omega$

Section 4.1.3 showed that it is possible to identify the source of frequency domain content by considering the successive differentials of the time domain waveform. An important characteristic of this was that high amplitudes in the differentials indicated a strong source of frequency domain content. The equations dictating the frequency breakpoints for a trapezoidal waveform (eqs. (4.6) and (4.7)) show that as either τ or τ_r are decreased, the corresponding break frequency will increase, which in turn will increase the amplitude of the high frequency harmonics. These small values of τ and τ_r correspond to high values in the first and second differentials.

$$f_{c1} = \frac{1}{\pi\tau} \qquad (4.6) \qquad\qquad f_{c2} = \frac{1}{\pi\tau_r} \qquad (4.7)$$

The relative amplitudes of each differential are illustrated in fig. 4.16 where the maximum value found in each differential for a number of switching speeds has been calculated and plotted after being normalised to the case of the slowest switching speed. This shows how with increasing switching speed the amplitude of the differentials tends to increase in sympathy. This is a potential candidate metric for quantifying the EMI generation capability of a waveform.

Bandpower is another metric which could be used for the quantification of EMI performance - in this method the total power in a frequency band is calculated. A signal with more high frequency content would therefore produce a higher figure for the value of bandpower. In this method the range of frequencies used to calculate the metric is an important consideration - the low frequency content in which power is transferred from the converter is not of interest

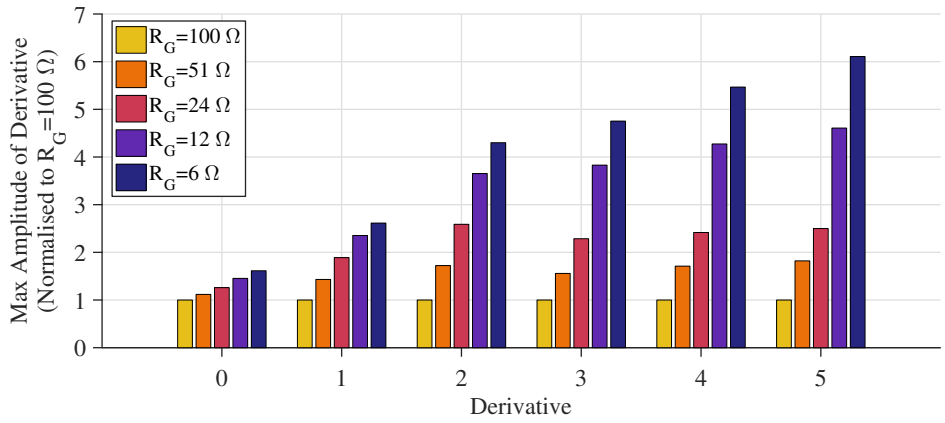

Figure 4.16: Comparison of the maximum amplitude in each derivative of the top device current waveform for various values of R_G

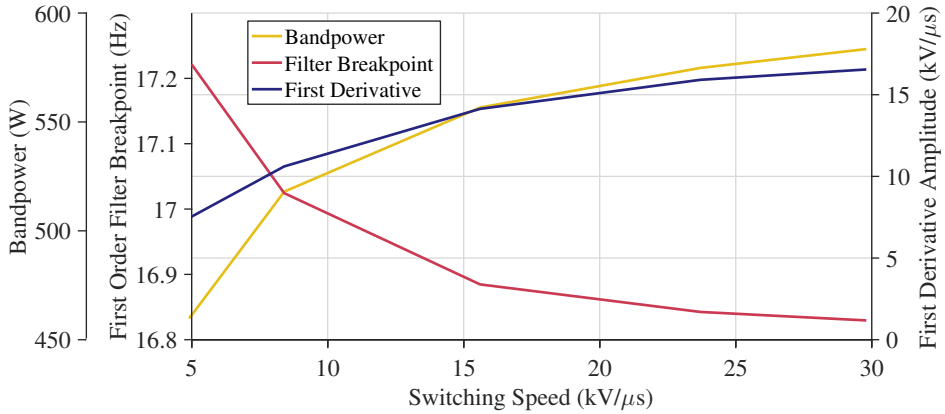

Figure 4.17: Comparison of the variation of each of the discussed metrics with transition speed

to the analysis so must not be included. It is proposed that a suitable range is 1 MHz to 1 GHz as this represents frequencies above the fundamental and responsible for high frequency EMI generation.

To compare all of the possible metrics for quantifying the EMI performance of a converter, the switching waveforms from the experimental system have been analysed with each of the metrics over a range of transition rates all of which are shown in fig. 4.17. It is expected that for the case here where the switching speed has been controlled simply through changing of the value of the gate resistance that there will be a direct trade-off between the EMI performance and the switching losses.

It is observed that each of the metrics does follow the predicted trend, giving three viable

options for a metric to use. The metric proposed in [123] will be discounted as it can be seen to be dominated by low frequency effects. It will also suffer from noise as the output is very sensitive to the position of peaks in the spectra. Of the two remaining metrics bandpower has the advantage of being frequency tunable (the bandwidth can be chosen). Additionally it will not be dominated by a small peak in the input signal. The maximum amplitude of a derivative is susceptible to such peaks dominating the output. As such bandpower is chosen as the metric to use in further work.

A fundamental challenge in using any of the presented EMI metrics is that they will be strongly influenced by the switching speed. Variation in the metric output with switching speed should be expected as models such as those explored in section 2.3.1 define this. However, it makes comparison of different converter designs challenging as they may require different switching speeds. This limitation implies that these metrics must be used to compare performance for converters operation under similar conditions.

4.4 Summary

Having been motivated by the high rate of high frequency roll-off observed in experimental data, this chapter has investigated methods for identifying the temporal source of high frequency characteristics. A method which allows the temporal features producing particular frequency domain characteristics has been explored and the impact of common temporal characteristics such as ringing have been reviewed. Finally, metrics for characterisation of the waveforms performance have been investigated, and a suitable method for evaluating the EMI generation capability of a switching waveform has been identified.

CHAPTER 5

DESIGN AND ANALYSIS OF SMOOTHED WAVEFORMS

The methods for analysis of waveform transition shapes such as those in section 4.1.3 show that the shape of the transition can have a large impact on the performance of a power converter. This motivates the design and use of smoothed transition shapes for control of the performance. This chapter will explore the design of smoothed waveforms for practical application as well as their definition and methods for characterising them.

A key aspect of smoothed waveform transitions is the opportunity to improve the way the transition interacts with parasitic elements in the circuit. Analysis of the interaction of certain parasitics during the switching transition will be presented and methods for predicting certain performance metrics from analytical data will be investigated.

5.1 Definition and Measurement

Mathematically, smoothness can be defined as the number of times a waveform can be differentiated before non-continuous features are observed. It was shown in section 4.1.3 that the deliberate introduction of additional derivatives to the waveform will improve the EM performance [176].

As well as the finitely differentiable waveforms discussed, it has also been shown in sec-

tion 2.4.2 that it is possible to design waveforms that are infinitely differentiable, and hence perfectly smooth as per the definition regarding the number of times the waveform can be differentiated. A switching waveform can be constructed through convolution of a base rectangular-wave having the correct parameters for the converter operation and a smoothing function as discussed in [108]. Suitable functions for this include the Gaussian pulse or a Bump function, as both of these are perfectly smooth [154].

Smooth waveforms have the potential to improve the EM performance, though the impact on switching loss must also be considered. A graphical analysis of this has been undertaken in Appendix 2 of [95]. [95] shows that provided the application of smoothing does not alter the relative rise and fall times of the voltage and current, the losses will be identical in both shaped and unshaped switching.

The data collected from experimental systems presents a challenge in that it is sampled. The process of sampling inherently means that the data is discontinuous and treating it otherwise will make it appear to be infinitely differentiable. This motivates the exploration of other techniques that provide measures of the smoothness of a given experimentally obtained waveform.

Geostatistics is a method for estimating the value of a variable with space, time, or some other variable:

> *...the estimation techniques can be used wherever a continuous measure is made on a sample at a particular location in space (or time), i.e., where a sample value is expected to be affected by its position and its relationships with its neighbours.*
>
> [177]

The tools available in the field of Geostatistics such at the Variogram [178] seem promising as techniques for analysing the smoothness of a waveform and producing a metric, however these tools are found to be better suited for analysing the noise in the data. A particular issue that makes these tools unsuitable is the requirement for data to be de-trended before analysis, this is impractical in this application as the trend is the feature that is the subject of the analysis.

The work of [118] discusses using the Continuous Wavelet Transform (CWT) to create a figure-of-merit for the integrity of a signal, though, as for Geostatistical tools, this has been found to first require an understanding of the characteristics of the required signal. As there is not a clear waveform profile that must always be aimed for this makes this an unsuitable way of measuring the smoothness.

[113–115] also discuss other methods of applying the CWT and wavelets to the problem of power converter signal analysis, though none present methods that allow effective analysis of the smoothness of the general case of a switching transition.

[179] discusses explicitly a measure of smoothness which can be applied to any waveform. The authors state:

> *A continuous differentiable relationship between two variables x and y is smooth at those values of the variables which are such that the value of h_3... ...is small...*
>
> [179]

Where h_3 is given by eq. (5.1), I is a constant scaling factor, and the terms y_n and x_n by eqs. (5.2) and (5.3) respectively.

$$h_3 = \left| \frac{y_3(1+y_1^2) - 3y_1y_2^2}{(1+y_1^2)^3} \right| = \left| \frac{x_3(1+x_1^2) - 3x_1x_2^2}{(1+x_1^2)^3} \right| \tag{5.1}$$

$$y_n = \frac{d^n y}{dx^n} \tag{5.2}$$

$$x_n = \frac{d^n x}{dy^n} \tag{5.3}$$

This metric can be applied to the waveform transients proposed previously to investigate their time localised smoothness. Figure 5.1 illustrates how the value of the metric h_3 varies with time for various transitions shapes.

The lower the smoothness of the waveform the higher the metric tends to be, though a metric which is less time localised would be preferable so that transitions can be compared easily. It is proposed that the average of the h_3 metric over the region of a transition would be suitable for this, and has been computed in fig. 5.2 for various transition shapes.

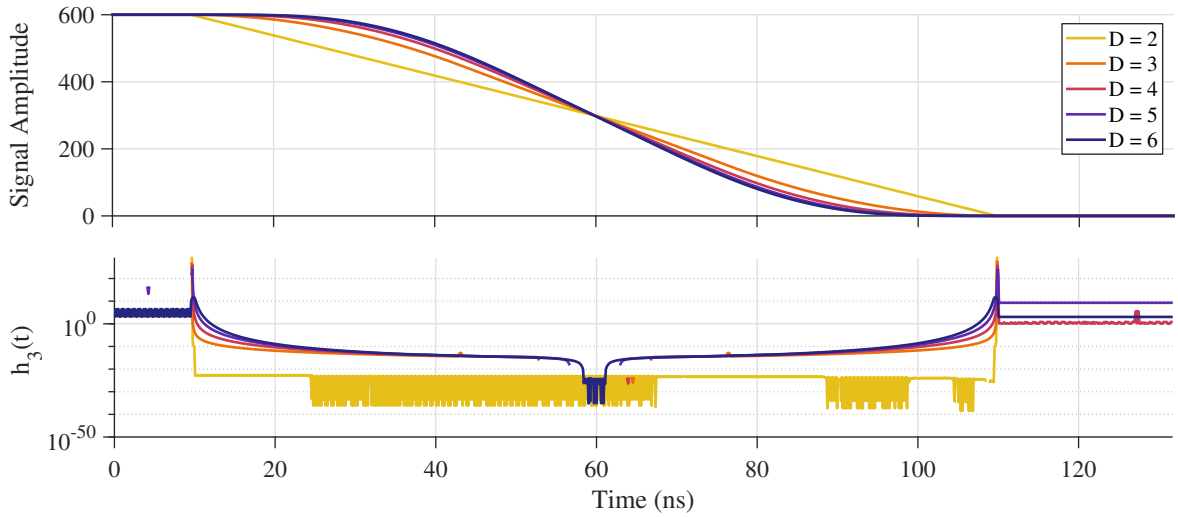

Figure 5.1: Illustration of how the value of the metric presented in [179] varies for various transition shapes with $D = 2 \rightarrow 6$ where D is defined in section 4.1.3

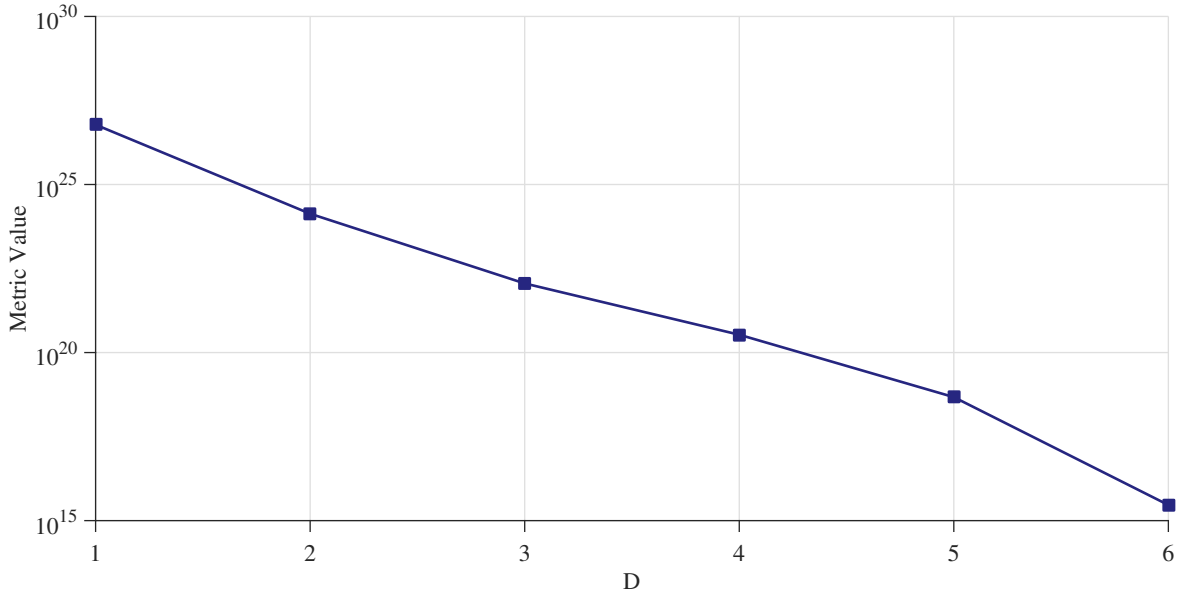

Figure 5.2: Illustration of how the average value of the smoothness metric varies with D where D indicates the number of times the waveform can be differentiated before observing discontinuities in the function.

From the figures shown this metric appears to be ideal for the application, though one flaw is found that prevents repeatability - the metric in its current form will vary as the sampling rate of the signal changes.

This effect was investigated to determine if it could be mitigated by normalising for the sam-

pling frequency and the window length. It was found that the variation in the metric value was not linear with sampling frequency and the function defining this was not found. It is proposed that the reason for the variation with sampling frequency is due to the sampled nature of the signal - changing the sampling rate may change the interpretation of what smooth is. This is fundamental to the definition of the metric and would imply that a new metric needs to be defined if sampling frequency is important. As it is anticipated that waveforms captured from a variety of pieces of equipment will need to be compared in this work this metric is not suitable for this application.

The definition of smoothness was the number of times a waveform could be differentiated before encountering non-continuous features. In section 4.1.3 this was the same view taken for the generation of EMI. Section 4.3 found that the metric 'Bandpower' was suitable for quantifying the EMI. As this shows that the smoothness and EMI are intrinsically linked the bandpower metric can be used for quantification of both.

5.2 Interaction with Parasitics

Given the potential offered through the use of transition shaping and smoothed waveforms it is important to understand how the realisation of such waveforms would interact with parasitic elements of a converter.

Typically parasitic networks can be considered as a network of passive elements. Often these will form filters or resonant tanks. As it has been shown that smoothed waveforms have lower high frequency content, it follows that applying a smoothed waveform should produce less ringing and noise from a given parasitic network provided the applied waveform does not have more energy at the network's resonance frequencies.

To explore this concept a test was conducted to validate this idea in which the circuit of fig. 5.3 was simulated with two excitations - a trapezoidal edge, and a smoothed one. The result of this test is presented in fig. 5.4.

This experiment shows that the use of a smoothed waveform could reduce the level of the ringing and overshoot in a parasitic network, though to what degree this is true is as yet unclear.

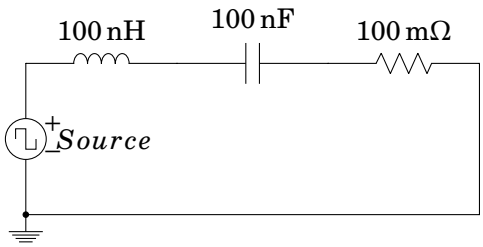

Figure 5.3: Simple simulation circuit for comparing the performance of a smoothed waveform with a trapezoidal waveform. The source is a controlled voltage and the output is the resulting current due to the controlled voltage

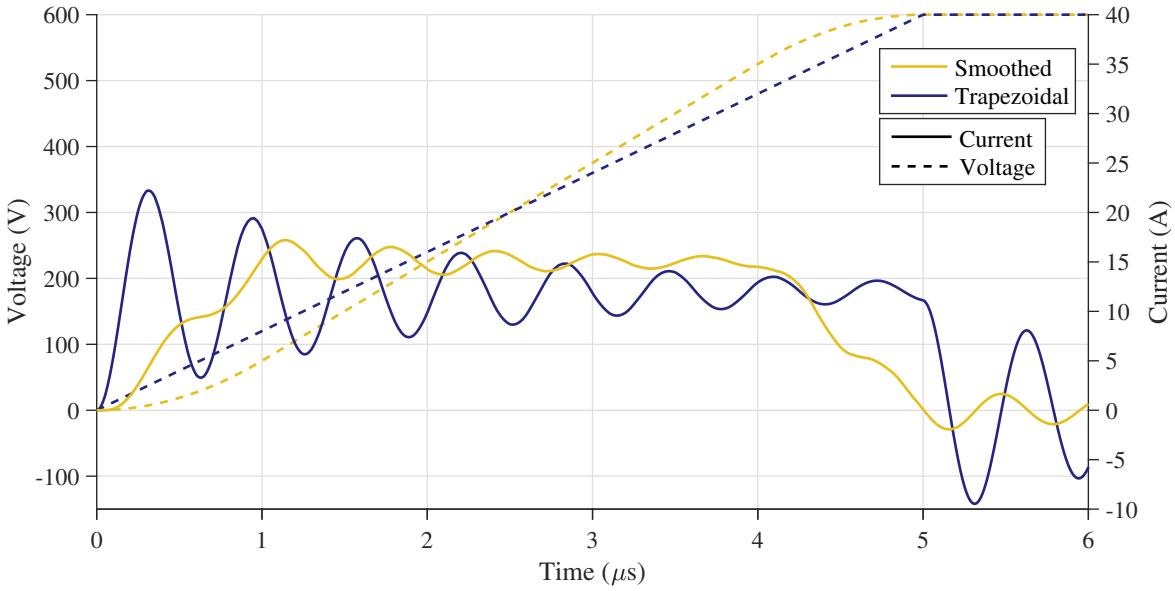

Figure 5.4: Comparison of the current in a series RCL circuit when using a trapezoidal waveform and a smoothed waveform

To explore the full potential of achieving smoothed waveforms several methods of analysing the system are investigated. To understand the impact that ringing will have on the system it is necessary to be able to predict the magnitude of the overshoot of the waveform. As already discussed, it is desirable to have an analytical solution to this problem such that predictions can be made quickly.

It was observed from simulations that the ratio of the peak of the DFT of the unmodulated sinusoid and the peak of the DFT of the modulated sinusoid were equal to the ratio of the integrals of the envelopes of each of the unmodulated and modulated sinusoid. This relationship is shown graphically in fig. 5.5. If this observation were found to be consistent it could help to

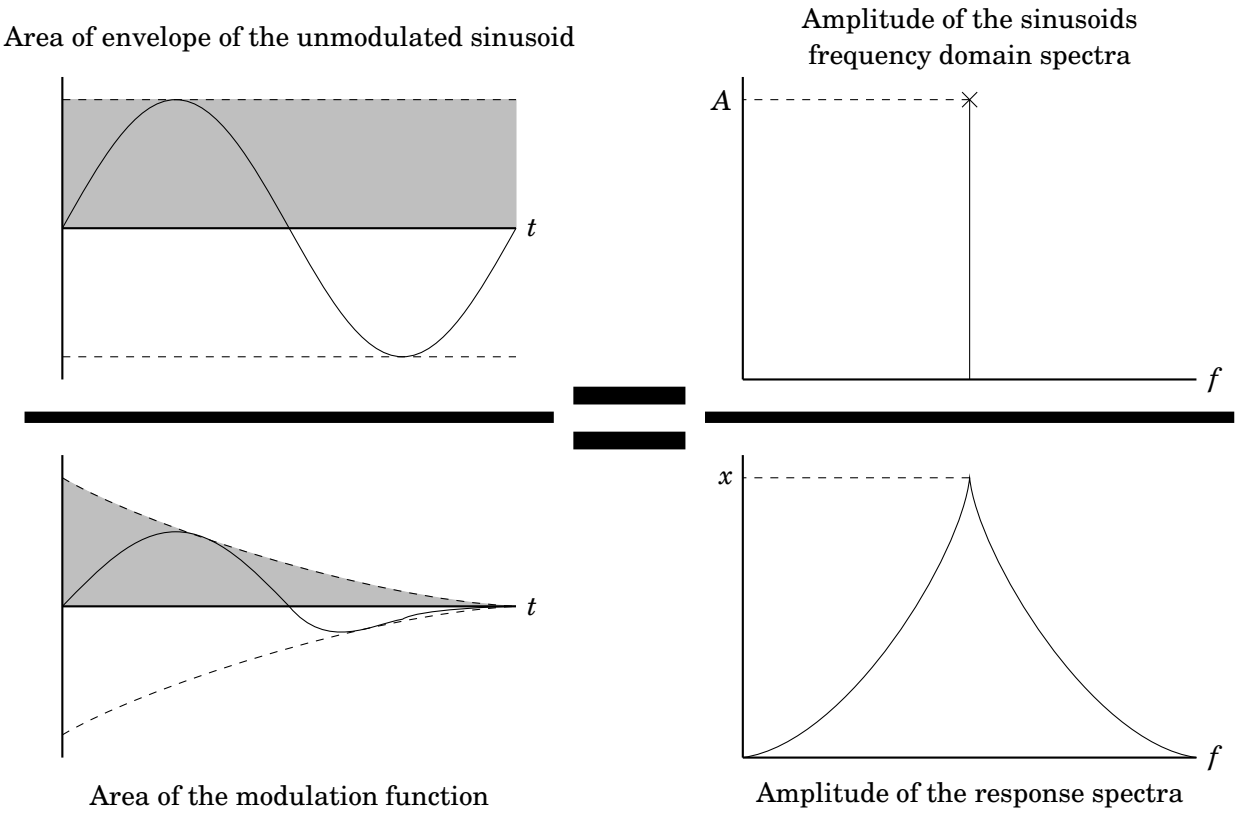

Figure 5.5: Proposed analytical relationship for the prediction of the current overshoot and ringing when a smoothed waveform is applied to a network. It is proposed that the graphical fractions presented left and right should be equal.

provide an analytical method of predicting the overshoot that occurs with the use of a smoothed waveform.

By using knowledge of the parasitic network, both the frequency of the ringing and its damping are known. The bottom of each of the fractions in fig. 5.5 are then known as the integral of the exponential decay defined by the damping of the network and the convolution of the DFTs of the excitation and modulating functions. This expression could then be solved for the amplitude of the unmodulated sinusoidal wave.

It was found through numerical testing that spectral smearing taking place during application of the DFT as well as a non-linear relationship with ω causes this relationship to only be valid under certain conditions, prohibiting this relationships use for analysis of the ringing and overshoot in the general case.

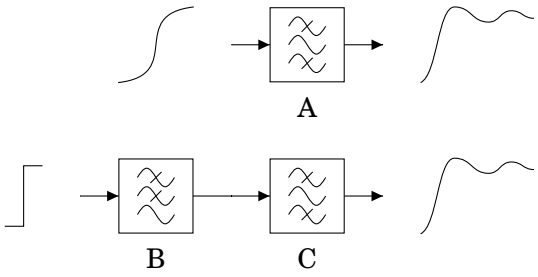

Figure 5.6: Illustration of a method for separating the complex plant and excitation such that each can be analysed independently

An alternative method to approaching this problem is to create a filter that produces the smoothed waveform from a simpler excitation. By doing this the expressions for the filter and the plant can be separated and then analysed in the same way as for a simpler system. This is illustrated in fig. 5.6 where the top case shows the current approach of trying to analyse the application of a smoothed waveform to the plant (A). Instead of this a simpler waveform can be applied to a smoothing filter (B) with the output of this then applied to the plant. The blocks (B) and (C) can then be combined mathematically to be analysed.

It is found that the combined expression for these two blocks is of a relatively high order (more than second order) and as such the overshoot cannot be predicted using well known methods. To resolve this issue it was attempted to approximate the system as a lower order one. However it is found that the poles of the parasitic network alone can be enough to exclude those from the smoothed waveform from the approximation, suggesting that in this simplification the effects of the smoothing are disregarded as insignificant. It was also found that methods such as the half rule [180] and those discussed in [181, 182] for model order reduction were not suitable for dealing with the mix of pole types seen here.

The expression for the system response ($R(S)$) is given by eq. (5.4) or graphically as fig. 5.7 where $Y(S)$ is the excitation, $G(S)$ is the system plant, and A is the amplitude scaling. In these representations, the system has been represented using a set of delay elements, this makes it is difficult to analyse in the time domain. It is possible to make this much simpler to analyse by splitting the system into a set of similar systems that are then summed as illustrated in fig. 5.8.

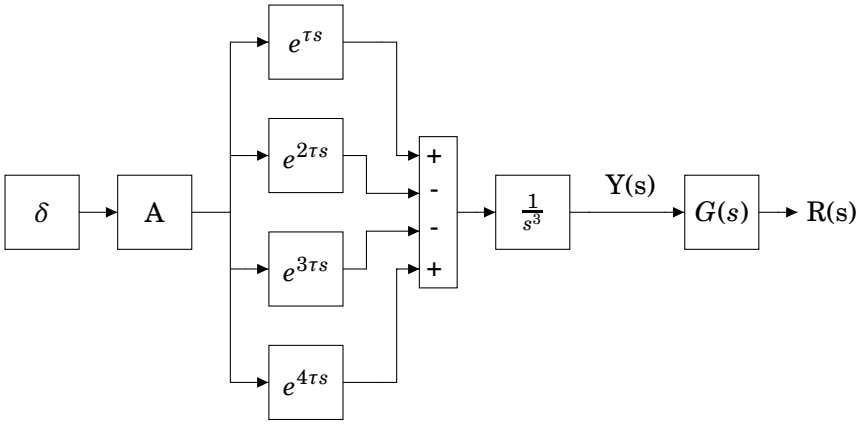

Figure 5.7: Block diagram representation of the system described by eq. (5.4)

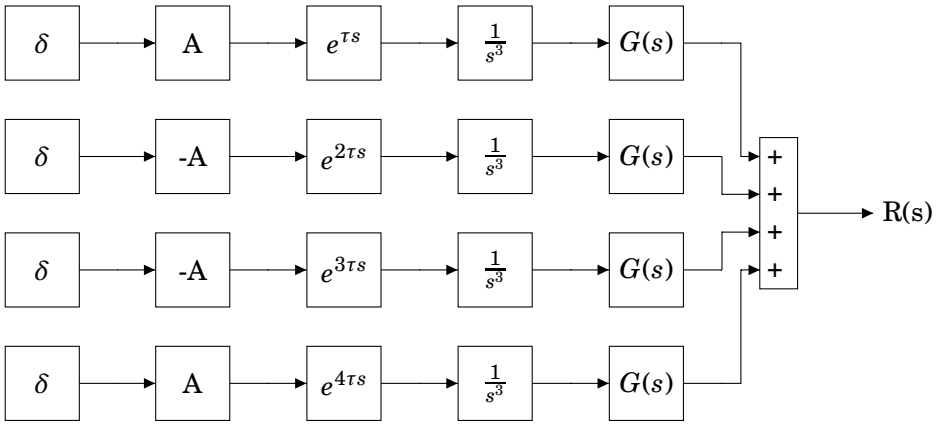

Figure 5.8: Illustration of a method for decimating the system of fig. 5.7 into the sum of simpler systems

$$R(S) = G(S) \bullet Y(S) = G(S) \bullet A \frac{1}{s^3} \left[e^{\tau s} - e^{2\tau s} - e^{3\tau s} + e^{4\tau s} \right] \tag{5.4}$$

In this new structure the smoothness of the excitation is increased by increasing the number of legs in the system and increasing the power of S in the integrator. Each leg is identical in response to all the others with just a time delayed response. This means that an understanding of the whole system could be obtained by considering only a single leg.

To predict the response of this system an example case was taken in which the excitation is applied to a series RLC network as considered previously. The Laplace expression describing the response of a second order system is given by eq. (5.5). More specifically for the case of one leg of the system with the circuit considered here it will be in the form of eq. (5.6).

$$R(S) = \frac{1}{s^3}\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n} \tag{5.5}$$

$$R(S) = A\frac{1}{s^3}\frac{s}{L\left(s^2 + \frac{R}{L}s + \frac{1}{LC}\right)} \tag{5.6}$$

As the plant system likely has complex poles, analysis becomes difficult - the time domain response of the system will be in the form of eq. (5.7).

$$r(t) = A\left(\frac{1}{C}t - Ru(t) + e^{-\frac{R}{2L}t}\left\{Rcos\left(t\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}\right) + \frac{\frac{R^2}{L} - \frac{1}{C} - \frac{R^2}{2L}}{\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}}sin\left(t\sqrt{\frac{1}{LC} - \frac{R^2}{2L^2}}\right)\right\}\right) \tag{5.7}$$

Though this expression appears difficult to analyse it is notable that the oscillatory part decays quickly and is relatively small. Hence the response of each part will be dominated by the other terms of the response.

To find the point at which overshoot occurs the gradient of each response can be considered. The maximum overshoot will occur at the time when the amplitude of differential of the negative legs becomes more than the amplitude of the differential of the positive legs. This is written explicitly in eq. (5.8).

$$\left|\sum f'_+(t)\right| = \left|\sum f'_-(t)\right| \tag{5.8}$$

The time domain expressions for each of the legs of fig. 5.8 do not enable a simple analytical solution to be presented, and must instead be analysed numerically. This does not enable a intuitive understanding of the response to be developed.

If the system is simplified to only include the highest order term in the response (the one that would be expected to be dominant) then it can be shown that no overshoot can be achieved. This has been tested for the cases where the system response is second or third order. The expression for each region of the response is tested to determine if the gradient can become zero. It is found for the second and third order cases that no solution exists.

A simple demonstration of the importance of the oscillatory term in the expression is produced by attempting to fit a polynomial of the expected order to the observed response. The simulated response of a single leg of the system in fig. 5.8 is shown in fig. 5.9.

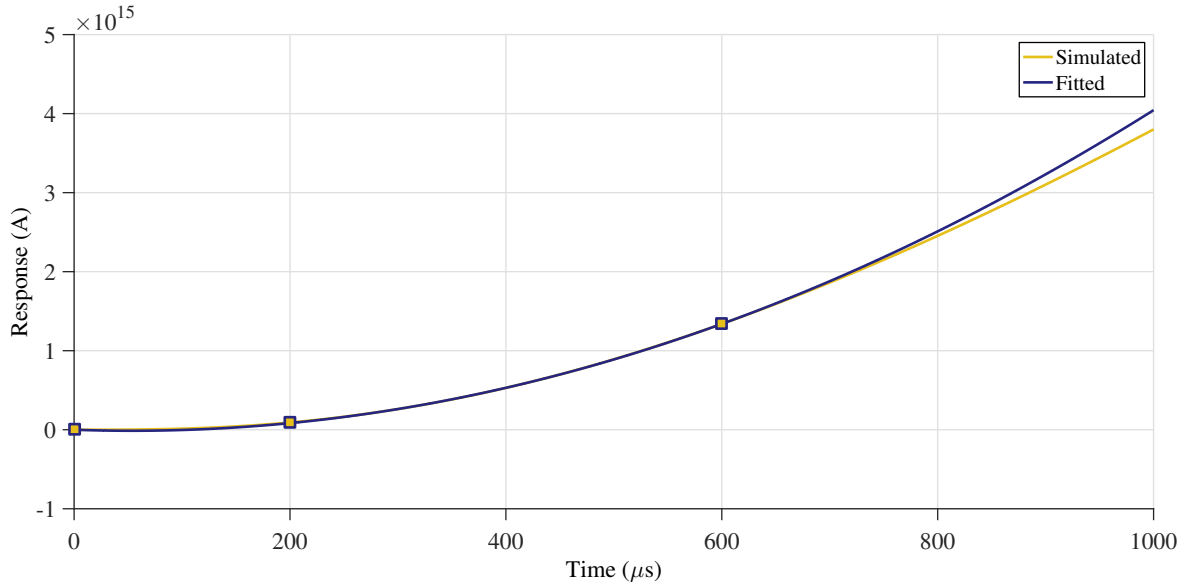

Figure 5.9: Response of a single leg of the system in fig. 5.8 comparing the simulated response with a fitted polynomial

The expressions here predict the response to be third order. The points 0 µs, 200 µs and 600 µs are used to fit a 3^{rd} order polynomial $y = Ax^3 + Bx^2 + Cx + D$. It is shown that soon after the last fitting point the two functions begin to diverge significantly. This must be attributed to the oscillatory term that has been excluded from the approximation made by the fitting. This is significant enough to present the possibility for ringing, particularly so when further responses are introduced. As such it can be concluded that this method of analysis is not adequate for accurate prediction of ringing or overshoot.

The three analytical methods explored here have all shown promise with regards to providing a simple method for predicting the overshoot and ringing when applying a smoothed waveform, though in all cases the simplifications required to make the model manageable have rendered it too inaccurate. This suggests that using an analytical model for this system is not appropriate and as such numerical models must instead be used. Such models will be the subject of investigation in the following section.

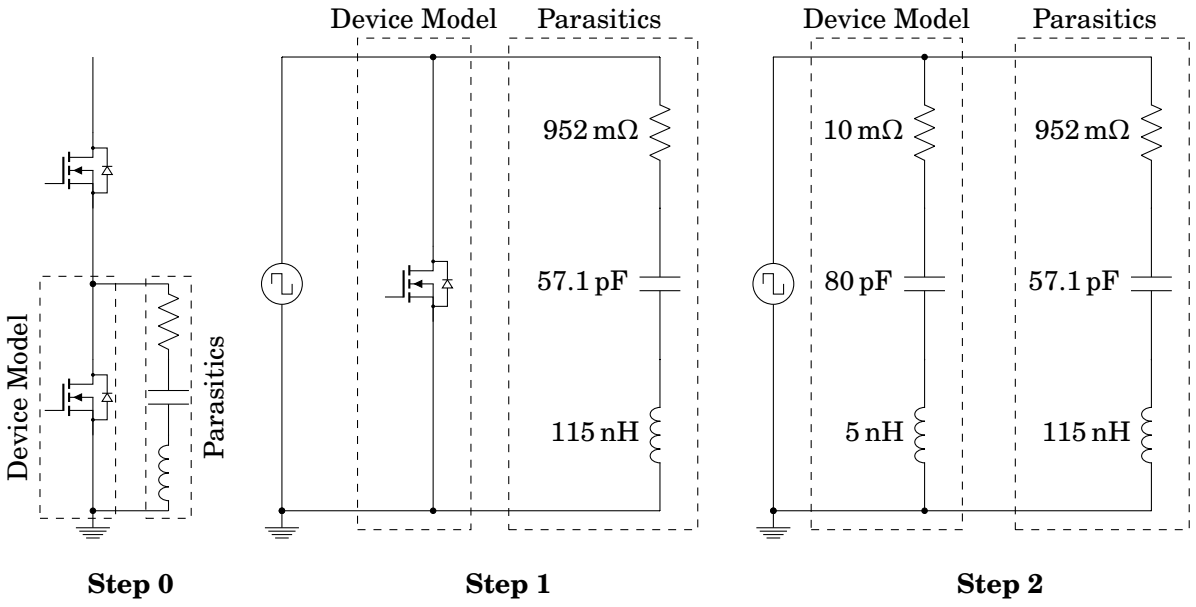

Figure 5.10: Development of the simple LTspice simulation circuit from the half bridge

5.3 Simulation Predictions

Section 5.2 attempted to present an analytical model that could predict the overshoot and ringing that would be expected when a smoothed waveform is applied to a parasitic network. The models presented are not serviceable for this purpose, so in this section a simulation model is designed to assist with the predictions.

The simulation models here are designed to simulate the case where the top switching device has effectively been controlled so as to make the voltage waveform fit the profile of a particular smoothed shape in simulation. This is done by replacing the top switching device with a controlled voltage source. The low side device is then simulated along with several parasitic elements. Elements of the accurate simulation model developed in section 3.2 are used to ensure that the model is as realistic in prediction as possible given the assumptions.

The first simulation model used is derived from the half-bridge with the top device being modelled by a voltage source. Figure 5.10 illustrates how the simulation model is developed, with the top switching device first being replaced by a voltage source, and then the lower switching device being replaced by a simple LCR model.

The overshoot and ringing observed on the current waveform for a range of voltage waveform

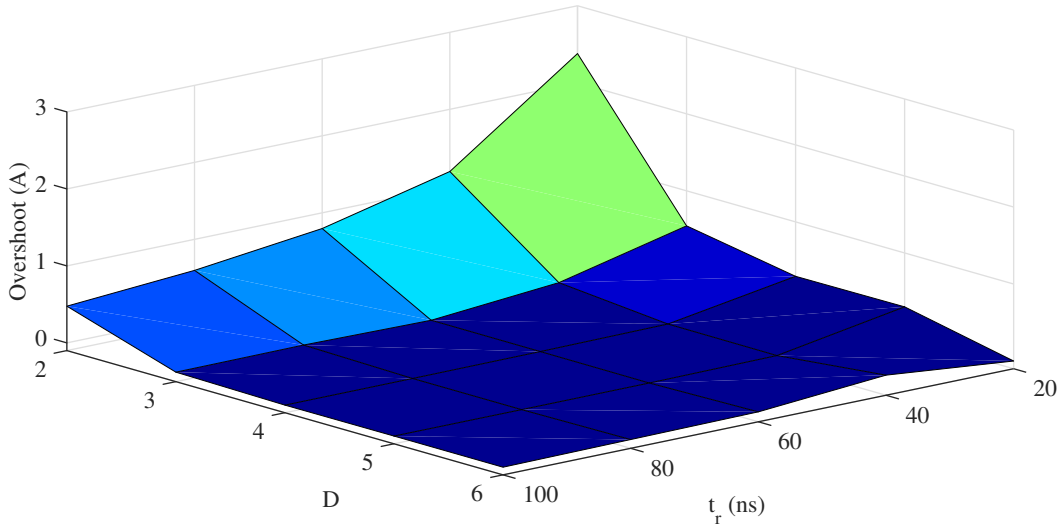

Figure 5.11: Current overshoot as a function of the waveform smoothness and rise time for the simple simulation model

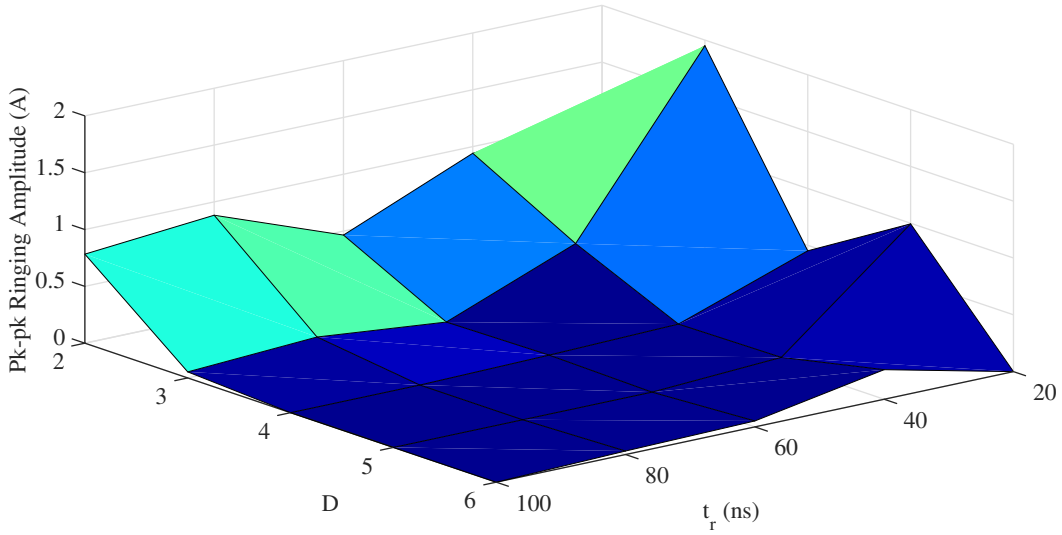

Figure 5.12: Ringing amplitude of the current waveform after switching with voltage waveforms of various smoothness and rise times for the simple simulation model

smoothness and rise times are plotted in figs. 5.11 and 5.12. The smoothness is indicated by D, with $D = 2$ corresponding to a trapezoidal waveform and higher values indicating the number of differentials required to observe discontinuities in the waveform. These results show that the highest overshoot will be observed with the waveform at its fastest and least smooth. At all the transition speeds investigated the increase in smoothness decreases the level of the overshoot.

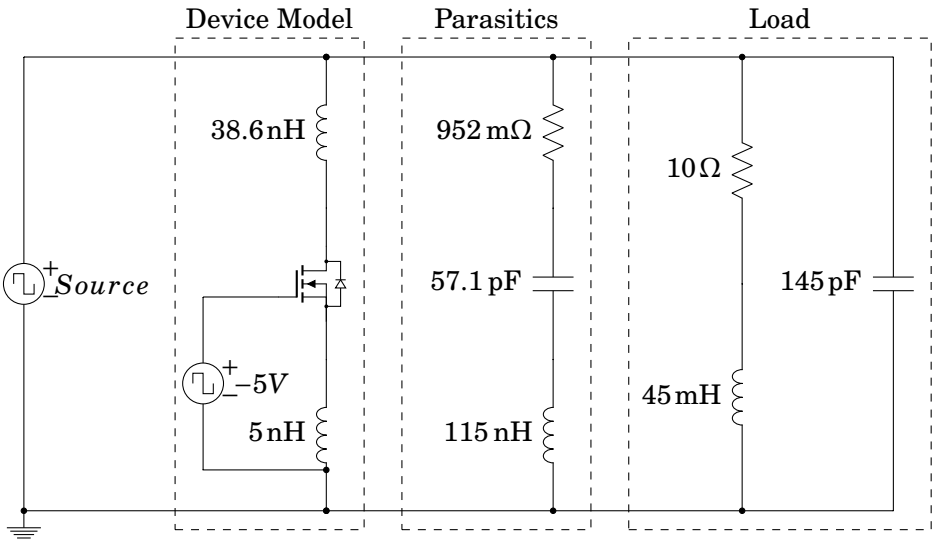

Figure 5.13: Full LTspice simulation circuit

Given that the results here show that for a simple network the application of smoothed waveforms increases the performance, it is justifiable to investigate the impact of using a full switching device model. Figure 5.13 shows the circuit used for a more complicated simulation in which the manufacturers Spice model for the switching device is used.

Figures 5.14 and 5.15 illustrate the current overshoot and amplitude of the ringing for each of the cases as for the simple experimental case. In general the overshoot and ringing are attenuated through the use of the smoothed waveform. It is notable however, that for the faster cases of switching, the increase in the peak transition rate of the waveform as it becomes smoother actually causes the overshoot to increase. This means there is an optimum operation point for each of the switching speeds.

The basic simulations undertaken here show that the use of smoothed waveforms can improve the performance of the converter in the presence of parasitic elements. It has shown that provided a particular voltage waveform profile can be attained by one of the switching devices the current waveform will be improved. If the voltage waveform can be reproduced then this will also reduce the switching losses as the current overshoot is reduced as discussed in section 1.1.2.

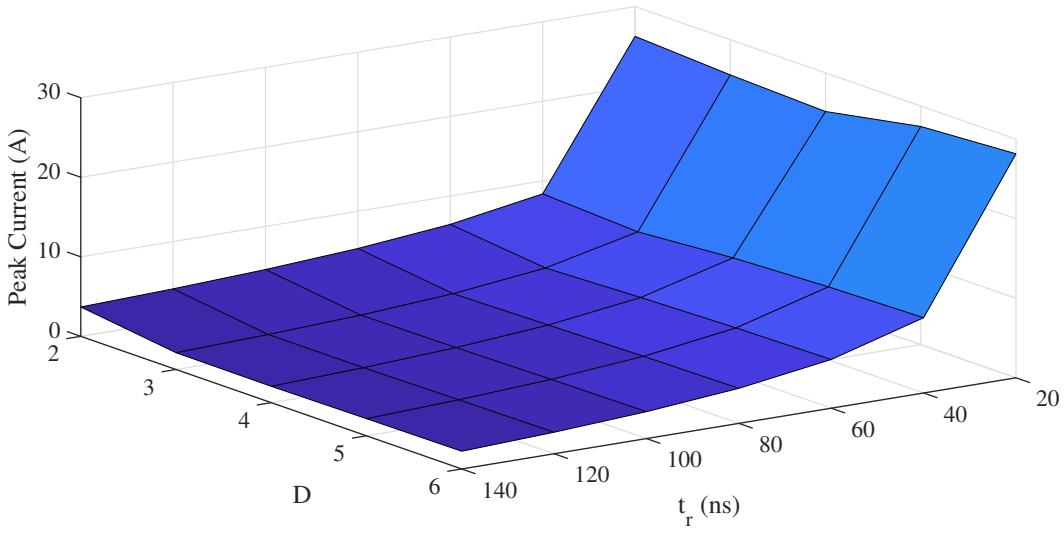

Figure 5.14: Overshoot characteristics of the current waveform in a more detailed simulation model

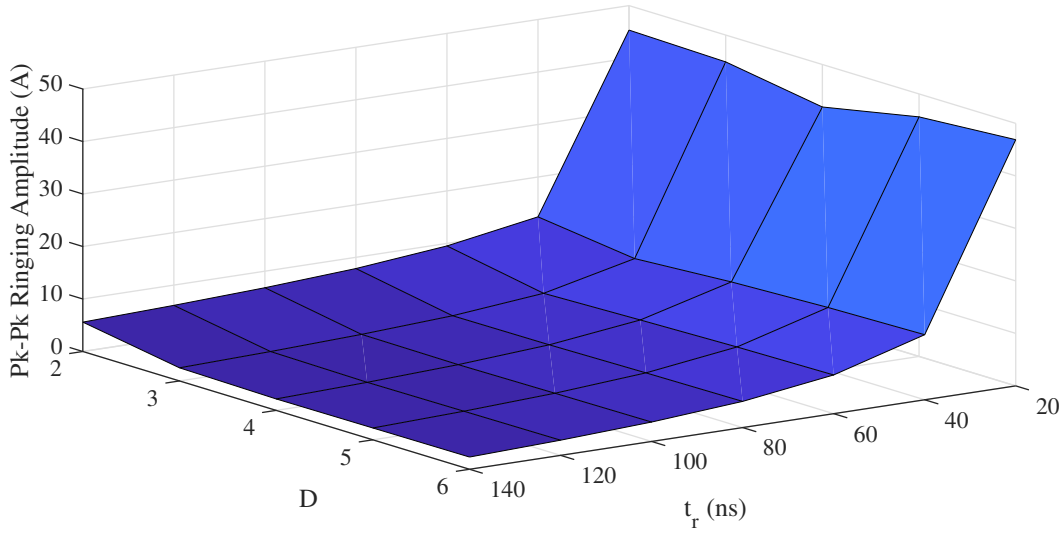

Figure 5.15: Ringing amplitude characteristics of the current waveform in the more detailed simulation model

5.4 Summary

The analysis techniques explored in section 4.1.3 motivated the investigation of creating smoothed transition shapes to improve the performance of power converter switching waveforms. It has already been shown that smoothed waveforms offer significant improvements in the EM performance, and this chapter builds on this by exploring the temporal performance implications and the interaction with parasitic elements.

Several attempts have been made to develop analytical techniques for predicting the overshoot and ringing that will be observed with the use of smoothed waveforms, though it has been found that the high complexity of the excitation and the network which is excited preclude the use of any of the simplified techniques investigated.

Simulation work has shown that the basic theory regarding the reduction of high frequency content introduced to the network through the use of a smoothed waveform can indeed reduce the high frequency content in the output. This has been demonstrated for both a simplified parasitic network as well as a full model including the device manufacturer's simulation model for the MOSFET used in this work.

Given the promising simulation results presented here, further experimental validation is motivated. The next stage of this work will explore how real switching devices respond to the application of smoothed waveforms.

CHAPTER 6

PRACTICAL REALISATION AND APPLICATION OF SMOOTHED WAVEFORMS

With the previous chapter having discussed and developed the concept of smoothed waveforms as well as demonstrating possible methods for applying them to a power converter, the subject now is to develop a system for practical realisation of these waveforms.

It has been shown in previous work that it is possible to shape a MOSFET current or voltage waveform through manipulation of the gate waveform profile [134, 136, 143–145, 149, 152] which is the technique that will be used here. As the largest benefits in performance will come from application to Wide Band Gap devices, the SiC MOSFET discussed in chapter 3 is what will be controlled. As these devices can switch at exceptionally high speeds, achieving control of the waveform profiles will require a very fast linear gate driver. Additionally, very high fidelity data capture will be required to produce meaningful results.

The work presented in this chapter is closely supported by the author's publication "Waveform profiling as a tool for suppressing the influence of parasitic elements" [183].

6.1 Target Waveform

Before attempting to experimentally verify the performance of smoothed waveforms, it is important first to define the goal. Section 5.1 defined and demonstrated a range of smoothed waveform profiles which could be used, whereas a single target is required here.

The initial waveform shapes for the device voltage (V_{DS}) and current (I_D) will be controlled via profiling of the gate waveform. The profile required at the gate of the device to produce a particular profile of voltage or current is not clear, though it is known that this technique can achieve some control. Therefore the approach to find a suitable gate waveform will be iterative, with alterations being made to the waveform empirically at each stage of the process.

As the initial shaping will require human intervention, the waveform target must be visually identifiable. The target selected is simply the 'S'-shaped transition as the characteristics of this are relatively simple.

6.2 Experimental Implementation

The goal of the experimental set up will be to validate that profiling of the MOSFET gate voltage waveform can achieve a smoothed V_{DS} transition shape. Doing so would indicate that a smoothed voltage waveform is applied to the parasitic networks which should in turn reduce the overshoot, EMI, and switching loss.

As the simulation model developed previously in section 3.2 is limited by the manufacturer supplied model, in particular the high frequency switching behaviour, the device model is not used. As producing a sufficiently reliable switching device model would be a highly time consuming task it is instead chosen to address the practical challenges directly.

The experimental set up will run with a DC-link voltage of up-to 600 V and device currents up-to 30 A. The switching speed will be around 500 ns moving to higher rates after initial verification. The gate of the active switching device will be controlled using a linear gate drive so that arbitrary gate waveform profiles can be applied.

Previous works have addressed the challenge of producing a voltage source gate drive for controlling switching devices in various ways. A closed-loop driver for a MOSFET is proposed in

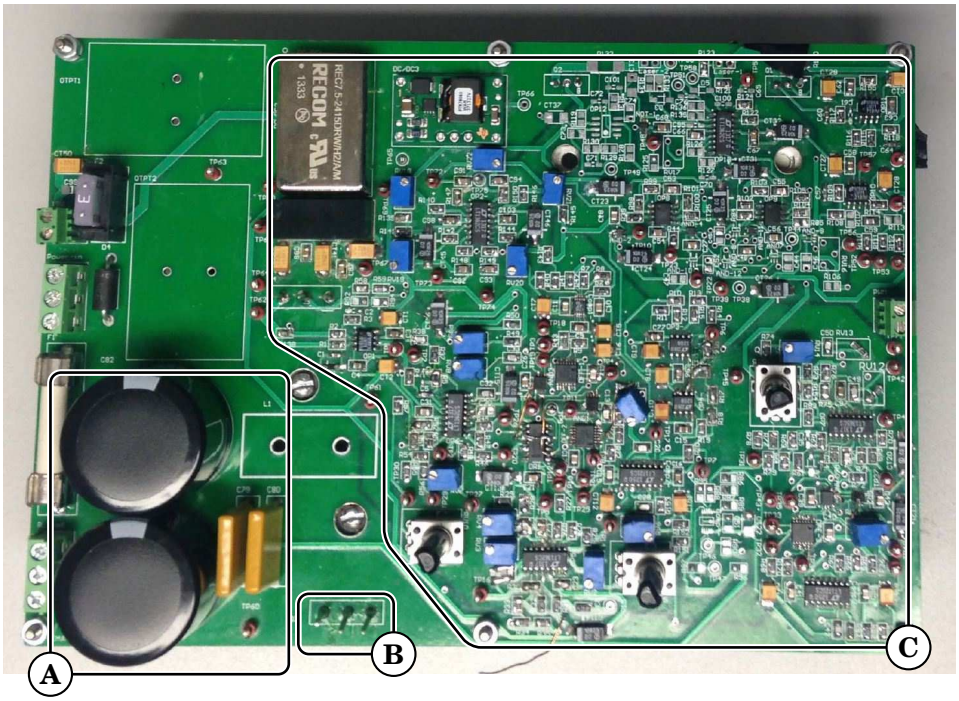

Figure 6.1: Photo of a closed-loop control gate driver implemented in [135]. (A) - The DC-link capacitance. (B) - The switching device. (C) - The active gate driver. Note that most of the board area is just the gate driver for one switching device.

[160] - this driver would seem to suit the application here. However, being closed-loop it requires very high speed components (an order of magnitude faster than the transition speed of the SiC MOSFET) making practical realisation complex. The work of [135] also suggests and shows the practical implementation of a driver for controlling the dI/dt and dV/dt of the switching device, though it is exceptionally complicated. Figure 6.1 shows the implementation of a single gate driver - note that the majority of the board area pictured is dedicated to the gate driver.

In contrast, the work of [95] has illustrated a gate drive for open-loop control of IGBTs which is comparatively simple. This design is used as the base of the design for use with the SiC MOSFETs in this work. The circuit diagram for the output stage of the gate driver is illustrated in fig. 6.2.

The chosen circuit design is based on an op-amp with a class-AB BJT stage in the loop. It has been manufactured on a PCB as shown in fig. 6.3. The finished circuit is able to achieve a full range signal bandwidth of 10 MHz while loaded with a switching device.

Each of the gate waveform profiles to be trialled is developed empirically using the specially

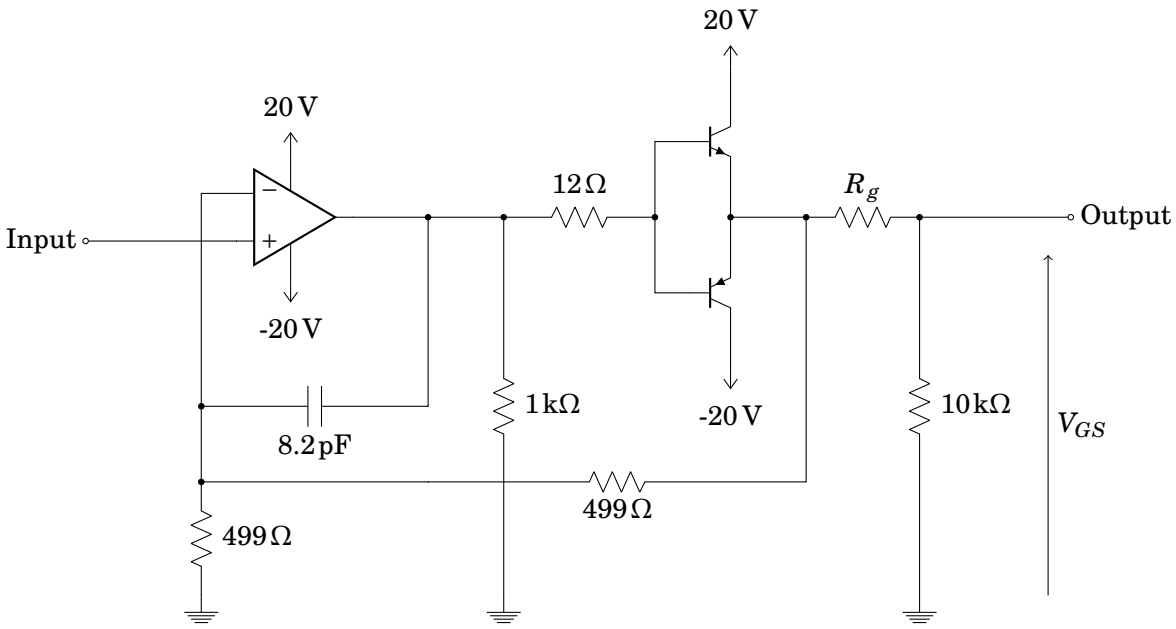

Figure 6.2: Linear gate drive output stage design

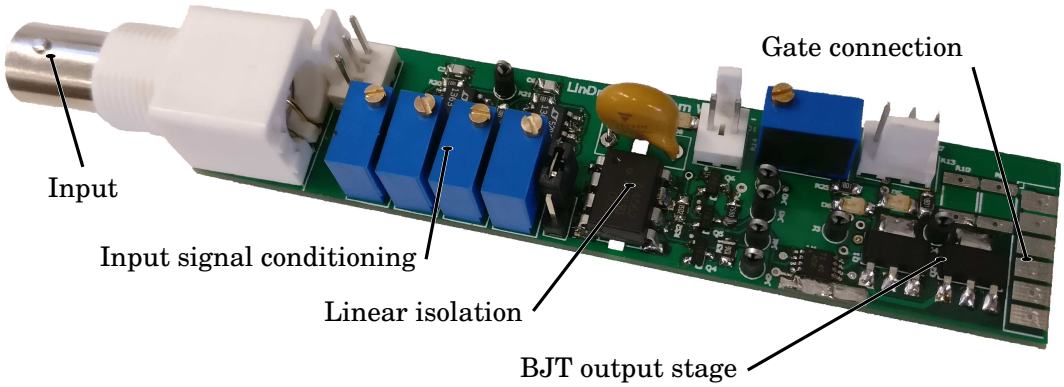

Figure 6.3: Third generation linear gate drive circuit for the application of profiled gate waveforms

developed waveform design tool illustrated in fig. 6.4. The waveforms are applied to the gate of the lower switching device using the linear gate driver in a DPT set up and the V_{DS} and I_D waveforms captured. The V_{DS} waveform is captured using a high voltage passive probe with the ground clip attached to the drain of the MOSFET. The I_D waveform is captured with a hybrid current clamp probe in the drain path. As the drain node is grounded no dV/dt will be applied

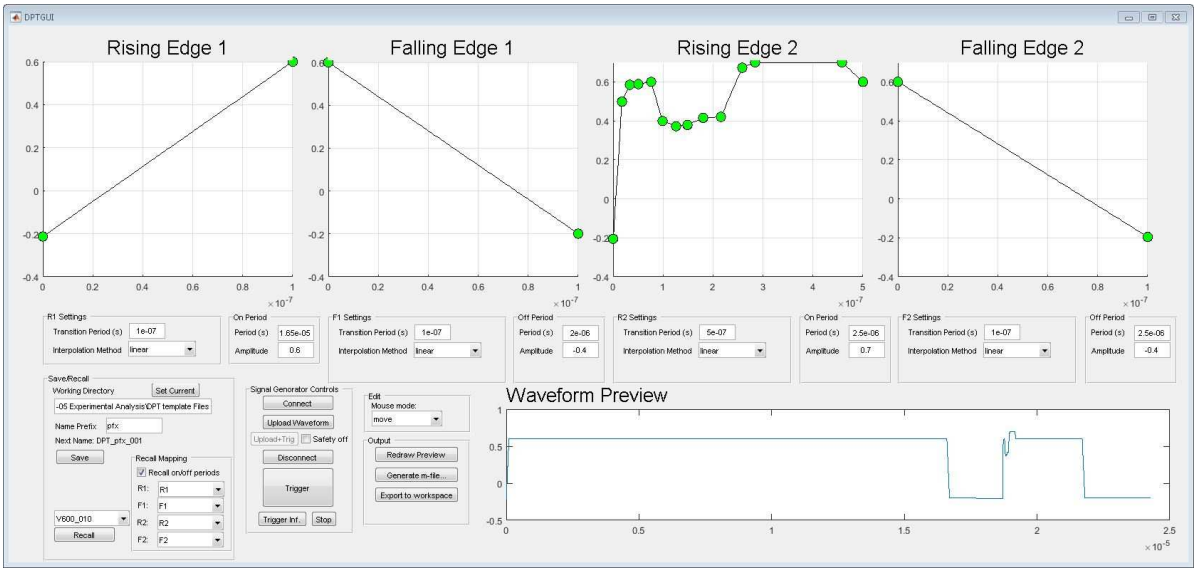

Figure 6.4: Software tool developed for the manual iterative development of gate waveform profiles

to the current probe.

The full experimental system is illustrated in fig. 6.5 - the waveform design and storage of the results is managed by the PC. The signal from the Arbitrary Waveform Generator (AWG) is isolated such that any device failures do not destroy the equipment. After this stage the signal is amplified, and applied to the gate of the device with the gate drive circuit discussed previously.

6.3 Experimental Results

Initial experimental tests are performed with a DC-link voltage of 60 V to prove the capability of the test set-up under safe conditions. Five different V_{DS} waveforms are produced under these conditions, presented in fig. 6.6. Also tested is the case where an un-shaped trapezoidal edge is applied to the gate of the switching device. The design of these waveform shapes has been directed by the objective of maximising the visual smoothness of the V_{DS} waveforms and making it as close to S-shaped as possible.

Metrics for the comparison of the 5 waveforms are computed and presented in fig. 6.7. The current overshoot and bandpower (30 MHz to 100 MHz) of every shaped case are improved when compared to the un-shaped case, though this is at the expense of increased switching loss. Shape

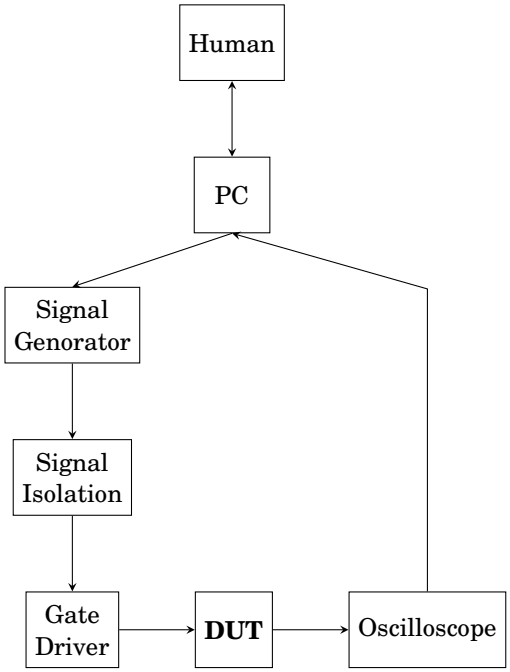

Figure 6.5: Design of the experimental system for fast iterative development of gate waveform profiles

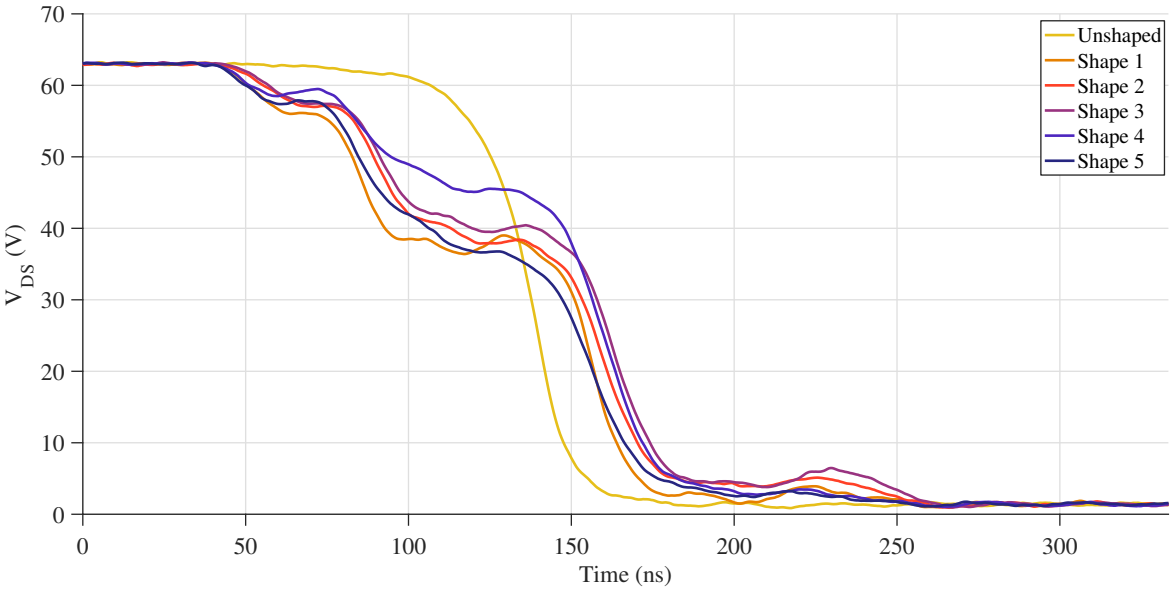

Figure 6.6: V_{DS} turn-on waveform profiles achieved in the 60 V DPTs

1 is the only exception to this - it achieves a large reduction in the switching loss. However, this is also a trade-off as the bandpower and overshoot are significantly increased. These results

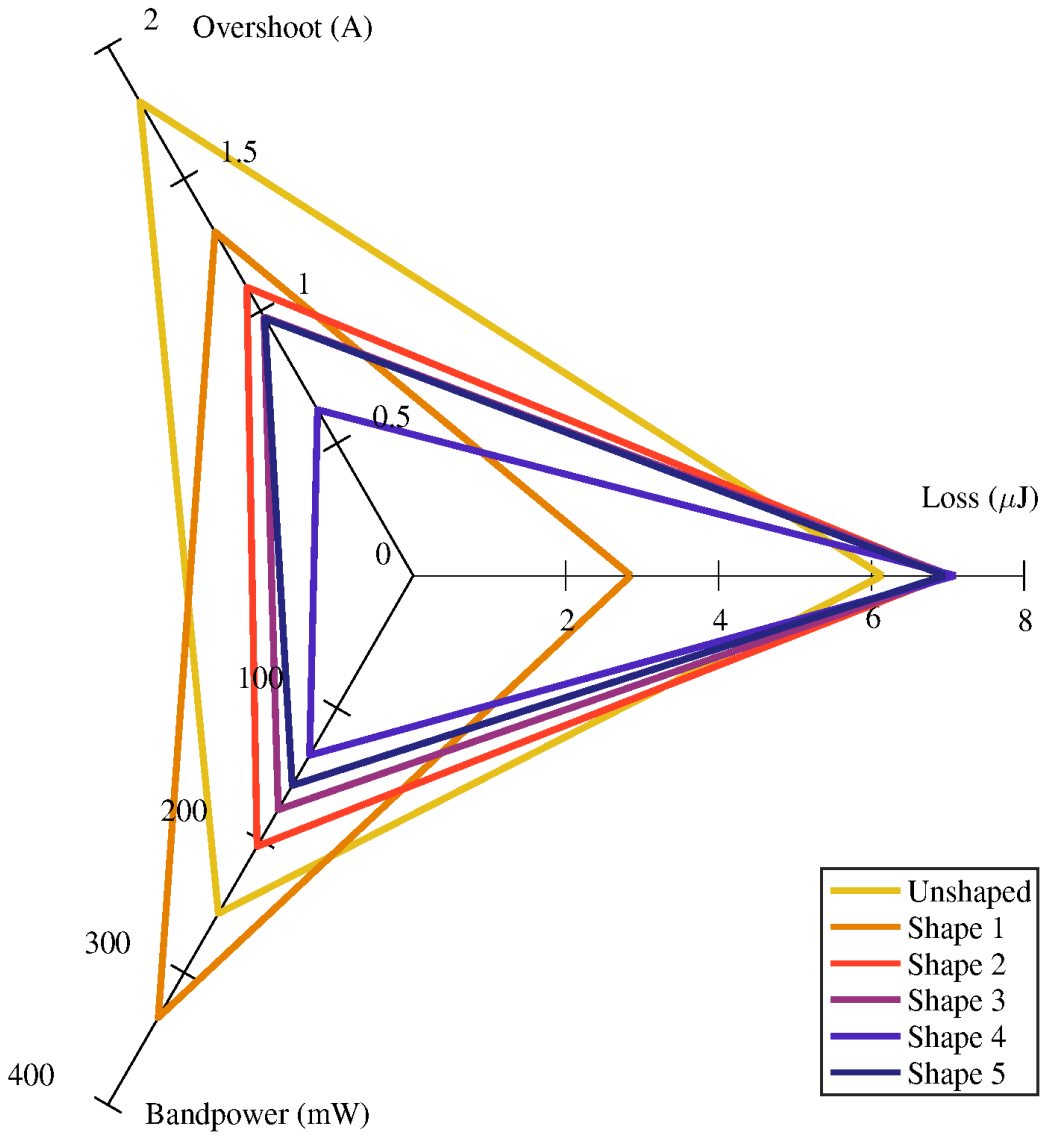

Figure 6.7: Comparison of the performance metrics of the five waveforms from fig. 6.6. For all three of the metrics presented here closer to the centre of the spider (ie. smaller areas) indicate better performance.

seem to show that transition shaping can improve the performance of some of the performance metrics, though at the expense of others.

Further results were captured under a range of operating conditions up-to a DC-link voltage of 600 V. With each set of conditions an un-shaped test was performed as well as a test with the best performance waveform that was achievable by eye. Figure 6.8 shows an example of the waveform shapes achieved at the maximum DC-link voltage and maximum drain current.

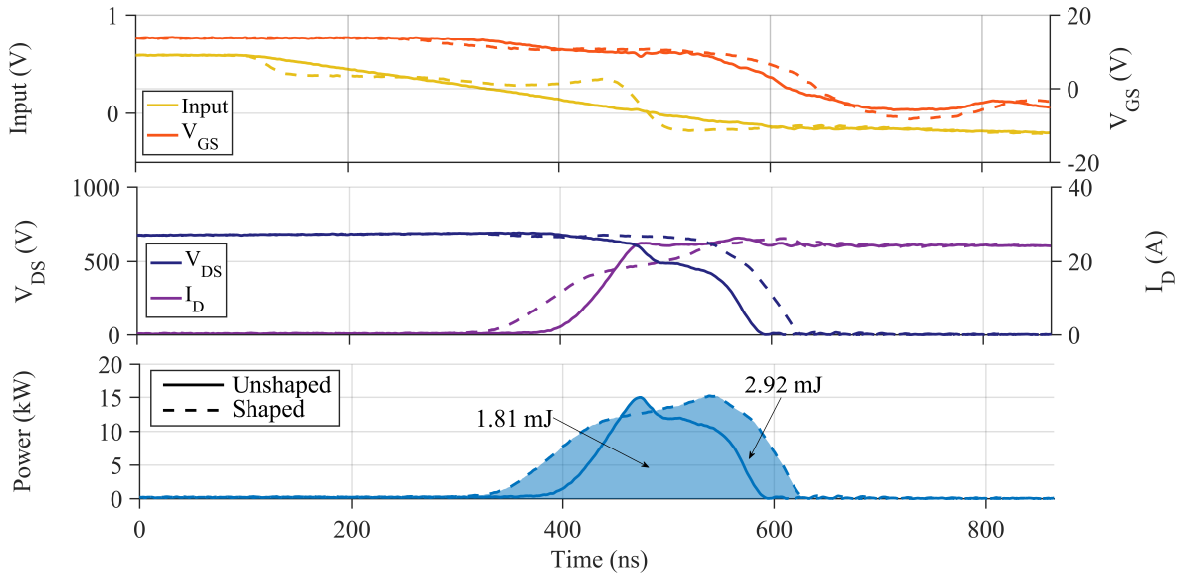

Figure 6.8: Comparison of the temporal waveform shapes from DPTs with V_{DS} = 600 V and I_D = 28 A showing the improved profile of the V_{DS} waveform

Though the figure shows that the shape has been affected in some way it is not apparent what performance implications this has other than the reduction in switching loss.

The experiments were carried out through the range of operating conditions and at each stage both turn-on and turn-off were independently manipulated to achieve the visually smoothest possible waveform. To compare the performance implications of the smoothing, metrics were computed in each case and the change from the value of the metric in the un-shaped case is presented in table 6.1. For each condition the turn-on and turn-off results are averaged to indicate the overall effect of the waveform smoothing.

The results presented in table 6.1 show that with the use of smoothing it is possible to decrease the current overshoot and in most cases it is possible to realise a reduction in the cumulative bandpower. However, it is also shown that the use of smoothing has led to dramatically increased switching loss in all of the cases explored here. This is not what was predicted, though the disagreement between the prediction and this result could be due to a number of factors. Firstly, the prediction was based on the application of a symmetrical transition waveform, which these excitations are not. Additionally, the optimisation strategy used was based purely on the visual interpretation of the waveforms shape, and not on the value of the metrics. As

Voltage (V)	Current	Switching Loss	Overshoot	Bandpower
240	10 %	+236 %	+5 %	+11 %
	50 %	+146 %	-13 %	+4 %
480	10 %	+19 %	-8 %	+122 %
	50 %	+75 %	-48 %	+58 %
	90 %	+21 %	-23 %	+237 %
600	10 %	+547 %	-29 %	-50 %
	50 %	+104 %	-16 %	+45 %
	90 %	+164 %	-26 %	-66 %

Table 6.1: Performance metrics achieved through the use of waveform shaping. Current is expressed as a percentage of the devices maximum rating. A negative change in any metric value indicates an improvement in that metric.

it is difficult to see from the V_{DS} waveform alone what the switching loss will be, it has been overlooked during the development of the excitation shapes. Optimisation of these metrics will require their consideration at the time of waveform development.

As the performance of the MOSFET varies with the operating conditions, such as switching current and junction temperature the ideal gate waveform profile required will also vary. The data-sheet for the C2M0080120D reveals the dependence of the capacitances on V_{DS} as well as the variation of the threshold voltage with temperature (0.5 V variation in the range 25 °C to 100 °C). As the conditions were varied for the DPTs each of the excitation waveforms used were captured and have been illustrated in fig. 6.9. These waveforms represent the excitations that produced the best smoothness in the V_{DS} waveform.

The excitations used in the turn-on of the switching device in fig. 6.9 indicate that the increase of the current level has some distinct impact on the characteristics of the excitation waveform required. As the current level is increased the level the excitation has to reach to begin the device switching transition increases - this indicates an increase in the threshold voltage with current. The time spent in the Miller plateau also seems to be reduced with the increase in the current level. Finally, it can be noted that the drive strength required at the end of the transition to finish the device switching transition must be increased with increasing current.

The turn-off excitations show some similarities to the trends seen for the turn-on excitations. Once again the drive strength required in the Miller plateau region increases with increasing

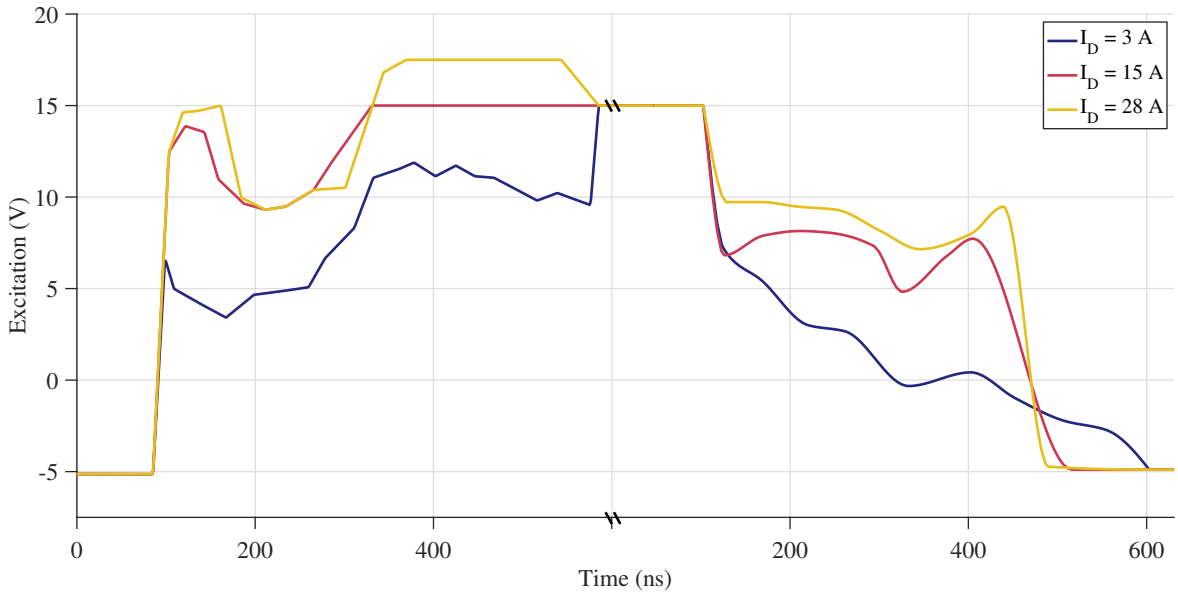

Figure 6.9: Optimal gate waveform profile under a range of switching currents with V_{DS} = 600 V. Left: turn-on. Right: turn-off. Note that the turn-off waveform has been fitted with a spline when being exported from the waveform design tool. The number of points used to create each waveform was identical when produced by the signal generator.

current.

The work of [162] has previously observed the increase in the Miller plateau level with increasing commutated current in alignment with what is observed here. The results here also show that as the current level changes other aspects of the waveform must be altered to continue to produce a useful excitation.

The experimental results here show that it is possible to shape the V_{DS} waveform of a MOSFET switching transition through manipulation of the gate waveform profile. While the performance implications of doing so are not positive in all respects as was previously predicted, it is demonstrated that significant improvement can be achieved in some metrics. These results highlight the limitations of the 'human in the loop' approach used. In addition to this, the requirement for considering a wide range of operating conditions when considering the effectiveness of waveform shaping is also revealed.

6.4 Summary

This chapter has shown how the theory of chapter 5 can be applied to physical experimental system. Firstly practical targets for waveform shape are discussed such that experimental work can be conducted. Following this, an experimental system has been developed which allows the fast iterative development of profiled gate waveforms for application to the gate of the SiC MOSFET in DPTs. The results presented show where it is possible to realise improvements to the performance while also highlighting issues in the system for development of the gate waveform profiles. The work here has also shown how the operating conditions of the system affect the required profile of the gate waveform. This indicates that it is important to carefully consider the applicability of any optimised waveform shape under a range of operating conditions.

CHAPTER 7

PASSIVE PROFILING GATE DRIVES

Waveform profiling has been shown by the work presented thus far to have the potential to control the switching performance metrics. However, a clear drawback of the proposed method is the exceptionally high complexity of the hardware to achieve even modest control of the gate waveform profiles. Such high complexity annihilates any of the positive impacts of the technique for anything but the most cost insensitive applications. This motivates the exploration of alternative techniques for realising the benefits of this technique.

A search of previous literature considering all switching devices technologies shows that a wide range of techniques have been employed for the task of waveform shaping. The approach in this work had been to use a voltage source gate-drive, whereas [138, 145] (amongst others) use an array of switched impedances within an ASIC. Others have shown some ability to influence the device performance through inclusion of additional gate-path components [184].

With motivation for finding a less complex technique for achieving profiled MOSFET switching waveforms and the knowledge that gate-path modification can be effective, this chapter will explore application of gate-path modification to the problem of waveform profiling.

The work presented in this chapter is closely supported by the author's publication "SiC MOSFET Switching Waveform Profiling Through Passive Networks" [185].

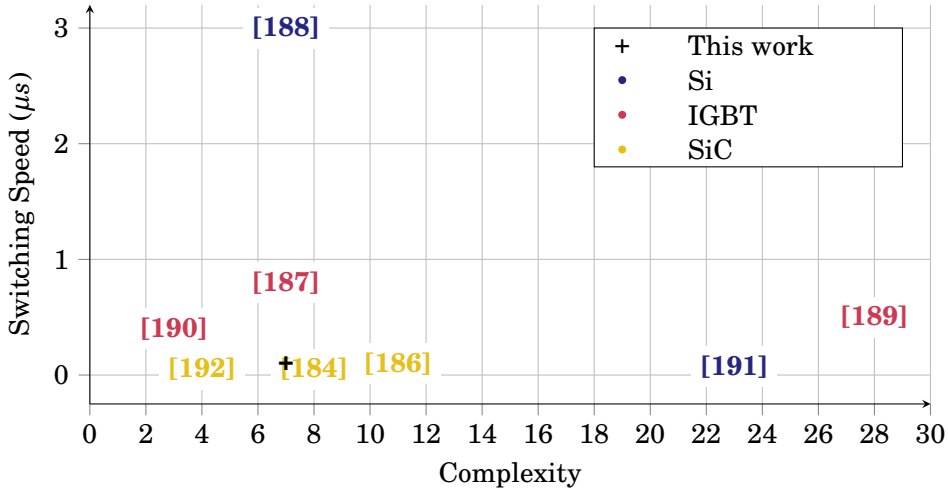

Figure 7.1: Comparison of the switching speed and complexity (number of additional elements) presented in previous works. The position of the driver proposed in this chapter is also shown for comparison

7.1 Design of a Passive Driver

Within the scope of gate-path modification, previous work has shown a wide rage of techniques applied to a range of device technologies. These are summarised in fig. 7.1 where the value 'complexity' has been loosely measured as a count of the additional components added to the gate-path over the standard fixed gate resistance driver. Full details on each of these works are also presented in table 7.1. The scope of interest has been extended to all device technologies as opposed to remaining focussed on SiC MOSFETs to allow consideration of all possible gate-path modifications.

The work of [184] is of particular interest as it presents a very simple network for controlling a SiC MOSFET at high speed. The design is centred around the use of 'speed-up capacitors' in parallel with each of the gate resistances. Variations in the value of this capacitance have a significant impact on the gradient of the turn-on and turn-off transients. This is an aspect of control that will be required in this work.

The work of [191] also implements a fast driver for the Si MOSFET, however, the design is very complex. Such complexity is comparable to the fully active gate waveform shaping investigated previously and is something that the design of the driver here should avoid.

Presented in [187] is a gate drive circuit for an IGBT which is able to profile the applied

Work	Technology	Switching Speed	Complexity	Publication Year
[131]	Non insulating WBG	n/a	5	2017
[184]	SiC MOSFET	50 ns	8	2017
[186]	SiC MOSFET	100 ns	11	2016
[187]	IGBT	800 ns	7	2008
[188]	Si MOSFET	3000 ns	7	2010
[193]	IGBT	n/a	1	2015
[189]	Insulated gate	500 ns	28	2003
[190]	Insulated gate	400 ns	3	2006
[191]	Insulated gate	70 ns	23	1996
[194]	GaN-JFET	200 ns	2	2011
[195]	SiC BJT	n/a	2	2017
[192]	SiC MOSFET	50 ns	4	2013

Table 7.1: Comparison of previous literature presenting simple gate drive designs for influencing the transition shape of switching device waveforms

rectangular waveform directly with minimal additional components. Though this design is not directly applicable to the SiC MOSFET used in this work, the adoption of this simple network for gate waveform profiling could be considered.

Reviewing the gate waveform profiles arrived at in section 6.3 (repeated in fig. 7.2) there are several key characteristics common to each of the profiles. Firstly, at the beginning of the transition a spike is required. Following this there is a gradually rising portion, and finally there is a sharp step to bring the voltage up to the on-state voltage quickly. As the switching conditions change the relative magnitudes of each of these elements varies, though each feature is still quite pronounced.

Simplifying the MOSFET gate as a purely capacitive load it is simple to construct a network to produce each of the features identified in the model gate profiles of fig. 7.2. Producing the initial spike can be accomplished when a rectangular waveform is applied to a series RC network - the gentle rise through the whole transition can be achieved with a series resistance - and finally, the step at the end can be created using a delay and another series RC network. The combination of these networks is proposed in fig. 7.3.

Having explored the achievements of previous work and using the basic gate-path modifications, the circuit of fig. 7.3 could be a promising candidate for producing the same profiles as were observed in the fully active shaping tests.

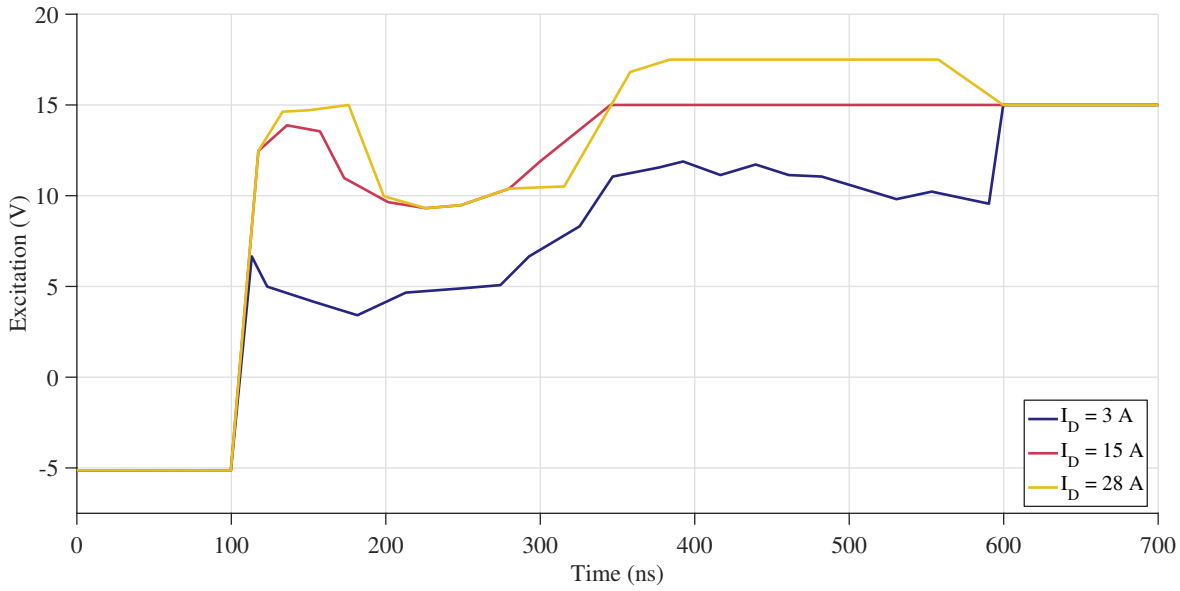

Figure 7.2: The turn-on excitations that were used during the fully active tests of section 6.3

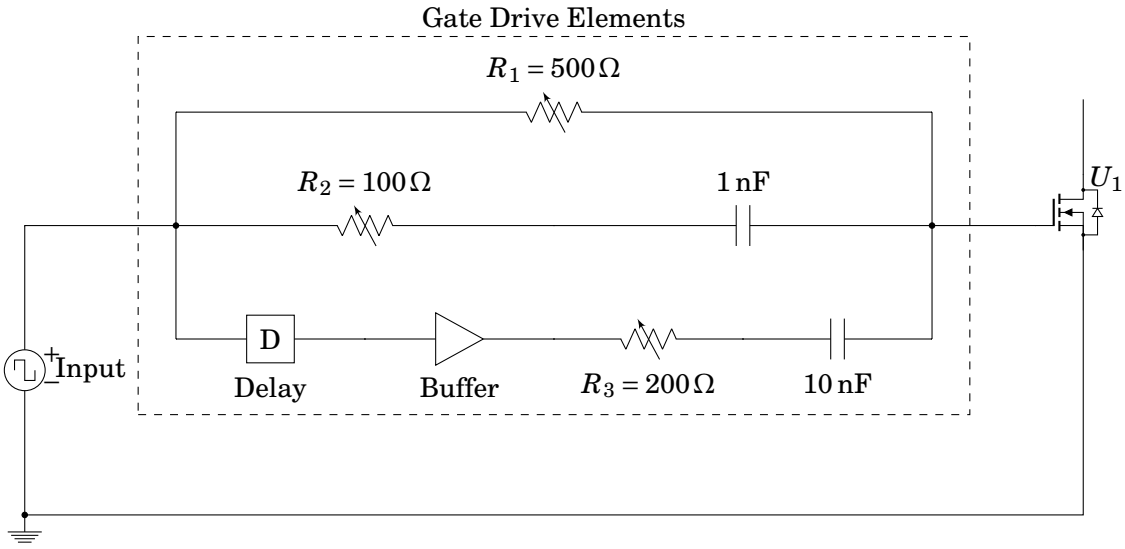

Figure 7.3: Design of a passive gate drive circuit with three gate paths for manipulating the gate waveform profile

7.2 Experimental Validation

Validation of the proposed passive gate drive circuit will be approached through simulation of the network, followed by experimental testing of a prototype.

7.2.1 Simulation

A simulation of the proposed circuit is created in LTspice. This simulation will test and inform initial values of the circuit components, as well as validate the fundamental operating principals before the design is committed to a physical test.

The simulation design includes the components illustrated in fig. 7.3 with the delay element emulated by a Schmitt trigger AND gate. The buffer is simulated by a repeat of the primary gate driver and the system is loaded with the SiC MOSFET model provided by CREE and used elsewhere in this work. The passive elements of the system are parametrised so that the effect of changing their values can be determined. The source waveform is square edged as the purpose of the shaping network is to shape a square waveform.

A selection of the simulated gate waveform profiles are illustrated in fig. 7.4. these shown that t_D controls the point at which the final 'step' response occurs and that R_2 controls the height of the initial spike as designed. Additionally, R_1 and R_3 have control of the overall charge rate and the step gradient, though these effects are convoluted with the effects of the other parameters. This indicates that changes in R_1 or R_3 will have side effects which will need to be countered for through variation of t_D and R_2. The control achieved with this simple circuit is sufficient to justify a physical implementation.

7.2.2 Initial Validation

To demonstrate a working passive gate drive, DPTs are done at a DC-link voltage of 60 V while varying some of the parameter values. This allows gate waveforms to be captured and evaluated with minimal risk of a destructive failure of the experimental set-up which could occur at 600 V.

The prototype passive gate drive is constructed on strip-board as shown in fig. 7.5. The resistors in the various gate paths are realised with multi-turn trimmer potentiometers - these allow accurate, fine grained control of their values to enable exploration of optimum settings. The primary gate driver is the linear gate driver used earlier in this work and the secondary buffer uses an identical output stage to this such that each path is matched.

R_1 was varied through the full range of 0 Ω to 500 Ω to investigate the effectiveness of the passive driver. Figure 7.6 shows the temporal waveforms resulting from this variation. It is

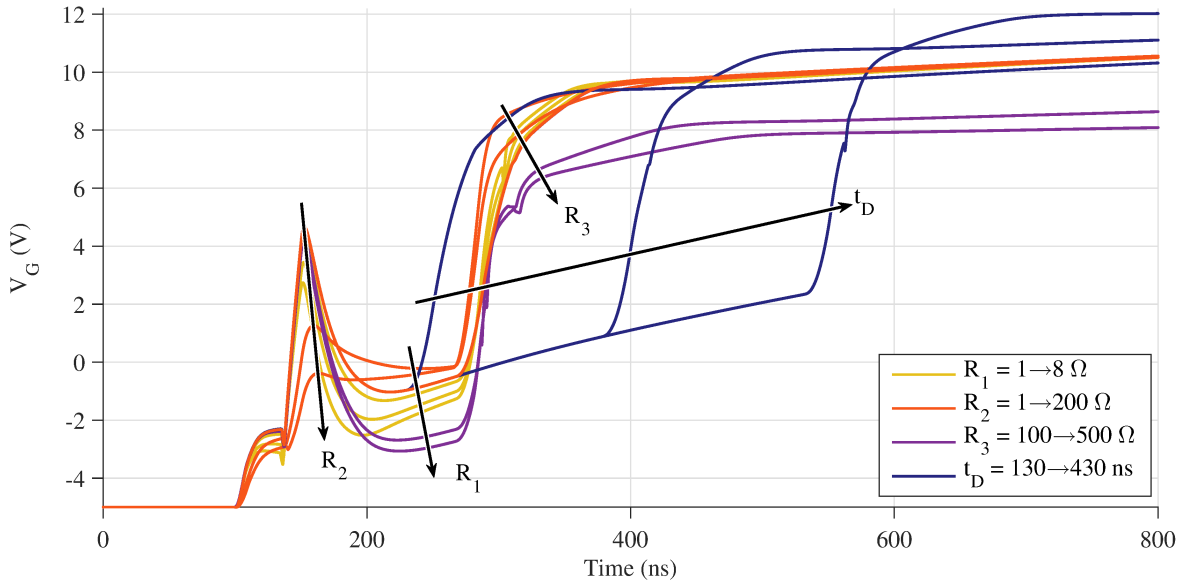

Figure 7.4: Gate waveforms achieved in simulation for the basic passive driver network showing the trend as each of the component values are changed

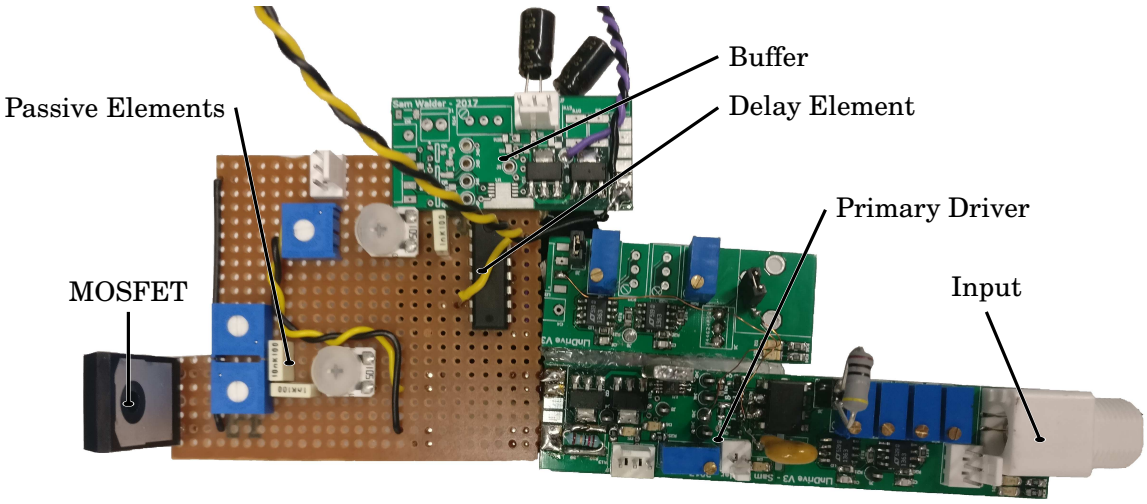

Figure 7.5: Prototype passive gate drive system

interesting to note that when R_1 is near its maximum value the rise of the gate voltage is so slow that the device switching transient is delayed by around 150 ns. It is also interesting to note that the highest values of current overshoot occur when R_1 is very low or very high.

To illustrate the impact of R_1 on some of the performance metrics for this transient the switching loss and current overshoot have been plotted in fig. 7.7. At low values the observed

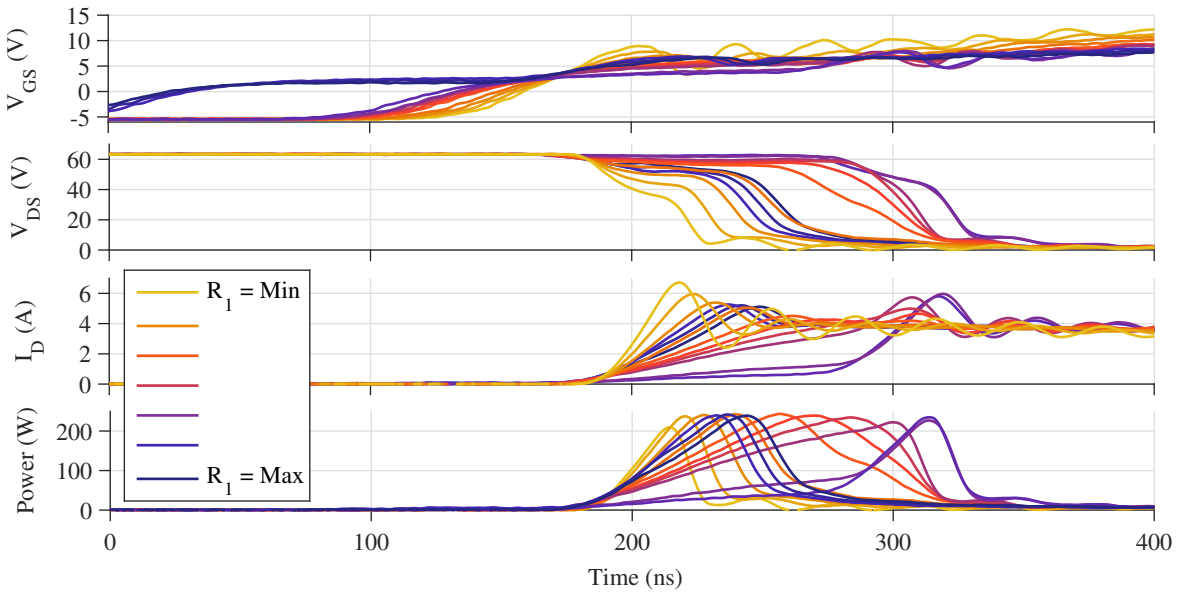

Figure 7.6: Temporal waveform variation as R_1 is swept in the prototype passive gate driver with $V_{DC} = 60\,\text{V}$

behaviour matches classic results - the current overshoot decreases with increasing R_1 and the switching loss increases. This is because R_1 emulates a classic single resistor gate circuit. At higher resistances the behaviour inverts, with an optimum point at around $R_1 = 425\,\Omega$. Referring back to the time domain waveforms in fig. 7.6 it is noted that this point corresponds to one where the rise of the gate voltage is so slow switching is delayed. The waveforms after the delay are actually more similar to those when $R_1 \approx 115\,\Omega$.

A search was conducted varying R_1, R_2, R_3 and t_D to find an operating point with minimised switching loss. The device waveforms resulting from this search are shown in fig. 7.8. The switching loss is similar to the minimum point seen previously in fig. 7.7 despite allowing further freedom in the control. This shows that performance optimums may be local optimums, and not global ones - this means that testing will need to be done in a way which prevents the search from becoming stuck at a local optimum point.

7.2.3 Automated Testing

To overcome the problems with local optimum points seen in the 60 V DPTs an automated test set-up is created. The design of this system is such that the values of the passive gate drive

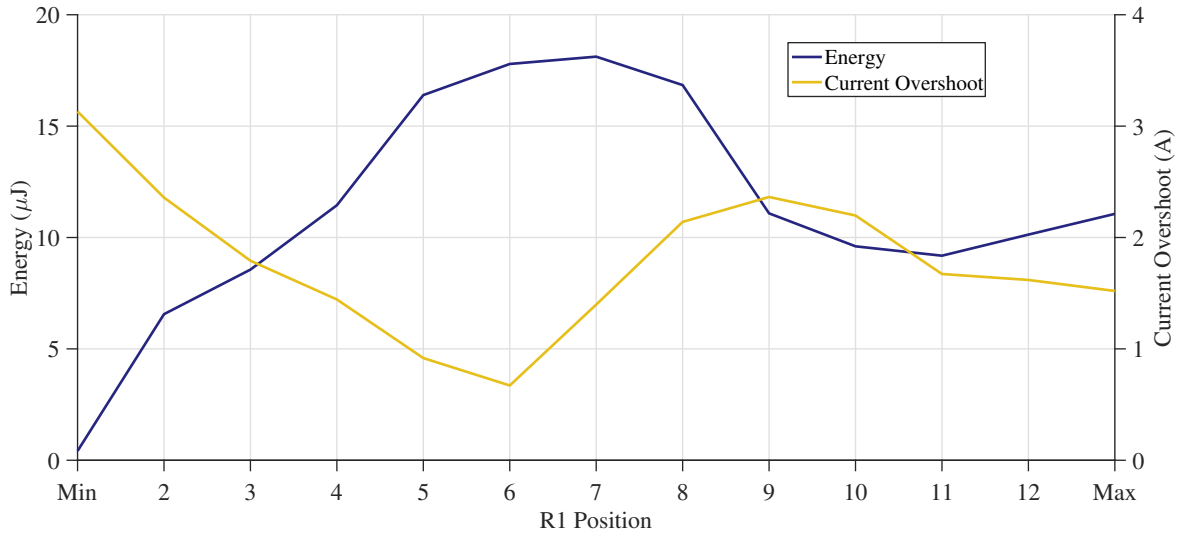

Figure 7.7: Variation of the switching loss and overshoot with R_1 for the prototype passive driver with $V_{DC} = 60\,\text{V}$

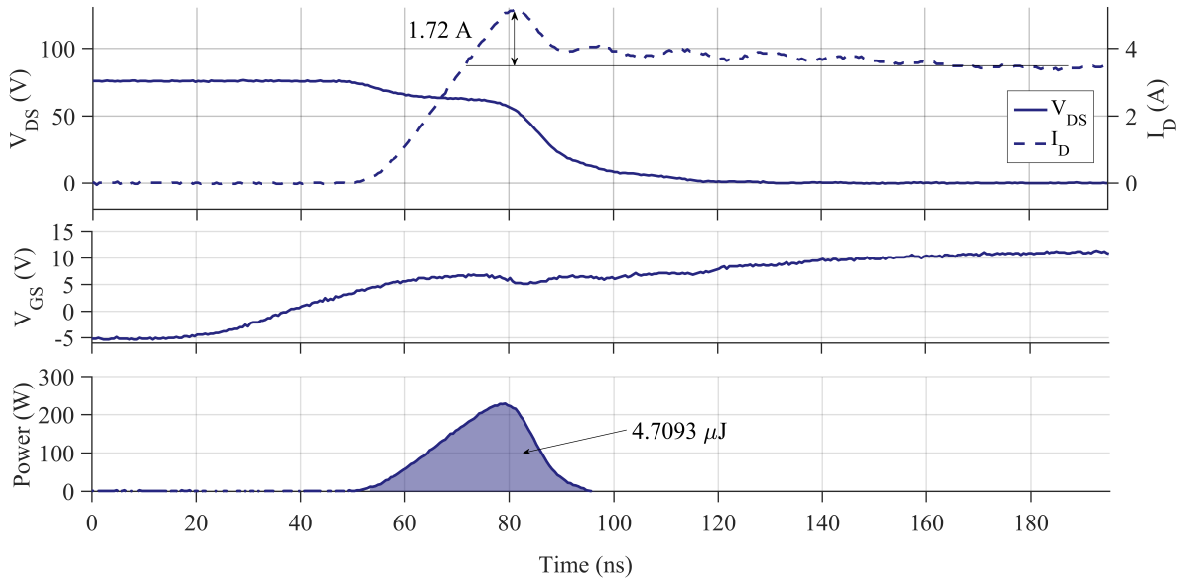

Figure 7.8: Minimum switching loss obtained during turn on with $V_{DC} = 60\,\text{V}$. All of the resistances were varied freely to find this operating point.

components can be varied with the system energised without risk to the operator. Tests can then be conducted in a low-resolution brute-force approach to gain initial knowledge about the shape of the search space.

The prototype passive gate drive of fig. 7.5 was connected to stepper motors as shown in

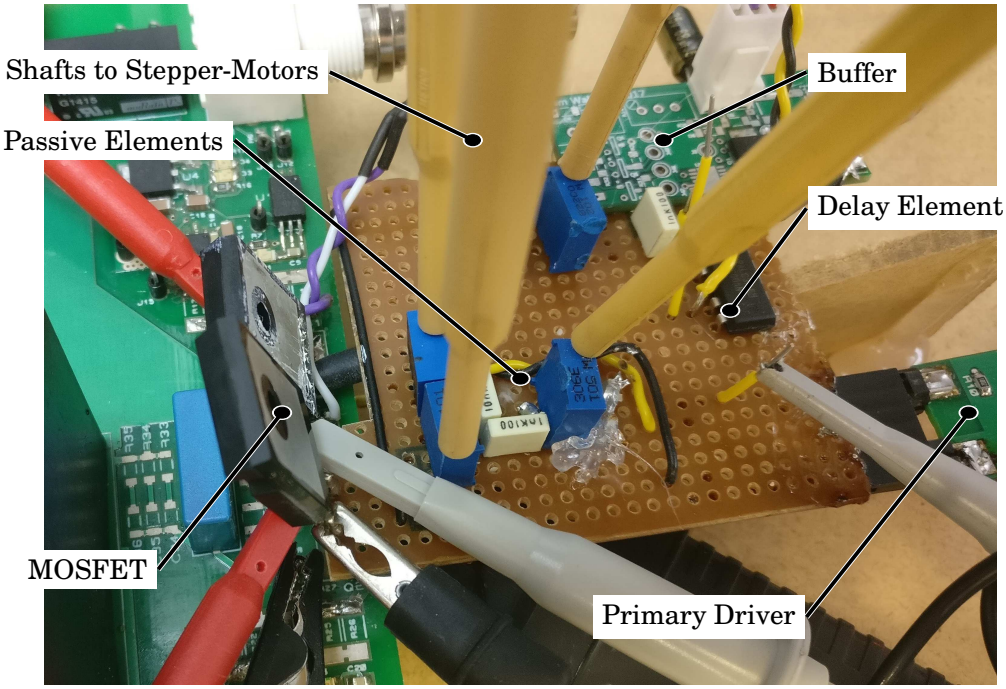

Figure 7.9: Prototype passive gate drive system in automated setup

fig. 7.9 such that their values could be accurately set in a repeatable fashion and with the system energised. The other aspects of the test set-up were also automated to allow a large number of tests to be taken in a short time and with a high repeatability.

The path resistances were varied in the ranges $R_1 = 50\,\Omega$ to $150\,\Omega$, $R_2 = 0\,\Omega$ to $20\,\Omega$ and $R_3 = 60\,\Omega$ to $200\,\Omega$. t_D was varied in the range 0 ns to 340 ns, the DC-link voltage was 600 V and the device drain current (I_D) was 10 A. The current overshoot and the switching loss are recorded for each of the operation points investigated. These results are displayed in figs. 7.10 and 7.11 in which the surface with the best current overshoot and the surface with the best switching loss have been displayed. The best switching loss occurs on the surface for which $R_3 = 30\,\Omega$, $t_D = 275$ ns and the best current overshoot is observed on the surface for which $R_3 = 200\,\Omega$, $t_D = 0$ ns.

The current overshoot at the point of device turn-on is illustrated in fig. 7.10 plotted against R_1 and R_2. The trend on each of the two surfaces is similar with a fairly uniform gap between them. In a single gate resistor gate drive the overshoot would be expected to be minimised with slower switching. Thus it is expected that the main influencer for the difference between the

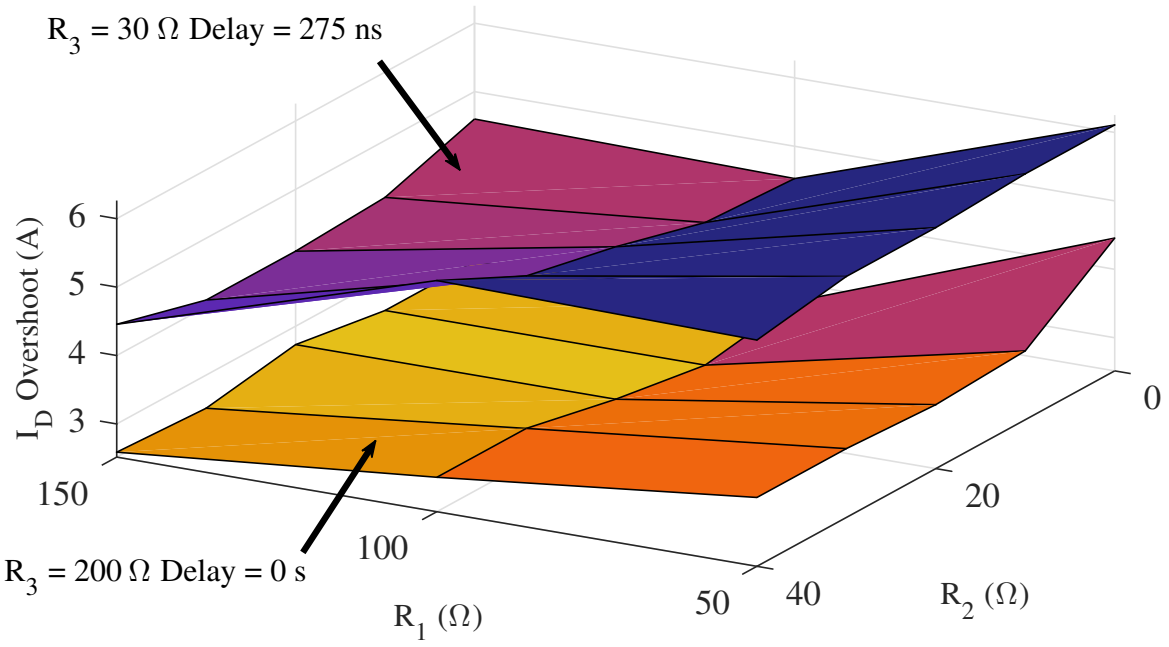

Figure 7.10: Current overshoot after turn-on with swept values of R_1 and R_2 showing surfaces on which the minimum overshoot ($R_3 = 200\,\Omega$, $t_D = 0\,\text{s}$) and minimum energy ($R_3 = 30\,\Omega$, $t_D = 275\,\text{ns}$) are found

two surfaces would be the value of R_3 as this can influence the switching speed - indeed the overshoot is minimised with R_3 at its higher value. Note that the point of minimised overshoot is also that where R_1 and R_2 are maximised - corresponding to the slowest possible transition time.

The switching loss is shown in fig. 7.11 in the same style as fig. 7.10. The trend here is less easily understood and requires more careful consideration. The surface on which $R_3 = 200\,\Omega$ shows a linear trend which suggests that as the speed of the switching transient is increased (corresponding to R_1 and R_2 decreasing) the switching loss is reduced. For the surface on which $R_3 = 30\,\Omega$ this trend is not followed and instead the trend suggests the switching loss is reduced with increasing R_1.

The mechanism for this trend is elucidated through investigation of the time domain waveforms for the points corresponding to the dotted line along $R_2 = 20\,\Omega$ in fig. 7.11. These are shown in fig. 7.12. While R_1 is high the gate driver does not actually reach a voltage level that will begin the device switching until the delay path energises. This means that in these cases

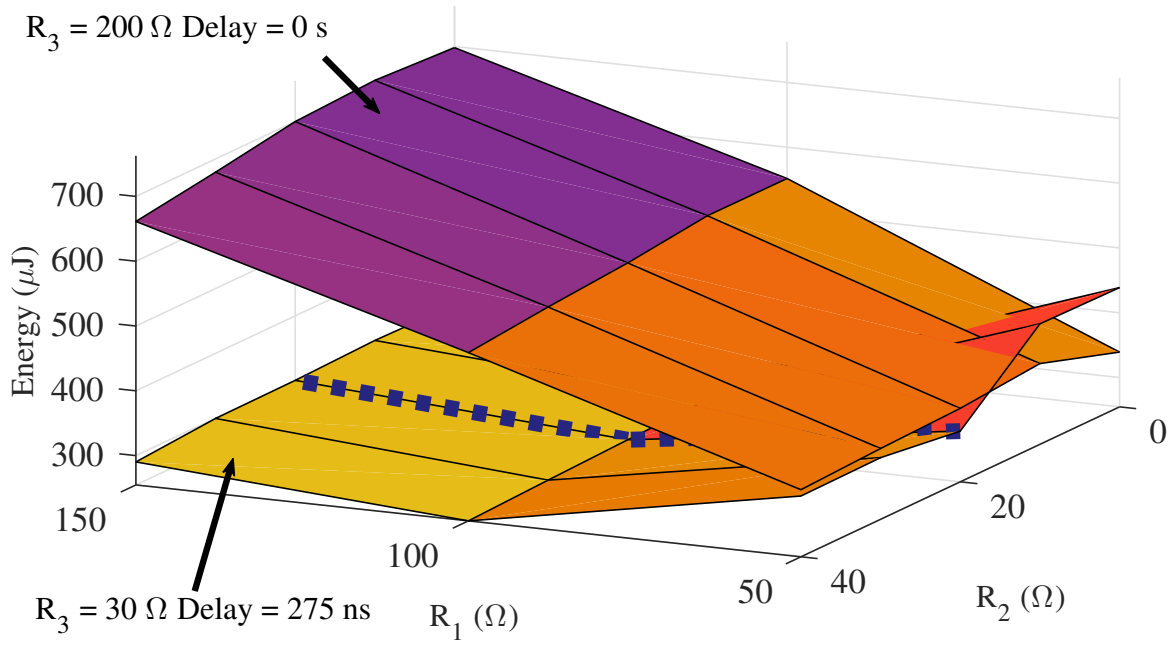

Figure 7.11: Switching energy during turn-on with swept values of R_1 and R_2 showing surfaces on which the minimum overshoot ($R_3 = 200\,\Omega$, $t_D = 0\,\text{s}$) and minimum energy ($R_3 = 30\,\Omega$, $t_D = 275\,\text{s}$) are found. The line along $R_2 = 20\,\Omega$, $R_3 = 30\,\Omega$ and $t_D = 275\,\text{ns}$ indicates points that will be explored further in fig. 7.12.

the value of R_1 is so high the path it is on is effectively not influencing the switching. As R_1 is reduced it comes to a point where it does begin to influence the switching waveforms, though it is too high to allow fast switching and instead causes the device to remain partially turned on for around 100 ns. This causes the unusually high switching loss.

These experiments have shown that a wide range of control can be obtained over the performance metrics for the device turn-on transient. It has also been shown that the interactions of each path are not limited to the waveform feature they were intended to control. This means that a lot of effort must be expended in producing useful settings of the passive components to achieve good performance. Though it has been shown that the metrics can be varied in a wide range, it is not clear how the performance of this driver compares with other alternatives. The next section will seek to evaluate the performance in relation to other gate driver options.

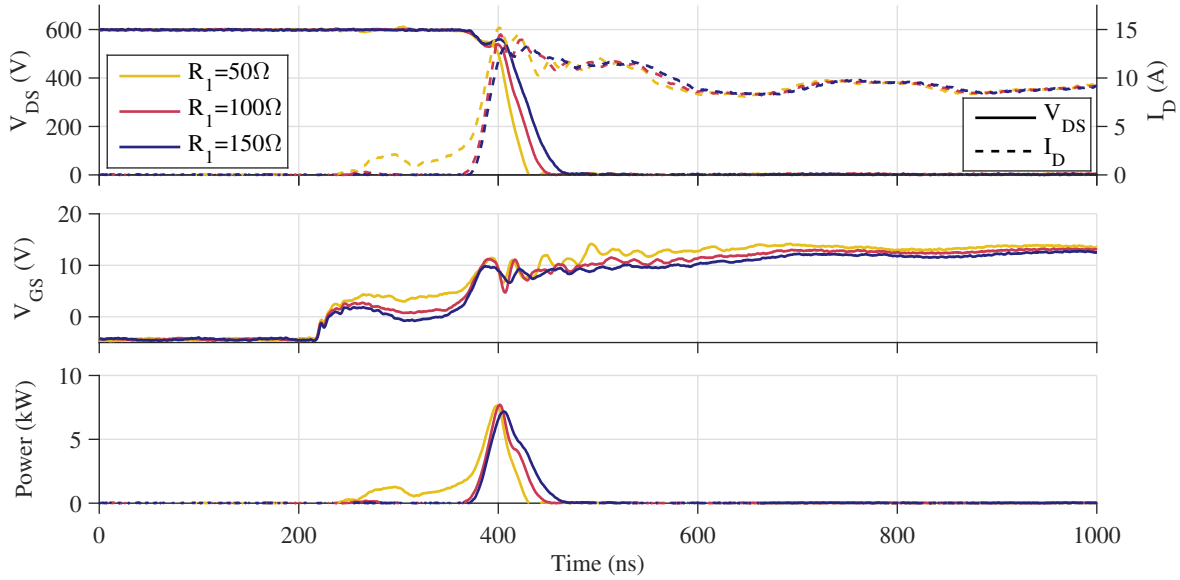

Figure 7.12: Temporal elucidation of the characteristics of fig. 7.11

7.3 Performance Evaluation

To evaluate the performance of the passive driver in comparison to the gate driving techniques explored already, performance metrics from each of the techniques will be compared. This analysis will allow the various performance trade-offs from each method to be evaluated.

When testing the active gate driver system with shaped waveforms the shapes produced tended to focus on the minimisation of the current overshoot as this was visible during the waveform design stage. Because of this focus the other performance metrics for these tests are in many cases very poor. As such many of those results are excluded from the comparisons here which results in three data-points with comparable performance.

The first metrics to be compared are the switching loss and the current overshoot. These are presented in fig. 7.13 - the bottom left corner at (0,0) represents the target performance (i.e. zero overshoot and zero switching loss). The points from the fixed gate resistance tests show the typical trend expected as switching speed and overshoot are traded off against each other - a higher gate resistance reduces the switching speed, lowering the current overshoot and increasing the switching loss.

The active shaping results here show the very low values of current overshoot discussed pre-

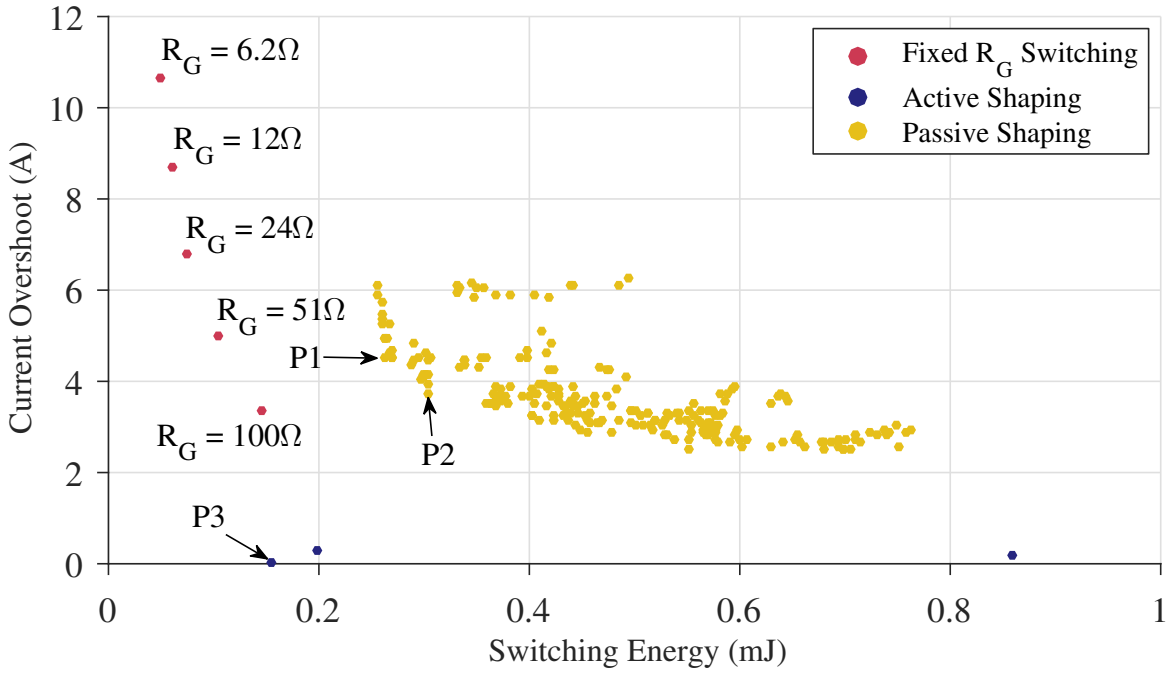

Figure 7.13: Current overshoot plotted against switching loss for a range of experimental tests illustrating that the passive shaping technique is not able to rival the performance of other techniques

viously, though only P3 competes with the switching loss achieved with the fixed gate resistance switching.

The points representing the passive switching results do not achieve switching loss or overshoot metrics that are as good as those for the fixed gate resistance switching or active shaping. This is a surprising result as in some of the limiting cases the passive gate driver will be the same as a fixed resistance gate drive - i.e. when R_2 and R_3 are very high R_1 will be the dominating effect.

Comparing instead the switching loss with the bandpower as in fig. 7.14, the passive driver is more favourable. As before, passive driving does not compete with fixed gate resistance switching, though it is able to achieve far better performance in terms of the bandpower. The active shaping results are leading with respect to the performance.

To clarify the mechanism for the difference in performance between the best of the passively controlled points and the actively shaped points in fig. 7.13, the points P1-3 are selected and their time domain waveforms shown in fig. 7.15. P3 shows the waveforms from an actively

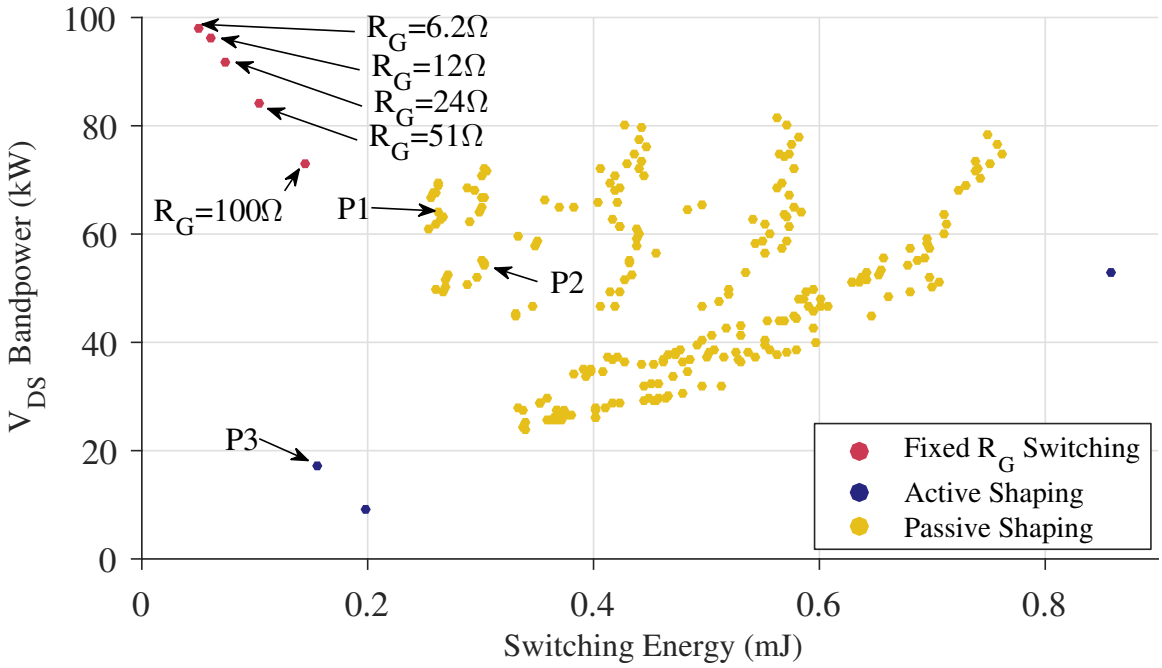

Figure 7.14: Bandpower metric against switching loss for a range of experimental tests

shaped transient with low switching loss, very low current overshoot, and low bandpower. The gate waveform shows that the passive shaping gate drive has not effectively emulated the gate waveform that achieves the best overshoot and bandpower metrics in this case. The actively shaped driver has been able to switch over a far longer time while still resulting in far less switching loss. This seems to arise from the beginning of the transition being too fast in the passive case.

Varying the excitation applied to a switching device will invariably have some impact on the transition time. This makes it challenging to fairly compare the waveforms here as they have very different transition times. The fixed gate resistance results have transition times in the range 20 ns to 80 ns, the actively shaped results have a range of 100 ns to 400 ns, and the passively shaped profiles have a range of 50 ns to 200 ns. Typically a faster transition rate is associated with higher EM generation as designers are used to using the trapezoidal model discussed in section 4.1 for analysis of these waveforms. Comparing the transition rate (dV/dt) and the EM generation capability (bandpower) of all of the test points in fig. 7.16 shows that this is not completely accurate. If this assumption were correct a perfect linear correlation should be

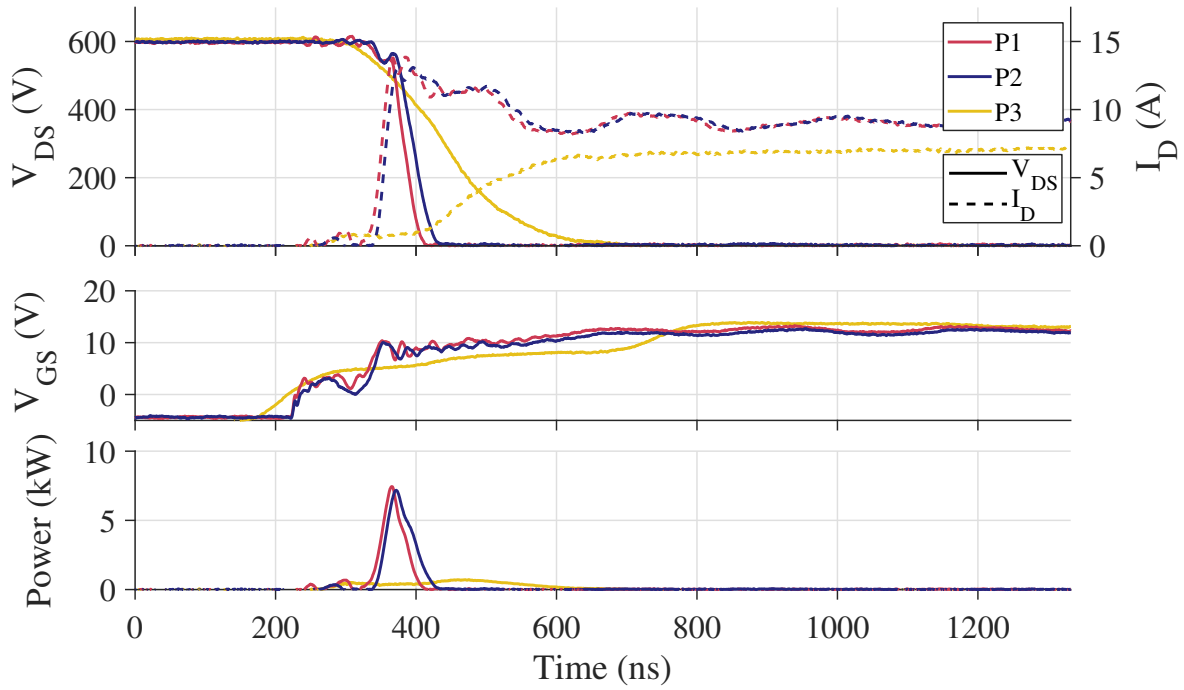

Figure 7.15: Time domain waveforms for the points P1-3 labelled in figs. 7.13 and 7.14 showing the very large reduction in switching loss achieved through the use of active waveform shaping.

seen between dV/dt and bandpower. The passively shaped results show that it is possible to reduce the bandpower independently from the switching speed.

The results here show that the performance of this prototype passive shaping gate driver is less than would be expected. Under certain conditions the passive driver should behave in the same way as the fixed gate resistance driver, therefore it should always be able to at least match its performance. This is not what is indicated by fig. 7.13 which suggests that there are fundamental implementation problems in the prototype design. Comparing the size of the strip board of fig. 7.5 with the fixed resistance gate driver in fig. 1.10 shows that the passive driver is far larger. This will introduce a large amount of parasitic inductance into the gate path which was shown to severely affect switching performance in section 3.1. Additionally, though the current design allows variation of t_D in the range 0 ns to 340 ns, it appears from fig. 7.15 that the delay should be at least 550 ns in order to emulate the performance of the actively shaping driver. Further work improving the performance of the passive shaping technique is justified by the results here.

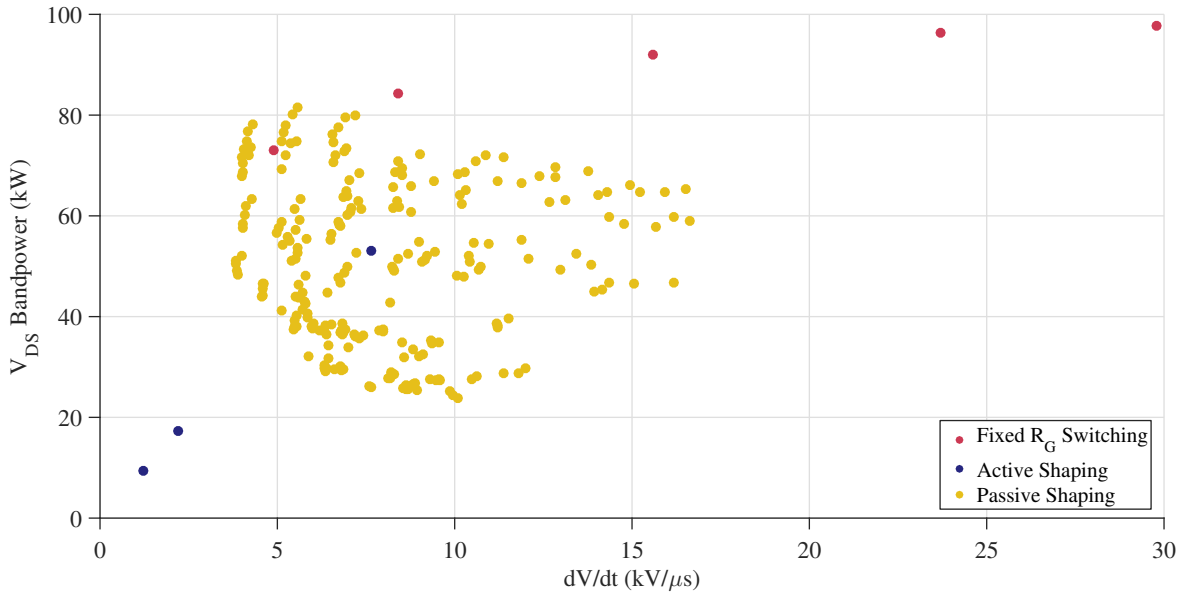

Figure 7.16: Bandpower plotted against the switching speed (dV/dt) for the range of experimental tests conducted in this work

7.4 Refined Design

The design of the prototype passive gate driver of the previous section has significant issues in that it introduced significant parasitic elements into the gate path along with the intended network. Despite this it was shown to be able to control various aspects of the switching performance. To attempt to compete with the performance of the other gate driving techniques that have been investigated, a PCB version of the board is designed that will reduce the gate path lengths and also use symmetrical driving stages.

7.4.1 New Driver

The new PCB based passive gate driver is shown in fig. 7.17. The two gate drive boards providing the primary and the delayed signal are based on the design of the driver integrated into the main test PCB so are a well proven design. These are connected close to the point where the device is also connected to reduce the parasitic inductance of the gate path as far as is possible while still allowing easy connection of the various elements.

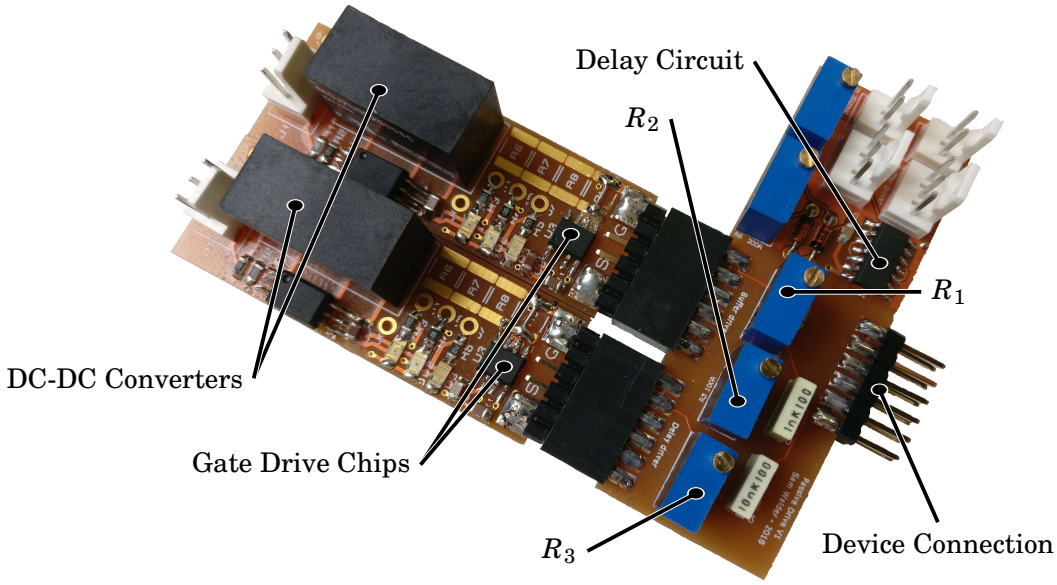

Figure 7.17: PCB based passive gate driver board with two standard SiC MOSFET gate driver boards attached

7.4.2 Initial Testing

The results with the prototype passive gate driver (fig. 7.13) showed that the proposed driver was not able to compete with even the basic fixed gate resistance case - for all cases of switching loss the fixed gate resistance driver was able to achieve a lower current overshoot. A similar result was observed for the case of the PCB based passive gate drive system of fig. 7.17. These initial results are shown in fig. 7.18 where, once again, the passive driver is unable to compete with the performance of the fixed gate resistance driving.

It was noted for the case where the prototype passive driver was used that it will introduce significant inductance into the gate loop, this was assumed to be why it could not achieve the performance of the fixed resistance driver. In the case of the PCB driver, the intention was for these parasitic elements to be reduced sufficiently for the performance to be comparable. It is reasonable to expect that the passive driver should be able to achieve the same performance points as the fixed gate resistance driver as this is just a special case of the passive driver in which R2 and R3 are high (i.e. only the first path of fig. 7.3 is active).

Further investigation in section 7.4.3 found that the use of the trimmer pots, as well as the length of the connections to the gate introduce significant parasitic inductance to the path. These

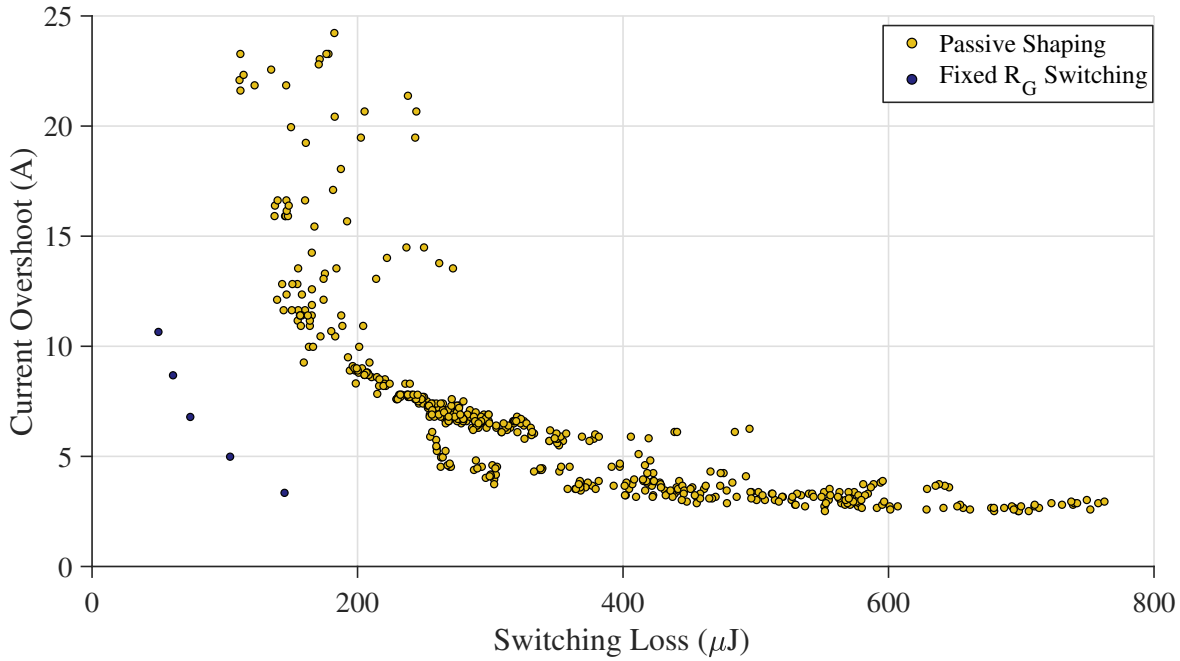

Figure 7.18: Comparison of the passively shaped driver performance with the original fixed gate resistance results showing that the proposed driver does not compete with the basic fixed resistance case

are elements that would not be introduced if the proposed drive topology were to be integrated onto the main PCB without using variable gate resistors, however, as this is an experimental setup, these features are required.

To allow fair comparison between the fixed gate resistance and passive driver results the two setups must share the same parasitic elements. To allow this, the fixed gate resistance tests were repeated using the passive gate drive PCB with the two additional paths disconnected. In this setup the two experiments share the same parasitics and are therefore more fairly comparable.

7.4.3 Measured Parasitics

The parasitic elements of the new passive gate driver were estimated from measurements of the path impedances taken with a Wayne Kerr 6500B precision impedance analyser. This also provides equivalent circuit parameters for the measured parasitic networks. The measured and estimated network impedances are illustrated in fig. 7.19. The PCB implementation of the passive gate drive in fig. 7.3 allows the impedance of the top two paths to be measured in parallel

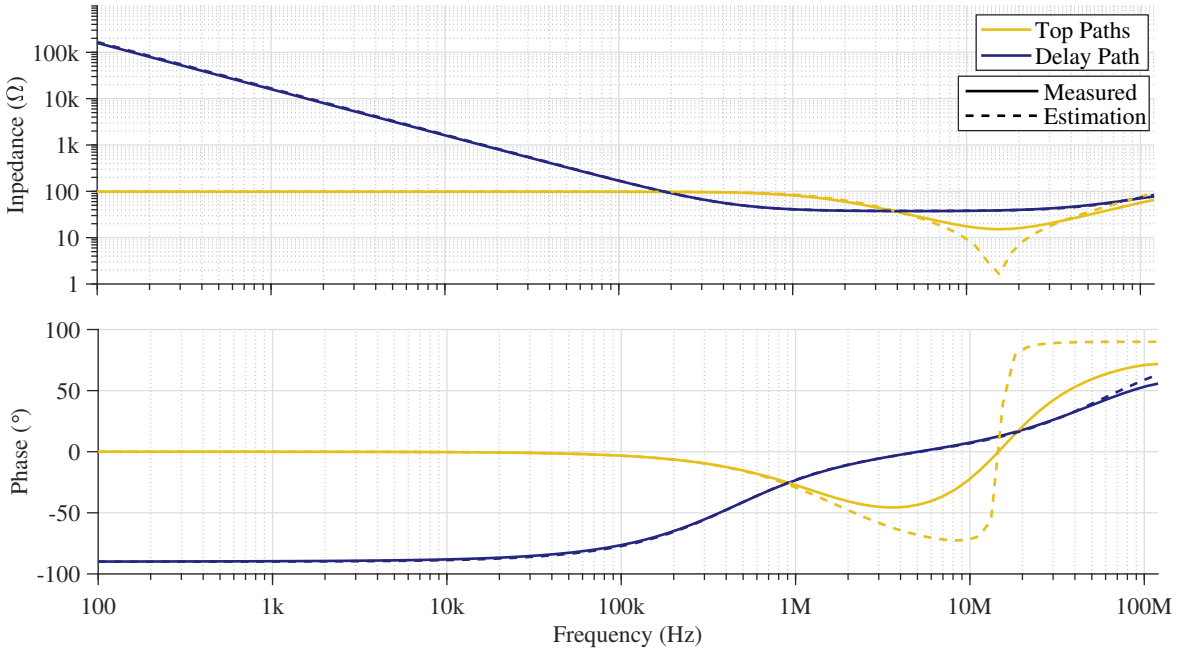

Figure 7.19: Illustration of the impedance of each of the two driver paths of the new passive gate driver with the equivalent circuit estimations.

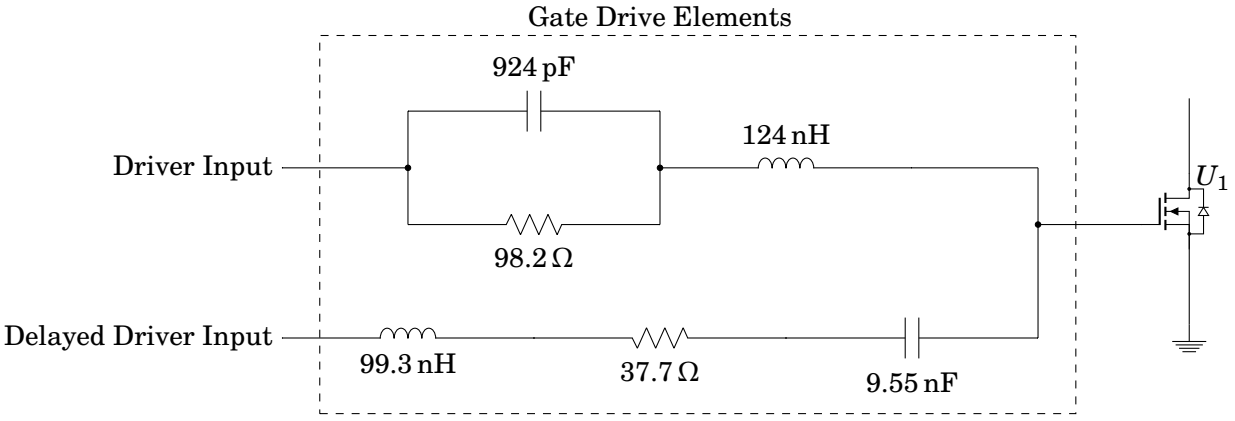

Figure 7.20: Equivalent circuit of the passive gate driver illustrating the measured impedance of each of the paths

and the bottom path to be measured separately.

The equivalent circuit estimations given by the impedance analyser can be used to redraw the equivalent circuit of the passive gate driver. This is illustrated in fig. 7.20.

Considering the top paths which are supplied by the non-delayed driver - the capacitance of 924 pF is similar to that of the design (1 nF). The resistance is controlled directly so is not

actually a parasitic element. The 124 nH of inductance in series with this is however a concern. This element has been introduced unintentionally and will slow the rate at which the driver can inject current into the gate of the switching device.

The bottom path presents a similar problem. The resistance measured is the directly controlled part, and hence not a parasitic element. The 9.55 nF capacitance measured corresponds to the 10 nF capacitor in the design. The 99.3 nH of inductance measured in series is not a designed element and will again slow down the rate at which the gate driver can inject current into the gate of the switching device.

7.4.4 Results

With the amended results for the case of the fixed resistance switching, the metrics of switching loss and current overshoot are plotted as in fig. 7.21. The results from the actively shaped switching are still by far the best performance, and the three points for this dataset can be seen to lie with a current overshoot close to 0 A. The fixed gate resistance results now sit within the space of the passively shaped results demonstrating that the comparison is more fair.

The passively shaped results shown here indicate that it is possible to increase the performance from the fixed gate resistance results in both the switching loss and the current overshoot. The point from the fixed resistance tests at the intersection of the dashed lines is taken as an example - from this point it is possible to decrease the current overshoot by 31 % or reduce the turn-on switching loss by 35.4 %.

The time domain waveforms for the points indicated by P1 and P2 in fig. 7.21 are compared with those of the fixed gate resistance point at the intersection of the dashed lines. P1 is a point from the passive dataset with similar switching loss to the fixed gate resistance point, but with minimised overshoot. P2 is a point with similar current overshoot to the fixed resistance point, but with minimised switching loss.

The V_{DS} and I_D waveforms measured on the actively driven device are shown in fig. 7.22. Both of the passively shaped waveforms have a slightly higher dV/dt than that of the fixed gate resistance case. The minimum switching loss case has the fastest dV/dt and dI/dt but manages to maintain a smaller current overshoot than that of the reference case.

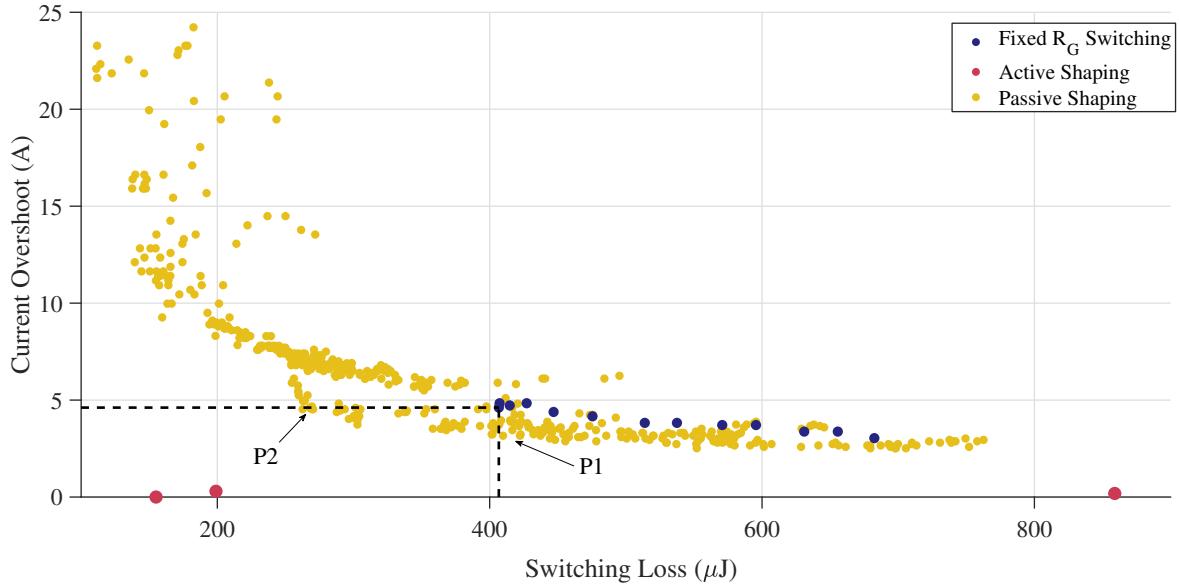

Figure 7.21: Illustration of the performance trade-off for switching loss and overshoot of the three gate drive technologies. The dashed lines intersect the fixed gate resistance setup with the lowest switching loss. P1 and P2 indicate the points from the passive gate driver results that will be investigated further.

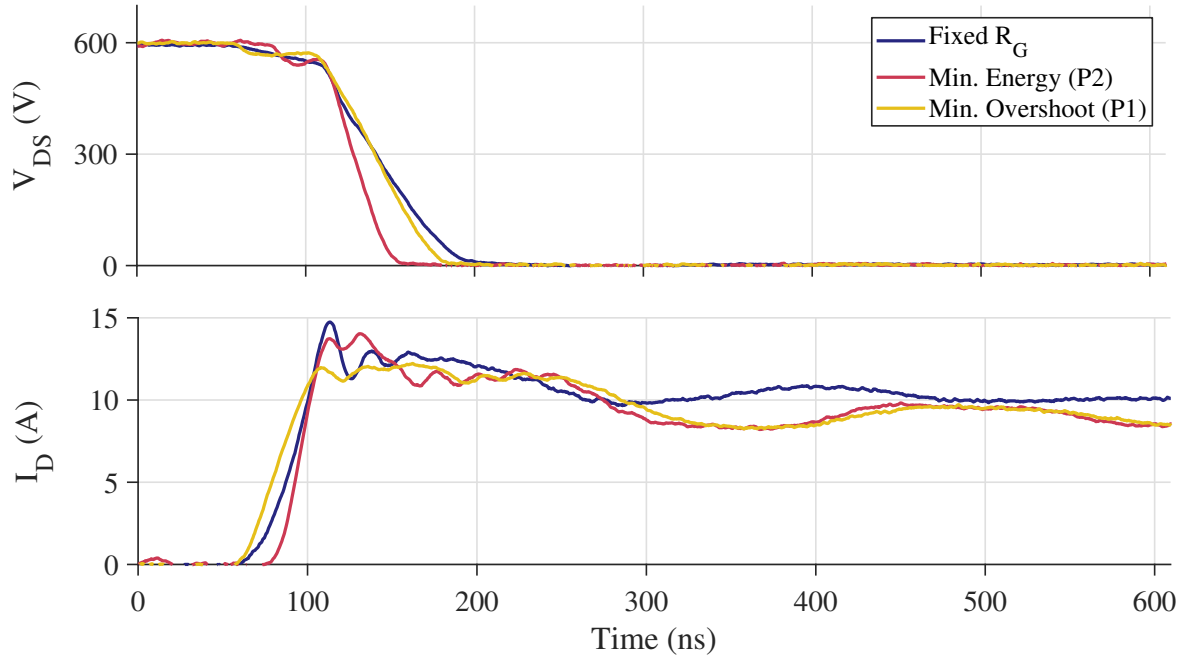

Figure 7.22: Comparison of the temporal waveforms for the points annotated in fig. 7.21

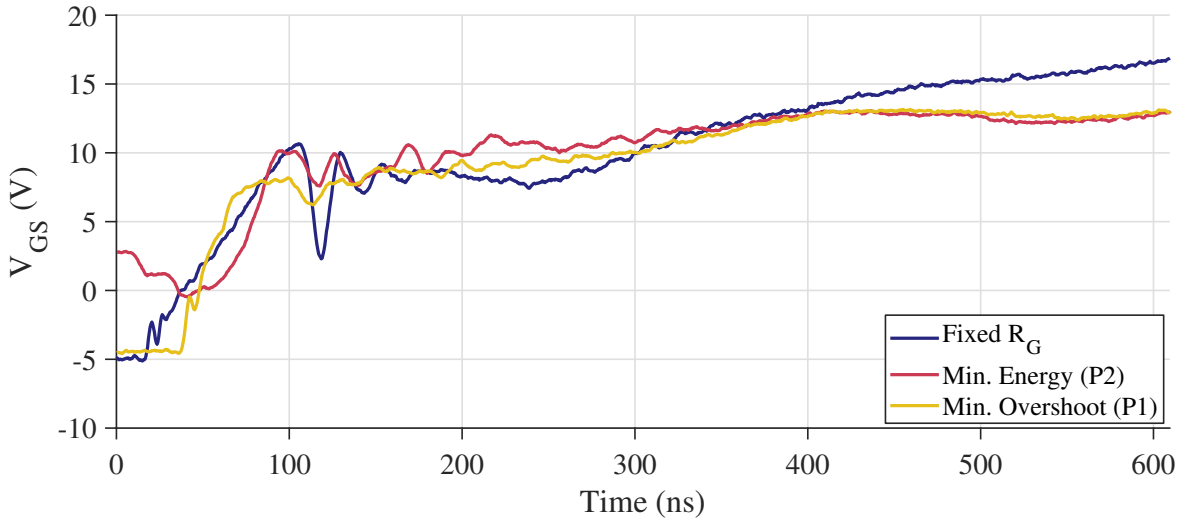

Figure 7.23: Comparison of the gate voltage waveforms observed at each of the operating points annotated in fig. 7.21. Note that in the case of the minimum energy waveform, the impedance of the driver is such that the gate is charged to a voltage just below the Miller plateau approximately 100 ns prior to the point where the device begins switching.

The gate voltage waveforms for the three operating points are compared in fig. 7.23. These waveforms are dominated by the coupling of noise from the nearby high dV/dt transient to the probe, making assessment of the detail difficult. It is interesting to note that the initial rise of the waveform only reaches around 10 V in any case before rising to the full holding voltage relatively gradually. Surprisingly the case in which minimum overshoot is sought has the highest dV/dt within the −5 V to 10 V region - typically we would associate this with faster, and hence more aggressive, switching characteristics.

The difficulty in identifying the key features of the gate voltage waveform suggests that clearer results would be obtained if the current waveform were also observed. Such measurement would require redesign of the test PCB to incorporate the passive gate driver and the measurement circuitry - this is out of the scope of this thesis.

Using the voltage and current waveforms of fig. 7.22, the dissipated power in the device can be inferred - this is illustrated in fig. 7.24. The power waveform for the case where minimum energy was sought shows a peak amplitude close to that of the original fixed gate resistance test. However, this peak is far sharper than the others, offering it the lower total energy dissipation. The case of minimum overshoot has a lower peak value of power, but an almost identical energy

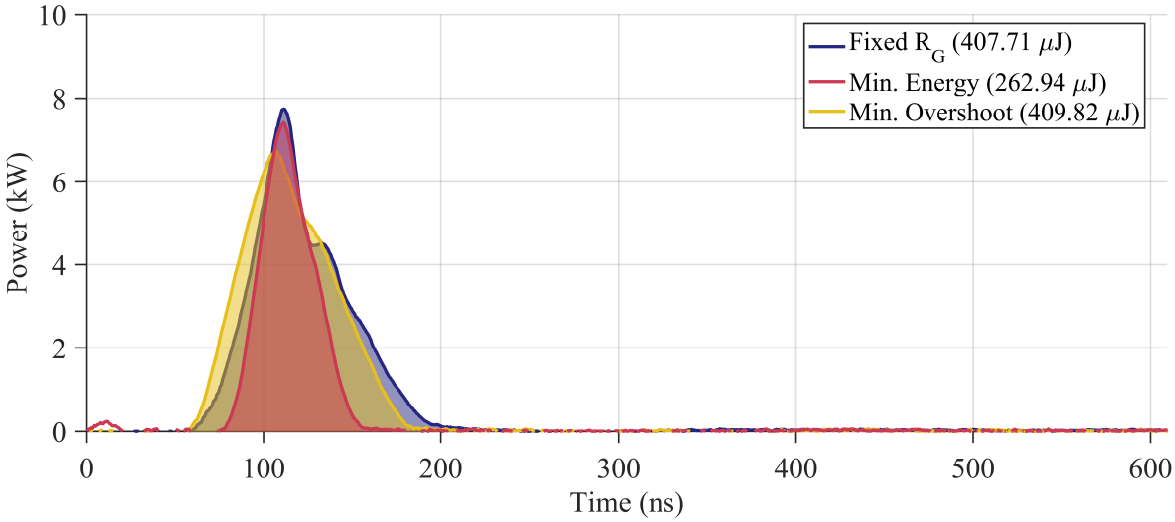

Figure 7.24: Comparison of the switching power and energy for the three cases annotated in fig. 7.21

dissipation - this is because it was picked explicitly from fig. 7.21 to have these characteristics.

7.4.5 Varying Current

An important question for any new gate driving technology is that of how it will perform under varying conditions. As inverter applications will require a sinusoidal output, the current and voltage levels will be perpetually changing. Thus far the DPTs performed have been conducted with I_D at 10 A, giving no indication of the performance of the driver as the current is increased or decreased.

As part of the testing with the PCB based passive gate driver the experimental setup was updated to automatically vary the current level with each test. This allows exploration of the performance of the gate driver at several current levels. The performance results of the PCB passive gate driver are presented in fig. 7.25 where the value of I_D at turn on was one of 3 A, 10 A or 28 A.

As the current in the device is increased, fig. 7.25 shows that the achievable range of operating points shifts higher on the current overshoot axis, and shifts much higher on the switching loss axis. It is not surprising that at higher current levels the switching loss will be increased, as it will take longer for the current to transition, making the power dissipation will be higher

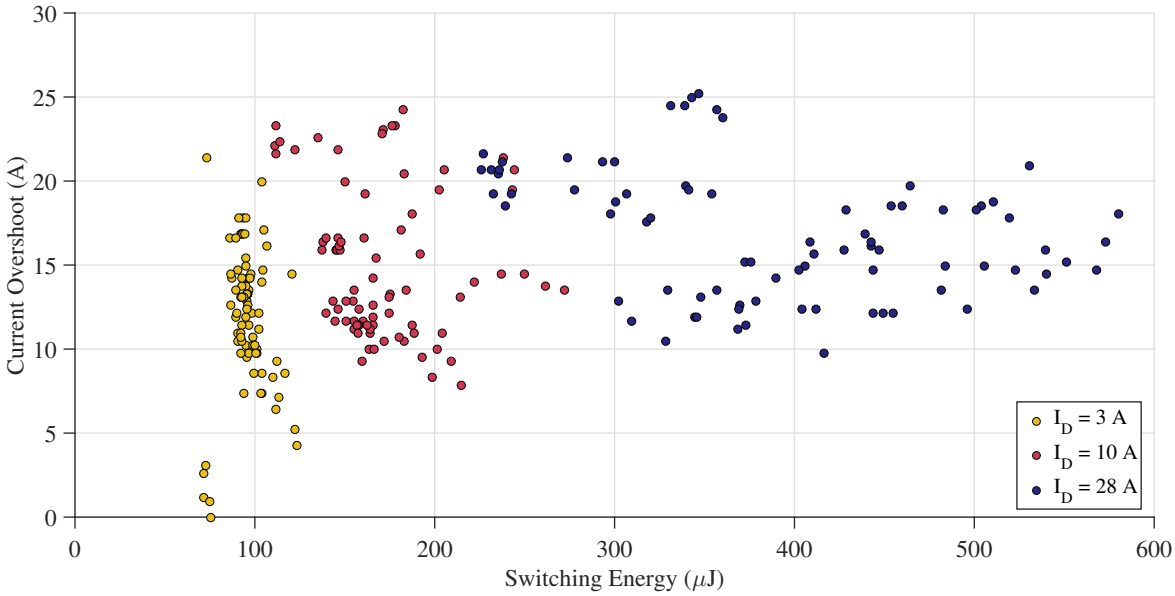

Figure 7.25: Performance of the passive gate drive with varying levels of current

throughout the transition. The current overshoot however is not as strongly influenced by the current level. This means that the current overshoot can be kept down in most all cases.

The limited variation in the current overshoot with the current level suggests that this is most strongly influenced by an effect other than the current level. This is supported by the results that were observed previously in section 3.1.1 where it was shown that the overshoot is a combination of the diode RRC which does vary with current, and other contributions such as the output capacitance inrush current, which will not vary with current level.

Though fig. 7.25 shows how the result space of a passive gate driver moves with the current level in the switching device it is only a very preliminary step towards realising such a driver in an inverter application. In order to satisfy the goal of simplicity in such a driver a practical version would need to use fixed values of resistance. This constrains the operating space to just one of the values illustrated, and though it is simple to determine this value under one set of operating conditions, the compromise that would have to be made to jointly optimise the performance under the range of realistic operating points presents a difficult challenge. Further analysis of the data is required to determine this optimum operating point.

Additionally, at present only changing current has been explored. In reality the converter

will likely need to be operated with a range of loads connected to the output as well as under a range of output voltages. These are parameters which as of yet are unexplored.

7.5 Summary

This chapter has explored the creation and implementation of a passive gate drive circuit for achieving shaped transition profiles for the SiC MOSFET. By considering the state-of-the-art in gate drive design and the excitation profiles used during the fully active gate drive tests a simple gate drive network is proposed.

This design has been implemented in a prototype form and tested in turn-on DPTs at 600 V. The experimental tests have shown that through variation of the driver's passive component values it is possible to influence the shape of the switching transients.

The results from the passive driver have been compared with those from the fixed resistance switching tests and the fully active shaping tests to evaluate what performance benefits the passive driver may allow. Though in many of the performance metrics the driver has not competed with the other switching techniques the results have highlighted specific issues with the prototype design, and solutions to these issues have been proposed. Several of the performance metrics investigated appear to be more controllable through the use of the passive gate driver, in particular, the EMI generation capability of the waveforms can be reduced significantly through the use of this driver without major reduction of the switching speed. Despite the limitations of the prototype, comparing this driver with other works as in fig. 7.1 show that this driver furthers the art of simple passive gate drivers.

Implementing the passive gate driver on a PCB was expected to reduce the parasitic elements sufficiently to allow this driver to compete with the original fixed gate resistance gate driver. It was found that the use of the trimmer potentiometers was the greater influence and prevented the characteristics of this driver from competing with the original driver. As such, the fixed resistance results were repeated with more comparable test conditions and it was found that the passive driver was then able to shift the performance from these points to achieve lower switching loss and lower current overshoot than the fixed value driver.

The extended testing performed with the PCB based driver showed that the current level has a significant impact on the performance that can be achieved. It was highlighted that understanding this impact is an important first step towards the realisation of a passive shaping driver in an inverter application. A practical implementation of this driver would not be able to use adjustable resistances and hence a position of optimal compromise between the performance under the various conditions will be required. Further testing is required to determine the performance of this driver with different load configurations and different voltage outputs.

Throughout this work on the passive shaping drivers only the turn-on transient has been considered. However, it is proposed that a similar network could be used to independently control the turn-off transient. Alternatively, if the performance gains are sufficient, then the turn-on circuit could be tuned to reach a compromise between both the turn-on and turn-off performance. Though feasible, this would be a complicated optimisation, as it would also have to take into account the other optimisations that must be performed as discussed previously.

CHAPTER 8

CONCLUSIONS AND CRITICAL REVIEW

The body of work presented has explored and expanded the area of waveform shaping, and in particular, passive profiling gate drives. This chapter will reflect upon the findings of the work, the contribution of the research to the field, and the limitations of the results presented. With the breadth of the subject area visited in this work, many areas have been left with opportunities for further work. These areas will be highlighted in the discussion as either promising areas for further research, or limitations of this work.

8.1 Understanding the Influence of Parasitic Elements in WBG Based Power Converters

8.1.1 Impact of Parasitics

It has been demonstrated that the impact of parasitic elements on the performance of wide band gap based converters is significant. A key finding was the sensitivity of the performance to what would be have previously been considered negligible parasitic elements. It was shown that to accurately understand the performance of a wide band gap based converter a detailed study of the parasitic elements is required, and in particular, 3D analysis of the PCB layout.

This work has explored the impact of parasitic elements in depth with particular focus on lay-

out elements such as the pad-to-pad capacitances. The layout elements considered were shown to contribute to loss, ringing, overshoot and EMI generation in the power converter. While some of the layout elements had little effect, a few were shown to have a large impact on the performance. In particular, the contribution of PCB C_{pp} was revealed to be a non-negligible contributor to the overshoot current which motivated techniques for controlling this overshoot.

8.1.2 Simulation

Using the results of the parasitic extraction process, a circuit simulation was created which allows investigation of the influence of a wide range of the parasitic components within the circuit. This simulation model matched the high speed characteristics (overshoot and ringing after switching) with enough accuracy to make predictions regarding the performance of the system when variations were made to the parasitic elements or mitigating strategies were implemented.

It was found that in order to achieve faithful observations in the simulation, it was necessary to model the parasitic elements of the probes and the impact that these have on the measured waveforms. Exploring these probe parasitics shows that they have a significant effect on the converter performance when it is operating at high speed. To mitigate this, the probing strategies discussed in section 3.1.4 were used to improve the accuracy of the measurements in all further experimental work.

The relative values of several of the key PCB parasitics were swept in the simulation model in order to determine their impact on the system. This illustrated the relative importance of each of these parasitic elements in determining the system performance. This highlighted the relative impact that some of the parameters have relative to others and focused the search for mitigating methods. Further work could be done in verifying these performance impacts experimentally to determine the impact on switching loss and EMI generation.

Chapter 3 showed that the capacitance between adjacent pads on the PCB (C_{pp}) was a significant contributor to the current overshoot and therefore switching loss. Though this was shown both analytically and through demonstrably accurate simulation, no experimental validation was performed. Such experiments simply require either multiple PCB designs exhibiting the various pad-to-pad distances or affixing additional capacitance to the existing setup. These were

not performed in this work as the experiments were deemed to be too time consuming, however, this validation may be essential to a full understanding of the effect.

The simulation model was limited in accuracy due to several factors. The extraction of the device parasitics using the impedance analyser in section 3.1 was done without a voltage bias in the measurements. As the converter will operates at 600 V the actual parasitics may deviate from those measured. Extracting the parasitics using a biasing rig for the impedance analyser would provide more accurate results. The extraction of the PCB parasitics in section 3.1.2 was limited in accuracy as it required the use of an optimisation algorithm. Running this algorithm for longer, or use of a multi-port impedance analyser would increase the accuracy of the results. Alternatively, 3D parameter extraction as discussed in section 2.2.5 would require less equipment than physical extraction.

8.1.3 Mitigation

A technique for mitigating the influence of the output cable and load capacitance was proposed in which a small, carefully designed inductor was introduced in series with the output. A design process for specifying the maximum allowable Equivalent Parallel Capacitance (EPC) of this component was detailed. Using this process, a suitable inductor was designed and shown to reduce the switching loss at turn-on by up to 35 %.

Though the use of the small inductor was shown to provide significant performance enhancement, the work presented has not explored in full the effect of the inductor reset during device turn-off and also has not investigated possible issues with inductor saturation at higher levels of current. Much of this could be investigated through further work with analytical models of the system, or through further experimental testing.

8.2 Understanding and Modelling the EM Impact of Device Switching Transients

8.2.1 Analysis

Through considering the waveform shapes presented in existing work, a generalisation was created. Using these definitions combined with a method of successive differentiation, a method for analysing the temporal source of high frequency content was developed. This technique has been demonstrated using experimentally obtained waveforms. This technique has particular value in the analysis of noisy experimental data, as the noise will make other analysis techniques difficult to interpret.

This technique still has limitations. In particular, in the examples demonstrated the experimental data does not clearly fit into one of the symmetrical patterns chosen for comparison. This suggests that further work is required to identify the frequency domain impact of switching transients with non symmetrical transitions.

The attempts here at frequency domain analysis of time domain signals will always be limited by the uncertainty principle. As the duration of the transition is small the spectral smearing in the frequency domain will be a big problem. This limitation of this work impacts the reliability of the frequency domain analysis as discussed in section 1.1.5. Further work considering the shape of the switching transient should rely on testing performed in the continuous mode as opposed to DPTs as this will ensure high accuracy in the frequency domain.

8.2.2 EMI Metrics

This work reviews and compares several methods for the quantification of EMI. It is found that this is a difficult performance metric to create as performance is somewhat subjective. However, a suitable metric was determined, and this is shown to be useful in a range of converter conditions and is subsequently used throughout the work. The comparison of previously presented metrics is also a new contribution of this work.

The EMI metrics presented and investigated in this work have limitations that prevent their usefulness in all applications. As was discovered, each of them is susceptible to being dominated

by an unintended effect. The simplest example of this was the metric that was based on the filter breakpoint - this metric would be dominated by whatever the low frequency content of the signal is. Other metrics can equally be misleading if applied to spectra with sharp or otherwise unexpected features. In addition to these issues, the metrics still require some careful processing of the waveform data in order to produce comparable results. Further work could address the robustness of any of these techniques to widen the range of useful application for them.

A difficulty in the analysis of the EMI performance of a power converter is that it will inevitably require the use of some output filtering as discussed in section 1.1.6. This work has concerned itself with the spectra of the waveforms at the switching node of the converter, which occur prior to filtering. All standards relating to the EMI performance of a converter include the output filter in the measurements. This means that comparison with the regulations is challenging from the point of view of reducing the emissions at source. No standard for the design of an output filter exists and there is presently no common baseline which can be used for comparison. This has led to this work comparing the switching node spectra directly with the specifications, which is not an informative exercise. Further work developing or defining the designs of a filter to use as a baseline for measurement, and subsequently for creating a metric would be informative.

8.3 Defining Smoothed Switching Transitions and Practical Realisation

8.3.1 Smoothness Metrics

As for EMI, classification of the smoothness of a waveform is a difficult challenge. Chapter 5 explored the possibility of a metric for the smoothness of a shaped waveform and a variety of options were investigated. However, it was found that these are not at present robust to practical experimental factors. As a compromise this work used the closely related metric for EMI, 'bandpower' as an alternative. To continue to further the field of waveform shaping in power electronics, a metric for the smoothness which is suited to the context will be required and should be the subject of significant further investigation.

8.3.2 Analysis

This work has presented three attempts at developing a simple, analytical method for analysing the performance impact of waveform shaping on the overshoot and ringing of the current or voltage due to parasitic elements. The attempts sought to connect the smoothness of the excitation waveform with the reduction in the current/voltage overshoot/ringing. These attempts have shown that the current definition of smoothness is too loose to allow a simple model to be proposed, and relies on the case-by-case numerical analysis of individual waveforms. Though the attempts to make the models were all unsuccessful, they do show some trends, and illustrates the complexity of shaped waveforms.

The work investigating analytical models for the overshoot and ringing caused by the application of a a smoothed waveform to a simple network was stopped before a satisfactory conclusion was reached. Though a significant amount of work was performed and no suitable model was evident, there is still motivation for further work in this area. The attempt to simplify the model to a 3^{rd} order polynomial seems to show that the model diverged too fast - though this was only considering a single branch of the model in isolation, and it may have been possible that the error could be balanced between the legs. It is suggested that there is still significant scope and opportunity in this area.

8.3.3 Simulation

Smoothed waveforms are proposed based on the extension of previous works. These are shown through basic analysis to be beneficial to the high performance of converters with parasitic elements. This analysis is validated by a simulation model of both the most basic interactions, as well as with more complicated interactions with the manufacturer's device models. The results suggest that the only limit to reducing the generation of EMI is the ability to achieve waveform profiling.

A limitation of these simulation modes is that they assume that one of the switching devices has been successfully profiled so as to produce the perfectly shaped voltage waveform. As shown in the experimental work, this assumption is poor, and as such a compromise must be met. These simulations are therefore illustrating a very limited and idealised case.

8.3.4 Practical Implementation

To validate the simulation results presented for the application of smoothed waveforms to networks of parasitics, experimental work was undertaken. As smoothed waveforms are typically defined by mathematical functions it is difficult to determine if they have been achieved in an experimental system. This work has presented practical targets for the shape of smoothed waveforms in a practical system.

Though practical targets for the waveform shape have been proposed, these targets were found to be highly subjective to the person viewing the waveform shape. During experimentation the adjustment to the excitation waveform was made based on the visual smoothness of the output waveform. Further work needs to identify a fast method of determining the smoothness of a waveform numerically so as to remove the subjective human element from the experimental work. The result of this subjectiveness was that the actively shaped experimental results tended to concentrate on long switching times which made losses very high. This is particularly apparent in the results of section 6.3 where all but one of the shaped waveforms had higher switching loss than the unshaped case. Development of the design and testing software could remove this subjectivity by showing the desired metrics in real-time, or by controlling the waveform design automatically.

A significant output of this work has been the development of tools for test rig automation and for the rapid development of shaped voltage waveform transients in DPTs. The tools that have been presented are Graphical User Interface (GUI) based, making their use fast and easy. These tools have enabled the work presented through this thesis, and contributed to other works.

Though the level of automation developed for the testing enabled the relatively fast development of waveform shapes, this still included the human in the loop, which, as discussed, introduced subjectiveness to the waveform profiles. This is a key limitation of this experimental testing as the result space is not fairly explored in all the directions that the parameters under control will allow. Further work in this area should remove the human from the loop.

It has been shown that through manipulation of the gate waveform voltage profile it is possible to shape the voltage and current waveforms of V_{DS} and I_D. Doing so has helped to reduce the voltage/current overshoots, and the EMI generation of the switching waveforms. In some

cases it has been possible to reduce the switching loss alongside these improvements, but the high sensitivity of the shapes to the noise at the gate means that a trade-off still exists even in the case of the fully active driver.

A severe limitation of the active gate driver that was developed in this work was the performance in the presence of high noise. Though the design was demonstrated to be able to perform at very high speeds, this was only so before it was subjected to the high noise environment of the power converter. Further work on shaping drivers should seek to integrate the driver onto the main test PCB to reduce the parasitics in the drive loop, create a more powerful output stage, and make the intermediary stages more noise tolerant. The impact of this on the work presented was to limit the switching speed that could be achieved with the active gate driver circuit and to limit the fidelity with which the gate of the switching device could be controlled. Only a voltage source based driver was considered, whereas in section 2.4.3.1 it was noted that current source based drivers will perform better at high switching speed. Further work should consider the implementation, focussing on how to accurately control the gate charge.

When analysing the performance of the active gate driving circuit, the waveforms that are looked at are the voltage waveforms measured on the pins of the switching device. Though these give an indication of the interaction between the switching device and the gate driver, they do not clearly represent the state of the gate within the silicon of the device. The parasitic inductance in the gate connection will hide the true voltage of the gate from the measurement point. The gate charge would give a better indication of the state of the device. This can be measured indirectly through integration of the current into the gate terminal and further work in which the gate current is accurately measured would elucidate the operation of the active driver. However, measurement of the gate current is a difficult challenge as the parasitics introduced must clearly be kept at a minimum while simultaneously the measurement must be robust to the noisy environment.

8.3.5 Changing Conditions

Through use of the fast waveform development tools and the hardware tests, a range of switching conditions have been investigated. This has allowed an optimised gate waveform profile to

be presented under each set of operating conditions. This has shown how the excitation must change with the changing load current if optimised switching is to be achieved.

In chapter 6 the excitations required to produce useful transition shapes were explored. It was found that the required excitation will vary with the conditions under which the power converter is operating - most notable of these conditions was the switching current. Still outstanding are the questions of how this excitation will vary with both voltage and temperature, and whether it is sensitive to the load conditions. If the operating conditions change the required excitation this will have implications on the switching loss and EMI. Further work investigating these sensitivities is essential for understanding how the excitation waveform needs to be controlled. In particular, in an inverter application, the current will be changing throughout the output cycle, so understanding the compromises in the gate drive design is essential.

In addition to understanding how the converter operating conditions will affect the required excitation waveform, it would also be beneficial to explore how the excitation needs to be modified for differing switching devices. This work has concentrated on only one SiC MOSFET, and thus only the waveforms required for this device have been presented. Investigating the use of other devices could show that the passive waveform shaping can provide performance enhancements to converters using other device technologies.

In this work, the search for the best excitation was empirical, with a human editing the excitation to maximise the performance visually. This approach is both very slow, and is liable to miss optimal solutions, as it follows only one search vector. However, this approach was taken as it is fast to get to initial results and implementation of an automated system would require development of safety cut off systems to prevent the algorithm destroying the MOSFET. To ensure that all of the optimal solutions are found, and to remove bias from the system, the process of iterative waveform design should be automated using an algorithm. Presently the test system operates in a largely automated fashion, and the introduction of an automated waveform design process would not be a highly complex task. This would enable faster testing of more waveforms, and would also enable multi-objective optimisation.

8.4 Development of Passive Gate Drivers for Waveform Shaping

8.4.1 Design

Having identified waveform smoothing as an effective way of realising improved performance with a fully active gate driver, techniques for simplifying this are investigated. A key finding of this work is that it is possible to create a predominately passive circuit to be fitted to an existing gate driver which can achieve some of the shaping targets discussed.

A significant and simple opportunity for further work would be in using the same techniques used here to determine a passive network for shaping of the turn-off transient. This could share elements of the network that has been proposed for the turn-on transient.

8.4.2 Simulation

Simulation of the passive gate driver design showed promise in shaping the gate voltage waveform into the desired profile. Each of the variable components was determined to have the desired effect on the waveform profile. Though each of these values was swept to explore its influence, there are two key elements that were kept constant - the capacitances. Additional work to determine the utility of varying these should be undertaken so as to inform the optimal choice of these component values. Additionally, the simulation model only considered the case where the switching device was modelled by a capacitative load. To assist with modelling the ideal operating point before performing experiments, the full converter model developed in chapter 3 could be utilised. This would first require optimisation to reduce the simulation run time. The model takes around 6 hours for each switching iteration, making searching for an optimum point slow. Reducing the required simulation time to <1 hour would enable this to be used for optimum point searching.

Further work could also focus on producing a full analytical model for the passive gate driver. This would greatly speed up the process of selecting the optimum component values by helping to determine the useful range of values to be investigated. The range of values to investigate was determined empirically in this work. As the response of a MOSFET was shown in chapter 6 to be very sensitive to the excitation waveform, the accuracy of modelling the MOSFET transient in

response to the gate excitation was a concern. Due to this concern, experimental implementation has been favoured as this eliminates the uncertainty of modelling inaccuracy.

8.4.3 Experimental Validation

The passive shaping driver has been demonstrated as a prototype under a limited range of conditions to be able to influence some aspects of the power converters performance. In particular the driver demonstrated an interesting control of the trade-off between switching speed and EMI generation capability.

Redevelopment of the passive gate driver to implement it on a PCB was successful in increasing the confidence in the results as well as the repeatability of the experiment. However, it was found that the implementation still introduced large parasitic values which required the results for the fixed resistance based gate driver to be repeated. To fully realise the potential of this style of driver this issue will have to be overcome by removing the reliance on the trimmer potentiometers.

Testing the driver under multiple levels of device current showed how the performance result space shifted. This is useful as the achievable performance under each condition can be determined. A shortcoming of this however, is that is is not clear how a single setting of the driver resistances maps from one of the result spaces to the next. As a practical realisation of this driver would rely on the resistances remaining fixed it is important to understand how a single setting maps under changing conditions. This should be the subject of significant further investigation.

An additional condition that has not yet been considered, is how the passive gate driver performs during the turn-off transient. As the present driver has been designed with a complete disregard to its influence on this transition no observations have been made of the transient. This is a significant shortcoming, as clearly a practical driver must balance the needs of the turn-on and turn-off transitions so as to reach optimal performance. Further work should investigate either the performance of the proposed driver, or a modified driver, during the turn-off transient.

The passive waveform shaping gate driver presented has been tested under only a very limited range of switching conditions, limiting the understanding of how such a system would

perform with varying conditions. Further work should investigate how such a driver performs with different load, supply, and switching conditions to determine the arrangement of resistances that should be used in each case, and identify possible resistance settings that provide a compromise between complexity and performance.

APPENDIX A

APPENDIX A - DOUBLE PULSE TESTING

Double pulse testing is a method for testing the switching characteristics of a switching device without running the device under full load. The voltage and current levels that are experienced in actual operation are achieved, but only transiently. This method is used as the power supply, load, and heatsink only need to be able to operate at the full power level transiently.

The typical shape of the switching device current waveform during a DPT is illustrated in fig. A.1. The device is switched on with a long pulse (t_1) to establish the desired current level in the circuit. The device is then turned off for t_2 and on again for t_3. The lengths of the pulses t_2 and t_3 are chosen to imitate the periods that would be observed in actual operation. To observe the turn on transient the transition between t_2 and t_3 is observed - here the device will be under the same operating conditions as in actual operation.

For the work presented in this thesis, the current level of the waveform is taken as the level that the device turns on at after the transition between t_2 and t_3. This is marked as A in fig. A.1.

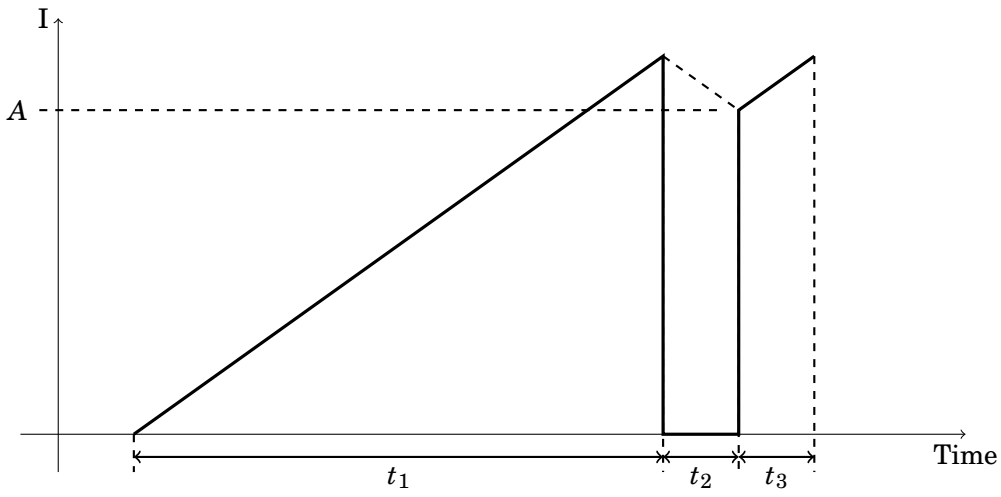

Figure A.1: Switching device current waveform during a double pulse test

A.1 Zero Current Switching

A special case of double pulse testing is used extensively in this work for the investigation of parasitic elements. This technique is zero current switching, and has been used to describe the special case where t_1 is 0 s. This results in no current having been established in the switching loop at the observed turn-on transient.

The typical load that the switching device will experience will be similar to that which is illustrated in fig. A.2. The rise of the current level in the inductor will typically take a number of μs. If the turn-on transient it observed in the ns scale then no inductor current will be observed as this can be treated as high impedance at this timescale. Any current observed in this timescale will be due to other factors. The capacitance in parallel with the load in fig. A.2 will cause a spike of current which will be visible in the ns scale. Hence we can use zero current switching to observe the impact of fast elements without observing them superimposed onto the inductor current.

In addition to the benefit of not observing the current spike superimposed upon the inductor current, there is an additional benefit of zero current switching. It is well established that the RRC provided to the diode of the co-device will be dependant on the current in the switching loop at diode turn-off. Using zero current switching the loop current is zero, and hence there will be no RRC. This makes the influence of other elements even clearer.

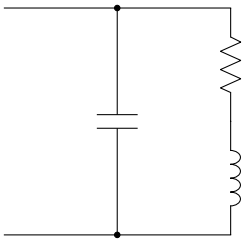

Figure A.2: Typical load connected to the switching device

APPENDIX B

APPENDIX B - CODE LISTINGS

This appendix lists the code for functions that were critical to this work.

B.1 Matlab DFT code

```
function [x_frequency,y_amplitude] = samfft(x_time, y_amplitude, varargin
    )
%SAMFFT Takes a time domian waveform and its time axis and produces the
%frequency domian vectors
%
%   Sam Walder - University of Bristol - 2013 - sam.walder@bristol.ac.uk
%   Apollo Charalambous - University of Bristol - 2015 - apollo.
    charalambous@bristol.ac.uk
%
%   * NOTE: You may wish to redefine how custom_step is defined as this
%           will controll the maximum frequency that is used in the case
    that
%           intopolation occores
%
%
    ========================================================================

%   Input arguments:
%       * x_time        - The time domain time axis
%       * y_amplitude   - The amplitude vector associated with X
```

```
%       * remove_zeros  - Set to 1 to remove zero values from the results
    .
%                         This helps with producing loglog plots as zeros
     cause errors
%                         Default is not to (0)
%       * window        - Window to use.
%                         Acceptable values are: 'flattop' 'hamming'
%                         'hann' 'blackman' 'none'
%                         Default is none, this argument does not need to
%                         be specified.
%       * correction    - Correction factor to use with the window.
%                         You can either correct for the amplitude or the
%                         energy.
%                         Valid entris are: 'none' 'amplitude' 'energy'
%    Output arguments
%       * x_frequency   - Frequency axis
%       * y_amplitude   - Amplitude axit to go with x_frequency
%       Dependencies
%               * num2eng       - Converts anumber into text with SI
    multiplier
%                         Can replace with num2str
%
    ========================================================================

%   CHANGE LOG:
%       * 2013 - Created
%       * 2015 - Apollo Charalambous - apollo.charalambous@bristol.ac.uk
%           Added the x2 multiplication
%       * 2015 - Sam Walder
%           Added remove zeros option
%           Fixed a bug in the remove zeros function
%       * 2015/11 - Sam Walder
%           Added the interpolation and windowing
%       * 2016/01 - Sam Walder
%           Fixed an error with line 187 (strcomp -> strcmp)
%       * 2016/02 - Sam Walder
%           Fixed bug causing interpolation to run unneceseraly
%       * 2016/06 - Sam Walder
%           Added input orientation auto corrention
%       * 2016/07 - Sam Walder
%           Fixed an issue in the maths whereby it would work out the
    wrong
%           frequency axis (used L instead of n)
%
    ========================================================================

%   EXAMPLES:
```

```
%       * Just do the DFT
%           [frequency, amplitudes] = samfft(time, amplitudes)
%       * Do the DFT and remove zeros
%           [frequency, amplitudes] = samfft(time, amplitudes, 1)
%       * Do the DFT with a window
%           [frequency, amplitudes] = samfft(time, amplitudes, 'hann')
%       * Do the DFT with a window and correct for amplitude
%           [frequency, amplitudes] = samfft(time, amplitudes, 'hann', '
    amplitude')
%       * Do the DFT removing zeros and apppling a window
%           [frequency, amplitudes] = samfft(time, amplitudes, 1, 'hann')
%       * Do the DFT removing zeros and apppling a window and correcting
%         for energy
%           [frequency, amplitudes] = samfft(time, amplitudes, 1, 'hann',
     'energy')
%
    ========================================================================


%% Decide what to do with the inputs
if nargin == 2
    % Only 2 inputs specified, assume defaults for others
    remove_zeros = 0;
    window = 'none';
    correction = 'none';

elseif nargin == 3
    % They have specified something else. Is it a string or a number?
    % If it is a string it must be the window
    % If it is an int then it must be zeros removal
    if ischar(varargin{1})
        % The 3rd input is a char array, they want a window
        window = varargin{1};
        remove_zeros = 0;
    else
        % The 3rd input must indicate if they want zeros removed
        if varargin{1} == 1
            remove_zeros = 1;
        elseif varargin{1} == 0
            remove_zeros = 0;
        else
            error('Invalid final argument, I accept 0, 1 or nothing');
        end; % if
    end; % if

    correction = 'none';
```

```
elseif nargin == 4
    % There are 2 unknown things specified. These could either be zeros
        and
    % a window OR window and correction.
    % If the first input is string then it is the latter

    if ischar(varargin{1})
        % The 3rd input is a character array.
        % They have specified a window and a correction
        window = varargin{1};
        correction = varargin{2};
        remove_zeros = 0;   % Default
    else
        % They must have specified the zeros and a window
        remove_zeros = varargin{1};
        window = varargin{2};
        correction = 'none';
    end; % if

elseif nargin == 5
    % Wow! they specified everything? Easy!
    remove_zeros = varargin{1};
    window = varargin{2};
    correction = varargin{3};

else
    % Cause an error
    error('Invalid number of arguments');
end; % if

%% Make sure the inputs are row vectors
sizeX = size(x_time);
if sizeX(1)>sizeX(2)
    x_time = x_time';
end; % if

sizeY = size(y_amplitude);
if sizeY(1)>sizeY(2)
    y_amplitude = y_amplitude';
end; % if


%% If the timbase is not uniform we need to do some intopolation of the
    data
% To check we need to see if the diff() of the timebase is a constant
    value
diff_time = diff(x_time);
```

```
accuracy = 1e-14;       % This gets us round the precision limits
if (all( (diff_time > (diff_time(1)-accuracy)) ) && all( (diff_time < (
    diff_time(1)+accuracy)) ))
    % They are all equal, this is good as we don't need to do anything
else
    % They are not all equal. This presents issues.
    % First find the minimum time step - we will use this as the time
        step
    % for our evenly spaced data (and issue a warning to the user about
    % this)
    warning('x_time is not uniform in step size - samfft will interpolate
        the data onto the custom step size. High frequency information
        will have been partially extrapolated!');
    min_step = min(diff_time);
    max_step = max(diff_time);
    mode_step = mode(diff_time);
    custom_step = mode_step/2;
    disp(['Extrapolation region: ', num2eng(round(1/max_step)), 'Hz to ',
         num2eng(round(1/custom_step)), 'Hz']);

    % Create a new uniform timebase
    uniform_time = linspace(x_time(1), x_time(end), range(x_time)/(
        mode_step/2) );

    % Intopolate the data
    uniform_amp = interp1(x_time, y_amplitude, uniform_time);

    % Overwrite the existing varaibles (Possibly not that efficent)
    x_time = uniform_time;
    y_amplitude = uniform_amp;
end; % if

%% Apply windowing
% Possible windows are: flattop | hamming | hann | blackman | none
switch window
    case 'none'
        % No window... do nothing
        window_amp = 1;

    case 'flattop'
        % Define a flattop window
        window_amp = rot90(flattopwin(length(y_amplitude)));

    case 'hamming'
        % Define a Hamming window
        window_amp = rot90(hamming(length(y_amplitude)));
```

```
    case 'hann'
        % Define a Hanning window
        window_amp = rot90(hann(length(y_amplitude)));

    case 'blackman'
        % define a Blackman Harris window
        window_amp = rot90(blackman(length(y_amplitude)));

    otherwise
        % They have not define a valid window. Tell them this! Make sure
        % they know they are wrong!
        error('The window type requested is not valid');
end; % switch

% Figure out the correction scaling values
amp_corr = 1/(sum(window_amp)/length(window_amp));          % (Mean)
   Scaling factor for amplitude
en_corr = 1/sqrt(sum(window_amp.^2)/length(window_amp)); % (RMS) Scaling
    factor for energy

% Apply this to the data
y_amplitude = y_amplitude .* window_amp;

%% Correct the amplitude or the power depending upon user input
if strcmp(correction, 'none')
    % Do nothing
elseif strcmp(correction, 'amplitude')
    y_amplitude = y_amplitude * amp_corr;
elseif strcmp(correction, 'energy')
    y_amplitude = y_amplitude * en_corr;
else
    error('The correction term requested is not recognised');
end; % if

%% Do the maths
% Set up a few useful things
L = length(y_amplitude);          % Number of samples

% Get the lenght to be the next power of 2
n = 2^nextpow2(L);

% Create Y axis
Y = fft(y_amplitude, n);
P2 = abs(Y/n);
P1 = P2(1:n/2+1);
P1(2:end-1) = 2*P1(2:end-1);
y_amplitude = P1;
```

```
% Figure out the time step
step = (x_time(end) - x_time(1)) / (length(x_time));

% Create X Axis
%x_frequency = 0: ((1/step)/2)/((n/2)-1) :(1/step)/2;
Fs = 1/step;
x_frequency = Fs*(0:(n/2))/n;

%% Deal with zeros
% Clear zeros if applicable
if remove_zeros == 1
    x_frequency = x_frequency(y_amplitude~=0);
    y_amplitude = y_amplitude(y_amplitude~=0);
end; % if

end
```

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