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A p-channel GaN Heterostructure Tunnel FET with High ON/OFF Current Ratio

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Abstract—A novel mechanism to achieve a non-ambipolar Tunnel FET (TFET) is proposed in this work. The method relies on polarization charge induced in semiconductors, such as group III nitrides, to enhance the electric field across the junction and facilitate unidirectional tunneling based on the polarity of applied gate bias. This also enables enhanced control over the tunneling distance, reducing it significantly in comparison to a conventional tunnel FET. The proposed p-channel device implemented in a novel vertical GaN nanowire geometry facilitates a reduction of footprint while still maintaining a comparable performance to that of conventional E-mode p-channel devices in GaN. This opens up possibilities for E-mode p-channel GaN devices.

Index Terms—Band-to-band tunneling, tunnel field effect transistor, subthreshold swing (SS), wide band gap materials, III-nitrides, tunneling resistance, Heterojunction TFETs.

I. Introduction

Increasing attention is being divested currently in low resistance tunnel junctions in III-nitrides in order to improve the efficiency of visible and ultraviolet light-emitting diodes (LEDs) [1]–[3] by elimination of p-type contacts in GaN [4]–[6]. Forming a tunnel junction in GaN with a low tunnel resistance is challenging, in part due to the large band gap that increases the tunneling barrier height and electric field required to produce sharp band bending. An increased diffusion of Mg ions at high temperature [7] and a large activation energy of $174\ meV$ [8] also make it difficult to achieve degenerately doped p-type GaN, necessary to form a tunnel junction with abrupt band bending. Therefore, a thin layer of either AlN [9], [10], InGaN [11]–[13] or InN [14] is sandwiched between p- and n- type GaN regions to introduce additional polarization charge at each of its interfaces to raise the electric field between the p- and n- type regions, thereby facilitating tunneling. This type of tunnel junction which is aided by polarization charge is referred to as polarization-induced tunneling junction (PITJ) [10].

A PITJ with a thin InN in a novel n-channel tunnel FET (TFET) in GaN was predicted with an on-current of $60\ mA/mm$ in a simulated fin geometry and a SS of $\sim 20\ mV/dec$ with an ON/OFF current ratio ~ 5 orders of magnitude in a sidewall-gated cylindrical geometry, respectively [14]. In another TCAD based simulation study, an inline-gated rectangular TFET with InN based PITJ demonstrated an on-current of $73\ mA/mm$ with a SS of $15\ mV/dec$, and an ON/OFF ratio of 5 orders of magnitude [15], while the maximum bias was kept at $0.5\ V$.

Recent progress in p-type doping in excess of $10^{20} cm^{-3}$ facilitated by low temperature MBE growth has led to demonstration of a direct tunnel junction between degenerately doped p- and n-type GaN [6], [16]. This device achieved a differential resistivity of $1 \times 10^{-5} \Omega\ cm^2$ [16], an order of magnitude lower than the lowest reported resistivity in a PITJ using $In_{0.25}Ga_{0.75}N$ [13]. Based on this study the realisation of GaN based TFETs without PITJs, can also be envisioned. In this work however, we have analysed TFETs with embedded PITJ for facilitating transport, rather than as low resistance contacts.

Conventional TFETs suffer from poor on-current, because the tunneling mechanism introduces an additional resistance in the source-drain path relative to a MOSFET. To date, no one has yet demonstrated a TFET of comparable current level to a MOSFET with subthreshold slope (SS) below $60\ mV/dec$ [17]. The best reported electrical characteristics were achieved in a vertical nanowire InAs/GaAsSb/GaSb TFET, which showed an on-current of $0.31\ mA/mm$ at $60\ mV/dec$ of SS [18]. At a minimum SS of $48\ mV/dec$ the maximum current degraded to $67\ nA/\mu m$ in this device. Moreover, conventional TFETs suffer from ambipolarity which results in high off-current [19] and limits their applicability in complementary circuits [20]. To address ambipolarity, short-gated TFET [21], asymmetric doping, and band gap engineering [22], have been proposed.

In this work, a p-channel heterostructure tunnel FET (HTFET), utilising a thin layer of AlN as a PITJ, is introduced. Despite the larger band gap of AlN, which results in higher tunneling resistance in comparison to InGaN or InN, a thin layer of AlN is adopted [5]. Since the polarity of polarisation charge arising from InN or InGaN is opposite to that of AlN, employing either InN or InGaN in forming a PITJ can be accommodated by simply inverting the device geometry. However, a significant lattice mismatch between GaN and InN $> 10\%$ [23] results in strain that can introduce challenges to the growth of InN or InGaN on GaN. In comparison, a lattice mismatch $< 2.5\ \%$ between GaN and AlN [23] implies that up to $5\ nm$ of fully strained AlN can be grown on GaN without the introduction of microcracks [24].

This article is organised as follows: In section II, the model of the tunneling current and its calibration with reported experimental results from the literature are presented [10]. Sections III and IV are dedicated to explaining the non-ambipolar operation of the p-channel HTFET. Section V presents a unique behaviour of the tunneling region and tunnel distance in this device in contrast to that in the conventional

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TFETs. Finally, in section VI, key results of our analysis are summarised.

II. Model and Calibration

All results are obtained using Silvaco TCAD [25], where the inbuilt non-local band-to-band tunneling (BBT) model along with III-nitride specific field-dependent mobility model [26], [27], Shockley-Read-Hall, and Augur recombination are selected for the tunneling current and device electrical characteristics. Unlike the local tunneling models, where the tunneling rate at each point is calculated from the localised value of electric field, a non-local BBT model that includes a local variation of energy bands is employed in the interests of accuracy [27], while quantum confinement effects are neglected. W. Li et al. [15] have previously reported that a negligence of such quantum effects in TCAD models leads to an underestimation of the drain current compared to nonequilibrium Green's function (NEGF) simulations of their HTFET utilising an InN based PITJ.

TABLE I
Summary of Parameters Used in the Simulations

Parameter	Description	Value
m_e^{GaN}	Electron tunnel mass in GaN	0.20[a]
m_h^{GaN}	Hole tunnel mass in GaN	1.00[a]
m_e^{AlN}	Electron tunnel mass in AlN	0.31[a]
m_h^{AlN}	Hole tunnel mass in AlN	0.69[a]
$\varepsilon_{Al_2O_3}$	Permittivity of Al_2O_3 gate dielectric	9.3 [27]
σ_P	Polarisation charge density at AlN/GaN interface	$6.67 \times 10^{13}\ cm^{-2}$ [28]
μ_h	Maximum hole mobility in GaN	$16\ cm^2/Vs$ [29]
E_G^{GaN}	Band gap of GaN	$3.42\ eV$ [30]
E_G^{AlN}	Band gap of AlN	$6.28\ eV$ [30]
$E_{AD}(Si)$	Activation energy for donor dopant	$30\ meV$ [31]
E_{AA} (Mg)	Activation energy for acceptor Mg dopant	$174\ meV$ [29]
N_D	Density of donor (Si) doping	$3 \times 10^{19} cm^{-3}$
N_A	Density of acceptor (Mg) doping	$3 \times 10^{19} cm^{-3}$
E_{TAT}	Energy level of traps with respect to valence band in TAT simulation	$0.4\ eV$[b]
[a] Calibrated from the values reported in [32]		
[b] Consistent with Mg^+ and other cation traps in GaN [33]		

In all simulations, the maximum hole mobility is limited to $16\ cm^2/Vs$ [29], while an activation energy of $174\ meV$ is used for acceptor dopants, consistent with the reported activation energy of Mg in GaN. Unless stated otherwise, the doping density in all n- and p- type regions is kept at $3 \times 10^{19}\ cm^{-3}$. A list of all the important material parameters employed in the simulations are provided in Table I.

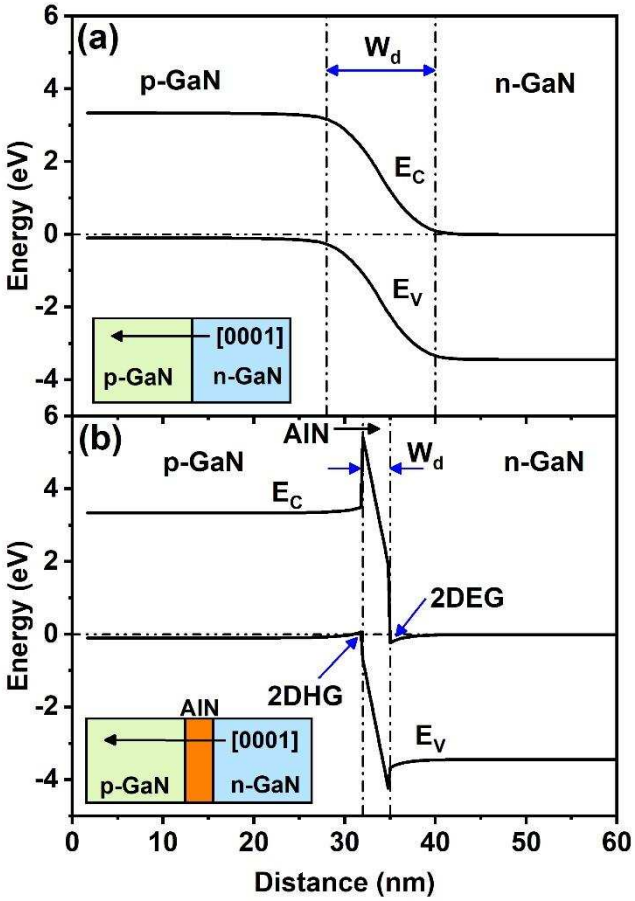

Fig. 1. Simulated energy band diagram of (a) a vertical p-n junction in GaN (inset) and (b) p-n junction with AlN barrier (inset), where the doping density in each n- or p- type region is $3 \times 10^{19} cm^{-3}$. The polarization charge at the AlN/GaN interface helps reduce the depletion width to facilitate tunneling.

In conventional tunneling devices, such as Zener diodes in Si, degenerately doped regions located adjacently, achieve high band bending that facilitates carrier tunneling through the energy band gap. Fig. 1 (a) and the inset therein show the simulated energy band diagrams for a degenerately doped ($N_A = N_D = 3 \times 10^{19}\ cm^{-3}$) p-n junction in GaN. The depletion width at the junction in this case is more than $10\ nm$, which greatly suppresses band to band tunneling of carriers on either side. To overcome this, a thin layer of AlN is sandwiched between p- and n- type regions (inset Fig. 1 (b)), which introduces polarization charge at each of its interfaces with GaN. This results in a high electric field across AlN ($\sim 12\ MV/cm$ [10]), thereby providing a sharp band bending to enable band-to-band tunneling, as observed in Fig. 1 (b). This mechanism has been utilized to implement tunnel diodes and light emitting diodes [9]–[11].

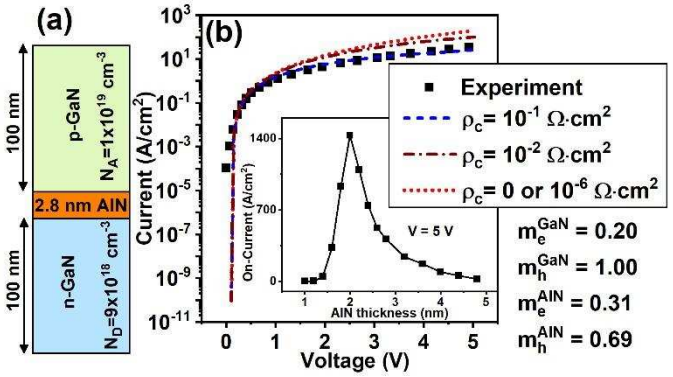

Fig. 2. (a) Schematic of a $56 \times 56\ \mu m^2$ GaN Zener diode with a 2.8 nm AlN barrier layer sandwiched between p-GaN and n-GaN, (b) Comparison of our simulation model with the reported experiment data reported from [10] (Adapted from Fig. 3 (a) with permission from [10] Copyright (2009) by the American Physical Society). The inset shows the simulation results of on-current for different AlN thicknesses.

The tunneling rate via the non-local BBT model is benchmarked by adjusting the effective electron tunnel mass m_e and hole tunnel mass m_h, using reported I-V data for a $56 \times 56\ \mu m^2$ GaN tunnel diode, a two-terminal device, with a 2.8 nm AlN barrier and Ni/Au and Ti/Au ohmic contacts for p- and n- GaN, shown in Fig. 2 (a) from [10]. This device showed a total specific resistivity (including the tunnel resistance) of $\sim 0.14\ \Omega\ cm^2$. Effective masses $m_e = 0.2$ and $m_h = 1.0$ for GaN and $m_e = 0.31$ and $m_h = 0.69$ for AlN [23], [32], produce simulated I-V results that closely follow experimental characteristics, as shown in Fig. 2 (b), plotted for different contact resistivity values of the p-GaN contact. A good match between the model and experimental results is achieved with a contact resistivity anywhere between $10^{-2} - 10^{-1}\Omega\ cm^2$, which agrees with contact resistivities in the range of $10^{-4} - 10^{-1}\Omega\ cm^2$ for Ni/Au [34], [35]. Since better contacts to p-GaN, with ρ_c as low as $10^{-6}\Omega \cdot cm^2$ have been realised with a proper choice of metal stack [36], we optimistically employ $10^{-6}\ \Omega\ cm^2$ as the contact resistivity in all the simulations of a three-terminal p-channel HTFET. With this value of contact resistivity, the behaviour of the on-current (current at 5 V of applied bias) at different thicknesses of AlN is plotted in the inset in Fig. 2 (b). As seen, the device current remains close to zero for AlN thickness less than 1.5 nm or greater than 4.5 nm. This is because a thin AlN layer fails to provide sufficient band bending required for the BBT, while a thicker AlN increases the length of the tunnel barrier, resulting in exponential degradation of the tunnelling current. The on-current of the device peaks around 2 nm of AlN thickness, resulting in a minimum total specific resistivity of $3.5 \times 10^{-3}\Omega\ cm^2$.

III. Non-ambipolar Operation Of P-Channel GaN HTFET

Fig. 3 (a) shows a schematic diagram of the p-channel GaN HTFET with its vertical direction along [0001]. From the bottom to the top, the structure consists of a 56 nm n-GaN source, 2 nm AlN tunneling barrier, 15 nm undoped GaN (u-GaN) channel and 27 nm p-GaN. The energy of carriers in the u-GaN channel is modulated by a 2 nm Al_2O_3 separated gate, either in rectangular geometry with double gate or cylindrical geometry with a gate-all-around architecture. Unless stated otherwise, the width of the device in either rectangular or cylindrical geometry is kept at 10 nm, in-line with the minimum reported GaN nanowire widths of 14 nm or 10 nm reported via experiment in [37], [38]. As shown in the corresponding band diagram in Fig. 3 (b), the u-GaN acts as channel and maintains the valence band sufficiently lower than both the hole quasi fermi level ($h^+\ QFL$) as well as the conduction band in the n-GaN, thus preventing the tunneling of carriers when the gate bias is zero.

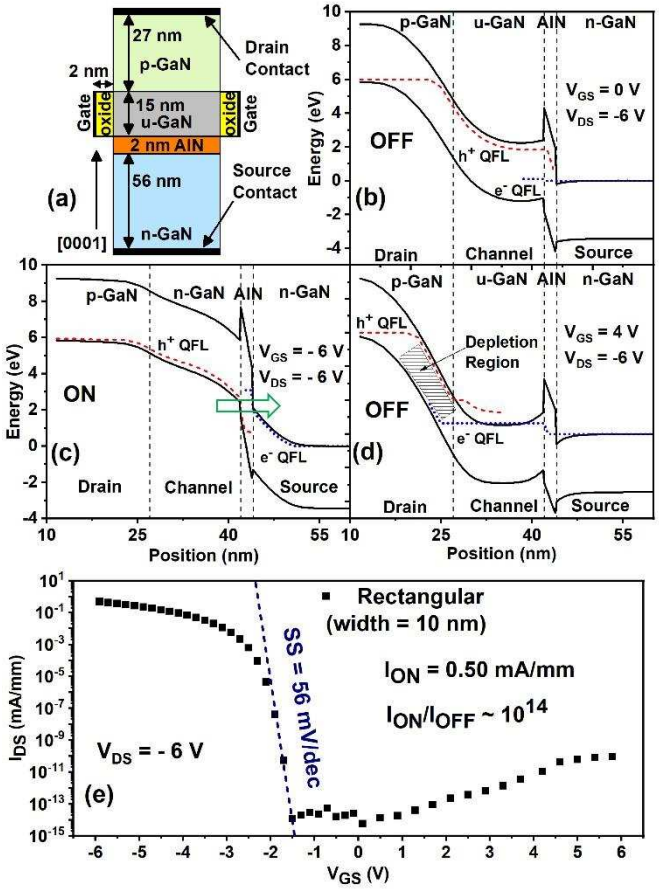

Fig. 3. (a) Schematic diagram of a p-channel GaN heterojunction tunnel FET (HTFET), and its simulated band diagrams along [000$\bar{1}$] (b) at zero gate bias (OFF state), (c) negative gate bias (ON state) and (d) positive gate bias (OFF state), and (e) transfer characteristics showing non-ambipolar behaviour, similar to a p-channel MOSFET.

A negative gate bias, raises the energy of the bands in the channel, moving the valence band closer to the hole quasi fermi level ($h^+\ QFL$), as shown in Fig. 3 (c), which leads to an increase in hole concentration. At sufficiently large negative gate bias, the valence band in the channel aligns with the conduction band of n-GaN, hence enabling tunneling across the AlN barrier, as indicated by the arrow in Fig. 3 (c) and turning the device on. On the other hand, a positive gate bias reduces the energy levels of the conduction and valence bands in the u-

GaN channel, as shown in Fig. 3 (d). However, since no AlN layer is present at the interface between p-GaN and u-GaN, the band bending between p-GaN and u-GaN occurs over a large distance, which greatly suppresses the tunneling current to maintain the device in the off-state.

The drain to source current I_{DS} with respect to V_{GS} for a rectangular or fin geometry is plotted in Fig. 3 (e) for a device or channel width of 10 nm. In contrast to the n-channel GaN HTFET reported in [14] where the channel is also doped, utilisation of u-GaN as a channel layer reduces the leakage by 10 orders of magnitude. However, the bias requirement of this device also increases to raise the energy of the valence band for alignment with the conduction band across the AlN layer. A lightly doped channel could also be employed to reduce the operating bias of this device. As can be observed, the drain current remains orders of magnitude lower at positive gate bias than at negative gate bias, thus confirming non-ambipolar behaviour, as indicated by the band diagrams (Fig. 3 (d)). Owing to the wide band gap nature of GaN, the off-current of the device remains much lower at $|10^{-14}|\ mA/mm$ even for a small channel length of 15 nm. A large band gap of AlN however, also introduces a large tunneling barrier height, which makes it difficult for the charge carriers to tunnel across the AlN. Hence the maximum drain current or on-current remains limited to 0.5 mA/mm in a fin geometry.

IV. Optimised Cylindrical P-Channel GaN HTFET

The most common technique to improve the on-current in TFETs is to introduce a highly doped pocket of opposite polarity in the vicinity of the source edge of the channel to enhance the electric field across the tunneling junction [39], [40]. Moreover, a better electrostatic gate control is expected in cylindrical or nanowire geometry. Hence, in this section, we analyse the electrical characteristics of an optimised cylindrical GaN HTFET, which utilises a thin ($\sim$2 nm) and highly doped ($N_A = 3 \times 10^{19} cm^{-3}$) pocket at the interface between channel and an AlN barrier of 1.7 nm thickness of GaN HTFET, as shown in Fig. 4, while the rest of the dimensions are kept the same as that for the device in Fig. 3 (a).

The electrical characteristics of the p-channel GaN HTFET are presented in Figs. 4 (a) and 4 (b), respectively. The current is normalised to the diameter of the cylindrical geometry. Owing to the thin p-GaN pocket, the maximum drain on-current $|I_{ON}|$ in Fig. 4 (a) is more than double in comparison to a rectangular device without the pocket (Fig. 3 (e)). An improved gate control in the cylindrical geometry also leads to a much steeper subthreshold slope (SS) of 32 mV/dec, in the absence of defect or trap states. In the absence of the thin AlN layer at the top edge of the gate, a positive gate bias alone is insufficient to produce a large band bending at this interface, hence the device continues to remain non-ambipolar. In Fig. 4 (b), it can be noted that a higher $|V_{DS}|$ is required to turn-on the device as $|V_{GS}|$ is increased. This is because a high $|V_{GS}|$ not only raises the energy of the valence band in the channel but also increases the energy of the conduction band in n-GaN across the AlN barrier layer (Fig. 3 (c)), thus requiring a higher $|V_{DS}|$ to align the bands to turn the device on.

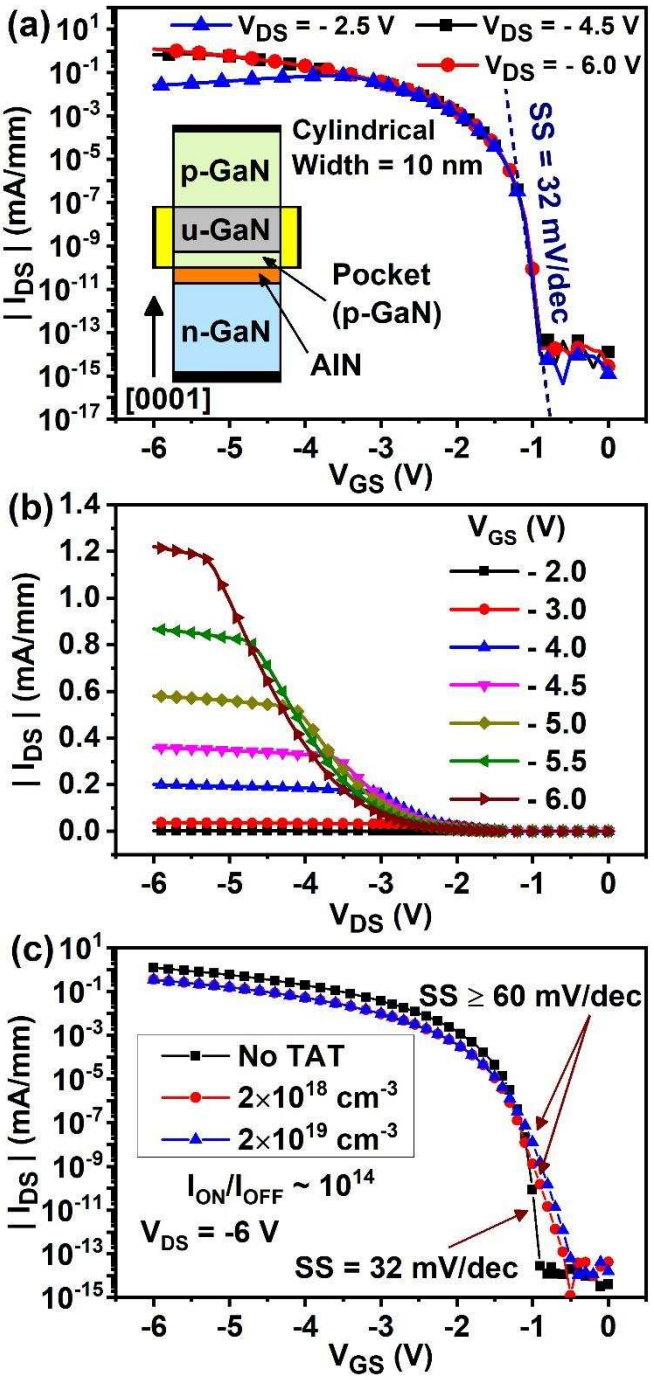

Fig. 4. Optimised (a) $I_{DS} - V_{GS}$ and (b) $I_{DS} - V_{DS}$ characteristics for the cylindrical p-channel GaN HTFET with a 2 nm pocket and 1.7 nm AlN barrier layer. (c) Impact of traps and trap-assisted tunneling (TAT) on transfer characteristics.

The impact of traps with densities $2 \times 10^{18}\ cm^{-3}$ and $2 \times 10^{19}\ cm^{-3}$ in AlN and resulting trap-assisted tunneling (TAT) is analysed in Fig. 4 (c). Owing to the higher recombination, the maximum drain current of the device degrades. Due to the increased leakage caused by TAT, the SS of the device no longer remains below 60 mV/dec. Even though the device turns on at a relatively smaller $|V_{GS}|$, it

maintains a large ON/OFF current ratio ($\sim 10^{14}$), which is due to the large barrier introduced by u-GaN (Fig. 3 (b)). This is to be expected, since the high density of traps is anticipated in the vicinity of PITJ and GaN channel is kept undoped.

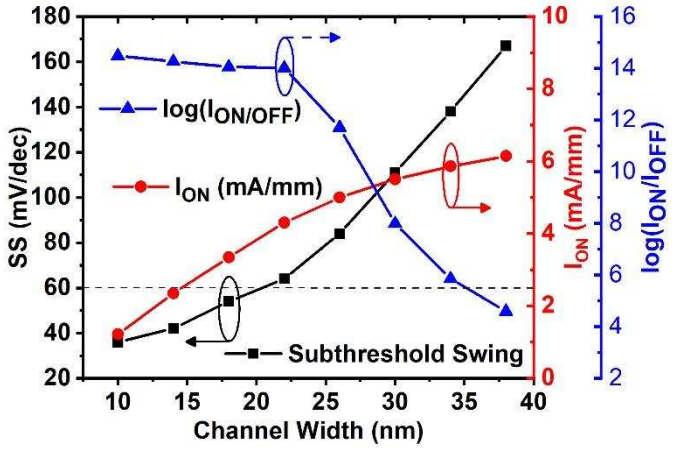

Fig. 5. Variations of I_{ON}, SS and $log(I_{ON}/I_{OFF})$ with respect to device width.

A further increase in $|I_{ON}|$ can be achieved by increasing the device width, W, as shown in Fig. 5. However, this increase comes at the cost of increase in SS and leakage current, which arises from an inability of the gate to maintain the same potential across a wider channel. For a channel width greater than $22\ nm$, the device begins to conduct even at zero gate bias, resulting in a reduction in I_{ON}/I_{OFF} and an increase in SS above $60\ mV/dec$.

Unlike MOSFETs, the presence of a tunneling mechanism in TFETs introduces an additional resistance R_{tunnel} due to tunneling, which appears in series with the channel resistance $R_{channel}$. The ON-state resistance of the device R_{ON}, can be calculated by dividing the maximum applied V_{DS} $(= -6\ V)$ with the corresponding I_{DS} at $V_{GS} = -6\ V$, i.e. $|6/I_{ON}|$. Fig. 6 (a) shows how the different regions in a p-channel HTFET contribute to R_{ON}. To determine the value of the tunnel resistance of an optimised cylindrical device (Fig. 4 (a)), R_{ON} is plotted as a function of gate to drain length L_{GD} and channel length L_G, in Figs. 6 (b) and 6 (c), respectively.

The contribution of the drain resistance R_{drain} to R_{ON} from the slope of R_{ON} vs. L_{GD} in Fig. 6 (b), yields an extracted R_{drain} for an L_{GD} of 27 nm, of $71.4\ \Omega\ mm$. Similarly the channel resistance $R_{channel}$ obtained from the slope of R_{ON} vs. L_G is $\sim 913\ \Omega\ mm$ at $L_G = 15\ nm$. Owing to a high electron mobility ($\sim 800\ cm^2/V \cdot s$) in comparison to the hole mobility ($\sim 16\ cm^2/V\ s$) in GaN, the contribution of the source resistance, R_{source}, is negligible in the present case. Therefore, R_{tunnel} is simply obtained as $R_{ON} - R_{drain} - R_{channel}$, which for an AlN barrier of $1.7\ nm$ results in $\sim 3.93\ k\Omega\ mm$, corresponding to a specific resistivity of $\sim 3.09 \times 10^{-4}\ \Omega\ cm^2$, for this cylindrical device, which is comparable to the best value for the tunnel resistivity of $1.2 \times 10^{-4}\ \Omega\ cm^2$ in a polarization induced tunnel diodes reported for GaN/InGaN/GaN hetero-tunnel junction [13]. This value of R_{tunnel} is an order of magnitude smaller than the minimum specific resistivity of $3.5 \times 10^{-4}\ \Omega\ cm^2$, obtained from a two-terminal PITJ based device in the inset of Fig. 2 (b). This reduction in specific resistivity is caused by primarily two factors: 1) enhancement in the electric field at the tunneling junction due to the lateral electrostatic control provided by gate and 2) A reduction in the optimum thickness of AlN, $1.7\ nm$ compared to $2\ nm$, in this geometry, which leads to an exponential increase in tunneling current.

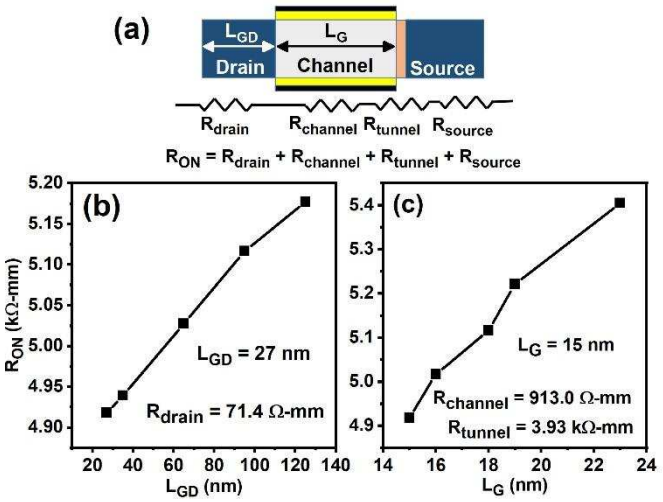

Fig. 6. (a) Contribution of different regions to the total on-resistance (RON) of the device. Variation of on-resistance with respect to (b) channel length and (c) gate to drain length, where the gate to source length and the device width are kept fixed at $56\ nm$ and $10\ nm$, respectively.

V. Analysis of Tunnel Distance

To contrast the operation of the PITJ HTFET, from a conventional TFET employing group IV semiconductor such as Si, in Figs. 7 (a) and (b), the band diagrams during the OFF and ON states are compared with a conventional double gated p-i-n TFET in Si. The figures indicate the tunnel distance, defined as the minimum horizontal distance between the valence and conductance bands. In Fig. 7 (a), with an increase of gate bias in a silicon TFET, the tunnel distance reduces from $6.1\ nm$ to $3.5\ nm$ as the device switches from OFF to ON. However as the tunnel distance gets smaller, the tunneling region also moves away from the gated channel region therefore resulting in a weaker gate control.

In the case of an HTFET in Fig. 7 (b), since tunnelling occurs only across the AlN barrier layer, the location of the tunneling region does not depend upon the value of gate bias. Therefore, a better control over the tunneling region is achieved resulting in a smaller tunnel distance than is possible in a conventional TFET.

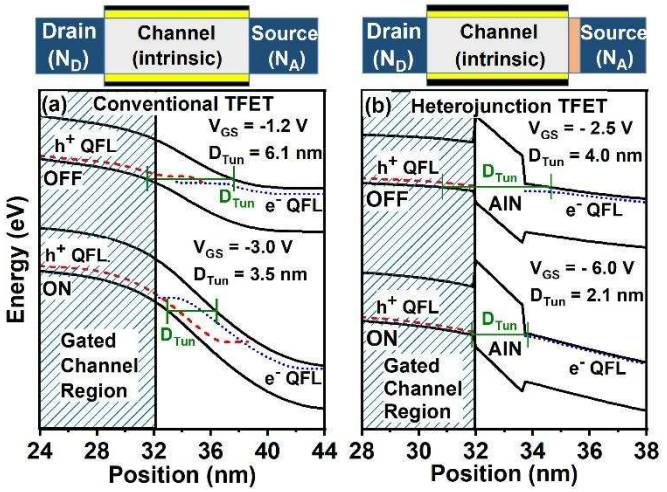

Fig. 7. Comparison of the band diagram in ON and OFF states of (a) a conventional TFET on Si and (b) a heterojunction TFET on GaN.

To further highlight the distinction in operation, the, transfer characteristics and tunneling distances of the two devices are compared in Fig. 8. Due to a large bandgap even though the maximum on-current is smaller, a wider band gap in GaN as well as a better control of the tunneling distance, limited only by the thickness of the tunnel barrier, lead to a higher ON/OFF current ratio and a steeper SS.

VI. Conclusion

In summary, an analysis of a p-channel heterostructure TFET in GaN reveals that owing to a polarization induced tunnel junction, transfer characteristics do not suffer from ambipolarity. Unlike contemporary p-channel MOSHFETs in GaN, the transfer characteristics show normally-off operation with a threshold voltage greater than $|-4|\,V$, along with a subthreshold swing of $36\,mV/dec$. Despite a low hole mobility and a tunneling mechanism, which raises the resistance of the source and drain path, the device is predicted to achieve a higher ON/OFF current ratio of $\sim 10^{14}$ at a much smaller footprint of $< 20\,nm \times 20\,nm$ as opposed to conventional p-channel MOSHFETs [41], while still maintaining a comparable drain-current of $\sim 1.2\,mA/mm$. An array of such devices could perhaps serve as a viable candidate to realise a p-channel device on GaN. In addition, since the region of tunneling is pinched to the location of the PITJ, a better electrostatic control over the tunneling region via the gate and reduction in the tunnel distance by a factor of 2 are shown in the present device compared to the conventional TFETs. Although the present mechanism is only explained utilising AlN to realise the polarization induced tunnel junction, further improvements in the on-current and reduction in the supply voltage are expected for the PITJ based on smaller band gap materials such as InGaN or InN instead of AlN.

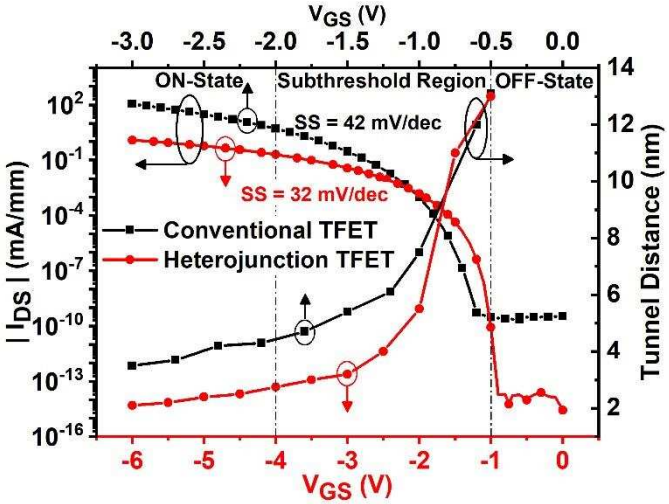

Fig. 8. Variation of the drain current and tunnel distance with respect to gate bias for a conventional TFET in Si and a heterojunction TFET in GaN.

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