Continuous Operation of Radial Multiterminal HVDC Systems Under DC Fault

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Rui Li, Lie Xu, *Senior Member, IEEE*, Derrick Holliday, Frederick Page, Stephen J. Finney, and Barry W. Williams

***Abstract* — For a large multi-terminal HVDC system, it is important that a DC fault on a single branch does not cause significant disturbance to the operation of the healthy parts of the DC network. Some DC circuit breakers (DCCBs), e.g. mechanical type, have low cost and power loss, but have been considered unsuitable for DC fault protection and isolation in a multi-terminal HVDC system due to their long opening time. This paper proposes the use of additional DC passive components and novel converter control combined with mechanical DCCBs to ensure that the healthy DC network can continue to operate without disruption during a DC fault on one DC branch. Two circuit structures, using an additional DC reactor, and a reactor and capacitor combination, connected to the DC-link node in a radial HVDC system are proposed to ensure over-current risk at the converters connected to the healthy network is minimized before the isolation of the faulty branch by mechanical DCCBs. Active control of DC fault current by dynamically regulating the DC components of the converter arm voltages is proposed to further reduce the fault arm current. Simulation of a radial three-terminal HVDC system demonstrates the effectiveness of the proposed method.**

***Index Terms*—Continuous operation, DC fault, HVDC transmission, modular multilevel converter (MMC).**

I. Introduction

Significant challenges to the development of multi-terminal HVDC transmission systems are protection during a DC fault and post-fault operation. In the event of a DC short circuit, high current flows through the freewheeling diodes in half-bridge (HB) modular multilevel converters (HB-MMCs), which are currently the preferred HVDC converter configuration, from the AC grid to the DC side. The low impedance of the short-circuit path leads to a steep rise in fault current which may cause serious damage to the converters or complete shutdown of the entire HVDC network [1-3].

Traditionally, AC or DC circuit breakers (switches) are required to disconnect the HB-MMC from the AC grid or DC fault point. Due to the slow operation of the ACCBs, the freewheeling diodes in the converters must be rated for full prospective short-circuit current during ACCB opening time, and the entire system will be shut down for a considerable time. The losses introduced by short-circuit currents expose the diodes to thermal stresses and are usually measured by the integral of the surge current I^2t. ABB, Infineon and Dynex provide IGBT and the anti-parallel diode with 3.3kV voltage rating and their diode I^2t are 911kA^{2}s, 730kA^{2}s and 720kA^{2}s respectively [4]. Bypass elements, typically thyristors, are used to protect the freewheeling diodes of the HB sub-modules (SMs) in MMC [5-9]. However, prolonged system outage still occurs.

In order to isolate the fault and protect the anti-parallel diodes in the faulty station, a handshaking approach is proposed in [10] to open the DC switches at both ends of the faulty branch. However, the DC switches on the healthy branches can potentially trip and the anti-parallel diodes have to withstand large fault currents due to the long opening time of DC switches.

By using the clamp circuit proposed in [11], the fault currents flow through the SM capacitors and are suppressed to zero by the capacitor voltages. As a result, the anti-parallel diodes do not suffer any over-current or thermal stresses. However, the use of clamp circuit results in additional power losses and capital costs.

DC circuit breakers (DCCBs) are usually categorized as mechanical, solid-state and hybrid DCCBs. The losses incurred in mechanical DCCBs are generally low and negligible compared to the power being transmitted. However conventional mechanical DCCBs are slower compared to other types and the converter semiconductors endure higher current stress during the response time [12, 13]. Interruption of remaining service can be avoided by connection of solid-state DCCBs at both ends of each cable and at converter station terminals, to give fast fault isolation [14]. However, this is at the expense of high capital cost and significant on-state operational power losses. Hybrid DCCBs have been proposed where a mechanical path serves as the main conduction path with minimal loss during normal operation, and a parallel connected solid-state breaker is used for DC fault isolation [15]. However, breaker footprint is relatively large and capital cost is high.

Based on active controlled power electronic components, DC transformers [5] can isolate DC faults rapidly and contribute to DC voltage and power flow control. Such added functionalities, however, are achieved at the expense of very high capital cost and power loss, and a larger footprint.

In addition to the previously described approaches to DC fault isolation, different MMC topologies, such as the full-

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bridge (FB) SM based MMC [16], the alternate-arm multilevel converter [17], the clamped double SM based MMC [18], the cross-connected SM based MMC [19], and the hybrid MMC [20, 21], have been proposed. Each can block DC faults immediately by blocking all of the switching devices. However, all of these approaches require additional semiconductor devices in the conduction path, resulting in higher power loss and capital cost than the equivalent HB-MMC. In addition, these configurations can only prevent over-current in the converters themselves, and cannot isolate the fault from the healthy network in the HVDC system. DC switches are still required to disconnect the faulted branch so that the healthy parts of the network can be restarted: all converter stations must be shut down prior to fault isolation by the DC switches [18]. Consequently, solid-state or hybrid DCCBs are still required to quickly isolate the fault and avoid the shutdown of the entire system.

DC-link capacitors in two-level voltage source converters (VSCs) can support the terminal voltages during a fault [22] though future systems are unlikely to use such configurations. Reactors can also be connected with fast acting DCCBs (e.g. solid-state or hybrid DCCBs) to limit the rate of rise of fault current and to decrease the fault current peak. However, all stations connected in the system are again blocked during the fault to avoid over-current, thereby causing the shutdown of the entire multi-terminal HVDC system.

The main contribution of this paper is on the use of additional DC passive components and novel converter control combined with low cost, low power loss mechanical DCCBs to ensure that the healthy DC network can continue to operate without disruption during a DC fault on one DC branch in a radial multi-terminal HVDC system. The paper is organized as follows. Consideration of DC fault-tolerant operation is presented in Section II. Fault current behavior is analyzed and a novel converter control strategy for limiting the MMC converter DC fault current is proposed in Section III. In Section IV, protection arrangements to isolate the DC fault and delay fault propagation to the healthy branches are introduced. DC fault-tolerant operation with the proposed protection structures and the novel active control of DC fault current is assessed in Section V, considering a pole-to-pole DC fault at the DC-link node in a three-terminal HVDC system. Section VI discusses the size of passive components in the protection structures and the extension to a meshed DC network. Finally, Section VII presents the conclusions of the study.

II. Consideration of DC Fault-Tolerant Operation

The aim of this study is to ensure continuous operation of the healthy parts of a radial multi-terminal HVDC system during a DC fault. Fig. 1 shows the three-terminal HVDC system considered. All converter stations are modeled as HB-MMCs using modified average models [7-9, 23]. The system parameters are listed in Table I. The SM capacitor energy per MVA is around 30kJ/MVA, which is in line with the value of 30-40kJ/MVA suggested by ABB in [24]. Station S_1 regulates the DC voltage of the DC network, with unity input power factor, while S_2 and S_3 inject rated active powers P_2 and P_3 into AC grids G_2 and G_3, also at unity power factors.

For symmetric monopole HVDC system considered in this study, a pole-to-ground DC fault exposes DC cables and converter transformers to DC stresses, but does not impose significant risk in terms of converter over-currents. Hence only pole-to-pole DC faults are considered.

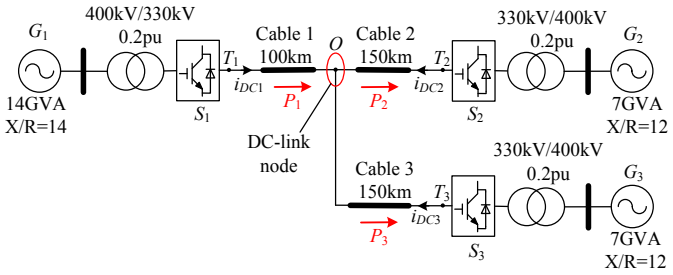


Fig. 1. Radial three-terminal HVDC transmission system.

TABLE I
Nominal Parameters of the Modeled Test System

Parameter	Nominal Value
DC-link voltage	±320kV
Power rating of stations S_1, S_2 and S_3	1200MW, 600MW, 600MW
Number of SMs per arm	304
SM capacitor voltage	2.105kV
Equivalent capacitance per arm of stations S_1, S_2 and S_3	30.5μF, 15.3μF, 15.3μF
Arm inductance	0.05pu
Number of DC cable pi sections	10
R, L and C of Cable 1	10mΩ/km, 1.5mH/km, 0.27μF/km
R, L and C of Cable 2	20mΩ/km, 1.3mH/km, 0.19μF/km
R, L and C of Cable 3	20mΩ/km, 1.3mH/km, 0.19μF/km

TABLE II
Time Interval between Fault Initiation and DC-link Voltage Falling below 0.8pu in the System of Fig.1 during a Pole-to-Pole DC Fault

Time Interval	Fault Location			
	T_1	T_2	T_3	O
t_{s1} (for Station S_1)	**0ms**	4.0ms	4.0ms	1.7ms
t_{s2} (for Station S_2)	4.4ms	**0ms**	4.8ms	2.3ms
t_{s3} (for Station S_3)	4.4ms	4.8ms	**0ms**	2.3ms
t_o (for DC-link node O)	2.1ms	2.5ms	2.5ms	**0ms**

The time intervals between fault initiation and DC-link voltage falling below 0.8pu are measured and listed in Table II. 0.8pu is chosen as the converters are likely to experience over-current once their DC voltages fall below this level. In order to eliminate the influence of converter active control on fault propagation, all of the stations are blocked immediately after the fault. Respective permanent pole-to-pole faults are applied at the terminals of the three stations and at the DC-link node. When the fault is applied, the voltage at the fault location drops to zero immediately and the corresponding fault time interval at the fault location is zero. As shown in Table II, a fault at the DC-link node propagates most quickly to the other terminals, taking only 1.7ms for the DC-link voltage of station S_1 to drop to 0.8pu. Hence, for the studied three-terminal HVDC system, a pole-to-pole DC fault at the DC-link node is the most serious challenge to continuous operation of the healthy parts of the network, and is therefore considered in this

paper.

To ensure continuous operating of the healthy DC network, a fault at the DC-link node must be isolated within 1.7ms for the studied system which is beyond the capability of any mechanical DCCBs and even hybrid DCCBs. Therefore, in order to achieve continuous operation of the healthy network without converter blocking, it is necessary that the fault propagation times are increased to match the operating speed of the used DCCBs, e.g. mechanical type. Additional passive elements are therefore first considered to delay the fault propagation.

To avoid converter blocking, the magnitude of the fault current flowing through the IGBTs must not exceed their current limit. Maximum fault current in the converter arms is therefore used to indicate whether or not a converter can ride-through the fault [25]. In this paper, maximum arm current is set at 2pu [10], and the mechanical DCCBs are modelled with 10ms opening time [26, 27].

III. Fault Current Analysis

In order to avoid converter blocking, the current in the converter arms must be within their safe operating limits. This section describes the characteristics of converter current (in particular, its DC component) during a DC fault.

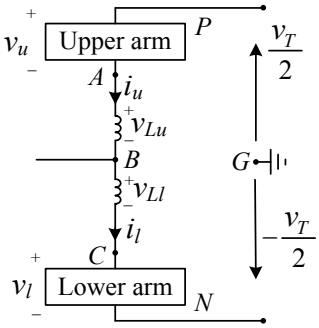


Fig. 2. Equivalent circuit for one converter phase during continuous operation without converter blocking.

A. Converter Fault Current during Continuous Operation

Once a DC fault occurs, the MMCs on the remote sides of the DC network continue operating. The generated upper and lower arm voltages are

$$v_u = (V_{DC}/2) - v_{ref} \tag{1}$$

$$v_l = (V_{DC}/2) + v_{ref} \tag{2}$$

where v_{ref} is the reference AC output voltage of the MMC, V_{DC} is the rated DC voltage, and u and l refer to the upper and lower arms.

Assuming the MMC terminal voltage drops to v_T ($v_T \leq V_{DC}$) after the DC fault, the voltages between A and G (v_{AG}), and C and G (v_{CG}), as shown in Fig. 2, can be expressed as

$$v_{AG} = (v_T/2) - v_u = v_{ref} - (V_{DC} - v_T)/2 \tag{3}$$

$$v_{CG} = -(v_T/2) + v_l = v_{ref} + (V_{DC} - v_T)/2. \tag{4}$$

As a result, the AC output voltage v_{BG}, and the upper and lower arm inductor voltages can be approximated as

$$v_{BG} = (v_{AG} + v_{CG})/2 = v_{ref} \tag{5}$$

$$v_{Lu} = v_{Ll} = (v_{AG} - v_{CG})/2 = -(V_{DC} - v_T)/2. \tag{6}$$

Equation (5) shows that the MMC can generate the required AC voltages in the short time after fault initiation, and thus, the AC current can still be controlled. However, during a pole-to-pole DC fault that results in significant reduction of the converter DC terminal voltage v_T, large DC voltages will be generated across the arm inductors if the MMC continues to generate the same DC voltage as it would under normal operation. Consequently, high DC fault current will be produced in the converter arms. Fig. 3 (a)-(c) show the simulated currents in the upper arm, and the DC and AC sides of an MMC during a remote DC fault, where the MMC continues operating without blocking. As the arm current is the sum of one third of the total DC current and half of the AC current, it can be observed from Fig. 3 that during the DC fault, the increase in the arm currents is mainly due to the increased DC components shown in Fig. 3 (b), while the AC components of the arm currents are still well regulated during the fault as shown in Fig. 3 (c).

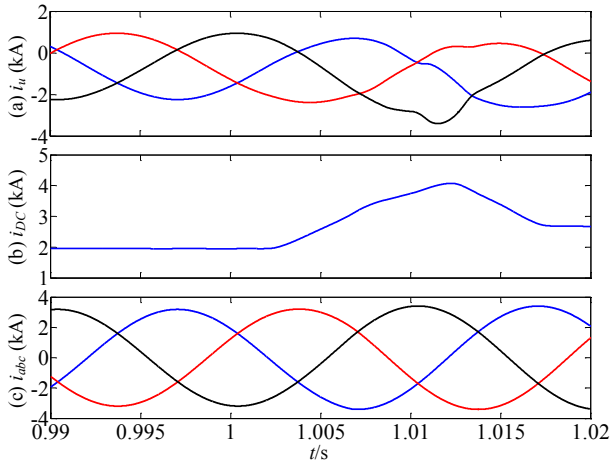


Fig. 3. Current waveforms during a pole-to-pole DC fault: (a) upper arm currents, (b) DC current, and (c) three-phase AC currents.

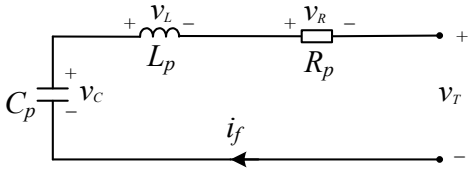


Fig. 4. SM capacitor discharging circuit.

B. DC Components in Arm Currents

To analyse the behavior of the DC component in the fault arm current during continuous operation, each phase of the MMC can be represented by the phase capacitor C_p in series with inductance L_p and resistance R_p, as shown in Fig. 4. Considering the total number of SMs per arm is N_{arm} and all the SM capacitors are discharged equally due to the capacitor voltage balancing control, the equivalent phase capacitor C_p, and L_p and R_p shown in Fig. 4 are expressed as

$$C_p = 2C_{SM}/N_{arm}, \qquad L_p = 2L_{arm}, \qquad R_p = 2R_{arm} \tag{7}$$

where C_{SM} is the capacitance in each SM, and L_{arm} and R_{arm} are the inductance and resistance of the arm reactor. The sum of SM capacitor voltages per arm is v_c and the DC offset of the produced arm voltage is $v_c/2$. Thus the total DC voltage seen across the upper and lower arms in each phase is v_c. It is assumed here that the initial value of v_c is the rated DC voltage V_{DC}.

According to the equivalent circuit shown in Fig. 4, the fault arm current flowing through the switching devices can be derived as

$$i_f(t) = \frac{V_{DC} - v_T}{2\omega_f L_{arm}} e^{-\frac{t}{\tau_1}} \sin(\omega_f t) \tag{8}$$

where $\tau_1 = \frac{2L_{arm}}{R_{arm}}$, $\omega_f = \sqrt{\omega_0^2 + \frac{1}{\tau_1^2}}$, and $\omega_0 = \frac{1}{2}\sqrt{\frac{N_{arm}}{L_{arm}C_{SM}}}$.

Assuming the SM capacitor voltages remain balanced during the fault, they can be expressed as

$$v_{SM}(t) = \frac{V_{DC} - v_T}{N_{arm}} \sqrt{1 + \frac{1}{\tau_1^2 \omega_f^2}} e^{-\frac{t}{\tau_1}} \sin(\omega_f t + \alpha) + \frac{v_T}{N_{arm}} \tag{9}$$

where $\alpha = \arctan(\tau_1 \omega_f)$.

It can be seen from (8) that, in order to reduce the fault current during continuous operation, terminal voltage v_T needs to be maintained as high as possible. Passive components are thus connected in the DC-link node to reduce the fault currents by maintaining the terminal voltage at a high value, as will be detailed in Section IV.

C. Active Control of DC Fault Current

Fault arm and DC-link currents can also be reduced by regulating the voltage v_c, i.e. the total DC voltage produced by the upper and lower arms in each phase. Therefore, in order to reduce the DC fault current, the DC components of the arm voltages need to be reduced accordingly during the fault. Based on this observation, active control of fault current is proposed where the DC components of the arm voltages are dynamically controlled during a fault to ensure maximum arm current is not exceeded.

As the HB SMs cannot generate negative voltage, the DC component of the arm voltage, v_{DC}, obtained from the proposed active fault current controller must meet the requirement defined in (10) to guarantee that the arm voltages are positive.

$$V_{DC} \geq v_{DC} \geq 2|v_{ref}|. \tag{10}$$

As the DC voltage produced by the MMC is now v_{DC}, according to (5) and (6) the AC output voltage v_{BG} and the voltages across the upper and lower arm inductors can be approximated as

$$v_{BG} = (v_{AG} + v_{CG})/2 = v_{ref} \tag{11}$$

$$v_{Lu} = v_{Ll} = (v_{AG} - v_{CG})/2 = -(v_{DC} - v_T)/2. \tag{12}$$

It can be seen from (12) that the proposed active control of fault current does not impact on the AC current control as the converter can still generate the required AC voltage. Comparing (12) to (6), the following equation can be derived

$$-(v_{DC} - v_T)/2 \geq -(V_{DC} - v_T)/2. \tag{13}$$

Equation (13) indicates that the voltages across the arm inductors can be reduced by the proposed active control, yielding smaller fault currents.

The block diagram of the proposed active fault current control scheme is shown in Fig. 5. As the MMC DC fault current increases due to a DC fault, the PID controller is effectively used to limit the DC fault current by regulating (reducing) the DC components of arm voltages. The DC components of the arm currents are obtained by subtracting half of the AC current i_{abc} from the arm current i_u. The resulting difference term i_f is used as feedback to the PID controller.

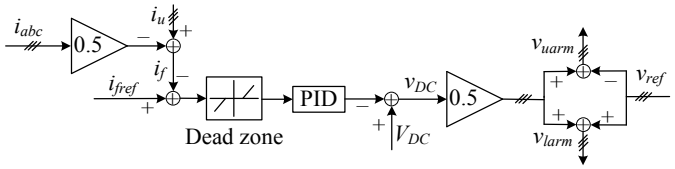


Fig. 5. Proposed active control of DC fault currents for MMCs.

During normal operation, the input of the PID controller is limited at zero by the 'dead zone' block such that the DC components of the arm voltages are at their rated values. If the fault current magnitude falls outside the predefined dead band, the PID controller output starts to increase from zero to dynamically regulate the DC components of the arm voltages to reduce the fault current. Note that the dead band needs to be properly set such that the active controller can be enabled quickly following a fault, whilst avoiding false triggering under normal operation.

IV. Protection Structures at the DC-Link Node

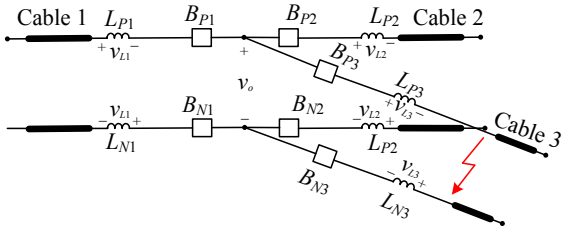
In the event of a DC cable fault, e.g. Cable 3 in Fig. 1, it is desirable that the converters connected to the healthy cables (i.e. S_1 and S_2) can continue operating without disruption. This requires that there is no over-current in converters S_1 and S_2 during the fault period until DCCBs are used to isolate faulty Cable 3 from the rest of the DC network. If slow mechanical DCCBs are used, it is necessary to slow fault propagation and to limit the current rise in S_1 and S_2, as previously described.

A. Protection Structure Configurations

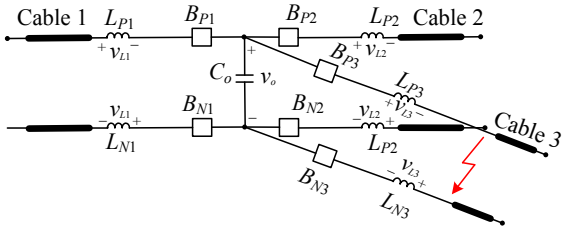
As shown in Fig. 6, mechanical DC circuit breakers B_{Pi}/B_{Ni} (i=1, 2 and 3) and DC inductors L_{Pi}/L_{Ni} are connected in series at the positive/negative DC-link node. The other ends of L_{Pi} and L_{Ni} are connected to station S_i through Cable i. Compared to the structure as shown in Fig. 6 (a), an additional DC capacitor is connected at the DC-link node to provide energy to support the DC-link voltage, as demonstrated in Fig. 6 (b). When the DC fault is applied at Cable 3, the corresponding DCCBs, B_{P3} and B_{N3}, are commanded to open once the fault is

detected, whereas the other mechanical DCCBs connecting the healthy branches remain closed in order to continuously transfer power. The selection of the correct DCCBs to open can be achieved by measuring the fault current directions at the DC-link node [22, 25, 28, 29].

The proposed active fault current control and protection structures do not depend on the detailed structure of DCCB. Apart from mechanical DCCBs, other types of DCCBs, e.g. the hybrid DCCB, can also be used in this study. If faster DCCB is used, the required additional DC inductance and capacitance in the protection structure can be reduced significantly (discussed in Section VI). Thus only the opening time of DCCB is critical to this study and is considered in this paper. This assumption has been used in [22], where the solid-state and hybrid DCCBs were both modelled as ideal switches and the difference is only on the opening times.



(a) Combined inductance L and mechanical DCCB



(b) Combined inductance L, capacitance C and mechanical DCCB

Fig. 6. Protection structures connected to the DC-link node.

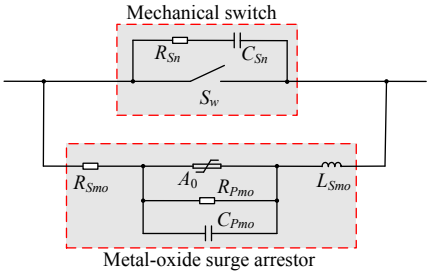


Fig. 7. Detailed model of mechanical DC circuit breaker where the metal-oxide surge arrestor is modeled as the physical model as presented in [30].

The DCCB in this study is modeled as a mechanical switch with an opening time of 10ms. A metal-oxide surge arrester is connected in parallel with each mechanical switch to absorb the energy in the DC line and to protect the DCCB against over-voltages. The detailed DCCB model in the MATLAB/Simulink® environment is shown in Fig. 7. The mechanical switch is represented by an ideal switch S_w in parallel with a series RC snubber circuit (resistor R_{Sn} and capacitor C_{Sn}). The switch S_w is controlled by a gate signal with a small on-state internal resistance while the off-state resistance is infinite. The metal-oxide surge arrestor is modeled as the physical model as presented in [30] where the non-liner resistance A_0 is paralleled with the leakage resistance R_{Pmo} and parasitic capacitance C_{Pmo} and then is connected in series with resistance R_{Smo} and inductance L_{Smo}. The DCCB model used in the paper should provide enough details for the type of studies carried out in the paper.

B. Influence of Protection Structures on Fault Currents

The simulated scenario assumes a permanent pole-to-pole DC fault at Cable 3 at time t=1s, as shown in Fig. 6. This is the most serious fault case for the continuous operation of stations S_1 and S_2. As previously described, the mechanical DCCBs isolate the fault 10ms after fault detection. Station S_3 is blocked due to over-current, while S_1 and S_2 remain operational. The diodes in S_3 are protected using bypass switches to avoid being damaged from high fault current and ACCB is used to isolate the converter from connected AC network [5-9].

Taking the structure shown in Fig. 6 (a), that combines inductances L with mechanical DCCBs, as an example to illustrate the influences of passive components on fault current, Fig. 8 shows the DC equivalent circuit of a healthy station where the DC-link node is represented by DC inductor L_o in series with resistor R_o. The DC cables are modelled as a pi section, whilst the converter station is simplified as the series connection of C_s, L_s and R_s where

$$C_s = 6C_{SM}/N_{arm}, \qquad L_s = 2L_{arm}/3, \qquad R_s = 2R_{arm}/3. \quad (14)$$

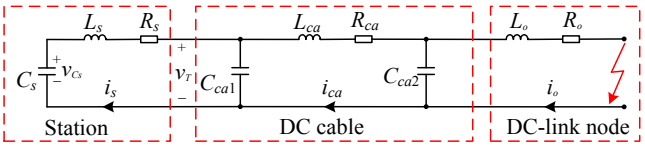


Fig. 8. Equivalent circuit of a healthy station for polo-to-pole DC fault applied at DC-link node.

Connecting DC inductors to the station terminals can increase the short-circuit impedance, yielding relatively low fault currents, especially for the station connected with the fault branch. However, it is not an effective approach for maintaining the terminal voltage of the healthy stations, as only the discharge of the equivalent converter station capacitance C_s is affected. In contrast, adding inductors at the DC-link node means that capacitors C_s, C_{ca1} and C_{ca2} are all discharged through the DC-link inductor, and therefore, it is more effective in maintaining the terminal voltage v_T of the healthy stations and reducing their fault currents.

Fig. 9 presents the peak fault arm currents and the minimum DC voltages (measured at T_1 as shown in Fig. 1) for station S_1 as the DC-link node inductance and DCCB opening time are varied. It can be seen that increasing the inductance and/or reducing the DCCB opening time reduce the peak value of the fault arm current and improve (increase) the minimum DC voltage for the healthy station.

For 10ms DCCB opening time, adding inductance of 500mH at the DC-link node reduces the peak fault arm current from 10kA to 3.5kA, and increases the minimum DC voltage from 280kV to 535kV. However, larger inductors incur

increased cost, weight, power loss, etc. Therefore, the tradeoff between performance and cost, etc. must be considered carefully when tuning the DC-link node inductances. If the mechanical DCCB is modeled with 5ms opening time as suggested in [26] and [27], the fault arm current peak is reduced significantly and the minimum DC voltage remains higher.

To simplify the analysis, all inductances at the DC-link node are set to the same value. In practical systems, the DC-link node inductances may have different values for the different cables that may be specified according to the rated power and current of the relevant converter stations, etc.

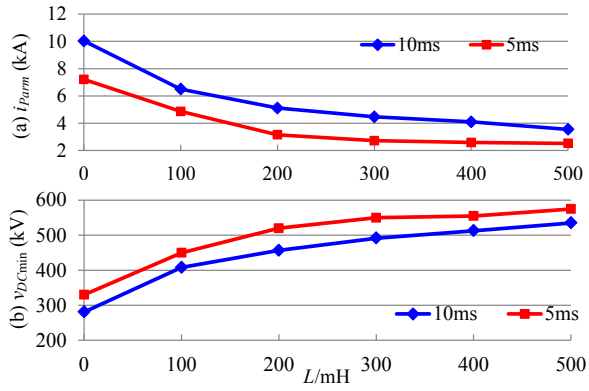


Fig. 9. Peak values of fault arm currents and minimum DC voltages with the variation of DC-link node inductance and different DCCB opening times: (a) peak fault arm current, and (b) minimum DC voltage.

C. Comparison of the Two Proposed Protection Structures

The difference between the two protection structures shown in Fig. 6 is on the capacitor connected at the DC-link node, which can provide additional energy to support the DC-link node voltage following a fault, so that station terminal voltage can be maintained and fault current magnitude reduced.

For the structure of Fig. 6 (a) that combines inductance L with a mechanical DCCB, application of a pole-to-pole DC fault at $t=t_0$ results in the immediate reduction of DC-link node voltage v_o from V_{DC} to $2V_{DC}/3$, whilst the rated DC voltage is shared between the DC inductors at the DC-link node immediately following the fault, as shown in (15) and (16).

$$v_o(t_{0-}) = V_{DC}, \quad v_o(t_{0+}) = 2V_{DC}/3 \tag{15}$$

$$v_{L1}(t_{0+}) + v_{L3}(t_{0+}) = v_{L3}(t_{0+}) - v_{L2}(t_{0+}) = V_{DC}/2. \tag{16}$$

The voltages across L_{P1}, L_{N1}, L_{P2} and L_{N2} increase from 0 to $V_{DC}/6$ immediately, as shown in (17).

$$v_{L1}(t_{0-}) = v_{L2}(t_{0-}) = 0, \quad v_{L1}(t_{0+}) = -v_{L2}(t_{0+}) = V_{DC}/6. \tag{17}$$

Due to the parallel connected capacitor in the structure of Fig. 6 (b), the DC-link node voltage cannot change instantly and must remain the same at instants t_{0-} and t_{0+} so that

$$v_o(t_{0+}) = v_o(t_{0-}) = V_{DC}. \tag{18}$$

DC inductor L_{P3}/L_{N3} supports the rated DC voltage at the instant following the fault, so that

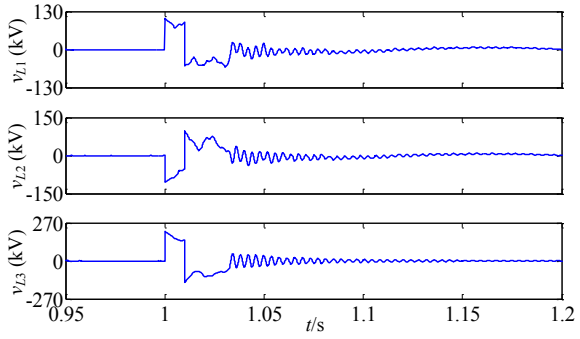
$$v_{L3}(t_{0+}) = V_{DC}/2. \tag{19}$$

As shown in (20) below, the voltages across DC inductors L_{P1}, L_{N1}, L_{P2} and L_{N2} are zero at t_{0+} and increase until the fault is isolated by mechanical DCCBs B_{P3} and B_{N3}.

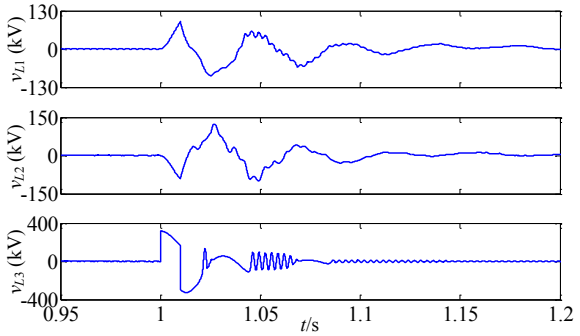
$$v_{L1}(t_{0+}) = v_{L1}(t_{0-}) = v_{L2}(t_{0+}) = v_{L2}(t_{0-}) = 0 \ll V_{DC}/6. \tag{20}$$

For the structure of Fig. 6 (b), the initial voltages across L_{P1}, L_{N1}, L_{P2} and L_{N2} immediately following the fault are much lower than for the structure of Fig. 6 (a). As a result, the increase in the fault current flowing through DCCBs B_{P1}, B_{N1}, B_{P2} and B_{N2} is slower.

Fig. 10 shows the voltages across the DC inductors in the two proposed protection structures. Prior to the fault, all the inductor voltages are approximately zero. As shown in Fig. 10 (a), after the fault is applied at t=1s the inductor voltages in the structure of Fig. 6 (a) step to 107kV, -107kV and 213kV respectively, which are in good agreement with (16) and (17). For the structure of Fig. 6 (b), voltage v_{L3} is 320kV whilst inductor voltages v_{L1} and v_{L2} increase from 0 after the fault, as shown in Fig. 10 (b).



(a) Combined inductance L and mechanical DCCB



(b) Combined inductance L, capacitance C and mechanical DCCB

Fig. 10. Voltages across the inductors at the DC-link node.

Compared with the structure of Fig. 6 (a) with additional inductance only, the structure with additional inductance and capacitance shown in Fig. 6 (b) can better support the DC-link node voltage after the fault, thereby reducing the fault currents in the converters. However, this benefit is at the expense of higher capital cost and higher fault current for the DCCBs connected to the faulty branch, when compared with the structure shown in Fig. 6 (a).

V. Performance Evaluation

A. Continuous Operation without Active Fault Current Control

Continuous operation of the healthy parts of the network in

the event of a DC fault at one DC branch is assessed using the multi-terminal HVDC model defined in Fig. 1 and Table I, in the MATLAB/Simulink® environment with a sample time of 5μs. The simulated scenarios are identical to those discussed in Section IV B. The two proposed protection structures shown in Fig. 6 are tested and the results are compared.

1) Combined inductance L and mechanical DCCB

The results for inductance L=500mH are shown in Fig. 11. As shown in Fig. 11 (a), (b) and (f), after the DC fault the minimum DC voltage of S_1 is approximately 0.84pu (535kV) whilst the peak fault arm current in S_1 is limited to 1.5pu (3.5kA), which is lower than its maximum current threshold of 2pu. The peak fault arm current in station S_2 is 1.4pu (1.5kA), and is lower than that in S_1 due to the larger short-circuit impedance (longer cable) and smaller initial current, as shown in Fig. 11 (c) and (d).

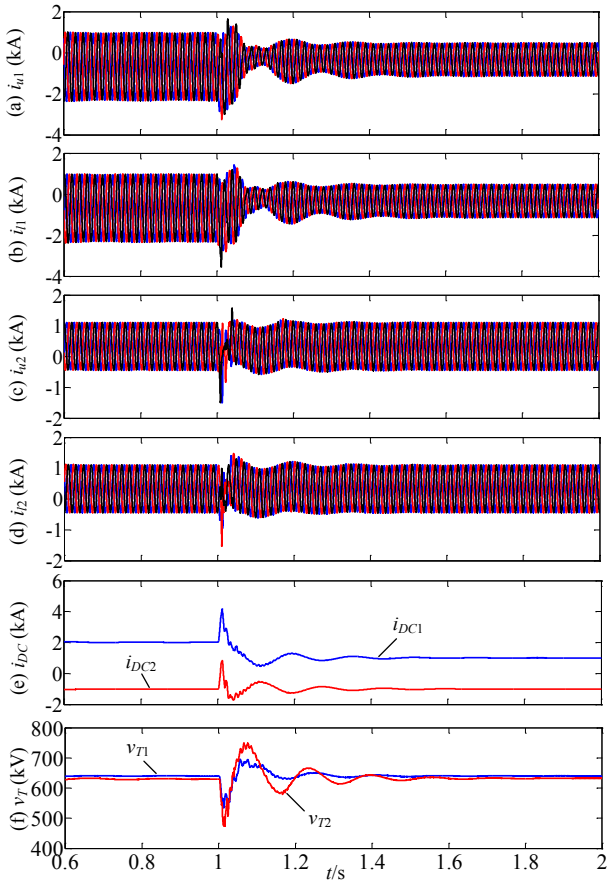


Fig. 11. Simulated waveforms during continuous operation, for a DC fault at t=1s using the combined inductance L and mechanical DCCB protection structure: (a) upper and (b) lower arm currents of station S_1, (c) upper and (d) lower arm currents of station S_2, (e) DC current, and (f) DC terminal voltage.

Once station S_3 and Cable 3 are isolated, the healthy parts of the network (S_1, S_2, Cable 1 and Cable 2) can resume normal operation. The steady-state DC current in S_1 is thus reduced from 2kA to 1kA, and is balanced by current flow of -1kA in S_2, as shown in Fig. 11 (e).

The DC terminal voltage v_{T3} of station S_3 is shown in Fig. 12, where v_{T3} oscillates following the pole-to-pole DC fault and drops to zero eventually. The opening of mechanical DCCBs B_{P3} and B_{N3} does not expose S_3 to significant over-voltage.

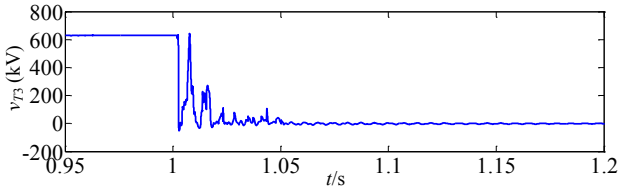


Fig. 12. DC terminal voltage of station S_3 which is connected with the fault branch.

The current and voltage stresses of the inductors at the DC-link node are shown in Fig. 13 and Fig. 10 (a) respectively. As breaker B_{P3} is connected to the faulty branch at the DC-link node, the fault current flows through the mechanical switch until the switch opens at around t=1.01s. The current previously flowing through the switch is then commutated into the surge arrestor and drops to zero at around t=1.035s. As seen, the voltage across the circuit breaker is limited without exposing to significant over-voltage. The current dropping rate following the opening of the mechanical switch is lower than the current increasing rate after the fault is applied.

Due to the series connection of DCCB and DC inductor, the DCCBs B_{P1}, B_{P2} and B_{P3} share the same currents with DC inductors L_{P1}, L_{P2} and L_{P3} respectively, as shown in Fig. 13.

The corresponding voltages across the DC inductors L_{p1}, L_{p2} and L_{p3} have been demonstrated in Fig. 10 (a). As V=Ldi/dt, it can be seen that the Ldi/dt is limited to 150kV following the opening of the mechanical switch, being much lower than that at fault initiation (213kV). This benefits from the voltage limitation function provided by the parallel-connected surge arrestor.

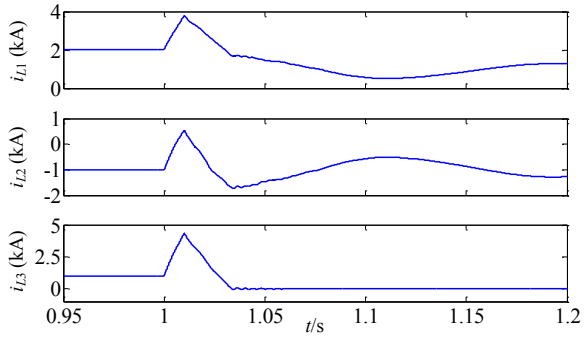


Fig. 13. Currents of the inductors at the DC-link node combined inductance L and mechanical DCCB.

Fig. 14 shows the waveforms of breaker B_{P3} connected on the faulty branch at the DC-link node. At around t=1.01s when the switch opens, the current flowing through the mechanical DCCBs reaches the peak of 4.4kA, as shown in Fig. 14 (a). In Fig. 14 (b), the voltage across the circuit breaker is lower than 480kV. Only circuit breaker B_{P3} opens after the fault while B_{P1} and B_{P2} continue to transfer power between stations S_1 and S_2. As a result, the voltages of the surge arrestors in B_{P1} and B_{P2} are around zero and they do not absorb energy during the fault. All the opening energy is absorbed by the surge arrestor in B_{P3}

and this energy is around 21MJ, as shown in Fig. 14 (c).

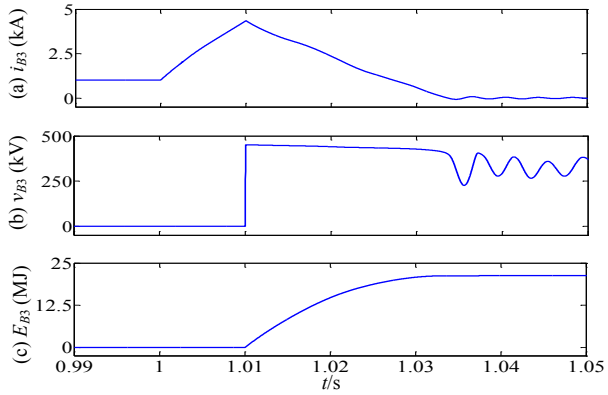


Fig. 14. Waveforms of DC circuit breaker B_{P3} at DC-link node: (a) current, (b) voltage, and (c) absorbed energy.

2) Combined L, C and mechanical DCCB

For this study, the same inductance of 500mH is used and the capacitance is set at 50μF. The simulation results show that the protection structure with additional capacitance can further improve performance. Peak fault arm currents are reduced by 14%, whilst the minimum DC voltage at station S_1 is increased by 4%, when compared to the other protection structure. However, this is achieved at the expense of an additional high-voltage DC capacitor, and the resulting comparative increase in capital cost.

For both scenarios, even under the most severe pole-to-pole DC fault conditions and using mechanical DCCBs, the healthy parts of the network can continue to operate without being subjected to significant fault currents. Shutdown of the entire multi-terminal HVDC system is thus avoided.

B. Active Control of DC Fault Currents

In this simulation scenario, 500mH inductors are connected to the DC-link node and a pole-to-pole DC fault is applied at the location shown in Fig. 6 (a). As the purpose of the study is to investigate the peak current 10ms after fault detection and to avoid the influence caused by transients, no DCCB opening is simulated and only the voltage and current waveforms during the first 15ms following the fault are shown. In the simulation, the fault is applied at t=0.2s.

Fig. 15 compares system performance during the fault, with and without the proposed active control strategy. In the initial stages of the fault, the fault current magnitude is still within the predefined dead band and the active controller does not act. Thus the conventional and the active control strategies both exhibit the same DC-link fault current. When the fault current reach the dead band limit, the active controller acts to suppress the fault current, as shown in Fig. 15 (a).

By regulating the DC components of the arm voltages, the proposed active control strategy reduces the DC components in the fault arm currents. This implies that SM capacitor discharge current is reduced and capacitor voltage can be maintained at a higher value during the fault, as shown in Figs. 15 (b) and (c). This characteristic improves the controllability of the converter and reduces current and voltage oscillations during system restoration following fault isolation. As the SM capacitors provide less energy to the DC side, the terminal voltage under active control is slightly lower than that with conventional control, as shown in Fig. 15 (b). The ability of the proposed active control strategy to regulate the DC components of the fault currents means that peak arm current 15ms after the fault is reduced from 1.7pu (4kA) to 1.4pu (3.2kA), as shown in Fig. 15 (c) and (d).

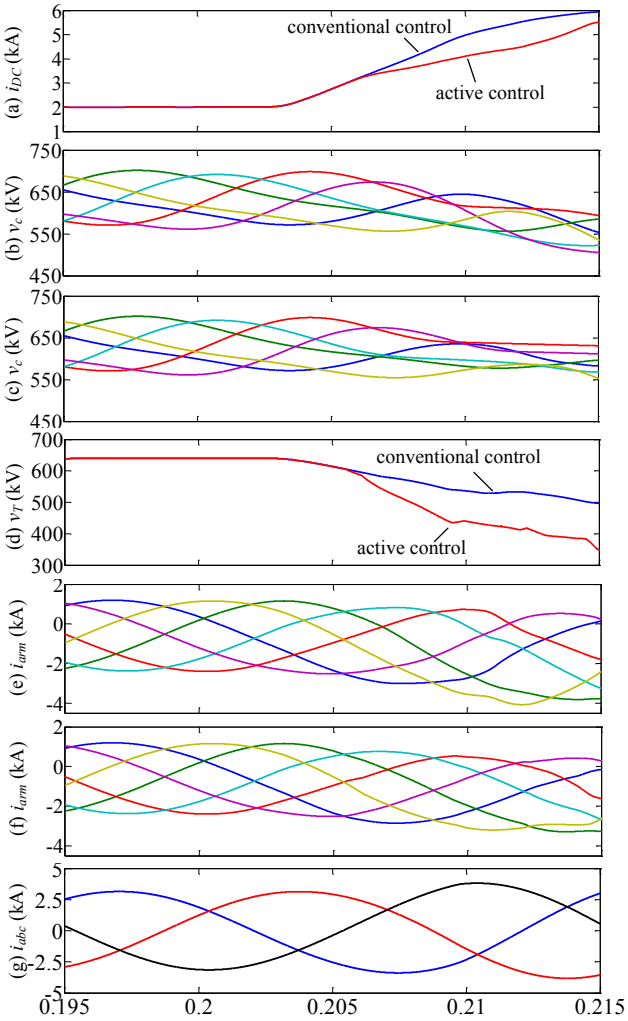


Fig. 15. Comparison of conventional and the proposed active control strategies: (a) DC current, (b) arm capacitor voltages under conventional control, (c) arm capacitor voltages under active control, (d) DC terminal voltage, (e) arm currents under conventional control, (f) arm currents under active control, and (g) three-phase AC currents under active control.

As the HB SMs are incapable of generating negative voltages, the proposed active control strategy cannot suppress the fault currents to zero. Fault currents can still, however, be reduced significantly. With the same peak current during the fault, the size of the passive components can be reduced by adopting the proposed active control, yielding lower capital cost and reduced volume. In the preceding scenario, the inductances in the DC-link node can be reduced from 500mH to 325mH by adopting the active control strategy, whilst the peak arm current is maintained at 1.7pu.

VI. Discussion

A. Consideration of Passive Component Size

With 500mH inductance at the DC-link node, the fault arm current is limited to 1.5pu, as shown in Fig. 11. When the DC inductance is reduced to 270mH, illustrated in Fig. 9, the fault arm current is still slightly lower than the threshold of 2pu (4.7kA). Another reason of requiring relatively large additional passive components is the long opening time of mechanical DCCB (10ms) considered in this paper. If the mechanical DCCB has 5ms opening time as suggested in [26] and [27], the DC inductance can be reduced from 270mH to 120mH. Additionally, the inductances at the DC-link node can be reduced further from 120mH to 70mH by adopting the proposed active control strategy, whilst the peak arm current is limited to 2pu. The DC-link node inductance of 70mH is in the similar range as the typical values of smoothing reactors in line commutated converter (LCC) HVDC [31, 32] and VSC HVDC systems [33, 34]. These factors reduce the DC inductance significantly, which makes the proposed scheme more applicable to potential offshore HVDC project where the volume requirement for DC reactor is critical.

Similar with the DC inductance mentioned previously, the DC capacitance at the DC-link node can also be significantly reduced by using mechanical DCCB with shorter opening time, relatively higher fault current and the proposed active control of DC fault current.

B. Extension to Meshed DC Network

The paper focuses on the DC protection of radial multi-terminal DC network where the simplest three-terminal system is taken as an example to illustrate the proposed approach. However, the proposed novel active control of DC fault current is universal and can be used for all the MMC stations, including that in a meshed DC network. Additionally, the modified DC fault protection structure can be used in meshed HVDC systems, as illustrated in Fig. 16, where both ends of each cable are equipped with the series connection of mechanical DCCB and additional DC inductance.

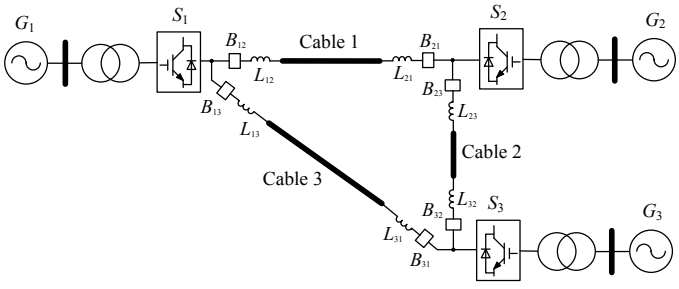


Fig. 16. Meshed three-terminal DC network incorporated with additional DC inductance and mechanical DCCB.

VII. Conclusion

This paper proposes the use of mechanical DCCBs combined with additional passive components and novel converter control to ensure continuous operation of the healthy part of an HVDC network during a DC fault. Two protection structures, comprising inductance L and a mechanical DCCB, and inductance L, capacitance C and a mechanical DCCB, connected to the DC-link node are proposed. The passive components in the DC-link node slow fault propagation, resulting in relatively high DC terminal voltages at the converters connected to the healthy DC network and reduced fault currents. Active converter control for reducing DC fault currents by dynamically regulating the DC components in the arm voltages is proposed. Simulation results show that continuous operation can be achieved, avoiding shutdown of the entire multi-terminal HVDC system. The proposed protection structures and active control of DC fault current provide an attractive approach with low power loss and cost, and high robustness and system availability for application in future multi-terminal HVDC systems.

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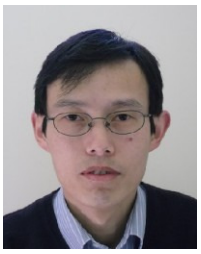

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