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Gate current analysis of AIGaN/GaN on silicon heterojunction transistors at the nanoscale

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The gate leakage current of AlGaN/GaN (on silicon) high electron mobility transistor (HEMT) is investigated at the micro and nanoscale. The gate current dependence $(25-310 \,^{\circ}\text{C})$ on the temperature is used to identify the potential conduction mechanisms, as trap assisted tunneling or field emission. The conductive atomic force microscopy investigation of the HEMT surface has revealed some correlation between the topography and the leakage current, which is analyzed in detail. The effect of introducing a thin dielectric in the gate is also discussed in the micro and the nanoscale. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4748115]

The gate leakage current is an important limitation of the III-V high electron mobility transistors (HEMTs). In particular, minimizing the off-state leakage currents in AlGaN/ GaN HEMT is primordial to their implementation into systems with low noise and low power consumption.¹ This is particularly true when the GaN buffer is grown on silicon. Its narrow bandgap, together with the lattice mismatch and the thermal expansion coefficient difference, makes the AlGaN/ GaN on Si stack challenging for sustaining high voltages with low leakage. In this letter, AlGaN/GaN-on-Si different HEMT gate architectures were investigated by the macroscopic I–V-T approach and scanning probes at the nanoscale. Schottky gate HEMTs were fabricated on a previously optimized stack to obtain a crack-free GaN layer up to $2-3 \,\mu m$ thick on commercial Si(111). AlGaN/GaN layers were grown by molecular beam epitaxy (MBE) using ammonia as the nitrogen precursor in a Riber Compact 21 MBE system. The Si/GaN nucleation layer was basically formed by 40 nm of AlN, 250 nm of GaN, and 250 nm of AlN grown at 920 °C. These nucleation layers were used to overcome the formation of cracks, which are due to the large difference in the thermal expansion coefficient between GaN and Si. Then, a 1.7 μ m GaN (0001) buffer layer was grown at 800 °C, followed by the active layers. The active layer of the HEMT consists in a 1 nm AlN spacer to reduce alloy scattering and to enhance the electron mobility, and a 21 nm undoped AlGaN barrier with 0.28 Al mole fraction. Finally, the structure was covered with an additional 5 nm GaN cap layer. The device isolation was achieved by means of a 150 nm deep mesa etch, realized by Cl₂/Ar reactive ion etching (RIE). Source/drain Ohmic contacts were formed by a Ti/Al/Ni/Au annealed for 30s at 750°C by rapid thermal annealing. HEMT gate contact was made with a Ni/Au bilayer. A way to further reduce the gate leakage current is the introduction of a thin dielectric between the gate metal and the GaN surface in an approach known as metal insulated gate HEMT (MIS-HEMT). Here, the previous structure was capped with 20 nm of silicon nitride (SiN) grown by remote plasma-enhanced chemical vapor deposition using a nitrogen plasma and pure silane. Fig. 1(a) presents the transfer curves characteristic of a Schottky gate HEMT with gate leakage current of $\sim 1 \,\mu$ A/mm ($W = 150 \,\mu$ m.). The MIS-HEMT gate current was effectively reduced one order of magnitude.

At the macroscale, HEMT reverse vs temperature characterization was performed in the temperature range of 25-310 °C (Fig. 1(b)). The gate leakage does not depend on the reverse bias or the temperature up to 150 °C. Then, I_{gs} appears to be constant ($V_{ds} < 75$ V) but strongly depending on T, thus suggesting a thermally activated process which follows an Arrhenius law $(I = I_0 \exp[-E_a/kT])$, where E_a is the activation energy and k is the Boltzmann constant. From the Arrhenius plot $\log\{I_{ds}\}$ vs 1/T, the activation energy can be determined as $E_a \sim 0.40 \,\mathrm{eV}$ (Fig. 1(e)). Analogously, two terminals gate-bulk (I_{gb}) I-V-T measurements were also performed to determine the vertical gate-bulk current (Fig. 1(c)). In this case, I_{gb} greatly degrades when the current is forced through the AlGaN region for $T > 160 \,^{\circ}\text{C}$. The fact that the vertical I_{gb} is nearly independent of T suggests the tunneling as the dominant transport mechanism of the current flow. Indeed, a plot of $\log\{J/V^2\}$ vs 1/V (Flowler-Nordheim plot)² confirms the very weak temperature dependence (not shown). For the smaller gate-to-bulk bias $(V_{gb} < 10 \text{ V})$, the measured macroscopic current densities are observed to be dependent on both the voltage and temperature. I_{ab} seems to follow the Poole-Frenkel mechanism,³⁻⁶ being linear in a $\log\{J/V\}$ vs $V^{1/2}$ plot (Fig. 1(d)). The experimental emission barrier height was determined to be $\phi_t = 0.3 \text{ eV}, 25\%$ lower than the one determined from the HEMT's reverse thermal activation. In any case, it is believed that the emission is from a trap state to a continuum band of states, located somewhere within the bandgap associated with threading screw conductive dislocations.³ This will be further investigated at the nanoscale by means of the conductive atomic force microscopy (CAFM) technique.^{7–9}

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FIG. 1. (a) Typical transfer curves I_{ds} (I_{gs}) vs V_{gs} curve for the HEMT and the MIS-HEMT gate architectures. (b) Three terminals gate-source leakage current (for different temperatures) during the off-state reverse bias. (c) Two terminal gate-bulk reverse current showing severe degradation for T > 160 °C. (d) Poole-Frenkel plot of the gate-bulk reverse current at varying *T*. (e) Arrhenius plot for the reverse gate current at $V_{ds} = -150$ V with an activation energy of $E_a = 0.4$ eV.

At the nanoscale, the electrical measurements were carried out with an AFM Agilent 5100 (from Scientec), equipped with a conductive tip and a picoamplifier with an overall amplification of 10^{12} V/A. The scan was performed in contact mode at a frequency of 0.5 Hz. The experiments were performed in dry nitrogen ambient, to protect the samples from oxidation, whilst the entire system works inside a Faraday chamber, to minimize external interference. The tips used in this investigations were conductive doped (Boron 6000–8000 ppms) diamond coated silicon tips with a radius of ~100 nm.

Fig. 2(a) presents a scanning electron microcopy (SEM) view of the HEMT surface. A focused ion beam (FIB) etch on the gate region shows the GaN buffer (delimited by arrows) and the Si substrate. Rough, pitted morphologies were revealed from the 3D AFM shown in Fig. 2(b). The sur-



FIG. 2. (a) SEM image of the HEMT device. The FIB partial etch shows the depth of the GaN buffer (GaN). (b) 3D topographic image of the HEMT surface. (c) Topography and (d) current map of HEMT' gate surface taken with the CAFM for the $10 \times 10 \ \mu m^2$ scan.

face is composed of mounds, in the form of a truncated elliptic parabolic corresponding to the morphological pattern, schematized in the inset of Fig. 2(b). The mound size distribution is rather uniform with, on average, a base of $1.5 \,\mu m$ and a height of 100-200 Å (peak to valley distance). The GaN buffer mode of growth is a complex process from spiral growth to kinetic roughening resulting in the mound topography.¹⁰ The strain in the upper AlN layer is almost totally relaxed and the 1.7 μ m thick GaN buffer layer is grown compressively strained. In the first stages of growth (below $0.7 \,\mu m$), surface diffusion can be enhanced by the compressive strain, leading to spiral formation via a Burton, Cabrera, and Frank (BCF) mode of growth. A coarsening of the growth mounds was observed and correlated to the dislocation density increase. It is believed that the misfit strain due to the heteroepitaxial growth plays a key role in the crossover from screw dislocation induced spiral growth to kinetic roughening. As the growth proceeds, the strain relaxation increases and the surface diffusion decreases. This leads to a transition from step flow-dominated growth mode to a mixed growth mode, where 2D nucleation is sufficiently active to give rise to kinetic roughening. Therefore, for thickness above 0.7 μ m, the mode of growth turns to a kinetic roughening characterized by the scaling behavior of the surface. After that, the MBE growth temperature is sufficiently low for avoiding thickness and composition modulation in the cap and barrier films.

Fig. 2(c) shows the morphological image of the gate region. White area corresponds to the gate strip. Fig. 2(d)shows the current map of the gate region (gate electrode was floating). The current was found to be superior in the pad strip, when compared with the GaN cap surface, probably due to an improved drainage of electron in the vicinity of the tip. The high current, in the boundaries of the gate, is believed to be due to a measurement artifact. When you zoom-in, in the gate pad area or in the gate-to-drain source (applying a sufficiently reverse vertical voltage of -2 V), there is also revealed preferential spots for the electron flow. This correlates with the vertical current (V_{gb}) in Fig. 1(c) being actually $-V_{gb}$ (the gate pad is depleting the GaN cap/ AlGaN/GaN surface). This is the same configuration we use for the AFM measurements. We put a positive bias on the back of the silicon and we ground the AFM tip. This is analogous to put a negative bias at the tip contact, and hence the $V_{tip} = -2 V$ and $V_{tip} = -10 V$ notation. Topographical images obtained with the AFM of the HEMT surface are shown in Fig. 3(a). The current profile, obtained with CAFM, shows the conductance distribution of the surface in Fig. 3(b). It is then possible to obtain different current signals along any line, showed in Fig. 3(c) for the biasing tip voltage of -2 V (top) and -10 V (bottom). At -2 V, the current flow is concentrated within reduced areas, which appear as white spots in the image, uniformly located. In principle, depressions in the topography are somehow correlated with the current peaks in the current map (Fig. 3(c)). Conductive areas, denoted as clear (white), means higher current through the tip ($\sim 6 \text{ pA}$), thought this represents just 7% of the measured area $2.8 \times 2.8 \,\mu\text{m}^2$. The current density of the conductive has been calculated to be as high as 2 A/cm² (CAFM tip area was $\sim 300 \text{ nm}^2$).

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FIG. 3. Conductive AFM scans of the HEMT surface in the drain-gate spacing with (a) topography and (b) current map of surface taken with the CAFM for the $2.8 \times 2.8 \,\mu\text{m}^2$ scan; (c) Respective cross-sectional profiles along the solid lines marked in (a) and (b) biased at -2 V (top) and -10 V (bottom).

As the CAFM bias voltage increases up to -10 V(which is the maximum of the measurement set-up), this correlation between the topography and current becomes more evident which is clearly visible in bottom current map of Fig. 3. In this case, the mean current is $\sim 1 \text{ pA}$ with maximum current of 2.6 pA. However, neither all the depressions exhibit large local leakage nor all the mounds are immune to some current spike. This is shown in Figs. 4(a) and 4(b)along the lines L1-L10 (the area scanned in Fig. 4(b) is the same as in Fig. 3(b) again with $V_{tip} = -10$ V). The relative peaks (maxima) of any of the scan lines are identified as Δ_i . In some of the scans (such scan number L7 depicted in Fig. 4(d)), some of the Δ_i peaks exhibit significantly higher current (I > 5 pA), when compared with any of the other relative current peaks. These peaks are labeled as Γ_i . We have observed that (for L1-L9) the 67% of Γ_i peaks take place in depressions between mounds, formed during the first spiral growth stages. However, only the 36% of the Δ_i peaks correlate with a depression. These results suggest that, indeed, there is some correlation between large current peaks and depressions (as suggested in the CAFM map of Figs. 4(a) and 4(b)), but in any case, the correlation is unique.

It is well know that there are many threading dislocations in GaN epitaxial layers and, these threading dislocations, cre-



FIG. 4. CAFM (a) topographic and (b) current map ($V_{iip} = -10$ V) showing the scan lines for the investigation of the correlation depressions vs leakage spots. (c) Cross-sectional TEM image of the MBE GaN grown on AlN. (d) Detailed scan through L7 showing the relative peaks ($\Delta 1$, $\Delta 2$, and $\Delta 3$). (e) Detailed scan through line L10 where four high current spots are found (e1-e4).

ate the boundaries of the network of the sub-grains, which enable the conductive vertical path. The dislocation density can be determined by either plain-view transmission electron microscopy (TEM) or near-field AFM microscopy. Using both methods, the density of threading dislocations in our MBE GaN layers can be estimated to be $5-7 \times 10^9$ cm⁻².¹⁰ The presence of small pits or depression is associated with the emergence of threading dislocations. Depressions linked to two (or a multiple of two) molecular step edge are associated with screw-type dislocations, while the other are connected to edge-type dislocations located at the crystallographic subgrain boundaries. GaN mounds (also known as hillocks) form around pure screw and/or mixed dislocations. It has been widely reported¹¹⁻¹⁵ that spots with enhanced conductivity are related with threading dislocations. In our case, these conductive dislocations appear to have a certain tendency to appear in the depressions, but only one can expect to find them all over the surface. In a similar CAFM study carried out in GaN on sapphire (350 nm MBE GaN), it was found that only ${\sim}10\%$ of growth mounds exhibited current leakage paths.¹⁵ It was postulated then that $\sim 90\%$ of hillocks grown around mixed dislocations, while the remaining $\sim 10\%$ grow around pure screw dislocations. These pure screw dislocations (with a density of $\sim 5 \times 10^8$ cm⁻²) were the solely responsible of the observed leakage paths. The two-regimen mode of growth of the GaN-on-Si can explain this difference. As stressed before, when the GaN (0001) is MBE grown on the AlN layer, screw dislocation induced spiral growth takes place up to a thickness of 0.7 μ m. Then, the screw dislocation induced spiral growth turns to kinetic roughening and the threading pits are visible no more on the top of the mounds (the final GaN thickness was of $1.7 \,\mu\text{m}$). Another significant difference comes from the fact that, in our experiments, the CAFM current is analyzed using a vertical configuration (forcing the electrons though the entire GaN buffer), rather



FIG. 5. Conductive AFM scans of the MIS-HEMT surface in the drain-gate spacing with (a) topography and (b) current map of surface taken with the CAFM for the $2.8 \times 2.8 \,\mu\text{m}^2$ scan; (c) Respective cross-sectional profiles along the solid lines marked at $-2 \,\text{V}$.

than in the commonly reported lateral configuration. Pure edge-type dislocations located at the crystallographic subgrain boundaries may be more effective in this case.

In this sense, one additional feature is clearly visible in the Fig. 4(b) scan. The line L10 analyzes four (e1-e4) of the strongly conductive spots in Fig. 4(e) (these spots are not visible when the tip is biased at -2 V (Fig. 3(b) top)). These spots have a diameter of 130-140 nm and the current peak is larger than the saturation established at 7.5 pA. The frequency of these spots is significantly lower than the expected for the threading dislocations (the estimated density according the CAFM map would be $\sim 6 \,\mu m^{-2}$). Both the size and the density of the highly conductive spots appear to correlate with the reported distribution of nanopipes.¹⁰ These nanopipes were commonly observed (with a density of $\sim 2 \times 10^8 \text{ cm}^{-2}$ and a diameter of 100-200 nm) in the first stages of the heteroepitaxial growth of GaN regardless the growth method and the substrate used.^{10,16} They are systematically ignored as they vanished for thickness larger than $0.7 \,\mu\text{m}$, again when the screw dislocation induced spiral growth turns to kinetic roughening. However, these nanopipes present in the bulk of the GaN layer may enable highly conductive path when the vertical current is sufficiently high. It should be noted that the spots are not visible when the scan is performed at -2 V (Fig. 4(c) top). The fact of having these nanopipe-conduction paths active for tip voltages larger than $V_{tip} = -10$ V correlates well with the double conduction mechanism observed during the I-V vs T microscale measurements resulting in dislocation related Poole-Frenkel $(-V_{gb} < 10 \text{ V})$ and Flowler-Nordheim tunnelling ($-V_{gb} > 10$ V), respectively.

When the same CAFM test is performed on the MIS-HEMT surface, the current at the nanoscale is also significantly suppressed as shown in Fig. 5. At -2 V, there is no correlation between the topography and the AFM tip current

being this current of ~ 0.3 pA. Nevertheless, it was observed after intensive testing that if the bias is increased and a weak point within the insulator is located, then again the AFM current and topography would partially correlate in the same fashion as described before.

In conclusion, AlGaN/GaN HEMT (on Si) gate current is investigated in the micro and nanometric scale. At the nanoscale, depressions in the topography appear to partially correlate with the current peaks in the current map. However, neither all the depressions exhibit large local leakage nor all the mounds are immune to some current spike. This complex relationship is attributed to the inhomogeneous distribution of threading dislocations (with a density of $\sim 70 \,\mu m^{-2}$) formed during the double spiral BCF-kinetic mode of growth and the fact of analyzing the vertical current. Besides, when the tip is biased at -2 V and -10 V, it seems to correlate with the macroscopic I–V-T tests suggesting Poole-Frenkel $(-V_{eb} < 10 \text{ V})$ and Flowler-Nordheim tunnelling $(-V_{gb} > 10 \text{ V})$, which, in turn, would be threading dislocation and/or nanopipe assisted conduction mechanism, respectively. A thin dielectric can effectively mitigate the leakage current also at the nanoscale.

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