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Degradation of polycrystalline HfO_2-based gate dielectrics under nanoscale electrical stress

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The evolution of the electrical properties of $HfO_2/SiO_2/Si$ dielectric stacks under electrical stress has been investigated using atomic force microscope-based techniques. The current through the grain boundaries (GBs), which is found to be higher than thorough the grains, is correlated to a higher density of positively charged defects at the GBs. Electrical stress produces different degradation kinetics in the grains and GBs, with a much shorter time to breakdown in the latter, indicating that GBs facilitate dielectric breakdown in high-k gate stacks. © *2011 American Institute of Physics*. [doi:10.1063/1.3637633]

Intrinsic process variability and aging mechanisms can strongly affect the performance and reliability of MOS devices. The polycrystallization of high-k-based gate dielectrics, which can occur even during relatively low temperature device fabrication steps (e.g., atomic layer deposition, forming gas anneal),[1] has been identified as one of the device-to-device variability sources. Conductive atomic force microscope (CAFM) experiments, which may address nanoscale topographical and electrical properties of dielectric stacks,[2–5] reveal significantly higher leakage currents through the grain boundaries (GBs) than through nanocrystal (NC) grains.[3,6] Theoretical models[7] suggest that the current through the GBs could be related to a large concentration of oxygen vacancies at the GBs, which might effectively act as conductive paths through the dielectric film.[8] However, the relative role of the vacancies vs. topological factors (e.g., the dielectric thickness at the GB region) as well as the evolution of GB electrical properties under electrical stress remains unexplored. In this work, a CAFM technique has been applied to investigate conduction characteristics of the GBs in polycrystalline HfO_2 gate dielectrics. Kelvin probe force microscope (KPFM) measurements were used to assess the charge state of defects in these structures.

The dielectric stack under investigation consists of a 5 nm atomic layer deposited (ALD) HfO_2 film (annealed at 1000 °C to induce polycrystallization) and a ~1 nm SiO_2 interfacial layer grown on a Si substrate. Gate stack properties were investigated using CAFM (air conditions and contact mode). Current and topography maps were measured by applying voltage between the tip and the substrate, and current-voltage (*I-V*) data were collected in a ramped voltage mode at different oxide locations (GBs and grains). Some *I-V* characteristics were also measured with a modified CAFM approach to provide a larger current dynamic range (enhanced-CAFM (Ref. 9)). KPFM (air conditions) was employed to obtain topography and the probe tip-sample contact potential difference (CPD) map, which is proportional to the amount of charge trapped in the dielectric at the probe tip position.[10]

Topographical (a) and CPD (b) images obtained with the KPFM on a fresh (before electrical stress) gate stack are shown in Fig. 1. The map of the topographical depressions associated with the GBs (Ref. 3) and higher CPD signals overlap. A higher CPD signal can be interpreted as downward band bending,[11,12] which indicates a larger concentration of positive charges at a given location. Note that the concentration of positive charges (based on the CPD signal) at the GBs does not depend on the magnitude of the surface depression at the GB, as can be seen in Fig. 1(c). Therefore, GB electrical properties are not caused by the thinner dielectric that is characteristic of the GB region. Fig. 2 shows three consecutive current maps obtained with CAFM on the same area at 4.2 V. The images again exhibit a clear granular structure (dashed lines), related to the polycrystallization of the high-k dielectric, with leaky sites (brighter areas) concentrated around the GBs.[3] The width of the GBs (Fig. 2(a), fresh oxide) was measured to be ~15 nm, which is wider than simulation-based estimations, <2 nm,[8] probably due to the limited CAFM resolution in air, Ø ~ 10 nm.[13] This could also explain why the grains are larger (Ø ~ 100 nm in Fig. 2) than the size obtained by transmission electron microscopy (TEM) experiments (~15 nm); the grains shown in Fig. 2 could correspond to only a subset of larger grains out of all grains in the sample. However, the limited resolution does not impede the ability of CAFM to clearly distinguish the most conductive GBs. Fig. 2 also shows larger (Ø ~ 50 nm) leaky sites. These sites are the breakdown (BD) spots (indicated by arrows) that are centered at the GBs and laterally propagate into the surrounding grains as was discussed in Ref. 14. The evolution of the leakage current with

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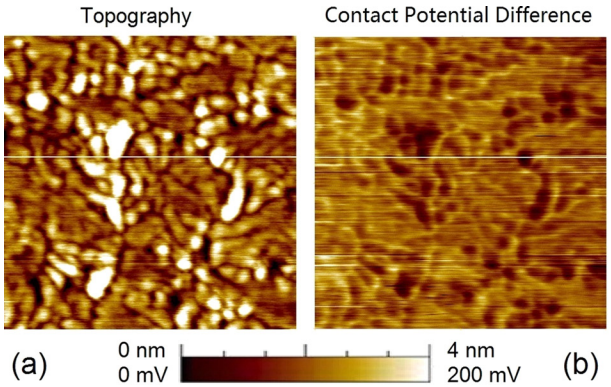

FIG. 1. (Color online) Topographical (a) and CPD (b) 1 $\mu m \times 1$ μm images. Dark lines in (a) and brighter lines in (b) correspond to GBs and higher CPD, respectively. (c) Statistical analysis of the CPD signal showing the potential on the GB sites (V_{GB}) vs. the depth of these sites with respect to the surface of the adjacent grains ($h_{NC} - h_{GB}$). Absence of a correlation between the CPD signal and magnitude of the GB recess indicates that the CPD profile is not caused by the surface topography.

subsequent scans over the same area is equivalent to that caused by electrical stress of different durations. The conductivity of the leakiest spots is observed to gradually increase under subsequent CAFM scans of the dielectric surface; in other words, under continuous stress, the GBs become more conductive. These qualitative results have been further verified by analyzing the evolution of the maximum current through different GBs as the stress proceeds. As an example, Fig. 2 shows that the maximum current through the GB crossing the A-B line for scans 1, 2, and 3 is 2.1 pA, 2.4 pA, and 4.0 pA, respectively. On the other hand, the magnitude of the background current in Fig. 2 (grains, dark areas) seems to be very stable under electrical stress

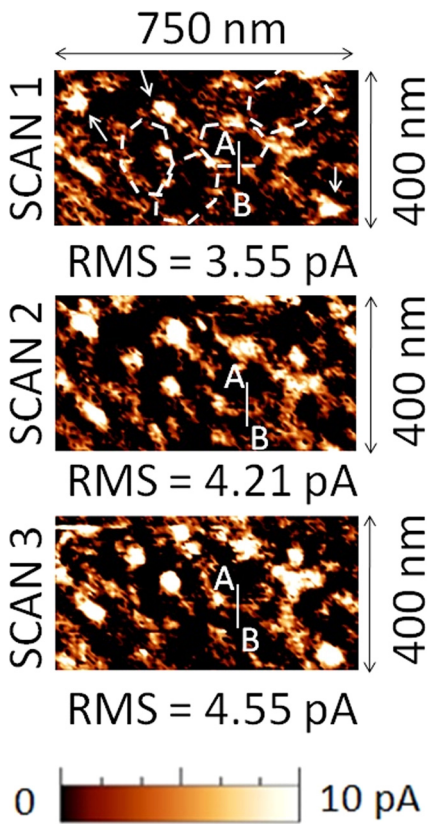

FIG. 2. (Color online) Changes of the current through the HfO_2 polycrystalline layer (with the grains clearly distinguishable) obtained by three consecutive current scans of the same area (750 nm $\times$ 400 nm). The current through the GBs (outlined by the dashed lines) increases with each subsequent scan, i.e., with longer stress time. In particular, the maximum values of the current measured along the A-B line during the scans 1, 2, and 3 are 2.1 pA, 2.4 pA, and 4.0 pA, respectively. Arrows indicates BD spots, which propagate into the surrounding grains.

(0.5 pA for all images), and no new conductive spots were generated. As a result, the overall inhomogeneity of the electrical conduction through the gate stack increases with stress time, which can also be quantitatively observed from the current dispersion magnitudes after different scans. Hence, the gate stack around the grain boundary regions becomes more conductive than the grain regions under the stress.

A comparative analysis of conduction characteristics of the GBs and grains used *I-V* curves measured on fresh and electrically stressed sites. Figure 3(a) shows typical sets of four *I-V* curves subsequently measured on the NCs (filled symbols) and GBs (open symbols) regions. By comparing the first measurements on the fresh locations (NC_IV1 and GB_IV1), it appears that the grains are less conductive than the GBs, in agreement with Ref. 15. Qualitatively different *I-V* dependencies measured on the GB and grain sites indicate that conduction through these structural features might be governed by different mechanisms. For the GBs, a dielectric BD was triggered by the first *I-V* sweep (Fig. 3(a), see differences between GB_IV1 and GB_IV2). On the contrary, when bias is applied to the grains (Fig. 3(a), NC_IV1-NC_IV4), the *I-V* curves progressively shift to lower voltages (stress-induced leakage current[15]) and BD is not triggered until several *I-V* sweeps have been applied. However, when BD is reached, it seems stronger than on the GBs: NC_IV4 exhibits an ohmic characteristic indicating its metallic nature.[16]

To further analyze electrical conduction at these locations, the *I-V* curves were measured with the enhanced-CAFM (having a larger dynamic range) on both GBs and grains (Fig. 3(b)). Again, the fresh *I-V* curves show greater currents at the GB locations (with two conduction regimes,

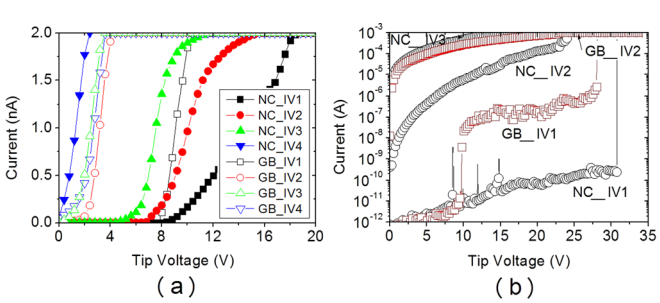

FIG. 3. (Color online) A typical example of the evolution of the current through the grain (NC IV) and GB (GB IV) during the sequential CAFM (a) and ECAFM (b) *I-V* measurements on the same spot. The maximum currents, which can be measured by CAFM and ECAFM, are 2 nA and 1 mA in (a) and (b), respectively. The first *I-V* curves (IV1) were taken on a fresh site.

similar to those observed in other HfO_2-based stacks[17,18]), at which the BD generally occurs at lower voltages. For grains, the initial current is, as a rule, lower, and the pattern of the two conduction regimes is not seen. Moreover, the BD is triggered only after several *I-V* sweeps, indicating greater grain robustness to electrical stress.[19] Higher initial currents at the GBs could be related to the higher concentration of positive charges there (Fig. 1(b)), likely associated with the segregation of positively charged oxygen vacancies at the GBs.[8] This conclusion is consistent with earlier reported simulations of the trap-assisted tunneling current through these defects.[7] Since the GBs in the HfO_2 film are more conductive, more of the voltage applied to the dielectric stack drops across the region of the interfacial SiO_2 layer overlaid by the GBs than the SiO_2 region under the grains. This leads to greater degradation of the former,[20] resulting in a gradual increase in the current measured at the GBs as the stress proceeds and eventual BD of the entire gate stack.

In conclusion, analysis of the electrical properties of GBs and crystal grains in $Si/SiO_2/HfO_2$ stacks before and after electrical stress demonstrates that the GBs are more conductive than the bulk of the grains. This higher electrical conductivity is caused by a different conduction mechanism through the GBs rather than the thinner dielectric regions associated with the GBs. This conclusion is supported by the observation of an elevated concentration of positive charges at GB locations, presumably due to the segregation of positively charged oxygen vacancies near the GBs, which were shown to form a conductive path through the HfO_2 dielectric.[8] Under electrical stress, the GBs degrade faster than the grains, which may be attributed to the degradation of the underlying SiO_2 interfacial layer, eventually leading to the dielectric breakdown of the entire stack.

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