A 135–150-GHz Frequency Tripler With Waveguide Filter Matching

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A 135–150-GHz Frequency Tripler With Waveguide Filter Matching

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***Abstract*— The design and performance of a WR-5 band 135–150-GHz Schottky diode-based frequency tripler which uses waveguide resonator filters for low loss impedance matching is presented in this paper. The filters used in this paper provide filtering, impedance matching, and microstrip (MS) to waveguide transitions in one structure. The matching optimization is achieved by scaling the external quality factors and adjusting the resonance frequency of the filter cavities. This approach transfers most of the tripler's matching networks from MS circuitry to lower loss rectangular waveguide resonators. This is desirable and useful in particular for submillimeter wave and terahertz frequencies. The device presented is a 47.5 to 142.5 GHz biasless frequency tripler with a 15-GHz output bandwidth. The tripler was measured to have a conversion loss of 13.1–14 dB across the band, at an input power of 17 dBm. The measured S_{11} at the input port is better than 15 dB and all the reflection zeros from the filter resonances are distinct. The good agreement between measurements and simulations verifies the accuracy of the filter-based design approach.**

***Index Terms*— All resonator structure, coupling matrix, frequency multiplier, planar Schottky diode, submillimeter wave component.**

I. Introduction

FILTERS and impedance matching networks are fundamental microwave circuit elements. The conventional approach is to design filters and matching networks separately, and then to combine them in series to fulfill the design requirement(s). Components with integrated filtering and impedance matching functions are also possible. Examples of matching networks, which have been integrated with filtering functions, such as impedance transformers with low-pass or bandpass responses, are reported in [1] and [2]. Examples of filters constructed by lumped *LC* components with integrated impedance matching functions can be found in [3] and [4]. These studies are based on coupled planar transmission lines or lumped components, so the methods cannot be easily used in applications where the components are not planar or distributed (e.g., waveguides) or, as in our work, a mixture of both.

Designing filters based on the coupling matrix method has been successfully demonstrated for many application examples [5]. Moreover, the method can also be used to design other microwave passive devices such as multiplexers [6]–[8], antenna filters [9], and Butler matrices [10]. Using the concept of external quality factor and coupling coefficients [5], any kind of resonator can be used to construct a passive microwave device, bringing great flexibility to the design. Such passive devices consist exclusively of coupled resonators, and can be completely defined by coupling matrices. Some combined filtering/matching networks, based solely on resonators and expressed by the coupling matrix, are detailed in [11]–[14]. These articles present a number of synthesis methods used for generating a coupling matrix for filters with arbitrary complex source and/or load impedances. The approach allows the derivation of a coupling matrix so that devices with complex input and/or output impedances can be directly integrated with a filter without the need of an extra matching network. Examples include passive components such as diplexers [11] and antenna filters [14]. Further examples are power amplifiers (PAs) presented in [15]–[18], here the input and output impedances of the active components, transistors, are directly matched by filters, leads to reduced circuit complexity and size.

It is worth noting that all the devices mentioned above operate at relatively low frequencies (below 20 GHz for the passive devices and only a few GHz for the PAs). It is worth extending this method to the design of devices working at much higher frequencies, where waveguides are commonly used for interconnectivity because of their low loss and are small in size. In this paper, filters providing impedance matching functions are used in the design of a WR-5 band, 135–150 GHz, frequency multiplier based on Schottky diodes, as shown in Fig. 1. With this design, the input and output of the diodes are coupled to the third and the sixth resonators

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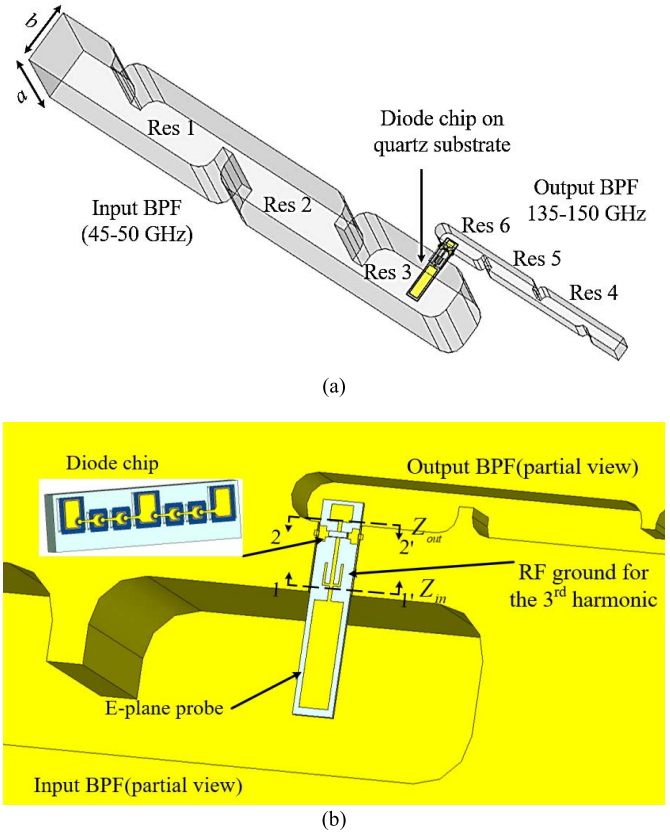


Fig. 1. Frequency tripler using six resonators to perform impedance matching. (a) 3-D model of the tripler with its BPFs $a = 4.78$ mm, $b = 2.39$ mm. (b) Enlarged view of the MS area. The GaAs Schottky diode chip used in this paper is part number SC6/6G2/16p3 from Teratech Components Ltd. This contains six anodes, each of area 1.6×10^{-11} m^2, in series.

via two E-plane probes on suspended microstrip (MS) lines. Impedance matching is directly realized within the filters, removing matching circuits in high loss planar (e.g. MS) structures into high unloaded quality factor (Q_u), waveguide resonators. To the best of the authors' knowledge, this paper reports, for the first time, comprehensive design approach towards high Q_u filters integrated with a high-frequency active device.

Schottky diode-based frequency multipliers are widely used at millimeter/submillimeter and terahertz frequencies, since the direct generation and amplification of signals at such frequencies is difficult [19]. Conventionally, large portions of the matching networks are integrated with the Schottky diodes in MS or coplanar line circuits and these can be lossy, especially at high frequencies. The matching technique adopted in [15]–[18], using coupled resonator filters, is particularly useful for applications at such frequencies since waveguide resonators in general have a lower loss than planar circuits. For instance, the Q_u of a MS resonator, realized at 142.5 GHz using a half wavelength long 50-Ω copper transmission line on a 50-μm-thick quartz substrate, is calculated using CST [20] as $Q_u = 224$. CST predicts that the corresponding WR-5 copper waveguide cavity resonator, operating at TE_{101} mode, has $Q_u = 1940$. Conversely, for a third-order bandpass filter (BPF) centered at 142.5 GHz with a fractional bandwidth (FBW) of 10%, the insertion loss is calculated as 0.54 and 0.062 dB for MS and waveguide filters, respectively [5]. Hence, at high frequencies, it is desirable to move the matching and/or filtering networks from the MS/coplanar circuit to lower loss waveguide equivalents. The application of waveguide impedance matching to the design of millimeter-wave and terahertz frequency multipliers has been reported before [21], [22]. These articles report coupling the Schottky diode chip to the waveguides using transitions and impedance matching using several nonresonant waveguide sections, i.e., reduced height waveguides. We report here on a significant extension of this prior work to include waveguide filtering. These filters provide filtering, impedance matching, and MS to waveguide transition in one structure. The transition is essential for any high-frequency active device design because the active components need to be mounted on a planar circuit where the input and output interfaces are usually waveguides. To include filtering in multipliers is also beneficial in a number of scenarios. For example, in the design of communication or frequency-modulated continuous-wave radar systems, where the RF is created by frequency multiplication of a modulated lower frequency [23], [24]. In such scenarios, the multiplier requires input and/or output filters to suppress unwanted tones from entering and leaving the device. The approach discussed here improves the performance of the system by reducing the component count (and the interconnections) and achieves a lower insertion loss due to the use of high Q_u waveguide resonators.

This paper is organized as follows. The design approach for BPFs with integrated impedance matching function using the coupling matrix is presented in Section II, which is followed by the description of the design of the 135–150-GHz frequency tripler in Section III. Fabrication and characterization of the tripler is discussed in Section IV, and conclusions are given in Section V.

II. Design of the Filter With Complex Port Impedances Using the Coupling Matrix

As discussed earlier, techniques for the synthesis of the modified coupling matrix for filters with complex port impedances have been previously developed. These methods need a well-defined impedance across the whole structure, which is difficult to use in our work as we are dealing with both waveguide and MS, as well as transition structures. As shown in Figs. 1(b) and 2, the input impedance of the diodes at reference plane 1–1′ is defined as Z_{in} and it is assigned as the load of the resonator in Fig. 2 (hence, here we have $Z_L = Z_{\text{in}}$). This impedance can be well defined in the suspended MS mode up to the edge of the waveguide cavity wall, where the transmission mode becomes different. The impedance presented to the waveguide resonator cannot be easily defined or calculated, because the current in the E-plane probe is transferring from the MS mode to the waveguide mode. As a result, the method used previously [15]–[18] is inappropriate in this paper. Therefore, we have used a new alternative approach, starting with the conventional coupling matrix, which does not require prior information about the port impedances.

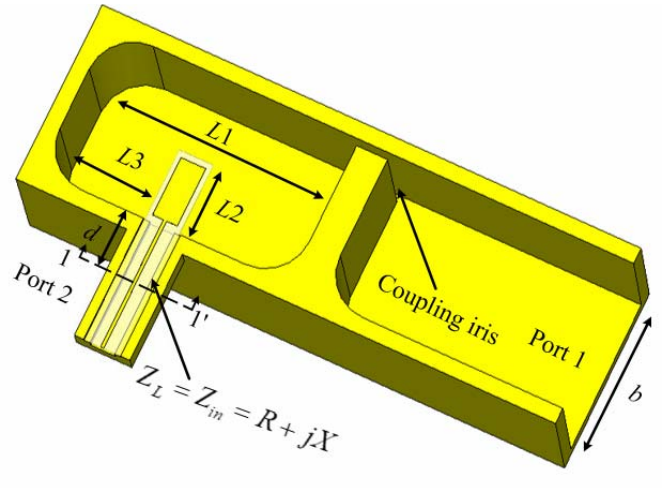


Fig. 2. Single resonator model for extracting Q_e. The input is weakly coupled to the waveguide and the output is coupled to the MS through the E-plane probe. Only the bottom half of the resonator is shown. The load impedance (Z_L) of port 2 equals to the input impedance of the diode cell (Z_{in}) at reference plane 1–1′ shown in Fig. 1.

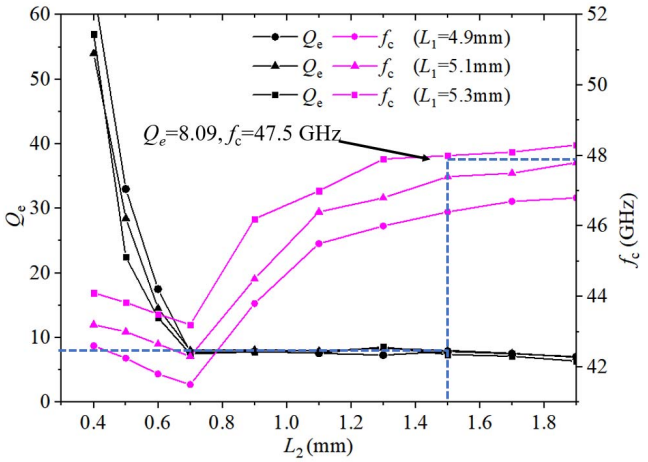


Fig. 3. Extracted Q_e and f_c as a function of the resonator dimensions (L_1 and L_2 varies, while L_3 is fixed at 1.93 mm). The impedance assigned to the microstip port is $Z_L = 47 + j44\ \Omega$ at reference plane 1–1′ shown in Fig. 2, which is $d = 0.10$ mm away from the waveguide cavity wall.

The design of a filter using the coupling matrix method is straightforward: First, the coupling matrix elements are calculated for the desired response [5]. The matrix then gives the coupling coefficients between resonators (M_{ij}) and the external quality factors (Q_e) between resonators and the source/load. To obtain the relationship between the Q_e and the physical dimensions of the structure between the resonator and the source/load, a weakly coupled resonator model is constructed in a full-wave simulator and the Q_e value is obtained from the simulated S_{21} response using [5]

$$Q_e = f_c / \Delta f_{3\,\text{dB}}. \tag{1}$$

Here, f_c is the center frequency of the resonance and $\Delta f_{3\,\text{dB}}$ is the 3-dB bandwidth.

The structure used to calculate Q_e for the input resonators of the tripler is shown in Fig. 2. A scaled version of the same is used for the output. The single resonator, with its output coupled to the suspended MS through an E-plane probe and input weakly coupled to the waveguide, is modeled in CST. For this resonator, the resonant frequency and Q_e are dependent upon the width (b), height, and length (L_1) of the resonator, the position of the probe (L_3), length of the MS feed (L_2), and the value and position (the distance away from the waveguide cavity, d shown in Fig. 2) of the load impedance Z_L. Here, the load impedance (Z_L) of the filter is equals to the input impedance (Z_{in}) of the diode chip in Fig.1(b). The resonant frequency and Q_e are found to be related to these parameters.

The value of Z_L plays an important role in determining the Q_e and f_c for a single resonator, as it defines the boundary condition for the resonator at the MS port. For given resonator dimensions, varying Z_L affects the S_{21} response of the resonator and hence the extracted values of Q_e and f_c. However, regardless the value of Z_L, the extraction process itself is unchanged. Thus, a filter with arbitrary complex load can be designed in the same way as a conventional filter terminated with real load; the only difference is assigning a complex impedance to the MS port.

As an example, consider a third-order Chebyshev filter with a −20-dB passband return loss and a bandwidth of 5 GHz centered at 47.5 GHz and a FBW of 10.5%. This is the input matching filter of the tripler designed in this paper and the coupling matrix is calculated as [5]

$$M = \begin{bmatrix} 0 & 0.108 & 0 \\ 0.108 & 0 & 0.108 \\ 0 & 0.108 & 0 \end{bmatrix}. \tag{2}$$

The calculated external coupling coefficient is $Q_e = 8.09$ (the same for the input and output couplings). In order to find the dimensions of the resonator and probe which corresponds to the center frequency of 47.5 GHz and a Q_e of 8.09, the structure in Fig. 2 is simulated. The load impedance of this filter is complex and taken as $Z_L = 47 + j44\ \Omega$, as discussed later. From the CST [20] simulation results and (1), a plot of Q_e and f_c as a function of the resonator dimensions (L_1 and L_2) can be constructed: Fig. 3. As expected, it is found that there is strong dependence of Q_e on the length (L_2) of the MS probe (because the probe provides coupling between the waveguide and the MS). The required Q_e can be obtained through varying L_2. This yields significant change in f_c, which can be compensated by changing the length of the resonator (L_1). Using Fig. 3, the dimensions of the resonator satisfying the Q_e and f_c requirement were found graphically. The optimal dimensions are $L_1 = 5.1$ mm, $L_2 = 1.5$ mm, and $L_3 = 1.93$ mm, as shown by the dotted lines in Fig. 3.

In this section, we have concentrated on the Q_e of the resonator connected to the diode with complex load impedance. The reason for this is that it is critical to the design of the device with the complex ports. In Sections III-A and III-B, we revisit the filters for the specific tripler design. In Sections III-A and III-B, we discuss the internal resonator couplings and the other Q_e where the impedance is conventional and real.

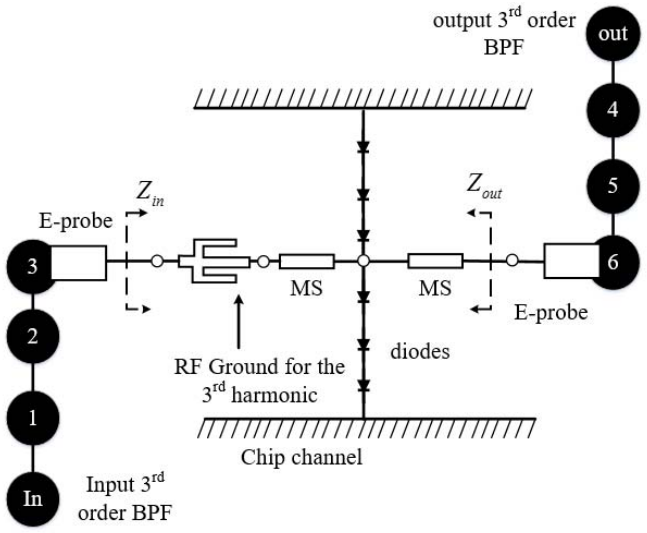


Fig. 4. Diagrammatic view of the resonators (black filled circles) and the couplings (arrows). The input and output of the diodes are coupled via a MS line and E-plane probe to the third and the sixth resonators.

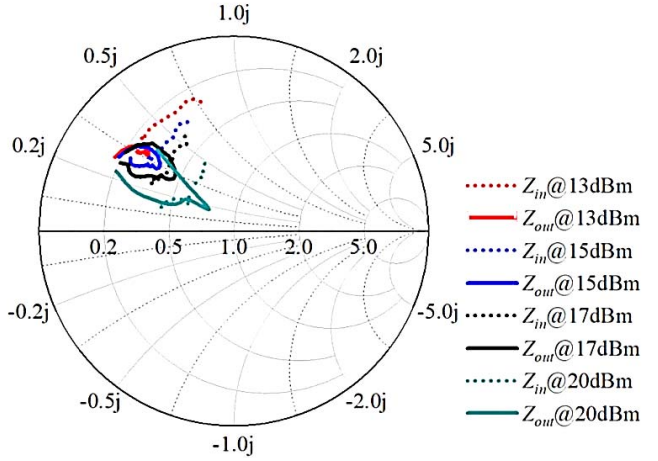


Fig. 5. Normalized input, Z_{in}, and output, Z_{out}, impedances of the diode chip at different input power levels.

We note that this technique is consistent with the calculation of a new coupling matrix with complex loads described in [15]–[18]. For example, if the impedance Z_L is changed in the simulation, the corresponding S_{21} response will be changed and so will the extracted Q_e and f_c. Hence, the size of the cavity (e.g., L_1) needs to be changed to maintain the desired center frequency and the length of the probe (L_2) needs to be changed to maintain Q_e. The former accounts for the additional diagonal term in the complex load coupling matrix [11] requiring a specific cavity frequency different from that of a coupling matrix with real terminating impedances, namely, a nonzero M_{33}. While the latter, changing the length of the probe, results in a different Q_e.

III. WR-5 Band Tripler Design Using Waveguide Resonator Matching

The tripler uses a split-block waveguide design with WR-19 waveguide for the input and WR-5 waveguide for the output, as shown in Fig. 1. The tripler is optimized for 17-dBm input power and an output frequency range from 135–150 GHz, with a 142.5-GHz center frequency.

The conventional topology for a frequency multiplier consists of an input low-pass filter, an input matching network, the diodes (or other nonlinear semiconductor device), an output matching network, and an output high-pass filter [25], [26]. For balanced designs, where a balun has been used, the input low-pass filter can be omitted [27], [28]. In some examples, the output high-pass filtering is implemented using output waveguide cutoff [28]. The new topology, which integrates the matching networks into the rectangular waveguide filter resonators, is shown in Fig. 4. In the chip channel, six anodes are connected in a series balanced configuration, which suppresses the generation of even harmonics [22]. In this all-resonator filter approach, the Schottky diodes are coupled to the third and sixth resonators via E-plane probes. The design procedure for this tripler are as follows.

1) The tripler model, shown in Figs. 1 and 4, is separated into three parts: a) the diode chip and its boxed MS housing; b) the input filter; and c) the output filter. The Schottky diode chip [Teratech Components Ltd device SC6/6G2/16p3, see Fig. 1(b)] was modeled using a 3-D model for the complete chip with internal ports at the anode positions. This enabled accurate S-parameters for this chip, including all parasitic elements, to be obtained, which is critical for obtaining the input and output impedances [29].
2) The embedding impedances of the mounted diode chip at the input and output frequencies, namely, Z_{in} and Z_{out}, need to be obtained for the filter design. Circuit simulation software such as ADS [30] is used to model the nonlinear Schottky junction and to apply harmonic balance simulation to this structure. Some critical diode parameters such as series resistance ($R_s = 2\ \Omega$), ideality factor ($n = 1.2$), saturation current ($I_s = 1.5$ fA), and the nonlinear junction capacitance at zero bias voltage ($C_{j0} = 24.2$ fF) are defined within the ADS diode model. The impedances can be obtained by optimizing the complex source and load impedances at the fundamental- and third-harmonic frequencies for 13–20-dBm incident power level. An open circuit is presented for nontuned harmonics during this process. The extracted impedances are shown in Fig. 5 and Table I. These are assigned to the MS ports of the matching filters.
3) The design procedure discussed in Section II was used to design the input and output filters as discussed in Sections III-A–III-C.

A. Input Filter Design

The input filter is shown in Fig. 6. The MS port is physically connected to the diode chip and the impedance presented to it is Z_{in}, which is a frequency- and power-dependent complex number. The filter is designed to match Z_{in} at 17-dBm input power with a Chebyshev response. A third-order design with

TABLE I

INPUT AND OUTPUT IMPEDANCES OF THE DIODE CHIP AT DIFFERENT INPUT POWER LEVELS AT 47.5 GHz

	13 dBm	15 dBm	17 dBm	20 dBm
Z_{in}	28+j63	38+j53	47+j44	65+j30
Z_{out}	32+j40	36+j34	40+j28	48+j17

*Impedance including the boxed microstrip housing and RF ground between reference plane 1-1' and 2-2' shown in Fig. 1.

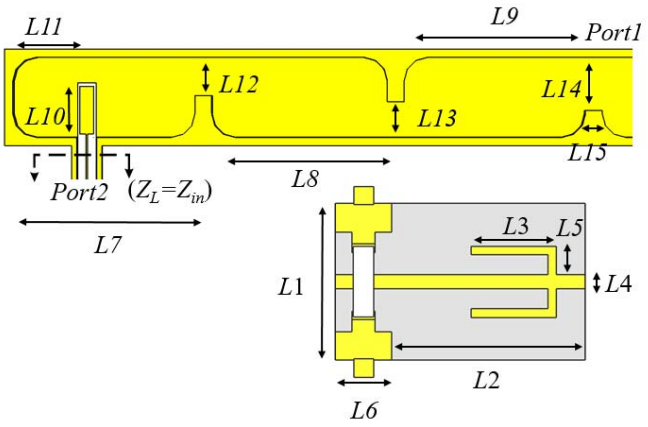


Fig. 6. Design of the input filter. Some dimensions are (in millimeters): $L_1 = 0.55$, $L_2 = 0.58$,$L_3 = 0.30$, $L_4 = 0.05$, $L_5 = 0.10$, $L_6 = 0.20$, and $L_{15} = 0.50$.

TABLE II

INITIAL AND OPTIMIZED DIMENSIONS (IN MILLIMETERS) OF THE INPUT FILTER

	L_7	L_8	L_9	L_{10}	L_{11}	L_{12}	L_{13}	L_{14}
Initial	5.15	4.90	5.10	1.50	1.93	1.00	1.00	1.55
Optimized	5.42	5.23	5.39	1.55	1.93	1.15	1.07	1.59

a −20-dB passband return loss and a bandwidth of 5 GHz centered at 47.5 GHz is chosen; the conventional coupling matrix was given previously in (2). Similarly, the relationship between M_{ij} and the physical dimensions of the waveguide resonators can be found by simulating a pair of coupled resonators with weak external couplings [5]. Once these relationships are found, the initial dimensions for the filter, marked as L_7–L_{14} in Fig. 6, can be estimated from the coupling matrix, as shown in Table II.

The filter with complex load impedance ($Z_L = Z_{\text{in}}$) can be constructed and optimized in CST as a conventional filter, the goal is to achieve the desired frequency response by tuning the dimensions based on their initial values obtained from the coupling matrix. The optimized dimensions are also shown in Table II. Some critical dimensions of the diode chip are shown in Fig. 6. The initial and optimized filter responses are shown in Fig. 7(a), demonstrating that the technique provides good initial values for the design.

B. Output Filter Design

The output filter is shown in Fig. 8, the design is similar to the input filter, the MS port is physically attached to the output

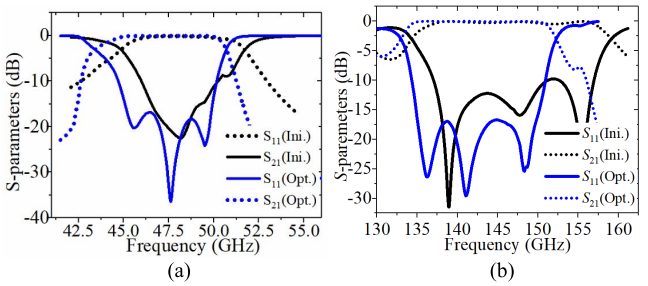


Fig. 7. (a) Input and (b) output responses for the matching filters.

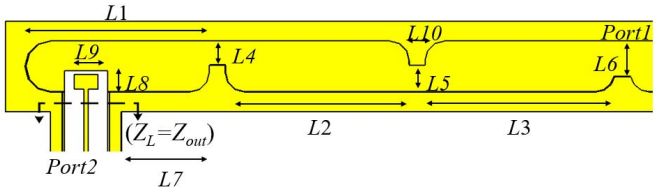


Fig. 8. Design of the output filter. Some dimensions are (in millimeters): $L_9 = 0.30$ and $L_{10} = 0.20$.

TABLE III

INITIAL AND OPTIMIZED DIMENSIONS (IN MILLIMETERS) OF THE OUTPUT FILTER

	L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8
Initial	2.15	2.18	2.20	0.39	0.39	0.45	1.27	0.25
Optimized	2.31	2.37	2.48	0.30	0.34	0.46	1.27	0.22

of the diodes hence the impedance presented to it is Z_{out} (see Figs. 1 and 8). The output filter passband is centered at 142.5 GHz and the filter chosen as a third-order design with a −20-dB passband return loss and a bandwidth of 15 GHz. The coupling matrix for the filter is the same as the input filter and it can be used to estimate the initial dimensions of the output filter. As before, optimization is then performed in CST with the load impedance equal to Z_{out} (at input power of 17 dBm). The initial and optimized dimensions are shown in Table III, with the corresponding filter responses in Fig. 7(b).

From Tables II and III, it can be observed that the differences between the initial and optimized dimensions are about 10%. Trust region framework, a local optimization algorithm [31] integrated in CST [20], is used to perform the optimization which converges fast.

C. Overall Simulated Tripler Design Results

By combining the S-parameter files of the optimized filters and the diode chip with the nonlinear diode model in ADS, the performance of the tripler can be modeled. The simulated tripler performance for 17 dBm of input power is plotted in Fig. 9. The predicted passband return loss, S_{11}, is around −18 dB and the conversion loss vary from 11.2 to 11.8 dB, corresponding to ≈7% conversion efficiency. Simulations for different input power levels were also performed and the S_{11} results are shown in Fig. 9, here the impedance matching deteriorates slightly as the power level deviates from 17 dBm,

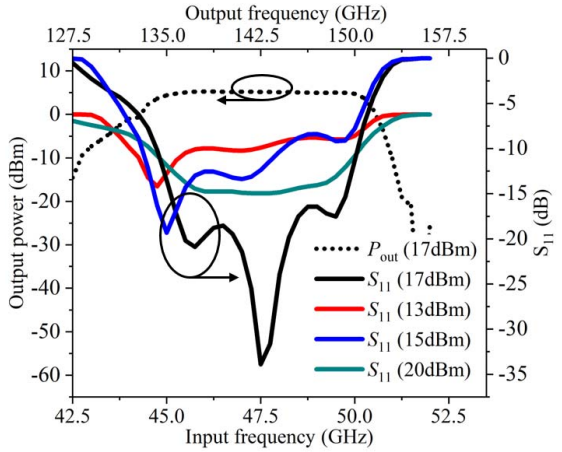


Fig. 9. Simulated output power (dashed curve, in dBm), and input return loss (black solid line), for the tripler at the nominal 17-dBm input power. Return losses for three other input powers are also shown.

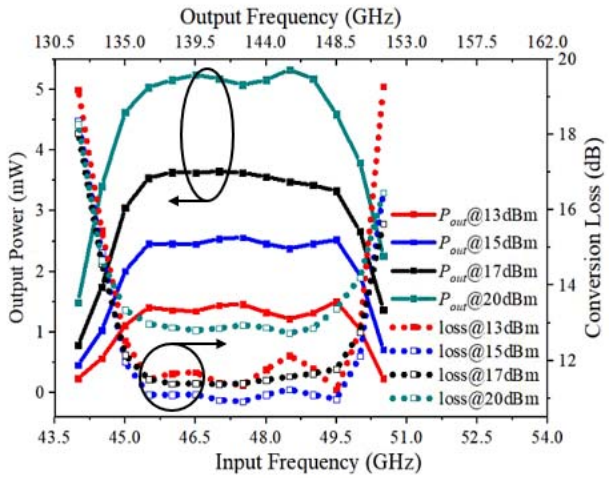


Fig. 10. Simulated conversion loss (broken lines) and output power (solid lines) of the tripler at four power levels.

as the input and output impedances of the diodes vary with power levels, as shown in Table I. The simulated conversion loss and output power for 13, 15, and 20 dBm of input power are shown in Fig. 10. It is noted that although the input impedance is frequency and power dependent, S_{11} for the filter is better than -10 dB across a fourfold power range, and the filter poles, evident as reflection minima in Fig. 9 curves, remain distinct. Only a small shift is predicted for center frequency and bandwidth of the filter, and the effect is that the tripler's power conversion loss is degraded by at most 1 dB as the input power varies.

IV. Tripler Fabrication, Measurement, and Discussion

The split-block waveguide was CNC machined from brass and gold electroplated. The substrate for the suspended MS circuit is 50-μm-thick fused quartz: the diode chip is flip-chip soldered to the gold MS. Fig. 11 shows some photographs of the components before completion of assembly.

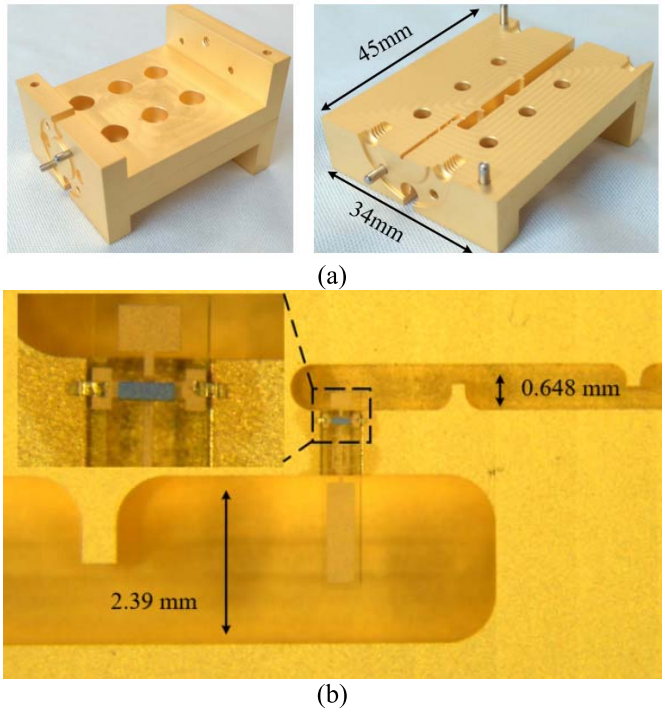
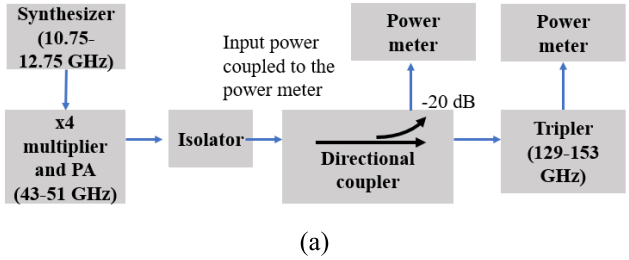
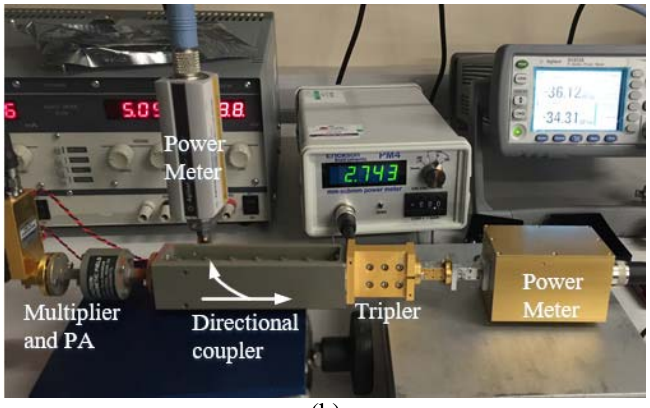


Fig. 11. Photographs of the fabricated tripler. (a) Assembled and split tripler block. (b) Enlarged views of the MS circuit area.



(a)



(b)

Fig. 12. Measurement setup for the tripler. (a) Setup for measuring the output power, where the input power is coupled to the power meter. (b) Setup for measuring the return loss, where the reflected power is coupled to the power meter, as illustrated using the arrowed lines.

The measurement setup for the tripler is shown in Fig. 12. A -20-dB bi-directional coupler was placed at the input of the tripler. A waveguide isolator was used to protect the

TABLE IV
COMPARISON OF SOME UNBIASED MULTIPLIER DESIGNS AT THE SIMILAR FREQUENCY BAND

Reference	Multiplication factor	Output frequency range (GHz)	Bandwidth (%)	Input power (dBm)	Conversion loss Simulated/Measured (dB)	Matching technique
[21]	2	177-202	13	17-20	10-12.2 / 10.5-13	Waveguide sections
[32]	2	135-160	17	20	13-15 / 13-17	Microstrip stubs
[26]	3	60-110	59	20 (typical)	13-16 / 16-22	Microstrip stubs
[33]	3	75-110	35	12-18	13-16 / 13.3-19	Microstrip stubs
[34]	3	114-135	16.8	20	N.A. / 14.5-23	Microstrip stubs
[35]	3	105-120	13.3	20-23	N.A. / 15.2-20	Microstrip stubs
This work	3	135-150	11	17 (typical)	11-12 / 13-14	Coupled resonators

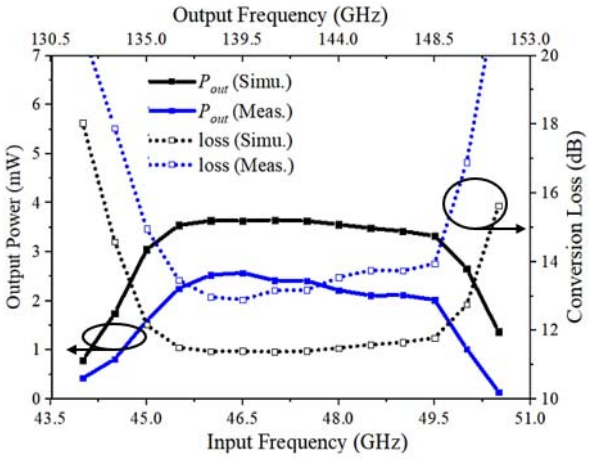


Fig. 13. Simulated and measured output power and conversion loss of the tripler at 17-dBm input power.

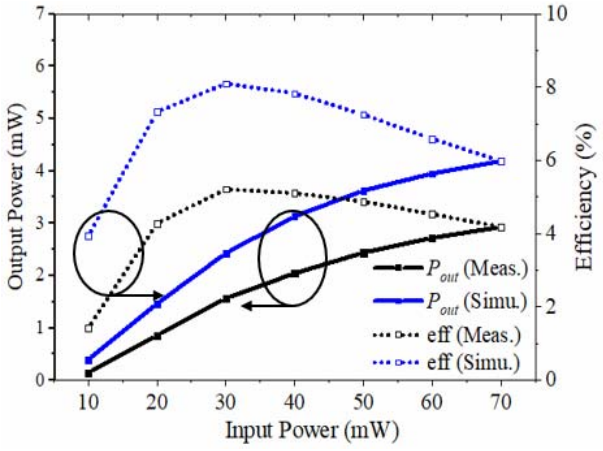


Fig. 14. Output power, solid lines, and efficiency, dashed lines, versus input power at 47.5-GHz input frequency.

driving PA from the remaining reflected power. An Erickson PM4 waveguide power meter was used to measure the output levels and an Agilent N1912A power meter was used to measure the power at the coupling port of the bi-directional coupler.

A. Output Power and Conversion Efficiency

As shown in Fig. 12(a), the directional coupler is placed in a direction that the input–output power can be monitored by the two power meters. Measurements of the tripler were performed for input frequencies from 43 to 51 GHz at a constant input power level of 17 dBm(50 mW). The simulated and measured tripler output powers and efficiency are shown in Fig. 13. The tripler response is also plotted as a function of input power at 47.5 GHz in Fig. 14. The conversion loss remains better than 14 dB up to 70-mW input power, the maximum available power.

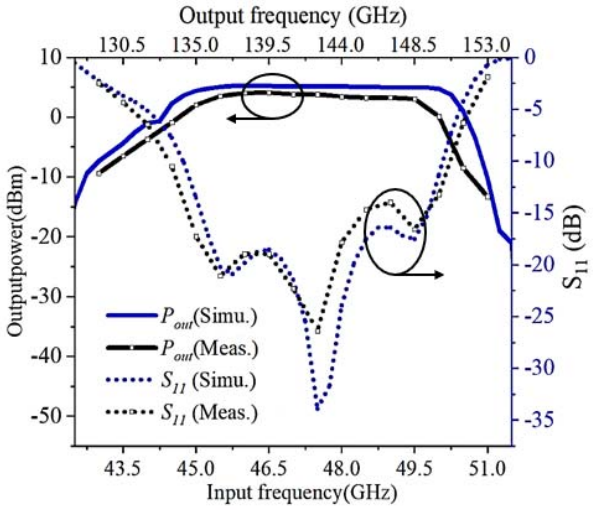


Fig. 15. Simulation and measured results for output power and input return loss of the tripler driven by an input power of 17 dBm.

B. Input Return Loss

As shown in Fig. 12 (b), the directional coupler can be reversed so that the power reflected from the tripler can be measured. The input power is kept at 17 dBm for all frequencies. The measured output power and S_{11} are shown in Fig. 15. Here, the maximum passband S_{11} is around -15 dB, while the conversion loss over the design band (135–150 GHz) is 13.1 to 14 dB, corresponding to 4%–5% efficiency. Overall, very good agreement between simulation and measurement is achieved, especially for the S_{11} response, where the three predicted reflection poles are clearly visible in

the measured response. The appearance of the poles demonstrates the validity the resonator matching method, the design procedure, accurate knowledge of the diode parameters, and the precision of manufacture and assembly. The demonstrated high-quality input match is advantageous in reducing standing wave effects between the multiplier and the driving source.

This paper is compared to some multiplier designs using diodes in unbiased varistor mode in Table IV. In each case the conversion loss reported is similar over the passband. However, unlike other designs, which are usually broadband, the achieved bandwidth of the tripler reported here is inherently narrow. This design aim, as previously stated, is a benefit where filtering is needed [23], [24].

V. Conclusion

A bias-less and fixed-tuned frequency tripler with 15-GHz bandwidth centered at 142.5 GHz, has been demonstrated using coupled resonator filter design principles described by the coupling matrix approach. The input and output connections to the six series connected Schottky diodes are coupled to the nearest, adjoining filter resonators.

Simulations of the tripler predict a conversion loss from 11.2 to 11.8 dB within the 15-GHz passband, while the measured conversion loss at the designed 17-dBm input power level is uniformly 2 dB higher. S_{11} response is accurately simulated, reinforcing the applicability of this filter matching technique to frequency conversion devices. The inherent filtering function of the tripler offer benefits, for example, in communication systems using multipliers stages where filters are needed for the spurious signal rejection. With the proposed method, the resulting matching/filtering circuit can result in a more compact and lower loss system.

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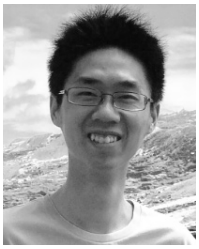

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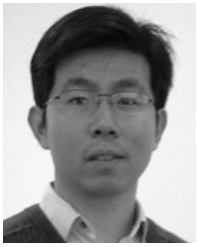

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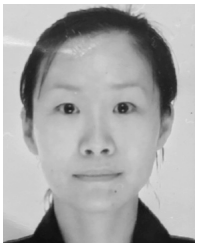

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