Interleaved DC-DC Converter with Wide Band Gap Devices and ZVT Switching for Flexible DC-Link in Electric Vehicle Powertrains

By

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ABSTRACT

The following report details the motivation, design, analysis, simulation and hardware implementation of a DC/DC converter in EV drivetrain architectures. The primary objective of the project was to improve overall system efficiency in an EV drivetrain. The methodology employed to this end required a variable or flexible DC-Link voltage at the input of the inverter stage. Amongst the several advantages associated with such a system are the independent optimization of the battery stack and the inverter over a wide range of motor operating conditions. The incorporation of a DC/DC converter into the drivetrain helps lower system losses but since it is an additional component, a number of considerations need to be made during its design. These include stringent requirements on power density, converter efficiency and reliability.

These targets for the converter are met through a number of different ways. The switches used are Silicon Carbide FETs. These are wide band gap (WBG) devices that can operate at high frequencies and temperatures. Since they allow for high frequency operation, a switching frequency of 250 khz is proposed and implemented. This helps with power density by reducing the size of passive components. High efficiencies are made possible by using a simple soft switching technique by augmenting the DC/DC converter with an auxiliary branch to enable zero voltage transition.

The efficacy of the approach is tested through simulation and hardware implementation of two different prototypes. The Gen-I prototype was a single soft switched synchronous boost converter rated at 2.5kw. Both the motoring mode and regenerative modes of operation (Boost and Buck) were hardware tested for over 2kw and efficiency results of over 98.15% were achieved. The Gen-II prototype and the main focus of this work is an

interleaved soft switched synchronous boost converter. This converter has been implemented in hardware as well and has been tested at 6.7kw and an efficiency of over 98% has been achieved in the boost mode of operation.

ACKNOWLEDGMENTS

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TABLE OF CONTENTS

CHAPTER Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

Chapter 1

INTRODUCTION

1.1 Trends in EV Systems

Global concern for climate change has resulted in accelerated efforts towards minimizing carbon dioxide emissions and reducing the greenhouse effect. At the forefront of these efforts have been policies that have engendered an increase in renewable energy penetration into the electric grid and electrification of vehicles. Due to these efforts, Electric Vehicles (EV) and Plug-in Hybrid Electric Vehicles (PHEV) have experienced a dramatic surge in sales over the past few years reaching over a million units sold globally in 2017 and the trend is set to continue, reaching over 11 million in total sales by the year 2025 [1]. 14% of global greenhouse gas emissions in 2010 were attributed to the fossil fuel powered transportation industry and that encouraged car manufacturers to push for electrification of the auto industry [2]. In this chapter, an overview of the proposed EV drivetrain architecture is provided, highlighting the current state of the art and the additional component proposed and tested as part of this thesis. Further, a number of important metrics for power converters within the drivetrain have been detailed, followed by a comparison of a number of different converter topologies and their suitability for an EV drivetrain.

1.1.1 Conventional EV Drivetrains

The powertrain block diagram shown in Figure 1.1 incorporates a DC/DC converter right after the battery. A typical, state of the art, drivetrain does not include such a converter and links the battery voltage to the inverter. The battery voltage is generally generated

through fuel cells, supercapacitors or a combination of both, [3]. The preferred technology when it comes to a battery stack, however, is lithium ion (Li-Ion) according the referenced works of literature [4] and [5]. The voltage output by the battery is input at the inverter stage, which generates the required 3-phase AC voltage as necessitated by the operating condition of the motor. The Electric Machine (EM) or motor is generally an Internal Permanent Magnet Synchronous Motor (IPMSM) or a conventional Induction Motor (IM). IPMSMs are the preferred type in the applications such as electric vehicles due to advantages in power density, compactness of size and ease of control.

The way the current EV drivetrains are constructed increase the dependence of design metrics for the inverter stage and the motor on the minimum battery voltage. This is because the battery output is directly connected to the inverter and as the battery undergoes a constant change and essentially reduction during operation in its state of charge (SOC), the inverter and motor have to be designed for the worst case battery voltage. What this means is that the worst case battery voltage is required to be sufficient for a certain speed and torque operation of the motor. In many cases, since the speed and torque requirements of the motor are predefine for a given model and make of a car, additional series cells have to be connected in the battery stack to increase the output voltage. This increase the size and weight of the drivetrain and makes the overall operation of the system much less efficient. Plus, for speeds higher than the designed base speed of the motor, which occurs at the rated system voltage, the inverter is incapable of driving the motor any faster because of the DC-Link or battery output voltage limitation. Additionally, the constant high voltage at the input of the inverter causes greater stress upon the semiconductor devices with the inverter

and leads to greater losses and is detrimental to thermal durability. A simple solution to these issues, proposed and implemented in this work, is a DC/DC converter in the EV drivetrain architecture that connects the output battery voltage to the DC-Link or the input of the inverter. Using a lower battery voltage, the DC/DC converter can perform boost operation of the voltage for higher speed operation and can maintain the voltage stress on the inverter at the minimum possible level for a range of operating conditions. Plus, with a lower battery output voltage requirement, the battery stack need not be bulky with too many series connected cells. Plus, the motor and inverter design and optimization can be carried out independently of the battery voltage constraint.

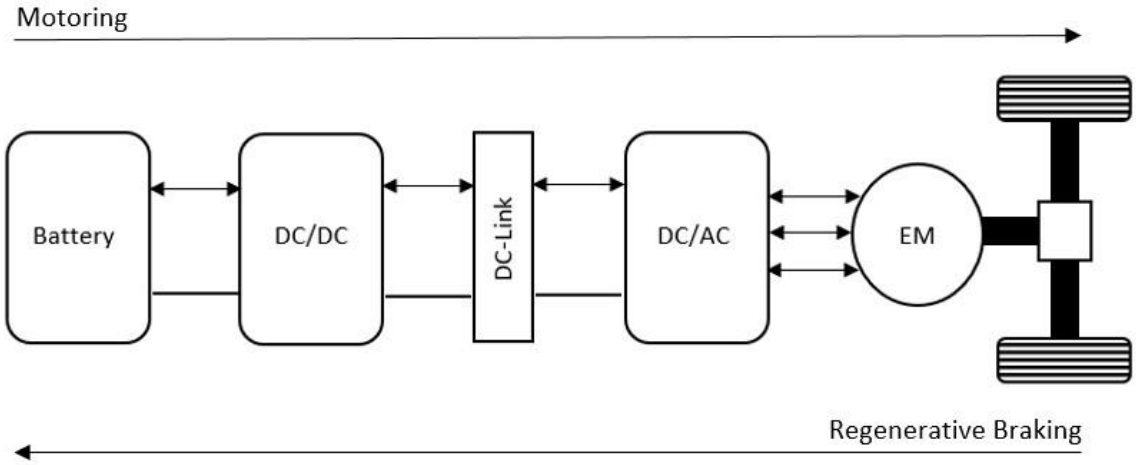


Figure 1.1: Proposed EV drivetrain architecture

1.2 EV Power Electronic Module Design Requirments

Certain design constraints, as outlined in [3], have to be adhered to during design for power electronic converters for electric vehicle applications. These have been briefly explained below:

a. Power Density

The power density requirement is necessitated by, primarily, the limited space within the EV to house electronic components. There are a number of point of load converters that have to be housed within a restricted volume. These include loads such as head and tail lamps, wipers, seat heaters, lighters, cruise control, engine control etc [8]. Adding an additional component such as the proposed drivetrain DC/DC converter into EV thus necessitates compactness of size and volume. A compact converter that is power dense also lends itself to the fact that it adds only marginal weight to the overall weight of the EV for the power level that it outputs. To ensure power density requirements are met, high switching frequencies and wide band gap (WBG) devices have to be used.

b. Efficiency and Thermal constraints

In addition to being one of the most important metrics to be considered for the design of an EV converter, the efficiency and thermal requirements have been at the forefront of the design of the converter proposed in this work. According to [9], operating ambient temperatures for EVs can range from anywhere between 125 ^{o}C to -40 ^{o}C, depending on both the geographical location and the mode of operation. To ensure that the designed converter can adhere to the efficiency and thermal requirements at such high temperatures, wide band gap (WBG) devices have been used for the two main as well as the two auxiliary switches in the proposed converter. WBG devices are a new class of semiconductor switches, including Silicon Carbide (SiC) and Gallium Nitride (GaN) switches. These devices have higher maximum tolerable junction temperatures and higher efficiency, [10]. Additionally, they can operate at higher frequencies and are therefore more compact. The

high efficiency target is, however, extremely important as the proposed converter is an additional component in the drivetrain and is added solely to ensure a highly efficient drivetrain. It is therefore imperative that the losses incurred in this new component are kept to a minimum. The additional converter is therefore designed with zero voltage switching for the main switches and zero current switching the auxiliary switches, which ensures efficiencies over 98%.

c. Electromagnetic Interference constraints

DC-Link voltage ripple has to strictly adhere to the limits set by the Society of Automotive Engineers (SAE). There are specific limits that apply to frequencies in the range between 150Khz to 108Mhz, [8]. This issue has been addressed in the design process by ensuring appropriate filtering, both at the input (as common mode chokes and inductors) as well as at the output (as a DC-Link capacitor). Layout design has also been done keeping in view issues such as common ground potential, low pass filtering through ferrite beads etc.

d. Switch and Component ratings for a wide range of operation

The typical battery voltage range is between 200V to 400V and depending upon the type of motor used, the output voltage generated by the DC/DC converter has to match the requirement at the highest speed of operation. This voltage has been set to a maximum of 800V for this project. This value is higher than the usual requirement but a wide range of operation is generally preferred and such a value lends itself to a better understanding of the converter operation during testing. Since the operation of the inverter is spread out over

a wide range, the switches and other passive devices have to be designed for the maximum rated values.

Since the designed converter follows an interleaved topology, it has some additional features as well. The input current drawn from the battery has significantly less ripple due to the phase shifting of the clock pulses. Plus, the voltage and current stress is distributed amongst the three interleaved stages. Moreover, it is a topology that aids power scaling through the interleaving architecture.

1.3 Converter Topologies Considered for Proposed Design

Three distinct topologies were considered for the design of the proposed converter. These have been detailed in the following section and a conclusion has been drawn based on the merits of each topology in relation to the power density, efficiency and power scaling requirements of the proposed converter.

1.3.1 Synchronous Boost Converter

The synchronous boost converter is essentially the conventional boost converter with an additional switch across the top diode. This switch is called the synchronous switch and it ensures that the converter can transfer current and power in both directions, which is a requirement for EVs as they are expected to operate both in the motoring mode and the regenerative braking mode. In the regenerative braking mode power is transferred back from the motor to the battery. This topology is simple in terms of both hardware implementation and control strategy. For high power operation, however, the passive components might be too large and will severely affect the power density of the design and

indeed the EV drivetrain. The increase in weight and size of the components at high power make this topology infeasible for high power operation. However, the low component count and single power pole do remain good advantages and make the converter a good solution at low power levels. Since it is essentially a boost converter, this topology can only be used to increase the input voltage to a higher value which means that the least voltage output by the converter is the battery stack voltage and this determines the low side operating point of the motor. A high duty ratio can impact the stress on the switches and for the worst case conditions, the DC-Link voltage and inductor current ripple can be high, [11].

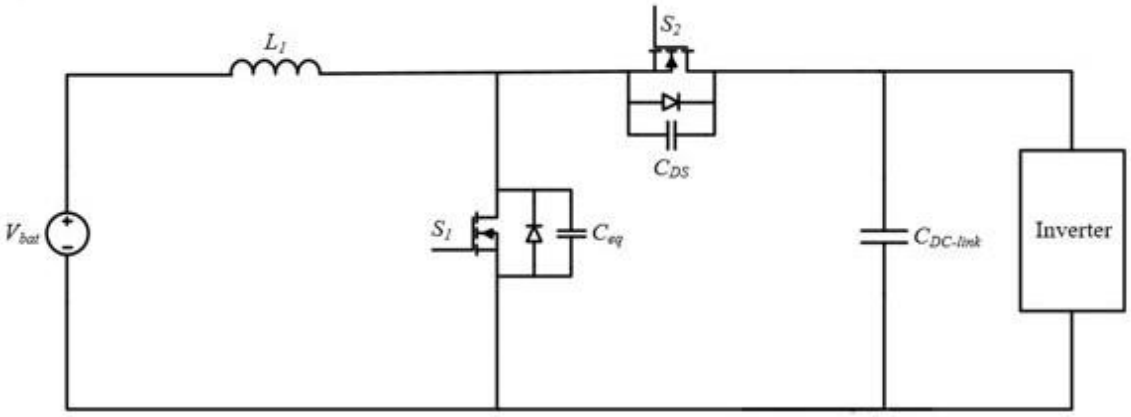


Figure 1.2: Synchronous boost converter schematic

1.3.2 Full Bridge Converter

The significant advantage of this topology over the synchronous boost converter is that it can both step up and down the input voltage. This further reduces the design limitations on the motor and inverter as far as the operating range of the system in terms of speed and torque is concerned. Again, as switches are used in stead of just diodes for current conduction, the topology allows for bi-directional flow of power, which, as stated previously is a requirement in EV drivetrains. The high frequency transformer is used to

provide isolation between the input and the output but at the same time, the leakage inductance of the transformer resonates with the equivalent capacitance across the switches at the output power pole, [10]. This results in ringing and noise in the output which needs additional filtering. The higher number of components add to the weight and complexity of the topology and affect the power density.

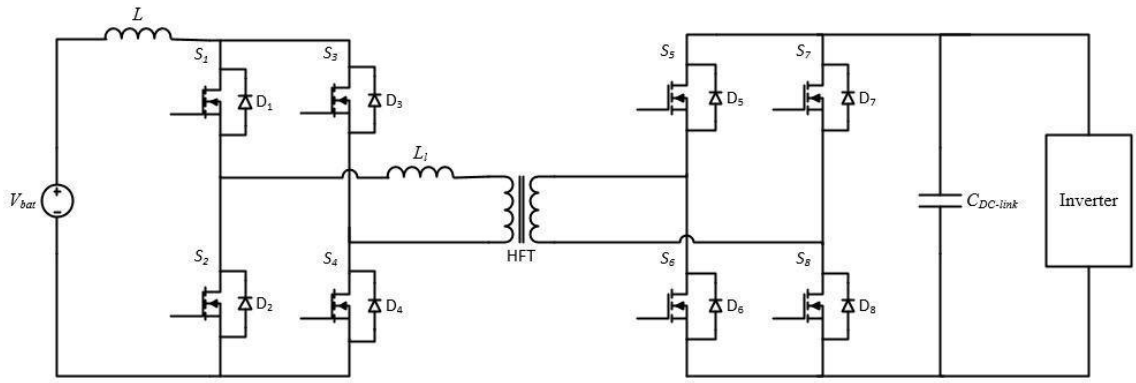


Figure 1.3: Bi-directional full-bridge converter schematic

1.3.3 Interleaved Bi-directional Boost Converter

The interleaved bi-directional boost converter is basically a number of different stages of the synchronous boost converter connected in parallel. The topology maintains all the advantages of the synchronous boost in terms of the component count, simple control, power density and cost. The additional advantages derived from interleaving are lower input current ripple, lower output voltage ripple, smaller passive filter devices, power scaling and improved power density.

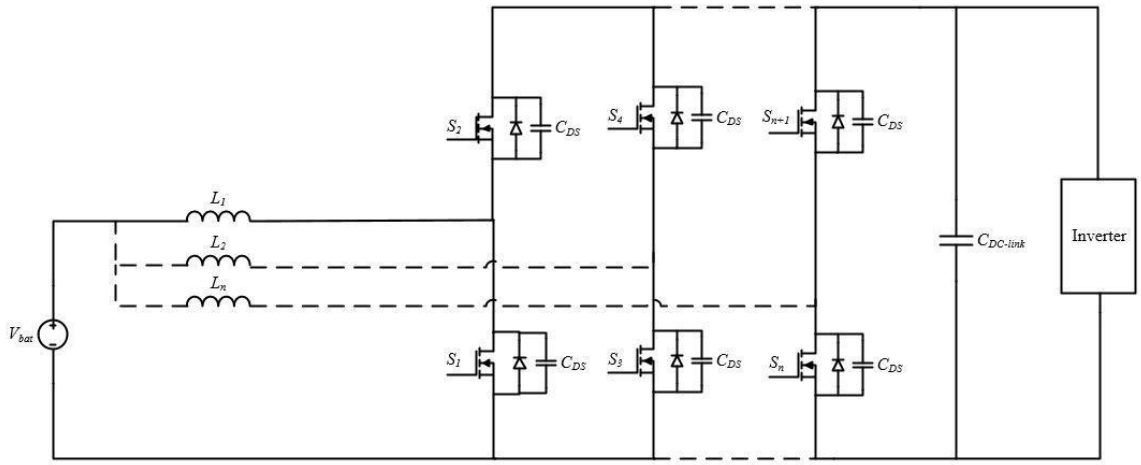


Figure 1.4: Interleaved bi-directional DC/DC converter schematic

1.4 Soft-Switching Converters

One of the major design restrictions other than efficiency requirement on EV power converters is high power density. High power density ensures that any power electronic module incorporated within an EV drivetrain is compact in size and weight and does not add an overhead in terms of load on the motor to carry. In order to achieve high power density, in many cases the switching frequency of the converter is increased. Since the size and weight of the passive components in any power electronic converter is inversely related to the switching frequency, the higher the switching frequency the smaller the passive components such as inductors and capacitors. This method does improve upon the power density of the converter but it has a huge drawback when it comes to the switching losses in the MOSFETs or IGBTs used. The switching losses are directly related to the switching frequency and this is shown in equation 1.1. It is the overlap of the blocking voltage across the switch at the switching transition and the current flowing through the switch at that instant that causes the switching losses. This is depicted in figure 1.5.

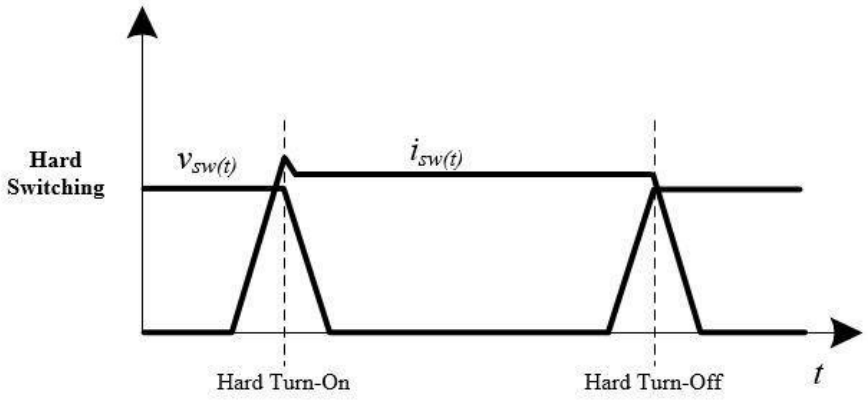


Figure 1.5: Voltage and current overlap in hard-switching schemes

$$P_{sw} = \frac{1}{2} V_{DS} I_{DS} (t_{on} + t_{off}) f_{sw} \quad (1.1)$$

$V_{DS}\ (V)$: Drain-to-Source voltage across the switch
$I_{DS}\ (A)$: Drain-to-Source current flowing in the switch
$t_{on}\ (s)$: Rise time of the switch
$t_{off}\ (s)$: Fall time of the switch
$f_{sw}\ (Hz)$: Switching frequency

Figure 1.5 shows both the turn on and turn off transitions of a given switch. During turn on, the full load current is diverted through the switch in addition to the diode reverse recovery current. As this happens, the voltage across the switch still hasn't dropped to zero. Ideally the switch should only start conducting the current once the voltage across it is zero, however, in the case of hard switching, this does not happen and it incurs losses given by the product of the current through the switch and the voltage across the switch at that instant. A similar behavior leads to turn off losses as well. The voltage across the switch builds up as it still continues to conduct current while the bypass diode of another switch is still not forward biased. During this transition, the turn off losses are given by the product of the instantaneous voltage and current through the switch. This mechanism of switching

is called hard switching and it results in greater stress on the switches which leads to lower durability and increases switch failures due to excessive heat dissipation during the transition periods. [12] has shown how hard switching results in high dv/dt and di/dt stress on switches. Increased frequencies also create EMI issues that require additional filtering and therefore contribute negatively to the power density issue.

A possible solution to reduce switch stress during the switching transitions is to have snubber circuits which are essentially RL or RC networks across the drain and source terminals of MOSFETs. What this does is that it reduces the dv/dt or di/dt, meaning that the rate of voltage or current rise or fall across a switch is reduced. This helps lower the stress on the switches in during these periods of transition from on to off and vice versa and transfers the switching losses to the snubber circuits. Even though this method contributes to the durability of the switches in the long term, it does not help converter losses as a whole and therefore for the purposes of this project, soft switching has been used to not only reduce switch stress but to actually help improve converter efficiency too.

There are three basic types of soft switching converter:

1. Quasi-resonant Converters
2. Load Resonant Converters
3. Resonant Transition Converters

The first two types of soft switching converters employed use frequency control and the voltage and current waveforms are sinusoidal. What this means is that the filters used in

these converters have to designed for low frequency signals and this drastically increases the size of the filters. This is undesirable as it adversely effects power density. On the other hand, resonant transition converters only have resonance between L and C components during the switching transitions. This means that the resonant frequency is very high and the L and C values can be very low. The resonance in such converters brings the voltage or current across or through a switch down to zero before the switching transition takes place.

Soft switching in the proposed converter is realized through an auxiliary conduction branch. This branch consists of two additional MOSFETs with antiparallel diodes and an auxiliary inductor. The two switches allow for motoring mode and regenerative mode of the motor and enable soft switching in both modes. The inductor is used to resonate with the equivalent power pole capacitance which is essentially the parallel combination of the switch capacitances of the main and synchronous switches. The detailed operation of the circuit and how resonance helps reduce switching losses is given in section 3.

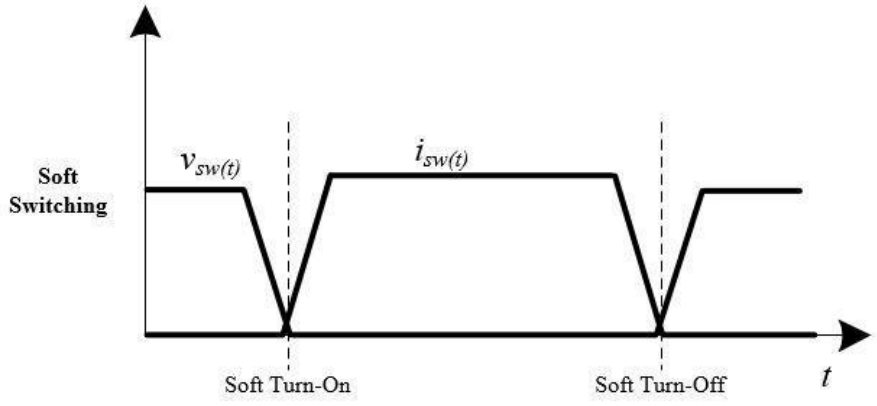


Figure 1.6: Voltage and current transitions in soft switching schemes

1.5 Objective and Organization of the Thesis

The primary focus of this project was to design a high frequency, power dense DC/DC converter for use in EV drivetrains. The motivation for such a converter, as mentioned previously, comes from the fact that the flexibility of the DC-Link voltage has a number of advantages. The most important of these is the improvement of system efficiency for a variety of operating conditions of the entire drivetrain even after the additional component, which is the DC/DC converter, has been squeezed into the drivetrain. In the first phase of the project, a synchronous boost converter rated at 2.5kw and utilizing a switching frequency of 250khz with SiC switches was designed and implemented. For the second phase of the project, three individual converters each rated at 10kw were designed and tested. Finally, the three phases were interleaved together and the interleaved bi-directional boost with ZVT was tested at 10kw. For each scenario, the expected efficiencies were over 98%.

Chapter 2 provides an insight into the motivation for the project through literature review of several relevant publications. The advantages of the DC/DC converter have been detailed here. The impact of the converter on the inverter stage, the motor and the battery stack has been analyzed by carrying out a thorough review.

In Chapter 3, the operation of the proposed topology is analyzed and explained. Each switching interval is dissected and the operating of the converter in terms of current path, voltage across switches during the given interval and the behavior of the auxiliary branch is explained. This is followed by a loss analysis of the converter and then a PLECS simulation schematic and results are provided.

In Chapter 4, the designed converters, both at 2.5kw single phase and 10kw 3-phase have been tested and the results documented. The 2.5kw module has been tested at full load for the motoring mode of operation and 2.0kw for the regenerative mode of operation. The 10kw interleaved 3-phase converter has been tested at rated power for the motoring mode of operation.

The work is concluded in chapter 5 and suggestions for future work to be carried out towards the completion of the project are provided.

Chapter 2

ADVANTAGES OF THE DC/DC CONVERTER AND FLEXIBLE DC LINK VOLTAGE

2.1 Introduction

After having touched upon the motivation behind incorporating the DC/DC converter into the EV Drivetrain architecture in the previous section, here we detail how the system efficiency is impacted by the many advantages of the additional converter and the resulting adaptive DC Link voltage.

2.2 Impact of the Variable DC-Link Voltage

To understand how components of the drivetrain, such as the battery stack voltage, the inverter and the motor itself, are impacted by the addition of the DC/DC converter, first we need to understand the advantage of the variable DC-Link voltage which is a consequence of the DC/DC converter.

Works of literature referenced in the following section show how a drivetrain topology that includes a DC/DC converter and therefore has an adaptive DC Link voltage can help improve the efficiency of the inverter stage and the motor by reducing the switching losses in the inverter and the iron core losses in the motor. This is primarily due to the DC/DC converter providing a stable voltage at the input of the inverter in keeping with the incumbent operating state of the motor, which is determined by the line to line voltage requirement of the motor for a given speed.

An experiment has been set up in [13] by Schoenen et al to show the impact of the DC/DC converter and flexible DC Link voltage on the efficiency of the system. It is shown that through a variable DC-Link the PMSM machine design requirement can be relaxed and it does not have to be designed for a minimum battery stack voltage but can be optimized for a wide range of phase voltages, which helps with physical design considerations such as winding turns of the PMSM. The battery voltage used in the experiment can vary between 235V to 350V while the maximum DC-Link voltage output by the DC/DC converter is set to 600V [13], which relaxes the design requirements on the motor windings from a stringent range of around 115V to over 300V. A high DC-Link voltage compared to the battery voltage is preferred to limit the switching losses within the inverter but at the same time, too high a value may result in additional core losses in the motor and this is where a good compromise between inverter switching losses and machine core losses has to be established when deciding upon the optimum DC-Link voltage.

Schoenen et al [13], further develop a control strategy to ensure the best DC-Link voltage for various operating points of the motor. The control strategy employs two different control schemes for the inverter stage, one for low voltage or low speed operation of the motor, also termed the Maximum Torque per Ampere method, and one for high speed operation of the motor, called the Field Weakening method. The control of the DC/DC converter follows traditional cascaded control design wherein the inner loop of the cascaded control regulates the input inductor current while the outer loop regulates the DC-Link voltage. It is shown through experimental results that as far as the system efficiency is concerned, which includes both the inverter and the motor, for lower speeds, a lower DC-

Link voltage is required. For higher speeds, when the DC-Link voltage is not sufficient enough to meet the line-line voltage requirement at the PMSM machine, field weakening regimes have to be employed which cause additional losses in the motor windings, thus affecting overall system efficiency. The case for lower DC-Link voltages for lower speeds of the machine can be made through the following tabulated results.

Table 2.1: Motor and inverter efficiencies through reduced DC-Link [13]

Low Speed Efficiency	**DC-Link Voltage**		
	400V	300V	200V
PMSM	95.8%	96.1%	96.9%
Inverter	86.3%	86.9%	87.4%

In [14], Prabhakar et al have endeavored to establish a direct comparison between drivetrain topologies with and without the additional DC/DC converter in place. One of the tested topologies, therefore only has a fixed DC-Link voltage and so provides a case study for efficiency comparisons between the two approaches. The topology referred to as P2 in the paper has an additional DC/DC converter realized using a Cuk converter while the topology referred to as P1 is the conventional state of the art with an inverter connected immediately after the battery stack voltage and therefore a fixed, battery voltage dictated DC-Link. It is shown through the experimental setup, as in [13], that the topology that is augmented by an additional DC/DC converter can produce higher efficiency numbers, both for low speed and high speed operations of the motor. This is achieved simply by matching the DC-Link voltage to the line to line voltage requirement of the motor for a given speed. The closer the DC-Link voltage is to this value, the higher the inverter and overall system efficiency. The calculation of the required DC-Link voltage is given by the following

equations. Here the parameters used are synchronous speed (w_s) in rad/s, machine poles (p), stator flux linkage (ϕ_s) and a marginal voltage value (V_m) which adapts the PMSM motor voltage for an inductor motor, which is the kind of machine used to setup the experiment in [14].

$$V_{DC} = \sqrt{3}(\omega_s p \varphi_s + V_m) \quad (2.1)$$

$$V_m = I_s R_s \quad (2.2)$$

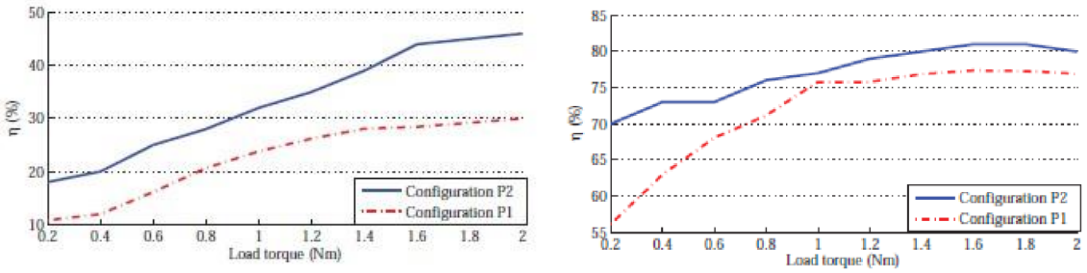
The induction motor used has a rating of 1.1kw and the specifications of the CUK converter used are given in table 2.2. it may be noted here that for interleaved topologies a more suitable DC/DC converter is one with lower component count, specially when implementing ZVS through an additional ZVT branch. This will help explain the approach taken while designing the converter proposed in this work.

Table 2.2: Cuk converter design specifications [14]

Parameters	**Value**
Switching Frequency	50kHz
Inductor (L_1)	1mH
Inductor (L_2)	1mH
Coupling capacitor (C_1)	0.6
Output filter capacitor (C_2)	8μF

Configuration P2 is shown to produce significantly better efficiency results than configuration P1. This is primarily due to the reduction of losses in the inverter stage through a minimization of switching and conduction losses in the IGBTs used. Two separate cases are shown to illustrate this improvement in efficiency. The first one, as

shown in the following figure, is at a lower speed of 250rpm. Here the efficiency improvement is drastic even when the overall system efficiency remains very low. For a load torque of 2Nm, the system demonstrates an efficiency improvement from around 30% to 45% just by having a variable DC Link. Even when the speed is increased and the overall system efficiencies increase for the case without the DC/DC converter, having the DC/DC converter further improves the situation as can be seen in figure 2.2 as well. Here, the maximum efficiency improvement is from around 60% to 75%, again a sizable improvement. The trend is expected to continue and system efficiencies continue to improve for higher speeds as the power delivered becomes more dominant with respect to the losses in the system and therefore for more realistic operating points of actual motors, in terms of speeds and torque, system efficiencies beyond 95% are expected and documented in various works of literature.



(a) (b)

Figure 2.1: System efficiency comparisons with and without DC/DC converter: (a) 250RPM (b) 2500RPM [14]

Efficiency improvement due to a variable DC-Link is obviously the prime advantage of having a DC/DC converter but there are other advantages derived from the this additional

component as well. These have been explored in [15], by Tenner et al. The DC/DC converter imparts flexibility onto the entire drivetrain wherein the a motor rated at a much higher voltage can be powered through a battery that outputs a much smaller voltage. This helps ensuring that much fewer series connected battery cells are used in the power train, which helps reduce the size and weight of the overall system, which in turn helps with the efficiency of the system in an indirect way as well. In [15] an algorithm is proposed to calculate the optimum d- and q-axis currents for the motor and an optimum line to line voltage as well, for each operating point of the motor. This helps decide upon an optimum DC-Link voltage for a given speed and torque condition of the motor.

When a high enough battery voltage is supplied to the motor through an inverter to ensure rated speed operation does not require any field weakening regimes to be followed, the voltage stress on the entire system, including the inverter and the motor is excessively large for most of the operating region. This incurs greater losses in the inverter stage and the motor itself. One solution is the state of the art today, to use a low battery output voltage and then to perform field weakening for higher speeds by injecting negative d-axis currents in the motor winding to enable high speed operation. The other, and more efficient, approach is to use a DC/DC converter in between the battery output and the inverter input. The DC/DC converter ensures that voltage stress on the system is reduced and that high speed operation is made possible without having to resort to field weakening schemes.

The authors in [15] have used the monte carlo algorithm to devise and solve a minimization optimization problem for the d- and q-axis motor currents depending upon the speed, torque and battery output voltage. This effort ensures that the current reference

and actual values for the motor are kept to a minimum for each operating point and thus incurs the least amount of losses in the motor windings. The following figures shows a comparison of a drivetrain with and without a DC/DC converter and the current reference generator methodology for the motor.

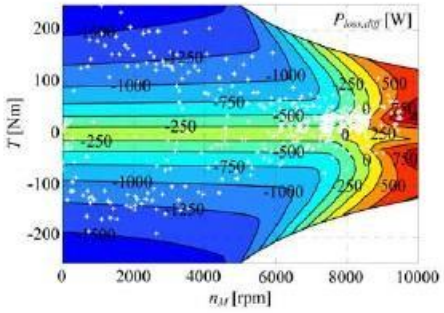


Figure 2.2: Loss difference between a system with and without DC/DC converter [15]

The efficiency improvement at lower speeds is much better for the case provided in [15] than at higher speeds. This is because a battery voltage of 300V is used and this has to be boosted to a higher value for high speed operations. Having to boost 300V to a higher DC-Link voltage incurs additions switching losses in the DC/DC converter and therefore undermines the efficiency numbers provided in [15]. However, these numbers can be significantly improved by incorporating soft switching techniques within the DC/DC converter to limit and minimize the switching losses therein. This is in fact, one of the major contributions of this thesis and will be detailed later in the report.

In [16] the authors have proposed a control strategy for a DC/DC converter in an EV drivetrain. This control strategy is different from the one implemented in [15] as it does not need to determine the mode of operation of the EV, whether motoring or regenerative, to

generate reference values of inductor current and DC-Link voltage for the DC/DC converter. The following figure shows a block diagram representation of the control scheme.

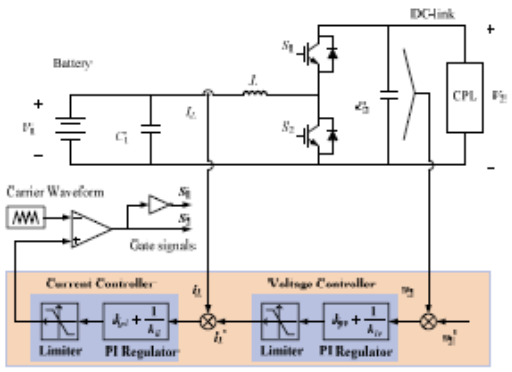


Figure 2.3: Proposed Control Scheme by Jia et al [16]

This control strategy is promoted as a better solution for EVs operating in and switching back and forth between motoring and regenerative modes of operation. The only drawback, as depicted in [16] is a slight fluctuation in the DC-Link output when a transition from one mode to the other takes place. However, since this fluctuation is small and occurs only during a period of a few milliseconds, it can be deemed innocuous enough to push for the viability of this control scheme. As a whole, the control is simple, as it employs to PI controllers, one each for the inner, inductor current control loop, and the outer, DC-Link voltage control loop.

In [7], Lemmens et al have taken a different approach towards showing the advantages related to have a variable DC-Link. They argue that since the voltage is adaptable, it can be used to help reduce the voltage stress on the switches in the inverter and can therefore

help increase the thermal reliability and durability of the switches. This causes fewer failures within the power electronic modules and can contribute towards decreasing upkeep cost of the components. A control strategy is employed in the paper referenced that helps maximize torque output of the machine while taking into consideration constraints that relate to thermal management of the switches in the inverter.

Thermal management of devices is important, specially in urban traffic when EVs are operated at low speeds and high torques. In such cases modulation frequency for equal torque outputs is reduced and power cycling becomes more frequent. Since this happens over a prolonged period of time, essentially for just as long as the vehicle remains in congested urban traffic, it puts thermal stress on the power electronic switches in the inverter. The switches themselves have a large chip surface and therefore a low junction to case thermal resistance but the body diodes of these switches can be undersized and may undergo a rapid increase in temperature at low speed and high torque operation. Since, in such a condition, the diodes are under greater stress as they conduct most of the DC phase current, they become susceptible to failure under thermal stress. A couple methods can be employed to remedy this situation. In either case, a limit on the current in the motor controller is set. This limit can either be static or dynamic. The dynamic approach, wherein the temperature of the switches and the diodes is read and then used to determine a suitable current limit is the preferred method, as it will not lead to a static limit on torque for all operating scenarios.

2.3 Optimization of Battery Stack Voltage

It is important to regulate the output of the battery stack in order to ensure a stable voltage at the input of the inverter stage. It is shown through the work carried out in [17] that for the US06 driving cycle and for a distance of around 50 miles, the battery voltage can decrease to just over 60% of its original value. This can be seen Figure 2.5.

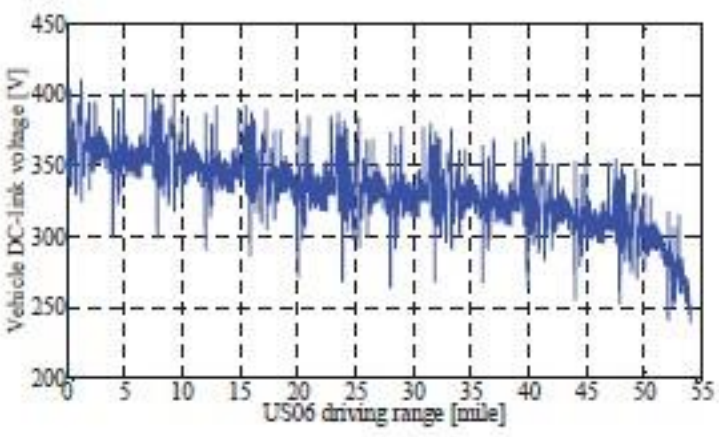


Figure 2.4: Battery Voltage trend for US06 drive cycle [17]

Figure 2.5, given below, shows how the field weakening capability of a machine is limited at low voltages when the motor has to be operated at speeds as high as 10000RPM. Since field weakening can not be resorted to, to increase motor speed at voltages as low as 240V at the DC-Link, it becomes essential to have a DC/DC converter in place to boost the DC-Link voltage to the required value to satisfy the requirement of a line-line voltage for a given motor speed. This way, the field weakening regime is circumvented, phase current magnitudes do not have to be controlled solely to increase motor speed and therefore motor

losses are minimized. It makes for a much more efficient approach to high speed operation when the battery stack voltage has reduced beyond a certain point due to distance travelled.

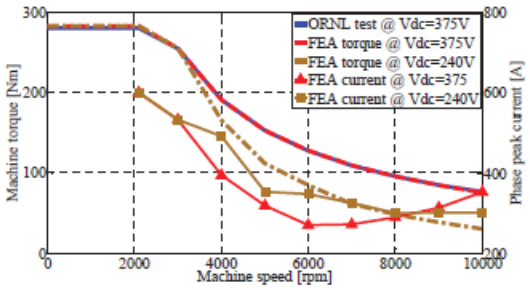


Figure 2.5: Machine Torque and Power against an adjustment in Phase Current [17]

Selecting the optimum battery stack voltage for a particular motor is very important when it comes to efficiency numbers as well. A lower battery stack voltage would mean that the drivetrain can give a higher efficiency at lower speeds when the output voltage of the battery matches the voltage requirement at the input of the motor. However, a higher battery stack voltage would mean that the same system can be operated at higher speeds for better efficiencies than at lower speeds. The other factors to consider when this selection is made is whether the drivetrain topology will have a DC/DC converter or not. Intuitively, having a DC/DC converter in both cases will help improve the system efficiency, essentially by making the output of the battery voltage adaptable. However, in the case when the battery voltage is low, the DC/DC converter can be realized with a simple boost topology that has low component count, easy control and is only required to boost the output voltage of the battery. In the case when the battery voltage is high, a more complicated topology will have to be employed to both boost and buck the output of the battery. Such topologies have higher component count, more passive components and more

complicated control. These factors will lead to lower system efficiencies and therefore the former approach is actually employed in the experimental and simulation set up of this report.

As detailed in [18], using a bi-directional DC-DC converter helps reduce system losses by independently using an optimal battery stack voltage as well as allowing for the input voltage at the inverter stage to be adjusted according to the operating point of the motor. The operating point of the motor is given by the speed and torque of operation, but in terms of selecting the inverter stage input, the back EMF generated by the motor is a good indicator. It is concluded in [18] that the DC-Link voltage has to be proportional to the back-emf generated by the motor to ensure that field weakening is not necessitated at higher speeds. The figure shown below, depicts how the system voltage and the speed of the motor are related, both in the constant torque and constant power regions.

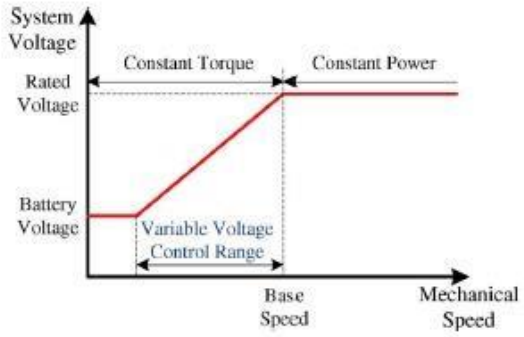


Figure 2.6: Required System Voltage vs Motor operating speed [18]

Figure 2.7, shown above, gives good insight into developing a relationship between the motor speed and the DC-Link voltage and indeed, helps in control design on the same. For lower speeds, the battery stack voltage is sufficient to drive the motor and so the DC/DC converter is not required to boost its input to higher output value. Beyond certain speed and while remaining in the constant torque region, however, the DC/DC converter is required to output a higher voltage that linearly increases with speed. This is done to maintain the value of torque while going to a higher value of speed. When the base speed of the machine is reached, the machine enters the constant power region of operation and here no further increase is system voltage is required as it is at its rated value.

System efficiency can be further improved if the motor load condition, and thereby the modulation index required within the inverter stage control to output the required line to line voltage, is used to determine the appropriate DC-Link voltage to be output by the DC/DC converter stage. This method regulates the DC-Link voltage so as to maintain the modulation index for the inverter stage at a predetermined reference value, [18]. This helps reduce voltage stress on the inverter, and by employing a high frequency ZVT converter for the DC/DC stage, system efficiency can be drastically improved. Furthermore, the entire system voltage is dependent on the dynamic operating load condition of the motor and therefore provides for a more uniform control scheme across all the components in the EV drivetrain.

In selecting a battery stack voltage for a given machine, a number of factor need to be considered when a DC/DC converter is not present. These include the driving profile of the vehicle and the machine's torque-speed characteristics. These factors have to be correlated

to the required line to line voltage required for carious operating points of the machine and then a suitable battery stack voltage opted for, one that ensures that the machine can operate throughout the entire range of its speed-torque capability. Figure 2.8, which is reprinted from [15], gives a relationship between the line to line voltages and the speed of a given IPMSM for a fixed DC-Link or battery output voltage of 400V. The battery voltage in this case has to be kept at a considerably high value to ensure that the line to line voltage requirement for all motor operating points is satisfied. Having a DC/DC converter in place can significantly reduce this requirement on the battery stack and therefore a battery voltage of 300V is chosen for the purposes of this project.

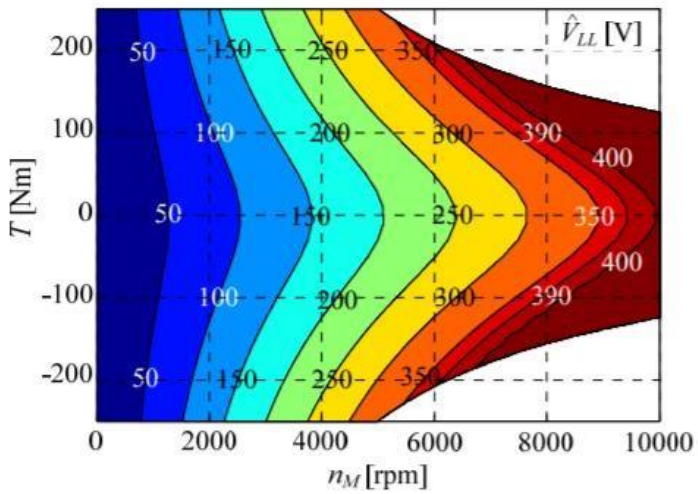


Figure 2.7: Optimal V_{LL} for IPMSM with fixed V_{Bat} = 400V [15]

The lower voltage is primarily selected to lower the voltage stress on the system when it is being operated at lower speeds and therefore reduce the losses in the system. Figure 2.9 is a good reference when it comes to deciding upon a battery voltage. It shows how most urban driving cycles fall within the 0-4000rpm range, which is considered a low

speed region of operation. Again, the correlation between speed and line to line voltage is made, and if the control scheme for system voltage proposed in [18], is to be used, then a battery and DC-Link voltage conforming to the low line to line voltage requirement has to be used. [15] shows that the optimum battery stack voltage for the US06 driving cycle is 300V. An even lower battery stack voltage is proposed for the NEDC and FTP-75 urban driving cycles. This voltage is set at 125V and a DC/DC converter is used in the topology to boost the DC-Link voltage. Under these test conditions, efficiency improvements of around 17% and 13%, respectively have been achieved.

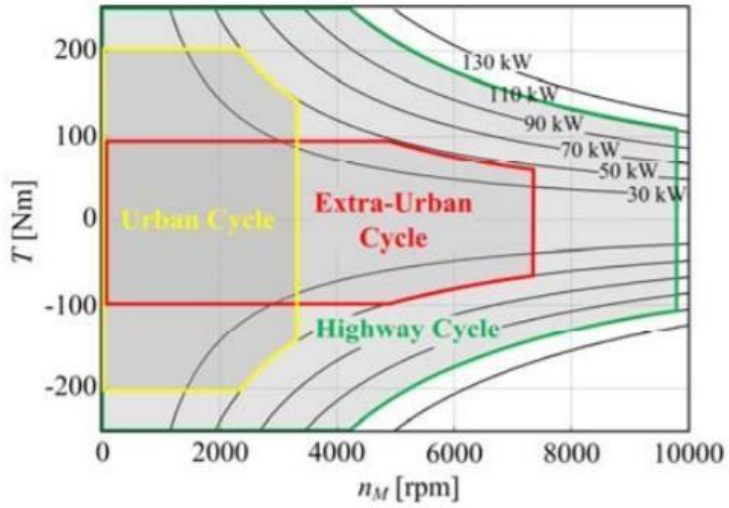


Figure 2.8: Driving cycle operating points [15]

2.4 Impact on Inverter Efficiency

The inverter has to be designed for high efficiency, both in terms of minimizing switching losses and maximizing thermal durability. The inverter stage couple the DC-Link voltage to the traction device and enables both the motoring mode of operation and the regenerative braking mode of operation where the energy from the freewheeling motor is

fed back into the battery stack for runtime charging and energy conservation purposes. Having a DC/DC converter in place helps optimize the design of the inverter as stringent constraints of a fixed range of battery stack voltages do not have to be imposed on the inverter design.

The inverter design essentially consists of the appropriate switch rating selection for the given input and output conditions. Most of these switches are IGBT devices with antiparallel diodes and design considerations have to take into account factor such as on-state resistance of the device, thermal conduction, frequency of operation etc. All these factors play a significant role in determining the efficiency of the inverter stage as there are two major contributors towards losses within the inverter, one is the switching losses in the IGBTs and the other is the conduction losses in both the IGBT switches and the antiparallel diodes, [19]. Each device's dynamic characters are also very important as device behavior in terms of thermal conduction and on-state resistance is expected to change for higher currents and essentially higher temperatures.

The modelling of the inverter losses is thus essential to the primary work of this thesis, which is to design a ZVT DC/DC converter for the EV drivetrain. The impact of the DC/DC converter can, however, only be measured through a systemic reduction of losses and for that purpose the impact has to be quantified on the inverter stage as well. The inverter model used is one derived from the Oak Ridge National Laboratory's Annual Merit Review of 2013, [20]. Here, the inverter used in a Nissan Leaf drivetrain is a simple 3-pole converter with 2 IGBTs and 2 Diodes for each phase. It takes its voltage input directly from

the battery stack and outputs a 3-phase AC voltage at the IPMSM motor. For our analysis, the only difference is going to be a variable input voltage at the inverter stage.

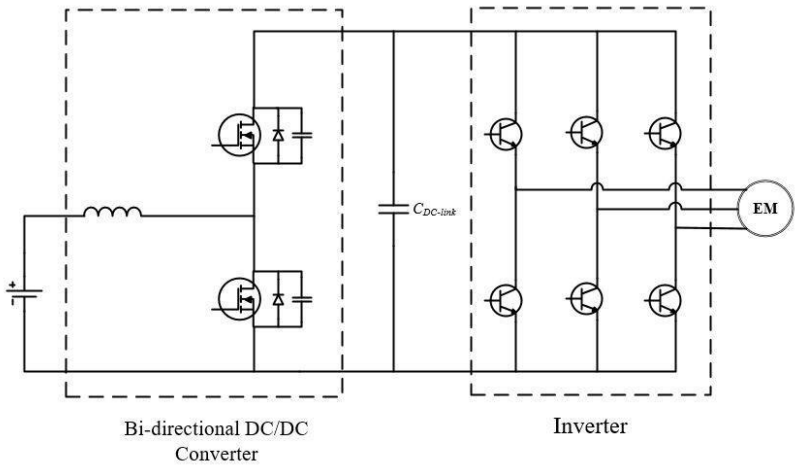


Figure 2.9: EV drivetrain schematic with the addition of a DC/DC converter

The calculation steps detailed below for the inverter switching and conduction losses assume that sine wave PWM technique is used as the modulation technique. In this technique, a line frequency sin wave is compared with a triangular wave at a much higher frequency (5khz). The output of the comparison is fed into a gate driver circuit for a given switch and the complimentary signal is fed into the gate driver circuit for the other switch of the same leg. Equations 2.3 and 2.4 give the phase current for the motor and the duty cycle. The modulation index, m_a varies between 0 and 1 and the phase current in the motor lags the phase voltage by the angle ϕ.

$$I_\phi = I_{\phi,pk} \sin(\theta) \tag{2.3}$$

$$d(\theta) = \frac{1}{2}[1 + m_a sin(\theta + \phi)] \tag{2.4}$$

Conduction losses:

The conduction losses ($P_{cond,inv}$) for the IGBT (P_{CT}) and the diode (P_{CD}) are given by the following equations:

$$P_{CT} = u_{CE0} I_0 \left(\frac{1}{2\pi} + \frac{m_a \cos(\phi)}{8} \right) + r_C I_0^2 \left(\frac{1}{8} + \frac{m_a \cos(\phi)}{3\pi} \right) \quad (2.5)$$

$$P_{CD} = u_{D0} I_0 \left(\frac{1}{2\pi} - \frac{m_a \cos(\phi)}{8} \right) + r_D I_0^2 \left(\frac{1}{8} - \frac{m_a \cos(\phi)}{3\pi} \right) \quad (2.6)$$

$$P_{cond,inv} = P_{CT} + P_{CD} \quad (2.7)$$

u_{CE0} (V): IGBT collector-emitter forward voltage
I_0 (A): Peak amplitude of sinusoidal current
m_a: Amplitude modulation ratio
ϕ (rad): Phase shift angle between the sinusoidal current and voltage
r_C (Ω): IGBT on-state resistance
u_{D0} (V): Diode forward voltage drop
r_D (Ω): Diode on-state resistance

Switching Losses:

The switching losses ($P_{sw,inv}$) for the IGBT ~~during turn-on~~ ($P_{sw,on}$), turn-off ($P_{sw,off}$), and reverse recovery for the anti-parallel diode (P_{rec}) are given by:

$$P_{sw,on} = \frac{1}{2} E_{on} \frac{V_{dc}}{V_{nom}} f_{sw} \quad (2.8)$$

$$P_{sw,off} = \frac{1}{2} E_{off} \frac{V_{dc}}{V_{nom}} f_{sw} \quad (2.9)$$

$$P_{rec} = \frac{1}{2} E_{rec} \frac{V_{dc}}{V_{nom}} f_{sw} \quad (2.10)$$

$$P_{sw,inv} = P_{sw,on} + P_{sw,off} + P_{rec} \quad (2.11)$$

$E_{on}\ (J)$: IGBT on-switching losses at nominal voltage and rated current
$V_{dc}\ (V)$: DC-link voltage
$V_{nom}\ (V)$: Nominal voltage at which E_{on} is defined
$f_{sw}\ (Hz)$: Switching frequency
$E_{off}\ (J)$: IGBT off-switching losses at nominal voltage and rated current
$E_{rec}\ (J)$: Reverse recover energy for diode

Total Inverter Losses:

$$P_{total,inv} = 6(P_{cond,inv} + P_{sw,inv}) \tag{2.12}$$

The calculation of the inverter losses is made for an IGBT module from Infineon (FS820R08A6P2B). When selecting this module it was ensured that the current and voltage ratings of the Nissan Leaf motor were exceeded by the ratings of the selected device. The Nissan Leaf Motor is rated for a peak current of 615A and the current rating of the device used is 820A. The loss analysis is carried out for a number of different speeds of the motor, both in the constant torque region and the constant power region of operation. The speed is varied by inputting a different line to line voltage at the input of the motor. This is done through a different modulation index for each speed as the modulation index defines the relationship between the input DC-Link voltage at the inverter and the output line to line voltage from the inverter. To enable high speed operation without entering field weakening, it is ensured that the DC-Link voltage at the input of the inverter is always high enough to avoid over modulation in the inverter.

The resulting surface plot is shown in Figure 2.11 that plots the total semiconductor losses in the inverter for the given parameters and in the constant torque region.

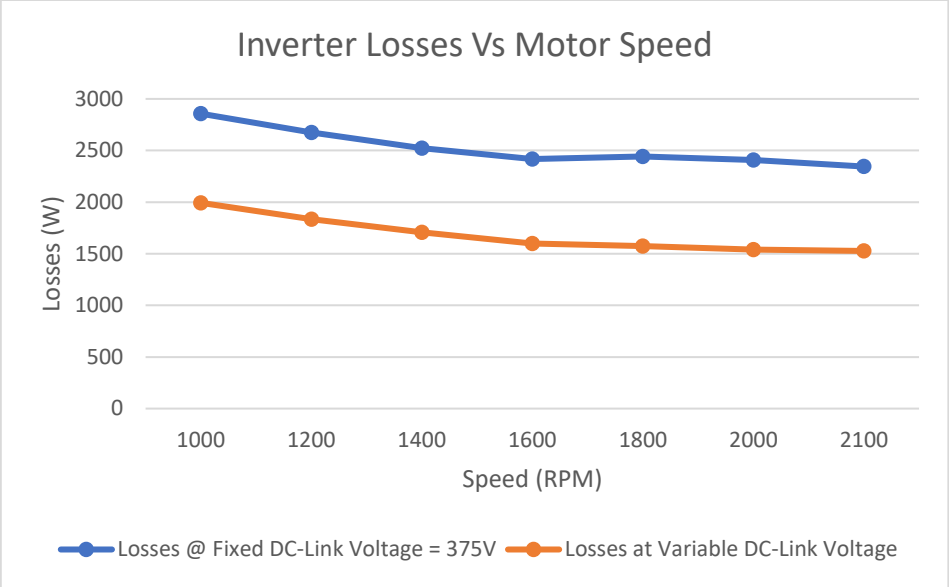


Figure 2.10: Total semiconductor losses for varying speed and DC-Link voltage in CT region

Table 2.3: Inverter loss comparison at fixed Vdc = 375V and Vdc=Vbat

Speed (RPM)	$V_{l-l,pk}$ (V)	Ploss @ Vdc = 375V (W) (Eff%)	Ploss @ variable DC-Link in W	Eff. At variable DC-Link (%)
1000	122.13	2857 (96.4)	1993 @ 200V	97.5
1200	132.49	2676 (96.6)	1836 @ 200V	97.7
1400	142.85	2524 (96.8)	1707 @ 200V	97.8
1600	153.21	2416 (96.9)	1599 @ 200V	98.0
1800	163.57	2441 (96.9)	1574 @ 200V	98.0
2000	173.93	2407 (97.0)	1540 @ 200V	98.1
2100	179.11	2345 (97.1)	1527 @ 200V	98.1

At lower speeds, as concluded before, it is beneficial to have a lower DC-Link voltage. This is why the battery voltage of 300V incurs lesser losses and results in higher efficiencies when compared to a Dc-Link voltage of 375V. The motor operation requirements for

speeds in the 3000 to 10000 RPM range fall into Constant Power region. The line-to-line voltages corresponding to different speeds in this regime are summarized in Table 2.4, along with the losses calculated for constant and variable DC-link voltages. The resultant losses are plotted in Figure 2.12, using the same Infineon FS820R08A6P2B IGBT module. As the speed increases beyond 5000 RPM, the required motor voltage increases beyond the supply capability of 375Vdc.

Field weakening regime is employed in DC/DC converter-less topologies to drive the Nissan Leaf motor, with the given inverter specs, above a speed of 6000rpm. This entails injection of negative d-axis currents into the motor windings and accounts for higher copper losses therein. To avoid this, the DC/DC converter is used to increase the Dc-Link voltage to a point where the inverter can carry out the required modulation keeping the modulation index between 0 and 1 and provide the necessary line to line voltage at the motor.

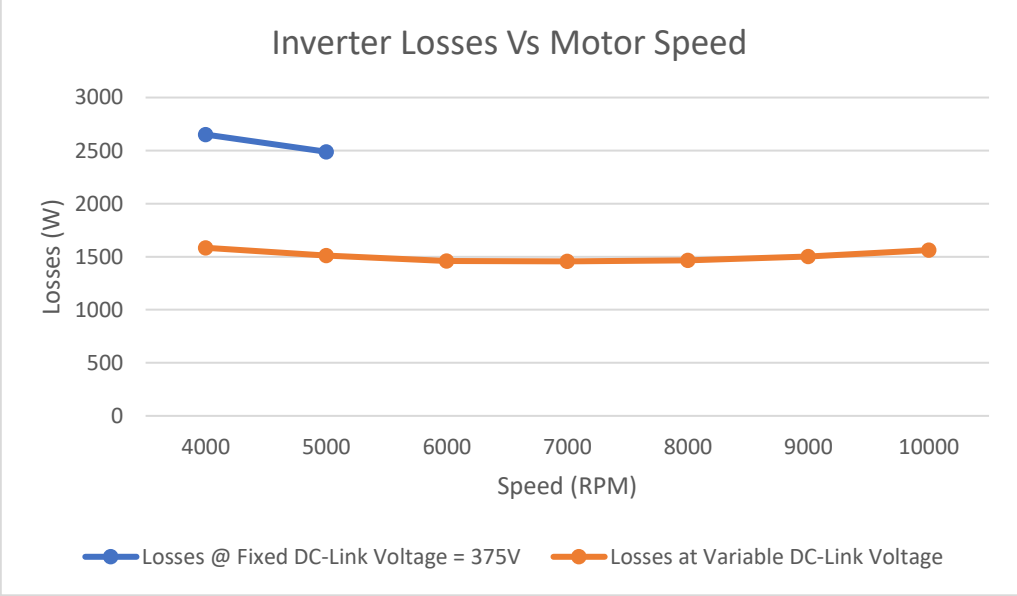


Figure 2.11: Total inverter losses for varying speeds and DC-Link voltages in Constant Power Region

Table 2.4: Inverter loss comparison at fixed Vdc = 375V and Variable Vdc

Speed (RPM)	$V_{l-l,pk}$ (V)	Ploss @ Vdc = 375V in W (Eff %)	Ploss @ variable DC-link in W	Eff. at Variable DC-link (%)
4000	288.057	2651 (96.79)	1584 @300V	98.10
5000	333.506	2489 (96.98)	1510 @335V	98.15
6000	377.691	FW*	1460 @380V	98.20
7000	427.851	FW*	1456 @430V	98.21
8000	426.137	FW*	1466 @430V	98.20
9000	444.427	FW*	1502 @445V	98.15
10000	469.403	FW*	1563 @470V	98.08

2.5 Review of Field Weakening and Impact on Motor

Optimization of the motor losses is another important benefit of incorporating a DC/DC converter in the EV drivetrain. We have touched upon the concept of field weakening but here we look at the motor efficiency numbers associated with employing a variable DC-Link as opposed to going with the aforementioned concept. To do this, first we need to establish a basic understanding of the working of a PMSM machine.

In a PMSM machine, there are two fields that act upon the rotor of the machine. One is fixed, and is produced by the permanent magnets on the rotor. The other field is induced onto the rotor by virtue of the currents flowing through the stator, once the stator is excited. The currents causing this field are direct axis currents that are injected into the stator. The excitation of the stator induces a field onto the rotor, the strength of which is directly proportional to the winding turns of the rotor, the strength or speed of rotation of the stator field and the currents flowing in the stator winding. As magnetic induction follows Lenz's law when it comes to the direction of induced EMFs and induced currents, there is a back EMF that is propagated to the stator by the rotor induction. This back EMF gets higher with increasing speed and at a given point is high enough that a constant voltage input at the stator will result in no further increase in speed of the rotor. At this point, one of two methods need to be employed to the increase the speed of the motor. The first, which is something that is targeted by the work carried out, is increasing the input voltage at the motor by increasing the DC Link voltage through a DC/DC converter. The other, and more lossy approach, is the field weakening method. What happens in the field weakening

method is that negative d-axis currents are fed into the stator winding. This weakens the field induced in the rotor windings and the back emf generated by the rotor field through the stator is reduced. Once this happens, the rotor currents increase and then lead to the rotor speeding up. This however incurs greater losses in the rotor as more current is made to flow through it to achieve the higher speed operation.

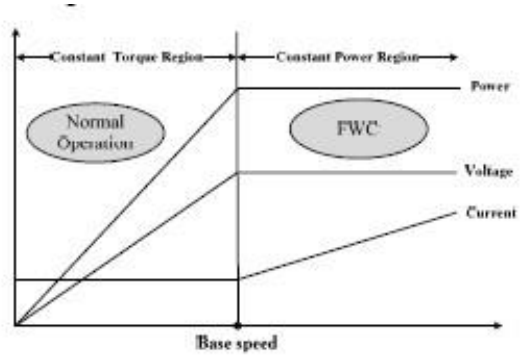


Figure 2.12: Motor parameters in relation with increasing speed [22]

Figure 2.10 shows how and when the field weakening regime needs to be applied. The first section of the figure is the constant torque region. Here the motor voltage is increased to increase the motor speed and in turn the motor power surges as well. Constant torque is maintained and that is why the current remains constant. After the base speed of the motor is reached, however, the voltage supplied at the motor can not be increased further because of the limitation imposed by the battery stack voltage. Beyond this point the current in the rotor is increased through the field weakening method explained above and this causes the motor speed to increase while not maintaining a constant torque, as it depends upon the motor current. This incurs additional losses which can be saved on if a DC/DC converter is used in the drivetrain. It is shown in [22], that having a variable DC-Link and the

capability to extract higher speeds from the motor through higher DC-Link voltage can actually increase motor efficiencies from 55.13% to 78.46% at 4000 RPM and 42.2% to 79.15% at 5000 RPM. This is an extremely significant improvement and justifies the motivation behind this project. These results have been tabulated in table

Table 2.4: Losses in FW mode vs DC/DC Converter [22]

RPM	Field Weakening Technique			DC/DC Converter		
	P_{in} (kw)	P_{out} (kw)	Eff. (%)	P_{in} (kw)	P_{out} (kw)	Eff. (%)
3000	2.04	1.577	77.3	2.05	1.577	77
4000	3.8	2.095	55.13	2.67	2.095	78.46
5000	6.2	2.62	42.2	3.31	2.62	79.15

Chapter 3

INERLEAVED SYNCHRONOUS BOOST DC/DC CONVERTER WITH ZVT FOR AUTOMOTIVE APPLICATIONS

3.1 Introduction

The implemented converters, both for the first and second phase of the project are explained in detail in this chapter. In phase one of the project, the proposal was for a single phase low power prototype that would couple a 200V-300V battery stack voltage to a DC-Link of a maximum of 800V. This converter is a synchronous boost topology with bidirectional power flow capability and a ZVT branch that ensures zero voltage switching for the main and the synchronous switches, depending on the mode of operation. This mode of operation can either be the motoring mode or the regenerative mode. The converter show in figure 3.1 was designed and implemented for the first phase of the project. Here, we have the two basic switches S_1 and S_2 in the boost topology as well as the two auxiliary switches S_{aux1} and S_{aux2} for the ZVT branch. The other components include the main power circuit inductor L_1 and the output or DC-Link capacity C_1. To ensure that the ZVT circuit resonates with the main circuit capacitance, dentoted by C_{eq}, which is the parallel combination of the C_{DS} across the two main switches, we have the auxiliary inductor, labelled L_{aux1}, [24]-[27].

Figure 3.2 shows the same topology, however the output capacitance and load have been modelled as an ideal DC voltage source for the purposes of simplicity of analysis. This voltage is input at the inverter stage before being converted to 3-phase output voltage for the motor, which can either be an IPMSM or an induction motor. In keeping with the

fundamental motivation for the project, Silicon Carbide (SiC) devices have been used for all the switches since they support higher frequencies, higher power densities, high thermal conduction and therefore better efficiencies. Reverse recovery times of the body diodes contribute to losses as well and therefore they have been augmented with fast acting SiC Schottky diodes in parallel with the switches to reduce reverse recovery losses.

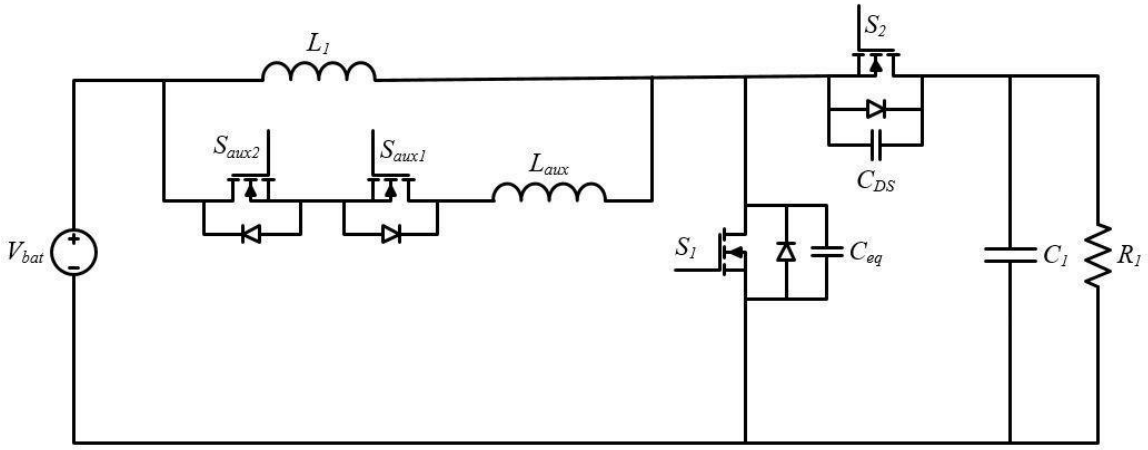


Figure 3.1: Implemented circuit for Gen-I

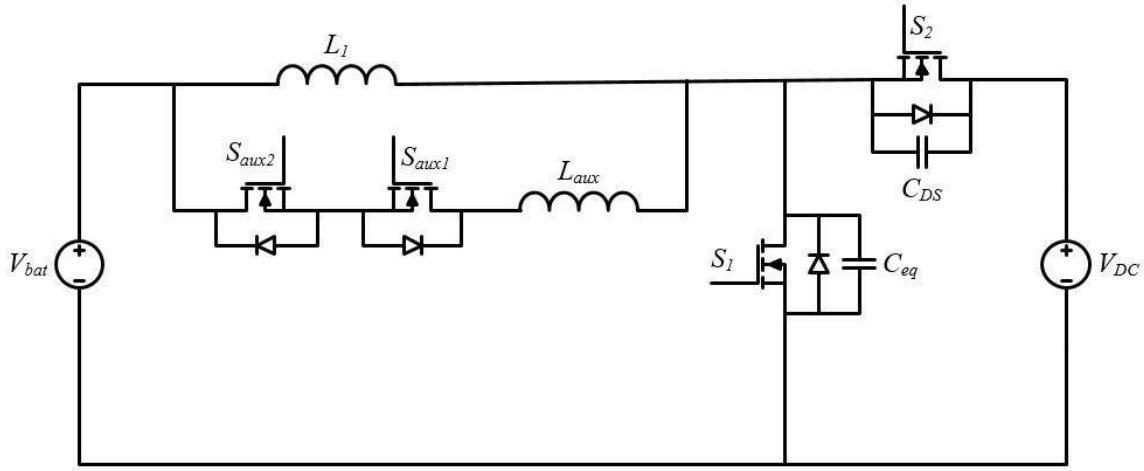


Figure 3.2: Equivalent circuit schematic for Gen-I

The converter designed for phase two of the project, and the main focus of the work is essentially an interleaved synchronous boost converter with an independent ZVT branch for each interleaved

stage. It was an extension of the phase-I design wherein three equivalent modules were interleaved to achieve a higher total output power rating. Figure 3.3 shows the interleaved topology and the ZVT branch for each interleaved stage.

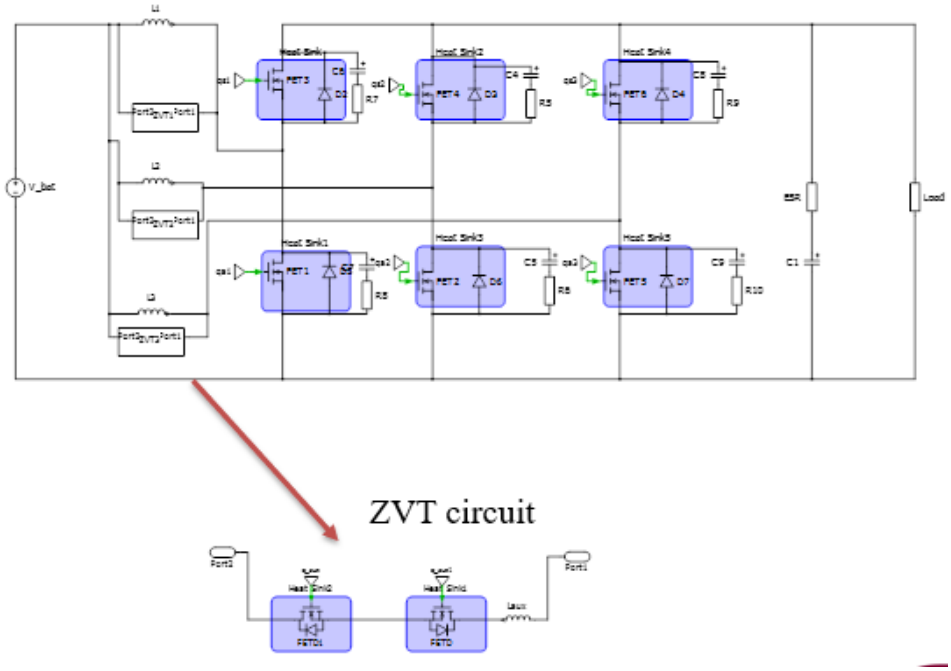


Figure 3.3: Complete schematic for Gen-II

3.2 Explanation of Operating Principles

This section elaborately deal with the operation of the converter under the boost mode of operation, clearly detailing the conduction path during each switching interval and explaining how zero voltage switching actually takes place for the main switch. The buck mode is the dual of the operation explain in the following section. For the sake of simplicity, idea components are assumed as far as the operation cycles are considered and it is assumed

that all transients have decayed. The related waveforms are provided after the explanations in Figures 3.4 and 3.5 and the conduction paths for a single phase module have been shown in Figure 3.6

The explanation for each of the eight subintervals within one complete switching cycle is as follows:

Interval 1 ($t_0 - t_1$):

The first interval is assigned to the time period when the synchronous switch alone is conducting. This is the off interval of the conventional boost converter and the stored main inductor energy is being supplied to the load. The main switch S_1 is off, as are both the auxiliary switches too. There is blocking voltage equal to $V_{DC} - V_{bat}$ across S_{aux1} and zero voltage across S_{aux2}. Since both the auxiliary switches are off, the auxiliary branch does not conduct.

Interval 2 ($t_1 - t_2$):

While the states of all the other switches from interval 1 remain the same, the switch S_{aux1} is turned on to divert the synchronous switch current through the auxiliary branch. The conduction path in the auxiliary circuit is through S_{aux1} and the body diode of S_{aux2}. The auxiliary inductor is charged during this time by a voltage of $V_{DC} - V_{bat}$. The current in the auxiliary branch is given by the following equation that defines the current through the auxiliary inductor.

$$i_{Laux}(t) = \frac{V_{DC} - V_{bat}}{L_{aux}} \cdot (t - t_1) \tag{3.1}$$

As the increase in the current in the auxiliary branch is a result of the diversion of the synchronous current, the decrease in the synchronous switch current is given by.

$$i_{S2}(t) = I_L - \frac{V_{DC}-V_{bat}}{L_{aux}} \cdot (t - t_1) \tag{3.2}$$

Interval 3 ($t_2 - t_3$):

During this interval, it is made sure that the synchronous switch turn off timing is optimized to incur the least switching turn off loss in S_2. This instant is determined to be short after the auxiliary branch current has equaled the main inductor instantaneous current. Once the value of the current in the auxiliary branch exceeds the value of the current in the main inductor, resonance between the equivalent power pole capacitance, C_{eq}, and the auxiliary inductor, L_{aux}, takes place. The mathematical formulae for the current $i_{Laux}(t)$ and $V_{s1}(t)$ are provided below.

$$i_{Laux}(t) = I_L + \frac{(V_{DC}-V_{bat})\cdot \sin(\omega t)}{Z} \tag{3.3}$$

$$v_{S1}(t) = V_{DC} + (V_{DC} - V_{bat}) \cdot \cos(\omega t) \tag{3.4}$$

Interval 4 $(\boldsymbol{t_3 - t_4})$:

As resonance between C_{eq} and L_{aux} occurs, the capacitance across the main switch S_1 discharges through the inductor in the auxiliary circuit. As there is no charge in the capacitance across the main switch at time t_3, the voltage across the switch has dropped to zero and this is when the gate pulse for the main switch can be triggered to ensure that it turns on as the voltage across it is zero. The current that recharges the capacitor is given by the current difference between the main inductor current and the auxiliary inductor current. The main switch should be turned on before this current takes on a positive value and recharges the capacitance at C_{eq}. .

Interval 5 $(\boldsymbol{t_4 - t_5})$:

This interval is importance with respect to the zero current switching of the auxiliary circuit. Once the main switch has been turned on in the previous interval, the auxiliary current starts decreasing as it is now diverted through the main switch. When the auxiliary current reaches zero, that is when the auxiliary switch is turned off to ensure no losses take place in the auxiliary branch. This instant occurs at t_5.

Interval 6 $(\boldsymbol{t_5 - t_6})$:

At t_5, the auxiliary switch is turned off and conventional boost operation is resumed with the main switch S_1 now conducting. The main inductor begins to charge up again and the output capacitance or the DC-Link capacitance discharges through the load.

Interval 7 ($\boldsymbol{t_6 - t_7}$):

This interval is when the main switch goes through its turn off transition as the gate drive is now removed. The switch capacitance ensures that the current through the switch drops linearly as there is a build up of voltage in the capacitance and therefore across the switch. This scheme incurs switch off losses in the switch, however, these losses can be minimized by having a large capacitance across the drain and source of the switch to ensure that the voltage build up is slow.

Interval 8 ($\boldsymbol{t_7 - t_8}$):

With the main switch now off, it blocks the full output voltage across its drain and source terminals which means that the potential difference across the source and drain terminals of the synchronous switch at this point is zero. This is when the synchronous switch is turned on during a natural zero voltage period for this switch. The main inductor is now discharged through the load.

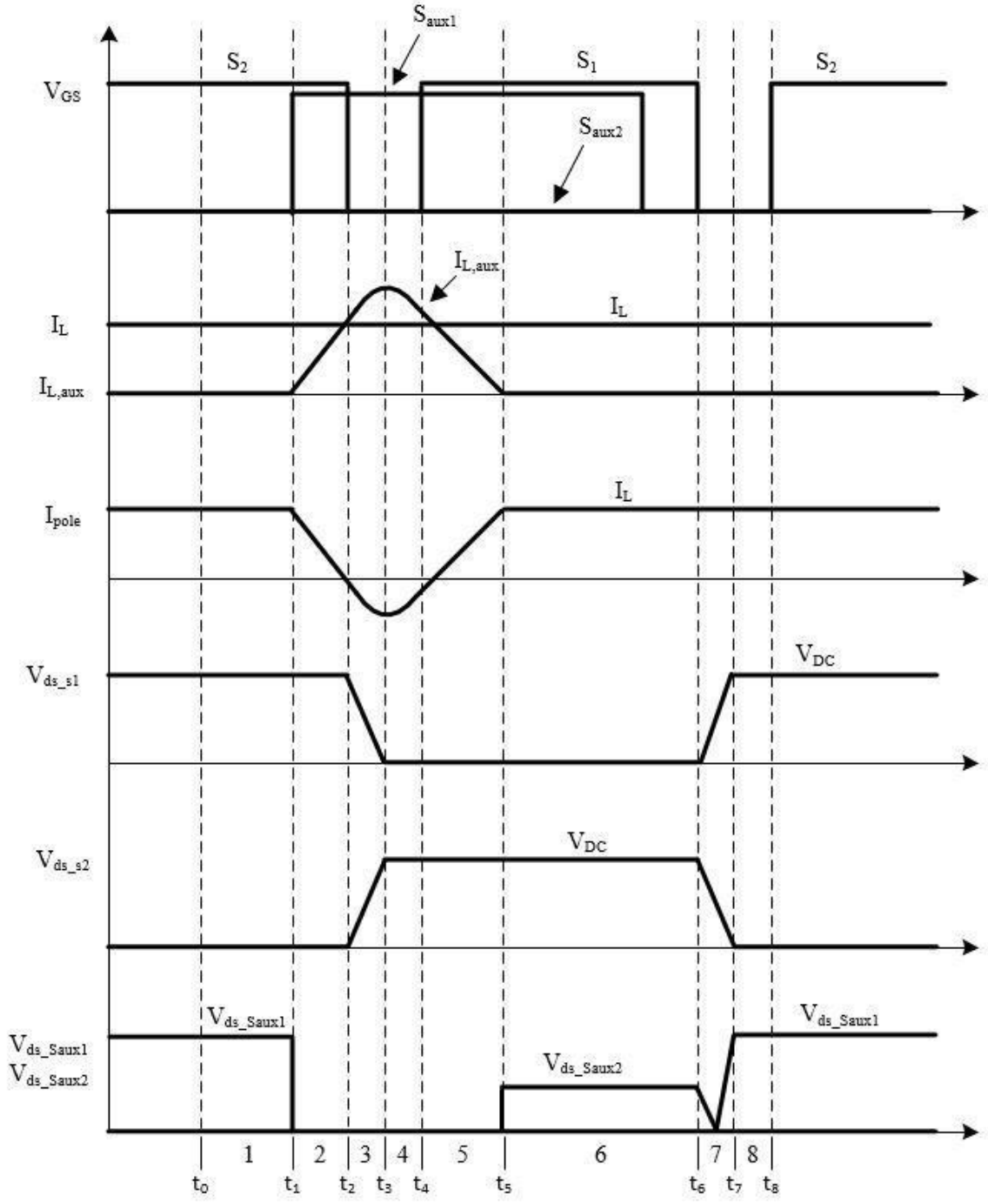


Figure 3.4: Salient waveforms in boost mode

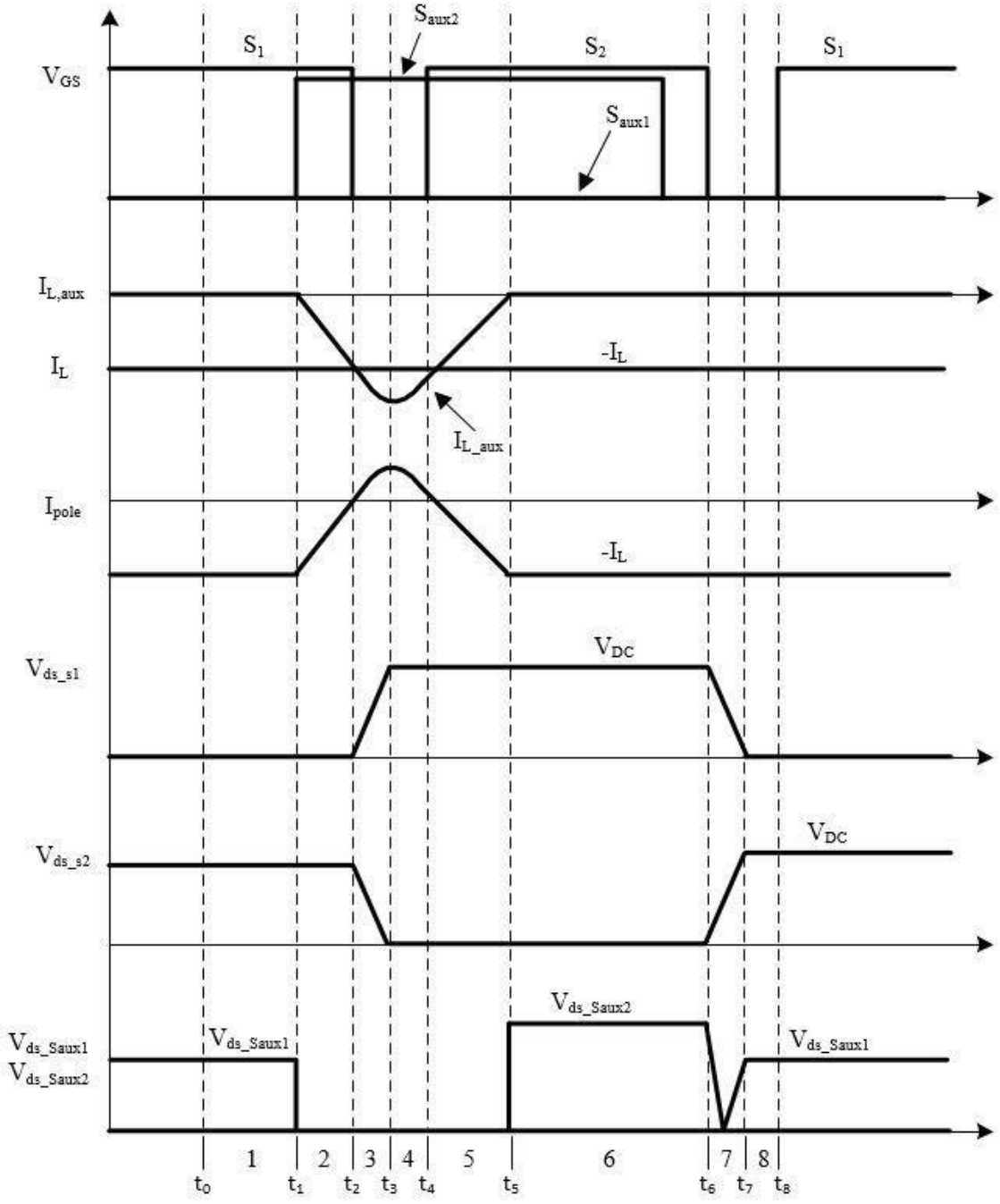
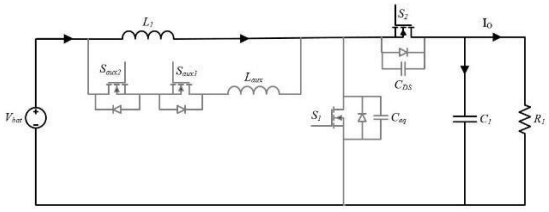
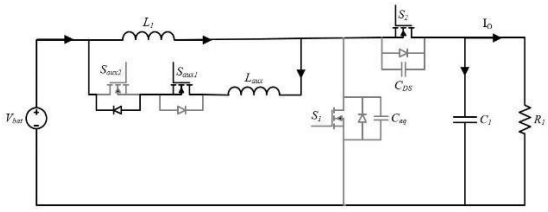


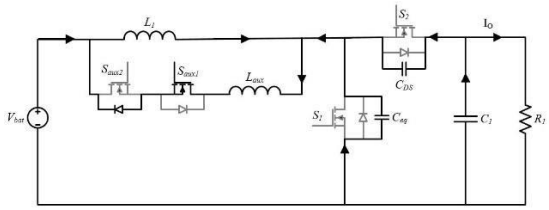
Figure 3.5: Salient waveforms in buck mode



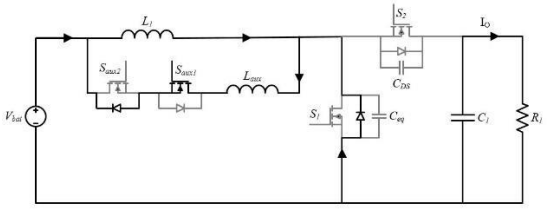
(a) Interval 1



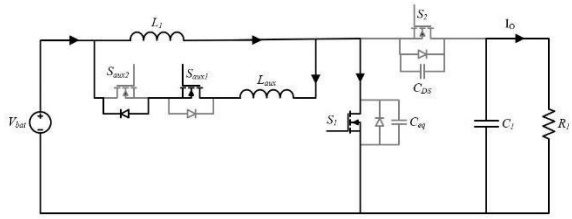
(b) Interval 2



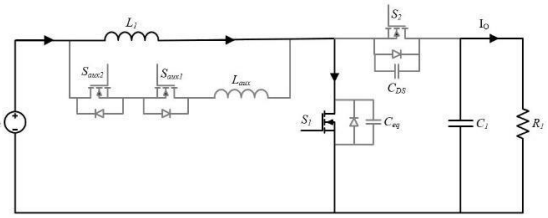
(c) Interval 3



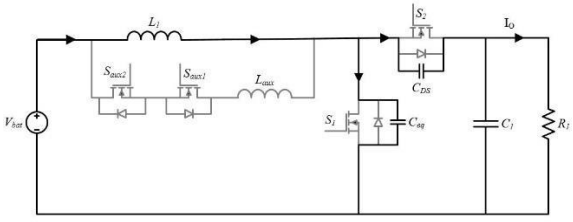
(d) Interval 4



(e) Interval 5



(f) Interval 6



(g) Interval 7

Figure 3.6: Conduction path in each switching interval of boost mode

3.3 Salient Features for Automotive Applications

The features required for a high efficiency converter for automotive applications were detailed in section 1.2 and now that we have shown the operating regime of the designed converter, a number of salient features have come to the fore that align perfectly with requirements within automotive power electronic modules.

a. Soft-switching for all switches

As seen in the previous section, the high efficiency of the designed and implemented converter is contributed to in main because of the zero voltage switching for the main and synchronous switches and zero current switching for the auxiliary branch switches. The sof switching for all the switching in the topology helps save on switching losses and thereby dramatically improves system efficiency even after having two extra switches per phase as compared to the conventional boost topology.

b. Minimal auxiliary branch losses

The auxiliary branch only conducts for a time period dictated by the linear rise time of the current in the auxiliary inductor and the quarter resonant period of the resonance between the auxiliary inductor and the power pole capacitance. Since this duration is only around 150ns, determined by the values of L_{aux} and C_{eq}, the conduction losses in the auxiliary branch do not add a significant overhead of losses and thereby having that additional circuitry actually improves system efficiency.

c. Flexible ZVT implementation

The linear rise time of current across the auxiliary inductor is based on the blocking voltage across the inductor. This voltage is variable, depending upon the input battery voltage and the output DC-Link voltage. Therefore, the auxiliary circuit can ensure ZVS of the main switch for a number of different operating points, hence making the ZVT implementation flexible with respect to the duty ratio, input voltage and output voltage.

3.4 Converter Design for Gen-II

After successfully designing and implementing a 2.5kw prototype during the first phase of the project, an interleaved topology as shown in section 1.3 has been designed and implemented during the second phase. Each stage of the interleaved topology has been designed for a rating of 10kw as the requirement within EV drivetrains ranges from as low as 30kw to around 200kw. The full power capacity of the designed, 3-phase interleaved topology is therefore 30kw. Interleaving multiple phases has a number of advantages. It reduces the voltage and current stress on each phase and the input inductor and the output capacitor can be designed for higher input current ripple and a higher output voltage ripple for each phase as the interleaving scheme whereby the clock pulses of each phase are phase shifted help with ripple cancellation at both ends. Another advantage of interleaving is the flexibility it lends to power scaling of the system. A summary of a single phase of the designed prototype's specifications is given below.

Table 3.1: Designed bi-directional DC/DC converter specifications

Rated Power	10kW
Input Voltage	200-300V
Output Voltage	310-800V
Switching Frequency	250kHz

3.4.1 Inductor Design

The following four parameters go into designing the inductor.

a. The inductance value, $L\ (H)$:

As mentioned in the previous section, the inductance can be designed for a high input current ripple due to interleaving. A value of 20% input current was used for the inductor value design. The worst case current, when boosting an input voltage of 200V to an output voltage of 800V at 10kw power yields an input current of 50A. The following equation gives the inductor value calculation for this case.

$$L = \frac{VoD(1-D)}{\Delta I L f sw} = 80uH \tag{3.5}$$

b. Peak inductor current is given by:

$$I_{L,peak} = I_{in,max} + \frac{\Delta I_L}{2} = \quad 52.5\ \text{A} \tag{3.6}$$

c. The RMS current rating of the inductor is given by:

$$I_{L,RMS} = \sqrt{I_{in,\max}^2 + \frac{(\Delta I_L)^2}{12}} = \quad 50.02\ \text{A} \tag{3.7}$$

d. The DC bias of the inductor is given by:

$$I_{in,max} = \frac{I_{o,max}}{1-D_{max}} = \quad 50\text{A} \tag{3.8}$$

Inductor Physical Design:

The physical design is an important consideration as well as it determines the core and copper loss to be expected within the designed inductor. Important features of the physical design include the core material, shape, size, number of turns of the wire used, the number of strands, the wire gauge and air gap. These parameters are calculated in the following section.

$B_{max} := 0.2\ T$ $J_{max} := 4\ \frac{A}{mm^2}$ $k_w := 0.4$ $I_{pk} := I_{on} = 55\ A$

a. Area product:

$$A_p := \frac{L \cdot I_{pk} \cdot I_{rms}}{B_{max} \cdot J_{max} \cdot k_w} = \left(6.886 \cdot 10^5\right)\ mm^4 \tag{3.9}$$

A ferrite E-core of dimensions 100/60/28 is selected to account for the calculated area product shown in equation 3.9.

b. Number of turns:

The number of turns required to obtain the desired inductance value is dependent on the expected current peak, maximum flux density, and minimum core area (A_c) obtained from the datasheet.

$$N := \frac{L \cdot I_{pk}}{A_{c1} \cdot B_{max}} = 31.792 \tag{3.10}$$

c. Wire gauge:

The minimum wire gauge requirement is dependent on the expected RMS current rating through the inductor and the maximum current density.

$$A_{cu} := \frac{I_{rms}}{J_{max}} = 12.521\ mm^2 \tag{3.11}$$

Litz wire of AWG No. 30 is selected with 245 strands and conductor diameter of 0.25mm.

d. Air gap:

The discrete air gap in the ferrite E-cores can be calculated using the permeability constant (μ_o), number of turns, minimum core area, and inductance:

$$l_g := \frac{\mu_o \cdot N^2 \cdot A_{c1}}{L} = 10.986\ mm \tag{3.12}$$

3.4.2 Capacitor Selection

The DC-link capacitor is primarily selected based on the RMS current requirement and voltage rating.

a. RMS current rating:

$$I_{C,RMS} = I_{o,max} \cdot \sqrt{\frac{D_{max}}{1-D_{max}}} \cdot \sqrt{1 + \frac{(1-D_{max})^2}{D_{max}} \cdot \frac{\Delta I_L^2}{12 \cdot I_{o,max}^2}} = 22\ \text{A} \tag{3.13}$$

b. Output voltage ripple:

The minimum capacitance required to restrict the output voltage ripple to 10% of the minimum output voltage expected is given by:

$$C \geq \frac{I_{o,max} D_{max}}{\Delta V_o \cdot f_{sw}} = 0.46\text{uf} \quad (3.14)$$

c. Equivalent Series Resistance (ESR) limit:

To reduce the conduction loss, it is desired to pick a capacitor with very low ESR. The selected capacitor must have an ESR that is less than the value given in below:

$$ESR \leq \frac{\Delta V_o}{I_{in,pk}} = 1.52 \text{ ohms} \quad (3.15)$$

d. Voltage rating:

The DC-link capacitor must be able to withstand the maximum output voltage expected plus a sufficient margin to account for voltage ripples and transients.

$$V_{o,max} = 800V + margin \quad (3.16)$$

3.4.3 Switch and Diode Selection

The switch and diode ratings are given as follows:

MOSFET Ratings:

a. Voltage rating:

$$V_{o,max} = 800V + margin \quad (3.17)$$

b. Peak current rating:

$$I_{swpk} = I_{inmax} + \Delta I_L/2 = 52.5\text{A} \tag{3.18}$$

c. RMS current rating:

$$i_{sw,RMS} = I_{in,max}\sqrt{D_{max}} = \ 43.3\text{A} \tag{3.19}$$

Diode Ratings:

a. Voltage rating:

$$V_{o,max} = 800V + margin \tag{3.20}$$

b. Peak Current Rating

$$I_{swpk} = I_{inmax} + \Delta I_L/2 = 52.5\text{A} \tag{3.21}$$

c. Average Current Rating

$$i_{D,avg} = I_{o,max} = \ \ 12.5\ \text{A} \tag{3.22}$$

3.4.4 Auxiliary Branch Design

The auxiliary branch design mainly incorporates the selection of an auxiliary inductor. The value of the inductor is essentially dependent on the conduction time of the auxiliary branch which is in turn dictated by the value of the equivalent capacitance of the power pole. Since the value of the power pole capacitance is fixed by the type of switches selected, the auxiliary inductor value determines the rise time of the current in the auxiliary branch for a given voltage across the inductor. This rise time has to be sufficient for the inductor

current to reach a current equal to the main inductor current for all modes of operation and essentially, for the worst case condition, when the input voltage is the lowest and the output voltage is at rated value. Therefore, a value of inductance is chosen that does not significantly increase the conduction time of the auxiliary branch for the worst case condition and the linear rise time does not exceed a value of more than 100ns to ensure that the conduction losses within the auxiliary branch remain low. Another factor that determines the value of the inductance, as alluded to before, is the resonant frequency between the inductor and the capacitor, and in fact, more appropriately, the quarter resonant period. This period, after the linear rise time, determines the point in time when the capacitor across the main switch is able to fully discharge through the auxiliary branch and the main switch voltage consequently falls to zero. An equation linking the time delay between the turn on of the auxiliary switch and the main switch is given below. This equation is used to calculate the value of the auxiliary inductance, while fixing a limit on the aforementioned time delay for the worst case condition.

$$t_{delay} = t_{rise} + t_{res} = \frac{\pi\sqrt{L_{aux}C_{eq}}}{2} + \frac{L_{aux}i_L}{V_{DC}-V_{bat}} \tag{3.23}$$

3.5 Converter Loss Analysis

3.5.1 Output Capacitance Loss (P_{OSS})

The output capacitance loss is given by the energy dissipated in each switch during the switching transition of that particular switch. This dissipated energy is denoted by E_{OSS} and is given in the datasheet for each switch. The formula for the loss is given in equation 3.24 and it can be seen that it is dependent on the switching frequency as well. The higher the switching frequency, the greater the number of switching transitions for a given period of time and the greater the capacitance loss in the switch.

$$P_{OSS} = 2 \cdot E_{OSS} \cdot f_{sw} \tag{3.24}$$

3.5.2 Gate Loss (P_G)

A number of parameters are required to calculate the gate loss associated with each switch. These include the Q_{GD}, Q_{GS}, $m_{QGslope}$, and $Q_{G(op)}$. The Q_{GD} is the charge that is required to bring the voltage across the gate terminal to zero or in other words, to turn the switch off during the turn off transition. The Q_{GS} is the gate charge required to turn the switch on and the drain-source terminals to start conducting. This charge is therefore required to increase the gate-source voltage beyond the threshold value for conduction. For the series of MOSFETs used in this project, the value of the threshold voltage is 2.4V. Another important parameter is obviously the slope of the rate of change of gate charge between the threshold voltage to the maximum or operating biasing voltage. This voltage can be variable but for the purposes of the project, it was maintained at 10V-12V. The

$Q_{G(op)}$ basically gives the charge that is required to increase the voltage beyond the threshold value to the bias value and is therefore required to measure the gate losses for the operating bias voltage value. The calculation of both the operating charge value and the losses in the gate of each switch is given by the following two equations.

$$Q_{G(op)} = (Q_{GS} + Q_{GD}) + (m_{QGslope} \cdot (V_{DR} - V_{pl})) \tag{3.25}$$

$$P_G = Q_{G(op)} \cdot V_{DR} \cdot f_{sw} \tag{3.26}$$

3.5.3 Body Diode Conduction Loss (P_{SD})

Since the topology being used for each phase is that of synchronous boost, the only times the body diodes or the antiparallel Schottky diodes conduct is when there is a dead-period between the transitioning of the two switches. This time coupled with the fall time of each diode determines the total conduction time of each diode and can be used to determine the losses in each diode knowing the voltage and the average current flowing through each diode for this period. This is given by the following equations for both the turn off and turn on transtions.

$$P_{SD,off} = V_{SD,off} \cdot I_{off} \cdot t_{diode} \cdot f_{sw} \tag{3.27}$$

$$P_{SD,on} = V_{SD,on} \cdot I_{on} \cdot t_{diode} \cdot f_{sw} \tag{3.28}$$

3.5.4 Switching Loss (P_{SW})

In the hard switched case, the switching losses of each switch account for the highest percentage of the total converter losses and therefore he ZVT branch is essential to the high efficiency operation of the selected topology for EV drivetrains. The synchronous switch goes through a natural ZVS as it either transitions to or from a very small diode voltage so the losses incurred in it are very small. However, the main switch incurs a high value of both turn on and turn off loss. The method of calculation of these switching losses is dependent on a number of factors as denoted in the next two equations.

$$P_{on} := \frac{\left(V_{out} \cdot I_{on} \cdot f_{sw} \cdot R_{Gon}\right)}{2} \cdot \left(\frac{Q_{GD}}{V_{DR} - V_{pl}} + \frac{Q_{GS2}}{V_{DR} - \frac{\left(V_{pl} + V_{th}\right)}{2}} \right) \tag{3.29}$$

$$P_{off} := \frac{\left(V_{out} \cdot I_{off} \cdot f_{sw} \cdot R_{Goff}\right)}{2} \cdot \left(\frac{Q_{GD}}{V_{pl}} + \frac{Q_{GS2}}{\frac{\left(V_{pl} + V_{th}\right)}{2}} \right) \tag{3.30}$$

3.5.5 Switch Conduction Loss (P_{cond})

This is where the switch selection plays an important role in lowering the total losses of the system under ZVS operation. The switching losses are minimized through ZVS, but the conduction losses can only be controlled through switch selection, opting for devices with a low R_{DSon}, which is the switch resistance as the switch conducts. This resistance determines the conduction losses through the switch as shown by the following equation.

$$P_{cond} = I_{sw2\,,RMS} \cdot R_{DS,on} \cdot D \tag{3.31}$$

3.5.6 Inductor Loss (P_{ind})

The major part of the losses within an inductor, for an unsaturated core, comes from the copper losses in the winding of the inductor. These losses can be controlled by designing the inductor in such a way that the DC resistance of the winding can be reduced to the minimum. A method employed is to house as many parallel paths for a single turn of wire around the core as possible. The other part of the inductor losses comes form the core. Calculating core losses can be an extremely involved exercise but some proprietary equations can at times be applied to certain cores, such as those provided by ferroxcube, to determine the core losses. The copper loss and core loss equations are given below.

$$P_{ind} = I_{L,RMS}^2 \cdot R_{dc} \tag{3.32}$$

$$P_v = C_m \cdot f_{sw}^x \cdot B^y \cdot \frac{Ct_2 \cdot T^2 - Ct_1 \cdot T + Ct}{1000} \tag{3.33}$$

$$P_{core} = P_v \cdot V_e \tag{3.34}$$

3.5.7 Capacitor Loss (P_{cap})

The loss in the DC-Link capacitor is straight forward to calculate and depends on the series resistance of the capacitor and the RMS current flowing through it.

$$P_{cap} = I_C^2{}_{,RMS} \cdot ESR \tag{3.35}$$

A loss comparison is carried out between the analytical values calculated through the equations given above and the simulated losses at the end of the next section. A comparison

is also made between the losses incurred in soft switching versus the losses that result due to hard switching.

3.6 Converter Simulation

This section details the simulation of the designed converter. The three phase interleaved version of the converter is simulated and the component values for each phase calculated in section 3.4 have been used. Figure 3.7 shows a schematic of the simulated converter. The simulation is carried out to verify the loss analysis as well as the operation of the converter in terms of the switching intervals and the behavior of switch voltages and currents during each interval.

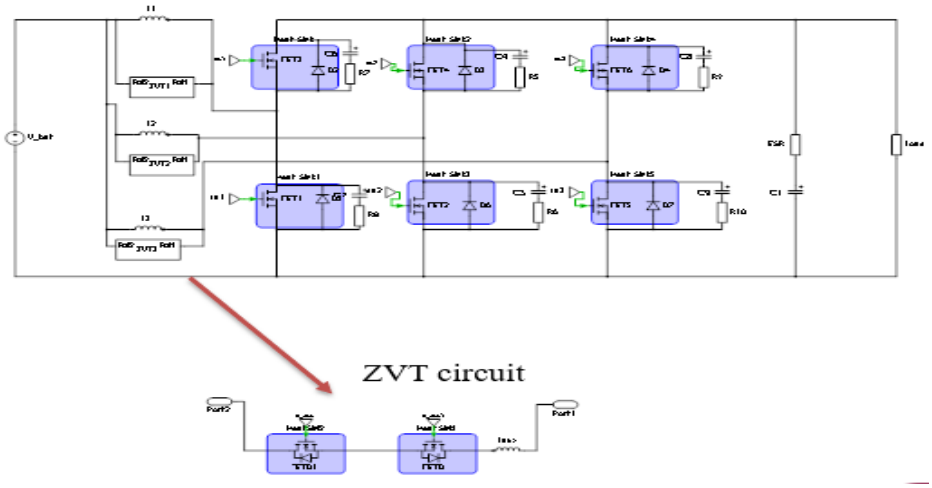


Figure 3.7: PLECS schematic used for simulating the proposed converter topology

K-factor control is used to regulate the input inductor current. The plant transfer function used for the controller design is given in equation 3.37 below.

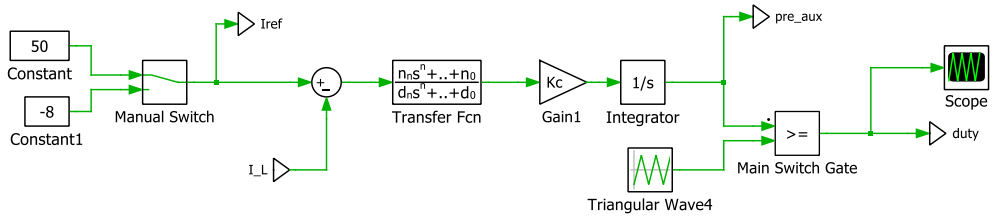
$$G_{plant}(s) = \frac{V_{in}}{R_L} \cdot \frac{1+sC(R_{ESR}+R_L)}{1+s\left(\frac{L}{R_L}+CR_{ESR}\right)+s^2LC\left(1+\frac{R_{ESR}}{R_L}\right)} \tag{3.37}$$

The plant transfer function phase and magnitude are dependent upon the input voltage, the output voltage, the power level and the values of the passive components L, C and the ESR. An input voltage of 200V, output voltage of 600V and power level of 10kw was used for the design of the controller. The values of the per phase passive components and ESR were the same as calculated in section 3.4. The desired phase margin was set at 60^{o} for controller stability and a Type-II K-factor controller was designed with the following transfer function and parameters.

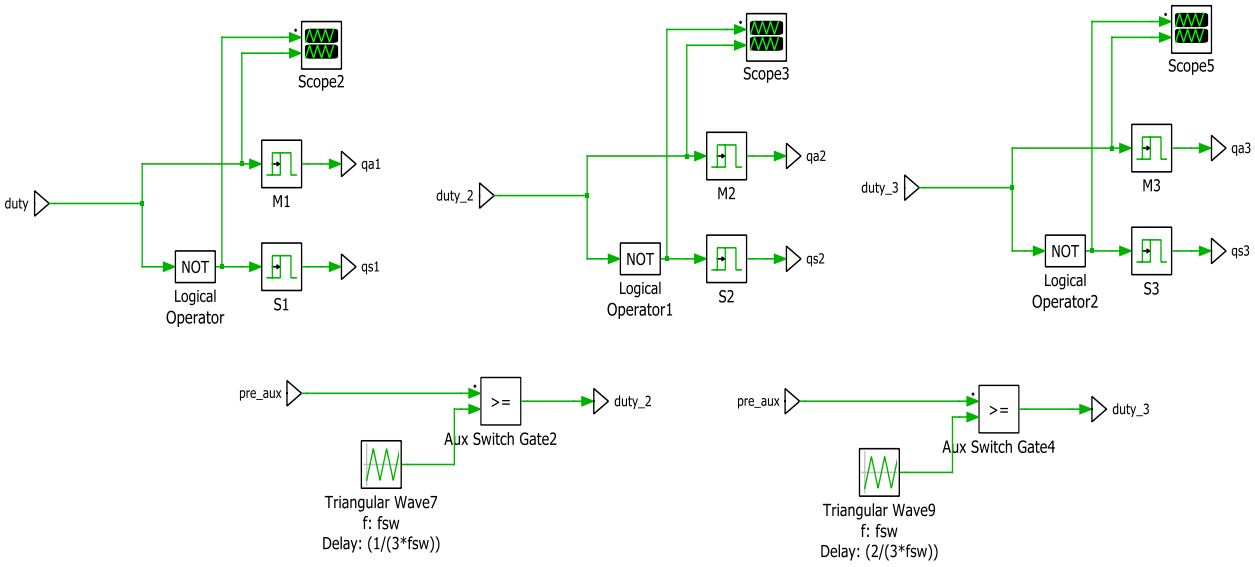
$$G_c(s) = \frac{K_c\left(1+\frac{s}{\omega z}\right)}{\left(1+\frac{s}{\omega p}\right)} \tag{3.38}$$

$$K_c = 9.619 \cdot 10^3$$
$$\omega z = 4.201 \cdot 10^4$$
$$\omega p = 5.855 \cdot 10^5$$

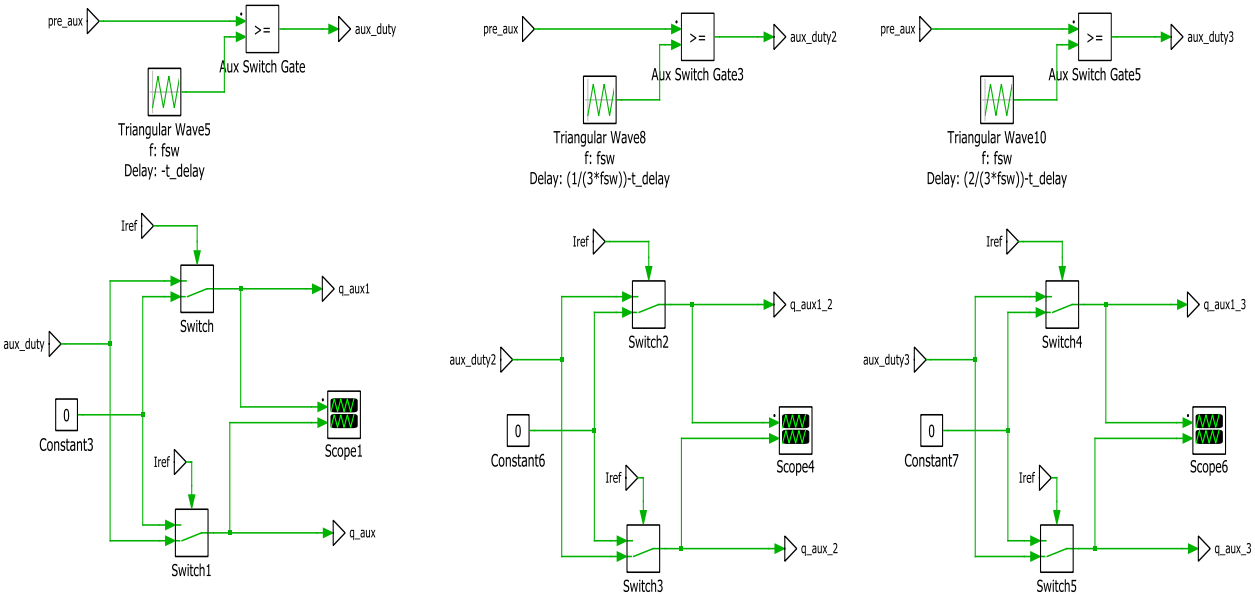
The resulting controller output is then phase shifted by 1/3 for each subsequent phase as there are a total of three interleaved phases. The entire implementation of the control strategy is depicted in figure 3.8.



(a)



(b)



(c)

Figure 3.8: (a) Current control implementation in PLECS through Transfer Function Implementation (b) Phase shifting gate signals of subsequent phases by 1/3 (c) phase shifting auxiliary gate signals by 1/3 for each subsequent phase

The value of -t_delay shown in figure 3.8 is derived by using the formula given by equation 3.23 in the previous section. This equation describes the linear rise time of the

current in the auxiliary branch which changes with the voltage across the auxiliary inductor which depends on both the input and output voltages. This means that the delay implemented for the auxiliary switch turn on is adaptive and factors in the operating condition. The other factor that the delay, which is essentially the delay between the turn on of the auxiliary switch and the turn on of the main switch, depends upon is the quarter resonant time of the auxiliary inductor and the power pole capacitance. Since the value of these passive components is fixed, by the selection of the auxiliary inductor and the switches in the main power circuit, this second term in the formula in equation 3.23 is fixed and equals about 41ns. Figure 3.9 thru 3.11 show the salient waveforms for all three phases in the interleaved converter schematic given by figure 3.9. The converter is simulated for motoring mode of operation and the waveforms obtained have been compared and verified with the expected operating principles.

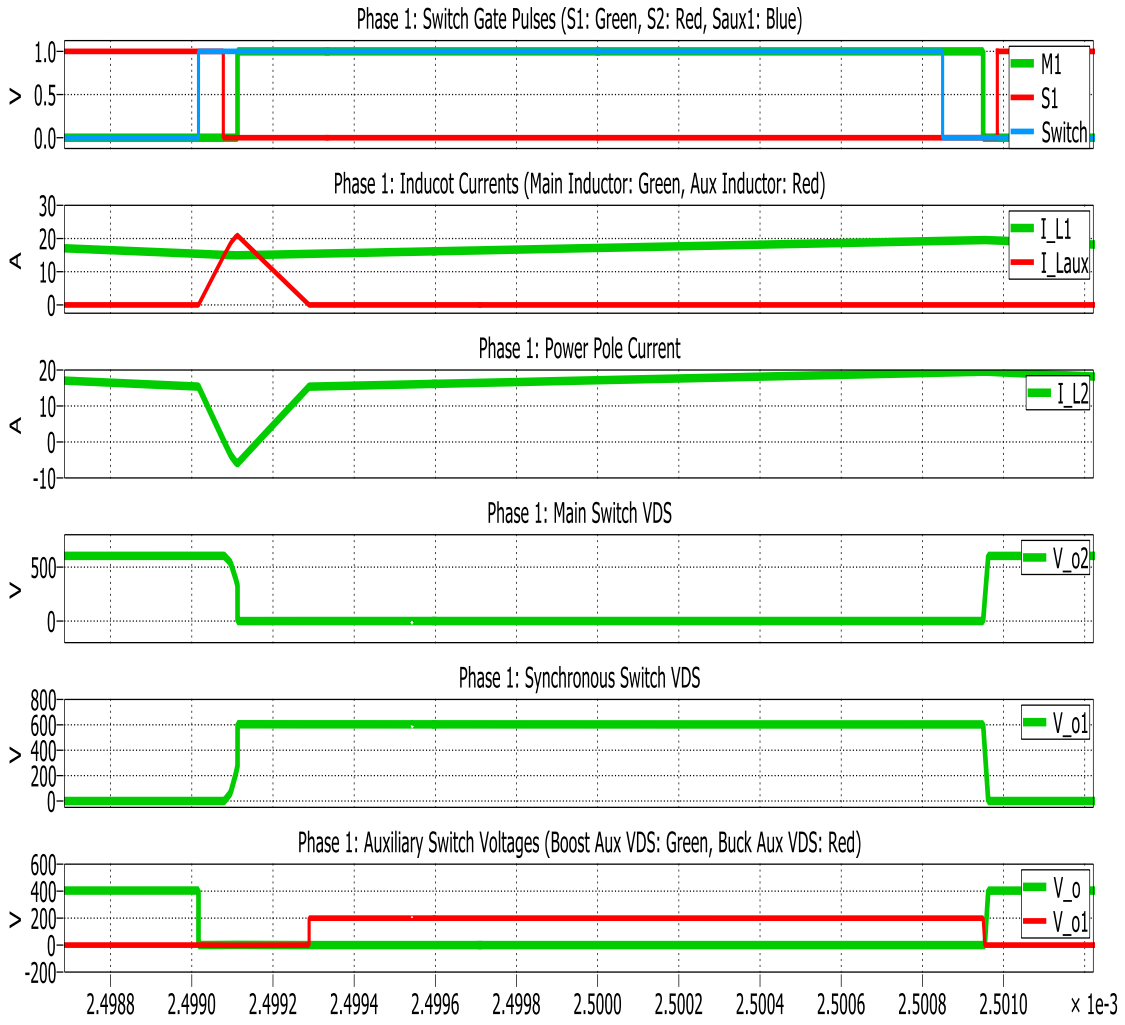


Figure 3.9: Simulated key operating waveforms for Phase 1 in boost mode

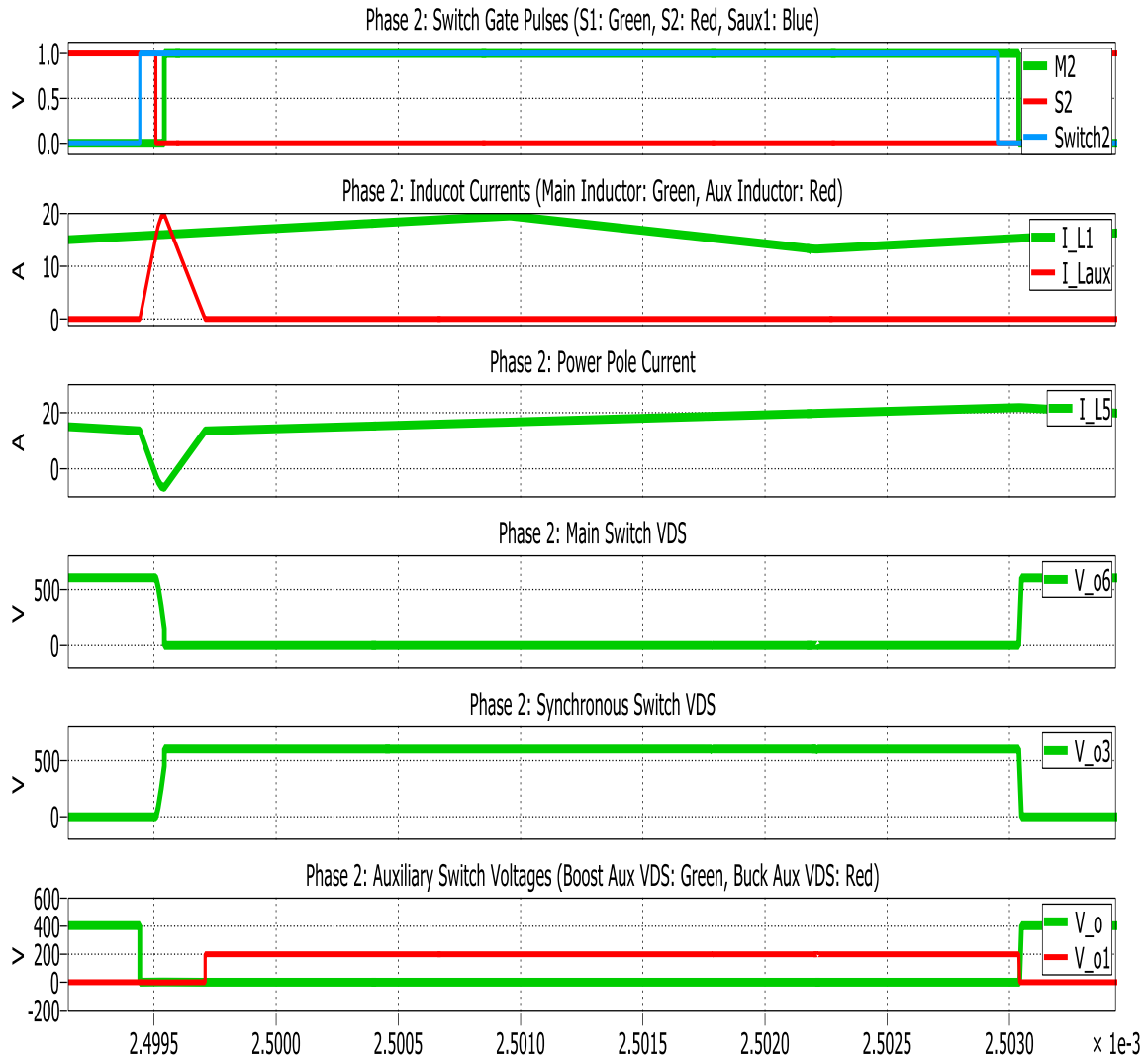


Figure 3.10: Simulated key operating waveforms for Phase 2 in boost mode

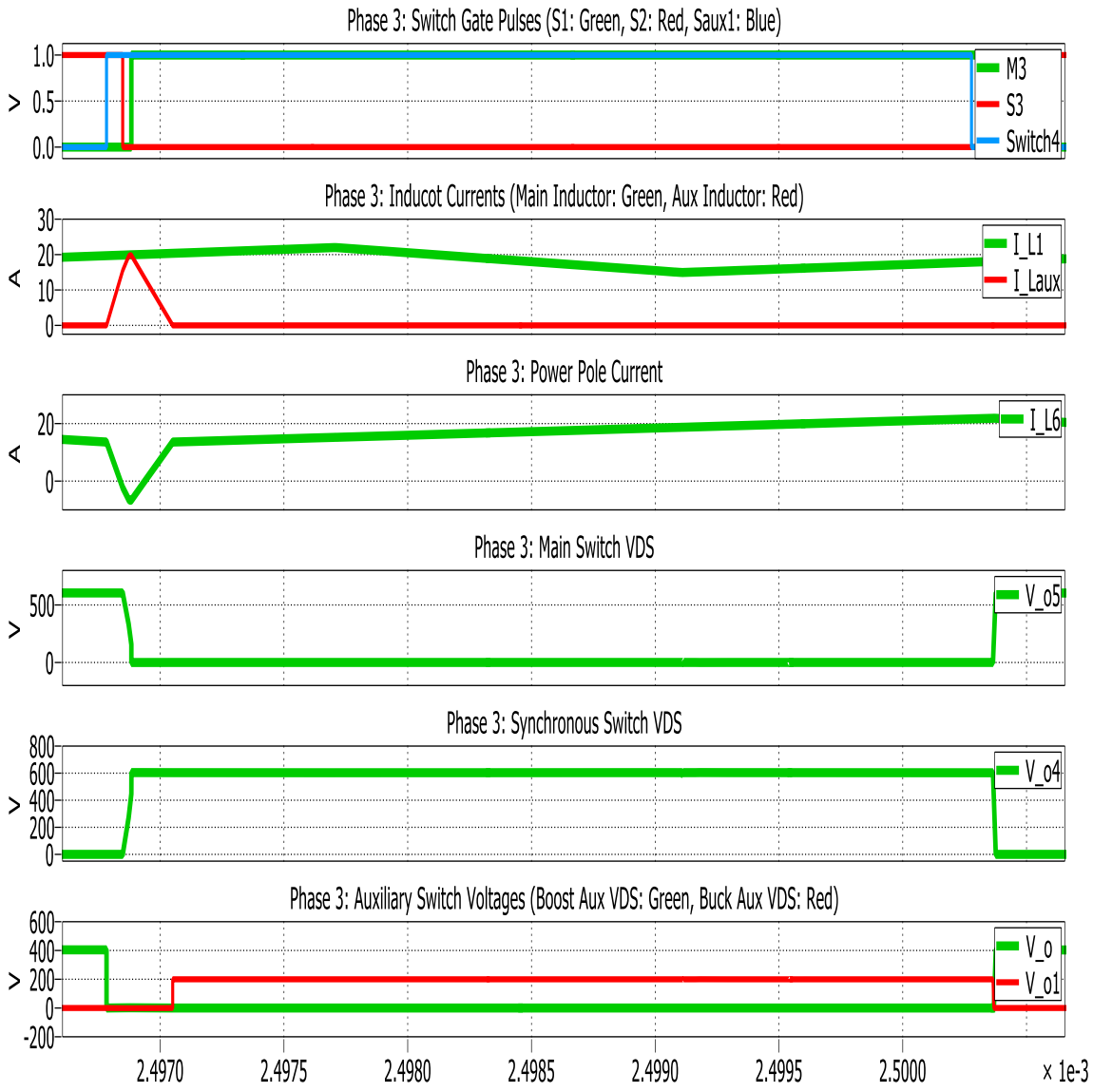
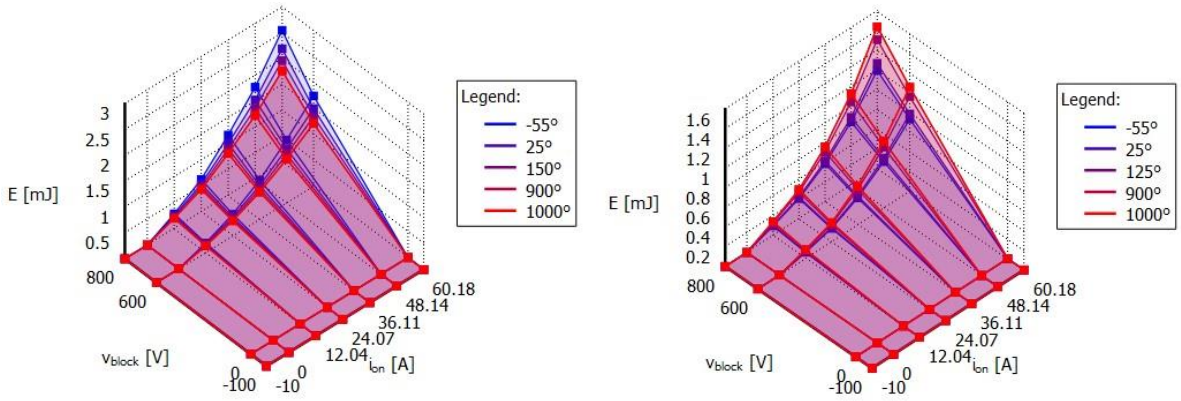


Figure 3.11: Simulated key operating waveforms for Phase 3 in boost mode

The waveforms shown in figure 3.9 thru 3.11 are in agreement with the operating principles described earlier in chapter 3. The boost auxiliary switch is gated prior to the turn on of the main switch by a time delay given by equation 3.23. This diverts the power pole current through the auxiliary branch and discharges the capacitor across the main switch through the auxiliary branch. This can be seen for each of the three phases in the interleaved topology by virtue of the waveforms provided. Soft switching is achieved as this discharge of the main switch capacitance leads to the voltage across the switch dropping to zero before it is gated on. The simulation confirms that the implemented control methodology ensures soft switching for each phase of the interleaved converter and the design can therefore be exported to hardware implementation.

Once the operation of the simulation setup is verified through the salient waveforms, the next step was to establish an agreement between the simulated converter efficiency and the analytical efficiency calculated. This was done for a single phase 10kw module for the soft switching case. To ensure that the semiconductor characteristics in simulation matched those used in the analysis, the PLECS models of MOSFETs and Diodes were linked to thermal models of the actual switches. The thermal models have been provided by Wolfspeed in [29]. The thermal models are basically look-up tables that describe the turn on and turn off characteristics in terms of energy dissipation against blocking voltage and on state current through the MOSFETs. The conduction losses are also by these thermal models and these depend upon the temperature of the device, the current flowing through the device and the on-state resistance. The switching characteristics for the main MOSFETs are given in figure 3.12 and the conduction loss characteristics are given in figure 3.13.



(a) (b)

Figure 3.12: C2M0025120D MOSFET (a) turn-on loss (b) turn-off loss

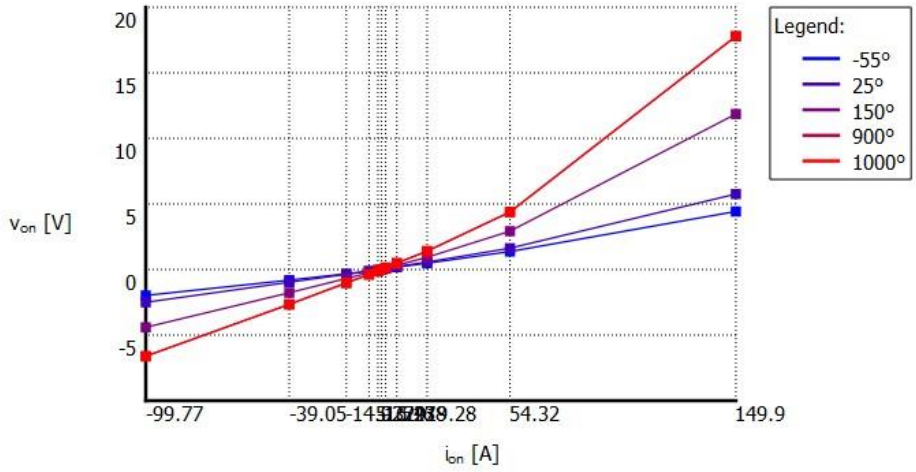


Figure 3.13: Conduction loss characteristic curves for C2M0025120D MOSFET

A summary of the comparison between analytical losses and simulated losses is given in the bar chart below.

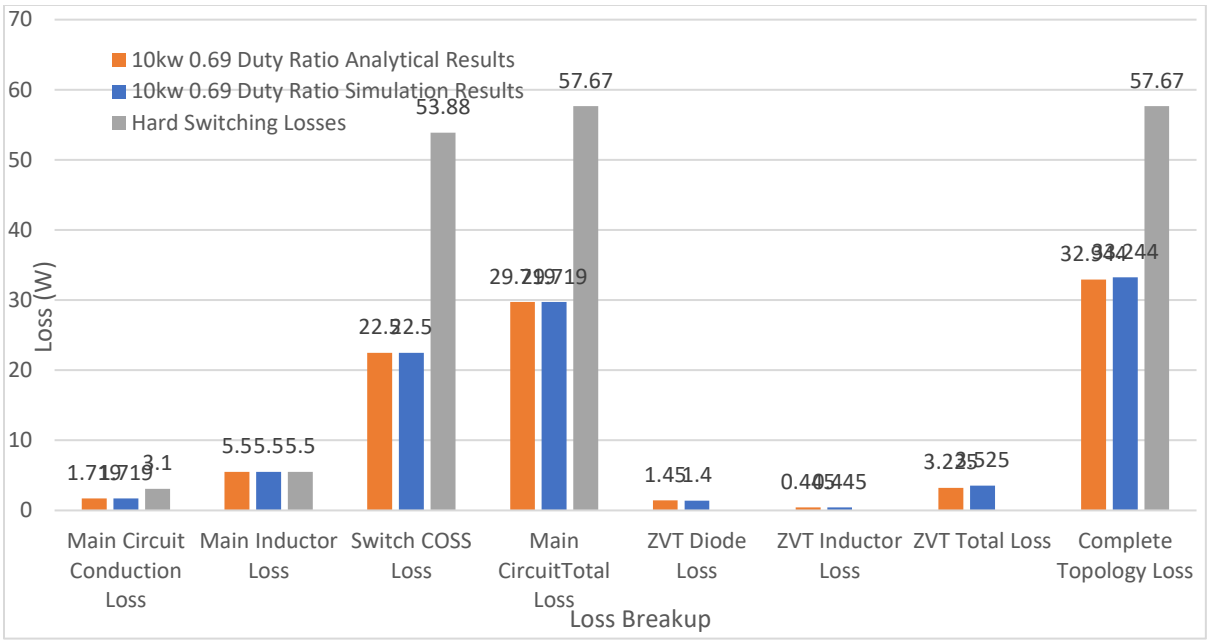


Figure 3.14: Comparison of simulated and analytical soft switching losses with analytical hard switching losses

Chapter 4

HARDWARE PROTOTYPE IMPLEMENTATION AND RESULTS

4.1 Hardware Implementation: Overview

Hardware implementation was carried out for both the 1st Gen prototype as well as the 2nd Gen prototype. The design details, loss analysis, simulation results and partial hardware results for the 1st Gen prototype were documented during the first phase of the project. Here, the improved hardware test results for the 1st Gen prototype are documented, both for the motoring mode of operation and the regenerative mode of operation. Following this, the 2nd Gen prototype is discussed in detail and the hardware implementation and results provided.

4.1.1 Gen-I Prototype

The result from the 1st Gen prototype are provided in the following section. Figure 4.1 shows waveforms for a soft switching case at 1.0kw for the motoring mode of operation. This particular set of waveforms is provided here to comment upon the nature of resonance occurring. It can be seen that the auxiliary current, given by the blue waveform, experiences two resonant peaks. This suggests that the auxiliary switch stays on for an unnecessarily long period before the turn on of the main switch. This is also supported by the main switch VDS dropping to zero and rising back up again before the second resonance which is when it drops back to zero and stay at zero as now the main switch has finally been turned on. Even though ZVS is occurring for the main switch, this is a more lossy scenario to when

ZVS is achieved during the first resonance as it allows for a greater conduction period in the auxiliary branch and causes greater conduction losses therein.

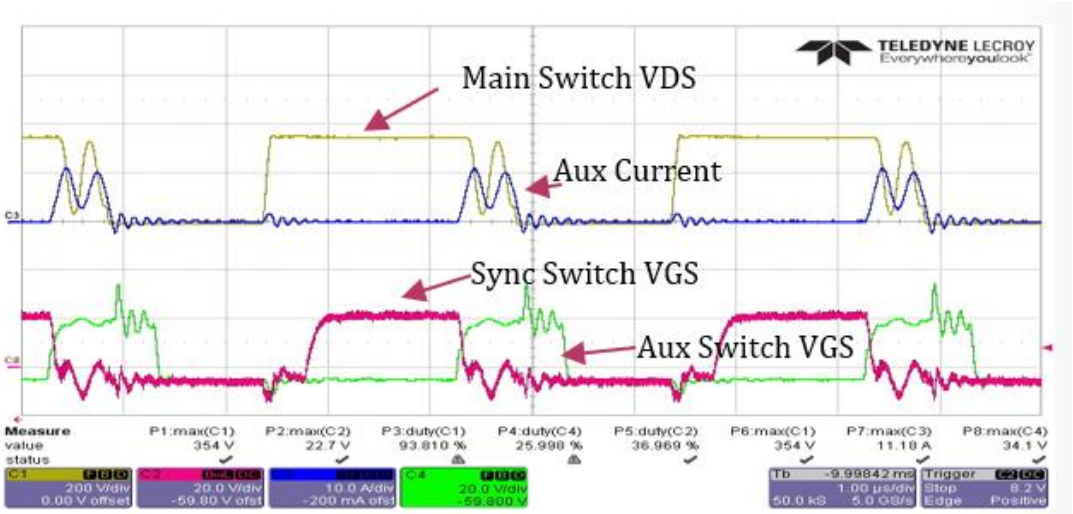
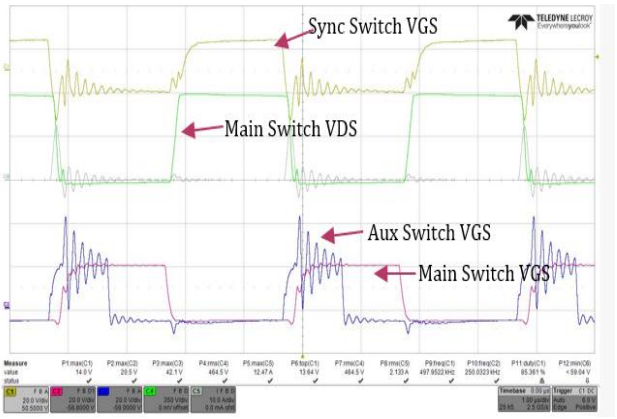


Figure 4.1: Waveforms for 1.0kw Soft switching in Boost Mode

This scenario is remedied by adjusting the timing of the auxiliary switch turn on based on the linear rise time of the current in the auxiliary branch and the quarter resonant time of the auxiliary inductor and the equivalent power pole capacitance, given by the following equation.

$$t_{delay} = t_{rise} + t_{res} = \frac{\pi\sqrt{L_{aux}C_{eq}}}{2} + \frac{L_{aux}i_L}{V_{DC}-V_{bat}} \quad (4.1)$$

Once this adjustment is made, the main switch turn on occurs during the first resonance and the conduction losses are limited in the auxiliary branch. The waveforms for a rated 2.5kw case for the boost mode of operation in Gen 1 are given in Figure 4.2. The corresponding power analyzer results are also given in figure 4.2 and it can be seen that an efficiency close to 98.2% is achieved for this case. Both the input and output voltages are also provided and the duty ratio used for this particular case is 0.5.



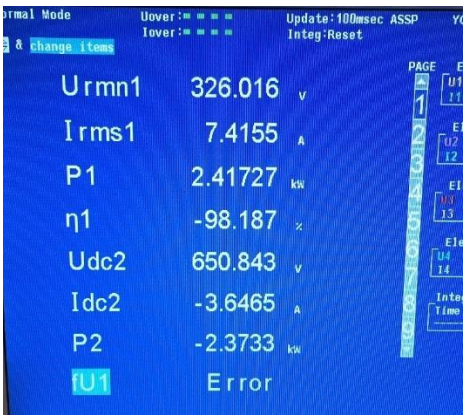
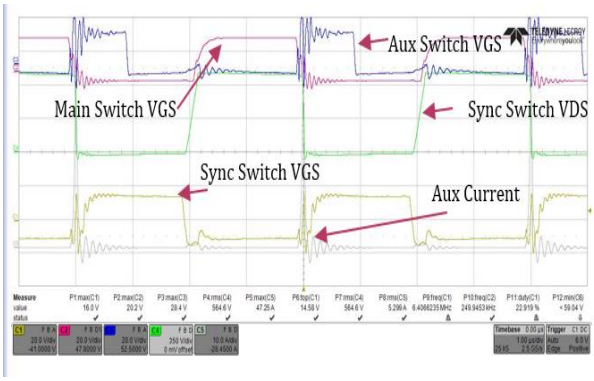


Figure 4.2: Waveforms for 2.5kw Soft switching in Boost Mode and Efficiency Results

Similarly, a soft switching case for the buck mode of operation at 2.0kw is provided in the figure 4.3. The corresponding efficiency results are also provided in the same figure. Again, an efficiency over 98% is achieved for this case. However, it may be noted that the battery voltage simulated by the low voltage side of the converter in this case is very high, i.e. 588V. This might be seen as a factor contributing to the high efficiency due to the correspondingly low buck side current but other scenarios with lower buck side voltage and higher current have been tested and similar efficiencies achieved.



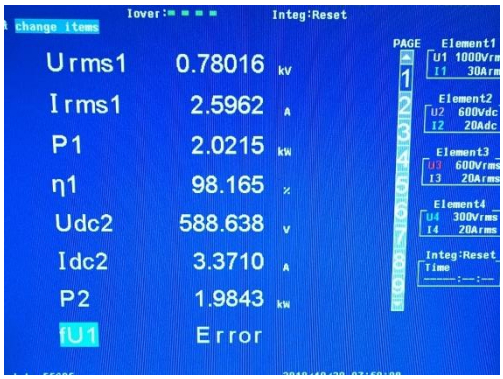


Figure 4.3: Waveforms for 2.0kw Soft switching in Buck Mode and Efficiency Results

A comparison of the boost and buck mode hard switching and soft switching efficiencies is provided in figure 4.4. Here, efficiencies are plotted against the power rating of the experiment carried out.

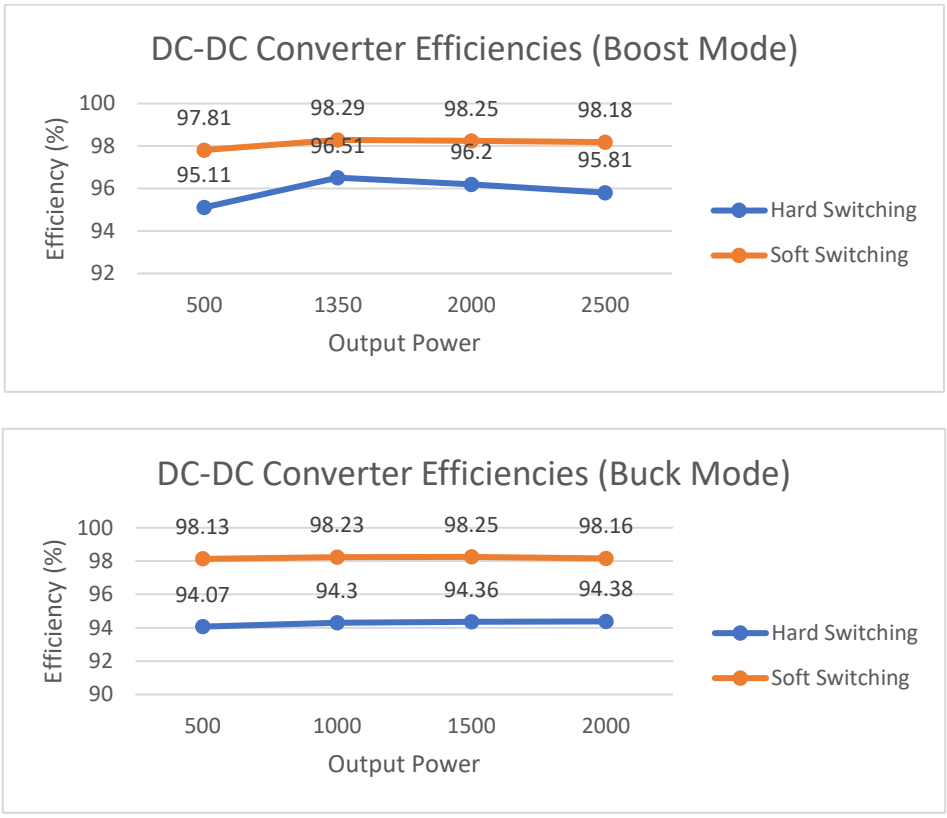


Figure 4.4: Soft and Hard switching efficiency comparisons: Boost Mode (top) and Buck Mode (bottom)

It can be seen that the maximum efficiency improvement in the boost mode is actually achieved at the highest power and it is almost 2.4%. The highest efficiency achieved in this scenario is almost 98.3% and this occurs at 1.35kw. This is because the duty ratio employed at this power level was lower than the other cases. This resulted in lower input currents and

lower conduction losses, accounting for the slightly higher efficiency. For the buck mode, the efficiency trends are constant as the same duty ratio, 0.5, was used for all test cases. The maximum efficiency improvement in this case was around 4% when going from hard switching to soft switching for almost all data points plotted.

4.1.2 Gen-II Prototype

The components designed and selected based on the calculations provided in the Section 3.4 have been summarized in Table 4.1. The switches used for the main power circuit are from the CREE C2M series of N-Channel SiCFETs. They have a maximum voltage rating of 1200V and a current rating of 90A, [30]. These switches have low R_{DSON} of 25mΩ which helps lower on state conduction losses. SiCFETs from the same series but with a lower current rating of 36A have been used in the auxiliary branch. The R_{DSON} of these switches is higher, at 80mΩ [31] but since the conduction time is lower (on the order of only up to 100ns) for the auxiliary branch, the higher R_{DSON} does not contribute to significantly higher conduction losses in the auxiliary branch. The C_{DS} across the selected switches is only 220pf which does not cause unwanted LC resonance and ringing in the circuit. The output capacitor is selected to meet the output RMS current requirement and a value of 20uf with an ESR of 4.25mΩ is selected. These ratings are realized by having two 10uf capacitors from the AVX Corporation [32] in parallel at the output.

The PWM signals required for both the main switches and the auxiliary switches are generated through a Texas Instruments™ TMS320F28335 Digital Signal Processor (DSP). The code is written, built and loaded onto the DSP using a Code Composer Studio (CCS)

by Texas Instruments and an ezDSP F28335 emulator is used to connect the DSP to the programming computer. The DSP has 6 independent PWM channels with two output for each channels so it is capable of generating 12 PWM signals at a given time. This is essential when it comes to interleaving operation as each phase of the converter requires exactly 4 pwm signals. This totals to 12 pwm signals for a 3-phase interleaved converter. The 12-bit on-chip Analog to Digital converter (ADC) is used to sense signals such as V_{in}, V_{out} and i_L. The ADC has a sampling rate of 80ns which helps implement an efficient control with low steady state error.

Table 4.1: List of selected components for the converter

Selection of Components for 10kw Module	
Main Inductor	
Core Specs	E100/60/28
Core Material/Shape	Ferrite/E-Core
Number of Turns	32
Air Gap, l_g	10.1mm
Wire Gauge	AWG No. 30
Number of Strands, n_s	245
Capacitor	
Capacitance	20uf
ESR	4.25mΩ
Voltage Rating	1100V
RMS Current Rating	22A
Main Switch + Synchronous Switch	
Switch Ratings	1200V, 90A SiCFET C2M0025120D
$R_{DS,on}$	25mΩ
Auxiliary Switches	
Switch Ratings	1200V, 36A SiCFET C2m0090120D
$R_{DS,on}$	80mΩ

The top layer of the fabricated PCB for one module of Gen 2 is shown in figure 4.5 and the bottom layer is shown in figure 4.6. The jumper wire visible in figure 4.5 connected the auxiliary branch to the main circuit at the power pole and is provided so the current through the external branch can be probed. The main inductor is also connected externally and can be seen in figure 4.7 where one module is connected for testing.

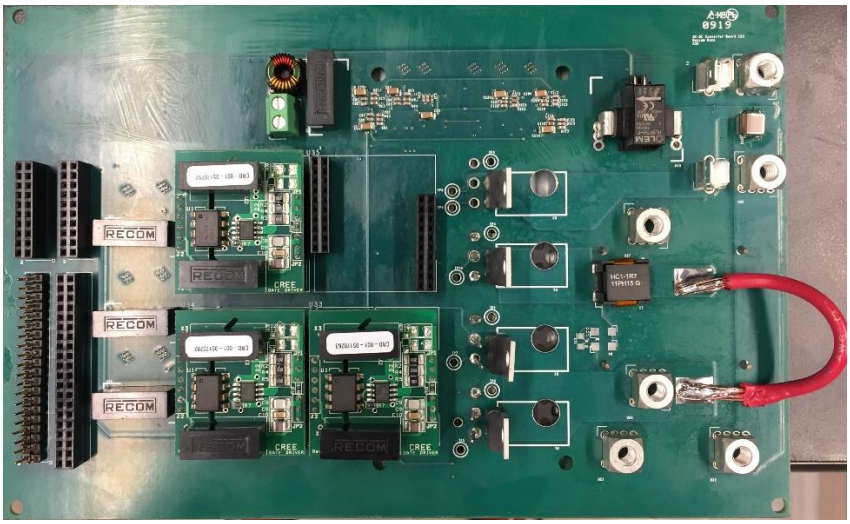


Figure 4.5: Top side of the PCB

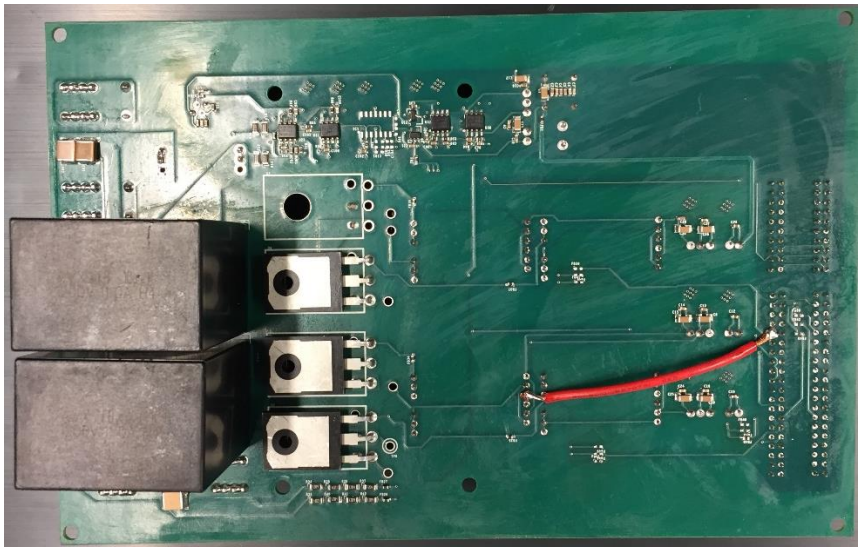


Figure 4.6: Bottom side of the PCB

The experimental setup for three phase shown below is connected to a Magna ARx20.25-1000-42 rated at 20.25kw and 1000V.

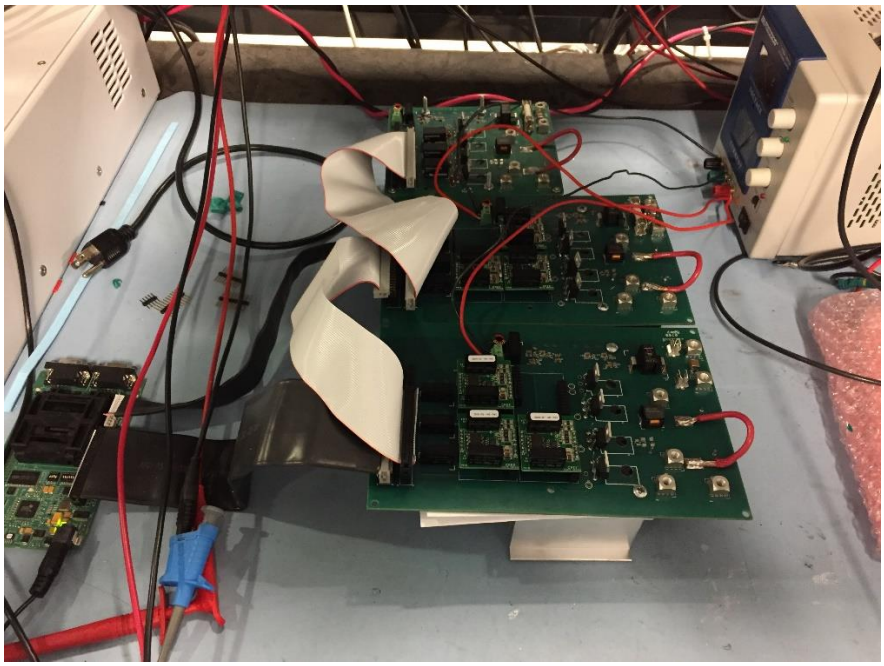


Figure 4.7: Experimental setup of the hardware prototype

4.2 Experimental Results for Gen-II

The objective of the experiment conducted in phase two of the project was to scale up power using interleaving. Each interleaved module was designed for 10kw power and tested for 3.3kw power so as to ensure that the interleaved 3-stage converter could be scaled up to at least 10kw in total.

4.2.1 Single Phase Results

The 3.3kw results for each module were very similar and have been shown in figure 4.8. Here the duty ratio is kept fixed at 0.5 and the voltage is boosted from 400V to 800V. The waveforms shown are main switch V_{GS} (yellow), main switch V_{DS} (green),

synchronous switch V_{GS} (red) and auxiliary switch V_{GS} (blue). It can be seen that soft switching is achieved as the main switch V_{DS} drops to zero before the value of the main switch V_{GS} exceeds the threshold value of 2.4V. The efficiency achieved for this test case is 98.18% and is in keeping with the required level of efficiency expected.

Figure 4.8: Waveforms and efficiency results for 3.3kw module

4.2.2 Two-Phase Interleaved Results

Once the 3.3kw results were achieved for each module, the next step was to interleave 2 modules and scale up the power to produce efficiency results at higher power. The results for the case with two interleaved modules are shown in figure 4.9. Here, the waveforms shown are phase-1 main switch V_{GS} (green), phae-1 main switch V_{DS} (red), phase-2 main switch V_{GS} (yellow) and phase-2 auxiliary switch V_{GS} (blue). The efficiency achieved at 5.6kw power is 98.04%. The duty ratio is maintained at 0.5 and the voltage is boosted from 300V input to 600V output.

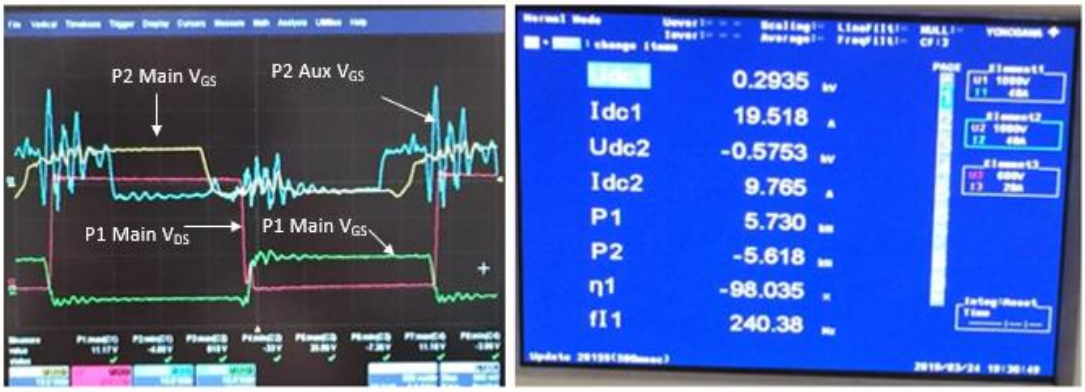


Figure 4.9: Waveforms and Efficiency results for 5.7kw two interleaved modules

4.2.3 Three-Phase Interleaved Results

Along with achieving high efficieincy results, implementation of three phase interleaving was the primary task of the project to ensure the developed prototype had significant power scaling capability over the Gen-1 model, while maintaing the same efficieincy. To achieve three phase interleaving, three identical single phase modules developed for Gen-2 were connected in parallel and the clock pulses of phases 2 and 3 were phase shifted by 120º and 240º each. The clock pulses for the main and boost auxiliary switches are given in figure 4.10 and the main and synchronous are given in figure 4.11.

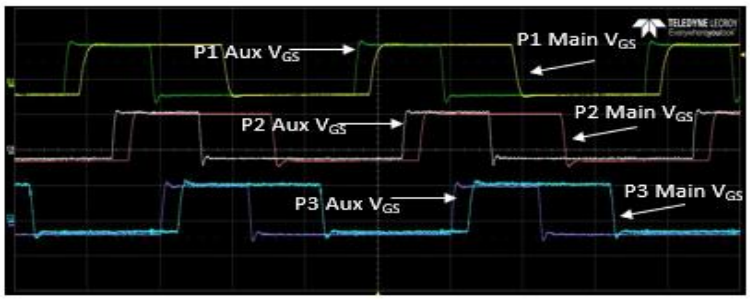


Figure 4.10: Clock Pulses: Phase-1 (Main: Yellow, Aux: Green), Phase-2 (Main: Red, Aux: White), Phase 3(Main: Indigo, Aux: Purple)

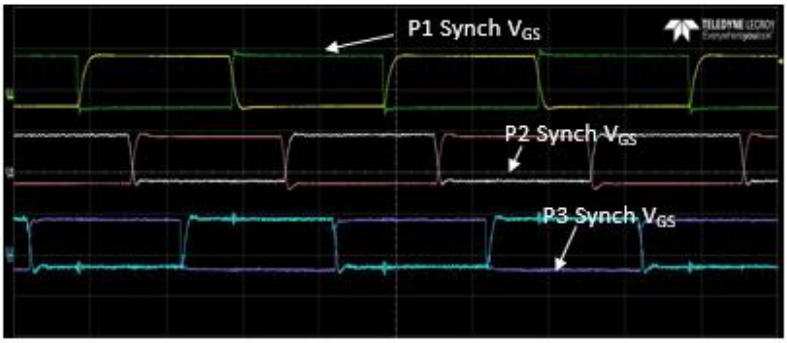


Figure 4.11: Clock Pulses: Phase-1 (Main: Yellow, Synch: Green), Phase-2 (Main: Red, Synch: White), Phase 3(Main: Indigo, Synch: Purple)

After setting up the clock pulses, the setup was connected as shown in figure 4.7 and power testing was carried out. The power was gradually increased to 6.7 kw while maintaining the efficiency at over 98% for each test case. The efficiency was maintained due to ZVS operation for each of the three interleaved phases and this can be verified in figure 4.12. The drain to source blocking voltage across each main switch is brought down to zero before the gate to source voltage across the given switch rises beyond the threshold voltage, turning the switch when the voltage across it is zero. This ensures ZVS for the main switch, and as explained in section 3 in detail, the auxiliary switches undergo zero current switching while the synchronous switch undergoes natural zero voltage switching.

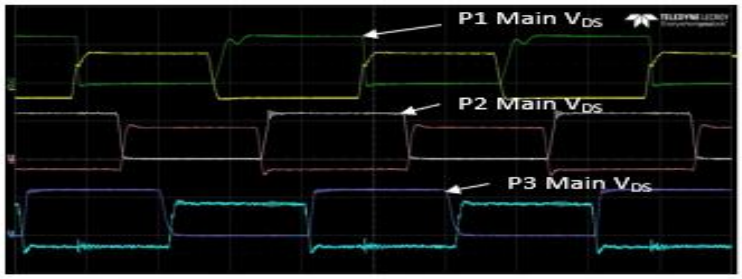


Figure 4.12: Main Switch V_{GS} and V_{DS}: Phase-1 (Main V_{GS}: Yellow, Main V_{DS}: Green), Phase-2 (Main V_{GS}: Red, Main V_{DS}: White), Phase-3 (Main V_{GS}: Indigo, Main V_{DS}: Purple)

The maximum power achieved so far in the three phase interleaving scenario has been 6.7 kw and the power analyzer results for this case have been givein in figure 4.13.

Figure 4.13: Power Analyzer Results 6.7 kw Three Phase Interleaved Case: V_{in} = 310V, V_{out} = 660V, Power = 6.78 kw, Efficiency = 98.007%

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

This thesis work has built upon the design and implementation of the first phase of the EV-STS project wherein a DC/DC converter was proposed for EV drivetrains. The single module DC/DC converter has been analyzed and tested followed by a complete, elaborate analysis, simulation, design and hardware implementation of the Gen-II prototype. Comprehensive literature review was carried out to ascertain the advantages of a flexible DC-Link within the EV drivetrain. These included independent optimization of the drivetrain components, including the battery stack, the inverter and the motor itself. The interleaved synchronous boost topology was chosen to realize the DC/DC converter over other topologies such as single phase boost and isolated full bridge topologies. The advantages of interleaving were analyzed and concluded that the impact of interleaving in terms of reduction of passive component sizes, current splitting, reduction in voltage stress and increase in effective frequency all contributed to better efficiency and power density of the converter. These two objectives of the project were further aided by the selection of SiCFET switches that inherently perform better than Silicon switches as far as efficiency, thermal conduction and power density is concerned. High efficiency was also ensured through a soft switching scheme for all main switches in each phase of the interleaved topology. Soft switching was implemented through an auxiliary branch with two auxiliary switches and an auxiliary inductor. The power pole capacitance in each phase determined

the designed value of the auxiliary inductor and this determined the timing of the auxiliary branch turn on and turn off with respect to the turn on of the main switch in each phase. The resonance of the auxiliary inductor and the power pole capacitance allowed the main switch capacitance to discharge through the auxiliary branch and allow for ZVS of the main switch. The synchronous switch underwent natural ZVS and the auxiliary switches were turned on and off during zero current in the auxiliary branch so no switching losses were incurred in the auxiliary branch either. This scheme helped improve converter efficiencies to beyond 98% in all test cases and justified the proposal of incorporating a DC/DC converter in the EV drivetrain architecture.

5.2 Future Work

The interleaved converter implemented as part of this thesis work has not yet been tested for the regenerative braking mode of operation. These tests will be carried out as part of the same project and efficiencies over 98% are expected. Once the all topological tests are concluded at 10kw power, the next steps will include pushing the interleaved topology to higher power as it is designed for a rating of 30kw. Rated power tests will be carried out for both the boost and buck modes of operation and 98% efficiencies will be targeted by ensuring adaptive ZVS at higher powers as well. The last endeavor towards the completion of the project will be to implement closed loop inductor current control.

REFERENCES

[1] Bloomberg NEF, “Electric Vehicle Outlook 2018,” *Bloomberg New Energy Finance*. [Online]. Available: https://about.bnef.com/electric-vehicleoutlook/#toc-download [Accessed 6 Jun. 2018].

[2] US EPA, “Global Greenhouse Gas Emissions Data,” [Online]. Available: https://www.epa.gov/ghgemissions/global-greenhouse-gas-emissions-data#Sector [Accessed 6 Jun. 2018].

[3] M. A. Sakka, J. V. Mierlo and H. Gualous, “DC/DC Converters for Electric Vehicles*,” in IntechOpen*, 2011.

[4] H. N. de Melo, J. P. Trovão and P. G. Pereirinha, "Batteries usability for Electric Vehicle powertrain," *Proceedings of the 2011 3rd International Youth Conference on Energetics (IYCE)*, Leiria, 2011, pp. 1-7.

[5] A. F. Burke, "Batteries and Ultracapacitors for Electric, Hybrid, and Fuel Cell Vehicles," *in Proceedings of the IEEE*, vol. 95, no. 4, pp. 806-820, April 2007.

[6] A. Baltatanu and L. M. Florea, “Comparison of Electric Motors used for Electric Vehicles Propulsion,” in International Conference of Scientific Paper AFASES 2013.

[7] J. Lemmens, J. Driesen and P. Vanassche, "Dynamic DC-link voltage adaptation for thermal management of traction drives," *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, 2013, pp. 180-187.

[8] M.Rashid, *Power Electronics Handbook.* New York: Academic, 2010.

[9] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson and M. Christopher, "The changing automotive environment: high-temperature electronics," *in IEEE Transactions on Electronics Packaging Manufacturing*, vol. 27, no. 3, pp. 164-176, July 2004.

[10] D. M. Bellur and M. K. Kazimierczuk, "DC-DC converters for electric vehicle applications," *2007 Electrical Insulation Conference and Electrical Manufacturing Expo*, Nashville, TN, 2007, pp. 286-293.

[11] M. A. Sakka, J. Van Mierlo, H. Gualous and P. Lataire, "Comparison of 30KW DC/DC converter topologies interfaces for fuel cell in hybrid electric vehicle," *2009 13th European Conference on Power Electronics and Applications*, Barcelona, 2009, pp. 1-10.

[12] B. K. Bose, "Need a Switch?," in *IEEE Industrial Electronics Magazine*, vol. 1, no.

4, pp. 30-39, Winter 2007.

[13] T. Schoenen, M. S. Kunter, M. D. Hennen and R. W. De Doncker, "Advantages of a variable DC-link voltage by using a DC-DC converter in hybrid-electric vehicles," *2010 IEEE Vehicle Power and Propulsion Conference*, Lille, 2010, pp. 1-5.

[14] K. K. Prabhakar, M. Ramesh, A. Dalal, C. U. Reddy, A. K. Singh and P. Kumar, "Efficiency investigation for electric vehicle powertrain with variable DC-link bus voltage," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 1796-1801.

[15] S. Tenner, S. Gimther and W. Hofmann, "Loss minimization of electric drive systems using a DC/DC converter and an optimized battery voltage in automotive applications," *2011 IEEE Vehicle Power and Propulsion Conference*, Chicago, IL, 2011, pp. 1-7.

[16] X. Jia, C. Hu, S. Du, M. Chen, P. Lin and D. Xu, "DC-link voltage control strategy of a bi-directional DC/DC converter for electric vehicles," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 92-99.

[17] N. Zhao, N. Schofield, R. Yang and R. Gu, "An investigation of DC-link voltage and temperature variations on EV traction system design," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-8.

[18] J. O. Estima and A. J. Marques Cardoso, "Efficiency Analysis of Drive Train Topologies Applied to Electric/Hybrid Vehicles," *in IEEE Transactions on Vehicular Technology*, vol. 61, no. 3, pp. 1021-1031, March 2012.

[19] K. Berringer, J. Marvin and P. Perruchoud, "Semiconductor power losses in AC inverters," *Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE*, Orlando, FL, 1995, pp. 882-888 vol.1.

[20] T. Burress, "Benchmarking state-of-the-art technologies," Oak Ridge National Laboratory (ORNL), 2013 U.S. DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting.

[21] S. Küttler, K. E. K. Benkara, G. Friedrich, F. Vangraefschèpe and A. Abdelli, "Impact of the field weakening on the iron losses in the stator of an internal permanent magnet synchronous machine," *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, 2014, pp. 4188-4195.

[22] A. Bakeer and A. A. Ahmed, "Performance evaluation of PMSM based on model predictive control with field weakening operation and bidirectional quasi Z-source

inverter," *2017 Nineteenth International Middle East Power Systems Conference (MEPCON)*, Cairo, 2017, pp. 741-746.

[23] R. Yang, "Electrified vehicle traction machine design with manufacturing considerations," Ph.D. thesis, McMaster University, Hamilton, Ontario, 2016.

[24] R. Ayyanar, "Zero-voltage transition in power converters with an auxiliary circuit," US patent application, January 2014.

[25] S. Kulasekaran, R. Ayyanar, "A 500kHz, 3.3kW Power Factor Correction Circuit with Low-Loss Auxiliary ZVT Circuit," *IEEE Transactions on Power Electronics*, 2017, IEEE Early Access.

[26] C. Nan and R. Ayyanar, "A high frequency zero-voltage-transition (ZVT) synchronous buck converter for automotive applications," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-6.

[27] Y. Xia, R. Ayyanar, "Naturally Adaptive, Low-Loss Zero Voltage Transition Circuit for High Frequency Full Bridge Inverters with Hybrid PWM," *IEEE Transactions on Power Electronics*, 2017, IEEE Early Access.

[28] Ferroxcube design tool. [Online] Available: https://www.ferroxcube.com/englobal/design_tool/index [Accessed 10 Mar. 2018].

[29] Wolfspeed inc. 2015. [Online]. Available: http://go.wolfspeed.com/all-models

[30] CREE, "Silicon Carbide Power MOSFET," C2M0025120D datasheet, Oct. 2015.

[31] CREE, "Silicon Carbide Power MOSFET," C2M0080120D datasheet, Oct. 2015.

[32] AVX, "Medium Power Film Capacitors," FB37M6P0106 datasheet, Jun. 2015.

[33] Spectrum digital inc. 2003. [Online]. Available: http://www.spectrumdigital.com