Enhanced circuit for linear ring VCO-ADCs

J. Borgmans✉ and P. Rombouts

Recently an extremely linear voltage-controlled ring-oscillator for use in VCO-ADCs was proposed by Babaie-Fishani and Rombouts. In this current Letter, a circuit-level technique to improve the bandwidth and noise performance of such a linear VCO is proposed. The key element is the modified delay cell, where the traditional cross-coupled inverters are modified into 'feed-forward' coupling inverters that pre-charge the subsequent elements in the ring. The resulting circuit maintains the excellent linearity, but has greatly enhanced bandwidth (up to 3 times higher) and considerably reduced power for the same circuit noise level (up to 2.5 times lower).

Introduction: With continuously decreasing feature sizes, conventional building blocks for analogue-to-digital (A/D) converters, such as operational amplifiers, transconductors and comparators, are becoming increasingly challenging to design. In addition, these analogue circuits have poor portability to other technology nodes. For this reason, researchers have attempted to find more 'digital' solutions for A/D conversion. This triggered an evolution from voltage- to time-domain based conversion techniques. A development in this evolution is the voltage-controlled oscillator (VCO)-based A/D converter [1–3]. An important limitation of this VCO-based A/D conversion is the poor VCO linearity. In [1] a substantial improvement regarding this linearity issue was made by using a circuit-level optimisation approach. In this work, we propose a further improvement over this prior work in terms of power efficiency and speed.

First-order high-speed VCO-ADC: The performance of first-order VCO-based ADCs is well understood [2]. Several parameters are known to affect the performance. Using a higher sampling f_s, as well as using a higher voltage-sensitivity k_v together with a higher effective free-running frequency $f_{0,\,\mathrm{eff}}$, both improve the performance. Here, the effective free-running frequency is defined as the free-running frequency of the VCO multiplied with the number of VCO phases [4]. From this, it is clear that it is beneficial to increase the speed of the delay cell in the ring VCO: a faster delay cell allows to increase f_0, or alternatively to add more delay cells (increasing the number of VCO phases) while maintaining the same f_0. Both these strategies result in a higher effective oscillation frequency, increasing the VCO-ADC performance. In this Letter, we propose a new delay cell which is faster, more power efficient and exhibits better noise characteristics than the prior art [1].

Novel delay cell: The resistive input network of the highly linear voltage controlled ring-oscillator (RO) of [1] is shown in Fig. 1*b*, which is used to tune the VCO with N delay stages (Fig. 1*a*). A key element of this VCO is the delay cell. The prior art solution of [1] is depicted in Fig. 2*a* and consists of a differential circuit with two main inverters with a weight M and two cross-coupled auxiliary inverters with a weight of one. Upon further inspection of the circuit, it was observed that these auxiliary inverters are bad for performance. First, the current used in these inverters is entirely wasted in terms of the oscillation frequency and in fact, even reduces the oscillation frequency. Secondly, during the charging phase, the inverters are always biased in triode, which is detrimental for the noise performance of the delay cell [5].

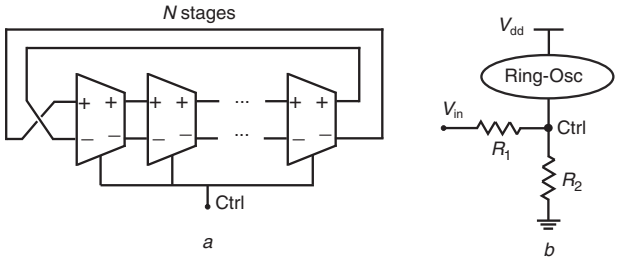

Fig. 1 *Extremely linear voltage-controlled ring-oscillator from [1]*
a Delay cell based ring-oscillator
b Resistive voltage control of the RO

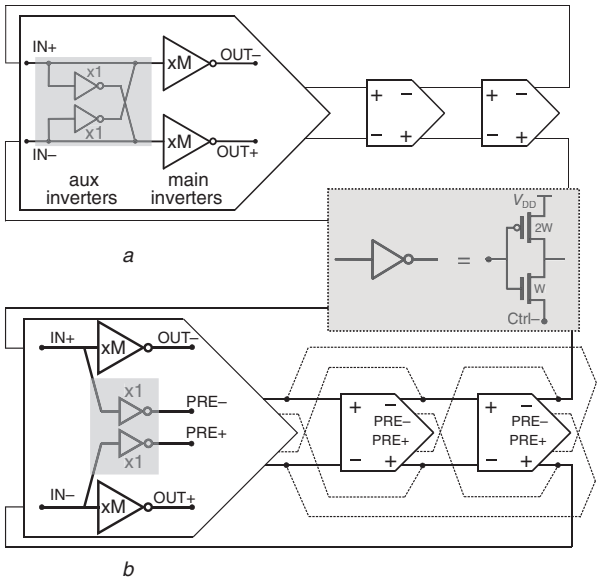

Fig. 2 *Three-stage voltage-controlled ring-oscillator*
a based on the prior art delay cell used in [1] and
b based on the proposed delay cell
Note: the prior art delay cell is drawn differently as in [1] for comparison purposes

Despite these flaws, the auxiliary inverters are necessary to ensure the differential behaviour of the ring oscillator [1, 3, 6]. The question that arises here is how strong they need to be with respect to the main inverters: i.e. what is the best value for the parameter M (see Fig. 2)? From a performance optimisation standpoint, the auxiliary inverters should be as weak as possible, to maximise the oscillation frequency and to optimise the noise characteristics of the circuit (i.e. M should be large). In contrast, the literature recommends that M should be small (close to unity) [3] to improve the circuit's robustness against mismatch and to guarantee that no oscillation failure can occur. However, based on the measurements reported in [1], it appears that the value of M could be increased to 4, sacrificing robustness for performance. But even then, the (unavoidable) auxiliary inverters still limit the performance. This begs the question whether a smarter cross-coupling could be inserted. In answer to this question, we propose the solution shown in Fig. 2*b*. Here the auxiliary inverters are used to create a feed-forward cross-coupling. This pre-charges the output of the subsequent delay cell, increasing the f_0 without incurring a current consumption penalty. A similar idea was developed for a VCO aimed at phase-locked loop (PLL) applications in [6]. However, unlike our proposed solution, the circuit of [6] is unsuitable as VCO-ADC as its linear tuning range and its k_v are far too small. Moreover, our proposed solution has superior noise characteristics compared to the prior art [1]. On the contrary, for the delay cell in [6], the noise performance is worse than the prior art.

Design example: To compare the novel delay cell with the prior art, a first-order VCO-ADC with a bandwidth of 10 MHz in a 40 nm CMOS technology with a 1.1 V power supply was designed. First, the high-performance (but low robustness) case of $M = 4$ was focussed on, where the main inverter is made 4 times as strong as the auxiliary inverters. To this end, the prior art 65 nm CMOS design from [1] was scaled to 40 nm CMOS. The resistors in the resistive input network (Fig. 1*b*) are chosen equal $R_1 = R_2 = R$. For both designs, the value of R is sized to obtain the same noise performance within the bandwidth of 10 MHz. The number of delay stages for the new VCO structure is selected in order to produce a free-running frequency of $\sim$ 600 MHz, with $k_v = 1.13$ GHz/V, which resulted in a design with $N = 8$, resulting in 16 VCO phases.

In order to achieve a fair comparison between both VCO designs, the number of stages for the prior art VCO is sized to result in an equal f_0 and k_v for a mid-rail input bias level. The result was a VCO design with $N = 5$ delay stages. Hence, there are only 10 VCO phases instead of 16, leading to an expected 4 dB worse signal-to-quantisation-noise ratio (SQNR). The circuit noise level for both designs was designed 6 dB below the quantisation noise level to

illustrate the improved quantisation noise performance of the new technique. This resulted in a resistance of $R = 1\,\text{k}\Omega$ for the proposed VCO while a lower resistance of $R = 0.81\,\text{k}\Omega$ was needed for the prior art design. Moreover, in spite of the smaller amount of delay cells, the prior art design consumes 30% more power than the new structure: 0.68 versus 0.86 mW. This is due to the inferior noise performance of the prior art delay cell, and by considering the fact that the phase noise improves with more delay cells in the design [5].

For evaluation, both VCOs are embedded in a pseudo-differential first-order VCO-ADC architecture as in [1]. Here, two identical VCOs are driven with a differential input signal atop a mid-rail common mode voltage (0.55 V). All the VCO phase signals are processed with an XOR-based readout circuit [2] with a sampling frequency of 1.2 GHz. Afterwards the outputs are subtracted.

We have designed the full layout of this circuit, but a test chip was not manufactured. Instead, we present simulation results gathered from an extracted view of the full layout with parasitic capacitors. We believe this is justified as the extracted simulation results for the circuit of [1] corresponded nearly perfectly with the measurements. Therefore we believe that these simulation results count as a proof-of-concept.

Fig. 3 shows the simulated input-referred non-linearity error, for both designs. For differential input signals up to 400 mV_{pp}, the input-referred non-linearity error is within ± 0.1 mV, enabling a signal-to-distortion ratio (SDR) of ~66 dB. From this figure, we observe that the linearity of both designs is almost indistinguishable. In conclusion, there is virtually no loss in linearity with our new technique.

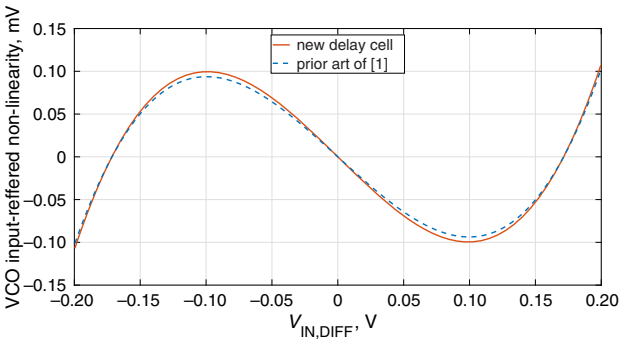

Fig. 3 *Input-referred non-linearity error for both VCO designs*

In another simulation, a 400 mV_{pp} differential input sine with a frequency of 500 kHz, is used to drive the pseudo-differential setup. In this, simulation transient noise is included. The output spectrum for the new circuit is shown in Fig. 4. The plot clearly illustrates the first-order spectral shaping and displays the attained signal-to-noise-and-distortion-ratio (SNDR) of 61 dB. The third harmonic is found at −66 dBc. As in [1], the second harmonic is suppressed by the pseudo-differential setup. The spectrum for the prior-art circuit is not shown, but looks very similar, with the same third harmonic at −66 dBc. However, the peak SNDR is only 58 dB now, due to its lower SQNR.

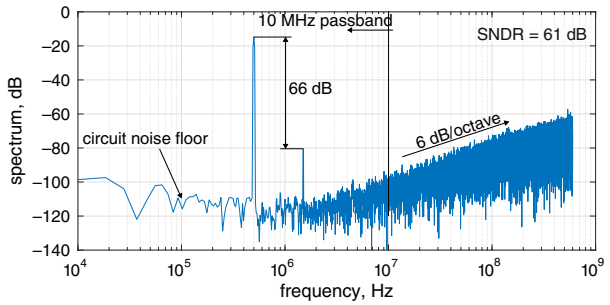

Fig. 4 *Simulated output spectrum of the new VCO in the pseudo-differential VCO-ADC architecture for the high-performance, low robustness case ($M = 4$)*

Similar simulations as that of Fig. 4 were performed to construct the dynamic range plot in Fig. 5. Here, a comparison is made between the VCOs by plotting the SNR, which is determined solely by the quantisation noise, together with the SNDR and SDR. From this plot, it is clear that, due to the difference in VCO phases, a 4 dB gain in performance is introduced in terms of SQNR, as expected.

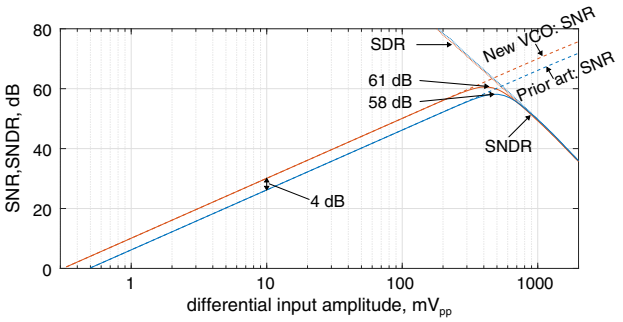

Fig. 5 *Performance comparison of the new VCO with the prior art for the high-performance, low robustness case ($M = 4$)*

Bandwidth comparison: An alternative approach to compare the prior art design with the proposed design, is by using the same amount of delay cells $N = 8$ and again scaling for a matching thermal noise performance. Then the bandwidth where the same peak SNDR of 61 dB is achieved, is determined. This evaluation is done for both the high robustness case ($M = 1$) and the high-performance case ($M = 4$), to showcase the trade-off between robustness and performance. The results are summarised in Table 1. The trade-off is very clear when considering the prior art, as a higher f_0 is obtained while using less power to result in the same SQNR. Also, when comparing the prior art to the proposed solution, the improved performance is unmistakeable. For the high-performance case ($M = 4$), the bandwidth is increased almost twofold, while requiring 30% less power. In the high robustness case ($M = 1$), the effect of the proposed technique is even more distinct. A threefold increase in bandwidth is observed, while consuming approximately 2.5 times less power. More importantly, when comparing the result for $M = 1$ with $M = 4$ for the new structure, it is observed that the performance in terms of bandwidth and power is nearly identical. This means that the trade-off where robustness must be sacrificed for performance is solved, and no compromise between the two has to be made.

Table 1: Bandwidth and power comparison of both VCO structures sized for a peak SNDR of 61 dB

		f_0 (MHz)	k_v(MHz/V)	R(kΩ)	BW(MHz)	P_{DC}(mW)
$M = 1$	prior art [1]	200	375	0.45	3.3	1.69
	this work	600	1140	1	10	0.69
$M = 4$	prior art [1]	380	700	0.81	6.3	0.87
	this work	600	1130	1	10	0.68

Conclusion: In this Letter, we have introduced a technique to improve the bandwidth and noise performance of extremely linear voltage-controlled ROs, such as the one proposed in [1]. The key element is the modified delay cell, where the traditional cross-coupled inverters are modified into 'feed-forward' coupling inverters that pre-charge the subsequent elements in the ring. The resulting circuit maintains the excellent linearity of [1] but has greatly enhanced performance. If the coupling inverter strength is chosen for optimal robustness ($M = 1$ as in [3]), the new solution offers a threefold increase in bandwidth at 2.5 times lower power. For a coupling inverter scaled for performance ($M = 4$ as in [1]), still an improvement of almost a factor of 2 in terms of bandwidth and 30% in terms of power is achieved. Additionally, we conclude our solution solves this trade-off between performance and robustness.

Acknowledgments: This work was supported by the Fund for Scientific Research Flanders (FWO-Vlaanderen), Belgium.

Submitted: *17 January 2019* E-first: *25 March 2019*
doi: 10.1049/el.2019.0241
One or more of the Figures in this Letter are available in colour online.

J. Borgmans and P. Rombouts (*Electronics and Information Systems Department, Ghent University, Ghent, Belgium*)

✉ E-mail: jonas.borgmans@ugent.be

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