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DTU Danchip
National Center for Micro- and
Nanofabrication

DTU

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Technology Development of 3D Silicon Plasma Etching Processes for Novel Devices and Applications

Presented to the Department of Physics at the
Technical University of Denmark, in partial fulfillment of the requirements for
acquiring the degree of Doctor of Philosophy
on October 31st, 2018

DTU Danchip
Technical University of Denmark

ACADEMIC DISSERTATION FOR DEGREE OF DOCTOR OF PHILOSOPHY

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To my parents

Abstract

Deep reactive ion etching (DRIE) is a standard technique for silicon micro- and nanofabrication in semiconductor industries. However, this technology is confronted with unprecedented challenges, as the critical dimension of structures is continuously shrinking following Moore's law, and various stringent technical requirements are becoming usual to enable emerging technologies and devices. Since there is still no other technique that can replace DRIE in a foreseeable future, profound process optimizations become a necessity for robust etching performances, high fabrication accuracies, more versatility and flexibility to enable complex structure manufacturing. As a typical strategy for DRIE, Bosch process has been studied extensively since last century, however, the high sidewall roughness induced by switched etching sequences make the process less favorable for nanoscale engineering.

In this thesis, a modified Bosch process has been proposed, which is termed as DREM (Deposit, Removal, Etch Method) process. Compared with a standard Bosch process, DREM process enables a much higher etching selectivity, more precise control over structure profiles, and less sidewall roughness. Various silicon micro- and nanostructures have been fabricated to demonstrate the capability of DREM process, e.g. silicon microstructure with aspect ratio of 50, nanostructures with aspect ratio of 26 and minimized sidewall roughness, etc. A modified DREM process is also developed for fabricating three dimensional (3D) silicon micro- and nanostructures. Up to 10 layers of suspended structures can be created conveniently by a single etching procedure, with a considerably better profile control compared with previous studies.

The fabricated 3D silicon micro- and nanostructures exhibit intriguing optical and mechanical properties. Two applications have been investigated: firstly, 3D silicon mesh structures are integrated with zinc oxide nanowires, and enhanced performances are observed for photocatalytic reactions and photocurrent generations; secondly, a 3D silicon photonic crystal membrane is fabricated, which possesses a complete photonic band gap, embedded planar cavities are also feasible for applications as organic solvent sensor and optical filters.

The above-mentioned technological developments are enabled by multiple real time monitoring techniques, such as optical emission spectroscopy and optical emission interferometry. Process optimizations have also been performed for electron beam lithography to achieve high resolution sub-10 nm patterns, which are employed for etching processes.

Resumé

Dyb reaktiv ion ætsning (DRIE) er en standard teknik i halvlederindustrien for fremstilling af silicium strukturer i både mikro- og nanoskala. Den veletablerede teknik står dog overfor store udfordringer i de nuværende forsknings- og produktionsaktiviteter, da strukurernes størrelse reduceres ned i nanoskala ifølge Moores lov, og specifikke tekniske krav bliver krævet for at kunne tilgodese den teknologiske udvikling. Da DRIE ikke kan erstattes af nye teknologier i en forudsigelig fremtid bliver procesoptimering en nødvendighed for robuste ætsningsprocesser, stor nøjagtighed i fabrikationen og fleksibilitet for produktion af komplicerede strukturer. Bosch proces er en typisk DRIE teknik, som er udviklet gennem de seneste årtier. I nanoskala er Bosch processen dog begrænset af tekniske ulemper på grund af overfladeruhed, som er fremkaldt af de skiftende ætsningsprocedurer under fremstillingen.

Denne afhandling drejer sig om en modificeret proces baseret på Bosch processen og kaldes DREM. (Depost, Remocal, Etch Method). Sammenlignet med en standard Bosch proces er der flere fordele ved DREM, fx. en højere ætsningsselektivitet, mere præcis kontrol af strukturernes profil og mindre overfladeruhed. I projektet er forskellige strukturer opnået med DREM processen i både mikro- og nanoskala for at demonstrere denne teknisk avancerede metode. Silicium mikrostrukture er fremstillet med en høj aspect ratio (dvs, højde divideret af bredde) på 50 og silicium nanostruckturer med en høj aspect ratio på 26 med en minimeret overfladeruhed. Baseret på DREM processen er en anden teknik udviklet for tredimensionel (3D) silicium struktur fabrikation. Op til 10 lag af løftede struktur kan blive fremstillet i en enkel proces, med forbedrede strukturkvaliteter i forhold til tidligere resultater fra andre forskningsgrupper.

De producerede silicium mikro- og nanostrukturer viser nogle interessante mekaniske og optiske egenskaber, som også bliver undersøgt i projektet. Først blev 3D silicium struktur integreret med zinkoxid nanotråd for forbedret effektivitet af fotokatalyse og fotoelektriske reaktioner. Dernæst blev fremstillet en 3D fotonisk krystalmembran og komplette elektriske energibånd som har bevist, at membranen kan bruges som optisk filter og sensor for organiske væsker.

Udførelsen af DREM proces er muliggjort gennem forskellige overvågningsteknikker, fx. optisk emissionsspektrometri (OES) og optisk emissionsinterferometri (OEI). Derudover er elektronstråle litografi også anvendt for en reduceret strukturstørrelse mindre end 10 nanometer.

Preface

This thesis has been submitted to the department of physics at Technical University of Denmark in partial fulfillment of the requirements for acquiring the PhD degree. The project has been carried out at Danish National Center for Micro- and Nanofabrication (DTU Danchip) from November 1st, 2015 to October 31st, 2018, funded by a DTU internal institute stipend.

During the three years of research and study, I have benefited from the encouragement and discussions from my supervisors, colleagues, friends and families, whom I would like to give acknowledgements to in the beginning of this thesis.

I would like to thank my supervisors, Henri Jansen, Flemming Jensen and Jörg Hübner for giving me the opportunity to pursue my academic dream in such a wonderful and vivid research environment at DTU Danchip. I have been spending a lot of cleanroom hours together with Henri seeking for the truths behind all the experiment results, not only did he share his experience and knowledge about micro- and nanofabrication to me, but also showed me a decent way to do scientific research. Whenever I have doubts about my project, Flemming and Jörg have always been available, thus I could feel reassured to move forward and make progress.

I cannot finish the project without the help and support from Danchip staffs. Tine Greibe guided me through various cleanroom techniques (especially on electron beam lithography), when I was still a rookie with zero cleanroom experience. Roy Cork and Martin Nørvang Kristensen have provided solid technical support to make Pegasus a happy horse. Jonas Michael-Lindhard has shared his insights on plasma etching, which is always helpful.

I would like to thank my collaborators, who helped me to broaden my mind and research horizons. Hongyu Sun at DTU nanotech inspired me with amazing new materials and their practical applications. I also benefited from in-depth discussions with fellow phd students and postdocs, e.g. Chen Zhou from DTU Nanotech, Yi Zheng from DTU Fotonik, Ding Zhao from DTU Danchip, Fei Ding and Yuanqing Yang from SDU.

In the last, I am deeply grateful to my parents for their endless love and support, without which I will not be able to achieve anything, even though I have mostly been thousands of kilometers away from them in the past three years.

Kongens Lyngby, October 31st, 2018

Bingdong Chang

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1 Introduction

Reactive ion etching (or ion enhanced plasma etching) is a standard technology for pattern transfer in semiconductor industries. Briefly speaking, etching gas species (e.g. SF_6, CHF_3, etc) are injected into a vacuum chamber and ionized (by radio frequency, microwave, etc), thus plasma is generated, containing ions and reactive radicals with high energy, and patterns defined by lithography can be transferred into wanted materials anisotropically. Since it was proposed in 1970s, [1, 2] reactive ion etching has been widely used to replace traditional wet etching method because of several advantages, such as anisotropic etch profiles, possibility to achieve high aspect ratio structures, clean process free from harzadous chemicals and particles, etc. However, reactive ion etching can be difficult to control compared with wet etching due to the complexity of etching mechanism and etching apparatus, therefore a much bigger parameter space is expected, and process optimization can be difficult without thorough understandings of etching process and system setup.

Types of lasma processes	With bias	Volatile etch product	Etch profile
Reactive ion etching	Yes	Yes	Anisotropic
Sputtering	Yes	No	Anisotropic
Plasma etching /plasma ashing	No	Yes	Isotropic
Plasma anodization (for O_2 plasma)	No	No	-

Table 1.1. A comparison of different plasma processes.

Based on the degree of ion bombardment (if the sample is on the target electrode) and if volatile etch products are produced, different types of plasma processes can be categorized as in **table 1.1**. Sometimes deep reactive ion etching (DRIE) is also referred, becaused of its large power generators and high plasma densities that enable a high etch rate for deep structures. Depending on the chemical properties, different materials can be etched with different etching species using reactive ion etching, e.g. silicon can be etched with fluorine-based species, while aluminum can be etched with chlorine-based species. In this thesis, we will focus on the technological development for etching silicon, which is a widely used semiconductor material in electronics and photonic industries, because of its appropriate bandgap (around 1.12 eV), high refractive index (around 3.88 @ 632 nm) and other superior properties. Although silicon etching techniques have been studied extensively before, there

are still some considerable challenges, when the industrial production and scientific research are constantly developing and pushing the limit of technologies.

One typical example is the semiconductor industries, where very-large-scale integration (VLSI) technologies are continuously shrinking the size of electronic devices (e.g. central process unit (CPU), random-access memory (RAM), etc) and benefit the society. The building blocks for integrated circuits (IC) by VLSI are the complementary metal–oxide–semiconductor (CMOS) transistors, or MOSFET (metal-oxide-semiconductor field effect transistors). Due to its high natural abundance, controllable doping process and other advantages, silicon is the mostly used material for MOSFET fabrications. Even though some novel materials have been proposed to replace the traditional FET design, [3, 4] silicon will still be the material for large scale fabrication in the foreseeable future. The density of transistors on IC chips are increasing following the Moore's law, [5] and the device sizes are shrinking drastically towards under 10 nm. However, this scaling is facing the challenge of broken down Dennard's scaling law, which suggests improved device performances and power consumption when the device size is scaling down. [6] In order to follow the pace of industries and overcome the technical barriers, plasma etching techniques need to be adapted and developed to solve some specific technical issues, e.g. to achieve a low sidewall roughness, to have a good geometry and size control of nanoscale structures, to reduce device damage from plasma processes, etc. Sometimes novel etching techniques can be applied for nontraditional FET designs, e.g. vertically integrated nanowire transistors, or gate-all-around vertical FET [7-11] are enabled by the three dimensional (3D) plasma etch process. Plasma etching is also a necessary technique for fabricating through-silicon vias (TSV) for 3D packaging. Compared with nanoscale FET fabrication, TSV have a larger critical dimension (CD) and higher tolerance for sidewall roughness, while the required etch depth is much larger (few hundred micrometers), thus a fast etch process is favored to achieve deep anisotropic profile. [12, 13]

By applying sophisticated fabrication technologies in semiconductor industries, silicon is also widely used in nanophotonics, optical communications and integrated photonic circuits. For example, owing to well-developed silicon-on-insulator (SOI) technology, silicon waveguide and optical resonators can be fabricated for biological sensor applications. [14, 15] Since the sensing performance is largely limited by the optical losses during light propagation, and roughness of fabricated structures contribute mostly to the scattering losses, thus it is crucial to create a smooth sidewall during plasma etching process for high quality factor (Q factor). [16] Other advanced applications for light manipulation, e.g. photonic crystals and metasurfaces, [17-19] also requires a well-defined geometry and small scattering loss from surfaces of silicon nanostructures. For applications like photovoltaics and solar cells, silicon nanostructures with deep etch profiles are preferred for trapping of incoming light, e.g. silicon nanowires [20] and "black silicon". [21]

For micro electro-mechanical systems (MEMS), nano electro-mechanical systems (MEMS), and the newly developed concepts of Micro opto-electro-mechanical systems (MOEMS) and nano opto-electro-mechanical systems (NOEMS), [22] sophisticated plasma etching techniques are also required. For example, capacitive accelerometers and gyroscopes normally use interdigital capacitor plates to sense external forces, and plates with larger surface area and smaller gaps are preferred in order to for a higher sensitivity, [23] this requires etching techniques that can achieve high aspect ratio (HAR) structures. For nanoscale optomechanical devices, [24] a precise control of etch process to minimize the roughness on structure surfaces is also a necessity.

Although specific requirements for etching performance need to be settled for different devices and applications, a fundamental issue during reactive ion etching is to have an anisotropic etch profile free from undercuts or sidewall corrosions. Since silicon can be etched spontaneously in a fluorine-based plasma (e.g. XeF_2 or SF_6), different techniques have been proposed to prevent this isotropic etching process for a desired etch profile. One popular technique is cryogenic etching, which was first introduced in 1988 [25] and has been studied extensively in the past years. [26] In cryogenic etching process, silicon substrate is cooled by helium to below -100 ˚C, and gas mixture of SF_6 and O_2 are applied, since ion-enhanced inhibitors of SiO_xF_y are covered on the sidewall, and the desorption is suppressed by the cryogenic temperature, thus the sidewall of structures can be protected from corrosion, and anisotropic etch profiles with smooth sidewalls can be achieved. Impressive etch results have been achieved with cryogenic etching for high aspect ratio structures and nanostructures, [27, 28] which is promising for fabrication of sensors and MEMS systems. [29, 30] However, this process is sensitive to substrate temperature and requires constant cooling at cryogenic temperature, which will in turn makes substrate into a "cryopump", where frozen compounds will fall on and become micromasks that are difficult to be removed. [31] These drawbacks make cryogenic etching not favorable for large scale industrial applications.

Bosch process was proposed shortly after cryogenic etching process, [32] and quickly become a widely used method for both scientific research and industrial productions. Instead of cryogenic temperature, Bosch process can be performed at room temperature, owing to C_4F_8, which is a much more efficient ion-enhanced inhibitor than O_2. When applying SF_6 and C_4F_8 in the same time, which is known as continuous process or pseudo-Bosch process, silicon can be etched with smooth sidewall while the aspect ratio is limited. By applying SF_6 and C_4F_8 subsequentially, also known as pulsed process, switched process or Bosch process, a much higher aspect ratio can be achieved, while the sidewall roughness is induced by the so called "scallops". Bosch process has already been successfully applied for microscale devices, where sidewall roughness is of less concern. [33, 34] However, for nanodevices with critical dimension of typically few hundred nanometers, the scallop sizes should be controlled to be below 20 nm or even below 10 nm, this sets technical challenges for process optimization and even hardware modifications are needed (e.g. fast mass flow controllers are installed to enable a fast switching process on PlasmaPro 100 Estrelas by Oxford Instruments, which are normally designed for atomic layer deposition).

Apart from the above etching techniques, which are mostly used, some novel etching technologies have been proposed. Atomic layer etching (ALE) is also a type of reactive ion etching, [35] which makes use of a self-limited chlorination on silicon surface in a chlorine-based plasma with a small bias, giving a monolayer of nonvolitile $SiCl_4$. The monolayer can then be removed by a mild argon ion bombardment. ALE is suggested to be able to control etch depth in atomic resolution and realize high pattern transfer fidelity. [36] However, the etch rate is limited and etching apparatus need to be modified, which limits the flexibility of this technique for various application purposes. Other etching techniques such as metal assisted chemical etching (MACE), [37] can realize ultrahigh aspect ratio nanostructures with low sidewall roughness, [38] however, this method is sensitive to multiple parameters, e.g. crystalline orientation of silicon, quality of metal masks, etc, thus the repeatability is undermined.

In this thesis, we will focus on process optimization for Bosch process, and novel applications will be explored with fabricated silicon micro- and nanostructures. A modified

Bosch process, called DREM (deposit, remove, etch method) process will be proposed, compared with traditional Bosch process, DREM process has the advantage of high etch selectivities, anisotropic etch profiles, minimized sidewall roughness caused by scallops, a much better control of etch processes and flexibility for process programming. By performing DREM process, combined with various lithography tools (e.g. high resolution electron beam lithography), we can achieve high aspect ratio (> 50) silicon microstructures, silicon nanostructures with smooth sidewall, and 3D silicon micro- and nanostructures with well-defined geometries. Applications of fabricated 3D silicon structures have been studied: e.g. 3D silicon nanostructures can behave like a 3D photonic crystal structures, and planar defects can be embedded for applications as optical bandpass filters and sensor of organic solvents; 3D silicon microstructures can increase the effective surface area, thus by integrating zinc oxide (ZnO) nanowires, the loading gain for photocatalytic performance and photocurrent generation can be improved.

The structure of the thesis is introduced as below:

- In chapter 2 we will discuss about pattern definition techniques that have been used in this study, especially electron beam lithography, which is an important technique to define nanoscale structures , we will show how process optimization was performed to achieve sub-10 nm high resolution patterns. Atomic layer deposition and its application will also be introduced.
- In chapter 3, plasma etching technique will be discussed in details, e.g. the basics of plasma etching process, how to characterize etching process with different parameters, etc. We will compare Bosch process and continuous mixed process, and introduce DREM process.
- In chapter 4, we will focus on the etching apparatus and different real time monitoring techniques, including high temporal resolution oscilloscope, optical emission spectroscopy (OES) and optical emission interferometry (OEI), we will see how these techniques can be used to optimize our etch processes.
- In chapter 5 we will show some state-of-the-art etching results, including HAR micro- and nanostructures, black silicon, and 3D micro- and nanostructures.
- In chapter 6, we will show some practical applications with 3D silicon structures.

2 General Introduction of Fabrication Methods

For a complete fabrication process of silicon micro- and nanostructures, there are several techniques that have been frequently used in this project. A brief summary is give as below:

- **Pattern definition**: Microscale pattern definition is performed with standard ultraviolet (UV) photolithography, while nanoscale patterns are defined by deep ultraviolet (DUV) stepper lithography or electron beam lithography (EBL);

- **Thin film deposition**: Electron beam evaporation has been used to coat thin metal films for lift-off purposes, thermal evaporation has been used for coating aluminum decharging layer before electron beam lithography, and atomic layer deposition (ALD) was used to deposit uniform thin films for different purposes.

- **Characterization**: optical microscope and scanning electron microscopy (SEM) have been used for structure inspections; atomic force microscopy (AFM) and profilometer have been used for structure surface characterizations and step height measurements; to analyze chemical element components of materials, energy-dispersive X-ray (EDX) spectroscopy, X-ray photoelectron spectroscopy (XPS) and X-ray diffractometry (XRD) have been performed; the thickness of thin film and optical properties are characterized with spectroscopic ellipsometry; wetting properties of sample surface are characterized with a drop shape analyzer.

- **Other treatment techniques**: different cleaning procedures are sometimes necessary for sample treatments, e.g. plasma ashing, RCA cleaning, Piranha solution cleaning, etc. Some simple thermal oxidation and thermal annealing processes have also been performed.

In this chapter, some of the techniques will be discussed in detail, especially the process optimization of electron beam lithography with HSQ resist, and optical applications with ALD deposited ZnO layer. While systematic analysis and discussions of reactive ion etching techniques will be elaborated in the following chapters.

2.1 OPTICAL LITHOGRAPHY

In order to create silicon structures with well-defined geometries, patterns need to be generated at the beginning of a fabrication process flow. The commonly used technique for pattern generations is optical lithography. Briefly speaking, substrates are first coated with polymers (named as photoresist) which contain photosensitive compounds, and then exposed by light, e.g. UV light from a mercury lamp or DUV light from an excimer laser. Depending on the photoresist chemistry, photon-induced chemical reactions can happen. Some kinds of photoresist can be degraded by light exposure and become soluble to certain chemicals (called developers), while some photoresists can be crosslinked and rendered stable during exposure, the former is called positive resist while the later called negative resist following the traditions. Depending on the mechanisms of exposure processes, optical lithography can be roughly categorized into contact lithography and projection lithography. For contact lithography, photomasks with designed light-shielding patterns are in contact with photoresist covered surface by vacuum or proximity mode; while for projection lithography, a lens system is used to capture a fraction of diffracted light from photomask. The main factors that limit the resolution of optical lithography are the wavelength of incoming light, numerical aperture of the optical system, and chemical properties of photoresist. [39]

In this project, different kinds of optical lithography tools have been used depending on the specific purposes, and some of the patterning results are shown in **figure 2.1**. For pattern generation on batch of samples, contact UV lithography is applied with Aligner MA-6 system (SUSS MicroTec Group), which is equipped with a 365nm UV lamp, and figure 2.1a shows arrays of holes (with diameter of around 5.5 µm) patterned by positive resist AZ MiR 701(Microchemicals GmbH).

To define patterns in a flexible manner for idea demonstration or prototype production, MLA100 maskless aligner (Heidelberg Instruments) has been used, which is a projection lithography system with 365 nm LED light source. In figure 2.1b are arrays of tuning fork structures patterned with negative resist AZ nLof 2020 (Microchemicals GmbH), each of the beams has a linewidth of round 1.5 µm. Since the exposure process in projection lithography is stepped between different writing fields, pattern nonuniformity and stitching errors can be noticed when defining large patterns (as shown in figure 2.1c). The patterns defined by maskless aligner can be easily used for different pattern transfer processes, e.g. plasma etching or lift-off. Figure 2.1d shows a simple electrode structure fabricated with maskless aligner followed by a lift-off process. The substrate used was borosilicate glass, 100 nm Au with 2 nm Ti adhesion layer are deposited by electron beam evaporation (Wordentec QCL 800 metal evaporator, Wordentec ltd).

While the feature size in UV lithography systems is limited by the wavelength of exposing light, in order to have patterns with a higher resolution, DUV stepper lithography was performed with a DUV stepper FPA-3000EX4 (Canon Inc.) equipped with a 248 nm KrF laser as light source. Patterns with sizes as small as 200 nm can be generated in a high throughput. In figure 2.1e are line arrays (linewidth of 1 µm) patterned with positive resist KRF M230Y (JSR Micro, Inc.). One of the advantages by DUV stepper lithography is the straight sidewall profile on resist patterns, which is shown in figure 2.1f. It should be noticed that a bottom anti-reflective coating (BARC) layer is applied beneath the resist layer to reduce pattern distortion caused by standing wave effects. The BARC layer we used is DUV42S-6 (Brewer Science, Inc.), which is a thermally crosslinked polymer that can be removed by O_2 plasma.

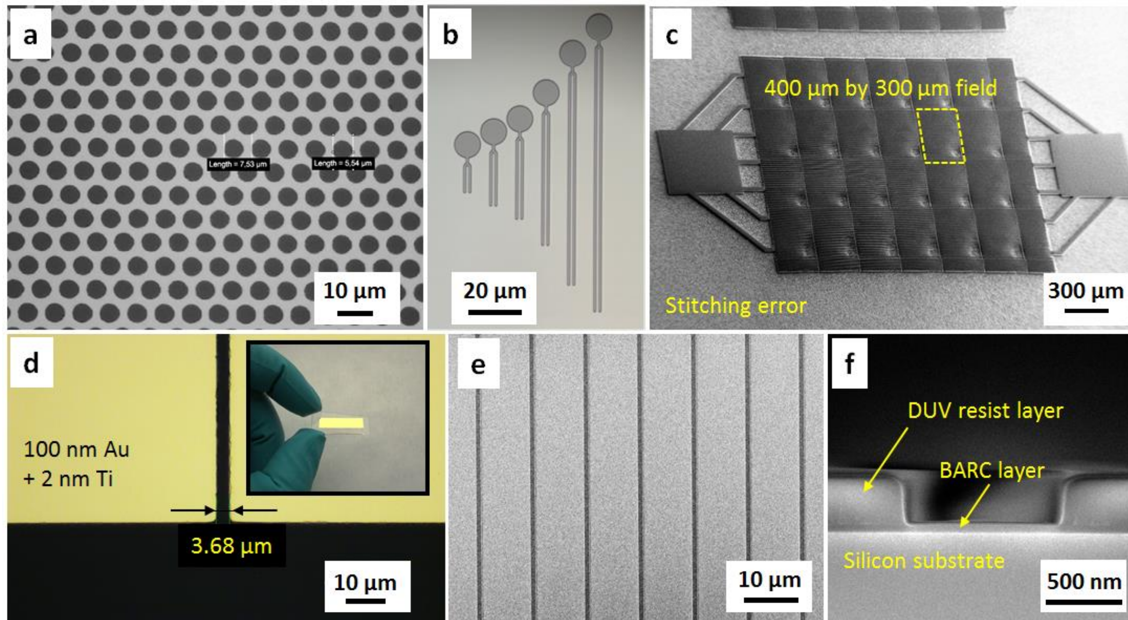


Figure 2.1. (a) Array of holes patterned by contact optical lithography; (b) Patterns generated by maskless aligner; (c) SEM image showing stitching error for large area patterning with maskless aligner; (d) Microgap fabricated by lift-off using maskless aligner generated patterns (inset: the whole chip); (e) SEM image of trench arrays defined by DUV stepper lithography; (f) Cross section the 1 µm wide trench patterns.

2.2 ELECTRON BEAM LITHOGRAPHY

For patterning nanostructures with feature size below 200 nm, electron beam lithography has been performed with a Jeol JBX9500 electron beam writing system (Jeol ltd.). Briefly speaking, free electrons are generated by a thermal field emission electron gun with an acceleration voltage of 100 kV. The generated electron beam passes through aperture equipped with a high frequency beam blanker (100 MHz), and then be deflected and focused onto the stage using magnetic lens systems. [40] Main writing fields of 1 mm × 1 mm and subfields of 4 µm × 4 µm can be achieved with a good writing uniformity by a vector scan method. The amount of electric charges that is applied on a unit area of substrate is defined as Q, for a total writing area of A and average beam current of I, the exposure time can be estimated as $t = QA/I$ (apart of the exposure time, extra time consumption can also be caused by stage movement, cyclic calibrations and data transfer). Since the writing process is limited by a maximum blanker frequency of 100 MHz, electron beam shots are thus separated by a finite distance called pitch P, with a minimum of $P_{min} = \sqrt{\frac{I}{Qf_{max}}}$, with f_{max}=100 MHz. When the pitch is larger than the single shot size d, dot array patterns with period of pitch size can be defined, with each dot exposed with a single beam shot. This method is sometimes called single spot lithography or dots-on-the-fly, [41-43] and will be discussed in detail later.

Before e-beam exposure is performed, substrates need to be coated by polymers (named as e-beam resist) which are electron beam sensitive. The resolution and quality of the patterns are highly dependent on the resist properties. In **Table 2.1** is a summary of different kinds of e-beam resists that have been used in this project.

Resist	Tone	Critical dose range	Contrast	Etch selectivity	CD	developer
CSAR 62	Positive	100 ~ 200 μC/cm²	~ 12	~ 2	15 nm	AR 600-546
ZEP520A	Positive	200~ 300 μC/cm²	~ 9	~ 10	50 nm	ZEP N50
HSQ	Negative	10000~ 20000 μC/cm²	~ 20	~ 50	7 nm	TMAH
AR-N 7520	Negative	100 ~ 200 μC/cm²	~ 5	~ 2	40 nm	AR 300-47

Table 2.1. A comparison of different e-beam resists used in this study.

The critical dose Q_c is defined as the minimum dose that should be applied for a total exposure of e-beam resist. For a fixed beam current, HSQ can take a much longer exposure time due to its higher critical dose compared with other resist. Critical dose is also dependent on other parameters, such as resist thickness, soft baking time, developing time, etc. In order to describe the resolution of an e-beam resist, the thickness of remaining resist is measured after exposure with different doses, and a plot is made known as contrast curve. The slope of the curve is mathematically defined as $\gamma = 1/log_{10}(Q_c/Q_0)$ with Q_0 is the base dose. For resists with a high contrast, like HSQ, a high resolution limit and straight sidewall can be achieved, thus is favorable for dense patterns; while for low contrast resist, the contrast curve is flatter, thus is ideal for grayscale lithography. [44]

For negative resist AR-N 7520 (Allresist GmbH), the substrate can be coated with different resist thickness by using different spin coating speed as shown in **figure 2.2a**. Sometimes resist is diluted for a smaller thickness. The contrast curves for AR-N 7520 with different thickness are shown in figure 2.2b, generally speaking, a thinner resist will require a higher critical dose, since there is less exposure from backscattered electrons, which are generated during interactions between electrons and resist.

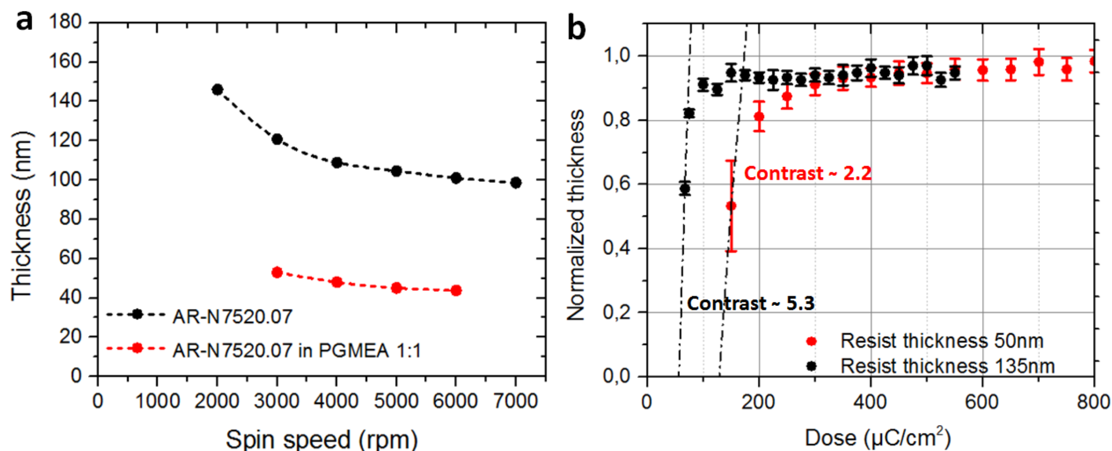


Figure 2.2. (a) Spin curves of AR-N 7520 and diluted AR-N 7520 to show the relation between spin speeds and final thickness of resist film; (b) Contrast curves of AR-N 7520 with different thickness.

As discussed earlier, the single spot lithography can be used to pattern dots with single beam shots. It is not only an efficient method for patterning dot arrays, but is also useful to study the focus and astigmatism of electron beam shots. [45] A simple test of single spot patterning is performed with positive resist CSAR 62 (Allresist GmbH) and negative resist AR-N 7520 (as shown in **figure 2.3**). The pitch size is fixed at 250 nm with a same beam current of 6.4 nA. It can be seen that the dot size increases with the dose applied, which is understandable, since the dwelling time of electron beams is increased for a higher dose, allowing for a more sufficient exposure of e-beam resist.

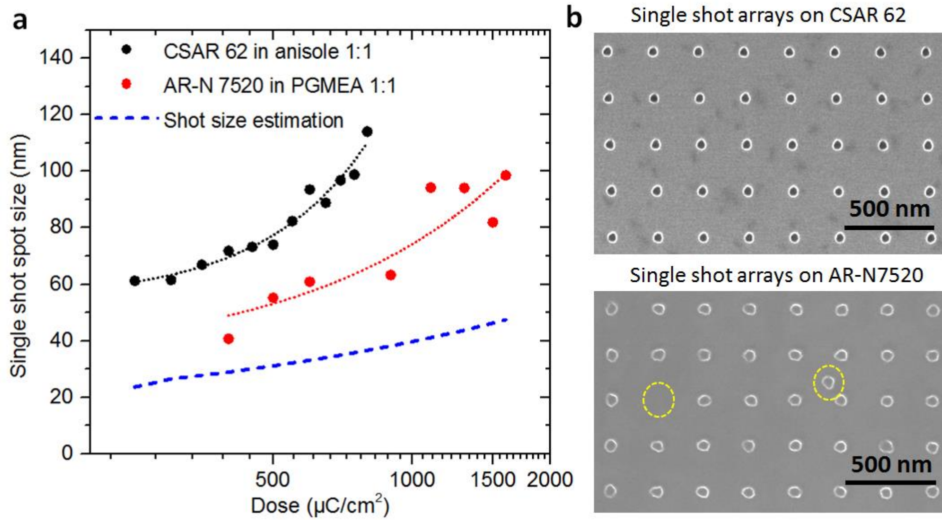


Figure 2.3. Single shot arrays with CSAR 62 and AR-N7520 resists. (a) Measured single shot sizes with different doses; (b) SEM images of single shot arrays on two resists, both with a pitch size of 250 nm.

Ideally, the single spot size d from an electron optics system can be estimated as below:

$$d = \left(\frac{4fQP^2}{\beta\pi\alpha^2} + \left(\frac{1}{2}C_s\right)^2 \alpha^6 + \frac{(0.61\lambda)^2}{\alpha^2} + \left(\frac{\Delta E}{E_0} C_c\right)\alpha^2\right)^{1/2} \quad (2.1)$$

In which α is the beam convergence angle, β is the brightness of electron beams, λ is the relativistical wavelength of electrons, which is around 4 pm for a 100 kV acceleration voltage. C_s is a coefficient accounting for the spherical aberration. C_c is the chromatic aberration coefficient with ΔE as the energy variation. [46, 47] The calculated spot size with (2.1) is plotted in figure 2.3a, which sets a lower limit of the dot sizes. The SEM images of exposed patterns are shown in figure 2.3b, we can notice that one of the dot seems to be shifted for AR-N 7520 resist, which might be due to a poor adhesion between resist and silicon substrate.

2.2.1 Proximity error correction (PEC)

A well-known phenomenon in e-beam lithography is the proximity effect, which can generate critical dimension variation, pattern nonuniformity and shape distortions. When materials are being exposed by electron beams, some backscattered electrons and fast secondary electrons can penetrate into the substrate surface with a depth of tens of microns, these electrons can be scattered back to the surface of e-beam resist, which will be exposed and the desired exposed area will be thus broadened. Lower acceleration voltage can be used to limit the penetration depth of incoming electrons, [48] and proximity error can be reduced, however, this will compromise the resolution limit. A more common strategy for proximity error correction (PEC) is to apply a dose modulation for different regions of patterns. Generally speaking, smaller patterns, isolated patterns and corner regions of the patterns will accept less exposure from backscattered electrons or fast secondary electrons, compared with large patterns, regions with high pattern density and center regions of the patterns. Thus a dose compensation can be assigned for the underexposed regions, and the correct size and shape can be achieved.

To illustrate how the dose compensation is performed, a simple simulation is shown in **figure 2.4**, in which dose intensity is simulated with and without PEC. The patterns are 5 lines with linewidth of 200 nm and period of 500 nm, and 5 lines with linewidth of 500 nm

and period of 1 μm (exposure substrate is set to be 100 nm HSQ on top of silicon wafer, with dose of 20000 μC/cm²). From the 2D map of dose intensity we can see that: without PEC, 200 nm lines are receiving less dose compared with 500 nm lines, the lines on the edge are underexposed compared with lines in the center. After PEC, the variation of doses is compensated, which can be clearly seen in figure 2.4b. 2% extra doses are assigned for 200 nm line, and around 1% extra doses are assigned for the lines on the edge. It should be addressed that depending on the specific patterns and the contrast of the resist, more than 10% dose compensation can be necessary sometimes. Other PEC strategies like GHOST, [49] can perform an extra exposure on the non-patterned areas with defocused electron beams, so the background exposure can be leveled.

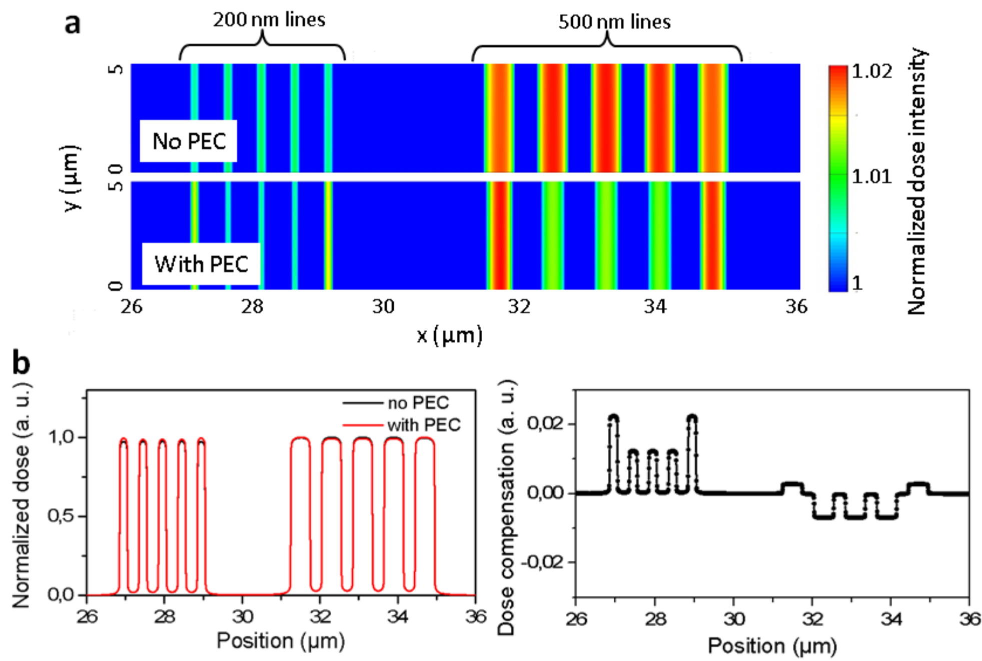


Figure 2.4. Dose compensation for PEC: (a) simulated dose intensity maps for patterns with and without PEC; (b) a 1D profile of the dose intensity with and without PEC (on the left), and the corresponding dose compensation (on the right).

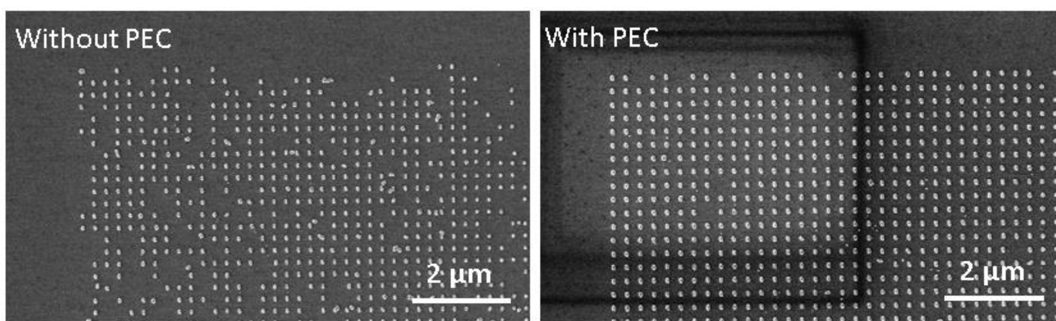


Figure 2.5. AR-N7520 dot arrays in the corner region with and without PEC.

A comparison of corner regions in dot arrays with and without PEC are shown in **figure 2.5**, the dots are patterned with AR-N7520, which has been shown earlier to have a bad adhesion with silicon substrate. The dots are patterned by a dot-on-the-fly technique, with a pitch size of 250 nm and dot diameter of around 50 nm. Since underexposure will reduce the cross linking degree of the resist, the dot structures in the corners will be more

vulnerable during developing, if no PEC is performed. However, when dose compensation is applied with PEC, most of the dots in the corner can still remain intact.

2.2.2 High resolution pattern definition

High resolution patterning with a critical dimension of around 10 nm or even below 10 nm is crucial for fabrication of devices like optical apertures and single electron transistors, and the resolution limit of lithography process is closely related to the physical and chemical properties of e-beam resist. HSQ is a negative tone e-beam resist that is widely used to fabricate high resolution patterns with low line edge roughness and sidewall roughness. By using a salty developer (e.g. 5 wt% NaCl in TMAH), a continuous bond breaking process of Si-O-Si network structures happens, and the resolution and contrast can be improved, [50, 51] even sub-5 nm structures has been reported before. [52] Since the dose contrast is high, it is especially favorable for patterning structures with small gaps [53, 54] and structures with complex geometries, such as metasurfaces and metalenses, [55, 56] etc. Besides, because of its silicon oxide-like structures, HSQ has a high etch selectivity that is comparable with thermal grown oxide (depending on the etch process, the selectivity can be over 100 to silicon). In this part we will discuss technical details and process optimizations when using HSQ for high resolution patterning.

The solvent of commercially available HSQ is methyl isobutyl ketone (MIBK), which has a relatively high vapour pressure of 19.95 mm Hg at 20 ˚C (other solvents of e-beam resists, such as PGMEA, has a lower vapour pressure of 3.7 mm Hg, and anisole has a vapor pressure of 3.54 mm Hg). [57] This will set some technical challenges during spin coating process. Since it always takes some time for spinner to reach target spin speed, and MIBK is constantly evaporize during the process and gives a high viscosity of the resist, thus the acceleration rate of spin coater can affect the final thickness of HSQ resist layer. In order to to find the optimum spin coating parameters, the thickness of HSQ resist was measured with different spin speed and different acceleration rate (the substrates were 4 inch silicon wafers, which were first baked out at 100 ˚C for 10 min, the spin coating time was 60 s, and the softbaking time was 80 ˚C for 4 min). We can clearly see from **figure 2.6** that a lower concentration of HSQ (2% for HSQ 1541-002) can generally give a thinner resist layer, while by increasing the spin acceleration rate, the film thickness can also be reduced significantly.

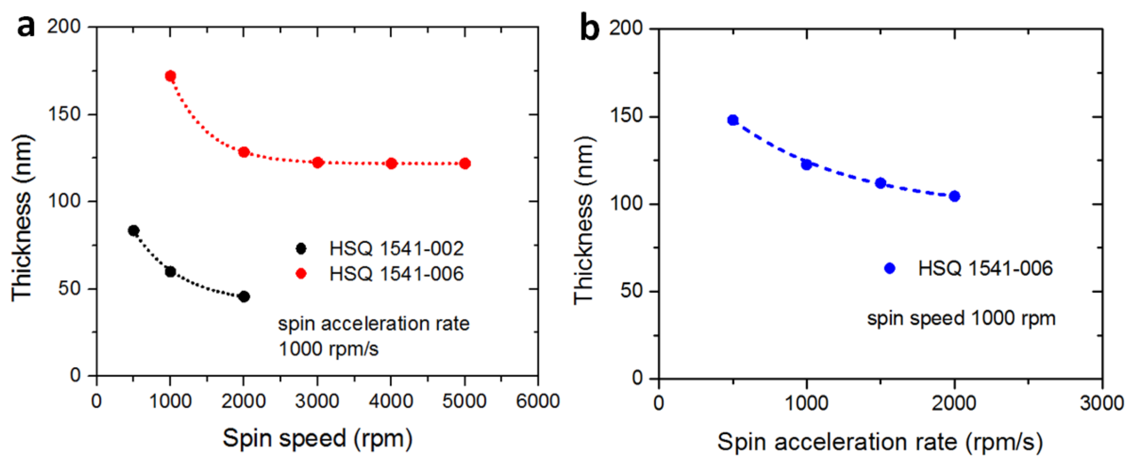


Figure 2.6. HSQ resist thickness with different spin speeds (a) and spin acceleration rates (b).

By reducing the thickness of HSQ film, we can sharpen the exposed area during e-beam lithography and thus achieve a higher resolution of the patterns. A Monte-Carlo simulation was performed with TRACER (GenISys GmbH) to calculate the electron energy density profile for 100 nm and 200 nm HSQ on top of silicon substrate (as in **figure 2.7a**). From the figure we can see, that for 200nm HSQ resist, there is a larger proportion of slow secondary electrons (corresponding to the yellow color), which are primary beams with reduced energies. The obtained energy density profile (or point spread function, PSF) was then fit with the sum of four Gaussian functions (as shown in figure 2.7b), assuming that electron scattering can be approximated as a Gaussian beam.

$$PSF(r) = \frac{1}{1+\eta+\upsilon_1+\upsilon_2}\left(\frac{1}{\pi\alpha^2}e^{-\frac{r^2}{\alpha^2}} + \frac{\eta}{\pi\beta^2}e^{-\frac{r^2}{\beta^2}} + \frac{\upsilon_1}{\pi\gamma_1^2}e^{-\frac{r^2}{\gamma_1^2}} + \frac{\upsilon_2}{\pi\gamma_2^2}e^{-\frac{r^2}{\gamma_2^2}}\right) \quad (2.2)$$

η, υ_1, and υ_2 are the proportion of backscattered electrons, secondary electrons and fast secondary electrons, α, β, γ_1 and γ_2 are the range parameters correspondingly. We can see that for 200 nm HSQ on top of silicon, the forward scattered electrons have a larger radical distance, besides, there is a large shoulder coming from secondary electron scattering (corresponding to a large υ_2 factor with a range parameter of 10 nm, as shown in **table 2.2**). Since the beam can be broadened by both forward scattered electrons and low energy secondary electrons, it is a preferable to use a thin layer of HSQ resist to pattern high resolution structures. However, in order to transfer the HSQ patterns into high aspect ratio silicon structures with plasma etching, the HSQ patterns should have enough thickness to sustain the continuous attack from ions and radicals. Here we also compared the fitted PSF between 50 nm HSQ and 100 nm HSQ on silicon substrate, and the results suggest that the difference of beam broadening is almost indistinguishable in these two cases. Thus 100 nm of HSQ resist will be mostly used in the study to achieve a good balance between pattern resolution and etching durability.

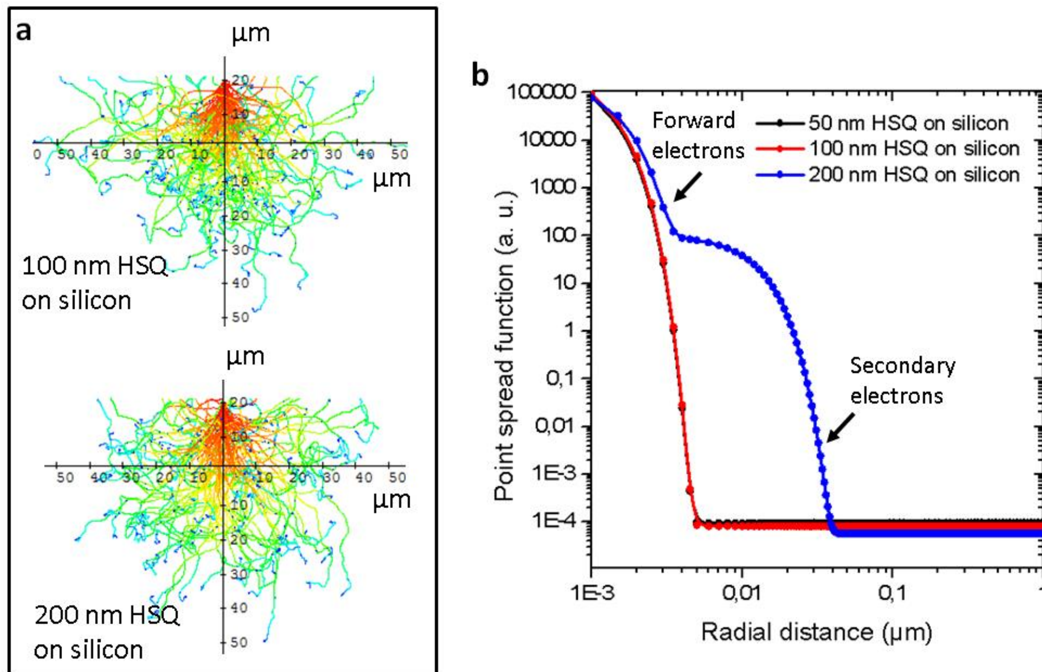


Figure 2.7. Monte-Carlo simulation of electron scattering in HSQ with silicon substrate (a), and fitted point spread functions (PSF) for electron scattering in HSQ with different thickness.

HSQ thickness (nm)	α (μm)	η	β (μm)	v_1	γ_1 (μm)	v_2	γ_2 (μm)
50	0.0010	0.2277	32.0221	0.2185	32.1365	0.0000	32.1365
100	0.0010	0.2449	27.5691	0.0000	7.5691	0.0000	27.5691
200	0.0012	0.3653	31.9715	0.0002	33.0399	0.0465	0.0101

Table 2.2. Fitted parameters of PSF for HSQ with different film thickness.

Design of experiment (DoE)

To define high resolution HSQ patterns with a reasonable reproducibility is a delicate process, since the resist has a relatively higher sensitivity to various processing parameters compared with other resists (e.g. ZEP 520 or CSAR). As discussed earlier, the spin coating acceleration rate can have a significant influence on resist thickness and thus accuracy of pattern dimensions, a longer softbaking time after spin coating can improve the crosslinking of resist, thus the resolution limit will be affected (for sub-10nm pattern definition with HSQ, some previous literature even suggested no softbaking at all, which however will increase the clear dose and reduce the throughput, in the same time there will be a risk for chamber contamination in e-beam writer). After exposure, a longer developing time can "cut" the tails of structure profile thus increase the contrast of patterns, however overdeveloping might also cause a "swelling" issue (increase of pattern size), which is quite common for negative tone resists. To reduce the residues caused by proximity error effect or developer, a higher temperature during developing might be needed. In order to judge which parameters have the most significant influence for the process, and if there is any coordinative effect between various parameters, a factorial experiment design was carried out, and analysis of variance (ANOVA) was performed. The summary of the parameter settings is shown as below in **table 2.3**,

Parameter number	Parameter	+	-
A	Soft baking time	4 min	2 min
B	Developing temperature	35 °C	Room temperature (22 °C)
C	Developing time	4 min	2 min
Fixed parameters: Resist: 100 nm thick HSQ 1541-006; Exposure current: 0.2 nA; Exposure dose: 20000 μC/cm²; Developer: AZ MiF 706 (with 4 wt% NaCl)			

Table 2.3. Parameter settings for a 2^3 factorial design of experiment

As shown above, three components are chosen, each of the parameters are assigned for two levels (+ and -). The exposed patterns are array of lines with a designed linewidth of 20 nm, the period is 40 nm (dense patterns) and 120 nm (isolated patterns). The linewidth was then measured by SEM after exposure. For the isolated patterns, the measured data are listed in **table 2.4**.

ANOVA is then performed and a F statistics is made to evaluate the factor effects, the interaction between different factors is also shown as in **table 2.5**. From which we can see that developing time has the most significant influence on the exposure results (with F_0 of

around 71.613), and the soft baking time has the least effect with F_0 of 28.493. The combination of different factors (AB, AC, BC and ABC) has a limited influence on the final results.

Run	Coded factors			Measured linewidth (nm)			Total	Notation
	A	B	C	#1	#2	#2		
1	+	+	+	28	23	23	74	abc
2	+	+	-	29	31	29	89	ab
3	+	-	+	27	27	26	80	ac
4	+	-	-	33	35	35	103	a
5	-	+	+	23	23	22	68	bc
6	-	+	-	28	29	26	83	b
7	-	-	+	29	25	26	80	c
8	-	-	-	30	32	30	92	1

Table 2.4. Data acquired for the 2^3 factorial design of experiment

Factors	Estimated effects	Sum of squares	Percent contribution	Degrees of freedom	Mean square	F_0
A	1.917	22.041	7.892	1	22.041	8.966
B	-3.417	70.042	25.078	1	70.042	28.493
C	-5.417	176.042	63.031	1	176.042	71.613
AB	0.083	0.042	0.015	1	0.042	0.017
AC	-0.917	5.042	1.805	1	5.042	2.051
BC	0.417	1.042	0.373	1	1.042	0.021
ABC	0.917	5.042	1.805	1	5.042	2.051
Error		39.332		16	2.458	
Total		318.625		23		

Table 2.5. Summary of effects from different factors

The results from ANOVA above can help us to further improve the exposure results. Since the soft baking time has the mildest effect on the exposure result, and it has a limited coordinative effect with other two parameters, thus we can reduce the soft baking time further to have a fine tuning of the final results (since increasing the soft baking time has a positive estimated effect as shown in table 2.3). If other two parameters (developing time or developing temperature) are changed, then a drastic effect should be expected, and we would lose track of process optimization. By reducing soft baking time from 2 min to 1 min, and keeping the other parameters the same, an improved exposure result was achieved with accurate dimension and a straight profile of lines, in the same time less residues are observed. By using the same procedure, some high resolution sub-10 nm patterns could be defined as shown in **figure 2.8**.

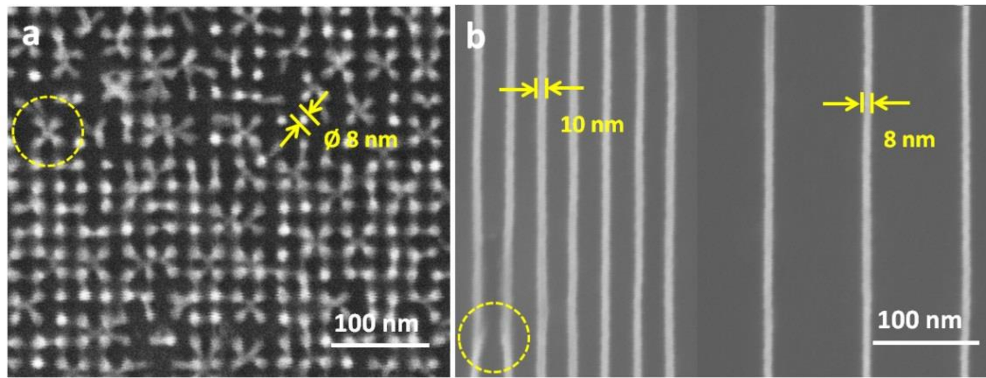


Figure 2.8. High resultion sub-10 nm HSQ patterns: (a) dot arrays; (b) line arrays with different periods.

It should be noticed that the HSQ resist has a thickness of 100 nm, since the pattern dimension is around or below 10 nm, such a high aspect ratio (> 10) will reduce the mechanical stability of HSQ structures. As shown in figure 2.8 inside the dash circles, these high aspect ratio HSQ structures can collapse to each other, possibily due to surface tension in the phase boundaries when the developer is drying from the gap between adjacent structures. This phenomenon is irreversible and can cause damage or even permanent collapse of the structures. [58] To avoid the problem, it is recommended to use critical point dryer, in which the structures are submerged in liquid CO_2, and the temperature slowly ramped up above critical temperature of CO_2 (where the gas phase and liquid phase can co-exist). Thus there will be no liquid/gas phase boundaries and the surface tension could be minimized, distortion of the structure morphology can thus be avoided. [59]

Improve HSQ process with hydrofluoric acid (HF)

As discussed earlier, HSQ resist suffers from cross linking issues in environment with high temperature or humidity, this process is irreversible and the reproducibility can be undermined, especially for high resolution patterns. These issues make HSQ less favorable for wider applications. To allow more flexibility in HSQ process, hydrofluoric acid (HF) was used before or after exposure to increase the pattern resolution.

Firstly, a thinner resist can reduce the beam broadening during e-beam exposure, however, the minimum resist thickness that can be reached with HSQ 1541-006 is around 100 nm (with maximum spin speed and spin acceleration rate that are allowed in our spinner), a lower concentration (e.g. HSQ 1541-002) can be used to achieve a thickness of 50 nm, however, it was observed that the low concentration HSQ normally gives patterns with a large line edge roughness, which is understandable, since the developing process is a Poisson process, and the probabilistic variation is inversely proportional to the concentration of exposed molecules. [60] Since HSQ contains inorganic fragments of O-Si-O, which can be etched chemically with HF, we can reduce the HSQ layer thickness in a controllable manner before exposure. By diluting HF with DIW in different concentrations, we can have different etch rate of spin coated HSQ layer, as shown in **figure 2.9a**, and the etch rate is proportional to the concentration of HF, suggesting a first order chemical reaction: reaction rate $\propto$ [HF]. It can be seen from figure 2.9b, that by applying 0.05 vol% HF, the thickness of unexposed HSQ layer can be reduced by 30 nm in 1 min. which is an appropriate etch rate to achieve a thin HSQ layer for high resolution pattering. When the concentration is 0.001 vol%, the etch rate is even lower 0.04 nm/s as shown in figure 2.9c.

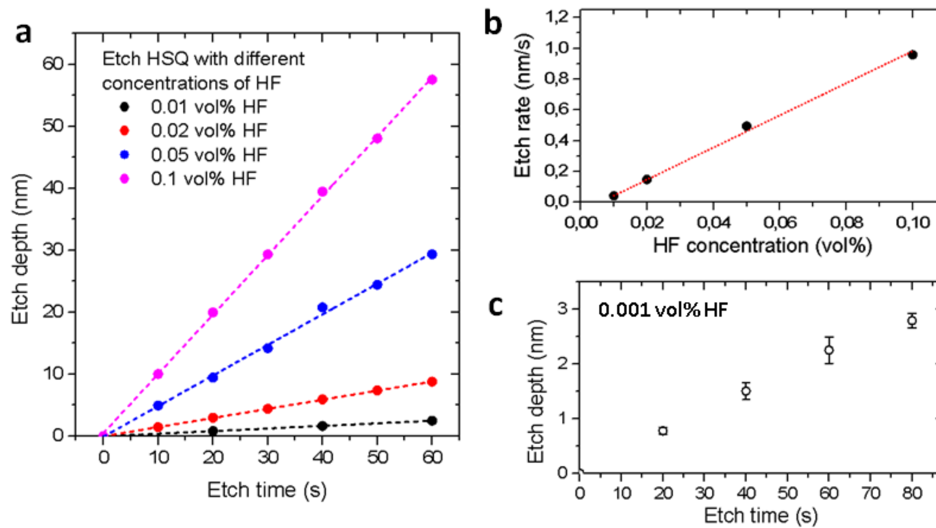


Figure 2.9. Etch rate of HSQ layer with different concentrations of HF.

HF can also be used after e-beam exposure to reduce the pattern size and to remove the residues (caused by proximity effect or insufficient developing). **Figure 2.10** shows some SEM images of HSQ high resolution line arrays. After exposure, the linewidth of isolated structures is around 12 nm, and 14 nm in dense structures due to the proximity effect. By using 0.05 vol% HF to etch the structures for 20 s and rinsed in DIW for 1 min, the linewidths reduce to 8 nm and 10 nm correspondingly. And a higher contrast on the edges could also be observed, implying that HF possibly cut the "tails" of structures. It should be noticed that the reduced etch rate compared with unexposed HSQ in figure 2.9 might be caused by a higher degree of crosslinking after e-beam exposure, and overetch with HF can cause structure collapse.

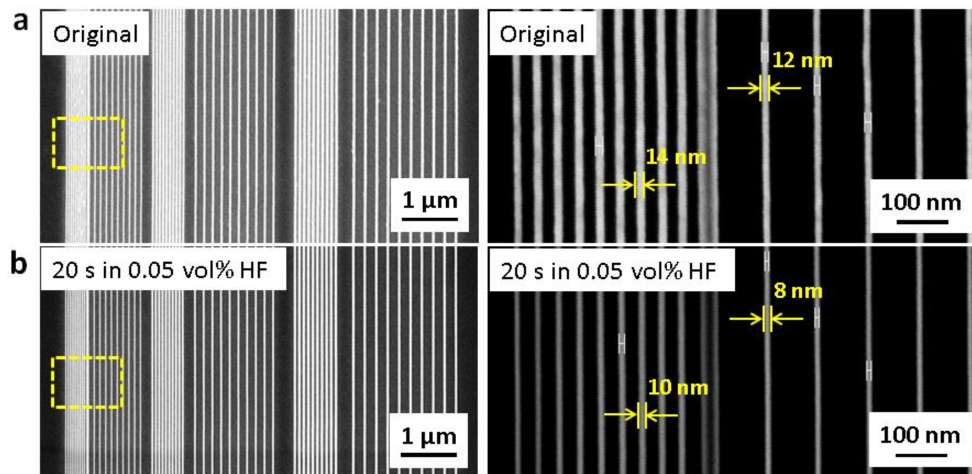


Figure 2.10. Using 0.05 vol% HF to thin HSQ line patterns.

2.2.3 Sidewall roughness characterization of patterns

The line edge roughness (LER) and sidewall roughness (SWR) are critical for patterns defined by e-beam lithography, since these roughness features could be transferred with a good fidelity into structures during lift-off or plasma etching, thus the performance of devices, like finFET, could be degraded because of the increased electron scattering on sidewall. While the line edge roughness is two dimensional information that can be easily

retrieved by image analysis from SEM inspection, sidewall roughness is three dimensional and needs special techniques to characterize, e.g. a flare tip og high aspect ratio tip for atomic force spectroscopy (AFM). Her we introduce a method that can be used to characterize sidewall roughness of resist patterns directly with traditional AFM tip. The principle is shown in **figure 2.11a**, firstly CSAR positive tone resist was spin coated with a thickness of around 200 nm, lines are then patterned with linewidth of 50 nm and 70 nm. Since the linewidths will reduce for overexposed patterns, these lines (with an aspect ratio up to 5) will collapse after developing, and a standard AFM scanning can be performed to characterize sidewall roughness directly. In figure 2.11b we can see the SEM images of collapsed lines (with linewidth of 50 nm) and upstanding lines (with linewidth of 70 nm), the exposure dose was 420 μC/cm². The scanning results suggests a root mean squared roughness (R_{RMS}, or R_q) of around 1 nm, depending on the dose and step size during e-beam exposure (a similar measurement was also done on HSQ structures, which also gives $R_q \sim 1$ nm).

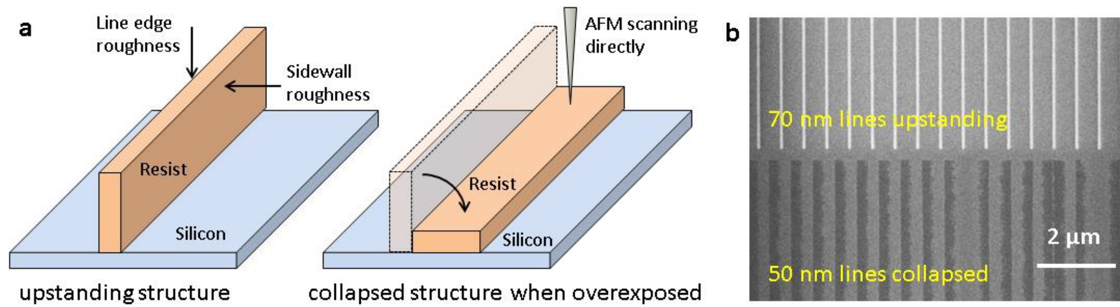


Figure 2.11. Sidewall roughness characterization of resist patterns: (a) A schematic view of the characterization method; (b) SEM images of collapsed 50 nm lines.

However, the measured R_q or R_a (arithmetical mean deviation) contains only statistical roughness information on the vertical direction. By performing a fourier transform of the height data in two dimensional surface, a whole spectrum of roughness could be obtained for different spatial frequencies, which is valuable information to study the light scattering on the sidewall or wetting behaviours on top of a surface. a two dimensional power spectral density (PSD) is defined as:

$$PSD(q_x, q_y) = \frac{1}{4\pi^2} \left| \int_{-\frac{L_1}{2}}^{\frac{L_1}{2}} \int_{-\frac{L_2}{2}}^{\frac{L_2}{2}} H(x, y) e^{-2\pi i x q_x} e^{-2\pi i y q_y} dx dy \right|^2 \quad (2.3)$$

In which q_x and q_y are the spatial frequencies in two surface directions. L_1 and L_2 are the dimensions in two directions, $H(x, y)$ is the two dimensional height map. The PSD has a unit of m⁴, while for one dimensional PSD, the unit will be m³. Here we will see how PSD can be used to study the relation between sidewall roughness and exposure doses. CSAR resist was exposed with 4 different doses: 420 μC/cm², 440 μC/cm², 460 μC/cm² and 480 μC/cm², and the sidewall roughness of lines (linewidth 50 nm) were measured using the above method. Although R_q measured for different doses are close to each other (1.1 nm ± 0.2 nm), the PSD shows evolution of surface roughness spectra when dose increases. In **figure 2.12a**, we can see that the spectral density for high spatial frequencies increases, while the intensity for the low spatial frequencies decreases with an increasing dose. This trend can be explained, since a higher dose can decompose and suppress the large polymer aggregates. [61] The surface morphology measured by AFM for different doses are also shown in figure 2.12b.

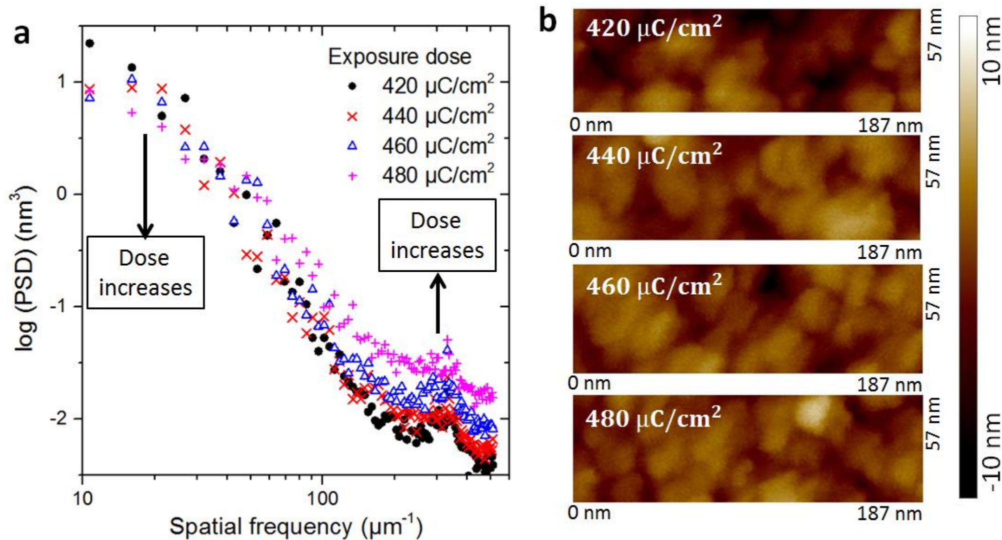


Figure 2.12. (a) Power spectral densities for sidewall profiles with different exposure doses; (b) Surface morphology of sidewall scanned by AFM.

2.2.4 Application with HSQ high resolution patterning

Here is an example of how HSQ high resolution patterning method is used to fabricate dielectric metasurfaces. The total metalense structure (with diameter of 50 μm) is composed of arrays of well-defined rectangular and elliptic units, each of the units have a size between 100 nm to 200 nm. Since the size and geometry are crucial to generate wanted phase change of incident light, it is quite important to define the patterns with a good resolution and transfer the patterns into silicon with a high shape fidelity. A process flow is shown in **figure 2.13**. Firstly, amorphous silicon with thickness of 500 nm was deposited on silica substrate by plasma enhanced chemical vapor deposition (PECVD), 100 nm HSQ 1541-006 was then spin coated for e-beam lithography. Since the silica substrate is a poor electric conductor which can distort the electron beam, 20 nm aluminum decharging layer is deposited by thermal evaporation. After e-beam exposure (beam current 6 nA and dose of 20000 $\mu C/cm^2$), the aluminum layer was removed with TMAH (with 4 wt% NaCl), which is also the developer for exposed HSQ patterns (with a developing time of 1 min). The patterns are then ready for plasma etching process (which will be discussed in details in the following chapters). The etching parameters of a Bosch etch process are carefully tuned, so that the etch rate of unexposed HSQ is around 3.8 nm/cycle, and a HSQ layer with omittable thickness is left after 25 cycles, while the silicon is fully etched. It should be noticed that, if the silicon is overetched, the straight profiles of silicon nanopillars will be destroyed due to the notching effect; if the silicon is not etched through, the transmittance of metalense will be compromised.

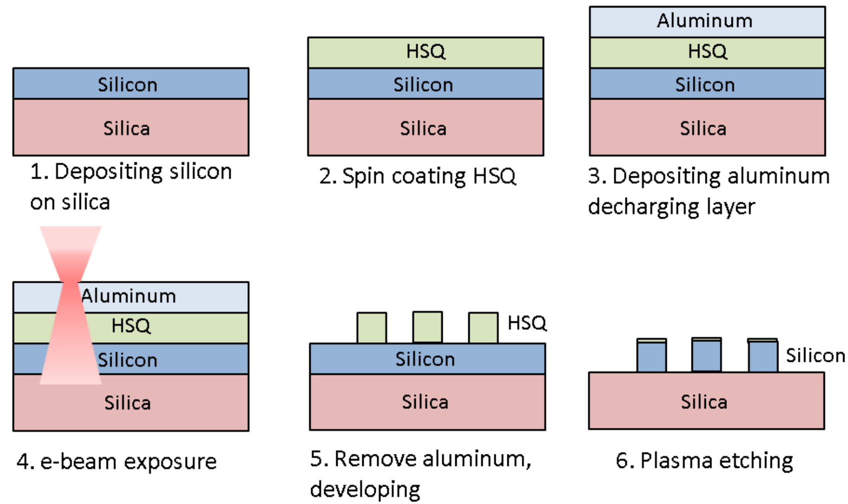


Figure 2.13. Process flow to fabricate dielectric metasurface.

The fabricated silicon metalenss are shown in **figure 2.14**, from the tilted SEM image we can see the directional profile of silicon nanopillars with well-defined geometries, which is attributed to the high resolution and etch selectivity of HSQ patterns. Besides, no residues or nanograsses can be observed on the silica substrate, which suggests a complete etching process. The bright field and dark field optical microscope image also shows a clean structure and substrate without unwanted residues.

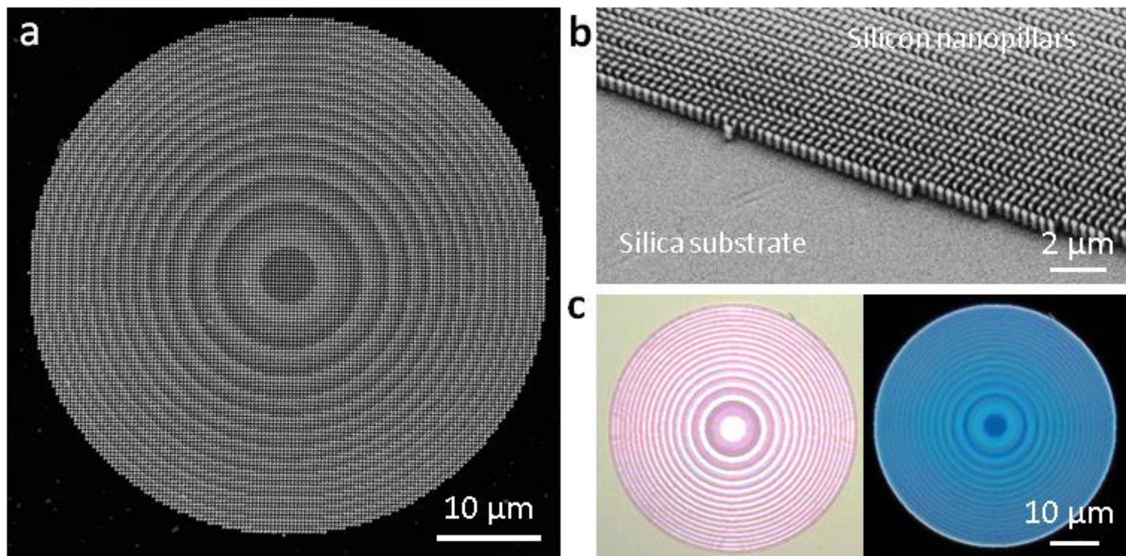


Figure 2.14. SEM images of fabricated metalense structures (a) top view and (b) tilted view; (c) Bright field and dark field view of fabricated metalense.

2.3 Atomic layer deposition (ALD)

Atomic layer deposition (ALD) is another technique that has been frequently used in this thesis for thin film deposition. Briefly speaking, vapor phase species (called precursors) are injected inside a vacuum chamber for self-limited surface reactions, leading to a binary growth of thin film on the sample surface. [62, 63] The deposition process is uniform and pinhole-free, and the film thickness can be controlled with a high precision at atomic or

monolayer level (however, a minimum thickness is normally required for a uniform coating). The growth process is uniform and conformal, thus is especially favorable for coating high aspect ratio structures or 3D structures. In this thesis, a thermal ALD system (Picosun R200) has been used, and three different materials have been deposited with ALD for different purposes:

- Aluminum oxide (alumina, Al_2O_3) is deposited on top of bare silicon wafer to be used as carrier wafers for etching small sample pieces. Since alumina has a high etching selectivity, the alumina coated silicon wafers can be used for many times as carrier wafers without being eroded by plasma, thus the effect from carrier wafer on etching experiments can be minimized. For this purpose, the film thickness is chosen to be between 100 nm and 200 nm to enable a longer lifetime of carrier wafers;
- Alumina is deposited on silicon samples before pattern definition with lithography. In this case, alumina will be used as a hard mask for etching micro- and nanostructures. For this purpose, the alumina thickness is chosen to be around 10 nm;
- Zinc oxide (ZnO) is deposited on silicon surface or 3D silicon structures as a functional material for photocatalysis and photocurrent generation. The thickness is chosen to be around 50 nm;
- ZnO is deposited on silicon surfaces for zeolitic imidazolate framework-8 (ZIF-8) particle transformation (which will be discussed later in the chapter);
- Titanium dioxide (TiO_2) is deposited on 3D silicon photonic crystal structures to tune the optical performance of structures. The film thickness is below 20 nm.

For thin film deposition with different materials as introduced above, the parameter settings are listed in **table 2.6** below, following the optimized recipes developed by engineers from DTU Danchip:

Deposited material	Temperature (°C)	Precursor #1	Time #1 (s)	Precursor #2	Time #2 (s)
Al_2O_3	200	TMA	0.1	H_2O	0.1
ZnO	250	DEZ	0.1	H_2O	0.1
TiO_2	200	$TiCl_4$	0.1	H_2O	0.1

Table 2.6. Parameters used in this thesis for ALD deposition of different materials (TMA: trimethylaluminium; DEZ: diethylzinc).

In the rest of the chapter, we will introduce an optical application with ALD deposited ZnO thin film, we will see how ZIF-8 nanoparticles can be grown from the ZnO seed layer, and the optical scattering properties will then be characterized and studied, this is reproduced from the authors' publication. [64] (Copyright 218 Wiley)

2.3.1 Structural colors of ZIF-8 crystals from ALD deposited ZnO

ZIF-8 is a type of metal-organic frameworks (MOFs) that have been widely studied in recent years due to their unique structures and applications in environment and energy. ZIF-8 possesses 3D zeolite crystal structures which are constructed by bridging zinc ions with methylimidazolate (MeIm) ligands. ZIF-8 crystals have large cavity sizes (11.6 Å), small connecting apertures (3.4 Å) and high thermal/chemical stability, endowing them outperform other MOF structures in a wide range of applications, including gas adsorption, [65] heterocatalysis, [66] low-κ dielectrics microelectronic devices [67] and The crystallization of ZIF-8 requires both zinc ion sources and imidazolate linkers. Traditional bulk synthesis methods use soluble zinc salts ($Zn(NO_3)_2$, $ZnSO_4$, $ZnCl_2$, etc) as zinc ion sources. [68, 69]

Nevertheless, the yielded powder-like ZIF-8 crystals are difficult to be integrated into MEMS or NEMS, where a mechanically robust structure is preferred. Recent studies show that ZnO nanostructures, e.g. nanoparticles or nanowires, can also be used as zinc ion sources for direct transformation of ZIF-8 crystals. For example, polycrystalline ZIF-8 thin film can be fabricated by converting ZnO layer grown either by ALD or sputtering. [70] Based on the compact ZIF-8 films, traditional top-down micro- and nanofabrication techniques, such as standard photolithography [71] and nanoimprint lithography, [72] can be used to pattern the ZIF-8 crystals in a regular manner. However, ZIF-8 structures fabricated using those lithography techniques are normally in colloidal forms aggregated by multiple ZIF-8 crystals and the critical dimension is normally in micrometer scale. A recent work [73] demonstrated the large optical nonlinearity of ZIF-8 material, making it a promising candidate for many emerging optical applications.

Here we will explore the resonant optical properties of wafer-based isolated ZIF-8 crystals at nanoscale dimensions. Briefly speaking, the ZIF-8 structures were converted from ZnO films deposited using ALD, and gold nanoparticles (Au NPs) were used to confine the crystallization of ZIF-8 structures, thus in a way "patterning" the ZIF-8 structures and thereby resulting in isolated ZIF-8 nanocrystals. The smallest size of the fabricated ZIF-8 crystals can be scaled down to ~100 nm with well-defined rhombohedral or rhombic dodecahedron morphologies. The synthesized ZIF-8 nanocrystals exhibited broadband scattering resonances in visible wavelengths, which gave prominent structural colors. Besides, an evident redshift of structural colors was observed when the sizes of single ZIF-8 nanocrystals increase. Such size-dependent resonant scattering behavior is of central importance for the applications in nanophotonics and bionanotechnology. [74]

2.3.1.1 ZnO deposition and ZIF-8 transformation

Figure 2.15 shows a schematic illustration of the process flow, in which three steps are included to fabricate ZIF-8 nanocrystals: firstly, growth of ZnO film was performed with ALD, the deposition parameter have been introduced earlier in the session, which can give a deposition rate of about 0.15 nm/cycle; [75] Secondly, dispersion of Au NPs (20 µL; average diameter 10 nm, stabilized suspension in 0.1 mM PBS, Sigma-Aldrich) with concentrations of 20%, 40% and 60% were dispensed on the top of deposited ZnO layer, The samples were left to be dried for 20 minutes, and then rinsed with deionized water (DIW) for 1-2 minutes to remove possible potassium chloride residues in the PBS buffer solution. The ZnO thin film was transformed into ZIF-8 crystals through solvothermal reaction. In a typical process, dimethylformamide (DMF, 45 mL) was mixed with 2-methylimidazole (0.2 g) and DIW (15 mL). ZnO thin films were then immersed in the mixed solution and placed inside a convection oven for 20 h at 75 °C. After the reaction, the samples were rinsed with DIW several times and dried for further characterizations.

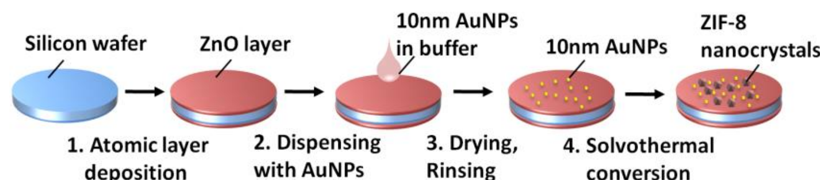


Figure 2.15. illustration of converting ZIF-8 nanocrystals from ALD grown ZnO layer, with steps of ALD, Au NPs dispensing and solvothermal synthesis.

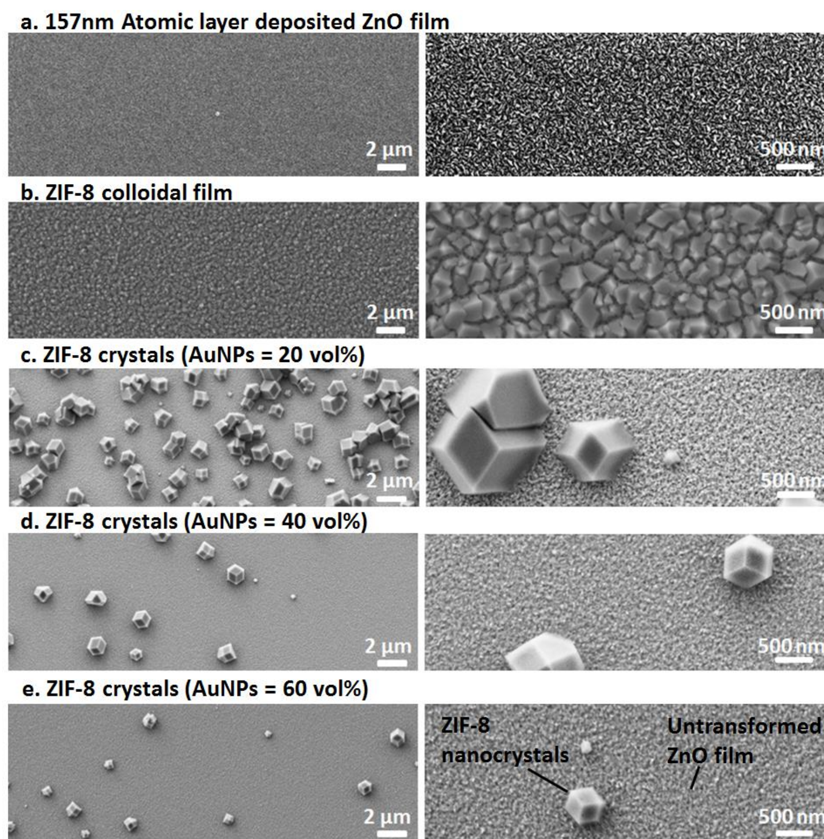


Figure 2.16. Low- (left column) and high- (right column) magnification SEM images of the samples. (a) 157 nm ZnO layer deposited by ALD on silicon substrate; (b) fully transformed ZIF-8 nanocrystals from ZnO film without the addition of Au NPs; partially transformed ZIF-8 crystals from ZnO film with different Au NPs concentrations: (c) 20 vol. %, (d) 40 vol. %, and (e) 60 vol. %.

After process, the representative SEM images of sample surfaces are shown in **figure 2.16**. From which we can clearly see the size and density dependencies of ZIF-8 crystals on concentration of Au NPs, which act as a growth inhibitor. While the study of ZIF-8 crystal growth, element verification and size distributions is less relevant to the main topic of the thesis, more detailed discussions can be accessible in the author's publication. [64] Here we will only highlight the intriguing optical properties of ZIF-8 crystals as below.

2.3.1.2 Optical properties of ZIF-8 nanocrystals

The light scattering properties of the synthesized ZIF-8 nanocrystals is investigated with dark field optical microscope (Nikon ECLIPSE L200N), randomly polarized white light was used to illuminate the sample and the scattered light was collected normally to the substrate through a 20 × dark field objective lens (Numerical Aperture (NA) = 0.8). A fused silica wafer was used as the substrate, which is transparent in the UV and visible spectral ranges. A silicon carrier wafer (150 mm) was used to prevent the conformal growth of ZnO on backside of fused silica wafer. A thinner ZnO layer with a thickness of 60 nm was deposited in order to make sure that all the ZnO was reacted and the substrate was purely optically transparent silica. A typical direct dark field image (**figure 2.17a**) shows a variety of colors that are produced by the ZIF-8 crystals. Corresponding SEM image (figure 2.17b) demonstrates the specific dimensions and orientations of the crystals, indicating a strong dependence of the different colors on the particle geometry. To verify this relation, dark field scattering of individual ZIF-8 nanocrystal with different size was studied as illustrated

in figure 2.17c and figure 2.17d. A red shift of the scattered light can be clearly observed from deep blue color to red color with the increasing sizes of the ZIF-8 nanocrystals.

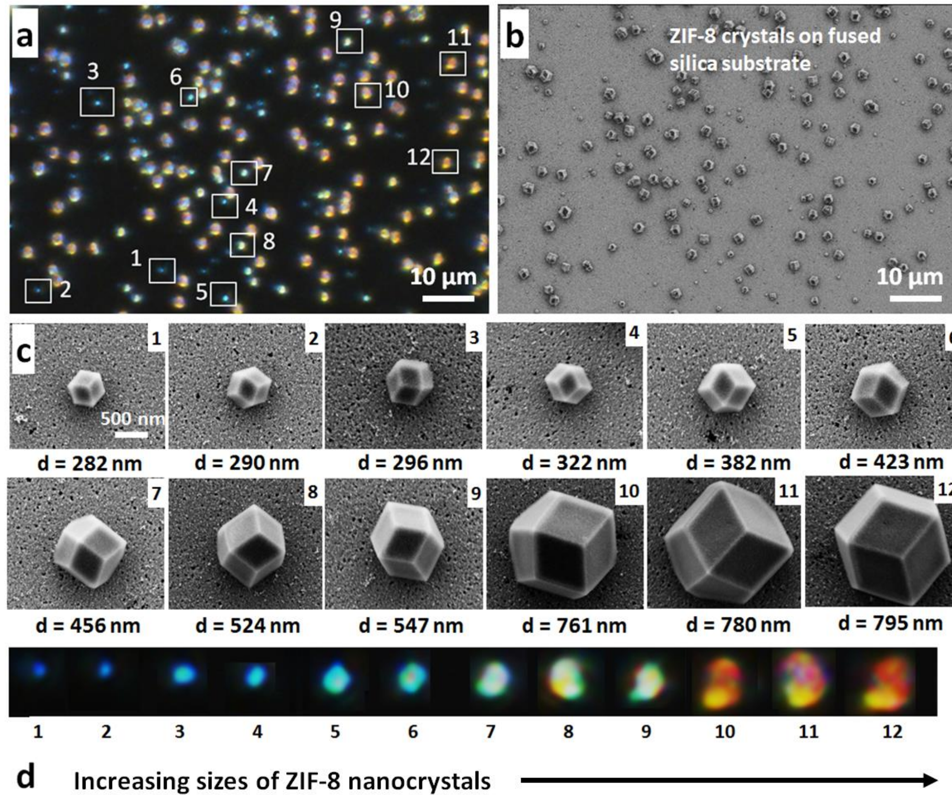


Figure 2.17. Light scattering and structural color of ZIF-8 crystals fabricated with the addition of 60 vol. % Au NPs. (a) Dark-field optical microscope images of ZIF-8 nanocrystals on a fused silica wafer; (b) SEM image of the corresponding area in (a); (c) SEM images of ZIF-8 nanocrystals with different size; (d) Structure colors of ZIF-8 crystals corresponding to (c).

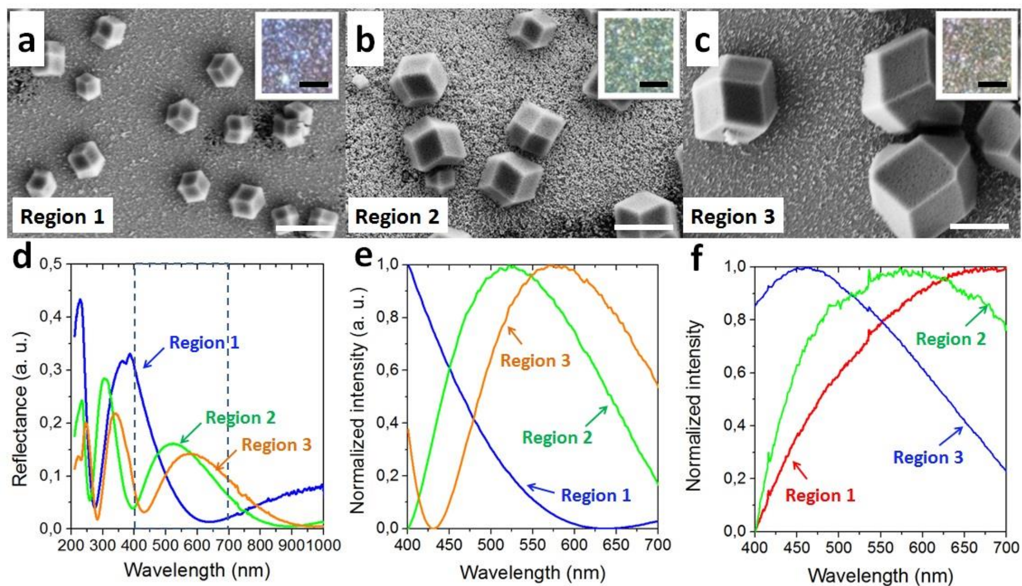


Figure 2.18. (a-c) SEM images of ZIF-8 nanocrystals with three different sizes (the scale bars are 1 µm), the insets are corresponding images under dark field optical microscope (the scale bars are 10 µm); (d) Reflection spectra of three different regions measured by ellipsometry; (e) Reflection spectra in visible wavelengths; (e) Transmission spectra of three different regions measured by UV-visible spectroscopy.

Given the practical constrains of our facilities to directly measure the dark-field spectra of individual ZIF-8 nanocrystals, we in turn performed proof-of-principle experiment to measure the collective response of a certain range of ZIF-8 crystals with relatively uniform size. Reflection and transmission spectra were measured by using ellipsometry and UV-visible spectroscopy respectively, which is shown in **figure 2.18**. Due to the spatial resolution of the incident beam size, all these spectra reflect the collective response of a cluster of ZIF-8 crystals. The variations on particle size, orientations and morphologies of the crystals would largely broaden the spectra, thereby leading to only one pronounced peak that can be readily seen. Nevertheless, all measured spectra show clear optical resonances in the UV-visible range and substantial size dependence, confirming the tunable structural colors produced by the ZIF-8 crystals.

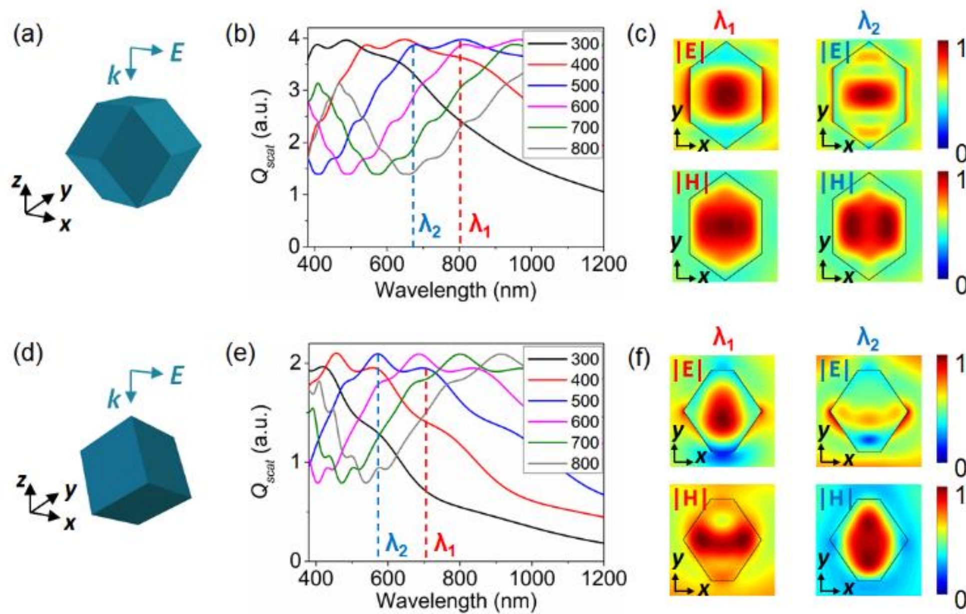


Figure 2.19. Calculated light scattering of rhombic dodecahedral (upper) and cubic (lower) ZIF-8 nanocrystals. (a, d) Schematic illustrations of the nanocrystals and the coordinate system. The incident polarization is in the x direction. (b, e) Spectral scattering efficiency of nanocrystals with different side length d ranging from 100 nm to 500 nm. (c, f) Electric and magnetic near-field distributions at scattering resonances of ZIF-8 nanocrystals with a side length d = 500 nm. The xy profiles are taken in the middle cross section of the nanocrystals. Corresponding resonant wavelengths are labeled in panel (b) and (e)

To fully analyze the progressive color evolution with the crystal size, finite-difference time-domain (FDTD) simulations (Lumerical FDTD Solutions, version 8.11) was performed to calculate the optical response of individual ZIF-8 nanocrystals (**figure 2.19**). A total-field scattered-field (TSFS) method was exploited to reduce computation effort and provide both near field profiles and far-field scattering spectra. A refractive index of 1.59 was adopted for ZIF-8 nanocrystals in the simulation. [76] Scattering response of rhombic dodecahedral and cubic nanocrystals are studied with different side lengths ranging from 300 to 800 nm. Given the high rotational symmetry of these two shapes, only specific orientations are considered for simplicity, as shown in figure 2.19a and figure 2.19d. Scattering efficiency Q_{scat} is calculated as shown in figure 2.19b and figure 2.19e, which is defined as the ratio of the scattering cross section to the geometric cross section. An enhanced scattering can be induced by an efficient light-matter interaction When $Q_{scat} > 1$. This enhanced scattering phenomenon can be found in most spectral regions of ZIF-8 nanocrystals with sizes larger

than 300 nm, covering the entire visible range. Substantial red shifts can also be readily seen in these scattering spectra with increasing crystal size, which is in good accordance with the above experimental observations.

The broadband scattering feature of the ZIF-8 nanocrystals is due to the low permittivity contrast between the crystal and the surrounding environment, which leads to a slightly dispersive polarization current inside the particles and further results in the Mie resonances and associated scattering colors. The scattering peaks can be attributed to the optically induced electric and magnetic dipolar or multipolar resonances. Figure 2.19c shows the near-field electric and magnetic distributions at first two peak wavelengths for rhombic dodecahedral ZIF-8 nanocrystals with d = 500 nm. At the first scattering resonance (λ_1 = 820 nm), the electric field shows a clear electric dipolar behavior with two hot spots at both ends of the crystal along with the incident polarization in the x direction while the magnetic profile demonstrates an evident magnetic dipolar response with a strong concentration of the magnetic field inside the particle. Such a confined magnetic dipolar contribution also contributes to the shoulder (~ 1020 nm) appeared on the long-wavelength side of the peak. At the second scattering peak (λ_2 = 680 nm), higher-order electric and magnetic multipolar responses can be seen with more complicated field distributions.

It is also worth mentioning that, it is only until very recently that people started to investigate the scattering properties and optical resonances from non-metallic nanoparticles. [77] The presented structural color and the scattering properties make ZIF-8 crystals to be a good candidate for a range of nanophotonic applications. Combined with the significant chemical features of ZIF-8 material, including thermal/chemical stability and selective-adsorption properties, a diverse set of interdisciplinary applications become promising , such as photochemical catalysis, chemical sensing and spectral imaging, etc.

3 General Introduction of Plasma Etching

In this chapter we will introduce basics about reactive ion etching, its mechanism and parameters for performance characterization, we will discuss about traditional Bosch process and continuous mixed process, DREM process will then be introduced and discussed in details. In the last, we will talk about the nonuniformity and etch defects that are commonly seen in etching processes.

3.1 General introduction of etching process

Plasma etching is a complicated process with multiple dynamic physical and chemical processes taking place simultaneously and interacting with each other, e.g. fluid dynamics of gaseous species, plasma generation and discharge, kinetic transport of ions and neutrals, chemical kinetics of etching reactions, adsorption and desorption of atoms and molecules on gas-solid interfaces, etc. Besides, most of these processes are participated by multiple species in different phases: gases, solids and plasma, making it extremely difficult to have a quantitative study of the whole process. [78] For Bosch process with switched process parameters, analysis based on theories and modelling can be even more difficult. [79] Although the deeper physical understanding of etch processes is beyond the scope of this thesis, we will give a brief discussion about mechanism of reactive ion etching, including RF plasma discharge and etching reactions on the surface of silicon. Some parameters will be defined to characterize etch processes following the tradition in semiconductor industries.

3.1.1 Basics of plasma

Plasma can be thought of as a collection of conductive ionic gas species, which is in total electrically neutral, but free charge carriers can move randomly. When sufficient external energy is supplied, continuous particle collisions will happen between electrons, ions, atoms and molecules, thus ions and free electrons can be generated constantly by ionization or dissociation processes and plasma can be sustained. The most important parameters to characterize plasma are ion densities and plasma temperatures, from which other parameters, like plasma frequencies, Debye length, plasma current and ion sheath, can be derived.

Ion density n_i is defined as number of ions in a unit volume (particles/cm^3). In a system where the characteristic size is much larger than the Debye length, the charge separation can be omitted and the system is electrically quasineutral, meaning that $n_i \approx n_e$, in which n_e is the density of electrons. If we define the density of neutral gas molecules as n_g, then the degree of ionization for a plasma can be written as $\frac{n_i}{n_i+n_g}$. The plasma processes in semiconductor industries are called weakly ionized plasma, since the ionization degree is on the level of 10^{-6} to 10^{-4}. Since the density of gas molecules in room temperature and pressure of 100 mTorr is around 10^{15} cm^{-3}, the ion density is on the level 10^9 to 10^{11} cm^{-3} in standard plasma systems, e.g. glow discharge and capacitively coupled plasma (CCP), while in the inductively coupled plasma (ICP) systems, a higher ion density of 10^{12} cm^{-3} can be achieved. [80]

Electron temperature T_e is defined by the mean kinetic energy of electrons as

$$\frac{3}{2}kT_e = \langle E_{k,e} \rangle = \frac{1}{2}m_e \int_0^\infty v_e^2 f(v_e) dv_e \tag{3.1}$$

In which k is the Boltzmann constant, $E_{k,e}$ is the kinetic energy of electrons, m_e is the electron mass, v_e is the electron velocity and $f(v)$ is the velocity distribution of electrons following Maxwell-Boltzmann distribution as $f(v)d^3v = \sqrt{\frac{m}{2\pi kT}}\exp(-\frac{mv^2}{2kT})d^3v$. [81] When the plasma is in thermal equilibrium, the ion temperature and electron temperature are approximately same $T_e \approx T_i$. In CCP or ICP etching systems, the energy is highly coupled to electrons, making electrons have a much higher temperature ($\sim 10^4 K$) than ions ($\sim 300\ K$), thus is also called a cold plasma. However, the wafers and chamber will not be heated up since the electrons have much smaller mass.

Since ions and electrons can be driven by electric field $\vec{E} = -\nabla\phi$, in which ϕ is the potential. The ion density and electron density follow the Boltzman relation as:

$$n_i(\vec{r}) = n_0 \exp(-\frac{e\phi(\vec{r})}{kT_i}) \text{ and } n_e(\vec{r}) = n_0 \exp(\frac{e\phi(\vec{r})}{kT_e}) \tag{3.2}$$

Suggesting electropositive ions and electrons are responding differently in an electric field because of the opposite charges. However, it should be noticed that electronegative ions can also be generated, e.g. by a dissociation like: $\mathrm{e} + \mathrm{O_2} \rightarrow \mathrm{O^-} + \mathrm{O}$, because of large positive electron affinity for O_2.

When inserting a charged particle inside plasma, coulomb force will repel the particles with the same charge away from the inserted particle, and a cloud of oppositely charged particles will be created, called Debye sheath (or electrostatic sheath), and the thickness Debye sheath is called Debye length λ_d, given by

$$\lambda_D = \sqrt{\frac{\varepsilon_0 kT_e}{en_e}} \approx 743\sqrt{\frac{T_e}{n_e}} \tag{3.3}$$

For an ICP system with $n_e \sim 10^{12}\ \mathrm{cm}^{-3}$, the Debye length is normally in the range of 0.01 to 0.1 mm, which is much smaller than the characteristic dimension of the reactor volume in an etching machine, thus the plasma can still be thought of as macroscopically stable, even charge fluctuation can happen inside a plasma.

Given Debye length, we can describe the fast oscillation of electron density inside a plasma, using a parameter called plasma frequency ω_{pe}, given by

$$\omega_{pe} = \frac{v_e}{\lambda_d} = \sqrt{\frac{n_e e^2}{m_e \varepsilon_0}} \tag{3.4}$$

For electrons and an ICP etching system with $n_e \sim 10^{12}\ \mathrm{cm}^{-3}$, the plasma frequency is estimated to be 10 GHz, which is much larger than the RF generator frequency of 13.56 MHz, suggesting that the electron density can be considered uniform in an RF discharge system. The characteristic time for collision events inside a plasma, however, is on the order of 10^{-16} to 10^{-15} s, which is much faster than the plasma oscillation.

3.1.2 RF discharge

As mentioned earlier, both CCP and ICP etch systems use RF sources (normally at a frequency of 13.56 MHz) for plasma generations, here we will give a brief introduction about RF discharge mechanism. In **figure 3.1a** is an illustration of a CCP etching system, electrons are driven by the oscillated electric field generated by RF source, at a frequency much lower than collision frequency and plasma frequency, thus electrons can constantly collide with heavy atoms and molecules and a stable plasma can thus be created. Since electron plasma frequency is much larger than ion plasma frequency $\omega_{pe} \gg \omega_{pi}$, charge seperation will happen. By adding two capacitively coupled plates, electrons can quickly charge up at the surface of electrodes and build up a sheath potential V_p, attracting the positively charged ions to bombard the electrode surface, the ion current j_i can be described by well-known Child law as

$$j_i = e n_i u_i = e n_i \sqrt{\frac{e V_p}{m_i}} = \frac{4}{9} \varepsilon_0 \sqrt{\frac{2e}{m_i}} \frac{V_p^{3/2}}{d^2} \tag{3.5}$$

In which d is the ion sheath thickness at the electrode, since electrons are blocked outside of the sheath, no collisions or scattering by electrons can happen, thus this ion sheath is also called dark space. By introducing a blocking capacitor on one of the capacitors, this electrode will be automatically charged up and become a cathode, the potential is called self-bias or DC bias V_{DC}, which can be over 200 V on an ICP etch system, the ion sheath thickness d_c can be described as below by introducing Debye length λ_D

$$d_c = \frac{2}{3} \sqrt{\frac{\varepsilon_0}{j_i}} \left(\frac{2e}{m_i}\right)^{\frac{1}{4}} (V_p - V_{DC})^{\frac{3}{4}} = \frac{\sqrt{2}}{3} \lambda_D \left(\frac{2(V_p - V_{DC})}{T_e}\right)^{\frac{3}{4}} \tag{3.6}$$

We can see that d_c is larger than the ion sheath thickness on anode d_a, because of the additional potential V_{DC} on the cathode side. For an ICP etch system, d_c is on the orders 0.01 to 1 cm.

The RF discharge is behaving electrically like a diode, with high potential drop on cathode side, while a smaller drop on anode side. Since the plasma is highly conductive, the total potential drop is mostly caused by anode and cathode (as shown in figure 3.1b), following

$$\frac{V_p - V_{DC}}{V_p} = \frac{C_a}{C_c} = \frac{A_a}{A_c} \cdot \frac{d_c}{d_a} = \frac{A_a}{A_c} \left(\frac{V_p - V_{DC}}{V_p}\right)^{\frac{3}{4}} \tag{3.7}$$

In which C_a and C_d are the capacitances on anode and cathode, A_a and A_c are the areas of capacitors. Thus the potential drop on two electrodes has the following relation $\frac{V_p - V_{DC}}{V_p} \propto (\frac{A_a}{A_c})^4$. On an ICP etching system, the anode size is normally much larger than the cathode, where wafer is mounted, thus the potential drop can be minimized on the anode to prevent corrosion of anode materials (sometimes a Faraday cage is mounted on the anode, so the ion bombardement can be shielded electrically).

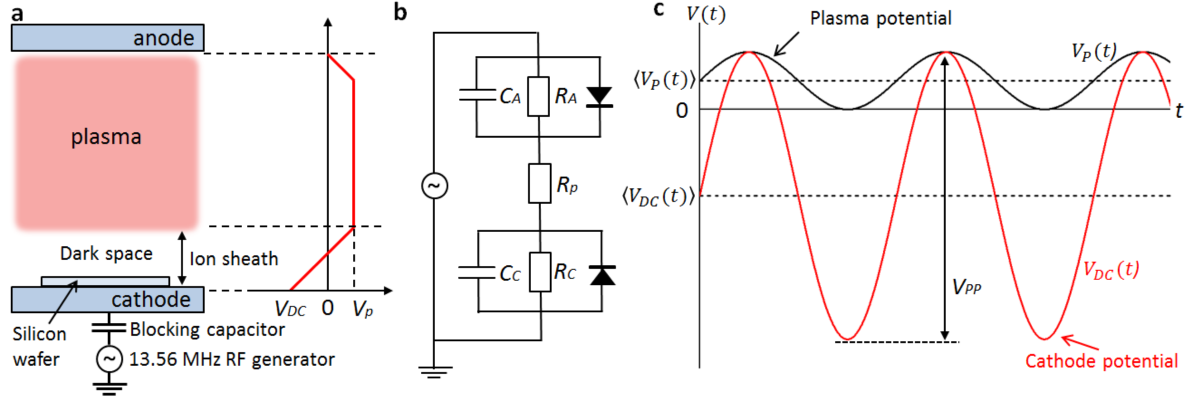


Figure 3.1. RF discharging with a parallel setup. (a) Illustration showing the ion sheath, time averaged potential in a RF plasma; (b) Equivalent electrical circuit of an RF plasma; (c) Plasma potential, DC bias and peak-to-peak potential in an RF plasma.

The plasma potential V_p, DC bias V_{DC}, and the peak-to-peak potential V_{pp} are shown in figure 3.1c, satiesfying following relation:

$$V_{pp} = 2(\langle V_{DC}(t)\rangle + 2\langle V_p(t)\rangle) \tag{3.8}$$

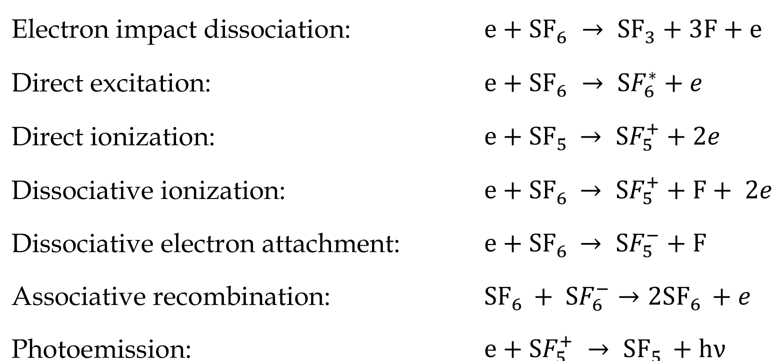
There are a few things that should be noticed:

- In order to have a separate control of plasma generations and ion bombardments to enable more flexibility and precision in etching processes, a separate RF source can be added to the cathode side (platen) to tune the wafer surface potential actively, this is used in the decoupled plasma source [82] and transformer coupled plasma source. [83] The applied power on platen RF source W_p, ion flux to the platen j_i, and the platen DC bias V_{DC} satisfy $W_p \propto j_i V_{DC}$;
- Since structure damage can be caused by strong ion bombardment, [84] some ICP etching systems apply a RF frequency larger than 13.56 MHz to increase the ion densities n_i, [85] so the platen DC bias V_{DC} can be reduced, and a smaller kinetic energy of ions can be achieved; [86]
- Compared with capacitively coupled plate designs in a CCP etching system, ICP etching systems have a coil-like design on the anode side, thus a magnetic field can be generated when RF power is added, which again will induce an electric field extended inside chamber, increasing the ion densities by over 10 magnitude compared with a CCP system, [87, 88] this will reduce the Debye length and ion sheath thickness following equation (3.6), giving a larger ratio between mean free paths of particles λ and ion sheath thickness d_c, thus ions can be transported onto wafer surface with less collisions and a sharper ion angular distribution (IAD), and a better etching directionality can be achieved.

3.1.3 Plasma chemistry and surface processes

In semiconductor industries, halogen-based plasma is normally used for silicon etching due to a relatively high etch rate. A simplified etch reaction can be written as: $\mathrm{Si(s)} + 4\mathrm{X} \rightarrow \mathrm{SiX_4}$ (g), (X: F, Cl). Here we will give a very brief discussion about the kinetics of a fluorine-based plasma and chemical reactions on the silicon surface.

SF_6 is widely used to generate a fluorine-based plasma for silicon etching (other gas species include CF_4, XeF_2, CHF_3, etc). When the plasma is driven by RF power source, collisions will happen between electrons, ions, and electroneutral atoms and molecules. When the collision is inelastic, energies and charges will be transferred through different processes. The interaction time between electrons and heavy particles is normally 10^{-16} to 10^{-15} s, while 10^{-15} to 10^{-14} s for interaction between heavy particles, both of them are at a higher frequency than the plasma frequency and RF frequency. Some of the typical collision processes in a SF_6 - based plasma are listed as below: [89]



Electron impact dissociation: $\mathrm{e} + \mathrm{SF_6} \rightarrow \mathrm{SF_3} + 3\mathrm{F} + \mathrm{e}$

Direct excitation: $\mathrm{e} + \mathrm{SF_6} \rightarrow SF_6^* + e$

Direct ionization: $\mathrm{e} + \mathrm{SF_5} \rightarrow SF_5^+ + 2e$

Dissociative ionization: $\mathrm{e} + \mathrm{SF_6} \rightarrow SF_5^+ + \mathrm{F} + 2e$

Dissociative electron attachment: $\mathrm{e} + \mathrm{SF_6} \rightarrow SF_5^- + \mathrm{F}$

Associative recombination: $\mathrm{SF_6} + SF_6^- \rightarrow 2\mathrm{SF_6} + e$

Photoemission: $\mathrm{e} + SF_5^+ \rightarrow \mathrm{SF_5} + \mathrm{h\nu}$

Two important parameters to characterize the collision processes are rate constant and enthalpy of different substances. The rate constant describes collision frequency of particles and is proportional to v/λ, in which v is the particle velocity and λ is the mean free path, thus collision frequency will be smaller for a plasma with low pressures, low temperature or low RF frequency. While the enthalpy H can be used to characterize the energy change during a process. To describe the charge transfer, electron affinity is also used.

When the radicals and ions are transported to the wafer surface by diffusion (for nanostructures and low pressure, it has been suggested that particles follow Knudsen transport regime [90]), series of surface processes will happen, which are shown in **figure 3.2.**

- Adsorption: adsorption includes physisorption, where the incoming particles are bonded to the surface by van der Waals forces, and chemisorption, where surface compound is produced by stronger adsorption energies from ions or radicals. Generally speaking, the adsorption potential increases with surface temperature, [91] thus for a cold surface, a higher coverage ratio can be expected, thus a higher sticking coefficient, defined by the number of adsorbed particles divided by the number of impinged particles on the surface. In order to reduce the depletion of species and in the same time avoid chamber contamination, the chamber walls and reactors are normally set at a much higher temperature than on the silicon surface;
- Reaction: Chemical reactions on the surface is important, since it determines if the etching process can give an isotropic, non-directional etch profile. The etching reactions on a silicon surface is a surface phase reaction: $\mathrm{Si(s)} + 4\mathrm{F} \rightarrow \mathrm{SiF_4}$ (g), For SiF_4, which has a negative standard molar formation enthalpy $H_f^{\theta}(25\ ^{\circ}\mathrm{C}) = -1614.9\ \mathrm{kJ/mol}$ and a low boiling point of $-95\ ^{\circ}\mathrm{C}$, the etching reaction is exothermal and the etching product SiF_4

is volatile to be pumped out of the chamber, making SF_6 a good candidate for silicon reactive ion etching. Pressure and temperature have huge influences on the chemical reaction equilibrium, e.g. a higher temperature normally leads to a higher etch rate, and strong corrosion on the structures sidewalls.

- Desorption: when the etch process is finished on the surface, etch products need to be desorbed, so the etch process can continue locally. For volatile species like SiF_4, the chemical potential at adsorbed phase is higher than at the gas phase, thus the desorption rate is higher than the nonvolatile species like $SiCl_4$. For nonvolatile species, a higher temperature is needed to overcome the potential barriers for desorption.

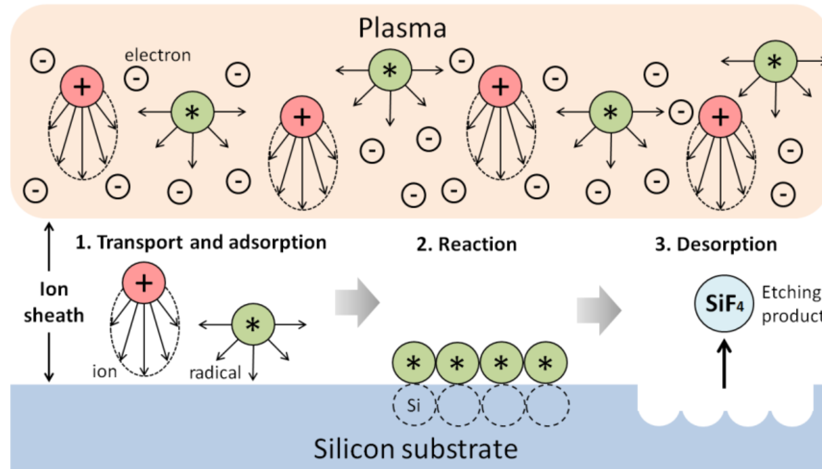


Figure 3.2. A schematic view of reactive ion etching process, red dots are positively charged ions, while green dots are fluorine radicals.

When the processing pressure is sufficiently low, ions will achieve high kinetic energy, both silicon substrates and masks will be sputtered away by a transfer of energy and momentum, the etch rate is highly dependent on the local electric fields, and normally a directional etch profile can be achieved with considerable mask consumptions, as shown in **figure 3.3a**. For neutral radicals, chemical reactions can happen on the surface and the etch profile is isotropic with less mask consumptions (figure 3.3b). In reactive ion etching, a synergistic process happens combining both physical sputtering and radical etching, the etch process is then enhanced by ions and a directional etch profile can be achieved (figure 3.3c). In order to further prevent sidewall corrosions from isotropic etching, ion inhibitors are often used. For example, octafluorocyclobutane (C_4F_8) can generate CF_2 radicals by electron impact dissociation in a plasma: $e + C_4F_8 \rightarrow 2C_2F_4 + e$ and $e + C_2F_4 \rightarrow 2CF_2 + e$. [92, 93] The generated CF_2 radicals can be adsorbed on the silicon surface and form a fluorocarbon layer, which is a nonvolatile etching inhibiting film, [94, 95] since the ions have a smaller kinetic energy on the off-normal directions, thus the sidewall can be protected efficiently and etching process can proceed in an anisotropic manner (figure 3.3d).

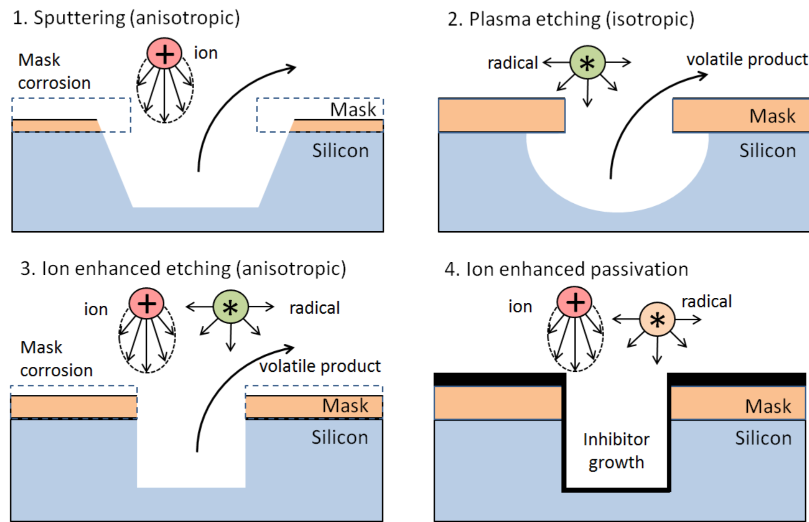


Figure 3.3. Illustration of different plasma processes: (1) Physical ion bombardment; (2) Isotropic plasma etching by radicals; (3) Anisotropic ion enhanced plasma etching; (4) Passivation with ion enhanced inhibitors.

3.1.4 Parameters for characterization of etch performance

For different purposes of applications and devices, we should specify requirements for the etch performances, e.g. in order to fabricate a microscale capacitive accelerometer, the sidewall of the capacitor regions should have a straight profile, and a large etch depth is favored to increase the sensitivity, while for nanoimprinting processes, a tilted sidewall is preferred so the resist can be easier released; compared with microscale structures, nanoscale devices, e.g. finFET and optical waveguides, are much more sensitive to the sidewall roughness. In order to set quantitative requirements for the etch results and also for further evaluations, some parameters are widely used, which are shown below in **figure 3.4**.

D_{Si} is the total etch depth during a process, for some applications as through-silicon via (TSV), an etch depth of around 500 μm is typical. During the etch process, an undercut is normally observed and it will broaden the trench opening to $W_1 = W + 2\delta$. And the aspect ratio (AR) is then defined as $AR = D_{Si}/W_1$, which is an important parameter to evaluate an etch process. Since a large surface to volume ratio can be achieved for high aspect ratio (HAR) structures, HAR micro- and nanostructures are widely used to integrate with other functional materials to form heterostructures. [96, 97] The sidewall of etched profile is sometimes not straight and the sidewall angle is characterized as θ_{Si}, normally we say the sidewall is negatively tapered if $\theta_{Si} > 90°$ and positively tapered if $\theta_{Si} < 90°$.

When a Bosch process is performed, scallops will be generated and sidewall roughness will be induced. The scallop size will normally decrease due to an effect called aspect ratio dependent etching (ARDE), which will be discussed in details later, it implies that $\frac{dD_{sc}(n)}{dn} < 0$ and $\frac{dW_{sc}(n)}{dn} < 0$, in which n is the number of Bosch cycles. For a Bosch process with N cycles (the duration of each cycle as t), the total etch depth will be $D_{Si}(N) = \int_0^N W_{sc}(n)dn$, and the time averaged etch rate for N cycles will be $\langle ER(n,t)\rangle_n = D_{Si}(N)/(N \cdot t)$, while the etch rate is $ER(n,t) = D_{sc}(n)/t$, which will also decrease along with the number of cycles.

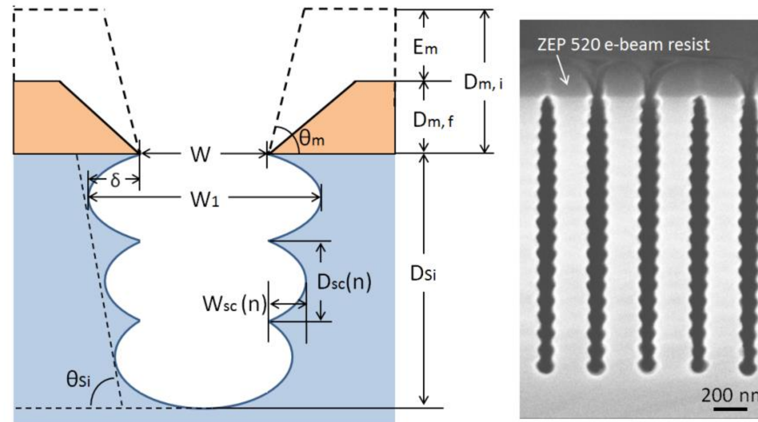


Figure 3.4. A schematic vew of parameters to characterize the etch result (on the left side), and a typical etch profile under SEM (on the right side).

During etch process, the mask is under continuous attack from ion bombardment and radical corrosion, thus the thickness of the mask will reduce from $D_{m,i}$ to $D_{m,f}$, with total etched thickness of E_m. The sidewall of original mask is normally not perfectly straight, but with a angle of θ_m, since most of the masks have poor electric conductivity (e.g. most of the polymer resist, SiO_x, Al_2O_3, etc), charges can build up during the etch process and deflect the incoming ions, for a thick mask, the profile of the mask can sometimes have a huge influence on the etch profiles.

In order to achieve a large etch depth and thus a high AR, and in the same time to reduce the influence caused by the mask, a thin layer of mask (with the thickness below 50 nm) is favored, and the mask layer is required to be able to sustain the etch process, this is described by an important parameter named as selectivity: $S = D_{Si}/E_m$, and the maximum etch depth is then limited by $D_{Si,max} = S \cdot D_{m,i}$. The etch selectivity is dependent on parameter settings in the etch process, e.g. normally a chlorine based etch process will give a smaller etch selectivity compared with fluorine based etch process, due to the heavier bombardment from chloride ion species; and Bosch process has normally a higher etch selectivity compared with continuous mixed process; by tuning the parameters during a Bosch process, an extremely high etch selectivity (even infinite) can be achieved, which will be introduced later. The material properties of mask also has an huge influence on the etch selectivity. Since certain amount of energy is required to desscociate the bond of compound in the mask material, thus materials with high bonding energy or lattice energy normally can give a high etch selectivity, e.g. alumina has a quite high ionic lattice energy of 15916 kJ/mol, [98] and the etch selectivity can be over 10000 depending on the process parameters; HSQ resist has a porous silicon oxide structure, and the bond dissociation energy is around 622 kJ/mol, larger than the bond dissociation energy for organic compounds, which is typically under 500 kJ/mol, thus the HSQ resist can be used directly as a hard mask and the selectivity can be over 100.

3.2 CONTINUOUS MIXED PROCESS

When ion enhanced inhibitors are applied in a reactive etching process, the sidewalls can be protected and silicon can be etched anisotropically. By tuning the gas flow ratios, the sidewall angles can also be controlled, which is favorable for making taper structures, [99, 100] this kind of processes is termed as continuous mixed process or pseudo-Bosch process, in

contrast with Bosch process, in which different gas species are switched and will be discussed later in this chapter. Here we will discuss briefly about etching silicon micro- and nanostructures with a continuous mixed process, where both SF_6 and C_4F_8 are applied in the same time.

To etch nanostructures, the parameter settings for process optimizations are as below: platen chiller temperature is set to be -19 ˚C to increase the sticking coefficient of C_4F_8 ion enhanced inhibitors, processing pressure 15 mTorr, coil power 900 W, platen power 25 W, gas flow rates for SF_6 and C_4F_8 are 35 sccm and 80 sccm correspondingly, the total etch time is 2 min. Line arrays with linewidth of ~ 45 nm are defined by electron beam lithography with 250 nm thick ZEP 520A resist. When increasing the C_4F_8 gas flow rates from 50 sccm to 100 sccm, while keeping other parameters the same, SEM images of etched profiles are shown in **figure 3.5**, suggesting a decreased etch depth in silicon and less undercuts, giving a positively tapered profile. Because of sidewall passivation from C_4F_8 gas species, the roughness is small on the sidewall, which is favorable to fabricate stamps for nanoimprint lithography. However, the upper part of trenches are constantly exposed in radical corrosions and ion bombardments, which will induce sidewall roughness when the etch process continues, as shown in figure 3.5b (C_4F_8 gas flow rate of 80 sccm and etch time of 5 min), thus the aspect ratio of structures is normally limited (< 10) with a continuous mixed process.

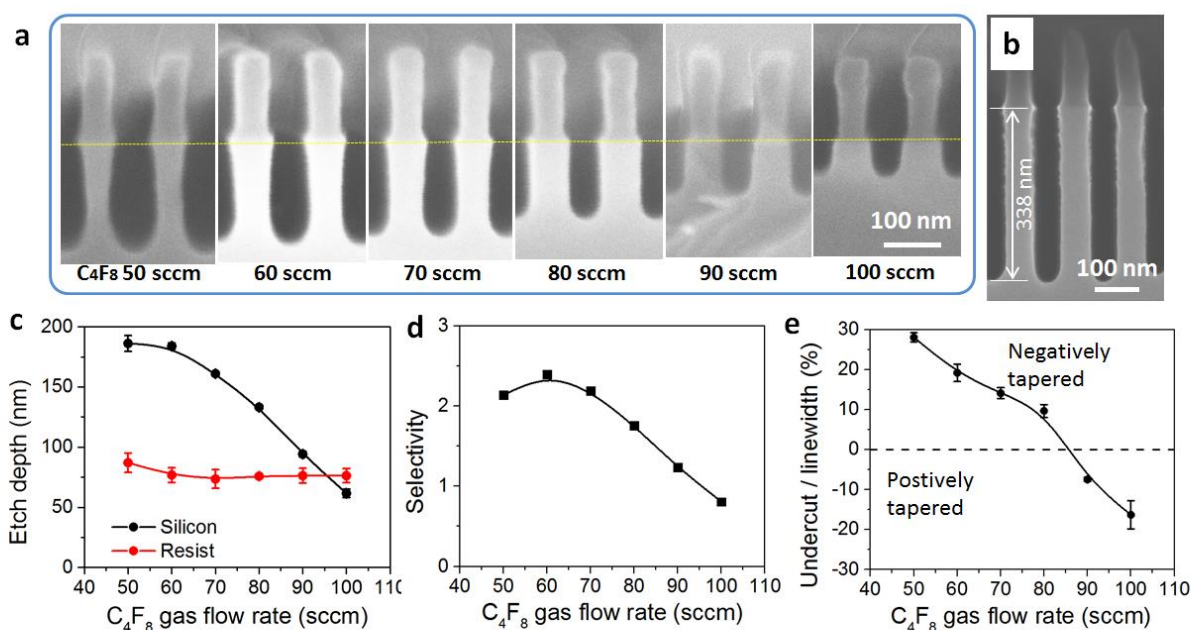


Figure 3.5. Continous mixed process for etching silicon nanostructures: (a) SEM images of etching profiles when C_4F_8 gas flow rate increases; (b) Silicon trenches with AR ~ 7.2 etched by a continuous mixed process, with observable sidewall roughness on the upper parts of trenches; Etching performances for different C_4F_8 gas flow rates are characterized in (c) Etch depths; (d) Etching selectivity; (e) Undercuts.

For microstructures, where the transport of ions and radicals is less limited by the structure dimensions, the continuous mixed process can be more sensitive to processing parameters and difficult to be controlled. In **figure 3.6a** are some etched profiles with a continuous mixed process, the parameter settings are: coil power 2000 W, platen power 140 W, platen chiller temperature 20 ˚C, pressure 25 mTorr, C_4F_8 gas flow rate 200 sccm and SF_6 gas flow rate varying from 200 sccm to 1000 sccm. The patterns are defined by UV lithography with

1.5 µm thick AZ MiR 701 photoresist. We can see that the sidewall become more positively tapered for a higher SF_6 flow rate. When SF_6 gas flow rate is set to be 550 sccm, a sidewall angle of around 68° is observed for trenches with linewidths of both 3 µm and 50 µm, and the bottom is flat with low roughness, a large undercut of 3 µm is also observed. When increasing the SF_6 gas flow rate even further, a “transition” on the sidewall can be noticed, with the upper part of trenches etched isotropically with a large sidewall roughness, while the bottom parts are still anisotropic with small sidewall roughness (figure 3.6d). This phenomenon, again, might be caused by less efficient passivation on the upper part of trenches, which is caused by more radical corrosion and ion bombardment compared with the bottom parts, thus a transition of profile can be observed. [101, 102]

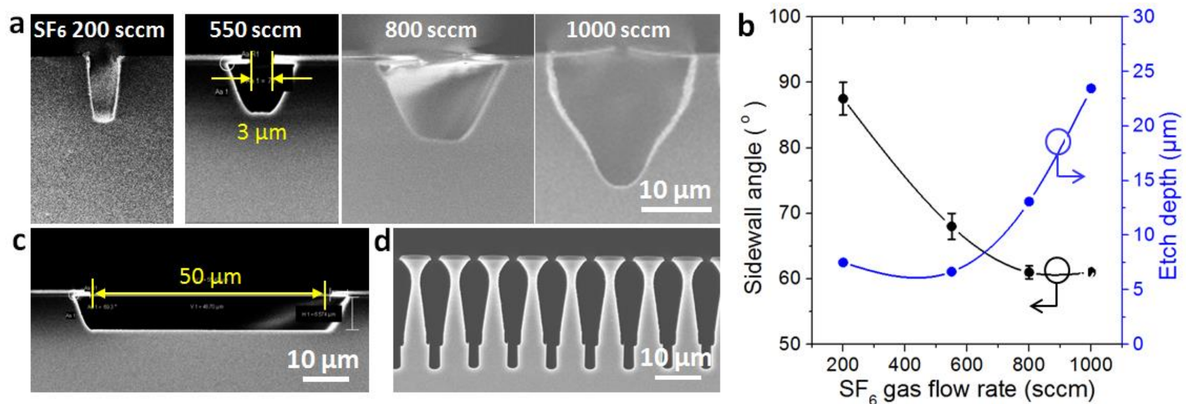


Figure 3.6. Continuous mixed process for etching microstructures: (a) SEM images of etched profiles for different SF_6 gas flow rates; (b) measured sidewall angle and etch depth; (c) A 50 µm wide trench with low roughness on both bottom and sidewall; (d) Transition of profiles from isotropic to anisotropic.

As discussed above, continuous mixed processes can give an etch profile with low roughness on sidewalls and bottoms, and the sidewall angles can be controlled by tuning the gas ratios between SF_6 and C_4F_8. The process doesn't require fast gas switching, thus is relatively easy to perform and optimize with a standard etching apparatus. However, this method is not suitable for etching high aspect ratio structures, due to an insufficient passivation on the sidewall that can cause structure collapse. Since the mask is under constant ion bombardment, the etching selectivity is normally not high enough to achieve a large etch depth. All these drawbacks limit a wider application of continuous mixed processes.

3.3 Bosch process

In section 2.2 we have discussed about continuous mixed processes, it is shown that the aspect ratio is limited by the insufficient sidewall protection. In this part we will introduce briefly about Bosch process, which separates sidewall passivation from silicon etching into two steps, thus ion enhanced inhibitors and etching species will not interfere with each other, and a better sidewall protection can be achieved. An illustration of a standard Bosch process is shown in **figure 3.7a**, each cycle of the whole Bosch process is composed of two steps: etch and deposit. During etch step, SF_6 plasma is generated by the coil source, and ions obtain kinetic energies from applied platen power, thus ion enhanced etching will happen on the silicon surface. The etch step is then followed by a deposition step, during which SF_6 gas flow is turned off, while C_4F_8 plasma is generated and a passivation layer is coated on the sample surface. The next Bosch cycle again starts with etch step, and the

passivation layer in the bottom of structures can be removed by energetic ion bombardments from a SF_6 plasma, and silicon will then be etched deeper when the bottom is free from fluorocarbon layer protection. Since the lateral etch always exist due to off-angle ion bombardment and spontaneous etch of silicon with fluorine based radicals, Bosch process can generate "scallops" on the sidewall, which is the major cause of sidewall roughness.

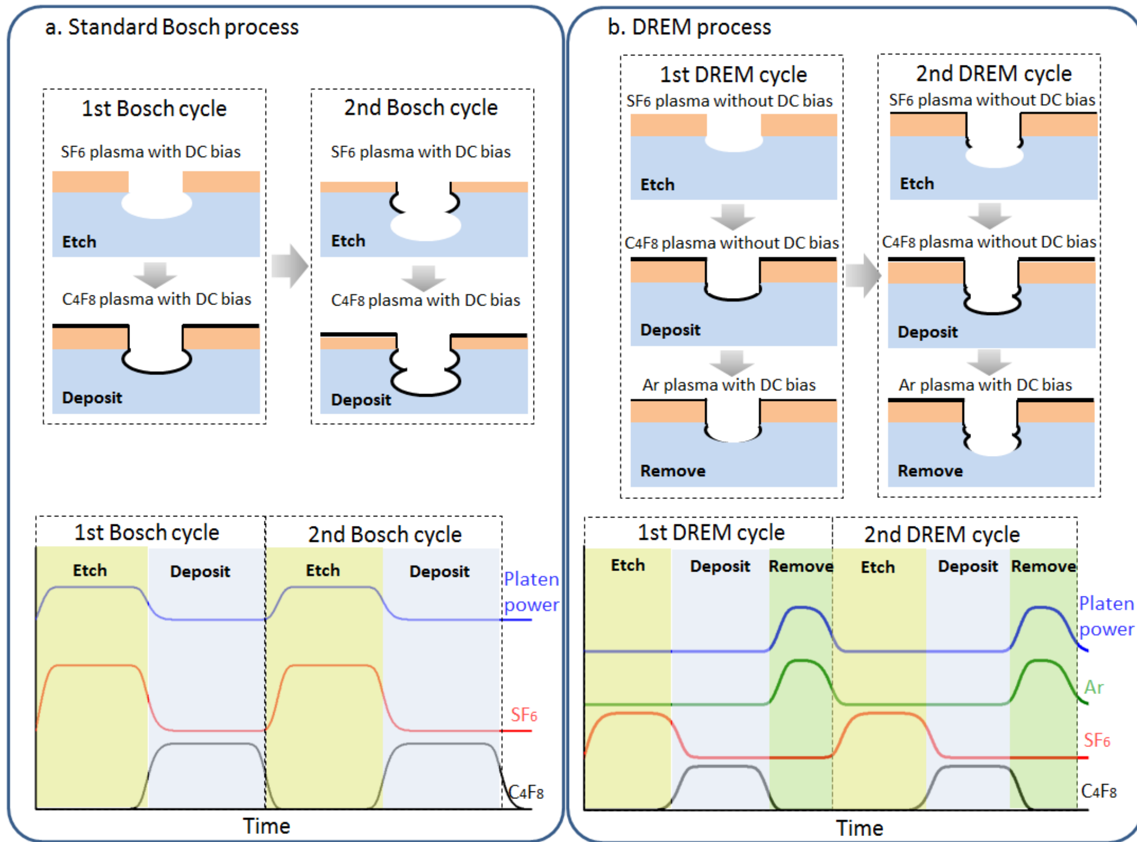


Figure 3.7. Illustration of a standard Bosch process (a) and a 3-step DREM process (b).

There are a few issues that should be addressed for a standard Bosch process:

- During the etch step, there are actually two processes going on: removal of fluorocarbon layer by ion bombardment and reactive ion etching of silicon. In the standard Bosch process, both of them are accomplished by applying SF_6 plasma with DC bias. However, the etching process is a dynamic process, thus optimal parameter settings need to be altered over time for each of the two processes. By merging these them together, there are much less freedom to optimize the parameters, thus less precision to control the etch processes;
- By merging bottom removal and etch steps together, mask is exposed in ion bombardments for excessive time, thus the selectivity of the recipe can be undermined, and the maximum achievable aspect ratio and etch depth will be limited;
- During the silicon etch step, when scallops are generated, both ions and radicals are transported to the sidewall surface and participate etch processes simultaneously, this will naturally lead to a higher etch rate, however, the scallop sizes will also be increased and induce a larger sidewall roughness. The enlarged scallops can also harm the stability of structures, especially in nanoscale, where the critical dimension can be

comparable with scallop sizes. **Figure 3.8a** and figure 3.8b show nanostructures of trenches and holes fabricated with a standard Bosch process, since scallops have a size of around 50 nm, which is close to the critical dimension of structures (linewidth, hole diameters), the shape of structures is undermined. Figure 3.8c shows the sidewall roughness caused by scallops in a microstructure.

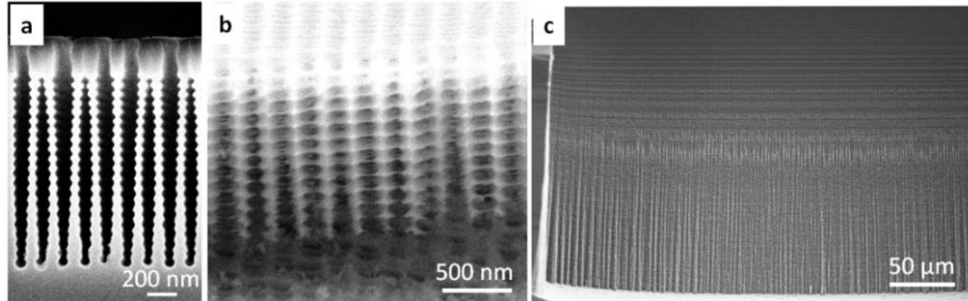


Figure 3.8. Scallop induced defects: (a) Trench arrays with linewidth of 50 nm; (b) Arrays of holes with diameter of 50 nm; (c) Sidewall roughness on the sidewall of a squared microhole.

From the discussions above, we can see that Bosch process shows strong advantages for high aspect ratio etching with anisotropic profiles. However, in order to achieve a better etch selectivity and smaller sidewall roughness caused by scallops, more precise control of etch processes can be necessary.

3.4 DREM PROCESS

In this part we will introduce the DREM process, which is reproduced from the author's publication, [103] copyright 2018 Elsevier. The basic parameter setting for a typical 3-step DREM process with an illustrative diagram is shown in table 3.1 and figure 3.9. In the first 1.8 s deposition step, C_4F_8 plasma is used to passivate the wafer with a fluorocarbon layer. A minimum of platen power is applied to ensure low mask erosion. [104] The processing temperature was chosen to be at the minimum of -19 ˚C, to improve the sticking coefficient of the passivation species (the deposition rate can be around 3 times faster than at 20 ˚C). Also the pressure is optimized with respect to the 3000 W coil power for maximum fluorocarbon deposition rate. In the second 1.9 s removal step, low pressure (5 mTorr) Ar plasma with high bias power (75 W, with DC bias of around 325 V) is used for 1.0 s to clear the fluorocarbon film from the bottom of the trenches. By taking rise time of mass flow controllers (MFC) and delay time caused by the reactor residence time into consideration, the process synchronization is established for optimal performance as suggested in previous literature. [105] It is easier to maintain low pressure plasma with Ar than with e.g. SF_6, because Ar is an electropositive gas whereas SF_6 is electronegative. To minimize the coil reflective power, the Ar gas flow was chosen to be 200 sccm during the deposition and 250 sccm during bottom removal and etching. The lowest possible pressure during bottom removal is needed to sharpen IAD as much as possible, thus ensure a maximum straight profile. In the etching step, SF_6-based plasma is used to etch silicon isotropically. Again a minimum platen power is applied to preserve the mask. By using time ramping during the etch step, the scallop sizes can be tuned to be almost identical along the trench. The initial etch step duration was chosen to be 0.6 s to ensure correct initial etches and the final etch step duration t_{end} was carefully tuned. It should be noticed that abrupt change of SF_6 flow can cause high coil reflected power, thus "shoulders" have been used to smoothen the gas flow changes.

		3-steps DREM cycle		
		Deposit FC	Remove bottom FC	Etch silicon
Duration (s)		1.5	1.9	0.6 → t_{end}
Gas flow (sccm)	C_4F_8	300	5	5
	SF_6	15	15	600
	Ar	200	250	250
Generators (W)	13.56 MHz coil generator	3000	3000	3000
	13.56 MHz platen electrode	1	75 (for 1 sec)	1

Table 3.1. Parameter settings for a typical 3-step DREM process.

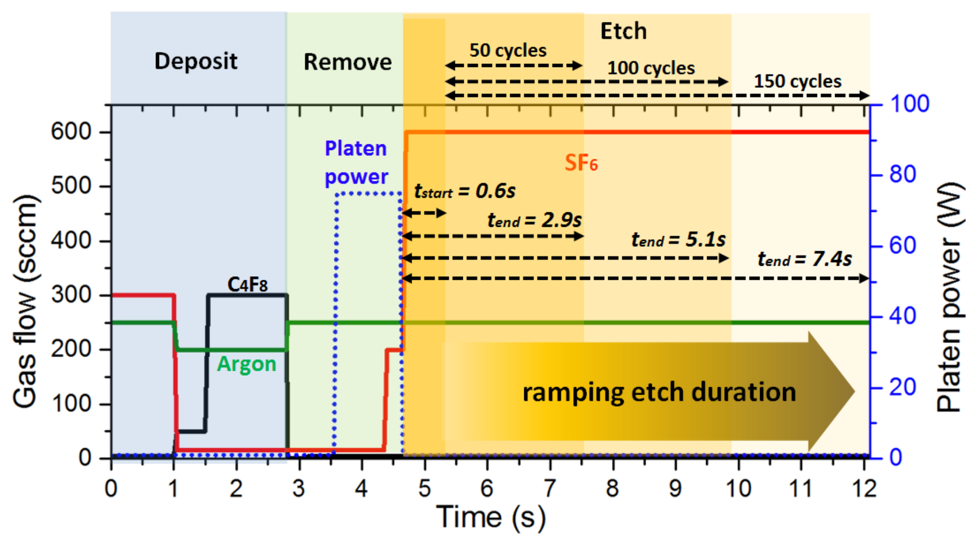


Figure 3.9. Illustration of the 3-step DREM process.

A special feature of the DREM process is the infinite etch selectivity it can achieve. Most resist-types have selectivity of around 100 or less. [106] Instead, the extraordinary high selectivity in DREM process is caused by the non-conformal fluorocarbon film deposition inside etched structures. This layer protects not only the features sidewalls, as well as the mask. The mechanism can be seen in figure 3.7b. Firstly, silicon is etched isotropically using SF_6 plasma; secondly, C_4F_8 is applied for fluorocarbon passivation. Due to depletion of species inside the trenches, the thickness of the fluorocarbon film is thicker on top of the resist compared with the bottom of the structures. Then, the fluorocarbon film is removed directionally by Ar plasma with a DC bias during the bottom removal step. If the applied DC bias is just enough for clearing the bottom of the trench, the resist will still be covered by some fluorocarbon film residue. Thus, when the etch process goes on to next cycles, the resist (or any other mask material) will always be protected.

The etch profiles of the 1 µm wide trenches are shown in **figure 3.10a**. After etching the BARC layer, 50 cycles were performed to reach an etch depth of 18.8 µm, while the 360nm resist remained intact; after 100 cycles, the etch depth was doubled and the resist was still undisturbed. Noticeably, a rather thick fluorocarbon layer started to grow at the topside of the etched structure thus narrowing the trench opening. When the number of cycles is further increased to 150, the etch depth was around 58.1 µm, which implied an aspect ratio

of more than 50, while the sidewall of the trench started to be slightly corroded (figure 3.10e). Furthermore, the trenches have the tendency to become a slightly more positive tapered towards the bottom of the trench. This is most likely the result of the slowly closing trench entrance while etching proceeds. The total etch depths and the duration of etch step in the last cycle t_{end} are shown in figure 3.10c, which suggests a linear relation between etch depths and total number of cycles, this is due to the identical scallop sizes given by parameter ramping. Thus, by carefully tuning DREM, silicon can be etched directionally with identical scallops and infinite selectivity. Therefore, DREM process is potential to realize ultrahigh aspect ratio structures with a free choice in masking material.

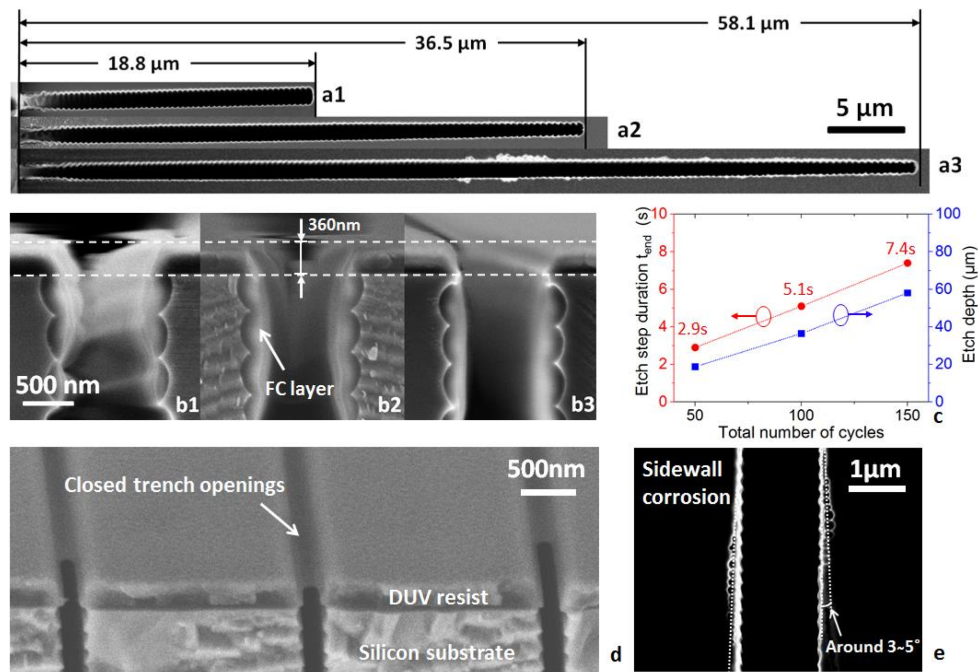


Figure 3.10. Etched 1 µm wide trenches with 50, 100 and 150 DREM cycles (a1-a3) and the corresponding SEM images showing top of the trenches (b1-b3), suggesting an infinite etch selectivity; (c) Etch depths and the final etch duration t_{end}; (d) Closed trench openings for 200 nm linewidth; (e) Sidewall corrosion on the sidewall.

There are two issues that should be addressed regarding DREM process. The first is the closing trench most likely due to the lack of surface migration of the growing fluorocarbon film. On the one hand the FC film will provide sufficient protection to the top part of the trench against erosion, but on the other hand the deposited layer will limit the incoming etching species and influence the IAD, both of which will cause non-uniformity in the etch process. When the process continues the trench will even be fully closed and the etch process will not be able to continue. This effect is especially pronounced for trenches with a very small linewidth (as shown in figure 3.10e), in which the top part of a 200 nm wide trench is totally closed by the fluorocarbon layer. The method to solve this problem is to add an oxygen plasma pulse after every SF_6 etch step. Thus the trench can be opened again and DREM can continue. So, in total there will be 4 steps during this process, named as DREAM process (Deposition with C_4F_8, Removal bottom with Ar, Etching with SF_6, Ashing with O_2, Method).

Another issue is the sidewall corrosion, which can be clearly seen when the AR is more than 50 (as shown in midsection in figure 3.10a3 and a close up view in figure 3.10e). The sidewall corrosion is closely related to the sidewall angle of the profile. Since the

passivation with ion inhibitors is increasingly limited with an increasing AR, therefore, the lower region of the sidewall will be less protected by fluorocarbon layer. However, during the bottom removal step the accelerated Ar ions can be transported down to the bottom of trenches, due to the non-ideal IAD, the sidewall will be continuously exposed to off-normal incoming energetic ions. Thus when the etch depth increases, the off-normal Ar ions will start to corrode the passivation layer and create weak points in the sidewall protection. [107] Since the middle part of the trench has less sidewall protection compared with the top part, and is exposed to the ion bombardment for a longer time than the bottom part, the sidewall corrosion is most pronounced in the middle of the trench. One way to solve this issue is to tune the profile to a slightly negatively tapered angle, either by increasing the platen power during bottom removal steps, or by reducing the passivation during the deposition steps. With the profile slightly negatively tapered, the sidewall will suffer less off-normal ion bombardment. The downside of this method is that the infinite selectivity might get lost.

3.5 BEYOND DREM – DREAM PROCESS

When the DREM process is repeated for many cycles, the overdeposited fluorocarbon film will block the trench openings, which can limit the incoming ion and radical flux and thus hinder the etch process to achieve HAR, in the same time, the transport of ion enhanced inhibitors will also be restricted, which will lead to a less sufficient sidewall passivation and might be the cause for sidewall corrosions as shown in figure 3.10. It has been proposed in the previous session that by introducing an ashing step with O_2 plasma, the fluorocarbon film deposited on top of structures can be efficiently removed, and the etch process can continue. Here we will give a brief discussion about this 4-step DREAM process.

An illustration of DREAM process is shown in **figure 3.11a**, compared with a DREM process in figure 3.7b, a step with O_2 plasma is inserted right after the etch step and before the deposition step in the next cycle. Thus the inlets for ion enhanced inhibitors can be cleaned and blockage by fluorocarbon film can be avoided. To demonstrate the effect of inserted O_2 plasma ashing step, trench arrays with linewidth of 1 μm and period of 10 μm are etched with DREAM process, with different durations of ashing steps from 1.0 s to 2.5 s. When the ashing is not sufficient (as shown in figure 3.11b), a positively tapered profile can be observed with a closed trench bottom, suggesting a limited etching in the end of process; when the ashing step is increased to 2.5s, a straight profile with a flat trench bottom can be observed, implying an unblocked etch process. The etch depth is measured to be increase with a longer ashing step (figure 3.11c). However, it is also noticed that, for long ashing steps of over 2.0 s, the corrosion of photoresist will start from surface and create nanoscale pinholes (figure 3.11d), even though the sidewall is still well protected by fluorocarbon layer. Etching processes will then start from these nanopinholes and destroy the structures.

For polymer-based photoresist, which can be chemically removed by O_2 plasma, the ashing step needs to be carefully controlled, so that the fluorocarbon film can be removed without damaging the photoresist. While for a hard mask like silicon oxide or alumina, the DREAM process can be a promising candidate for HAR structures etching, and only a thin layer of mask is required. More detailed study of DREAM process is still in progress.

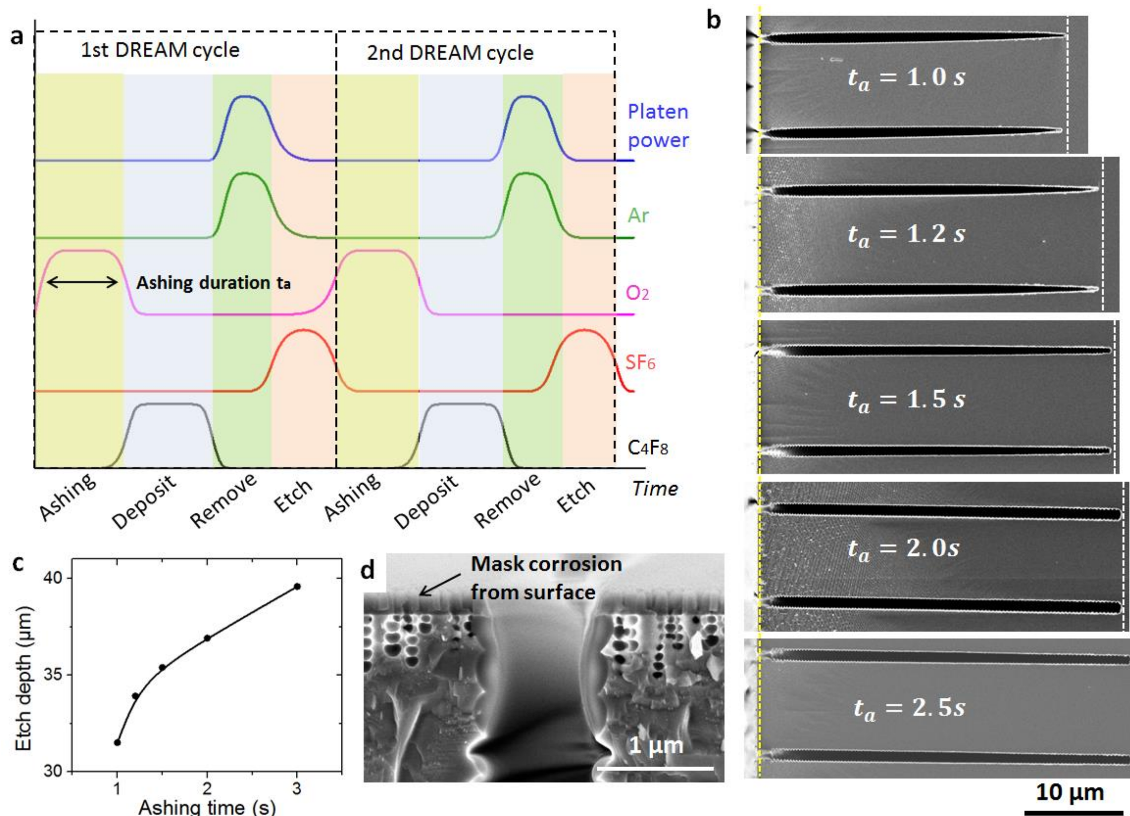


Figure 3.11. DREAM process: (a) Illustration of DREAM process; (b) Etch profiles with different duration of ashing steps; (c) The relation between etch depth and ashing time; (d) Corrosion from resist surface when ashing time is 2.5 s.

3.6 DEFECTS IN ETCH PROCESSES

Now we have discussed about plasma etching processes and introduced DREM process. However, there are some etching defects that we should be aware of during an etch process, and most of them can be avoided by parameter optimizations. In this part, we will show some common etching defects in plasma etching processes.

Loading effect

Due to depletion of etching reactants, the local etch rate will be reduced when a larger area of silicon surface is exposed in the plasma. [108] When multiple wafers are loaded in the same chamber (e.g. in a barrel type plasma etching chamber), the etch rate of each single wafer will decrease, this is sometimes termed as macroloading effect, to distinguish from microloading effect, which describes the etch rate dependency on the local pattern density. [109, 110] According to the model in previous studies, the etch rate $ER(A)$ and the loading area A has relation as $ER(A) = 1/(1 + \frac{NA}{V})$, in which V is the chamber volume, and N is a constant about etchant generation rate and mean lifetime of etching species. The loading effect is tested with four wafers with different loading areas: 10%, 20%, 50% and 80%, and lines with different linewidths are patterned on each of the wafers. After 50 cycles of Bosch process, the etch depths are measured by SEM and etch rates are shown in **figure 3.12**, we can see the decreased etch rate for smaller linewidths, which is caused by the RIE lag, when the loading area increases from 10% to 80%, the etch rate for each of the linewidths decreases.

Although loading effect is a side effect for etching process, it can be used to achieve a smaller scallop size, and thus less sidewall roughness, which is shown in figure 3.12b: same etch process was applied for samples with different carrier wafers: silicon wafer coated with 200 nm alumina by ALD, and bare silicon wafer, corresponding to less than 1% loading area and more than 99% loading area. From the SEM images we can see the reduced etch depth for samples on a silicon carrier wafer and smaller scallop sizes (figure 3.12c). However, we should notice that the sidewall of etched profiles with silicon carrier wafer is more negatively tapered. This is understandable, since the depletion of ion induced inhibitors will reduce sidewall protection efficiency for a large loading area, and sometimes an undercut can even happen.

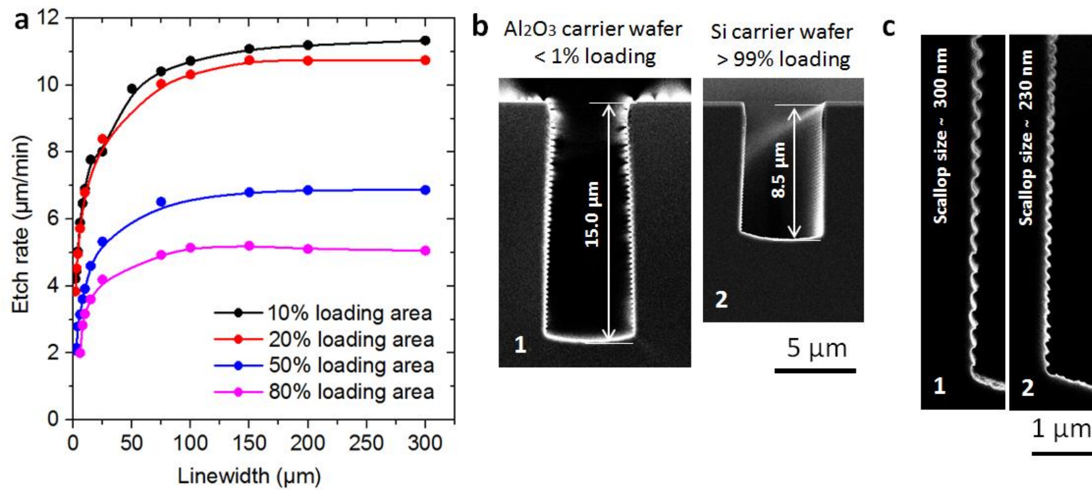


Figure 3.12. Loading effect for Bosch process: (a) Measured etch rates for different loading areas and linewidths; (b) Etch profiles with the same recipe but on two different carrier substrates, showing difference of etch depth caused by loading effect; (c) A zoomed in view of the sidewalls of the etched profiles in (b).

Another nonuniformity caused by the loading effect is the cross wafer nonuniformity, meaning that there exists a variation of etch rate across the wafer. [111] This is understandable since the depletion of etching species is less on the peripheral regions on a wafer, which will then lead to a higher etch rate. In **figure 3.13** is the etch depth for microtrenches with 12 μm linewidth, the etch depth was measured on 19 points across the wafer, the etch recipe was a standard Bosch process with 30 cycles. It can be seen that the etch depths on the edge of wafer is larger than in the center region (the etch depth difference can be around 20%). When changing the recipe by increasing processing pressure, the trend can still be observed. It can also be seen that on the right side of the wafer, which is closer to the pump location during etch process, the etch depth is around 4% smaller than on the other side of the wafer, this can also be concluded as a result of higher depletion of etch species closer to the pump. Since the ion sheath is following the silicon surface, thus the curvature on the wafer edge will also distort the etch profile, creating a tilted etch structures towards the center of the wafer, which is shown by SEM images in a, b and c positions. To avoid this nonuniformity, device patterns are normally not designed on the outer range of the wafer. By using a etch apparatus dedicated for a larger wafer process, e.g. etch machines for 8 inch wafer with larger funnels and electrostatic chuck, this nonuniformity can be reduced, by tuning the distance between funnel and the sample surface, this nonuniformity can also be reduced. [112]

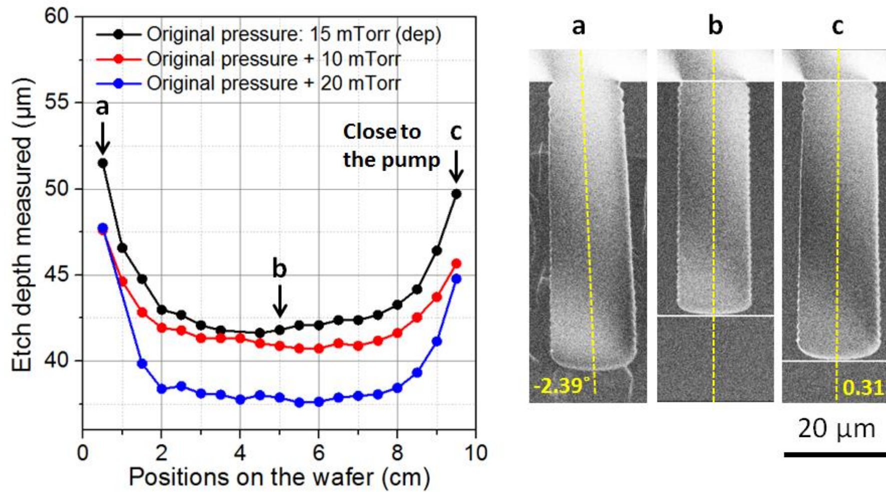


Figure 3.13. Cross wafer nonuniformity, the measured etch depth is shown on the left side, while the SEM images of structures on the edge and in the center are shown on the right side.

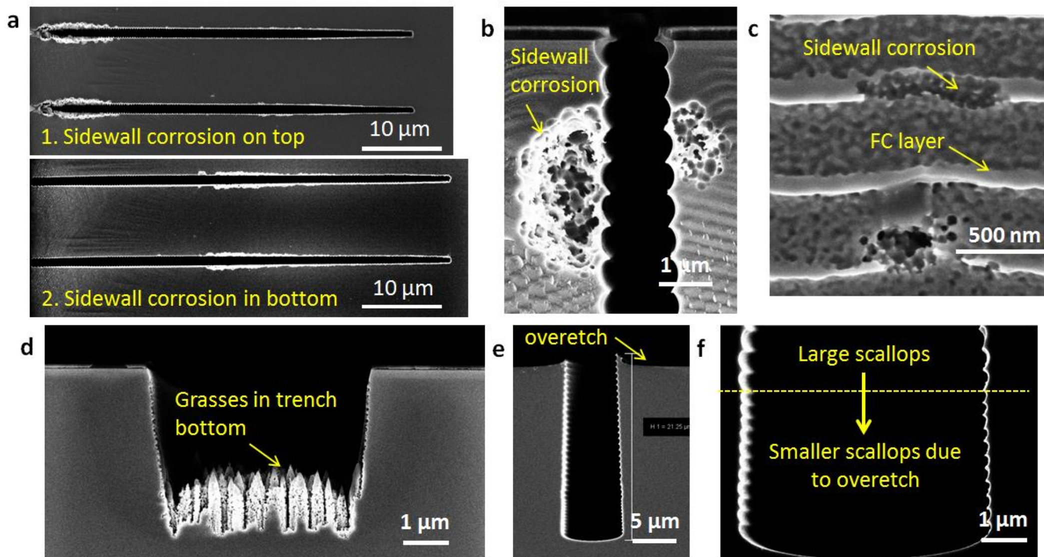


Figure 3.14. SEM images showing different etching defects: (a-c) Sidewall corrosions; (b) Grass generation in the bottom of structures; (e-f) Overtetch.

Sidewall corrosions, grasses and overetch

These are the most common etching defects that can happen in an etch process and destroy the silicon structures. Sidewall corrosion is generally due to an insufficient passivation of fluorocarbon layer, it can happen both in the bottom of the structures and also at the top of structures thus causing a strong undercut, which is shown in **figure 3.14a**. Normally a longer deposition step can provide a better sidewall protection, however the effect can be limited for HAR structures, since the fluorocarbon deposition is like PECVD process, and the passivation in the bottom of the trench is much weaker than the top. A platen DC bias can be added during deposition step to enhance the transport of ion enhanced inhibitors, however, the top of the trench will be under stronger bombardment and start to be corroded (figure 3.14b-c). In our process, the sidewall angle is controlled to be slightly negative, thus the sidewall is not under direct ion bombardment and better sidewall protection can be achieved. The sidewall corrosion can also imply some other issues, e.g. a less efficient wafer cooling which can weaken the adsorption of ion enhanced inhibitors.

Grasses in the bottom of the structures is another well-known etching defect (figure 3.14d), which is normally due to an incomplete removal of deposited fluorocarbon layer in the bottom, and larger structures are more susceptible to grass generation. By increasing the DC bias or duration of bottom removal step, the grasses can be removed efficiently. There are also other factors that can contribute to the grass generation, e.g. the dirt inside chamber, or a hard mask that is sputtered and generate micromasks.

When the total process time is not controlled correctly, mask layers can be consumed completely and silicon structures will start to be etched (named as overetch). When the resist is gone, the total loading area is almost 100%, thus the etch rate will decrease and smaller scallop sizes can be observed (figure 3.14e-f). To avoid overetch, OES is performed to have a real time monitoring of etch process, and the endpoint can be detected where silicon starts to be overetched, this will be discussed in next chapter.

Trenching and faceting

For etching process with high ion density and ion energies, a well-known etching defect is trenching effect, meaning that the corner of the structure bottoms will be etched more compared with other parts in the bottom of the structures (as shown in **figure 3.15a**). This is typical for etching process where the etching products are nonvolatile, e.g. etching silicon with chloride-based etching species, or etching alumina with argon plasma. In such cases a positive tapered sidewall will deflect the off-angle incoming ions, and the ion fluxes will be "focused" into the corner of structure bottoms, [113 - 115] thus the etch rate will be enhanced in the corners. It has also been suggested [116] that the electron flux is isotropic, while the ion flux is anisotropic, thus for materials with bad electrical conductivity, the sidewall will be more negatively charged compared with the bottom of the trench, thus the positive ions will be deflected towards the sidewall, and the trenching effect will be enhanced.

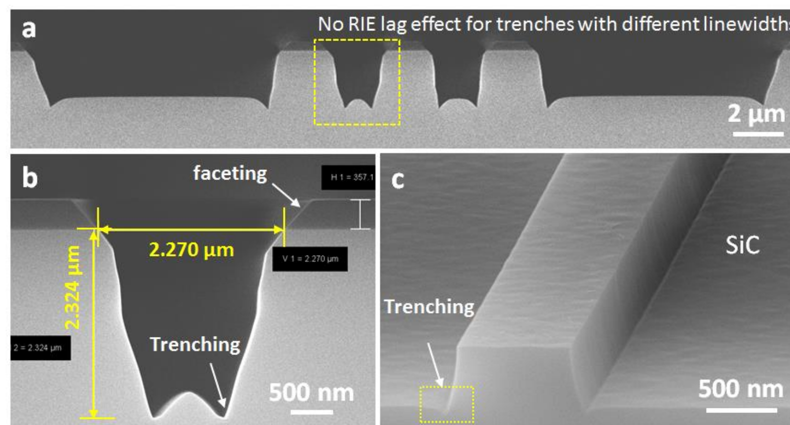


Figure 3.15. Trenching effect by strong ion bombardment: (a-b) Silicon etched with chlorine-based plasma; (c) Silicon carbide structures etched with fluorine-based plasma.

In figure 3.15a-b are SEM images showing trenching effects in silicon etching, the etching parameters are: 900 W coil power, 60 W platen power, 20 sccm Cl_2 and 2 mTorr processing pressure. Figure 3.15c shows the trenching effect in silicon carbide (SiC) etching, the processing parameters are: 800 W coil power, 80 W platen power, 120 sccm SF_6 and 5 mTorr pressure. Another phenomenon we should notice is the faceting on the top of trench, this is also a byproduct from strong physical etching process. Because of the large curvature on the corner of mask, incoming ions will be impinged due to the local electric field and the mask corrosion rate will be increased, thus the sidewall of mask will slowly become

positive tapered. [117] When the etching process proceeds, the mask will regress and the faceting effect will happen. This effect can be clearly seen in figure 3.15b. Both trenching and faceting are unwanted etching effect that can distort the etch profile and undermine the final structures.

RIE lag and inverse RIE lag

RIE lag is a phenomenon in which the etch rate depends on the feature widths of the patterns. [118] Some studies show that the etch rate is scaling with aspect ratio instead of absolute feature widths, [119] thus sometimes the RIE lag is discussed together with aspect ratio dependent etching (ARDE), which will be introduced later. **Figure 3.16a** shows SEM images of three etching phenomena: for RIE lag, the 10 μm wide trenches are etched deeper than 2 μm trenches; for inverse RIE lag, the 2 μm wide trenches are etched much deeper; while the etch depths can also be approximately the same when no RIE lag is observed. The measured etch rates for different trench openings are plotted in figure 3.16b, where we can see different trends of etch rates with feature widths. Inverse RIE lag has been studied before for silicon oxide etching, and it was suggested to be caused by a stronger aspect ratio dependency of neutral fluxes than ions. [120] Since the aspect ratio increases faster for a smaller feature sizes, the neutral flux for deposition on the bottom will decrease, while the ion flux still remains the same, thus an inverse RIE lag can be observed.

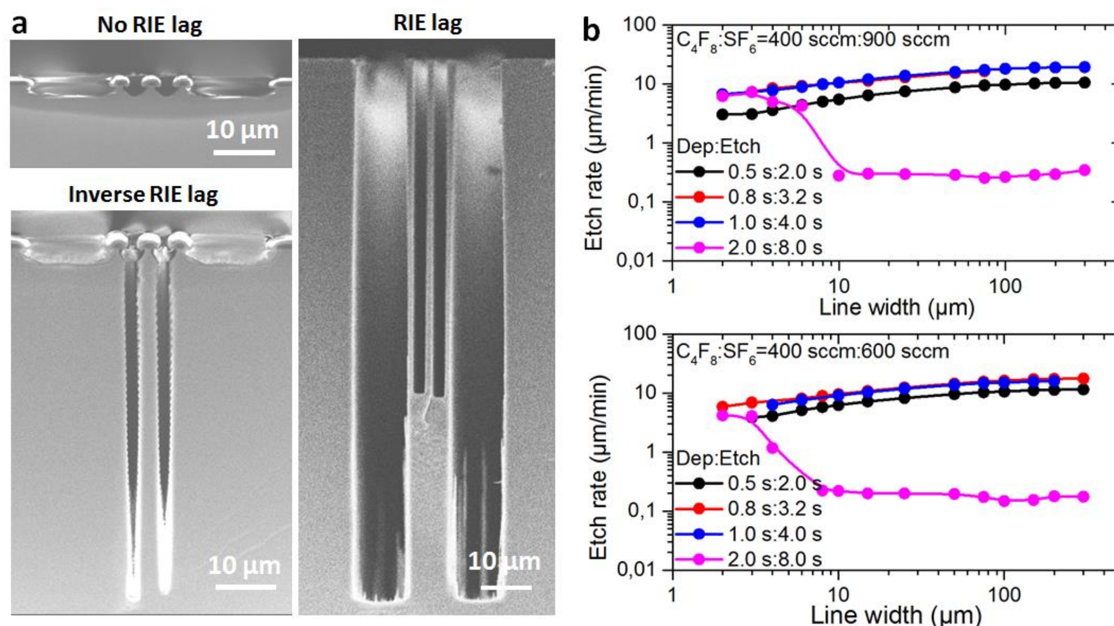


Figure 3.16. (a) SEM images of RIE lag, inverse RIE lag and no RIE lag; (b) Measured etch rates for different linewidths showing RIE lag and inverse RIE lag.

ARDE

Another well-known etch nonuniformity is ARDE. In order to discuss the effect, a quantitative characterization of etch profiles is necessary, however, the direct measurement of scallop sizes along the sidewall can be difficult, and several techniques have been reported before, e.g. using a specially built AFM system, [121, 122] or using a conventional AFM system to scan the surface of a replica from the trench structures. [123] In our experiment, in order to quickly get a quantitative analysis for process optimization, the samples were first manually cleaved and pictured with SEM and further studied by Matlab. Based on the pixel size and coordinates of sidewall edges, the scallop sizes can be calculated and analyzed.

Two experiments were performed to prove the increased uniformity of scallop size distribution. In the first experiment, standard 50 Bosch cycles were performed with a 1.5 s deposition step and a fixed 6.0 s etch step. The etch depth was 29.4 µm as shown in **figure 3.17a**. In the second experiment, to counteract the effect of changing scallop size and profile straightness due to ARDE, the SF_6 time was linearly ramped from 3.5 s to 8.5 s during 50 DREM cycles. The other parameters were unchanged. The etch depth was 27.5 µm as shown in figure 3.17b. Although the etch depth of exp.1 is slightly larger than in exp.2, the scallop sizes can be observed to be more uniform when ramping is performed for the etch step duration. The samples were also cleaved manually along the trench openings, which gave a direct view of 2D sidewall surface as shown in figure 3.17. The etch profiles of both experiments were extracted from SEM images using Matlab, from which we can clearly see an increased uniformity of scallop sizes and profile straightness when performing time ramping. By extracting the brightness matrix of the SEM images as shown in **figure 3.18**, and performing a 2D fast Fourier transform (FFT) of the images, we can also notice a less high frequency noise and a better periodicity of the scallops.

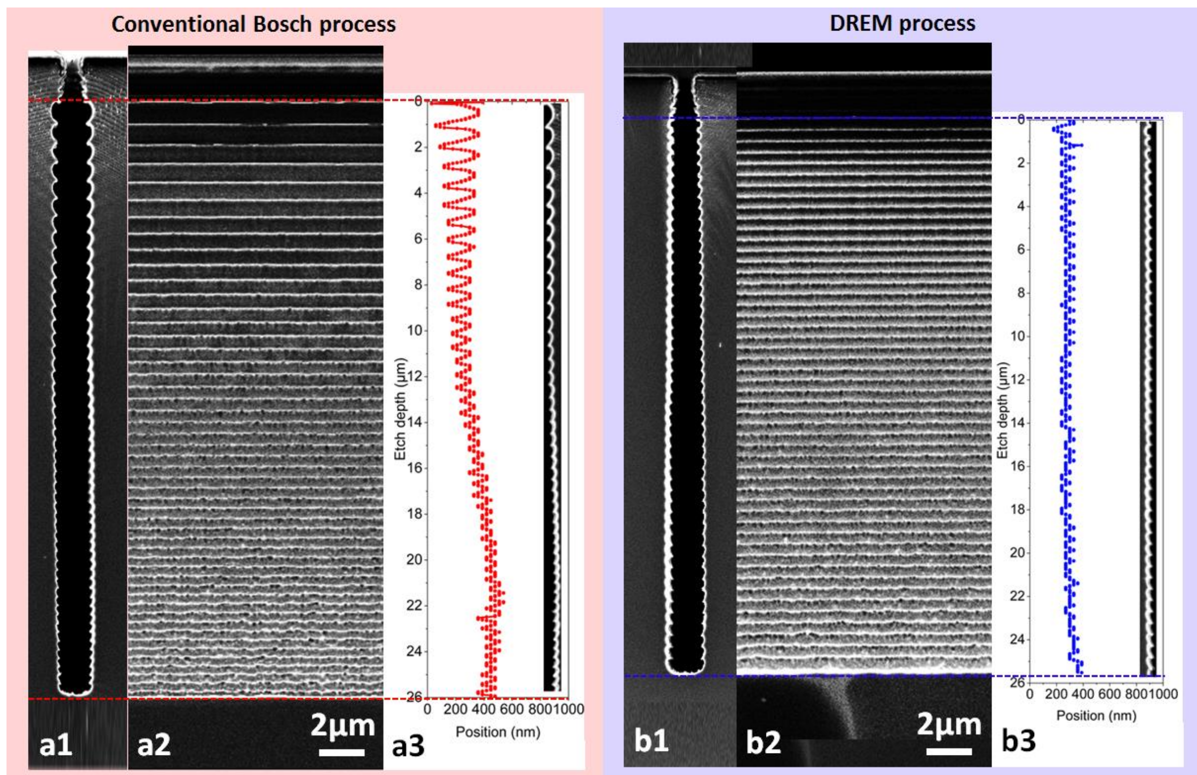


Figure 3.17. Etch profiles of 1 µm trenches (a1) without ramping performed and (b1) with ramping performed; A 2D surface view of sidewall surface (a2) and (b2); Extracted etch profiles (a3) and (b3).

This decreasing scallop size (etch rate in each cycle) for an increasing AR is caused by the well-known etch nonuniformity called ARDE. Some studies explain this by ion angular distribution, which will cause depletion of ions and radicals along the trench and slow down the etch process. [124] Other studies suggest attenuated neutral transport along the trench passage to be the reason. When AR increases, the etch rate (scallop size divided by cycle time) for both experiments decreases as shown in **figure 3.19a**, nevertheless, while in Exp.1 the average scallop size decreases monotonically, the scallop sizes for Exp.2 remains roughly identical (507 nm with 40nm standard deviation) as shown in figure 3.19b. The etch depth as a function of time is still nonlinear for both experiments as in **figure 3.20a**, which also suggests a decreasing etch rate, which is described by the slope of the curves. However,

the etch depth as a function of number of cycles (figure 3.20b) is linear for Exp.2. A qualitative explanation of this linear relation can be, that in our experiments the linearly increasing etch time can compensate for the decreasing average etch rate, which can be approximated as a quadratic function of aspect ratio. [125] However, depending on different models, the relation between the average etch rate and aspect ratio can be more complicated, [126, 127] and for HAR etching, a quadratic fitting will deviate from the real average etch rate, thus a linearly increasing etch time will not be sufficient to compensate for the drop of average etch rate.

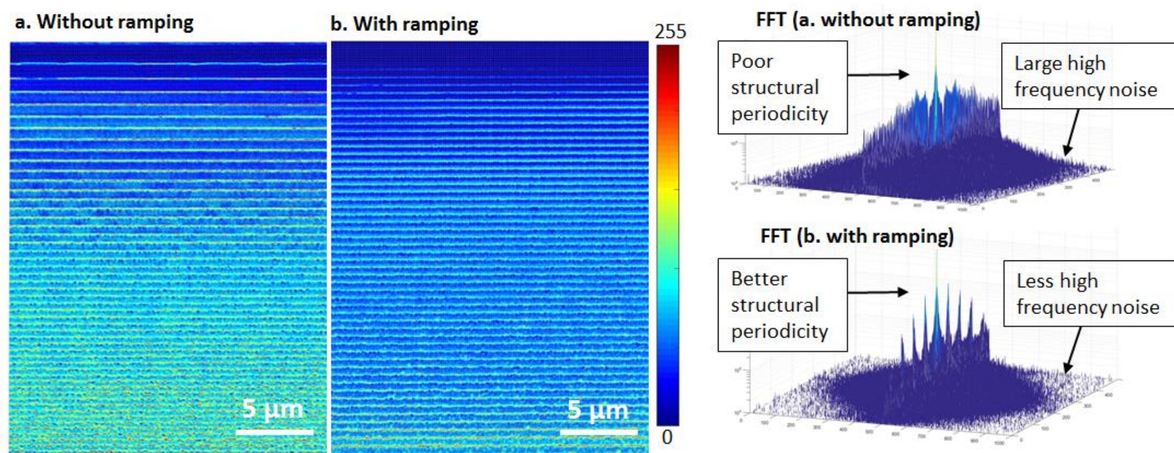


Figure 3.18. Extracted 2D sidewall surfaces from SEM images showing the brightness from pixel points, and 2D FFT of the images showing better periodicity and less roughness when ramping is performed.

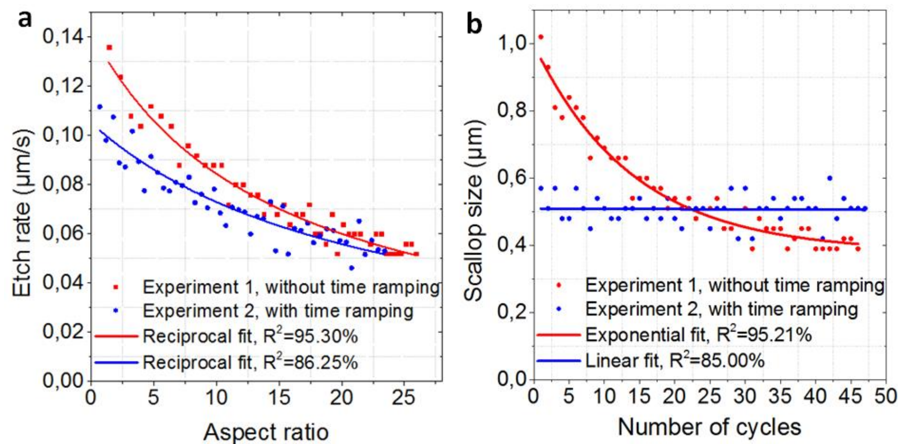


Figure 3.19. (a) Etch rate as a function of AR; (b) Scallop size as a function of number of cycles.

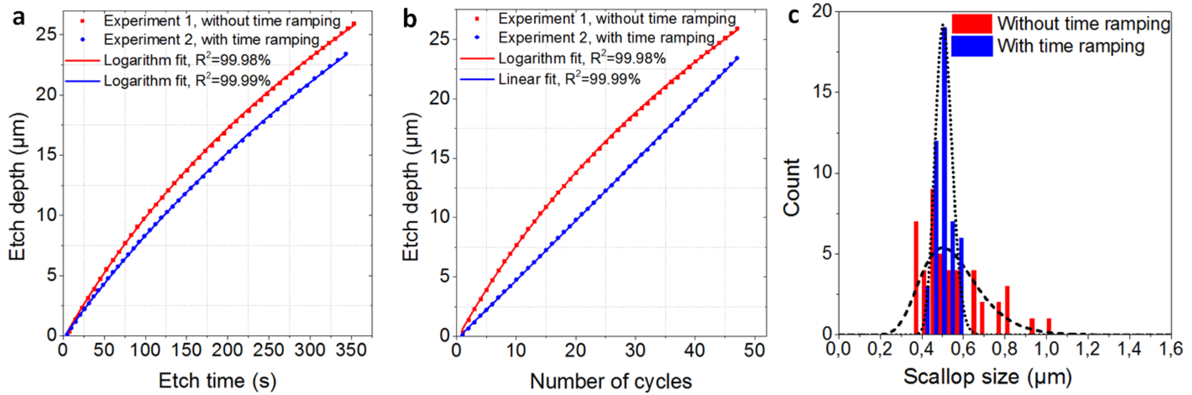


Figure 3.20. Etch depth as a function of (a) etch time and (b) number of cycles; (c) scallop size distributions with and without ramping.

Side effects generated by other process steps

Sometimes etching nonuniformity can be caused by defects from other processing steps. For example, when defining patterns with UV lithography in a hard contact mode, particles or surface curvatures will leads to inhomogeneous contact between the mask and resist surface, thus an air disk or air wedge can be created, and a constructive interference will enhance the light reflection, and photoresist in the local area will not be exposed sufficiently. This is a well-known defect in photolithography, and patterns can be disrupted. [128] For a positive tune resist, this underexposure will give resist residues after developing, when an air wedge is generated, interference will lead to periodic arrays of resist residues, hindering the following plasma etching process. If the selectivity of etch process is high enough, the shapes of resist residues will be transferred into silicon, giving etch profiles with a wave-like nonuniformity, which is shown in **figure 3.21a** and figure 3.21b, where AZ MiR 701 resist is used to define patterns of microtrenches.

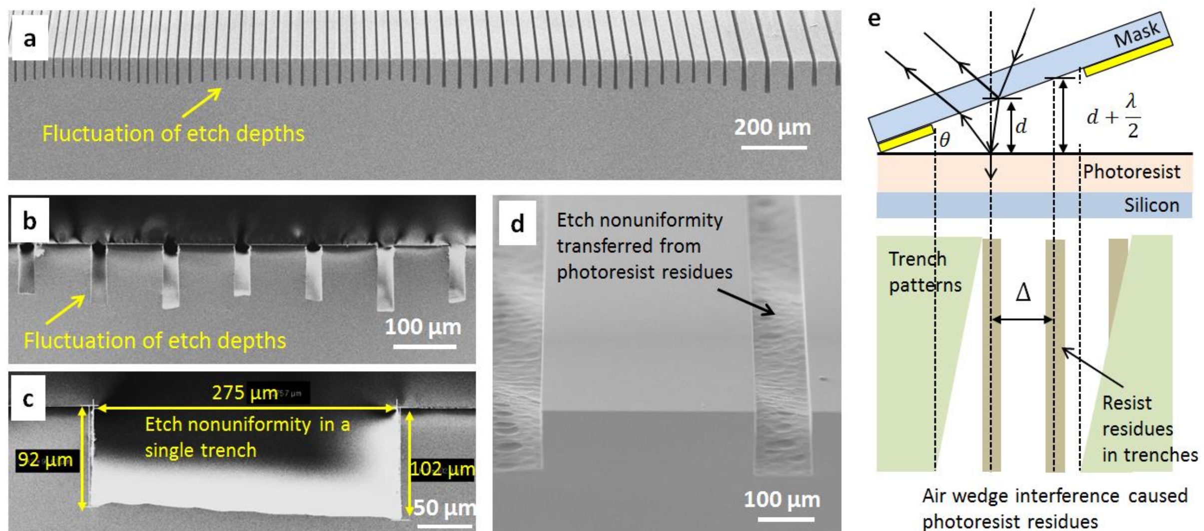


Figure 3.21. Etch nonuniformity caused by photoresist residues. (a-d) SEM images of etched trench arrays, tilted cross section; (e) Illustration of air wedge interference caused by inhomogeneous contact between mask and resist surface, which gives resist residues in the bottom of trench patterns.

In figure 3.21c, we can see that the etch nonuniformity can give a non-flat bottom in the trench cross section. In figure 3.21d, we can see the "bumps" in the trench bottom from a tilted view, the "bumps" follow the patterns of periodic arrays, suggesting the etching nonuniformity are transferred from resist residues caused by air wedge interference. An illustration to explain the patterns in figure 3.21d is shown in figure 3.21e, the distance between the arrays of resist residues is given by $\Delta = {}^{\lambda}/_{2n_0 \tan\theta}$, in which Δ is the distance between arrays, θ is angle between mask and resist surface, λ is the light wavelength for exposure, which is 365 nm on our system, n_0 is the refractive index of air. It can be seen that for $\Delta \sim 300\ \mu m$ as shown in figure 3.21d, thus the angle between the mask and resist is estimated to be around 0.04°, and the maximum height of the air wedge (corresponding to the size of a particle contamination) can be a few microns. To avoid this problem, it is always recommended to give a mask cleaning procedure after the same mask has been used for multiple times, e.g. using piranha solutions (mixed solutions of 98% sulfuric acid and 30% hydrogen peroxide in a ratio of 4:1). However, this defect can be promising to fabricate sinusoidal surfaces, e.g. by adding a wedge with thickness of 500 μm on the edge of a 100 mm wafer surface, and performing lithography with bare glass mask, then sinusoidal surface with period of 30 μm should be fabricated. This can be an interesting research topic for surface sciences and optics, [130, 139] but is beyond the topic of this thesis.

4 Etching Apparatus and Real Time Monitoring Systems

In this chapter we will introduce our etching system. Firstly we will give some technical details of hardware on our etching apparatus. Then we will discuss about the real time monitoring systems installed on the etching machine, which enables real time diagnostics of plasma conditions and etching process, and also help us to understand the technical limitations, e.g. pressure response time, set point accuracy of gas flow ratios, valve response time, etc. With all these valuable information, we can design etching processes with a good repeatability and reliability.

4.1 General introduction of etching apparatus

The etching apparatus used in our study is DRIE Pegasus (SPTS), which is a dual source inductively coupled plamsa (ICP) etching machine that is designed for etching deep structures. The plasma is generated by both an inner coil and an outer coil with 13.56 MHz RF generators, and the maximum power is 5000 W, a platen electrode is installed to provide potentials for ionic species, thus ion generation and ion bombardment are decoupled to achieve a more accurate control of etching processes. For the platen RF generator, we have options of 13.56 MHz high frequency (HF) with a maximum power of 300 W and 380 kHz low frequency (LF) with a maximum power of 500 W. The HF generator can create a high DC bias and a high etch rate of over 20 μm/min can be achieved. The LF generator is more suitable for substrate with bad electric conductivity, since both positive and negative ions can reach the surface and the accumulated charges on the substrate can then be neutralized.

The silicon wafer is clamped on the chuck by attractive coulomb force between silicon and a bipolar electrostatic clamping chuck (ESC), with a high voltage (HV) of 2 kV applied. The clamping force can be described as $F = \frac{1}{2}\varepsilon_0\kappa^2(\frac{V_{HV}-V_{DC}}{d+\kappa g})^2$ following a simple parallel plate capacitor model, [131, 132] in which κ is the relative permittivity of dielectric layer between HV electrode and wafer, V_{HV} and V_{DC} are applied HV and DC bias created during plasma process, d is the thickness of dielectric layer, and g is the gap distance between wafer and chuck. It can be seen that when the backside of silicon is contaminated by particles, a larger gap size g will reduce the electrostatic clamping force significantly, e.g. for gap size $g = 0.1d$ and a medium of alumina ($\kappa = 10$), the clamping force will be reduced by 75%. It

should also be noticed that for insulators as glass substrate, the electrostatic chuck will not give sufficient clamping force. Since the etch process of silicon is an exothermeric process, temperature of silicon wafers will rise if no sufficient cooling is performed, and a higher substrate temperature will alter the absorption and desorption rate of gas species inside plasma chamber, thus the etch rate will be varied. On our system, the wafer is cooled from backside by injecting helium gas, which has a high thermal conductivity and a high bonding energy to be ionized. The backside cooling pressure is 10 Torr, and the helium gas leaking rate is controlled to be below 20 sccm, so the effect of helium gas on gas species inside the chamber can be minimized. A platen chiller is also installed on the chuck, and the chiller temperature can be set to between -20 ˚C and 30 ˚C. The etch system is shown in **figure 4.1**.

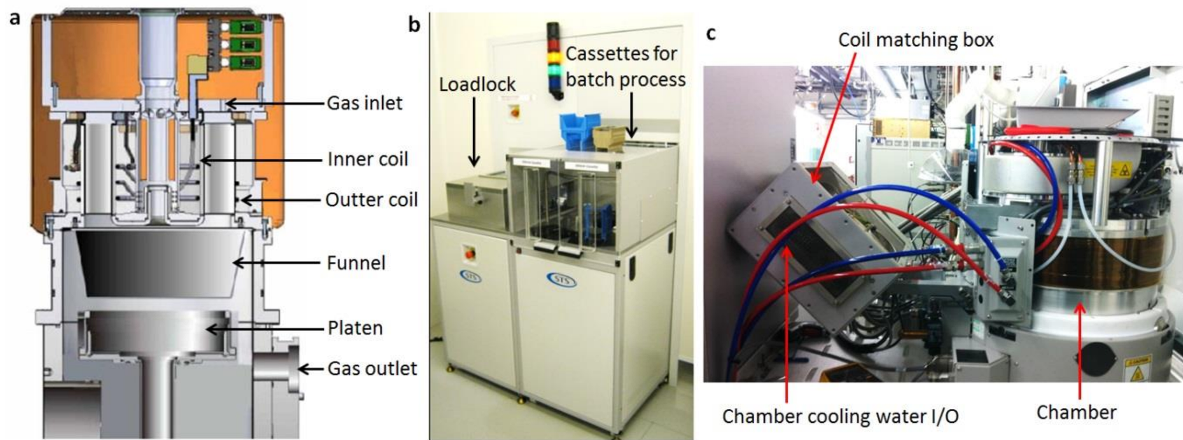


Figure 4.1. The setup a DRIE Pegasus system: (a) An illustration of the chamber setup; [133] (b) The loading system for the etching apparatus; (c) The chamber setup with no shield on.

To confine the plasma inside the chamber for a higher ion density, the system offers options of either electromagnetic confinement or physical confinement by installing a funnel. In our study, a funnel is used (to process wafers with larger sizes, the funnel also need to be modified to achieve a good etch uniformity). Since the inner surface of funnel is constantly exposed to plasma, thus can slowly get contaminated by FC layer deposition, and the deposited FC can be sputtered onto wafer surface and undermines the repeatability of etch process. To reduce this effect, the chamber is always set to a relatively high temperature at 120 ~ 140 ˚C.

Our etching system is equipped with a pendulum valve (VAT groups AG), which enables a fast and accurate control of chamber pressure by tuning the position of a throttling plate, so that the conductance of outgoing gas can be regulated. A high capacity turbomolecular pump is connected to the valve, which can give a vacuum condition with a base pressure of around 10^{-3} mTorr (for a cold chamber). The chamber pressure is measured with a Baratron manometer (MKS Instruments). Besides, a rough pump with a separate vacuum gauge is also installed.

To reduce the cross contamination from materials like metals and III-V materials, this etching system is dedicated for silicon etch. To perform etching processes, fluorine-based gases (SF_6 and C_4F_8) are used with installed MFCs to have a fast tuning of gas flow ratios. Besides, argon and oxygen gas lines are also installed with MFCs, nitrogen gases are installed without MFC for purging purposes.

4.2 GENERAL INTRODUCTION OF REAL TIME MONITORING SYSTEM

The etching parameters (gas flow rates, pressure, coil and platen reflective powers, temperature, etc) are grabbed by the sensors, and feedback control is performed by a programmable logic controller (PLC) to the etching systems. It should be addressed that even though the sensors can record the data with very high temporal resolution, the feedback system is only grabbing the data with a much lower frequency of around every 1 s. This means that the system will "overlook" and cannot respond to some fast events, e. g. a high reflective power of more than 5000 W from coil can happen within less than 1 s, if the matching unit is not in the correct position, this will create a high voltage that might be larger than the breakdown voltage of matching capacitors, and severe hardware damage can be induced. A slow reacting system is also not helpful for process development, since the parameters cannot be displayed and recorded systematically in real time, a precise analysis and diagnostics cannot be performed. In order to have a nonintrusive, in situ monitoring of etch parameters and plasma parameters, several monitoring tools are installed on our etching machine, the illustration and user interfaces are shown in **figure 4.2**. The basic functions of these tools are introduced as below:

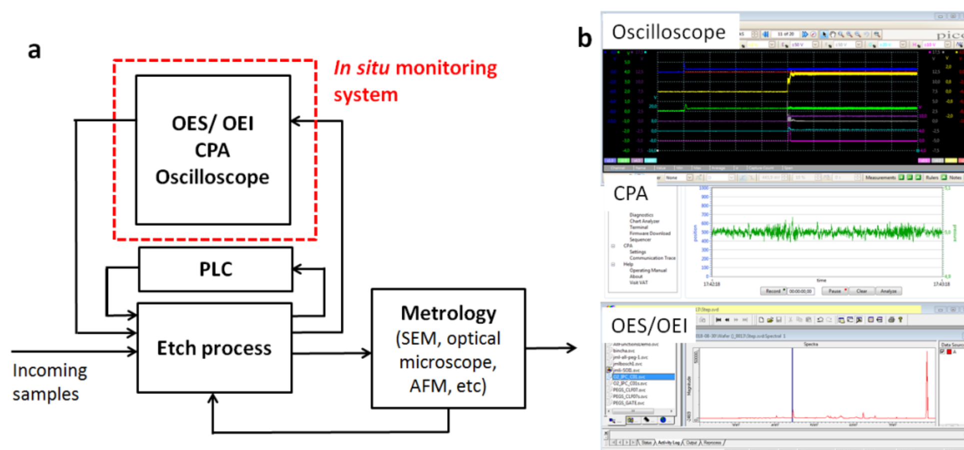


Figure 4.2. (a) Illustration of real time monitoring systems on DRIE-Pegasus etching machine; (b) Interfaces for different monitoring systems.

- Oscilloscope (Pico Technology): A digital oscilloscope with fast sampling rate is installed to read the sensor data. 8 parameters with special interest are monitored: SF_6 gas flowrate, C_4F_8 gas flow rate, processing pressure from the Baratron vacuum gauge, platen electrode DC bias, forward power and reflective power from platen RF generator, forward power and reflective power from coil RF generator. A maximum sampling rate of 80 MS/s is possible, which enables monitoring with high temporal resolution of 12.5 ns.
- Control performance analyzer (CPA, VAT groups AG) enables real time monitoring of processing pressure and throttle position of the pendulum valve. The temporal resolution can be around 20 ms.
- Optical emission spectroscope (OES) is used for time resolved monitoring of optical emission spectrum caused by photon generation from de-excited electrons, thus the species inside the plasma can be identified, and endpoint detection can be realized. The wavelength range is from 200 nm to 800 nm, with a wavelength resolution of 0.5 nm, and a temporal resolution of 0.5 s.
- Optical emission interferometer (OEI) is a interferometric tenchnique derived from OES. The time evolution of optical emission spectrum is recorded, and multi-wavelength

signals are analyzed to monitor the real time etch rate of a thin film or high contrast silicon grating structures.

These in situ monitoring systems will be introduced in details in this chapter.

4.3 Real time monitoring with control performance analyzer (CPA)

The processing pressure is one of the most important parameters for an etching process. Since the mean free path of radicals and neutrals and the ion angular distributions are highly dependent on the processing pressure, thus a variation of pressure can give a strong influence on the final etch profile. In this part we will have a brief discussion about how to monitor the pressure in situ and to control the pressure for different gas species. We also have to know about the technical limit of pressure controlling, e.g. the response time, which is crucial for a switched Bosch or DREM etching process. Here, the control performance analyzer (CPA, VAT groups AG) is installed to enable real time monitoring of pressure and throttle position, with a good temporal resolution of around 20 ms.

Firstly, the relation between valve position and measured pressure is calibrated as shown in **figure 4.3a**. We can see that for 200 sccm O_2 gas flow (without coil power or platen power), the minimum pressure is 3.38 mTorr with valve fully opened. In order to increase the pressure to above 10 mTorr, the valve position should be less than 10%. It can also be seen from the figure that when the valve position is below 10%, a minor change of the valve opening will cause a drastic change of pressure, thus a manual control of valve position in this region should be avoided for a precise control of pressure. It should also be addressed that changing the platen position will not give a big influence on the pressure (less than 1% difference), even though the funnel is physically confine the space for the incoming gases. In order to reach a higher pressure, the gas flow rate can also be increased as in figure 4.3b and figure 4.3c.

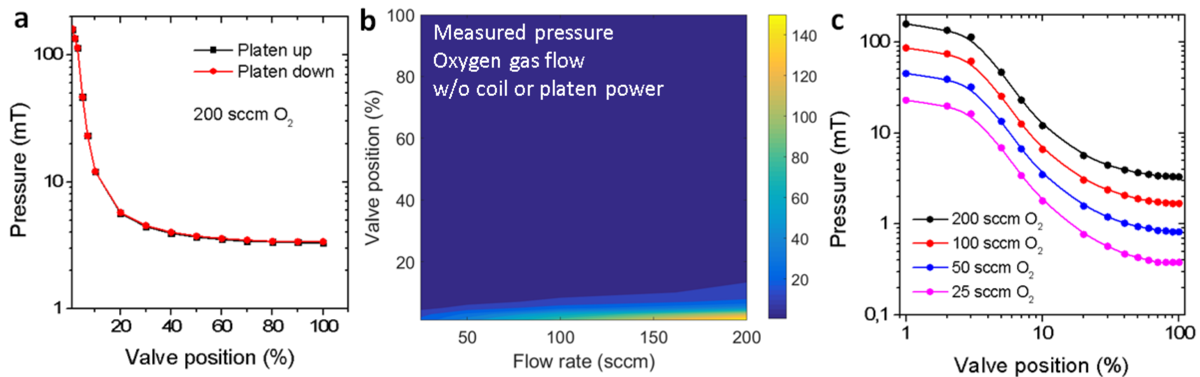


Figure 4.3. Relation between valve position, gas flow rate and measured pressure.

It should be noticed that even applying the same gas flow rate, the measured pressure will be different for different gas species. **Figure 4.4a** shows the pressure increase with an increasing gas flow rate (valve position fixed at 1% without coil power or platen power), For gases with small molecular weight (Ar and O_2), the measured pressure is smaller than gases with a large molecular weight (SF_6 and C_4F_8). This can be explained as below: different gas molecules have the same kinetic energy when temperature is fixed, larger molecules have a smaller velocity and thus more difficult to be captured and pumped out by the turbomolecular pump, which will lead to a higher measured pressure. For heavy

C_4F_8 molecules, a high pressure of over 200 mTorr can be reached as shown in figure 4.4b, however, since the mean free path of gas molecules decreases to around 250 µm at 200 mTorr, the turbomolecular pump cannot work efficiently to maintain such a vacuum condition. All the above discussions about the vacuum pressure are in a situation where no coil power is applied, thus no ionic or radical species are generated. When the RF generator is turned on for the coil source, the measured pressure will increase, especially for C_4F_8, which is a large molecular compound and can be ionized or dissociated into smaller ions and neutrals, while for smaller molecules as O_2 and Ar, this change is almost omittable even with a high coil power of 2000 W as shown in figure 4.4c.

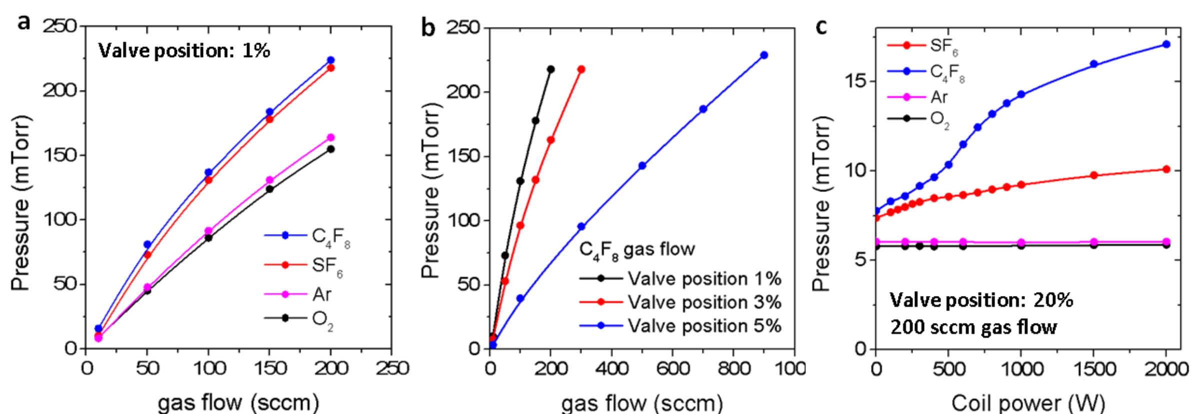


Figure 4.4. (a) Pressure for different gas species; (b) relation between pressure and C_4F_8 gas flow with different valve positions; (c) pressure change caused by applied coil power.

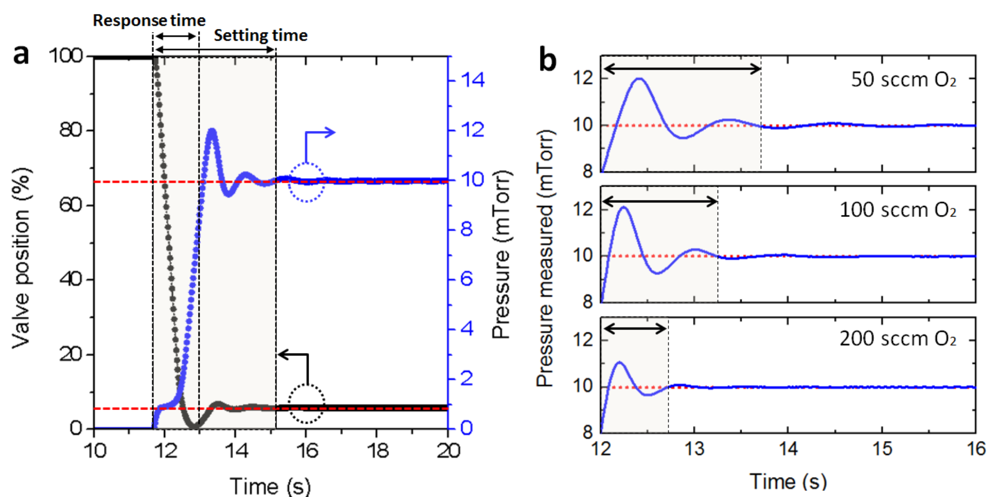


Figure 4.5. Valve response to reach a pressure setpoint.

Since the valve position is controlled mechanically and it always takes some time, before the valve position and pressure are stabilized to the set point, we have to investigate the limit of the setting time. Here we applied three different gas flow rates of O_2 (50 sccm, 100 sccm and 200 sccm), and the pressure is set to be 10 mTorr. It can be seen from **Figure 4.5a**, that for gas flow rate of 50 sccm it takes around 4 s of setting time, before the valve position reaches the set point, and pressure is stabilized to 10 mTorr with a variation of 1%. When the flow rate is increased, the stabilization time decreases, as shown in figure 4.5b. However, it should be noticed that even though the same pressure can be achieved with different gas flows, a higher gas flow rate can generally lead to a higher density of ions and radicals, thus

lower plasma temperature. These factors will give an influence on the etching process, especially the profile of etched structures.

In switched Bosch process or DREM process, different processing pressures are often assigned for different steps during an etch process, e.g. a relatively high pressure (e.g. more than 10 mTorr) is favorable for passivation steps, since the sidewall can be protected efficiently; while a lower pressure (e.g. below 5 mT) is favored during removal steps to achieve a straight profile, since a sharper IAD can be achieved. Thus the valve should have a reasonable fast response to enable the switching between different pressure setpoints during a Bosch process or a DREM process, and we have already seen earlier that few seconds is required for pressure stabilization. Here we switch 50 sccm O_2 with two pressure set points: 5 mTorr and 10 mTorr, the duty cycle is 50%, and the total period is decreased from 10 s to 1 s as shown in **figure 4.6 (a-d).** For a long period of 10 s and 4 s, the pressure and valve position still have enough time to reach the correct positions, however, for shorter periods, the pressure and the valve movement cannot follow. Since a stable plasma condition is always favored for a repeatable and controllable etching process, the lower limit of the switched process period should thus be aware of, if the pressure is switched manually between different steps. In this study, to prevent the pressure fluctuation caused by valve movement, the valve position is mostly fully opened at 100%.

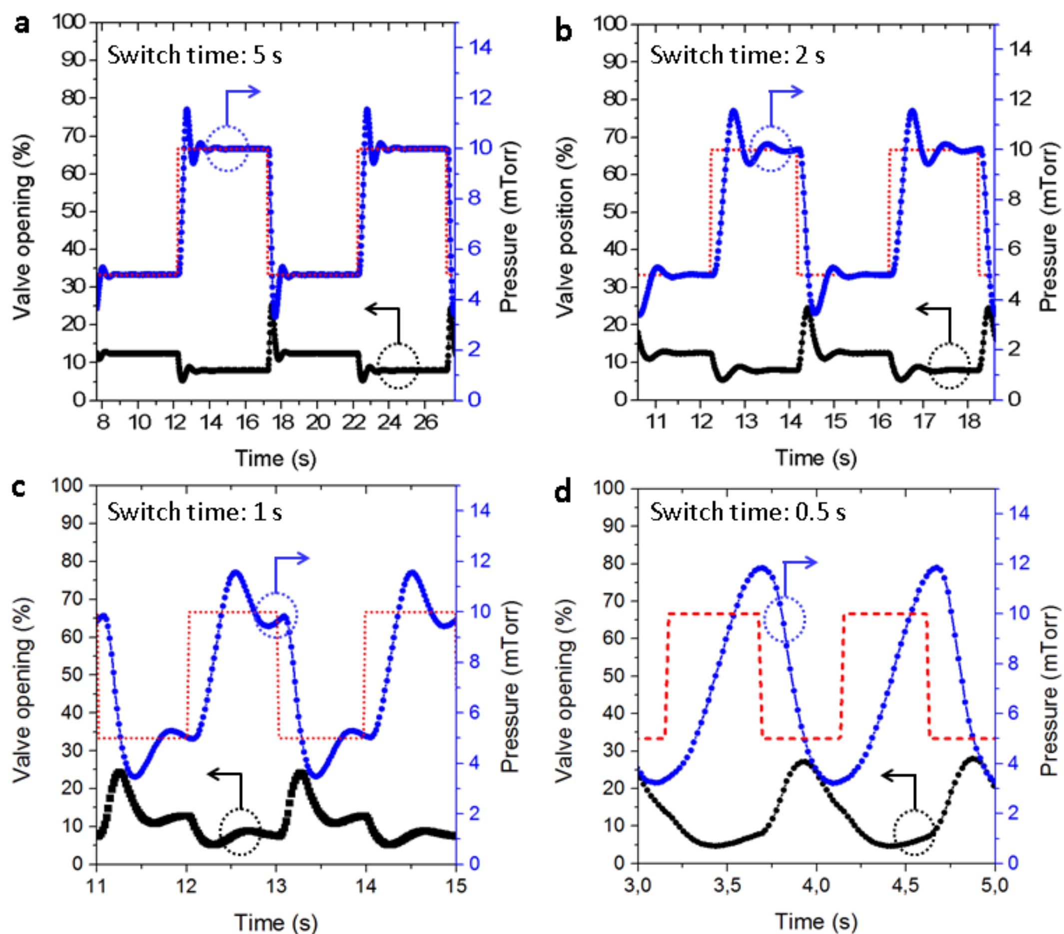


Figure 4.6. Response of valves and pressure in a switched mode with different switch time: (a) 5 s; (b) 2 s; (c) 1 s; (d) 0.5 s. 200 sccm O_2 was used without coil power or platen power applied, the pressure was set to switch between 10 mTorr and 5 mTorr. The red dot line is the targeted pressure.

4.4 Real time monitoring with oscilloscope

As introduced earlier, the oscilloscope (Pico Technology) is picking up the sensor data directly, and displays at a much higher temporal resolution compared with the PLC system on the etching machine. In this part, we will introduce how the oscilloscope can be used to study and optimize etching processes.

On our system, 8 parameters are monitored separately with a maximum time resolution of 12.5 ns. The 8 chosen parameters are the ones which we are mostly interested in, including: gas flow rates of SF_6 and C_4F_8 measured on MFCs; processing pressure measured on the Baratron manometer; DC bias on platen electrode; forward and reflective power on the coil generator; forward and reflective power on the platen generator. The first four parameters are calibrated as below in **figure 4.7**, with x-axis as the measured parameter values, and the y-axis as the outputs on oscilloscope. It should be noticed that since MFC of SF_6 has a higher capacitance (1200 sccm) compared with MFC of C_4F_8 (400 sccm), a larger variation of SF_6 flow readout should be expected.

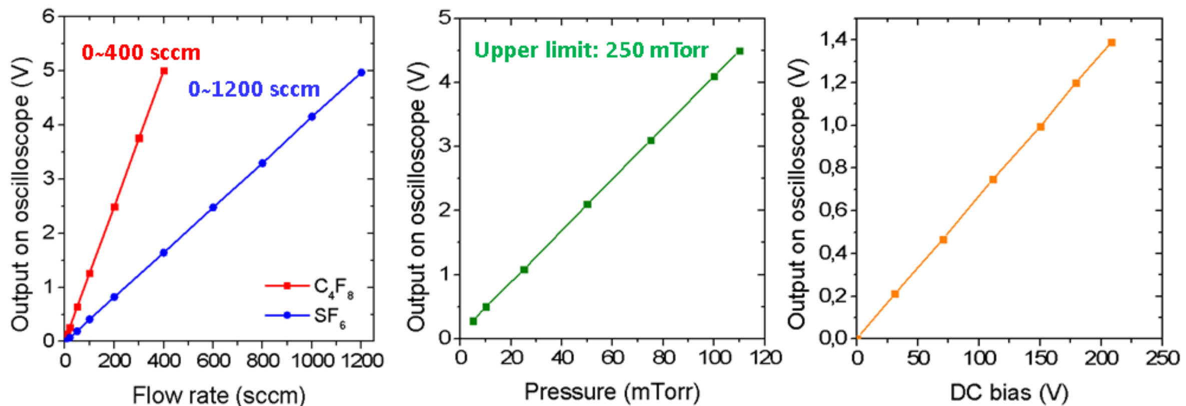


Figure 4.7. Calibration of measured parameter values corresponding to the outputs on oscilloscope.

The first parameters we are going to investigate with oscilloscope are the gas flows of C_4F_8 and SF_6, since these are the gases that are most frequently used during Bosch or DREM processes. On our etching apparatus, several thermal based MFCs are installed to give an accurate flow control over gas flows. As discussed earlier, it takes a few seconds for the processing pressure to stabilize due to the movement of the pendulum valve. Here we will also see that the MFCs can also introduce inaccuracy of gas flow rate and a time delay for gas stabilization. Different gas flow rates are applied for C_4F_8 and SF_6 with the whole range of gas flow capacitances, the valve position was 100% all the time without power applied. From **figure 4.8a** we can see that a short response time of around 50 ms is required for the C_4F_8 gas flow when the gas line is turned on from 0 sccm. However, an overshoot is observed, which will introduce a delay for gas stabilization, and the total setting time can be more than 0.5 s for a small gas flow of 10 sccm. The variation of C_4F_8 gas flow (known as set point accuracy or S. P. accuracy) is below 1% when the flow rate is larger than 100 sccm, for smaller gas flow rate, an relatively unstable gas flow can be expected, and thus a less stable plasma condition. For SF_6 gas flow, a longer response time of 0.25 s is observed for flow rate larger than 1000 sccm, for smaller gas flows, a overshoot can be seen as for the C_4F_8 gas flow, and the total setting time can be more than 0.5 s for a gas flow rate smaller than 50 sccm. A lower S. P. accuracy is shown for SF_6 gas flow compared with C_4F_8, it will say, to reach a S. P. accuracy of less than 1%, more than 250 sccm SF_6 should be used.

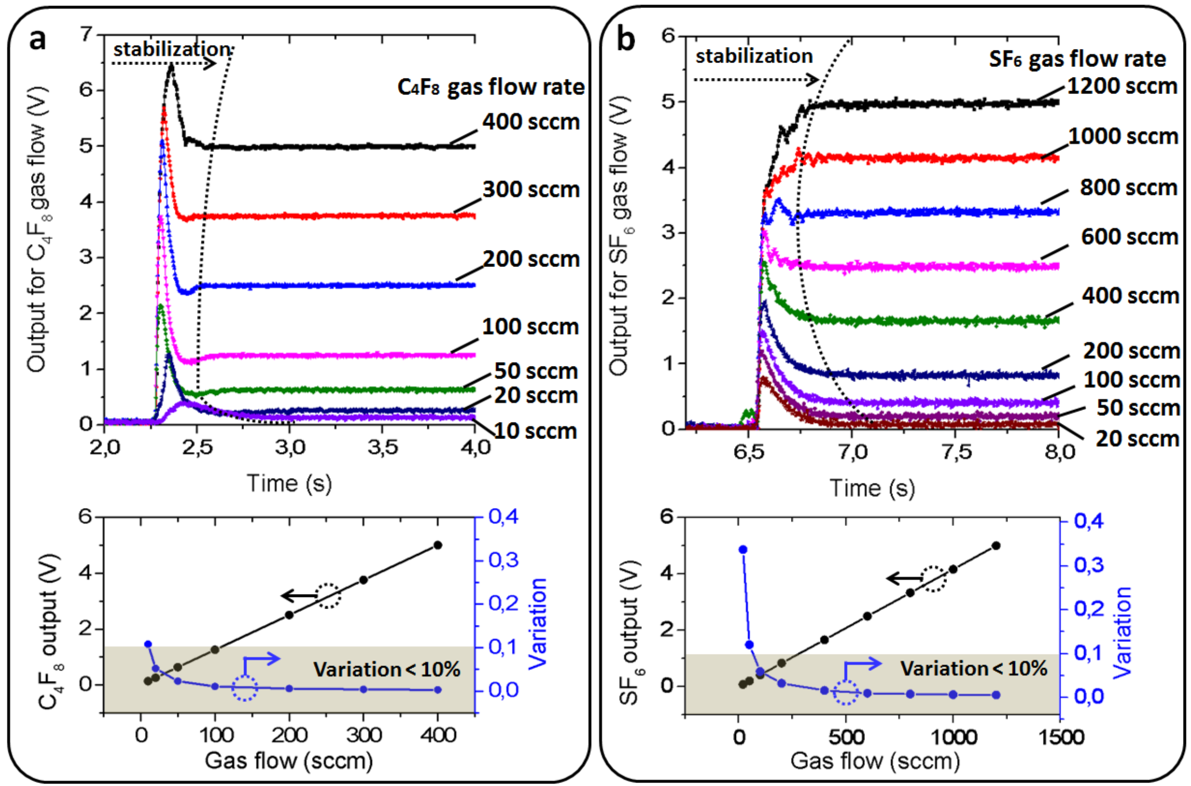


Figure 4.8. Gas flow rate outputs on oscilloscope: (a) C_4F_8 and (b) SF_6. The S.P. accuracies of MFCs are also shown below in the images.

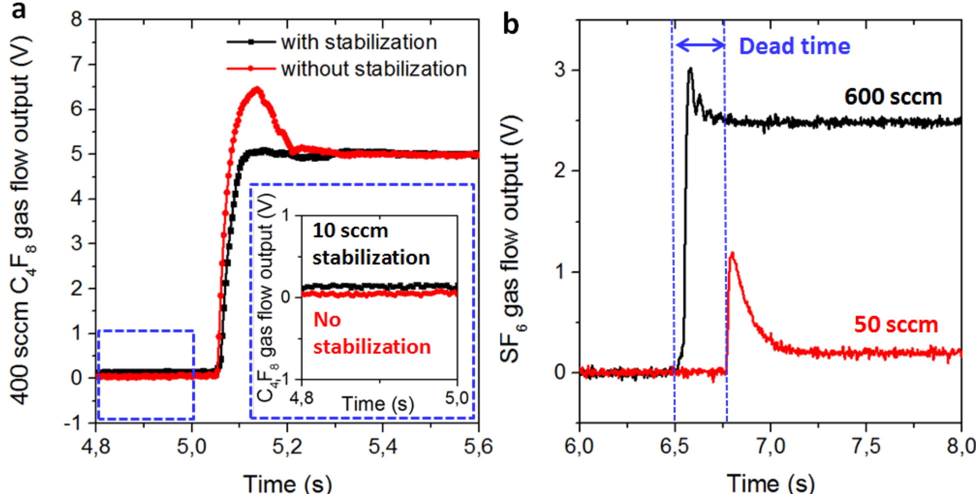


Figure 4.9. (a) Applying gas stabilization to reduce the overshoot of gas flow; (b) The dead time of SF_6 MFC when a small amount of gas flow is applied.

From the above discussion, we can see that either a large gas flow or a small gas flow can lead to a long setting time of around 0.5 s, this will set limit to our etch process, especially for switched processes. In order to avoid an unstable plasma condition caused by unstabilized gas flow rate, a proper amount of gas flow should be applied, and the duration of different steps should be sufficiently larger than the setting time. To reduce the overshoot of gas flow rate, a stabilization gas flow can also be applied, instead of shutting the gas line totally. As shown in **figure 4.9a**, a much smaller overshoot of C_4F_8 gas flow can be achieved when the flow rate switches from 10 sccm to 400 sccm, while a large overshoot is shown

when flow rate switches from 0 sccm to 400 sccm. Since the influence of 10 sccm C_4F_8 gas on the etch process is quite limited, we can always keep the "background" C_4F_8 gas flow rate at 10 sccm, thus allowing for a better controlling of gas flow and thus pressure condition.

For small gas flows, some extra issues should be addressed: firstly, a lower S. P. accuracy is observed, especially for SF_6 gas flow, this will give some challenges for nanoscale etching, where small amount of gas flows are favored. Another issue is the dead time associated with a small gas flow amount, meaning that there is a delay of time after the demand is sent to the MFC, before MFC starts to respond and flow rate can be registered. This is shown in figure 4.9b, for 50 sccm C_4F_8, it takes around 0.25 s extra time for the MFC to start compared with 600 sccm C_4F_8 (sometimes the dead time can even be few seconds). This issue can be solved by replacing current MFCs with MFCs that are dedicated for a smaller range of gas flows.

4.4.1 Pressure response monitoring

Since the etching apparatus has a large chamber volume, and there is a distance between MFCs and chamber connected by the pipe lines, it will always takes some time for the pressure to rise and stabilize, even when MFCs are already opened for gas flows. This is shown in **figure 4.10a** and figure 4.10b, it can be seen that after 200 sccm C_4F_8 or SF_6 gas are turned on and reach the set values, around 1.5 s time delay is required, before pressure can be stabilized (the valve position is set to be 10%). It would be expected that, if the coil generator power is turned on in the same time with the gas flows, the pressure will still not be settled and an unstable plasma condition might lead to a high coil reflective power (which will be discussed later). The difference of the outputs on C_4F_8 and SF_6 gas flows is due to different capacitances of MFCs, and the pressure difference measured is caused by the molecular weight difference of two gas species, which has been discussed earlier. It should also be noticed that during a process, where the coil generator is turned on to generate plasma, the processing pressure will increase depending on the gas species, as shown earlier in section 4.3. It can be seen in figure 4.10c that when 1500 W coil power is applied after pressure is stabilized, an increase of pressure outputs with around 100% can be observed (200 sccm C_4F_8 is applied with 10% valve position), this agrees with previous discussions.

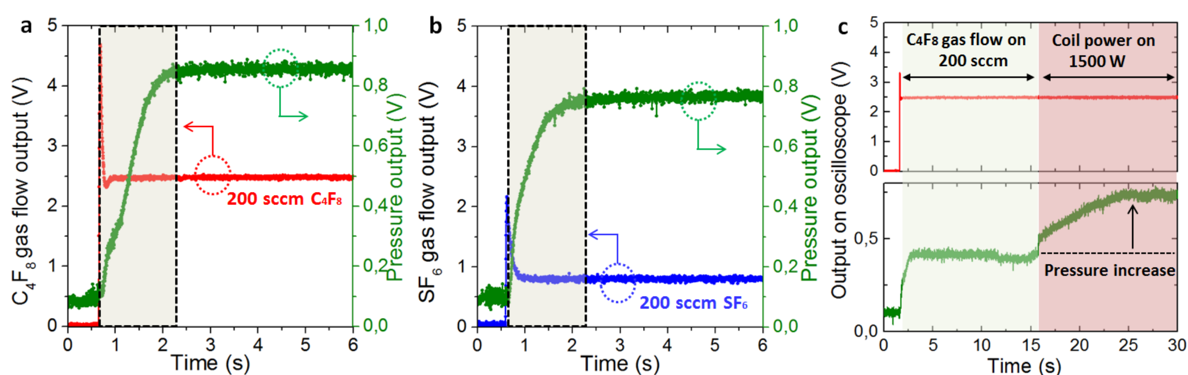


Figure 4.10. Monitoring pressure response with oscilloscope: (a) Pressure response for C_4F_8 gas flow; (b) Pressure response for SF_6 gas flow; (c) Pressure response for C_4F_8 gas flow with coil power applied.

The pressure response time can be crucial during a switched Bosch process or DREM process, where the pressure should be relatively stable in each of the steps, otherwise the repeatability of the process can be undermined. **Figure 4.11** shows 200 sccm SF_6 in switch mode with different switch times (0.1 s, 0.2 s and 0.5 s). From the oscilloscope output of gas

flow rates and pressure, we can see that for short switch time of 0.1 s, the gas flow rates cannot be switched between two stable states, giving a quite unstable pressure condition; when the switch time is increased to 0.5 s, the gas flow rates can fully reach the target position and stabilize, and the pressure outputs show a clear difference between the gas on and gas off states. When designing a Bosch process or a DREM process, the switch time during each step should be sufficiently large for the pressure to stabilize.

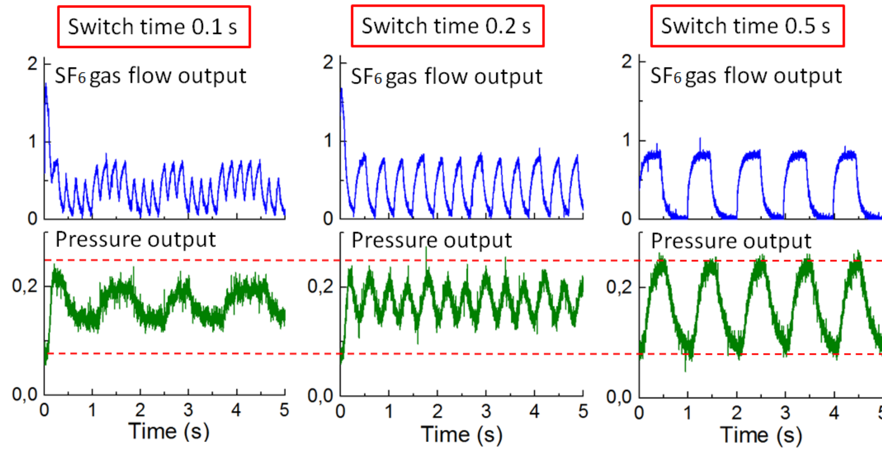


Figure 4.11. 200 sccm SF_6 in switched mode with different switch times and the pressure outputs.

4.4.2 Coil reflective power monitoring

When the chamber condition (e.g. pressure, gas flow, etc) is not stable, a high reflective power can be observed from coil generator, which can lead to a failure in plasma ignition or even arcing in the components of etch apparatus.

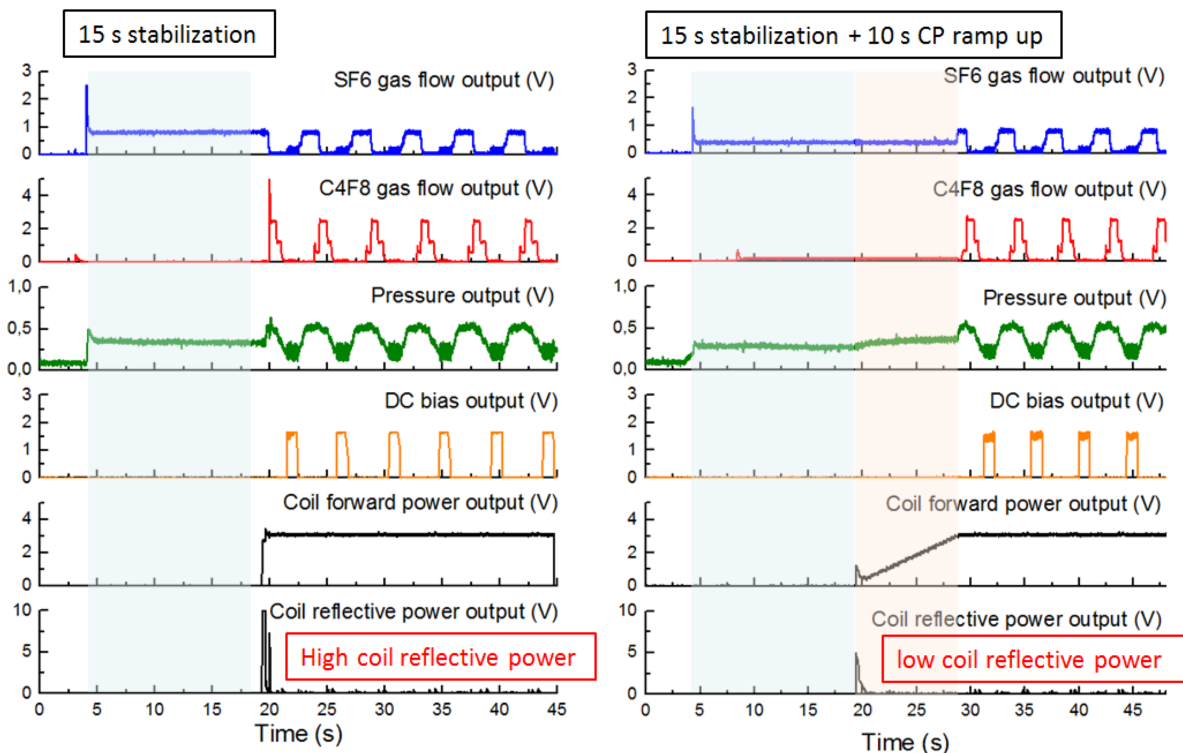


Figure 4.12. Reduce the coil reflective power by introducing a power ramping up stage before the process starts.

In **figure 4.12** the oscilloscope signals from 6 different channels, when a DREM process is started and last for a few cycles. Normally gas flow is turned on for 15 s to be stabilized, before the coil power is applied, so a stable chamber condition can be reached and the coil reflective power can be minimized. However, a high reflective power can still be observed, which can generate some "spikes" in the beginning of the process. The duration of the "spikes" is less than 1 s, however, the amplitude can be larger than 6 kW and cause severe troubles both for the process and for the etching tool. In our process, the coil power is slowly ramped up from 0 W to the set point (2 kW in figure 4.12) after 15 s of gas stabilization, thus a much smaller coil reflective power is generated.

4.2.3 Platen reflective power and DC bias monitoring

In order to have an efficient power delivery in the platen electrode RF discharge, a matching network is normally used to have a good matching between the impedance of platen RF source $Z_S = R_S + jX_S$ and the impedance of the load $Z_L = R_L + jX_L$. The forward power P_F and reflective power P_R are measured on the transmission lines, the total effective load power is then given by $P_L = P_F - P_R$. Impedance mismatching can not only reduce the effective load power, but also increase the risk for RF source damage, since a high voltage caused by a high reflective power may induce arcing in source components. [134] A simple description of the load power is given as:

$$P_L = \frac{1}{4} Re(IV_L^* + I^* V_L) = \frac{1}{2}|I|^2 R_L = \frac{1}{2}\frac{|V_L|^2 R_L}{|Z_S+Z_L|^2} \leq \frac{1}{8}\frac{|V_L|^2}{R_L} \tag{4.1}$$

The maximum load power is achieved, when the impedances of source and load are matched and satisfy: $R_L = R_S$, $X_L = X_S$.

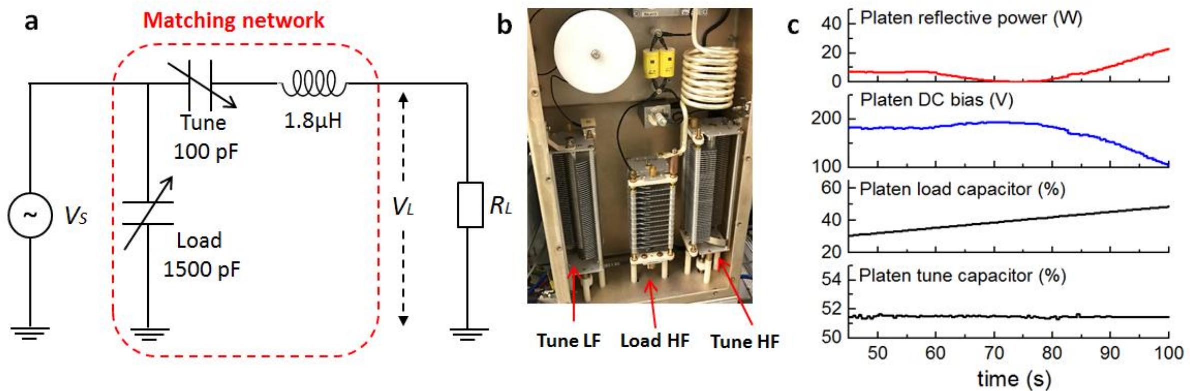


Figure 4.13. (a) A simple illustration of matching netwok in platen electrode; (b) Photographic image showing the platen matching box; (c) Reflective power measured when ramping up the platen load capacitor position.

In DRIE Pegasus etching system, a matching box with motor-driven capacitors is used: two capacitors are installed to control the magnitude and phase of RF voltage applied on the transmission line. These two capacitors are called load and tune, which are shown in **figure 4.13a** and figure 4.13b (a separate tune capacitor is also installed for LF platen generator). The load and tune capacitors should be in the optimum positions for a repeatable etching process. To show how the position of platen matching capacitors can affect the reflective power, the tune capacitor position is fixed at 51.5%, while the load capacitor position is ramped up from 30% to 50%, other parameters are: valve position 20%, platen chiller at 20°C, 200 sccm O_2 gas flow rate, coil power 200 W and platen power 50W. We can clearly

see that when the load capacitor position is at around 40%, the platen reflective power is minimized, thus the load power is maximized, giving the highest DC bias value (figure 4.13c). However, it should be noticed that the capacitors are driven mechanically by motors, which sometimes can be retarded to response the change of plasma condition. Thus in our study, the positions of both load and tune capacitors are normally preset, so the process can have a good starting point without delay caused by matching network stabilizations.

Platen DC bias V_{DC} and peak-to-peak voltage V_{PP}, which have been introduced in chapter 3, can also be monitored during an etching process, and some general information of plasma etching can be studied. In **figure 4.14a** we can see that both V_{DC} and V_{PP} increase with the platen power, when the same amount of O_2 gas flow is applied (coil power fixed at 200 W). This is understandable, since the ion current is almost constant defined by the coil power, thus $V_{DC} \propto W_p$. When decreasing the gas flow rate from 200 sccm to 100 sccm, both V_{DC} and V_{PP} decrease slightly, implying a reduced ion density for 200 sccm O_2, which might be due to a smaller mean free path. In figure 4.14b, we can see that the platen DC bias decreases with an increasing coil power because of an increased ion current. When the pressure is increased, more ionic species are generated giving a larger ion current, thus V_{DC} and V_{PP} will reduce as shown in figure 4.14c and figure 4.14d. For large molecules of SF_6 and C_4F_8, more charges are generated during ionization compared with small molecules of O_2 and Ar, thus V_{DC} and V_{PP} will be lower. As mentioned before, DC bias is an important parameter to characterize ion energies and the influence of physical sputtering. By performing real time monitoring on DC bias, an adequate amount of bottom removal can be applied and DREM process can be optimized.

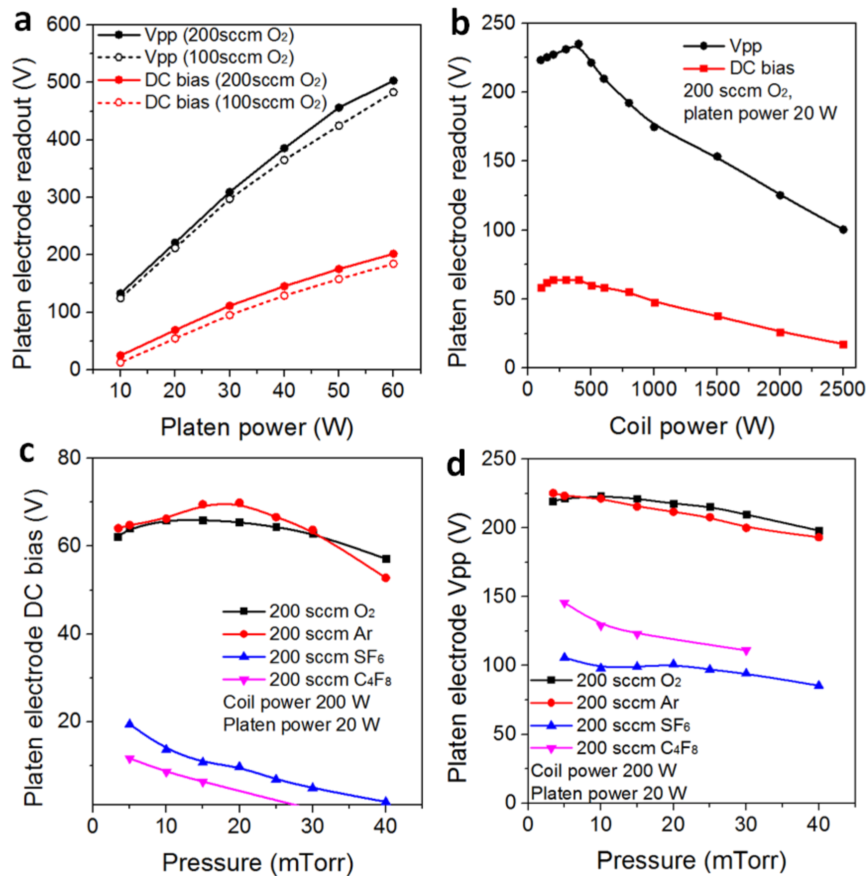


Figure 4.14. Platen DC bias and peak-to-peak voltage when changing different parameters: (a) Platen power; (b) Coil power; (c-d) Pressure and gas species.

4.5 REAL TIME MONITORING WITH OPTICAL EMISSION SPECTROSCOPY (OES)

Optical emission spectroscopy (OES) is a standard method for non-intrusive in situ plasma diagnostics. When the plasma is ignited by external RF electromagnetic field, the ion densities and electron temperature will increase, thus electrons can attain sufficient kinetic energy to impact and excite neutral atoms. A transition of electron energy levels will take place from ground state (with energy of ξ_i) to excited state (with energy of ξ_{i^*}), which is unstable and can release to a lower energy state (with energy of ξ_f). The emission wavelength is given by $\lambda = \frac{2\pi c}{\omega}$, in which ω is the angular frequency: $\omega = \frac{e}{\hbar}(\xi_i - \xi_f)$. The relaxation time of the excited state is on the order of 10 ns, [135] which is much smaller than the time resolution of 0.1 s on our OES system, thus sufficient integration time can be achieved to have a stable time averaged spectrum. Since the optical emission process follows the classic selection rules, which is again determined by the quantum numbers of the atomic systems (e.g. azimuthal quantum number, spin quantum number, etc), thus the optical emission spectra can be used to identify different chemical species inside a plasma. Since the emission signal has a quite small linewidth on the order of 0.01 Å caused by Doppler broadening (much smaller than the wavelength resolution of 5 Å on our OES system), this method can be quite accurate to trace down the "finger prints" of plasma species. Apart from the position of the spectra lines, the intensity of the emission can also give us information such as plasma temperature [136] and ion densities. [137] It should be noticed that, apart from photon emission caused by interlevel energy transition of excited atoms, the vibrational energy relaxation of molecules can also give photon emissions, when the molecules are excited into a vibrational mode with higher energy, however, the wavelength of the emitted photons is normally in the infrared region.

An illustration is given in **figure 4.15** to show the OES system (Verity Instruments, Inc.) installed on our etching apparatus. An etching resistant UV quartz window is used to ensure a high optical transmission in the wavelength range from 200 nm to 800 nm (the transmittance can be around 60% at 200 nm, and 90% for wavelength larger than 300 nm). The emitted light is coupled into the optical fiber on the top of the chamber, thus the plasma species over the surface of the wafer can be directly monitored. It is also important to mount the optical coupler to the chamber on an optimum position, thus a sufficient intensity of signals from plasma can be recorded, this is particularly important for optical emission interferometry, which will be discussed in the next section.

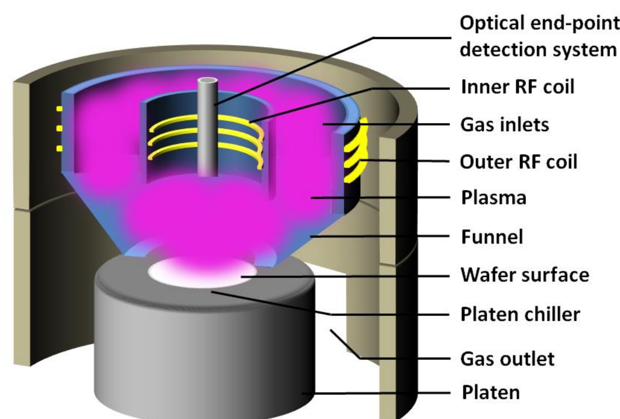


Figure 4.15. An illustration of DRIE-Pegasus system with optical end-point detection system installed.

In **figure 4.16** are some typical optical emission spectra from four different gas species: C_4F_8, SF_6, Ar and O_2. The gas flow rate is 200 sccm, processing pressure is 20 mTorr, coil power is 3000 W without platen power. A silicon dummy wafer is used with platen chiller temperature of 20 ˚C. We can see that for large molecules as C_4F_8 and SF_6, multiple spectra lines can be observed, while for O_2 plasma, we have a significant emission at wavelength of 777 nm, for argon plasma, several spectra lines can be found due to multiple kinetic processes between different energy levels (there is a cut off of intensity for Ar spectra lines around 700 to 800 nm, due to a saturated signal from CCD detector). It should be mentioned that by comparing the relative intensity from Ar I (404 nm) and Ar II line (426 nm), it is also possible to retrieve the information of electron density, with the hypothesis that the distribution of excited states and ground states follows a Boltzmann statistics. [138]

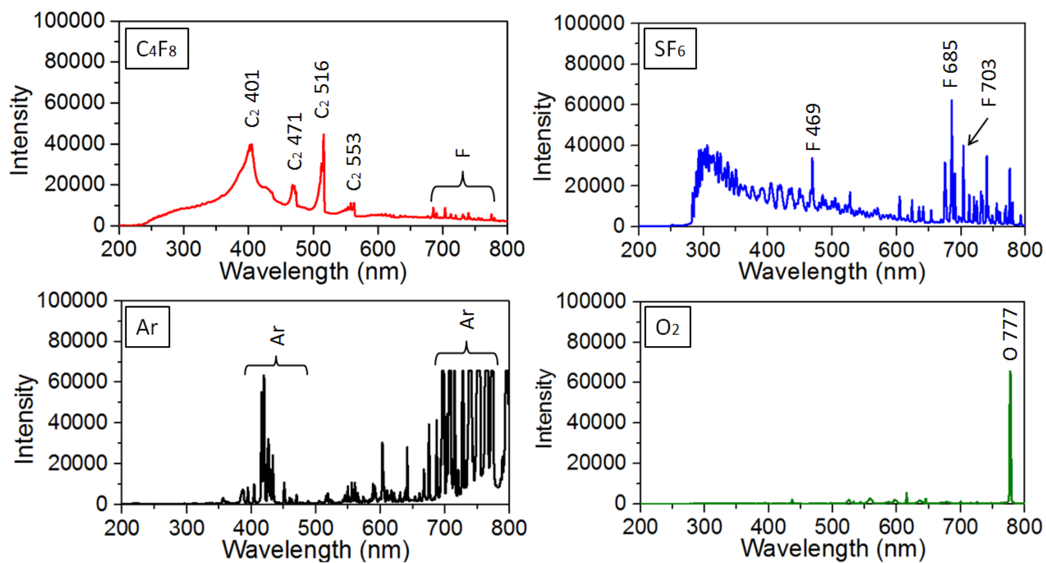


Figure 4.16. Optical emission spectra of 3 different gas species: C_4F_8, SF_6, Ar and O_2.

In order to have an optimum performance of OES system, the integration time of CCD camera should be chosen in such a way, that the white noise can be reduced, which is caused by the heated resistance in the CCD circuits, while the signal to noise ratio could be maximized. On our OES system, the maximum integration time of the CCD image sensor is 100 ms, which will give good signal intensity and a high signal to shot noise ratio, however, such a long integration time can saturate the signals on certain plasma conditions, and a higher level of white noise can also be expected. In **figure 4.17** are the OES spectrum retrieved with different integration time, the process is a continuous mixed process with both SF_6 and C_4F_8, both average intensity and standard deviation increases with the integration time, while the signal to noise ratio also increases, since the photoelectrons collected by CCD camera follows a Poisson distribution. To achieve a good signal to noise ratio and in the same time to avoid saturated signals, the integration time is set to be 50 ms in this study.

One of the most important applications of OES is the endpoint detection, [139, 140] meaning that a variation of optical emission spectra can be observed, when the chemical components of exposed sample region is changed inside plasma. Thus by monitoring the time evolution of optical emission spectra, the "end point" can be detected and etching process can be precisely controlled. This is especially useful for etching samples with multiple layers, e.g. silicon on top of insulator (SOI), [141] so that overetching and other etching defects (e.g.

notching) can be avoided. In modern VLSI industries, vertical integration of multiple layers with different materials is quite common, and OES has become a standard method to give a precise control of etching processes, together with other techniques such as laser interferometry [142, 143] and mass spectrometry. [144]

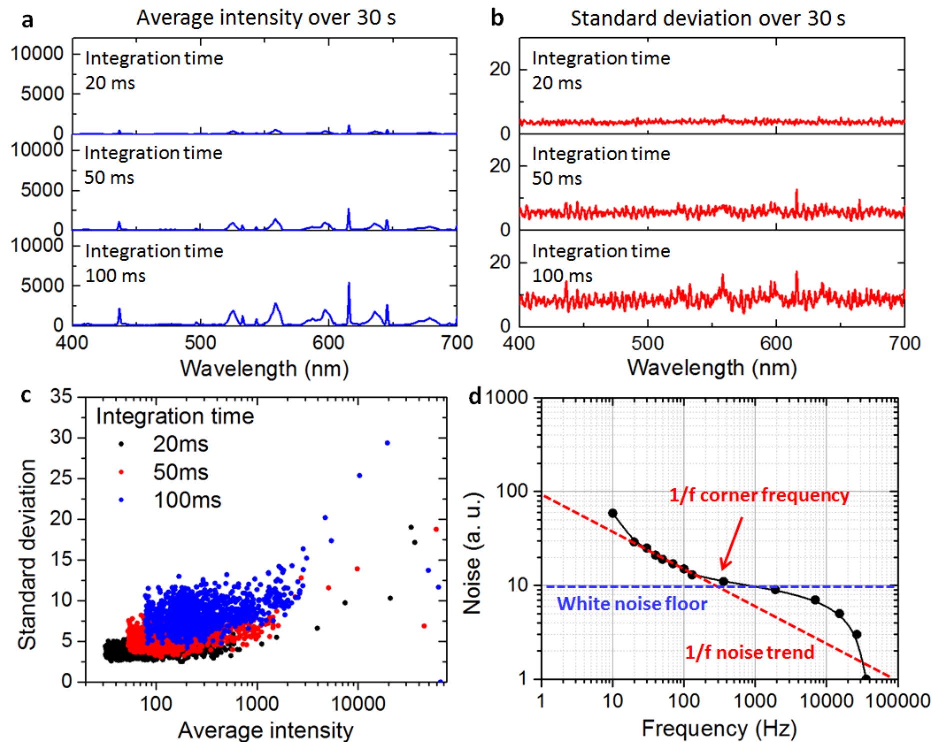


Figure 4.17. Influence of CCD detector integration time on (a) mean intensity and (b) noises. 3 different integration times are compared in (c): 20 ms, 50 ms and 100 ms; (d) the relation between noise and noise frequencies, showing the white noise floor and trend of 1/f flicker noise.

However, there are several technical challenges for end point detection with OES.

- The first is the choice of wavelengths, which are most suitable for monitoring a specific etching process. Since the optical spectra covers a range from 200 nm to 800 nm in our system, and only a few emission signals can have a significant change at the end point, thus it is crucial to choose the optimum wavelengths for monitoring. In our study, a principal component analysis (PCA) is performed to give an evaluation for all the wavelengths both before and after the end point, thus the best candidates of wavelengths can be chosen to monitor a process.
- The second is that the intensity of optical emission spectra is highly dependent on the loading area of the samples. For samples with extremely low loading area, the detection of end point can be difficult. To solve the problem, some additional data analysis can be performed to increase the signal to noise ratio. [145 - 147]
- The third is that depending on the installation position of OES system, some signals can be difficult to be captured. For example, in our system, the OES system is installed on top of the chamber in the center of inner coil generators, while the etching products SiF^*, which can generate emission signal at 440 nm, is rapidly fluorinated into SiF_4, and pumped out of the chamber, thus the SiF signal can be difficult to be observed and is normally covered by the broad C_2 peak from C_4F_8 spectrum as shown in figure 4.16. A

method to solve the problem is to install another plasma generator to crack the SiF_4 etching products, thus the signals can be monitored with another OES system. [148]

In the following sections, we will discuss how to perform end point detections of two different etching processes: one is the overetching of silicon from photoresists; the other one is to monitor the etching of BARC layer. We will see how PCA can be used to choose the optimum wavelengths for monitoring.

4.5.1 End point detection for silicon etch

The first case we are going to study is to monitor the end point when silicon is overetched from a resist layer. The sample is a 100 mm wafer covered by 1.5 µm AZ MiR 701 resist, the etching process was performed with 200 sccm SF_6 and a pressure of 10 mTorr, with 1000 W coil power and 200 W platen power. The evolution of the whole spectrum is shown in **figure 4.18a**, from which we can see that there are some wavelengths, where the intensity is increased significantly, e.g. signal from 685 nm, as shown in figure 4.18b.

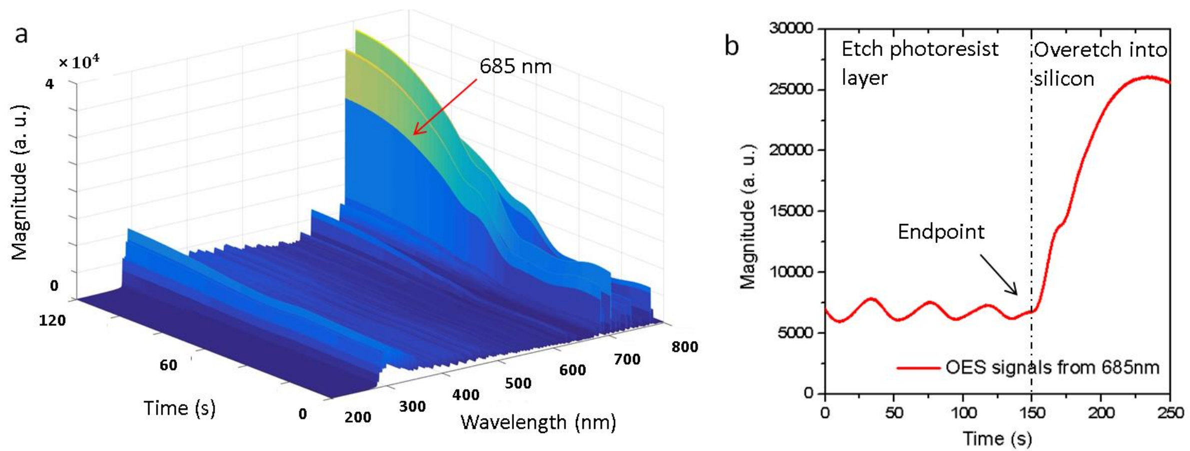


Figure 4.18. Time evolution of optical emission spectrum, when silicon is overetched from photoresist (a), endpoint can be observed on the wavelength of 685 nm.

To extract the most important information from the spectra evolution, PCA is performed, which is a popular statistic tool for multiple variants. [149] Here we use a matrix $\boldsymbol{S}$ to represent the evolution of spectrum, with dimension of $m \times n$, and each matrix element S_{ij} represents the optical emission intensity at time i and wavelength at j. The single value decomposition (SVD) suggests that such a matrix can be decomposed as $\boldsymbol{S} = \boldsymbol{P}\Delta\boldsymbol{Q}^{\boldsymbol{T}}$, in which $\boldsymbol{P}$ has the dimension of $m \times l$, $\boldsymbol{Q}$ has the dimension of $n \times l$ and is orthogonal $\boldsymbol{Q}\boldsymbol{Q}^{\boldsymbol{T}} = \boldsymbol{I}$, Δ is a diagonal matrix, with element σ_{ii} satisfying $\sigma_{ii} = 0$ for $i > n$. The SVD performed above can be interpreted as a projection of matrix $\boldsymbol{S}$ as $\boldsymbol{S}\boldsymbol{Q} = \boldsymbol{P}\Delta\boldsymbol{Q}^{\boldsymbol{T}}\boldsymbol{Q} = \boldsymbol{P}\Delta$. Since $|\boldsymbol{S}|^2 = \boldsymbol{S}\boldsymbol{S}^{\boldsymbol{T}} = \boldsymbol{P}\Delta^2\boldsymbol{P}^{\boldsymbol{T}}$, σ_{ii}^2 is the eigenvalues, and $\boldsymbol{P}\Delta$ is called the scores of the principal components, and $\boldsymbol{Q}^{\boldsymbol{T}}$ is called the loadings of the principal components. The loadings and scores are related to the measurements of OES spectra evolution, and the principal component with largest eigenvalue is called the first principal component, and having the highest contributions (the kth principal component will have the contribution defined by $ctr_{ik} = p_{ik}^2\sigma_{kk}^2/\sum_i p_{ik}^2\sigma_{kk}^2$). Briefly speaking, by performing PCA, we can make a projection of whole spectra evolution on to different components, each component corresponds to a spectrum, that has independent evolution trend compared with other components, and the component that has the highest contribution can provide the most information during the spectra evolution.

By performing PCA for the spectra evolution around the end point (where silicon is overetched from resist), the loadings and scores of the first 4 principal are shown in **figure 4.19**. From the first principal component we can see significant signals corresponding to fluorine-based species between 600 nm and 800 nm, and the score increases significantly at the endpoint. Since the resist can be thought of as chemically inert to fluorine-based etching species, thus when resist is removed physically and silicon is exposed, the generation of SiF_x etch reactants will break the equilibrium of fluorine-based chamber chemistry, more fluorine-based ions and radicals will be generated and increase the intensity of emission peaks. It should be noticed that the optical properties of sample surface can also give an influence on the measured optical emission signals, since silicon surface has a higher reflectance compared with resist surface, the measured optical emission spectra will also shift to a higher intensity when resist is removed.

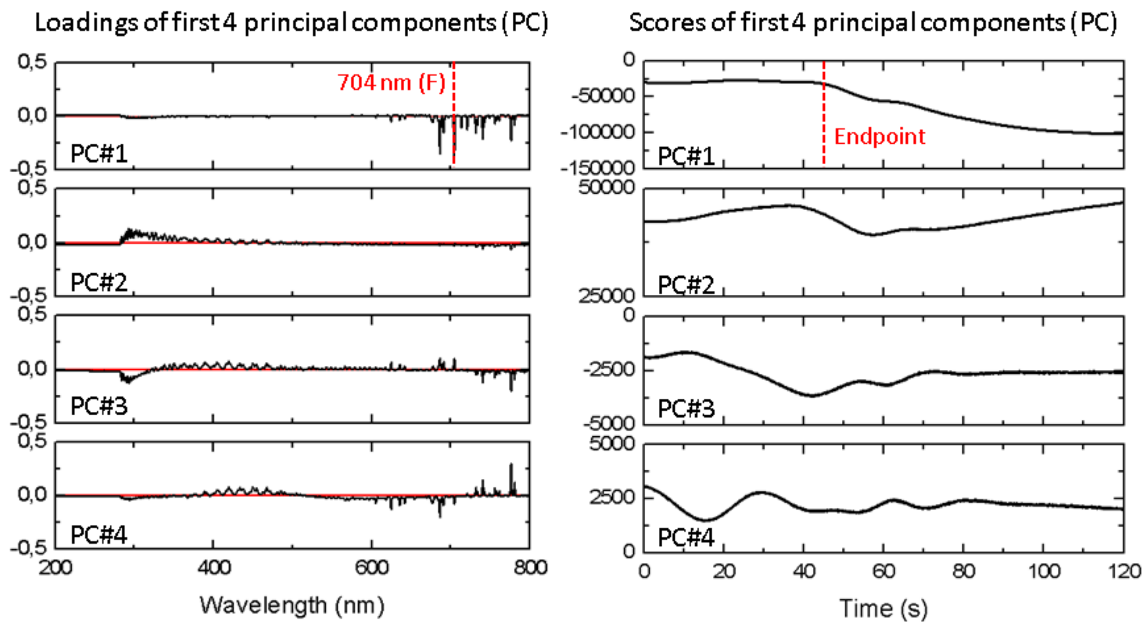


Figure 4.19. Loading and scores of first 4 principal components.

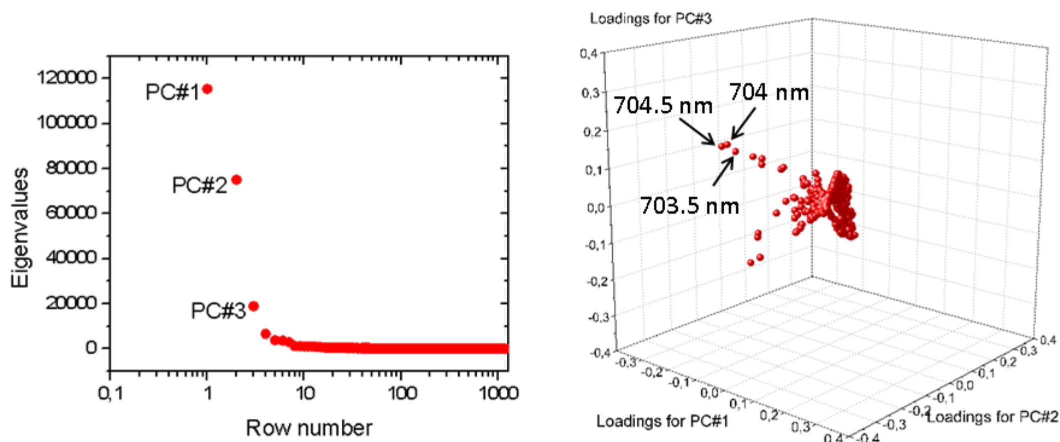


Figure 4.20. Eigenvalues of principal components, and loading plots for the first 3 principal components.

The eigenvalues of all principal components are shown in **figure 4.20**, from which we can see that the eigenvalues of the first three principle components add up to around 66% of the

sum of all eigenvalues. Thus to monitor the end point, we should only compare these three principle components, which have largest contributions to the evolution of total spectra. To find the wavelength, which has the most "distinctive" trend during the spectra evolution, the first three principal components are drawn in a single plot as shown in figure 4.20, and it suggests that the wavelengths of 704.0 nm, 704.5 nm and 703.5 nm is most far away from the center point, thus having the highest contrast before and after end point, and is suitable to monitor the end point, where silicon is overetched. Since the wavelength resolution on our OES system is 0.5 nm, in our study we will integrate the signals between 703 nm and 705 nm to have sufficient signals coming from silicon etching.

4.5.2 End point detection for BARC etch

Another case to study is the end point detection for BARC layer etch, which is more difficult compared with monitoring silicon etch because of a lower signal to noise ratio. After DUV stepper lithography, the BARC layer beneath resist layer needs to be removed before the silicon etch, a SEM image in **figure 4.21a** shows the cross section of 200 nm trench defined by DUV lithography. A standard method to remove BARC layer is to apply O_2 plasma with a DC bias, in our study, 200 sccm O_2 is applied, with 2000 W coil power and 200 W platen power. Since the BARC layer has a high crosslinking degree, it has a lower etch rate compared with positive tone DUV resist (as shown in figure 4.21b). This means that a over-sufficient BARC etch will reduce the thickness of DUV resist significantly, thus the maximum etch depth in silicon will be limited. To find the end point during the BARC layer etching process, we have monitored the whole OES spectrum evolution in 2 min, which is shown in figure 4.21c.

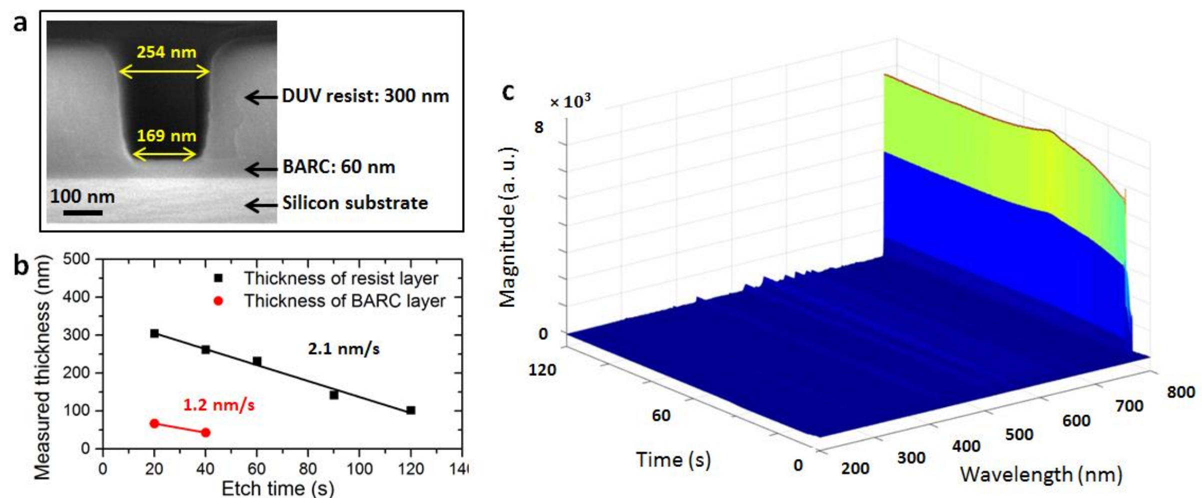


Figure 4.21. (a) SEM image of a 200 nm trench defined by DUV stepper lithography, showing the BARC layer and resist layer; (b) Remaining thickness of BARC and resist layer when O_2 plasma is applied; (c) Time evolution of the spectrum, when BARC layer and resist layer are etched by O_2 plasma.

By performing PCA, the loadings and scores of the first 4 principal components are shown in **figure 4.22**. We can see that the first principle component corresponds to an increase of oxygen signal at 777.2 nm, however, the end point is difficult to monitor in the scores diagram. While the second principle component has a clear trend for end point monitoring, it is difficult to identify a significant peak in the loading diagram. The third principal component also exhibits a clear end point, and two wavelengths are easy to be identified: OH signal from 308.9 nm and H signal from 656.0 nm. These two signals correspond to the removal of BARC layer, and thus are chosen as the wavelengths to monitor the end point.

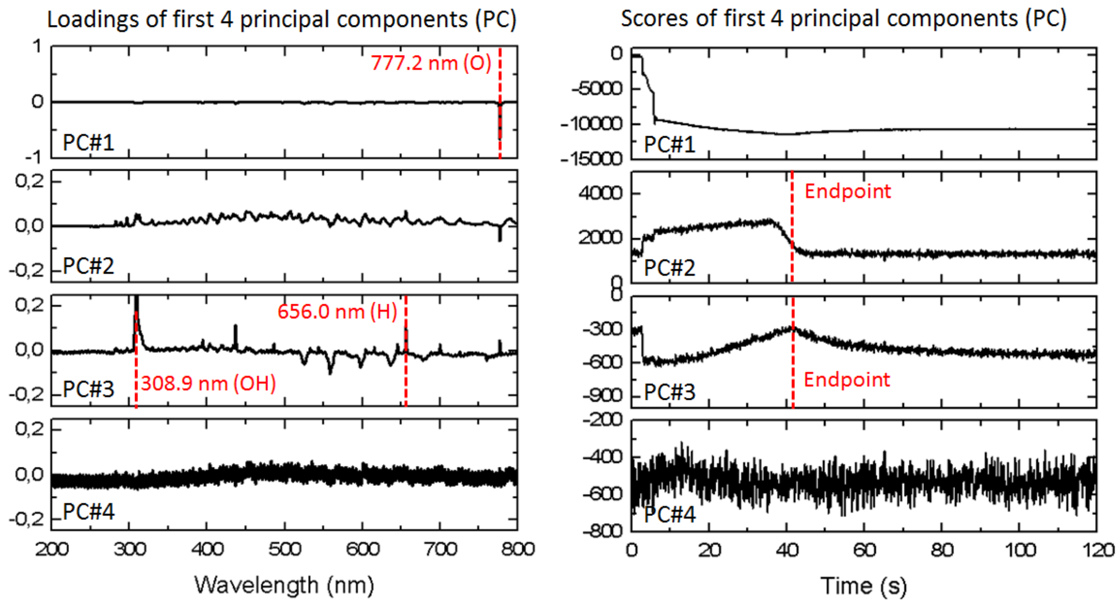


Figure 4.22. Loadings and scores for the first 4 principal components.

During the monitoring process, oxygen signals will be filtered away, even though it provides the highest eigenvalue among all principal components, as shown in **figure 4.23a**. By comparing the loadings of the second and the third principle components (as shown in figure 4.23b), we can see that OH signal at 308.9 nm can give the highest contrast, and thus is most favorable for end point detection.

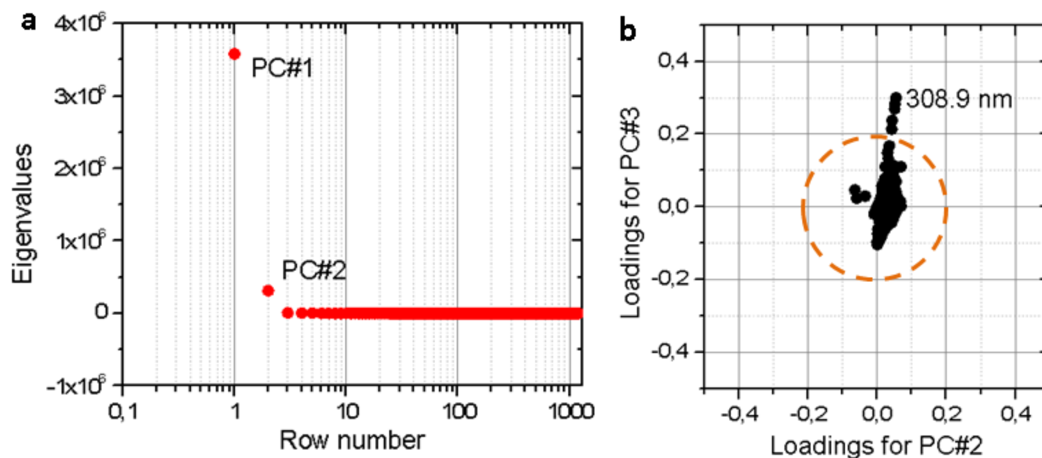


Figure 4.23. Eigenvalues of all principal components (a) and loading plot for second and third principal components.

In **figure 4.24a** we can see the time evolution of optical emission intensity from 4 different wavelengths, when the BARC layer is etched away by oxygen plasma. When the plasma is turned on at around 4 s, we can see intensity increase from OH (308.9 nm), H (656.0 nm), F (703.5 nm) and C (516.5 nm) signals, the signal intensities maintain above 100 for around 40 s, before the intensity drops again after the end point, where BARC layer is removed. A higher signal intensity and signal to noise ratio is observed for signal from OH, as shown in figure 4.24b. It should be noticed that, the signal intensity can be even lower for a small pattern loading area, thus the signal to noise ratio can be degraded and the end point

detection becomes difficult. For nanotrenches, a smaller etch rate of BARC layer can be expected, and a slight overetch is recommended to fully remove the BARC layer.

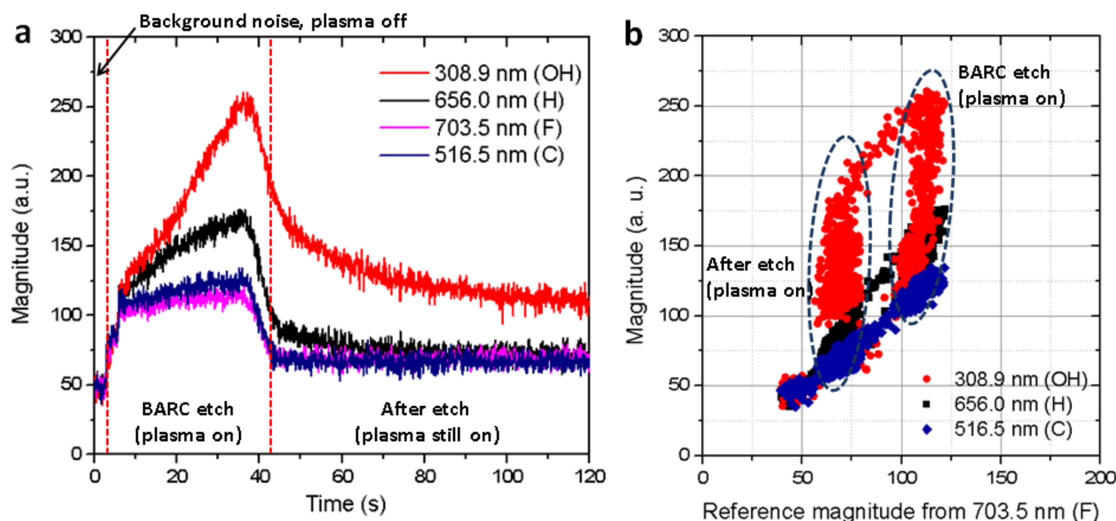


Figure 4.24. (a) Endpoint detection when BARC is totally etched; (b) Comparison of signals from different wavelengths, suggesting a higher signal-to-noise ratio for wavelength at 308.9 nm (OH).

For a continuous process with stable plasma conditions, the time evolution of optical emission intensity is a continuous process, thus the end point detection is relatively straightforward, while for Bosch process and DREM process, some signals will be switched on and off during the process when the gas species are varied, in this case, we should analyze the envelope function of the intensity evolutions, and the end point (e.g. when the silicon is overetched from photoresist during a DREM process) can still be monitored, this will be discussed in the following sections.

Apart from end point detection, which is the most widely used in real time monitoring in plasma etching processes, there is other valuable information that can be retracted from optical emission spectra. Here we will give two examples: firstly, the fluorine to carbon (F/C) ratio in a plasma process can be estimated by compare the relative intensities of F peak (at 703 nm) and C peak (at 516.5 nm). Since silicon is etched by fluorine radicals and passivated by carbon-based polymers, the F/C ratio can be used to characterize the relative influence of etching and passivation. [2, 150, 151] **Figure 4.25a** shows the F (703 nm)/C (516.5 nm) intensity ratio when SF_6 gas flow rate is increased from 0 to 55 sccm in a continuous mixed process, which has been introduced earlier in chapter 3. When the ratio is larger than 1.5, excessive fluorine radicals will overetch and create undercut in silicon structures; when the ratio is below 1, carbon contained inhibitors will dominate and passivate the structure, thus etching processes cannot proceed. Only when the ratio is in a certain range around 1.5, a straight etch profile can be achieved with a balance between etching and passivation. Thus by monitoring the optical emission spectra, a etch profile control can be performed for a continuous mixed etching process.

The outputs from oscilloscope and optical emission spectra can also be correlated and a more systematic study of the etching processes can be achieved. In figure 4.25b are the oscilloscope output of coil reflective power and evolution of optical emission intensities from three different wavelengths, when a continuous mixed process is performed. There are a few things we can notice: firstly, a large coil reflective power can be monitored and give “spikes” on the oscilloscope output, in the same time it can also cause “blinking” of

optical emission intensity (inside the blue square). This is understandable, since a poor power delivery to the plasma can reduce the ion density and thus less induced optical emission; Another thing we can notice is, it takes approximately 3 s for the plasma to be ignited and stabilized after the coil power is turned on (inside the red box). This time delay needs to be considered, especially for a short etch process.

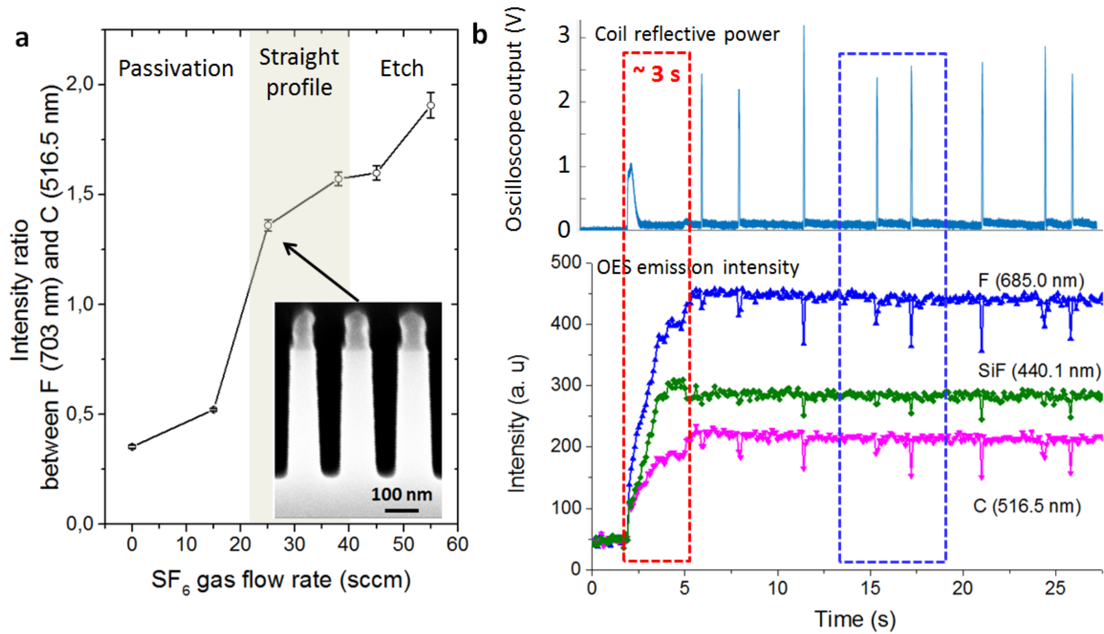


Figure 4.25. (a) Emission intensity ratio between F (703 nm) and C (516.5 nm) during a continuous mixed process for different SF6 gas flow rate; (b) Coil reflective power caused "blinking" of optical emission from plasma.

4.6 Real time monitoring with optical emission interferometry (OEI)

By applying the same system setup as OES, another type of in situ monitoring technique can be performed, which is termed as optical emission interferometry (OEI). Instead of monitoring the plasma chemistry directly from inside the chamber, OEI exploits the information of emission intensity variation from multiple wavelengths, which is caused by the interferometric phenomena from sample surfaces.

4.6.1 Basics of OEI

Just as laser interferometry, OEI is used to monitor the emission intensity change, which is caused by, e.g. interference from a thin film with a changing thickness during etching processes. However, compared with laser interferometry, OEI uses plasma glow as the light source, and interferometric information from a broader spectrum of wavelengths can be retrieved from a larger spot size on the sample surface. In the previous literature, OEI has been successfully applied to study etching processes of samples, which are coated with a uniform thin film, e.g. a dielectric thin film, [152] multiple layers of III-V materials, [153] a polysilicon layer, [154] etc. In this study, we will see that OEI can be used not only to study the etch process of a uniform thin film, but also surfaces with microstructures.

Firstly we will give a brief discussion about the physical basis of OEI, including how a stationary interference pattern can be generated and how it can be used to analyze the thickness change of a thin film, or the etch depth of silicon microstructures.

The plasma glow can be considered as spatially isotropic inside the chamber, and the part which can be detected by the detector is composed of two components: the first is the light that travels directly from plasma glow towards the detector, which can be considered as constant for a stable plasma condition; the second is the light that is reflected from the wafer surface, since the reflection and absorption of the surface change continuously during a plasma process, this part is thus variant in time, and the total time-average intensity can be written as below:

$$I(t) = \alpha \langle |\vec{E_1}(t)|^2 \rangle + (1-\alpha) \langle |\vec{E_2}(t)|^2 \rangle + \sqrt{\alpha(1-\alpha)} \left(\langle \vec{E_1}(t) \cdot \vec{E}_2^*(t) \rangle + c.c. \right) \quad (4.1)$$

In which α represents the loading percent of the sample surface. $\vec{E_1}(t)$ and $\vec{E_2}(t)$ are the electric field of the reflected light from silicon and mask surface as shown in **figure 4.26a**. The first two terms in equation (4.1) correspond to the intensity of reflected light from silicon and mask, while the interference between the two is represented in the third term, here we omit the interference from silicon gratings themselves, since we assume the light collected from the surface is in a small region, and the detector is on top of structures, thus no significant optical path difference can be generated.

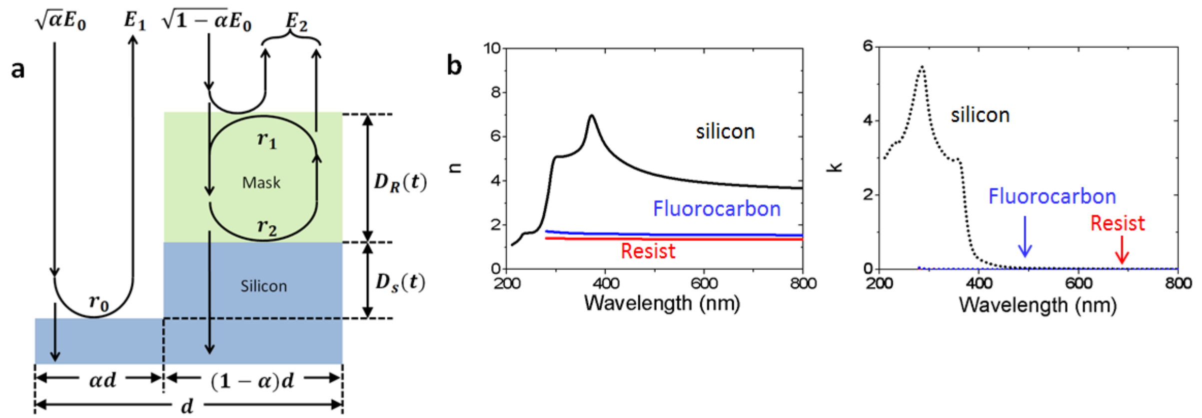


Figure 4.26. (a) An illustration of light paths on the sample surface with both silicon and mask; (b) Refractive indexes of silicon, fluorocarbon layer and photoresist measured by ellispsometry.

The reflectance from silicon surface is $I_1(t) = \alpha r_0^2 \langle |\vec{E_0}(t)|^2 \rangle$, which can be considered as time independent (in real situations the increasing surface roughness caused by etch processes can actually increase the scattered light collected by the detector, and a higher optical emission intensity can be measured). Because of the high absorption of silicon surface in the UV wavelengths, the magnitude of this term decreases for wavelength typically below 500nm. (The refractive indexes of silicon, resist and fluorocarbon layer are measured by ellipsometer and shown in figure 4.26b). Since the silicon-resist interface and resist-air interface are not perfect reflective surfaces, here we treat the resist layer as an etalon based on the classic Fabry-Perot interferometry theory, then the time average intensity from resist can be written as

$$I_2(t) = R_{etalon}(t) \langle |\vec{E_0}(t)|^2 \rangle = \frac{4(1-\alpha) r_1^2 \sin^2(\frac{2\pi n_1 D_R(t)}{\lambda})}{(1-r_1^2) + 4 r_1^2 \sin^2(\frac{2\pi n_1 D_R(t)}{\lambda})} e^{-\frac{8\pi k_1}{\lambda} D_R(t)} \langle |\vec{E_0}(t)|^2 \rangle \quad (4.2)$$

Here $R_{etalon}(t)$ is the time dependent reflectivity from resist film, n_1 and k_1 are the refractive index and extinction coefficient of resist films, and $D_R(t)$ is the thickness of the

resist which is slowly reducing in time. We consider the incident angle of incoming light as 90 degrees, thus $\vec{k} \cdot \overrightarrow{D_R}(t) = 2\pi n_1 D_R(t)/\lambda$. This suggests a condition for constructive interference when $D_R(t) = \lambda N/2n_1$, in which N is the order of interference. Notice that the absorption from resist is almost 0 because of the low extinction coefficient as measured in figure 4.26b, thus when the resist is being consumed during a plasma etch process, a periodic pattern caused by interference can be observed.

For materials with large extinction coefficient (e.g. silicon in UV range), the interference will become stronger when the high absorption layer become thinner, which can be observed typically for a SOI sample. To illustrate this, the interference from films with two different extinction coefficient are calculated and compared, with the original film thickness set as 1 µm and an etch rate of 100 nm/min. We can notice the increasing intensity when the film thickness is reduced for the light absorbing film (**figure 3.27a**), while for a film with no absorption, a stable interference pattern can be observed (figure 3.27b).

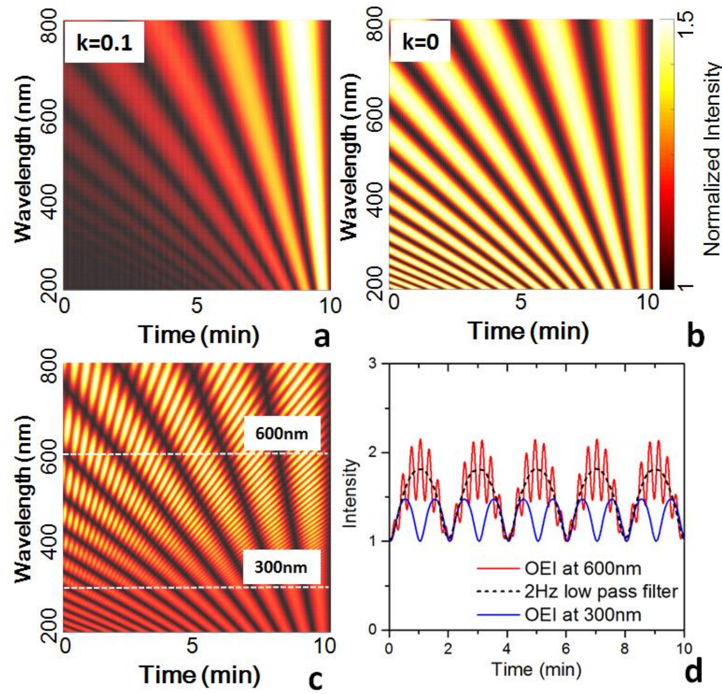


Figure 4.27. (a) Interference patterns of the whole spectra when etching an absorbing film; (b) Interference patterns of the whole spectra when etching a film with no absorption;

The interference between fields $\overrightarrow{E_1}(t)$ and $\overrightarrow{E_2}(t)$ is caused by optical path difference combined by silicon etch depth $D_S(t)$ and the remaining resist thickness $D_R(t)$. Here we assume that the etch rate of silicon is much larger than etch rate of the resist $\left|\frac{dD_S(t)}{dt}\right| \gg \left|\frac{dD_R(t)}{dt}\right|$, thus the reflection from the thin film is constant in time $R_{etalon}(t) = R_{etalon}$ (this is a reasonable assumption, since the resist we used has an etch selectivity of around 200 to 300). And the interference terms in equation (4.1) is caused mainly by the increasing etch depth of silicon.

$$I_3(t) = 4\sqrt{\alpha(1-\alpha)}|r_0|^2 R_{etalon}\left|\overrightarrow{E_0}(t)\right|^2 \left(\sin^2\left(\frac{2\pi(D_R(t)+D_S(t))}{\lambda}\right) + constant\right) \quad (4.3)$$

This term is varying faster in time compared with $I_2(t)$, with the condition for constructive interference as $D_S(t) + D_R(t) = \lambda N/2$. The total intensity $I(t)$ will thus be a combination of two interferometric periods, and by identifying the periods, we can retract information for $\left|\frac{dD_S(t)}{dt}\right|$ and $\left|\frac{dD_R(t)}{dt}\right|$, and thus the silicon etch rate and resist consumption rate, which are given by $|\partial_t D_R(t)|$ and $|\partial_t D_S(t)|$ correspondingly. Assuming the silicon etch rate is 1 $\mu m/min$, then the evolution of optical emission intensity in the whole spectrum is shown in figure 4.27c, from which we can clearly see, that on top of the interference caused by changing thickness of resist film (as shown in figure 4.27b), the etched silicon structures are also generating interferometric signals, but mainly at large wavelength because of the high absorption at UV range. We can also notice that for different wavelengths, the fast varying signal start from the same phase at t = 0 min because of zero etch depth in silicon; while the slowly varying signals all end at the same phase at t = 10min. Signal from wavelength of 300 nm and 600 nm are shown in figure 4.27d, this kind of combined interferometric effects is easily observe on 600nm, while on 300nm, a small value of $|r_0|^2$ gives a low intensity from $I_3(t)$, thus only the changing thickness of resist can be monitored.

Unlike laser interferometry which has a coherent light source, the light generated by plasma glow in OEI is fluctuating and random in phase both spatially and temporally, but still a stationary interference pattern could be generated. This can be explained following the van Cittert-Zernike theorem, which states that for large distance between observer's plane and light sources, two incoherent ordinary light sources act like coherent. And such relation should be satisfied $\lambda > \rho d/R$, in which ρ is the critical dimension of the structures which create a light path difference, d is the size of the detector, and R is the distance between structures and the detector, in our set up, d is estimated to be 2 cm, and R is around 26 cm, this sets a size limit of around 10 µm for structures, upon which a stationary interference cannot be observed.

To consider about the temporal coherence, the light generated by plasma glow from certain species can be thought of as quasi-monochromatic, e.g. Ar plasma can generate light at 703 nm with linewidth of around 3 nm, which corresponds to a bandwidth of around 467 kHz. This translates into a coherence time of 340 ns and a coherence length of around 2.3 mm, which is way larger than the critical dimension of the structures. Of course both spatial and temporal coherence of OEI are not comparable with laser interferometry, and for some species as C (which gives a broad emission peak), the temporal coherence will be even worse, and an accurate monitoring will be limited for a longer process time.

4.6.2 Studying C_4F_8 passivation process with OEI

To demonstrate how OEI works, we will start with a simple case and study how OEI can be used to study the C_4F_8 deposition mechanism under different conditions, where coil power, platen power, temperature, pressure are varied. We will see how the thickness of deposited fluorocarbon layers on silicon can be directly measured with OEI, and the measurement results agree nicely with ex-situ measurements by ellipsometry.

Firstly, fluorocarbon film is deposited by 400 sccm feed gas of C_4F_8 with coil power of 3000 W, platen power of 25 W, platen chiller temperature of 20 ˚C and valve position at 100% (which corresponds to a processing pressure of around 20 mTorr). The optical emission spectrum is shown in **figure 4.28a**, and the growth process of the fluorocarbon film during 200 s was monitored and recorded by OEI. To compare the thickness measured by OEI with ellipsometer, 5 different durations of deposition were performed from 41 s to 180 s, and the thickness was calculated using 3 different wavelengths of 440.1 nm, 516.5 nm and 696.5 nm.

The evolution of signal intensity at 440.1nm is shown in figure 4.28b. Since deposition process all started on a clean wafer surface, the waveforms have the same initial phase and overlap with each other, in the same time, because of the absorption of fluorocarbon layer at 440.1 nm, the intensity and amplitude of the sinusoidal waves decreases when the C_4F_8 deposition process continues. The measurements from OEI and ellipsometer agree nicely as shown in figure 4.28c, which gives a deposition rate of around 5.4 nm/s. Unlike laser interferometry, OEI can provide information from a whole spectrum of wavelengths. Here the signal from 440.1 nm shows the least variation (< 5%) from ellipsometry measurement (figure 4.28d), which is understandable, since the signals from smaller wavelengths have smaller peak to peak distances, corresponding to a smaller thickness change and thus a higher measuring accuracy. [155]

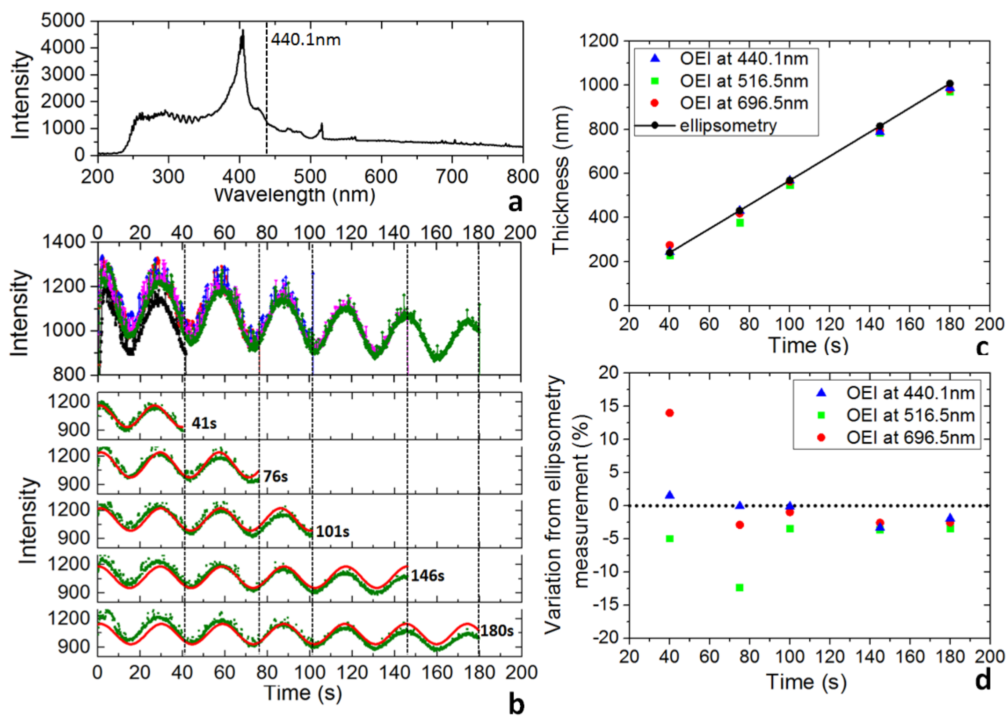


Figure 4.28. (a) Optical emission spectrum during a fluorocarbon film deposition using C_4F_8; (b) Evolution of optical emission intensity at 440.1 nm for different process times; (c) Comparison of ellipsometry with OEI measurements of fluorocarbon film thickness; (d) Measurement variation between OEI and ellipsometry.

To study the passivation mechanism of fluorocarbon layer, different parameters were chosen and the deposition rates are then compared. By setting platen chiller temperature at -19 ˚C and 20 ˚C, a significant difference in deposition rates can be observed from the interference patterns by OEI, which is shown in figure **4.29a-b**. Here we will choose 440.1 nm to calculate the fluorocarbon layer thickness. Firstly, a higher coil power gives a higher deposition rate (as shown in figure 4.29c), which can be explained by a higher dissociation level of deposition species, thus passivation layer can be grown at a faster speed. In the same time, a lower temperature at -19 ˚C can give a deposition rate which is 3-5 times faster than the deposition rate at 20 ˚C, this is due to a higher sticking coefficient of ion enhanced inhibitors on the cold sample surface, which will also slow down the desorption rate and increase the deposition rate. This coil power and temperature dependency of deposition rate confirms the previous studies. [156, 157] When increasing the platen power as shown in figure 4.29d, the deposition rate will increase, but achieves a maximum at around 50 W, this

is possibly due to more ion bombardment at a higher platen power, which will instead sputter away the passivation layer and reduce the deposition rate. The deposition rate is also highly dependent on the processing pressure. In the experiment, pressure is controlled by manually tuning the valve position, and the deposition rate decreases for a lower pressure (figure 4.29e), possibly due to a lower density of available deposition species.

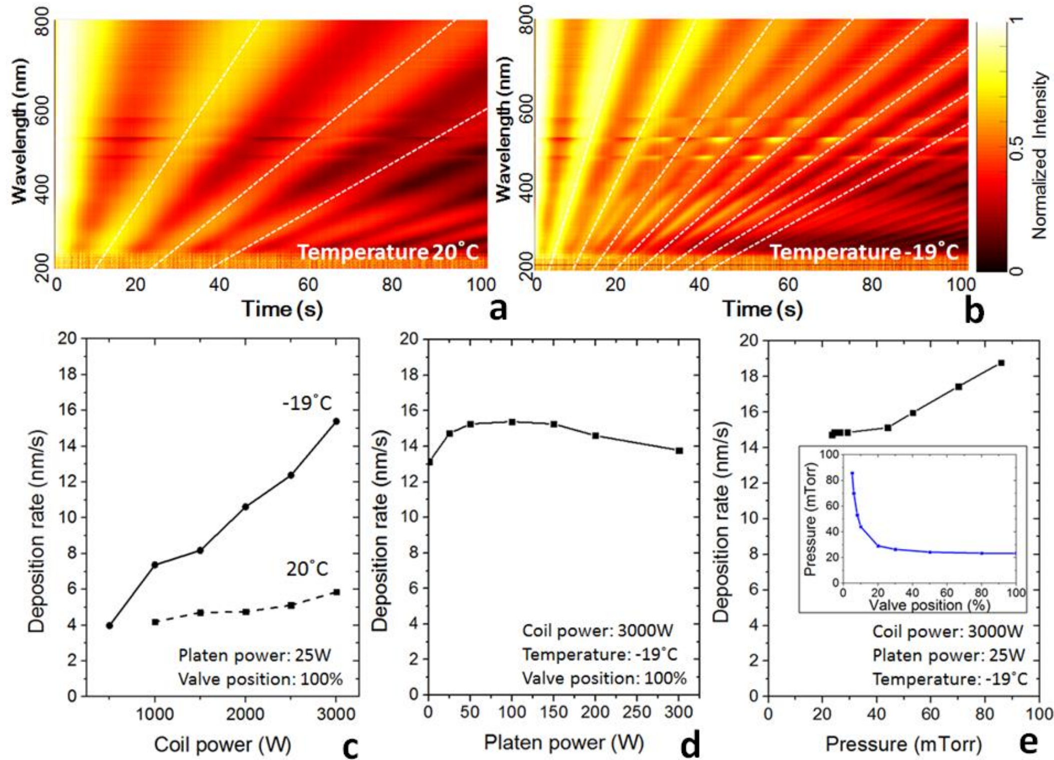


Figure 4.29. Using OEI to study fluorocarbon film deposition: (a-b) The evolution of whole spectrum during a deposition process with different platen chiller temperatures at 20 ˚C and -19 ˚C; (c) Deposition rate measured for different coil powers and platen chiller temperatures; (d) Deposition rate measured for different platen power; (e) Desposition rate when pressure is varied.

From the results above, OEI measurement has been calibrated with ellipsometry measurements for fluorocarbon film deposition, the thickness measured with two methods agree nicely with each other, verifying the efficiency of OEI method to study C_4F_8 passivation process, which can give us an idea about the passivation mechanism and also directions for process optimizations.

4.6.3 Studying continuous mixed process with OEI

In this part, we will see how OEI can be used to monitor the silicon etch process with a continuous mixed process, which has been discussed earlier in section 3.2. We will show how to monitor the resist etch and silicon etch in the same time by OEI technique.

During the process, 50 sccm SF_6 and 50 sccm C_4F_8 were applied simultaneously with coil power of 800 W and platen power of 80 W, temperature was set to be -19 ˚C to increase the coating efficiency of fluorocarbon layer, which was also discussed and studied with OEI in the last part, therefor less amount of C_4F_8 is necessary to achieve the same sidewall passivation effect, and a lower processing pressure of 8 mTorr can be then reached, which is favorable for an anisotropic etch profile.

The optical emission spectrum is shown in **figure 4.30a**, and the evolution of optical emission intensities from 3 different wavelengths (703.0 nm, 440.1 nm and 369.0 nm) were studied during a total process time of 145 s, which is shown in figure 4.30b. Unlike signals from 440.1 nm and 369.0 nm, the signal from 703.0 nm shows a coexistence of two periodicities, including one slowly varying term which implies the changing thickness of photoresist layer, and one fast varying term which corresponds to the interference from etched silicon structures. The fast varying term is only pronounced on longer wavelengths. As discussed earlier, silicon surface gives strong light absorption in the UV range, thus only the interference from resist films can be observed at 440.1 nm and 369.0 nm, while the signal from 703.0 nm can give interference information for both resist etch and silicon etch. SEM images of etched profiles of a 5 μm trench are shown in figure 4.30c, with different process time of 50 s, 100 s and 120 s. The trench openings can be seen to be widened due to lateral etch and recession of photoresist. The etch depths in silicon were estimated with the OEI signal from 703.0 nm, and the remaining thickness of photoresist was estimated with the OEI signal from 369.0 nm. Calculated results from OEI were then compared with direct SEM measurements, showing a good agreement with each other (figure 4.30d). In order to verify the signal from 703.0 nm is a combined interference effect from both photoresist film and etched silicon gratings, a low pass filter was applied to eliminate the high frequency noises, and a FFT was performed as shown in figure 4.30e-f, which suggest two periodicities at frequencies of 0.042 Hz and 0.014 Hz, corresponding to the silicon etch rate of 14.7 nm/s and resist etch rate of 1.7 nm/s, this agrees with the measured etch rates of silicon (15.3 nm/s) and photoresist (1.5 nm/s).

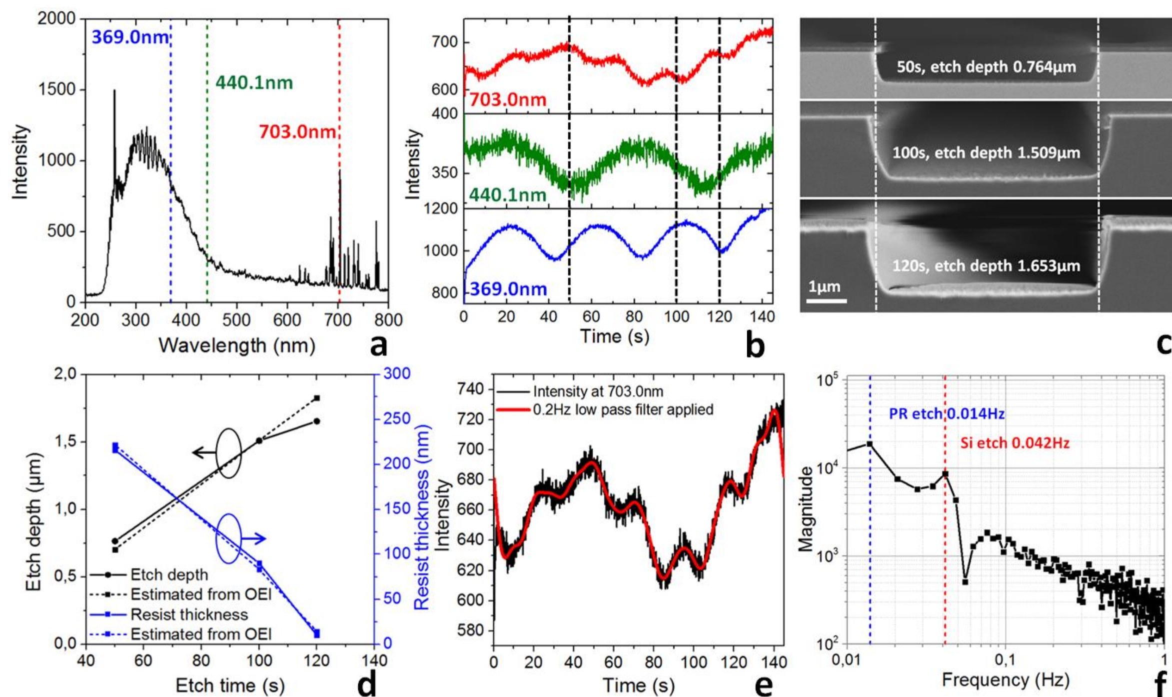


Figure 4.30. Using OEI to study a continuous mixed process for etching silicon microstructures: (a) The optical emission spectrum during process; (b) Evolution of optical emission intensity at three different wavelengths; (c) SEM images of etched silicon microtrench with different process time; (d) Etch rate of silicon and resist calculated with OEI, compared to SEM measurements; (e,f) Processed signals from 703.0 nm, showing both silicon etch and resist etch.

Owing to the large spot size in an OEI setup, more surface information can be retracted in the same time. Therefore both silicon etch and resist etch can be monitored simultaneously

during a continuous mixed etching process, this is an advantage which laser interferometry cannot provide.

4.6.4 Studying DREM process with OEI

As a main topic of the thesis, DREM process has been introduced and discussed in the last chapter, here we will show how OEI can be used to monitor DREM processes, during which plasma condition is switched constantly, generating unstable signals of optical emission intensities, but still we can manage to monitor the resist etch rate, and in the same time have a rough estimation of the silicon etch rate.

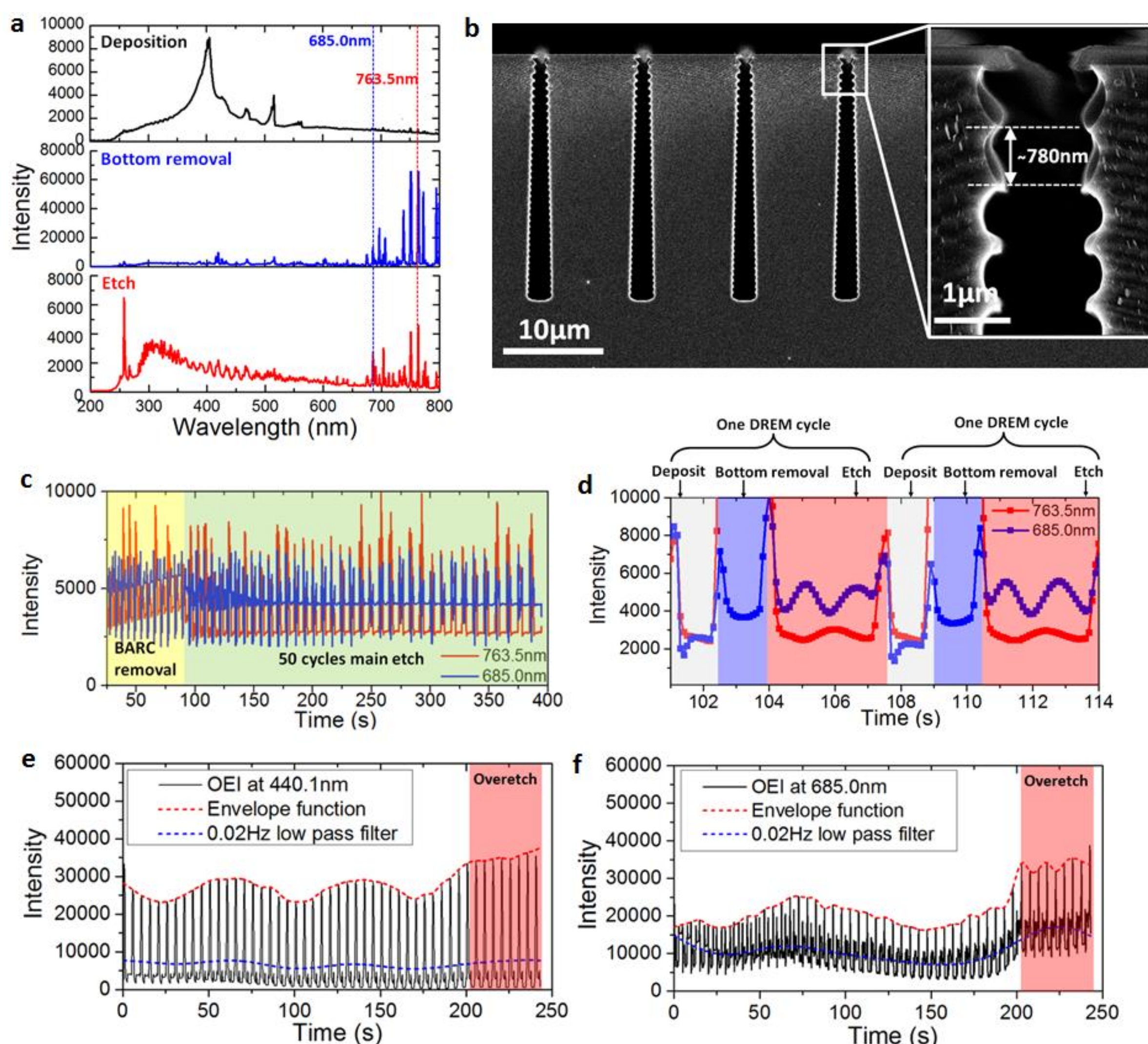


Figure 4.31. Using OEI to study a DREM process: (a) Optical emission spectra for deposition, removal and etch steps during a DREM cycles; (b) SEM images of etched silicon trench by 50 cycles of DREM process; (c) Evolution of optical emission intensities from two wavelengths during the whole DREM process; (d) OEI signals showing silicon etch during a single DREM cycles; (e) OEI signals at wavelength of 440.1 nm showing overetch; (f) OEI signals at wavelength of 685.0 nm showing overetch.

The patterns we used were trenches with 1μm linewidth defined by DUV stepper lithography. The parameter settings for DREM process is briefly introduced as below: deposition time is 1.5 s with 300 sccm C_4F_8, afterwards 200 sccm Ar was applied with 140 W platen power for 1.0 s to clean the passivation layer in the bottom of the trench, finally 600 sccm SF_6 was added to etch into silicon, and the etch time was ramped up linearly from 3.5

s to 8.5 s during 50 cycles, thus etching nonuniformity caused by ARDE is compensated. The coil power was set at 3000 W and platen chiller temperature was -19 ˚C.

The optical emission spectra during deposition, bottom removal and etch phases are shown in **figure 4.31a**, and two wavelengths at 685.0 nm and 763.5 nm were studied. The SEM images of etched profiles are shown in figure 4.31b, in which the scallops can be seen with a size of around 780 nm, the etch depth is around 24 μm with a negatively tapered profile. The evolution of optical emission intensities from 763.0 nm and 685.0 nm shows two stages of etch process: first step of BARC removal and then main etch into silicon structures (figure 4.31c). It should be noticed that in the first few cycles, there is strong interference signals during the etch step, which is zoomed in and shown in figure 4.31d, this feature is again the outcome of interference from silicon microstructures, suggesting an etch depth of around 760 nm during each DREM cycle, which fits nicely with the direct measurement from SEM images. However, the interference signals from silicon microgratings will slowly fade away when the etch depth is beyond 10 μm, this sets a technical limit to the OEI monitoring of etching deep structures.

While the OEI signals from a single DREM cycle can give us information regarding scallop sizes, when looking at the whole trend of a DREM process, other valuable information could be retracted. For example, by observing the envelope function of OEI signals from the whole DREM process, or by applying a low pass filter, the etch rate of resist can be estimated. In figure 4.31e and figure 4.31f, the slowly decreasing thickness of resist layer generates an interference pattern which is resembled in both envelope function and the low pass filtered signals. Thus the end point becomes easy to be monitored when the interference pattern ends, suggesting the silicon is overetched.

5 Plasma etching for silicon micro- and nanostructures

In chapter 3 we have discussed basics of plasma etching processes, importantly, we introduced DREM process. Afterwards, we have shown how real time monitoring is performed on our etching apparatus in chapter 4. In this chapter, we will discuss how the process optimization is performed for a DREM etch process, some etched structures will be demonstrated, including: high aspect ratio microstructures, black silicon, nanostructures with minimized sidewall roughness. In the end of the chapter, we will show how a modified DREM process can be used to fabricate 3D micro- and nanostructures.

5.1 GENERAL STRATEGY FOR DREM PROCESS OPTIMIZATION

Due to the large parameter space of plasma etching processes and the complexity of etching apparatus, a standard procedure should be established for recipe development and parameter optimization, thus a higher efficiency can be achieved and the fabrication costs can be reduced. **Figure 5.1** shows a general strategy for process development and parameter optimization, before devices are finally manufactured. The whole process includes three modules, which are discussed in details as below:

- *Preliminary parameter test*: In this step, some basic parameters will first be settled according to specific requirements for etch performances. For example, in order to etch deep microstructures, a high coil power of 3000 W and high gas flow rates of over 200 sccm can be chosen; while for shallow etch of nanostructures, coil power should normally be less than 1000 W and small gas flow rates of less than 200 sccm could be a better starting point. Once the parameters are settled, an acceptance test of recipe has to be performed on the etching machine. Especially, high reflective powers from coil and platen generators should be avoided in order to reduce the risk of damage to etching apparatus, and in the same time a good repeatability can be achieved. Parameters need to be adapted if the recipe can cause large reflective powers that are over tolerance levels;

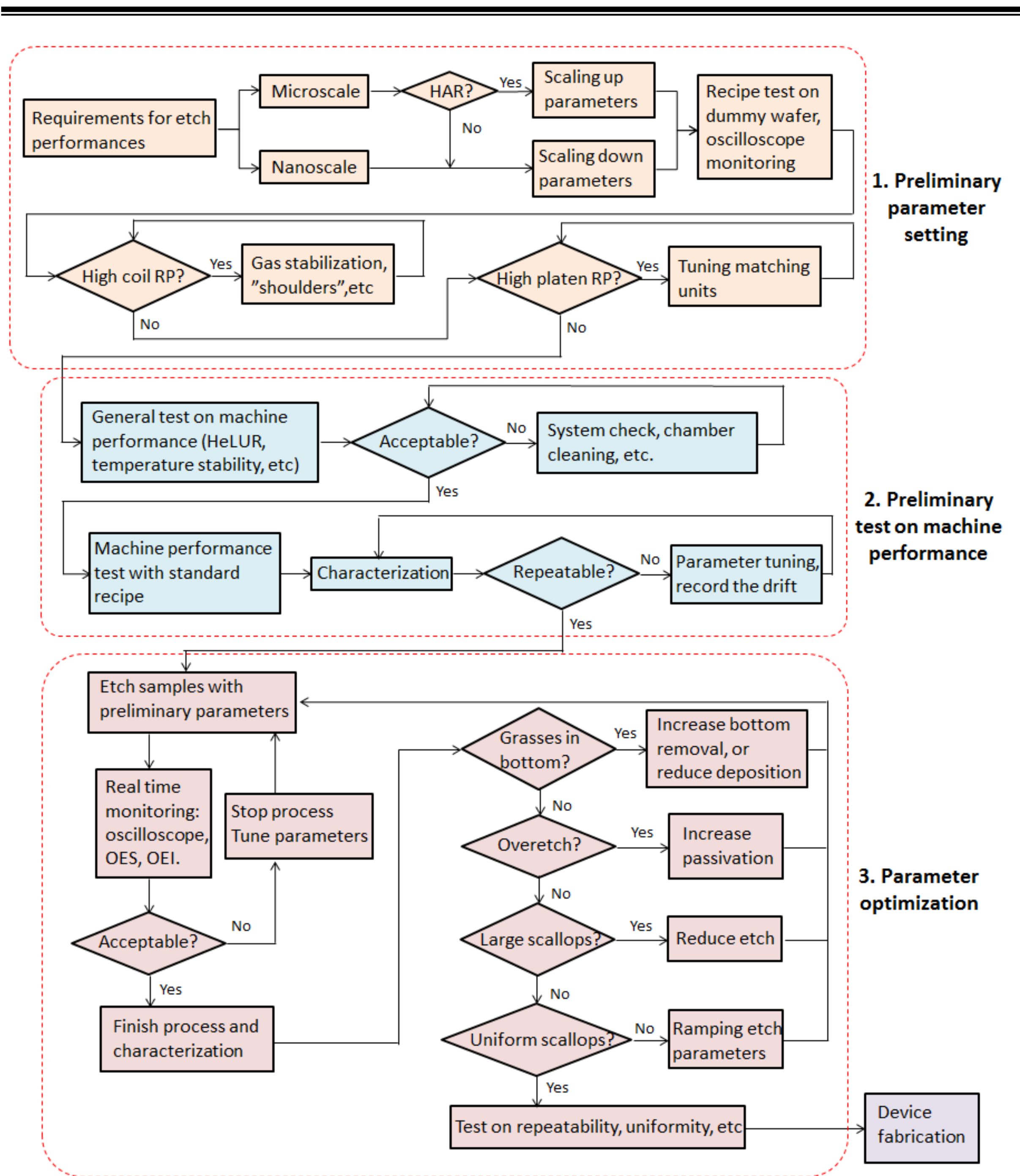


Figure 5.1. A general procedure to optimize DREM processes.

- *Preliminary test on machine performance*: Because of the complexity of etching apparatus and a multi-user environment, the status of the machine can be drifted even during a single day, leading to a bad repeatability of etching results. For example, if the previous user had a sample that left some large particles on the chuck, then the electrostatic gripping force on the wafer will be reduced, and a high helium leakup rate (HeLUR) will limit the cooling efficiency, and the samples might be overetched or even drifted away inside the chamber. To ensure that the machine performance is within in an acceptable fluctuation range, a preliminary test on the machine status is always performed in our study. Firstly, some general parameters will be monitored with a dummy wafer, e.g. helium leakup rate, temperatures on the chamber and the coil

generator, etc. Secondly, a standard recipe will be applied to etch a standard sample (e.g. trench arrays with 1 µm linewidth), and the etch results will be compared with previous results to make sure that the machine status is stable and can be trusted for further processing. This step is crucial, since the following optimization process has to be based on a stable machine status;

- *Parameter optimization of a DREM process*: In this module, samples will be etched using recipes developed from last step. Since etch processes are well-defined by the 3-step DREM process, parameter optimizations can be performed in a relatively easy procedure. Firstly, the samples will be etched and the processes are monitored in-situ, etched samples will then be characterized by optical microscope or SEM. Secondly, parameters in bottom removal step (e.g. platen power) and deposition step (e.g. C_4F_8 gas flow) will be tuned for a straight structure profile without either overdeposition (which can cause a positively tapered profile or even grasses in the bottom) or overetching (which can cause a negatively tapered profile or undercut). When a straight profile is achieved, the scallop size will be tuned by modifying parameters in the etch step, e.g. SF_6 gas flow or duration of etch step. To achieve a good size uniformity of scallops, data ramping will be performed, e.g. by increasing the duration of etch step slowly along with the etching process. When the structure profiles satisfy the requirements for device fabrication, the repeatability and uniformity will be tested, before the recipe is finally used for device manufacturing.

This procedure has served as a standard strategy for process optimization in thesis, and etched structures will be shown in the following sessions. It should be noticed that although the strategy can be generally applied for other etching tools, which are capable to perform DREM processes, the parameter setting are dedicated for the DRIE Pegasus system.

5.2 ETCHING HIGH ASPECT RATIO SILICON MICROSTRUCTURES

To demonstrate how an etching process can be developed following the procedure as introduced in the last session, we will first give an example, in which HAR silicon microtrenches are fabricated, the linewidth of patterns is 1 µm and period is 10 µm. The starting recipe is in **table 5.1** as below

		3-steps DREM cycle		
		Deposit FC	Remove bottom FC	Etch silicon
Duration (s)		1.5	1.9	1.6
Gas flow (sccm)	C_4F_8	200	5	5
	SF_6	15	15	600
	Ar	200	250	250
Generators (W)	13.56 MHz coil generator	3000	3000	3000
	13.56 MHz platen electrode	1	50 (for 1 s)	1

Table 5.1. The initial recipe for etching HAR silicon microtrench structures.

The etched profile has a positively tapered sidewall as shown in **figure 5.2a**, suggesting there might be overdesposition during the deposition step, thus the bottom will close and

etching cannot go deeper for HAR structures. Based on the procedure introduced in section 5.1, following parameter optimization steps have been performed:

- (a → b): In order to achieve a straight profile, platen power was increased from 50 W to 75 W. The etched profile has a etch depth of 34.23 μm, with a broadened bottom width of 1.89 μm, sidewall corrosion can be observed (figure 5.2b);
- (b → c): To reduce the sidewall corrosion and linewidth broadening, the C_4F_8 gas flow rate is increased from 200 sccm to 300 sccm. A straight profile is achieved without sidewall corrosion, the etch depth of 26.55 μm with large scallop size of ~ 550 nm (figure 5.2c);
- (c → d): To reduce the scallop sizes, the duration of etch step is reduced from 1.6 s to 0.6 s. The etched profile shows much smaller sidewall roughness and less bowing effect; the etch depth is 18.60 μm and scallop size is ~300 nm (figure 5.2d);
- (d → e): For a higher aspect ratio, total number of DREM cycles is increased from 50 to 100, with etch duration ramping up from 0.6 s to 6.0 s. The etched profile is still straight with an etch depth of 36.43 μm (AR ~ 33) (figure 5.2d) ;
- (e → f): To further increase AR, the number of DREM cycles is increased to 150, and etch duration ramping up from 0.6 s to 9.3 s. An etch depth of 57.74 μm can be achieved, corresponding to AR ~ 50. Minor sidewall corrosion can be seen in the middle part of sidewalls (figure 5.2e)

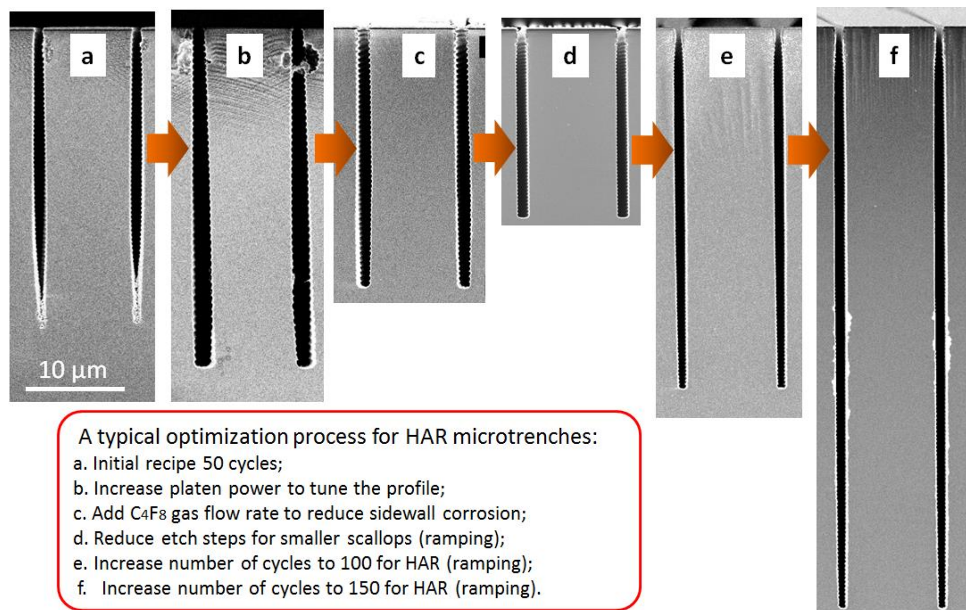


Figure 5.2. The optimization process to achieve HAR trench structures (with linewidth of 1 μm and etch depth of 57 μm).

From the procedure above we can see how DREM process can be programmed in an easy and logic way, this is due to minimized coordinative effect between different parameters, when three separate steps are clearly defined in a DREM process.

By modifying the etch recipes in a similar procedure, we can also achieve silicon micropillar structures with diameter of 1 μm and HAR ~ 50. Compared with trench structures, incoming ions in pillar structures suffers less from image force, [158] thus a larger ion current can reach the bottom and etch rate is observed to be larger compared with trench structures. The etched pillar structures are shown in **figure 5.3**. The etch depth is around 45.76 μm with

a good size uniformity from top to bottom (as shown in figure 5.3b and figure 5.3c), the pillar diameters are 0.980 µm and 1.048 µm, and scallop sizes of 223 nm ad 286 nm on top and bottom of the pillars correspondingly. It should be mentioned that, due to the high aspect ratio, fabricated micropillar arrays are susceptible to capillary force, which can cause structure collapse and cluster formation, [159 - 161] as shown in figure 5.3d.

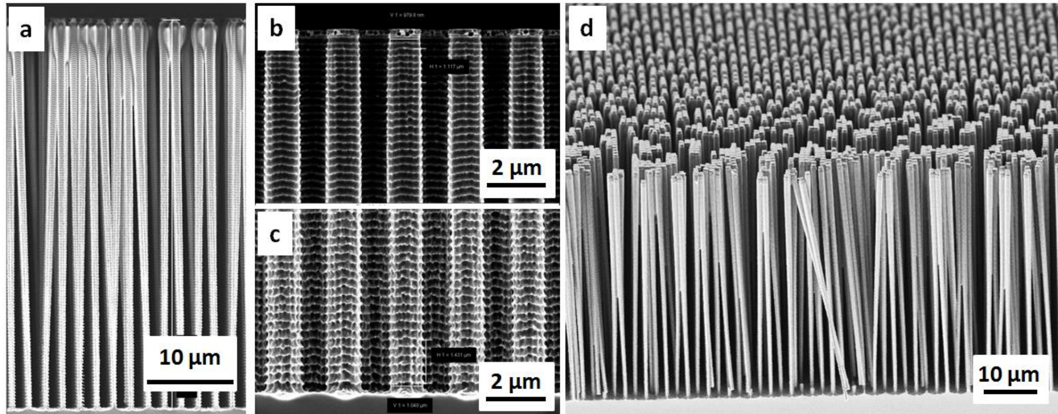


Figure 5.3. SEM images of silicon micropillar arrays: (a) Cross section view; (b) Top of the pillars; (c) Bottom of the pillars; (d) Tilled view of pillar arrays.

Because of the efficient bottom removal for pillar structures, the duration of deposition should be increased to have a straight profile without structure collapse. In order to achieve an even larger AR, a 20 nm-thick alumina ALD deposited layer is used as a hard mask. The etch results are shown in **figure 5.4a**, the etch depth is measured to be 51.83 µm with minor clustering of micropillars. Due to the long etch process, fluorocarbon protection layer on top of the pillars starts to be eroded away, and a strong undercut can be seen (figure 5.4b), which give suspended alumina mask structures (figure 5.4c). It was suggested in previous literature [162] that when mask and substrate only have a point contact due to strong undercut, the mask will be flipped due to electrostatic force, however, this is difficult to be identified in this experiment.

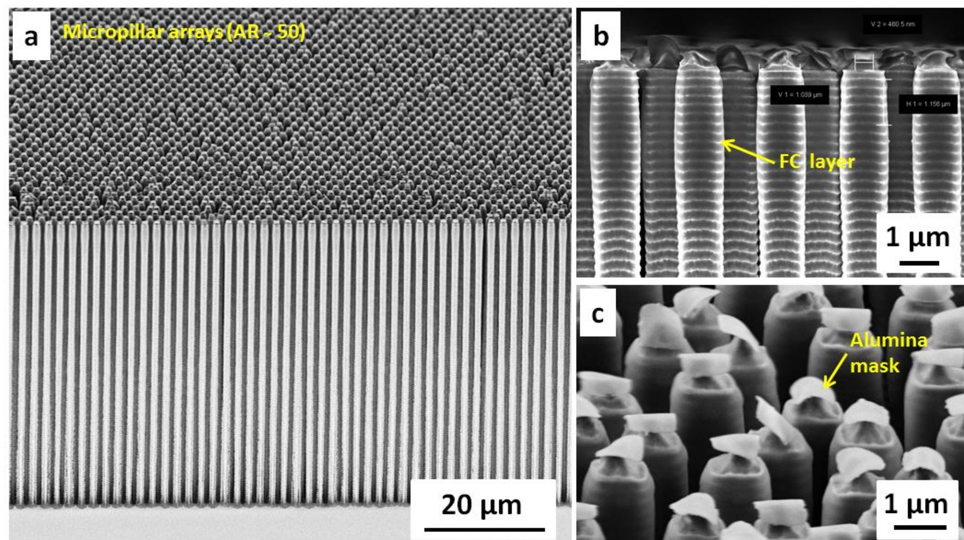


Figure 5.4. SEM images of silicon HAR micropillar arrays: (a) Tilted view of pillar arrays; (b) Top of pillars; (c) Zoom in on the alumina hard masks, showing a strong undercut.

It should be noticed that when introducing an isotropic etch step after a numbers of DREM cycles, the silicon micropillars can be sculptured into a 3D profile, which is shown in **figure 5.5**. We can see that periodic structures are defined by a thinner "neck" created by an isotropic etch, while the straight parts are still etched by DREM cycles. A good shape geometry and uniformity can be seen in figure 5.5a, where the pillars have 6, 7 and 8 repeating periods, and the total number of repeated periods can be up to 10 times without structure collapsing as shown in figure 5.5c. This is the base of the 3D silicon engineering, which will be discussed in details later in the chapter.

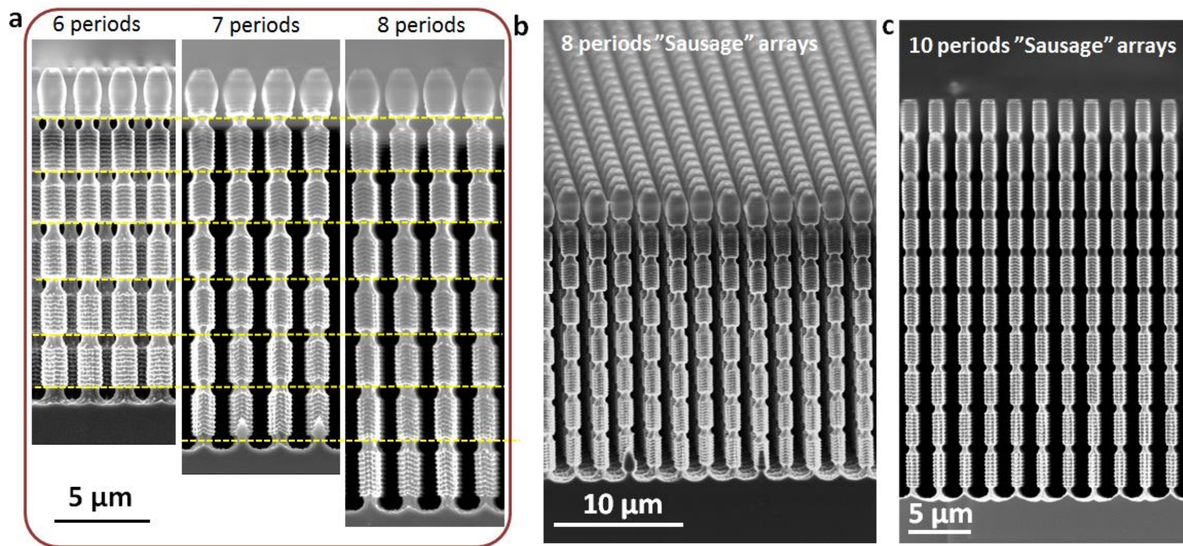


Figure 5.5. Relation between valve position, gas flow rate and measured pressure.

5.3 ETCHING BLACK SILICON

Black silicon is a kind of surface engineered silicon material, which has a strong broadband optical absorption in visible and infrared wavelengths. [163] The black silicon surfaces are microscopically composed of subwavelength nanocone structures, which can give interesting physical properties such as antireflection and hydrophobicity. By exploiting these properties, several applications have been successfully realized, e.g. sensors based on surface enhanced Raman spectroscopy, [164, 165] solar cells, [166] superhydrophobic surfaces, [167] etc. While the black silicon is proved to be of practical use, the fabrication process can be quite straightforward without any lithography steps, [168] sometimes the black silicon can even emerge as a side effect during device fabrications and undermine the device performances. Thus it is quite important to have a strict control of black silicon generation. Traditionally, black silicon can be fabricated with wet etch methods or a continuous plasma etch process with a gas mixture of SF_6 and O_2, in this part, we will discuss how to fabricate black silicon by DREAM processes, which have been proposed earlier in chapter 3, we will also see how the black silicon generation can be related to the etch profiles of structures and monitored by OES system.

The samples we used were bare silicon wafers from enclosed wafer boxes. The process parameters for the 4-step DREAM process are shown in **table 5.2**. In order to understand the black silicon generation, we will tune two parameters: deposition time and the gas flow rate of O_2. Theoretically, by increasing the deposition time, the deposited fluorocarbon layer will not be removed efficiently, thus the etch process will be blocked and black silicon

cannot be generated; while by increasing the O_2 gas flow rate, the etch profile will be more anisotropic, thus the gradient of optical constant is destroyed on sample surface, [169] and black silicon cannot be generated.

		4-steps DREAM cycle			
		Deposit FC	Remove bottom FC	Etch silicon	Ashing
Duration (s)		2.4	0.5	2.0	1.0
Gas flow (sccm)	C_4F_8	400	5	5	5
	SF_6	15	15	200	15
	Ar	200	250	250	200
	O_2	1	1	1	25
Generators (W)	13.56 MHz coil generator	3000	3000	3000	3000
	13.56 MHz platen electrode	1	50	1	1

Table 5.2. The recipe for a DREAM process to create black silicon.

SEM images of etched silicon surfaces are shown in **figure 5.6a**, 20 DREAM cycles were performed (corresponding to less than 2 min total process time) with the O_2 gas flow rate fixed at 25 sccm and the deposition time varying from 2.0 s to 2.8 s. We can clearly see a decreasing grain sizes when the deposition time is increased. Figure 5.6b shows the SEM images of structures from a cross section view, the scallops can be observed on the sidewalls of nanocone structures, we can see that the etch depth decreases for a longer deposition time, when the deposition time is set to 2.8 s, silicon is not etched, but the surface is covered with a thin layer of fluorocarbon film. While for a short deposition time of 2.0 s, the etch profile of the nanocones becomes more anisotropic with a larger etch depth. The measured etch depths and the diameters of nanocones are shown in figure 5.6c.

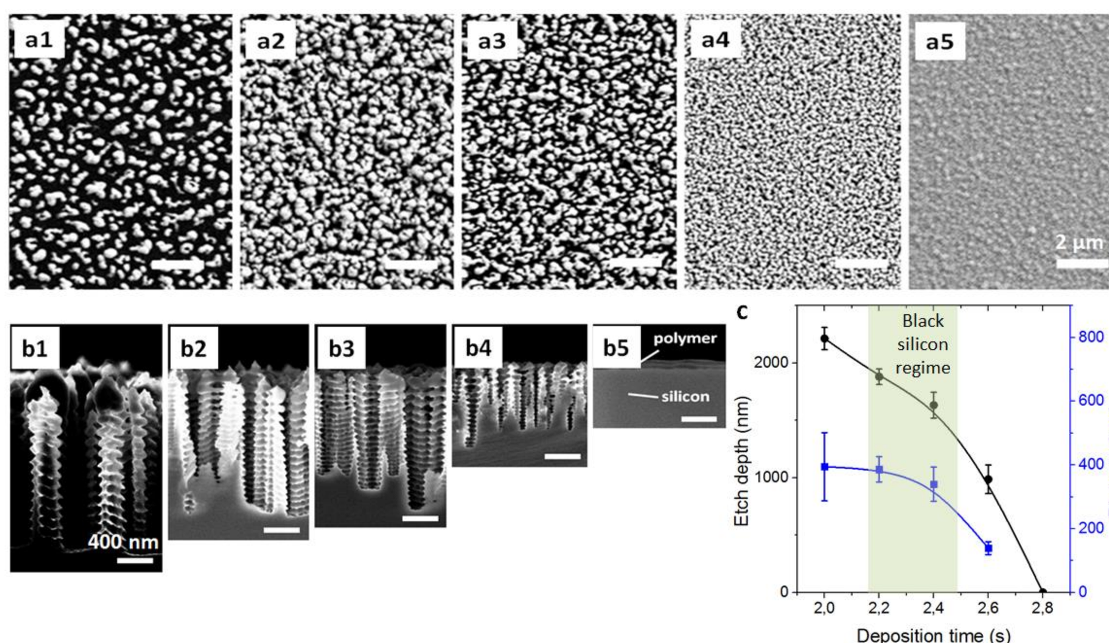
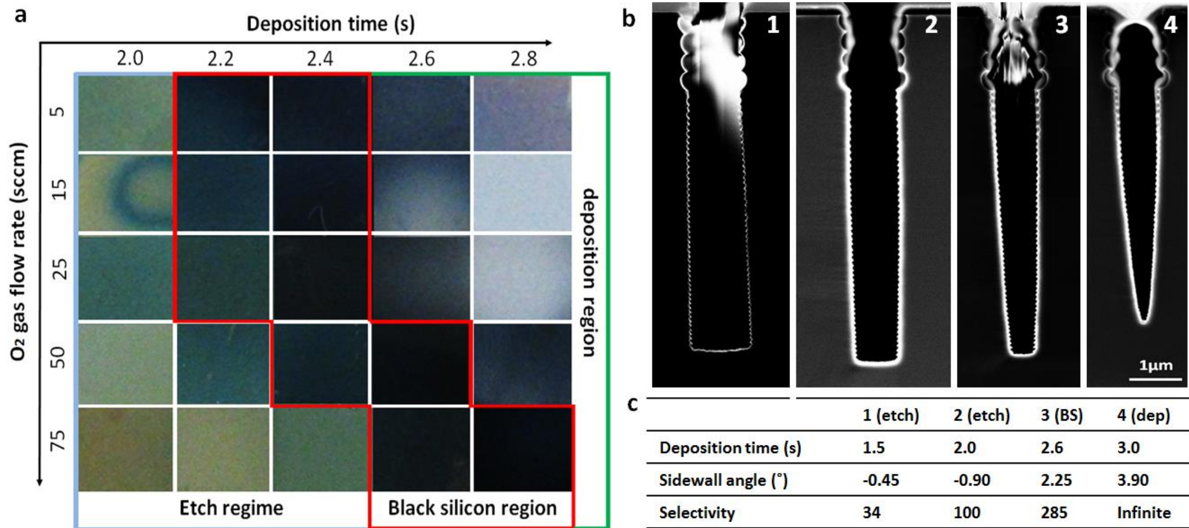


Figure 5.6. SEM images of (a) Etched silicon surface and (b) Etched silicon cross section; the measured etch depths and nanocone diameters are shown in (c).

The photographic images of etched silicon surfaces are shown in **figure 5.7a**, from which we can see the parameter space for black silicon generation. In order to eliminate the

influence from resist residues and fluorocarbon film, the samples in etch regime and black silicon regime have been cleaned with O_2 plasma ashing for 30 min. When the deposition time is increased, the etch process will fall into the deposition regime, and black silicon cannot be created. In order to bring the etch process back into black silicon regime, the O_2 gas flow should be increased. For a "perfect" black silicon with least optical reflections, the parameter window of deposition times is only around 0.2 s, which is quite narrow and makes the process sensitive to factors like gas flow stabilities, platen reflective powers, etc. This narrow process window makes black silicon as a good candidate to characterize the status of the etching apparatus.



	1 (etch)	2 (etch)	3 (BS)	4 (dep)
Deposition time (s)	1.5	2.0	2.6	3.0
Sidewall angle (°)	-0.45	-0.90	2.25	3.90
Selectivity	34	100	285	Infinite

Figure 5.7. (a) Photographic images of etched silicon surface to show the parameter space of black silicon; (b) SEM images of etched structure profiles with recipes for black silicon generation; (c) Etch performances of etch processes in (b).

It should be noticed that the black silicon can be correlated with the profiles of etched structures, which is known as the black silicon method. [21] In figure 5.7b are SEM images showing four etch profiles of 1 μm wide trench, which are created with different deposition time from 1.5 s to 3.0 s. For deposition times of 1.5 s and 2.0 s, which can create "brownish" silicon on a bare silicon surface, the etch profile is anisotropic with a slightly negative sidewall angle. For deposition time of 2.6 s, which can create a black silicon surface, the etch profile is straight and positively tapered. When the deposition time is increased to 3.0 s, the bottom of the trench is closed, and the trench opening is blocked by over deposition of fluorocarbon film. Having these corresponding correlations, we can "predict" the etch performance of patterned structures, just by etching a bare silicon wafer first and check if the surface is brownish, black or deposited with a layer of thin film.

The high optical absorption feature of black silicon also gives some special "fingerprints" on the OES monitoring systems, thus the creation of black silicon can be monitored in situ. In **Figure 5.8a** is a trend of optical emission intensity at 703.0 nm during 22 Bosch cycles, a decreasing intensity of more than 50% can be observed. The decreasing emission intensity can be observed in the whole spectrum from 200 nm to 800 nm as shown in figure 5.8b, and is considered to be the indication of black silicon formation, which will give a broadband optical absorption. It can also be noticed that, the decay of emission intensity at smaller wavelength happens before the decay at larger wavelengths, this is understandable, since the incoming light with large wavelengths is less "sensitive" to the nanoscale textures

compared with incoming light with small wavelengths. This trend of optical emission intensities can be used for end point detections of black silicon surface formation.

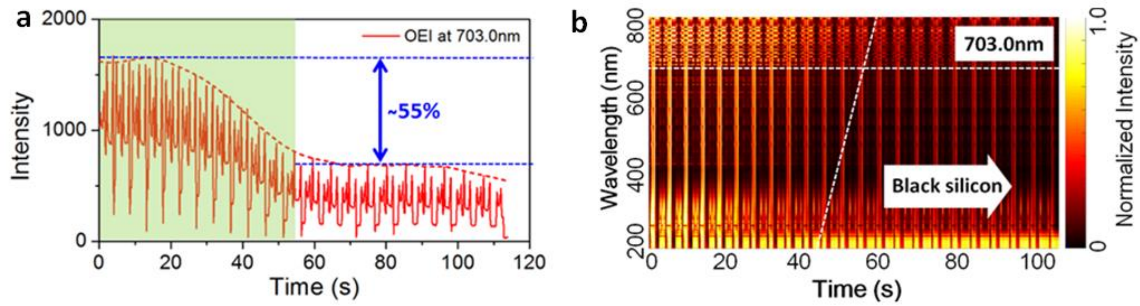


Figure 5.8. Monitoring black silicon formation with OES system. (a) The trend of optical emission intensity at 703.0 nm; (b) The trend of whole optical emission spectrum.

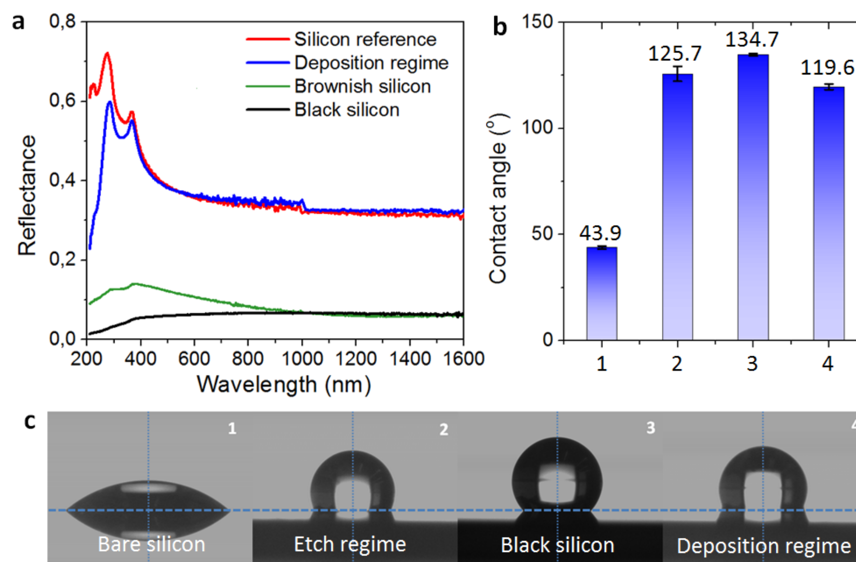


Figure 5.9. Properties of black silicon surface. (a) Reflectance spectra measured by ellipsometry; (b) Contact angles comparison for different substrate; (c) Photographic images of DIW droploets on different substrates.

The properties of fabricated black silicon are characterized. Firstly, the reflection spectra are measured by ellipsometry (with incident angle of 45° and reference sample as a silicon wafer coated with 25 nm thick silicon oxide). The spectra are shown in **figure 5.9a**. When the etch process is in a deposition regime, the reflectance is slightly reduced compared with bare silicon surface at wavelengths below 400 nm, possibly due to a strong UV absorption of deposited fluorocarbon film. For the black silicon surface, the reflectance is reduced to below 10% at the whole spectrum range from 200 nm to 1600 nm, which agrees with studies in previous literature. For "brownish" silicon, which lies in the etch regime, the reflectance is slightly higher than black silicon at wavelengths below 800 nm.

The hydrophobic properties are characterized with a drop shape analyzer (The Krüss DSA 100S). The DIW drop volume is set to be 1 μL and the flow rate is 30 μL/min. The measured contact angles are compared in figure 5.9b and the photographic images of drop shapes on different substrates are shown in figure 5.9c. While a bare silicon surface (with native oxide) is hydrophilic with a contact angle of 43.9°, the other substrates behave as hydrophobic. Compared with brownish silicon surface and silicon surface covered by fluorocarbon film,

the black silicon surface can give a larger contact angle of 134.7˚. This hydrophobic behavior is attributed to the stable trapped airpockets following the Cassie-Wenzel model. [170, 171]

5.4 ETCHING SILICON NANOSTRUCTURES

Plasma etching of nanostructures can be more tricky and delicate compared with etching microstructures. Since nanostructures are more vulnerable to structure roughness due to the small dimension, any instability of process parameters can introduce disruption to the structure geometries. Besides, effects from etching defects and nonuniformity will also be amplified on nanostructures. Generally speaking, for etching nanostructures, process parameters need to be scaled down compared with microstructures (as shown in the procedure for process optimization in figure 5.1). This again will approach the technical limits of etching apparatus, e.g. the flow rate accuracy of MFCs for gas species.

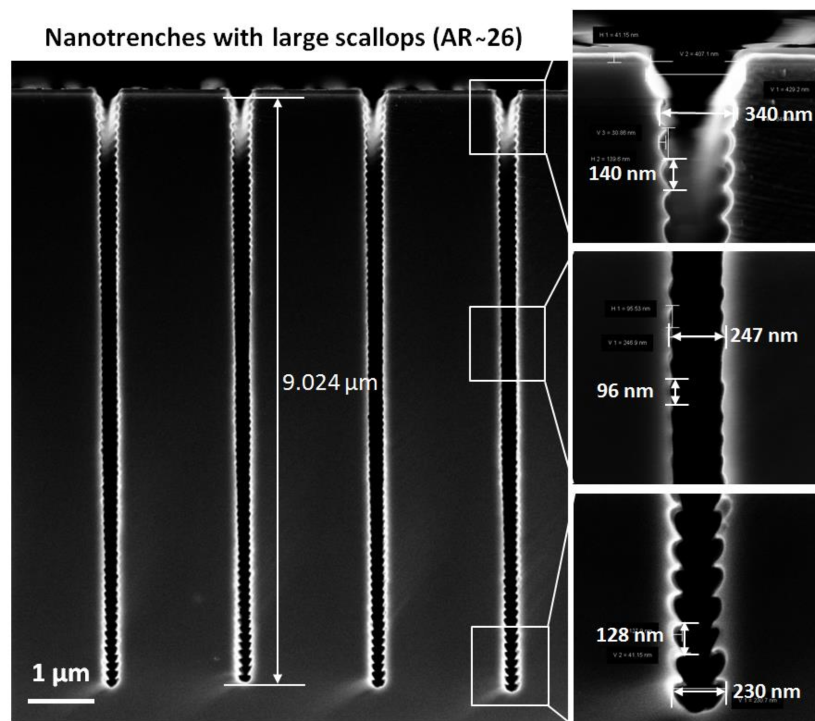


Figure 5.10. SEM images of silicon nanotrenches with large scallop sizes (100 DREM cycles).

Firstly, the applied coil power should be reduced compared with microstructures etching. Since a large coil power can increase the ion densities, the etch rate will be increased due to a larger ion flux and more radical corrosions, for a DREM process, the scallop sizes will be increased; in the same time, the processing pressure can also be increased due to a higher coil power (as shown in chapter 4), thus the directionality of incoming particles will be undermined, and more lateral etch will also generate larger sidewall roughness. Secondly, the platen power should also be reduced. Since the reduced coil power gives a smaller ion current, thus platen DC bias will increase if the platen power is not reduced correspondingly. Since nanostructures are more sensitive to nanoscale masks generated by mask sputtering or dirt from the chamber, the DC bias should be kept at a relatively low level, thus sputtering generated micro- and nanomasks can be avoided. Thirdly, the gas flows should be reduced to realize a low processing pressure, thus the ions can obtain better directionality during the ion transport process, and a better geometric fidelity can be

achieved, which is especially important for nanostructures. The low gas flow rates, however, can introduce inaccuracies as discussed in chapter 4, this is due to the technical limits of large capacity MFCs, and can be compensated by increase the duration of each step inside a DREM process.

We will demonstrate that silicon nanostructures with less sidewall roughness can be fabricated by scaling down the parameters as discussed above. **Figure 5.10** shows etched nanotrenches with a recipe that is dedicated for etching microstructures. The patterns are defined with DUV stepper lithography, with a 300 nm thick DUV resist and a 60 nm BARC layer. The patterned lines have a linewidth of around 200 nm and a structure period of 2 µm. An etch depth of 9.024 µm can be achieved after 100 DREM cycles etching (11 min 07 s), corresponding to an aspect ratio of ~ 26.5, with a straight profile. However, the scallop size is around 100 ~ 140 nm (depending on the position of the scallops), giving a lateral scallop size up to 40 nm, which is far away from the industrial requirements, e.g. the international technology roadmap for semiconductors 2.0 (2015 edition). [172]

		3-steps DREM cycle		
		Deposit FC	Remove bottom FC	Etch silicon
Duration (s)		3.2	1.0	2.5
Gas flow (sccm)	C_4F_8	40	5	5
	SF_6	15	15	40
	Ar	100	75	100
Generators (W)	13.56 MHz coil generator	1000	1000	1000
	13.56 MHz platen electrode	1	80 (for 1 sec)	1

Table 5.3. Parameter settings to etch silicon nanotrenches.

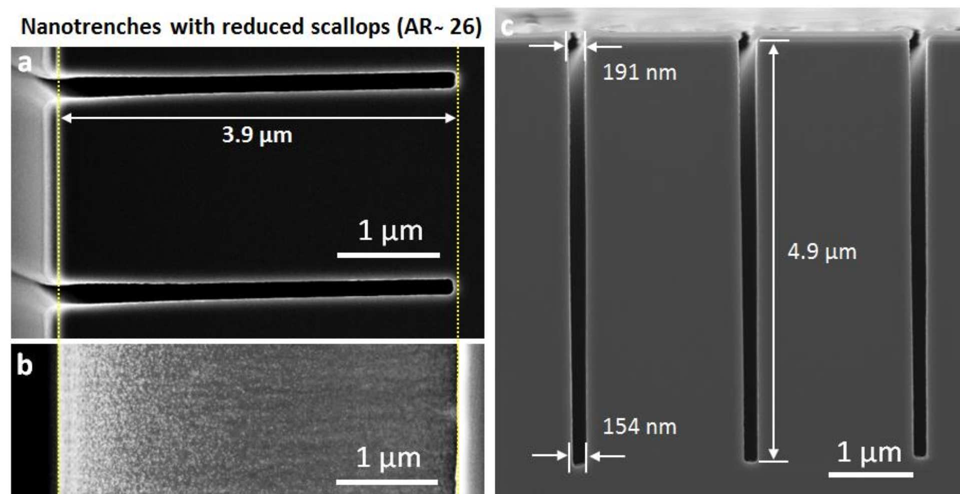


Figure 5.11. SEM images of silicon nanotrenches: (a) 100 DREM cycles; (b) Sidewall morphology after 100 DREM cycles; (c) 150 DREM cycles.

To reduce the sidewall roughness, the etching parameters (coil power, platen power and ga s flow rates) are scaled down as shown in **table 5.3**. SEM images of etched profiles are shown in **figure 5.11**, the pattern designs are the same compared with etched structures in figure 5.10. The etch depth is around 3.9 µm after 100 DREM cycles (etch time 10 min 19 s), with a smaller aspect ratio of 20.4. However, the scallop sizes are minimized, giving a

straight and smooth sidewall profile without undercut or linewidth broadening. The sidewall surface is shown in figure 5.11b, from which we can see the minimized sidewall scallops without any sidewall corrosions. When increasing the total number of cycles to 150 (etch time 16 min 44 s), the etch depth is increased to 4.9 μm, corresponding to an aspect ratio of around 26.

To etch trenches with even smaller linewidths, the patterns are defined by electron beam lithography with HSQ high resolution e-beam resist, which in the same time acts as a strong etching resistant mask. Lines with linewidths of 15 nm, 30 nm and 45 nm are patterned, with structure duty cycle of 50% and 20%, the thickness of HSQ resist is 50 nm. The etched profiles after 10 DREM cycles are shown in **figure 5.12** in which we can see the uniform etch profiles for lines with different linewidths and duty cycles. For line arrays with linewidth of 16 nm and duty cycles of 20%, a uniform etch depth of 390 nm can be achieved, corresponding to an aspect ratio of 24, while for duty cycles of 50%, a strong non-uniformity of etch depth can be observed, possibility due to the linewidth roughness of HSQ patterns after electron beam lithography, which then generate RIE-lag during plasma etching process. The etched structures have a minimized scallop size of ~40 nm, and the width of scallops is below 5 nm, thus the geometry of nanostructures is well-maintained.

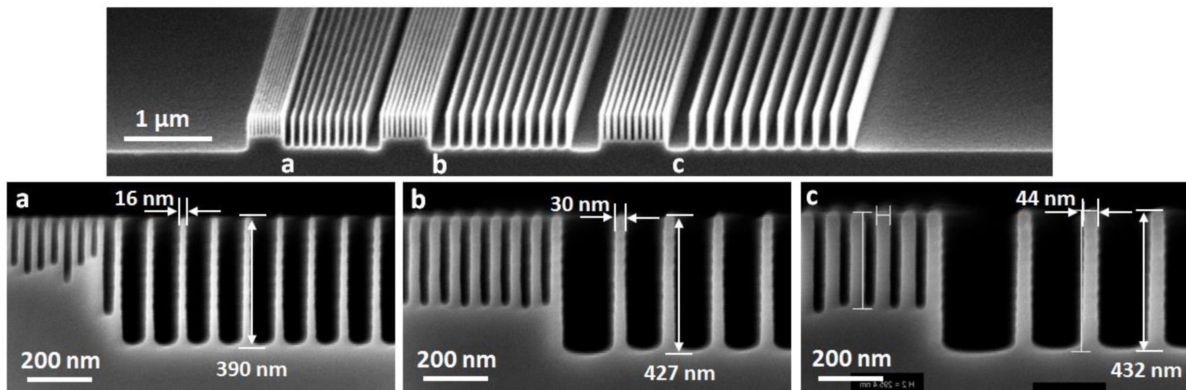


Figure 5.12. SEM images of etched silicon nanotrences with linewidths of (a) 15 nm; (b) 30 nm and (c) 45 nm. (10 DREM cycles)

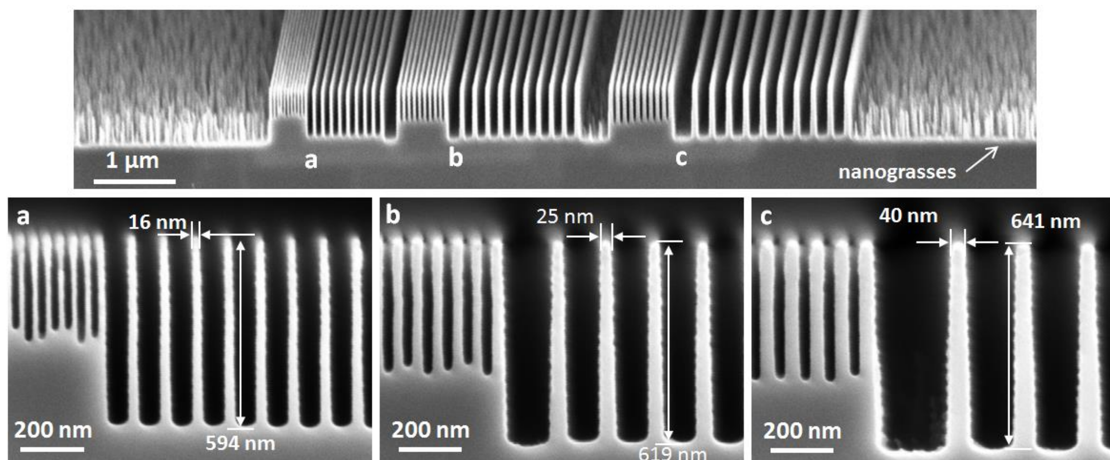


Figure 5.13. SEM images of etched silicon nanotrences with linewidths of (a) 15 nm; (b) 30 nm and (c) 45 nm. (20 DREM cycles).

When the total number of cycles is increased to 20, a higher etch depth can be reached, as shown in **figure 5.13**. For linewidth of 15 nm and duty cycle of 20%, the etch depth is increased to 594 nm, corresponding to an aspect ratio of ~ 37, and the etch profile remains straight with minimized scallop sizes. However, it can be noticed that there are nanograsses generated close to the structure area. Since the height of nanograsses is less than the etch depth of nanotrenches, and there are no grasses after 10 DREM cycles, we speculate the nanograsses might be generated during the etch process, possibly related to the sputtering of HSQ hard mask.

For silicon nanopore structures, an erosion effect is well known, which can damage the sidewall inside nanopores and lead to structure collapse. [173] In the same time, the standard cleaving method for sidewall inspection can be difficult to have a "clean" cut along the arrays of pores, setting obstacles for SEM characterization. In our study, holes with diameter of 220 nm are patterned by DUV stepper lithography with a 300 nm thick DUV resist and a 60 nm thick BARC layer, the hole-arrays have a square lattice type with a period of 400 nm. By performing 100 DREM cycles, an etch depth of 2.7 μm can be reached, corresponding to an aspect ratio of ~ 10 (as shown in **figure 5.14a**), the sidewall is slightly positive tapered, no sidewall erosion is observed. When the number of cycles is increased to 150, an etch depth of 3.8 μm is achieved with an aspect ratio of around 16 (as shown in figure 5.14b). However, sidewall erosions can be seen in the bottom part of the pores, which will destroy the structure geometry and limit the maximum achievable aspect ratio, common explanations of the sidewall erosion effect include ion angular distributions and image forces. The former suggests that when the aspect ratio increases, ion angular distribution will become sharper, inducing a positively tapered profile that is more vulnerable to direct ion bombardments, thus passivation layer in the bottom part will be removed and erosion will happen. The later suggests that the negatively charged silicon sidewall will attract incoming ions, thus the deflected ions will attack the sidewall directly and cause sidewall erosions. Because of the confined space inside a pore structure, both of the effects are enhanced, which will cause not only sidewall erosion, but also a smaller etch rate compared with other structures, like pillars or arrays. To reduce sidewall erosions, a smaller gas flow rate of SF_6 can be used as suggested in previous literature.

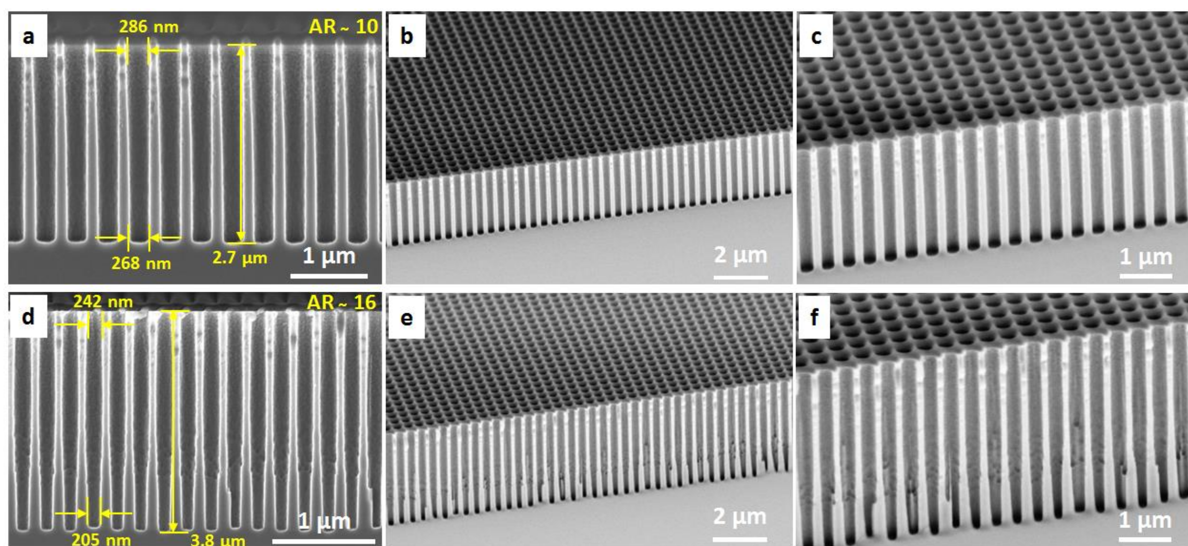


Figure 5.14. SEM images of etched silicon nanopores structures: (a-c) After 100 DREM cycles; (d-f) After 150 DREM cycles.

To etch silicon nanopillar structures, HSQ nanodots arrays are patterend by electron beam lithography and used as a mask. The diameter of the nanodots is 50 nm, with a square lattice type and period of around 150 nm. The SEM image suggests a straight profile of nanopillars after 10 DREM cycles (**figure 5.15a**). After 20 DREM cycles, an etch depth of 792 nm is reached, corresponding to an aspect ratio of 14. The silicon nanopillars remain a straight profile, while mask erosions can be noticed.

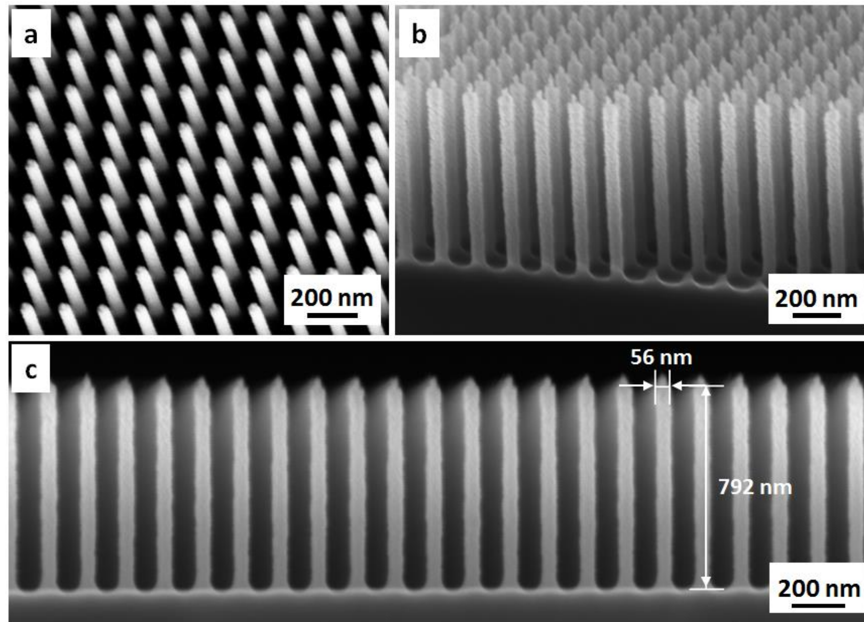


Figure 5.15. SEM images of etched silicon nanopillars: (a) After 10 DREM cycles; (b-c) After 20 DREM cycles.

5.5 Etching 3D silicon structures

3D silicon micro- and nanomachining has attracted a lot of interest in recent years for both research and industrial uses, and several promising applications have been proposed and demonstrated, e.g. vertically stacked silicon nanowires for FET, [174, 175] unified memory [176] and biosensors, [177] shape-modified silicon nanopillars for quantum transport study, [178] etc. However, to easily fabricate 3D micro- and nanostructures, and simultaneously obtain a good size and shape control of the fabricated structures, is still considered to be difficult. In this part, we will show how a modified DREM process can be used for 3D silicon engineering. This is based on the author's publication, [179] copyright 2018 IOP.

Firstly, a short review of previous studies is given on 3D silicon fabrication. Bottom-up methods can create single crystalline silicon nanostructures, and the morphology can be encoded, [180] however, this method is difficult to be integrated in traditional CMOS industries. Top-down approaches, which can transfer the 2D lithography patterns into silicon in a 3D structure have been studied extensively before, e.g. using wet etching [181] or plasma etching. Some of the plasma etching methods reported before rely on an additional oxidation procedure to protect the sidewall of the structures during the dry release step, [182, 183] however, the oxidation step and bottom opening step add extra fabrication complexity. Some other studies make use of the scallops generated during a Bosch process and the self-

limited oxidation process, however, the removal of the oxide layer after the etch processes requires special techniques, such as vapor release or critical drying release, especially for nanostructures, which are easily collapse under capillary forces.

Having the DREM process, which has been introduced in chapter 3, we can now create 3D structures conveniently by adding an extra isotropic etch in the total sequence. The process flow is shown in **figure 5.16a**. First the patterns were defined by traditional UV lithography (maskless aligner) with negative resist AZ nLOF 2020. Afterwards an anisotropic etch profile was created by a number of DREM cycles, then an isotropic etch was applied to provide an undercut to the anisotropic structures. These structures will then be freestanding and act as a mask for the second round of DREM process steps and another isotropic etch. Since the sidewalls of the anisotropic structures are well protected owing to the DREM process, the iteration of DREM processes followed by an isotropic etch could be repeated several times, thus more freestanding layers (each layer is defined by one DREM cycle) could be fabricated without collapse of the structure.

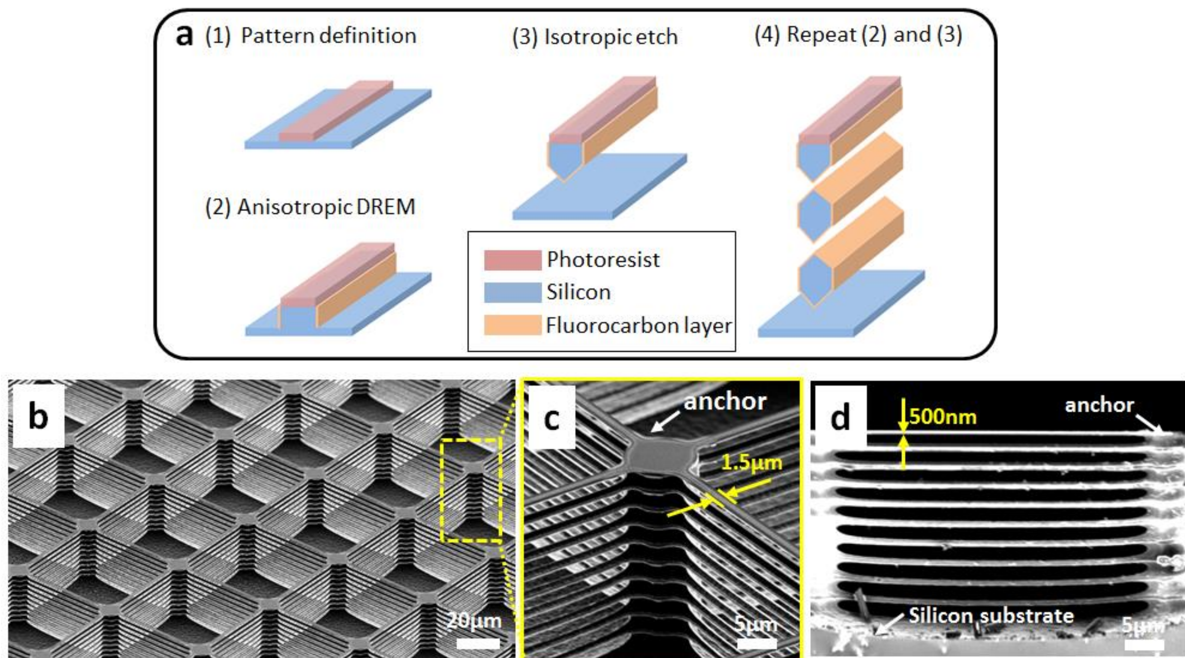


Figure 5.16. (a) Process flow for fabrication of 3D silicon structures; (b) SEM image of a 3D silicon microstructures with 10 isolated stacked layers, (c) zoom in of the region in (b), which shows the anchor part that holds 10 stacked silicon beams, (d) A cross section view of the 3D silicon structures.

A technical challenge during the process is the precise control of the geometry of the structures, e.g. to fabricate all the layers with an identical thickness (i.e. exact same etch depth per cycle independent of the aspect ratio). This is crucial for the fabrication of 3D structures that suitable for practical applications. In our study, this technical issue is solved by applying a process parameter ramping technique, which has been introduced earlier in chapter 3 to compensate for the etch nonuniformity caused by ARDE. In the 3D fabrication process, both the etch rate during each cycle of the DREM process and the isotropic etch rate will slowly decrease as the etch process progresses down into the silicon, and this issue can become particularly significant when we want to create a number of suspended (freestanding) layers. To compensate for this effect, we slowly increase the time of the etch cycle in our DREM process, so the scallop size will be constant down into the silicon, and an excellent thickness uniformity of the different suspended layers can be achieved. At the

same time, the duration of the isotropic etch cycle is also increased, thus the size of the gap between each two suspended layers is identical. This parameter ramping procedure is crucial in order to have precise size control of the fabricated 3D structures, which is otherwise difficult and cumbersome with alternative fabrication techniques. All the parameter settings are shown in **table 5.4**. Figure 5.16b shows a fabricated 3D silicon microstructure, consisting of 10 suspended layers of beam structures supported by pillars, which are larger in size and act as anchors, so the isotropic etch step will not undercut and release the whole structure. An enlarged view is shown in figure 5.16c, where we can clearly see the suspended beams (with a width of 1.5 μm, and length of 50 μm), and the vertical supporting anchors (with a diameter of 10 μm). A cross section view is shown in figure 5.16d, where we can see the suspended beams, which have a uniform thickness of around 500 nm, and the gaps between each two suspended layers also have a uniform size of around 2.5 μm.

	DREM process step			Isotropic etch step
	Deposition	Bottom removal	Etch	
Time (s)	1.0	0.5	Ramping up from 2.5s	Ramping up from 10s
C_4F_8 gas flow (sccm)	400	5	5	5
SF_6 gas flow (sccm)	15	15	600	600
Argon gas flow (sccm)	250	75	250	250
Coil power (W)	3000	3000	3000	3000
Platen power (W)	0	300	0	0
Pressure (mTorr)	20	5	20	20
Temperature (°C)	-19	-19	-19	-19

Table 5.4. Parameter settings of a modified DREM process for etching 3D silicon microstructures.

By applying the fabrication technologies discussed above, different kinds of freestanding structures can be fabricated. In **figure 5.17** are three kinds of structures etched from the same mask design, which is a double spiral structure with anchors and beams (with a linewidth of 2 μm). Three different fabrication sequences were applied as shown in figure 5.17d. Figure 5.17a shows a cantilever like beam structure, which is fabricated by 10 DREM cycles followed by an isotropic etch release. Figure 5.17b shows capacitor-like structures, which are etched by 50 DREM cycles followed by a final isotropic etch step. Figure 5.17c shows five isolated structures, each layer is etched with 10 DERM cycles followed by an isotropic etch, giving a thickness of around 2 μm for each isolated layer. From the results we can see the flexibility of this approach, which makes fabrication easy to program for different applications. However, it should be noted that, in order to have a uniform size distribution of different suspended layers, the etch speed should be controlled precisely, so the scallop size distribution is uniform (as shown in figure 5.17e). This is accomplished by the parameter ramping technique discussed earlier.

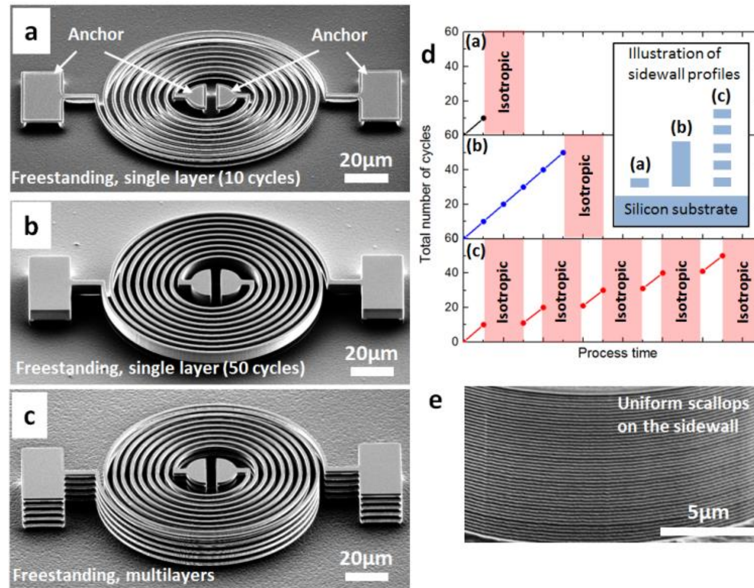


Figure 5.17. Different strategies to create freestanding structures: (a) one suspended layer which consists of 10 DREM cycles; (b) one suspended layer which consists of 50 DREM cycles; (c) five suspended layers, each layer consists of ten DREM cycles; (d) A schematic view of the processes in (a) (b) and (c), and an illustration of cross section view of the structures in the inset; (e) a zoom in view of the scallops on the sidewall of structures in (b).

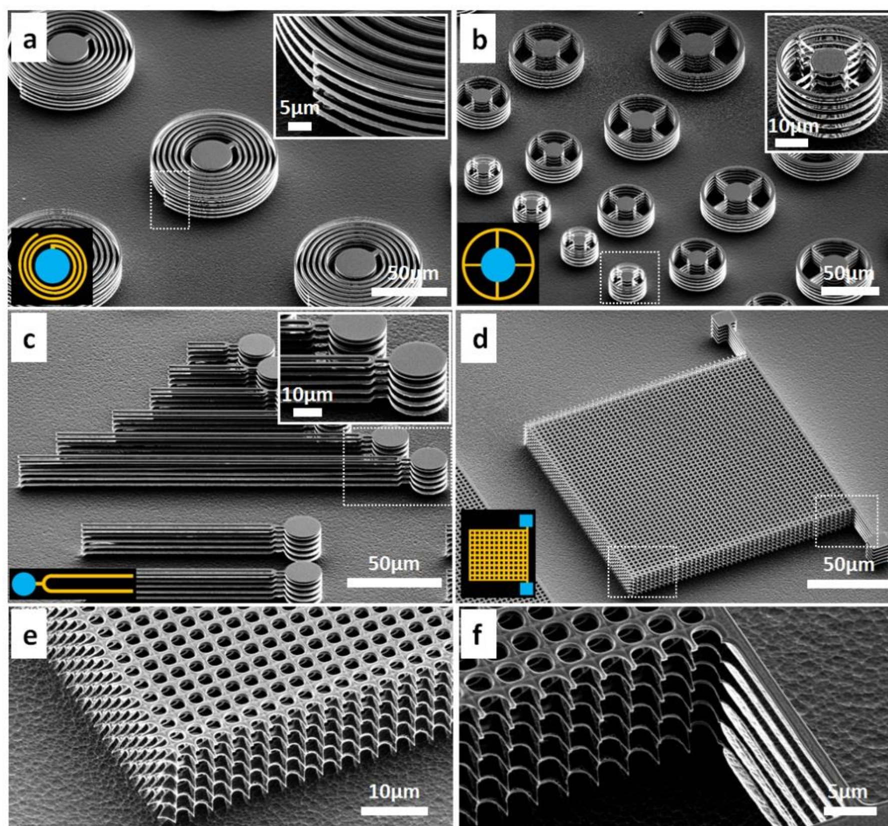


Figure 5.18. SEM images of different complex 3D microstructures (from (a) to (d)). A schematic view (bottom-left corner in each image) shows the anchor parts (blue) and the stacked layer parts (yellow). Zoomed in images are shown in the insets (top right corner) in (a), (b) and (c), which show the details of the parts in dashed squares in the SEM images. (e) and (f) are zoom in images from two regions labeled in (d).

By designing the patterns properly, different structures with complicated pattern designs can be fabricated as presented in **figure 5.18**. Five sequences of ten DREM cycles each followed by an isotropic etch were performed in (a), (b) and (c). Figure 5.18a shows arrays of spiral-like structures with the anchor in the middle, the linewidth of the suspended beams is 2 μm, and the gap between the beams is 2 μm. Figure 5.18b shows arrays of stacked ring resonator-like structures with different diameters, the linewidth of the ring is 2 μm. Figure 5.18c shows arrays of tuning fork-like structures with different length from 20 μm to 200 μm, the linewidth of the suspended beams is 2 μm. An enlarged section of the image is shown for each structure, which gives more details regarding the isolated layers. In Figure 5.18d is a 3D photonic crystal-like structure, which is created by six sequences of five DREM cycles each followed by an isotropic etch. The fabricated structure has six stacked layers of holes with a square lattice type, the diameter of the holes is 3 μm and the periodicity is 4 μm (an enlarged view of the structures are shown in figure 5.18e and figure 5.18f). A simple illustration is also shown in the bottom left corner of the image to show the anchors (blue) and suspended structures (yellow). This figure shows the flexibility of our fabrication technique.

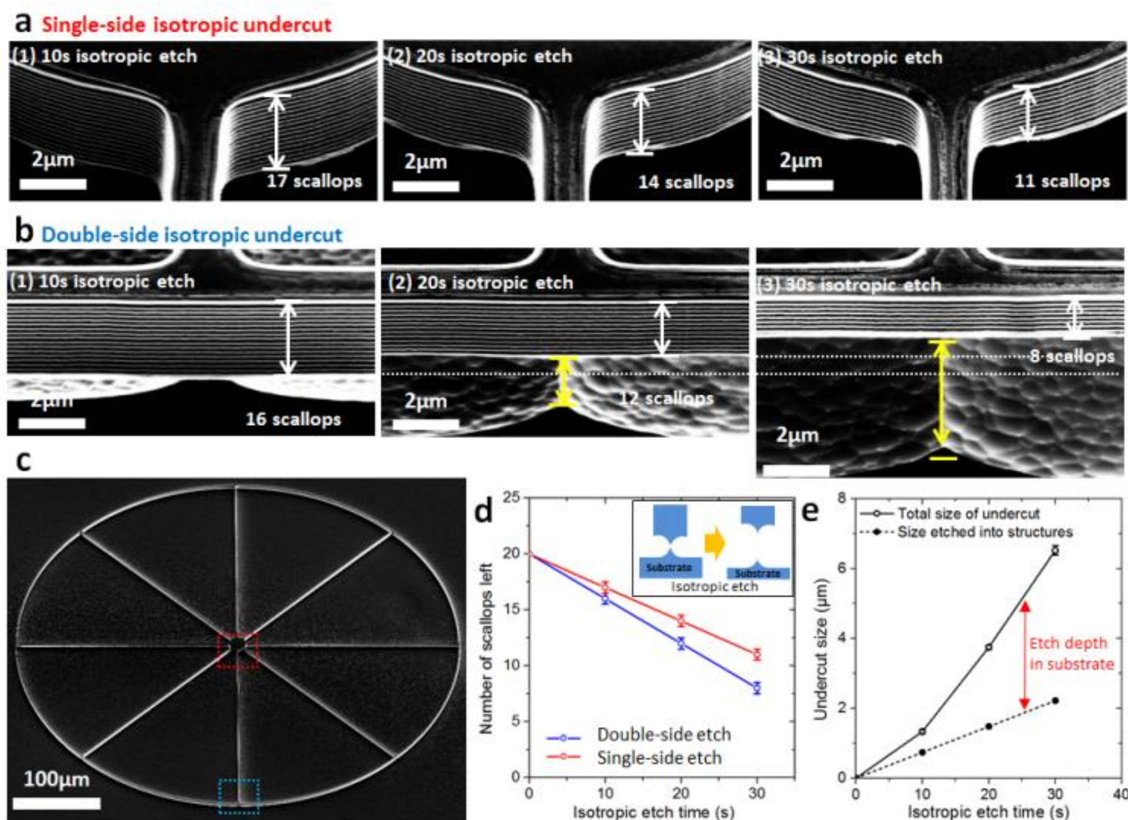


Figure 5.19. The influence of isotropic etch on freestanding structures. For regions with single-side isotropic undercut (a) and double-side isotropic undercut (b) with different isotropic etch time. The regions in (a) and (b) correspond to regions in the structure as shown in (c). The isotropic etch rates of the scallops being etched are shown in (d), with a schematic view of the structure change after isotropic etch process. The gap size between freestanding structures and the substrate is shown in (e).

It should be noted that the bottom part of anisotropic structures will be consumed slowly upwards during the isotropic etch step, which will change the thickness of the suspended structure and additional calculations are thus needed to have a precise size control of these structures. To illustrate the demolishing effect of isotropic etch on anisotropic structures, a wheel-like pattern with diameter of 500 μm is designed as shown in **figure 5.19**. The rim of

the wheel and the spokes has a width of around 2 μm, and the whole structure is supported by an anchor in the center, which has a diameter of 15 μm. In the experiments, 20 DREM cycles were first applied to create anisotropic structures, and then an isotropic etch was applied with different durations of 10 s, 20 s and 30 s. It is found that the number of remaining scallops on the anisotropic structures decrease linearly with increased isotropic etch time (figure 5.19a and figure 5.19b), which suggested a constant isotropic etch rate into the structures of 60 nm/s (in the anchor region) and 80 nm/s (in the rim region) as shown in figure 5.19d. This phenomenon can be explained qualitatively as follows: while the sidewall of the anisotropic structures is well protected by the FC layer, SF_6 based etching species will etch isotropically and undercut structures, thus the bottom of the structure is exposed to fluorine radicals and slowly gets thinner. This process is geometry (shape) dependent, thus spokes and rims will be attacked from different directions after being released, thus the etch rate into structures will be higher than in the central support, where the isotropic etch can only attack the structure from one side. This phenomenon is important, since it will determine both the thickness of suspended structures and the size of the gap between two adjacent suspended layers, which are two important parameters to design 3D structure based devices. The anisotropic structures will be slowly etched away from the bottom, which will give a contribution to the final size of the gap (figure 5.19.e) and should be considered during design. To give a practical example, in some cases a large gap size is favored, to achieve this, we shouldn't just increase the isotropic etch time, since it will totally demolish the anisotropic structures. A more proper way, however, is to increase the number of cycles during the DREM process, and in the same time increase the isotropic etch time.

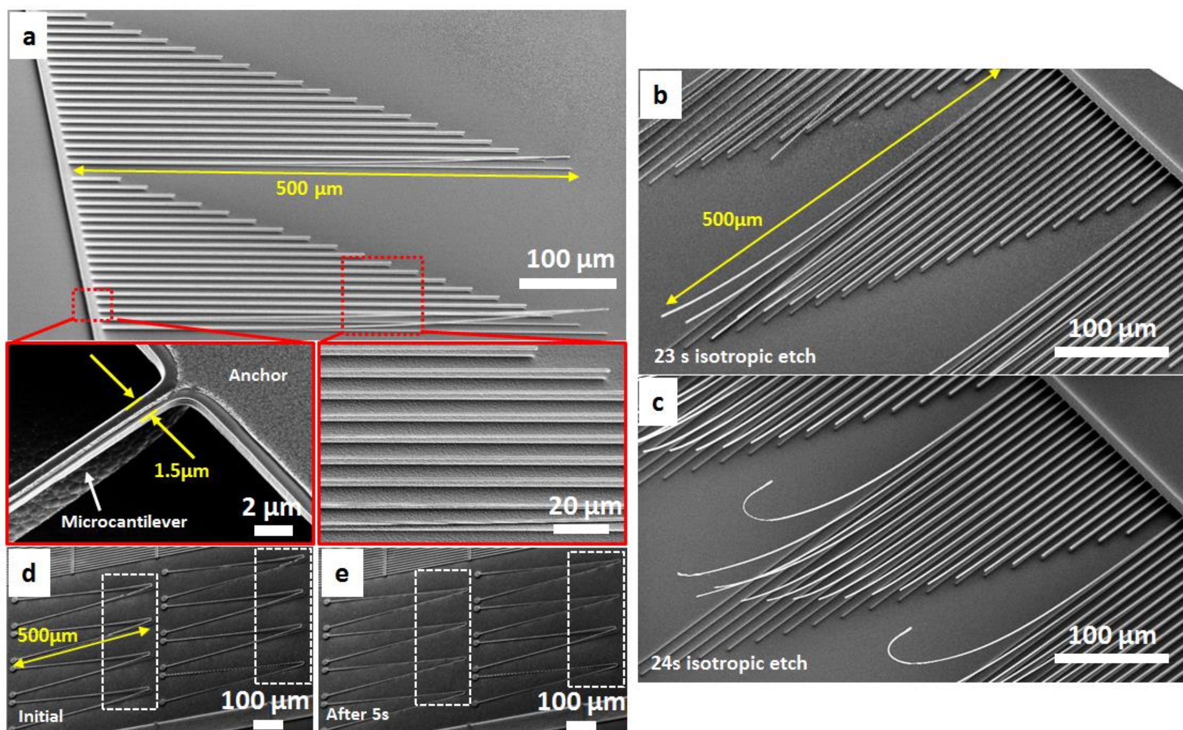


Figure 5.20. Ultralong silicon micocantilevers created with 20 DREM cycles followed by 22 s isotropic etch. (a) Cantilevers with length up to 500 μm, with enlarged view from the anchor region and the center of the cantilevers; (b-c) Curving of ultralong silicon microcantilevers when the isotropic etch time is increased; (d-e) Attaching phenomena for microcantilevers under SEM showing the initial morphology and after 5 s.

By precisely controlling the isotropic etch step, we can fabricate some ultralong cantilever-like structures, which normally require silicon on insulator (SOI) wafers and the buried oxide layer is then removed after the plasma etch. To prevent the structures from collapse due to the capillary force, some special techniques are needed, e.g. critical point drying after HF solution removal, [184] XeF2 etching, [185] or vapor-phase HF etching. [186] In our experiments, the undercut is created directly during the plasma etching process, thus the stiction effect can be avoided. **Figure 5.20a** shows two sets of cantilever structures, which were fabricated by 20 cycles of DREM followed by 22s of isotropic etching. The width of the cantilever is around 1.5 μm and the thickness of the cantilevers is around 300 nm, the lengths of the cantilevers are from 50 μm up to 500 μm, and they are completely free-hanging above from the substrate (shown in the enlarged view). When the isotropic etch time is increased, the cantilevers start to bend upwards, while the silicon cantilevers should be stress free, the reason behind the phenomena is still not clearly, and will be studied in the future. During the scanning with SEM, the tips of fabricated cantilever beams are also observed to clamp on the substrate (figure 5.20d and figure 5.20e). This can be explained as the electrostatic attraction force caused by the charge accumulation on beams and substrates, implying potential applications for switches and electrostatic actuations. [187, 188] This type of long cantilevers with thin thickness have also been demonstrated to have small spring constants to detect small forces [189] or to measure the mechanical properties of thin films coated on silicon. [190]

3D microstructures can already bring new possibilities to microfluidics, micromechanics, microelectronics and other applications. To shrink the CD further and create 3D nanostructures can give us novel insights into fundamental phenomena. This becomes very relevant when the CD of the structures is comparable to or below some characteristic lengths of a physical system, e.g. the wavelength of light, the mean free path of electrons or the electron phase coherence lengths. Compared with the methods to fabricate 3D silicon microstructures as discussed above, some additional technical issues need to be addressed for nanoscale, and the major challenge is to have a profile control with higher precision, which has been discussed earlier in section 5.4. Since the CD of the nanostructures can be below 100 nm, which is even smaller than the scallop size for already presented 3D microstructures, the recipe has to be adapted and parameters need to be scaled down, so that the sizes of scallops and undercuts can be minimized.

	DREM process step			Isotropic etch step
	Deposition	Bottom removal	Etch	
Time (s)	0.4	1.0	2.5	1
C_4F_8 gas flow (sccm)	40	5	5	5
SF_6 gas flow (sccm)	10	10	30	30
Argon gas flow (sccm)	100	75	100	100
Coil power (W)	500	500	500	500
Platen power (W)	0	80	0	0
Pressure (mTorr)	6	3	6	6
Temperature (˚C)	-19	-19	-19	-19

Table 5.5. Parameter settings of a modified DREM process for etching nanostructures.

In **table 5.5** we can see the parameter settings to create 3D nanostructures. In order to reduce the etch rate, the density of radicals should be decreased, thus a smaller coil power

of 500 W is applied, and the gas flow ratio of SF_6 is also reduced. By doing so a scallop size of around 15 nm could be achieved (compared with the large scallop size of around 200 nm for microstructures). The platen power is also reduced during the bottom removal step of DREM process, which helps to reduce the roughness caused by resputtering (which is more crucial for nanostructures). The parameter ramping technique was not performed for the nanostructure etching, since for nanostructures the aspect ratio is not as large as for the microstructures, thus the ARDE or RIE-lag is less prominent.

Some 3D silicon nanostructures are shown in **figure 5.21**. EBL and HSQ e-beam resist were used to define the high resolution patterns, which include cross-like structures (figure 5.21a1) and nanowire structures (figure 5.21b1), the smallest size of the patterns is around 20 to 25 nm, and larger patterns are defined to act as anchors for the suspended 3D structures. After several iterations of DREM and isotropic etch, 3D nanostructures are created from cross-like patterns (two stacked layers in figure 5.21a2, three stacked layers in figure 5.21a3, four stacked layers in figure 5.21a4, and nanowire patterns with four stacked layers in figure 5.21b2. Five DREM cycles were applied during each anisotropic etch part, thus giving a height of around 50 to 60 nm for each layer of nanostructures, and the size of the gap between each two layers is around 50 nm. The LER of the HSQ patterns is measured to be below 3 nm, and the sidewall roughness is minimized by reducing the etch rate, thus the fabricated silicon nanowires (SiNWs) arrays in figure 6b (2) show a very good size uniformity, which is favorable for applications in nanophotonics and nanoelectronics, where the exact geometry of the structures is crucial.

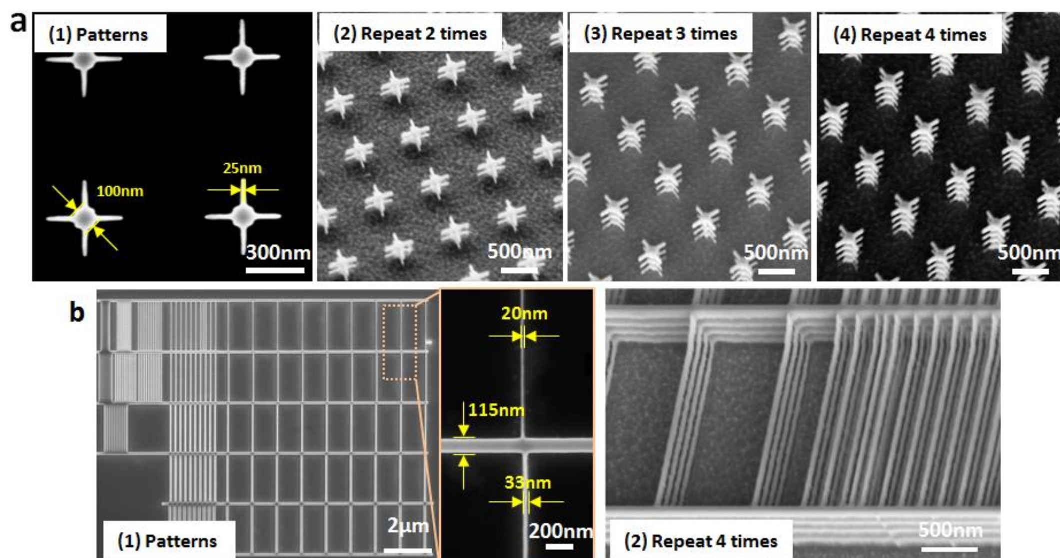


Figure 5.21. Fabrication of 3D silicon nanostructures: (a) Cross-like structures defined by EBL (1), after plasma etching to create different numbers of stacked layers as shown in (2), (3) and (4); (b) SEM images of SiNWs structures patterned by EBL (1), and 4 stacked layers of SiNWs after etching (2),

5.5.1 Vertically stacked silicon nanowires for structural colors

To briefly demonstrate one possible application of the 3D SiNWs, pixels were written (with pixel size of 2 µm by 2 µm) to form a graph, each pixel is composed of two stacked layers of SiNWs with linewidth of 50 nm, height of 50 nm, length of 2 µm and pitch of 300 nm as in **figure 5.22a**. These SiNWs have been shown previously to possess size and polarization dependent light scattering properties, which can give enhanced light scattering intensity in certain wavelength regions. [191 - 193] By tuning the period and the linewidth of SiNWs, vivid

structural colors can be generated in a wide spectrum. The resolution of the color printing is limited by the size of a single pixel, when each pixel unit is reduced to 1 µm by 1 µm, a spatial resolution of 25000 dpi (dots per inch) can be achieved. In figure 5.22b, pixels are used to pattern letters of "DANCHIP" with a bright yellow color. When the polarization of light is perpendicular to the direction of SiNWs, the resonance can be induced, while when the polarization is rotated by 90˚, the electromagnetic field is not confined, thus no structural colors can be observed. Nanomesh structures, which can be considered as a 2D extension of SiNWs, can also generate polarization dependent structural colors. To verify this, different patterns are defined with EBL as shown in figure 5.22c and figure 5.22d. Cross-like structures are defined by two sets of SiNWs with different linewidths of 40 nm and 60 nm, while 4 different nanomesh structures are patterned, #1 and #2 are composed of lines with different linewidth, with 40 nm in vertical direction and 60 nm in horizontal direction, the period of lines is set to be 200 nm for #1 and 250 nm for #2; #3 and #4 are nanomeshes with the same linewidth in both directions but different periods of lines. After stacked two-layer structures are created by a modified DREM process, structural colors can be observed in a bright field optical microscope (figure 5.22e). It can be noticed that the structural colors of #1 and #2 are polarization dependent, while #3 and #4 are polarization independent. This type of 3D silicon nanomesh structures is promising for applications like 3D metasurfaces or dual color printing in nanoscale. [194]

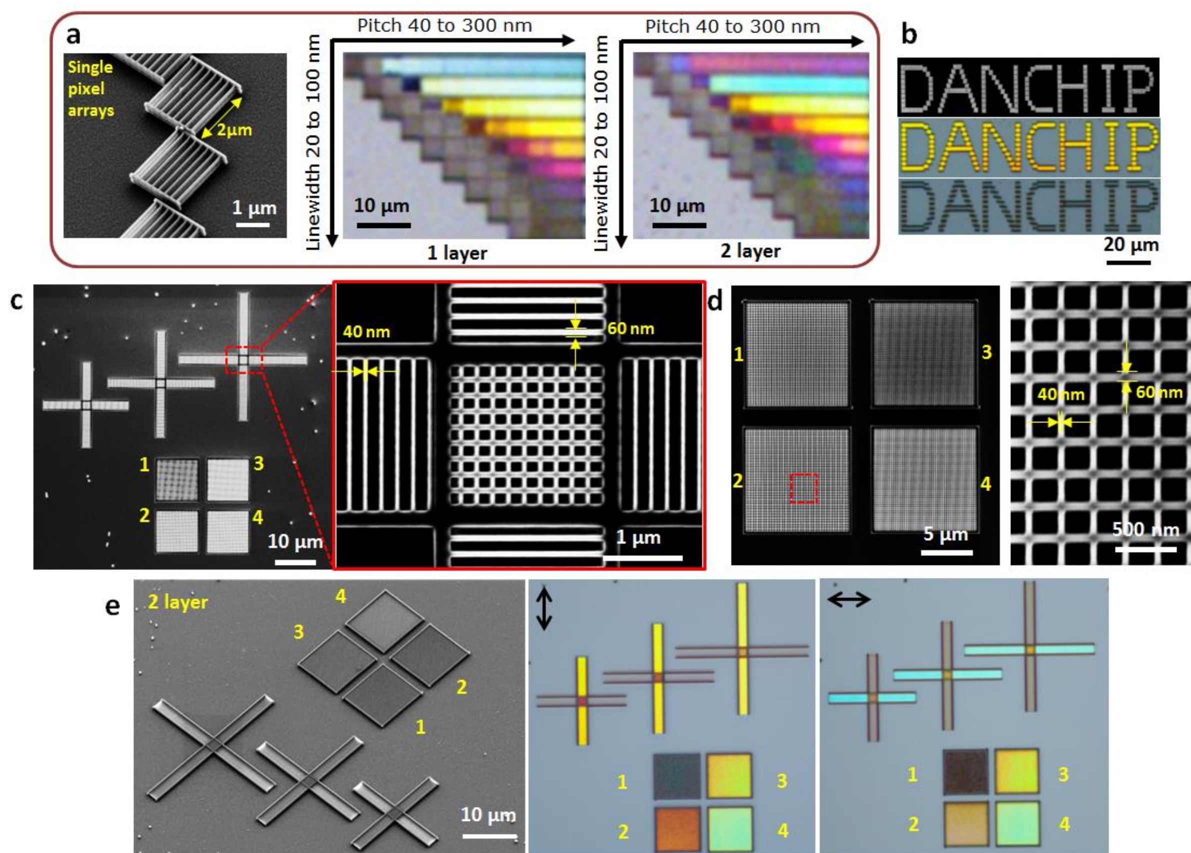


Figure 5.22. (a) SEM image of a single pixel made by two stack layers of SiNWs, and the generated structural colors depend on the period and the width of SiNWs; (b) A graph of "DANCHIP" patterned by pixels of stacked SiNWs, from top to bottom: SEM image, optical microscopic graph when the incident light polarization is perpendicular to the direction of SiNWs, and the optical microscopic graph when the incident light polarization is along the direction of SiNWs; (c) EBL patterns to create both SiNWs and nanomeshes; (d) SEM image of EBL patterns for nanomesh structures; (e) 3D nanostructures after etching with two stacked layers, and the generated structural colors.

Compared with previous studies on structural colors induced by light scattering of SiNWs, this method doesn't rely on a complicated SOI structure. By changing the gap size between stacked layers and the period of the nanowires, the optical coupling strength of resonance modes from adjacent SiNWs can be modified, allowing for a fine tuning of resonance light scattering. This subject will be studied in the future.

6 Novel devices and applications

Now we have discussed thoroughly about improvements of plasma etching techniques for micro- and nanofabrication of silicon structures, importantly, we have introduced DREM process and modified DREM process for engineering 3D micro- and nanostructures, which can be promising for a wide spectrum of devices and applications. In this part, we will demonstrate two examples of novel applications with fabricated 3D silicon structures. Firstly, we will see how functional materials can be integrated with 3D silicon micro-mesh structures, and the loading gain of the photocatalytic and photoelectric performances can be then enhanced, this work is based on and reproduced with permission from the author's publication [195] (Copyright 2018 Wiley). We will also demonstrate a 3D photonic crystal (PhC) membrane nanostructure, which possesses a 3D simple cubic (SC) periodicity. This part is based on a submitted work of the author (Copyright 2018 Wiley).

6.1 Highly ordered silicon micro-mesh structures integrated with ZnO nanowires for photocatalysis and photocurrent

In this part, we will see how ZnO nanowires (NWs) can be integrated with 3D silicon microstructures fabricated with modified DREM processes. The photocatalytic and photoelectric properties will then be characterized for the fabricated hybrid structures.

6.1.1 Background introduction

Low dimensional materials, e.g. nanoparticles or nanowires, have some attractive properties and have been studied extensively in the past years. In order to achieve an improved performance of their desired functions, a common strategy is to integrate the low dimensional materials onto 3D substrates to increase the loading gain of the functionalities, sometimes heterojunctions can also be formed and new properties can be explored. Although the potential of 3D structures is attractive, a reliable fabrication strategy is considered to be technically difficult. Bottom-up synthesis of 3D foams constituted by metals (Cu, Ni, Al, etc.) or graphene are widely used, however, the geometry and morphology of the 3D structures are difficult to be controlled. Another category of top-down fabricated 3D structures employs traditional micro- and nanofabrication techniques

from the semiconductor industry, which show the superiority for on-chip integration and mass production.

ZnO, as a typical direct wide band gap (E_g = 3.37 eV) semiconductor, can generate free carriers by incident photons and be utilized for a wide range of purposes, e.g. dye sensitized solar cells (DSSC), [196] photocatalytic reactions, [197] supercapacitors, [198] etc. Besides, the notable piezoelectric properties in ZnO nanostructures also make it a good candidate for applications as electric generators [199] and piezo-phototronic devices. [200] Apart from the intrinsic physical and chemical properties, the geometry and morphology of ZnO nanostructures are also important parameters. By adjusting the nucleation and growth during the materials synthesis, ZnO nanostructures with a wide range of morphologies have been successfully achieved. [201] Among these, ZnO NWs show unique advantages due to the facile fabrication process and the high spatial density, making ZnO NWs outperform other nanoscale counterparts in different applications, such as sensors [202] and field electron emission. [203]

By increasing the spatial density of ZnO NWs, more reactions will take place in a unit volume of surrounding medium, mass and ion transportation will also be accelerated during device working. For example, branched hierarchical ZnO NWs have been proposed before with a repeated seed deposition-hydrothermal growth method. Compared to the conventional ZnO NWs without branches, the 3D ZnO nanotrees show a density increasing with 1-2 orders of magnitude, and 5 times improvement of the overall light-conversion efficiency for DSSC applications. [204] Another strategy is to use different 3D structures as substrate for the growth of ZnO NWs, i.e. graphene foams, [205] nickel foams, [206] or silicon NW arrays, [207] but the geometry control of the substrate is normally poor, and on-chip integration can be difficult.

Here we will apply the well-developed DREM process to create mesh-like microstructure. The surface area can be increased by around one order of magnitude compared to a 2D planar substrate. The fabricated 3D mesh structures are then integrated with high density ZnO NWs. The photocatalytic degradation performance of the structures is tested with rhodamine B (RhB), and photocurrent response property is characterized with UV light illumination. ZnO NWs can also be used as self-sacrificed templates and chemically converted into other zinc-based compounds, such as zinc sulfide (ZnS) and ZIF-8, while the original 3D NW morphology can still be inherited. It should be noted that the whole process is carried out at a relatively low temperature of below 200 ˚C, which is within the process limit of CMOS systems and most of the polymer materials, [208] enabling flexibility and freedom for different applications.

6.1.2 Fabrication and characterization

Double side polished silicon wafer (100 mm, n-doped, 1-20 Ω cm) was used to fabricate 3D silicon micro-mesh structures. Patterns were defined by maskless aligner system (MLA100, Heidelberg) with a negative tone resist AZ nLOF 2020 (MicroChemicals). Modified DREM processes were then performed to create 3D silicon mesh structures with DRIE Pegasus system (SPTS). After etching, the samples were cleaved into pieces with size of 1.2 cm by 1.2 cm, and cleaned with O_2 plasma inside a barrel-type 2.45 GHz microwave plasma ashing system (PVA TePla 300). ZnO seed layers were deposited on the cleaned 3D silicon substrates using a thermal ALD system (Picosun R200), the parameter settings for thin film growth has been introduced in chapter 2. ZnO NWs were then synthesized by a hydrothermal reaction. Typically, hexamethylenetetramine (HMTA, 0.1 g) and zinc nitrate

hexahydrate ($Zn(NO_3)_2$, 0.22g) were mixed and dissolved in 60 mL of DIW. The mixture was then transferred into a Teflon-lined stainless-steel autoclave with 100 mL capacity. The chips were put upside down in the solutions, and the autoclave was sealed for solution reaction at 90 °C for 20 h. A schematic view of the fabrication process flow is shown in **figure 6.1a**, which includes pattern definition with conventional UV lithography, creation of 3D silicon microstructures with a new plasma etching process, ZnO layer coating with ALD, and the final step of hydrothermal reactions to grow ZnO NWs onto the 3D silicon structures.

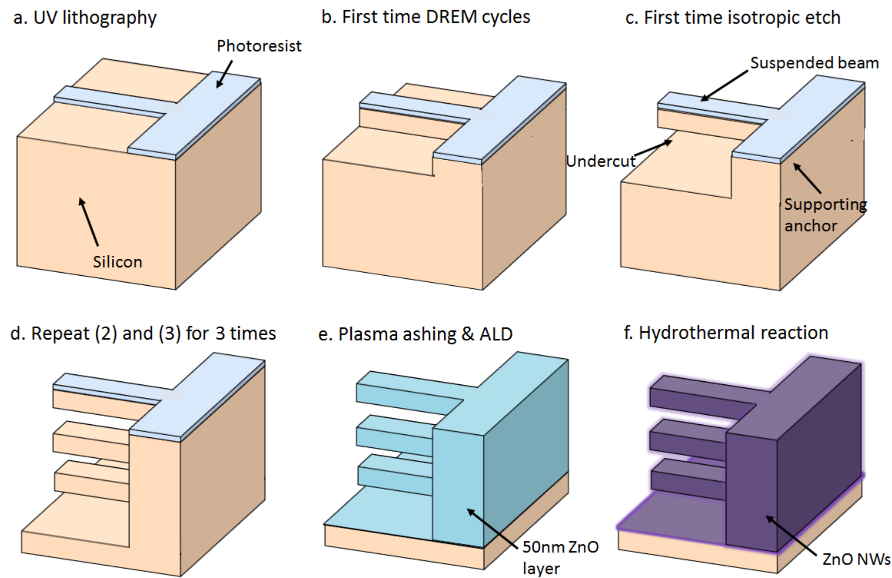


Figure 6.1. Process flow to fabricate ZnO NWs/3D silicon structures: (a) UV lithography; (b) first DREM cycle to create structures; (c) first isotropic etch to create suspended structures; (d) repeat DREM cycles followed by isotropic etch for 3 times; (e) plasma ashing to clean the polymers and deposit ZnO with ALD; (f) hydrothermal reaction to grow ZnO NWs.

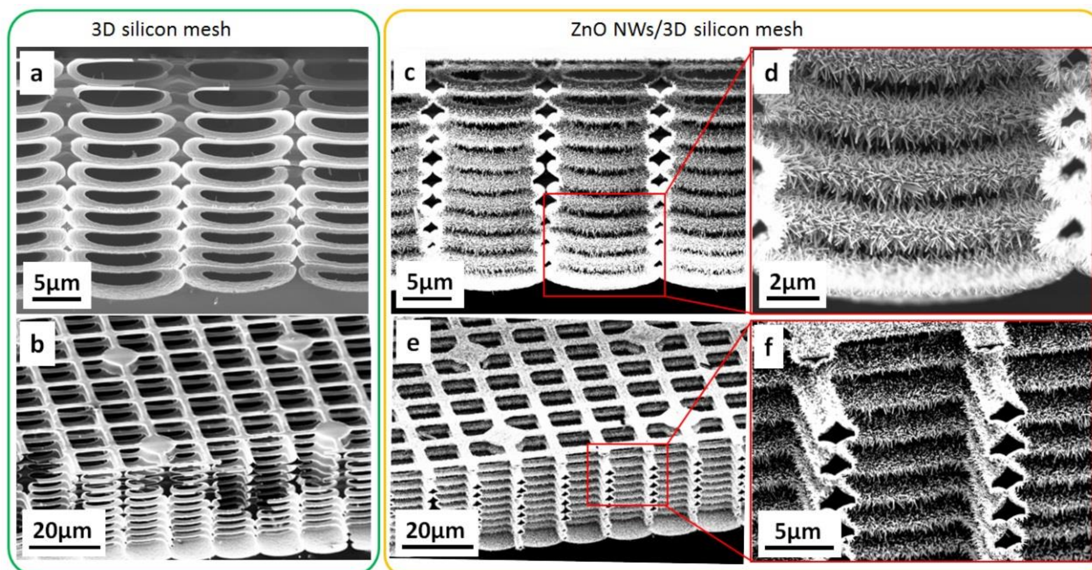


Figure 6.2. SEM images of 3D silicon micro-mesh structures (a-b); ZnO NWs/3D silicon structures in a cross section view (c-d) and a tilted view and (e-f).

The morphology of the highly ordered 3D silicon micro-mesh substrate and ZnO NWs/3D silicon structures were studied by SEM. **Figure 6.2a** and figure 6.2b show the fabricated 10 layered silicon micro-mesh structures. The length of the silicon microbeams is 10 μm and the width is 2 μm, anchored on large pillars with 10μm diameter. After depositing ZnO seed layer and hydrothermal reactions, ZnO NWs can grow conformally following the surface of the silicon structures as shown in figure 6.2c-f. The length of ZnO NWs is controlled by the hydrothermal reaction time. The reaction time was carefully controlled to avoid the overlap of ZnO NWs between each two layers of silicon structures.

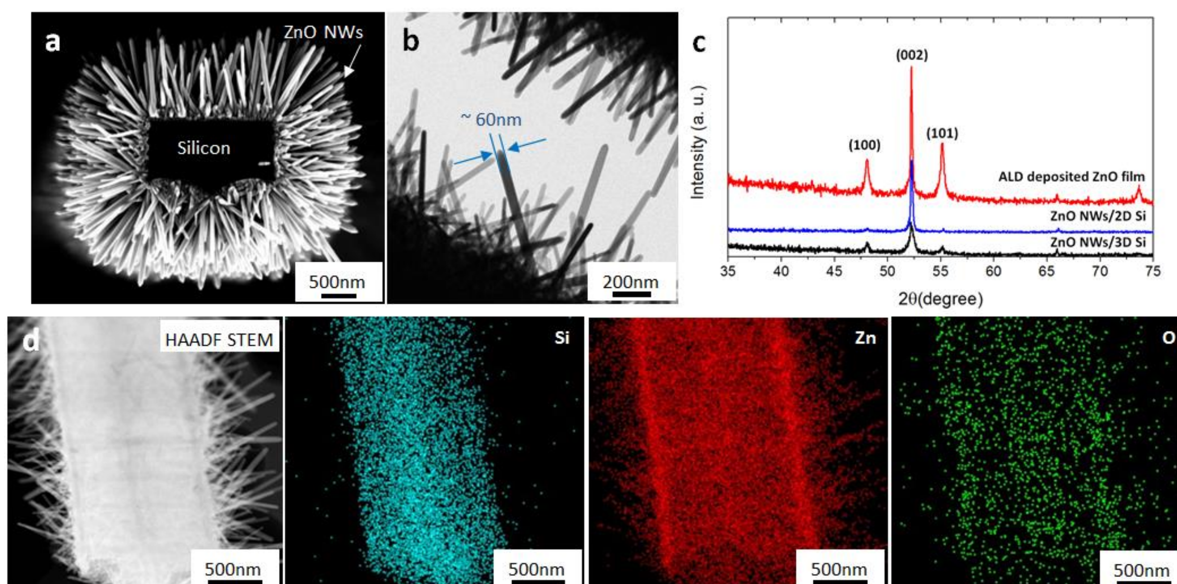


Figure 6.3. (a) SEM image of silicon microbeam covered with ZnO NWs; (b) TEM image of ZnO NWs; (c) XRD pattern of ZnO NWs/3D silicon structures; (d) HAADF-STEM image and element mapping of a silicon microbeam covered with ZnO NWs.

Figure 6.3a shows a magnified SEM image of a single silicon microbeam covered by ZnO NWs. It can be seen that high density of ZnO NWs are grown conformally on the suspended silicon microbeam. Transmission electron microscope (TEM) image of the sample is shown in figure 6.3b. The average length of the ZnO NWs is around 1 μm and the diameter is around 60 nm. Figure 6.3c shows the crystalline structures and phase of the sample, which were characterized by X-ray diffraction (XRD) using a Bruker Model D8 Advanced powder X-ray diffractometer (XRD) with Cr Ka irradiation (2.08 Å). All the diffraction peaks are well matched with the wurtzite ZnO according to the standard diffraction card (JCPDS number: 36-1451). A strong (002) diffraction peak is observed, indicating the growth of ZnO NWs follows the crystalline orientation of ALD ZnO thin film. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) was performed (Tecnai G2 T20, 200 keV, FEI), and elemental mapping (figure 6.3d) show the spatial distribution of Zn, O, and Si elements in the products.

6.1.3 Photocatalytic performance

When irradiating ZnO materials by light with photon energy larger than the band gap of ZnO, electron-hole pairs will be generated, and the unpaired holes react with water to form hydroxyl radicals, which is a strong oxidizers and can degrade organic dyes into simple organics and finally into carbon dioxide. [209] This process has been widely studied for the purpose of decontamination and purification of polluted water. Many strategies have been proposed to increase the photocatalytic degradation efficiency, e.g. by modifying the

morphology, [210] introducing dopants, [211] integrating ZnO with other substrates, [212] etc. Here we demonstrate that the ZnO NWs/3D silicon microstructures possess high photocatalytic activities towards the degradation of organic dye RhB.

For comparison, three different samples were prepared using different silicon substrates, including 3D silicon with large 2 μm beam size (ZnO NWs/3D Si-L), 3D silicon with smaller 1μm beam size (ZnO NWs/3D Si-S), and planar silicon (ZnO NWs/2D Si). The typical morphology of the three samples is shown in **figure 6.4**. The photocatalytic activity of the sample was evaluated by the degradation of rhodamine B (RhB, 1.0×10^{-5} M) aqueous solution under UV light (365 nm), using a 300 W Xe arc lamp (CEL-HXF 300) equipped with an UV cutoff filter as a light source. The samples were put into 100 mL of RhB solution. The aqueous solution was stirred in the dark for 1 h to reach a complete adsorption-desorption equilibrium. The reaction system was placed in a sealed black box with the top opened, and was maintained a distance of 15 cm from the light source. After initiation of the reaction by irradiation, a 5 mL sample of the suspension was taken out at regular intervals (~ 20 min). In order to measure the RhB degradation, UV-visible spectra of the solution was recorded by using UV-2550 UV-visible spectrophotometer (Shimadzu, Japan).

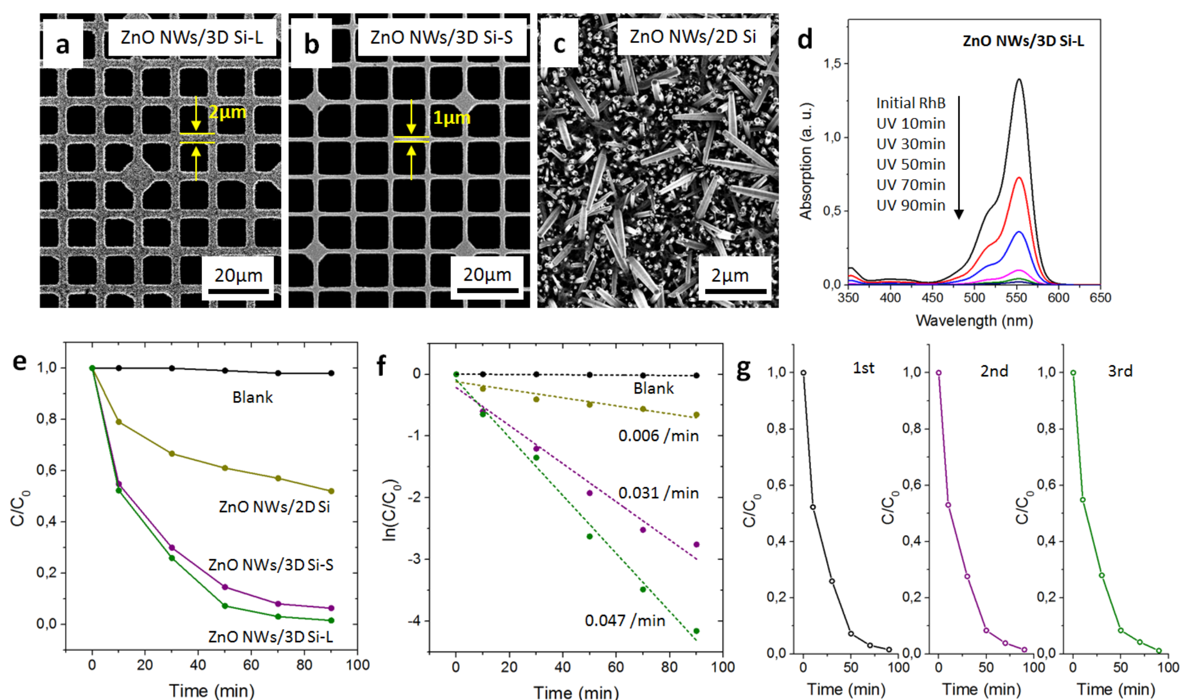


Figure 6.4. (a-c) SEM images (top view) of ZnO NWs/3D Si-L, ZnO NWs/3D Si-S, and ZnO NWs/2D Si; (d) Time dependent UV-visible spectra of RhB solutions with presence of ZnO NWs/3D Si-L; (e-f) Degradation curves for different photocatalysts under UV light illumination; (g) Time profile of the change in concentration of RhB for the first three cycles in the presence of ZnO NWs/3D Si-L.

Figure 6.4d shows a series of UV-vis absorption spectra of the aqueous solution of RhB, when ZnO NWs/3D Si-L was used as the photocatalyst exposed to UV light for different durations of time. The characteristic absorption peak of RhB dye centered at 554 nm decreases rapidly with increasing exposure time. Figure 6.3e shows the comparison of the photocatalytic activity of the three samples under the same experimental conditions. The blank experiment without the addition of photocatalyst shows almost no degradation of RhB under UV light illumination. While with the presence of different photocatalysts, the degradation of RhB is observed. The degradation of RhB follows the order of ZnO NWs/3D

Si-L > ZnO NWs/3D Si-S > ZnO NWs/2D Si. Figure 6.3f shows the linear relationship between $ln\frac{C_t}{C_0}$ and illumination time t, indicating the photocatalytic reaction follows first-order kinetics $ln\frac{C_t}{C_0} = -kt$, here C_0 and C_t are the initial concentration and the concentration at reaction time t of the RhB solution, respectively, and the slope k is the apparent reaction rate. The calculated rate constant for ZnO NWs/3D Si-L is 0.047 min^{-1}, which is 1.5 times faster than ZnO NWs/3D Si-S (0.031 min^{-1}), and 8 times faster than ZnO NWs/2D Si (0.006 min^{-1}). The results confirm that the ZnO NWs/3D Si-L sample is superior in degrading RhB dyes. The enhancement of photodegradation efficiency is attributed to the significant increase of ZnO NWs density, thus more photocatalytic reactions can take place in the same unit area. To test the stability of the photocatalytic performance, ZnO NWs/3D Si-L was rinsed after each photocatalytic process and a new process was repeated right afterwards, and the same degradation rate could be observed for 3 processes as shown in Figure 3g. This demonstrates the good reusability of ZnO NWs/3D Si microstructures for photocatalytic applications.

6.1.4 Photocurrent generation

The semiconductor nature of ZnO material makes it a favorable material for photosensitive devices, e.g. photovoltaics and solar cells. [213] In order to improve the efficiency of the free charge migration, conductive substrates (such as graphene) are used to form into heterostructures with ZnO. [214] This strategy, however, increases the economic cost for the fabrication process, thus hinders the large scale applications. Here we demonstrate that photocurrent response can be enhanced by integrating ZnO NWs with the 3D silicon micro-mesh structures.

Measurement was performed with a standard three-electrode system , with Pt wire as counter electrode, saturated calomel electrode (SCE) as reference electrode, and ZnO/3D Si samples as working electrodes. Aqueous solution of Na_2SO_4 (0.5 M, pH = 7.0) was prepared as the electrolyte. The working electrodes with half area of the sample were dipped into the electrolyte, and irradiated from the front side under a UV light (λ ~ 365 nm). The distance from the light source to sample was around 10 cm.

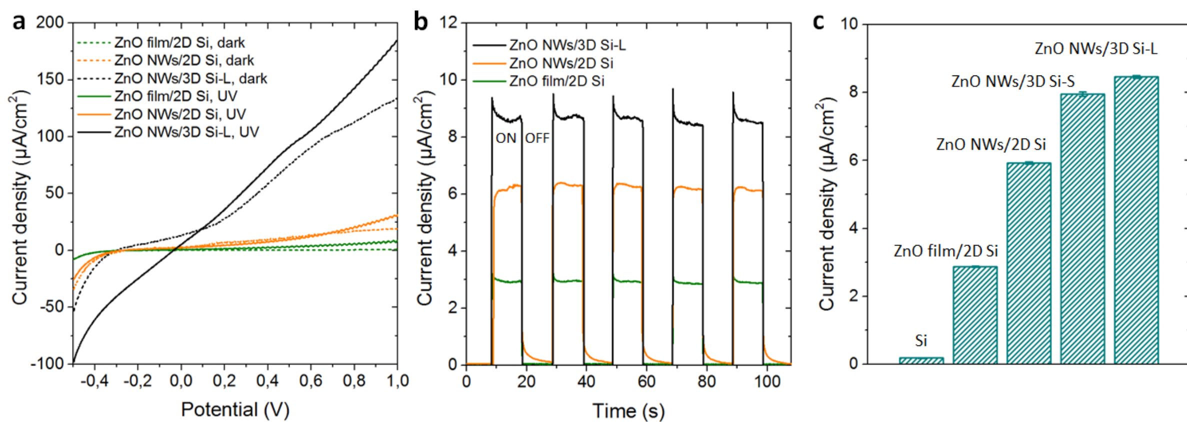


Figure 6.5. (a) Line sweep voltammograms; (b) photocurrent responses with UV light five on/off cycles at a bias of 0.5 V vs. SCE; (c) average photocurrents for different samples at a bias of 0.5 V vs. SCE.

The photocurrent response performances of ZnO NWs/3D Si -L, ZnO NWs/2D Si, and ZnO film/2D Si were investigated by running the line sweep voltammograms (LSV) with and without UV light irradiation (λ ~ 365 nm) under ambient conditions. The bias potential was ranging from −0.5 to +1.0 V vs. SCE. As shown in **figure 6.5a**, ZnO NWs/2D Si and

ZnO film/2D Si show negligible current in the dark. When illuminated with UV light, the two samples exhibit non-zero current densities. For ZnO NWs/3D Si sample, it is interesting to find that an obvious current is generated even without UV light illumination. A prominent photocurrent response can be observed with the UV irradiation. Specifically, a current density of ~0.18 mA/cm^2 can be achieved at a bias of 1.0 V, which is around one magnitude larger than the photocurrent density for ZnO NWs/2D Si and ZnO film/2D Si, respectively. This photocurrent enhancement is related to the high density of ZnO NWs and more free charge carriers generated in a unit area. The amperometric $I\!-\!t$ curves with the chopped illumination at the bias potential of 0.5 V vs. SCE were measured for the three samples as shown in Figure 6.5b. A photoresponse with a stable photocurrent for all the samples was observed. The current returned to the original values immediately as the light was switched off. Figure 6.5c compares the photocurrent density at the bias of 0.5 V vs. SCE for the different samples. The results of bare silicon and ZnO NWs/3D Si (beam size of 1 µm) are also shown for comparison. It can be seen that ZnO NWs/3D Si-L (beam size of 2 µm) gives a higher current density compared with ZnO NWs/3D Si-S (beam size of 1 µm), both are significantly higher than ZnO NWs/2D Si, ZnO film/2D Si, and bare Si. The improvement of photocurrent response demonstrates the ZnO NWs/3D silicon micro-mesh as efficient alternative structures for photoelectric applications. It should be mentioned that by increasing the number of isolated layers, the photocatalytic and photocurrent performance could also be improved, however, this is limited by the fabrication process, thus a maximum number of 15 layers can be achieved and the highest photodegradation rate and photocurrent density are limited.

It should be mentioned that the enhancement of both photocatalytic performance and photocurrent generation are closely related to the increased ZnO NWs densities. The ZnO NWs density dependences of photodegradation rate and photocurrent densities are plotted in **figure 6.6** below.

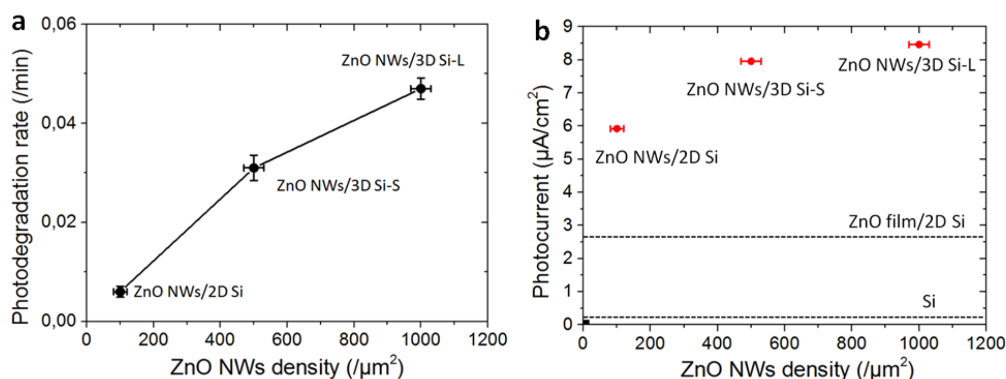


Figure 6.6. Relation between ZnO NWs density and (a) Photodegradation rate; (b) Photocurrent densities.

6.1.5 Material conversion for hybrid heterostructures

ZnO is a versatile material that can be conveniently transformed into other functional materials, e.g. ZnS and ZIF-8 structures, which show a broader range of applications. By using a simple hydrothermal or solvothermal reaction, the present ZnO NWs/3D silicon microstructures can be converted into ZnS NWs/3D silicon and ZnO@ZIF-8 NWs/3D silicon microstructures, while the original 3D morphology can still be preserved.

ZnS is a typical semiconductor with a bandgap of 3.67 eV, and has been studied for photoelectric, [215] and photovoltaics [216] applications. In the project, ZnO/Si samples were put into a Teflon lined autoclave (100 mL capacity) containing 50mL of thioacetamide (TAA, 0.2M, Sigma-Aldrich), and then kept at 120 °C for 10 hours, a hydrothermal growth process can then happen and ZnO NWs can be converted to ZnS nanostructures, during which a nanoscale Kirkendall effect happens inducing the formation of hollow structures. [217, 218] The TAA amount was estimated to be sufficient for a maximum conversion of ZnO nanowires. In **figure 6.7a**, we can see that the structures remain intact after hydrothermal reactions, with "tubular" nanostructures covering the whole 3D substrate. From an enlarged view, the tube-like morphology can be distinguished (see the yellow square area in figure 6.7b). The rough surface of the ZnS NWs indicates the converted sample is polycrystalline (figure 6.7c), which is further confirmed by the selected area electron diffraction (SAED) pattern (figure 6.7d inset). The diffraction rings can be identified and indexed to (111), (311) and (220) planes of zinc-blend ZnS. Figure 6.7d shows a typical high-resolution TEM (HRTEM) image, and the lattice spacing was calculated to be 0.32 nm, which corresponds to the (111) crystalline plane of a cubic ZnS crystal. HAADF-STEM image and elemental mapping results show a uniform distribution of Zn and S over the Si microbeam. The observation of some weak O signals suggests the coexistence of ZnO residues.

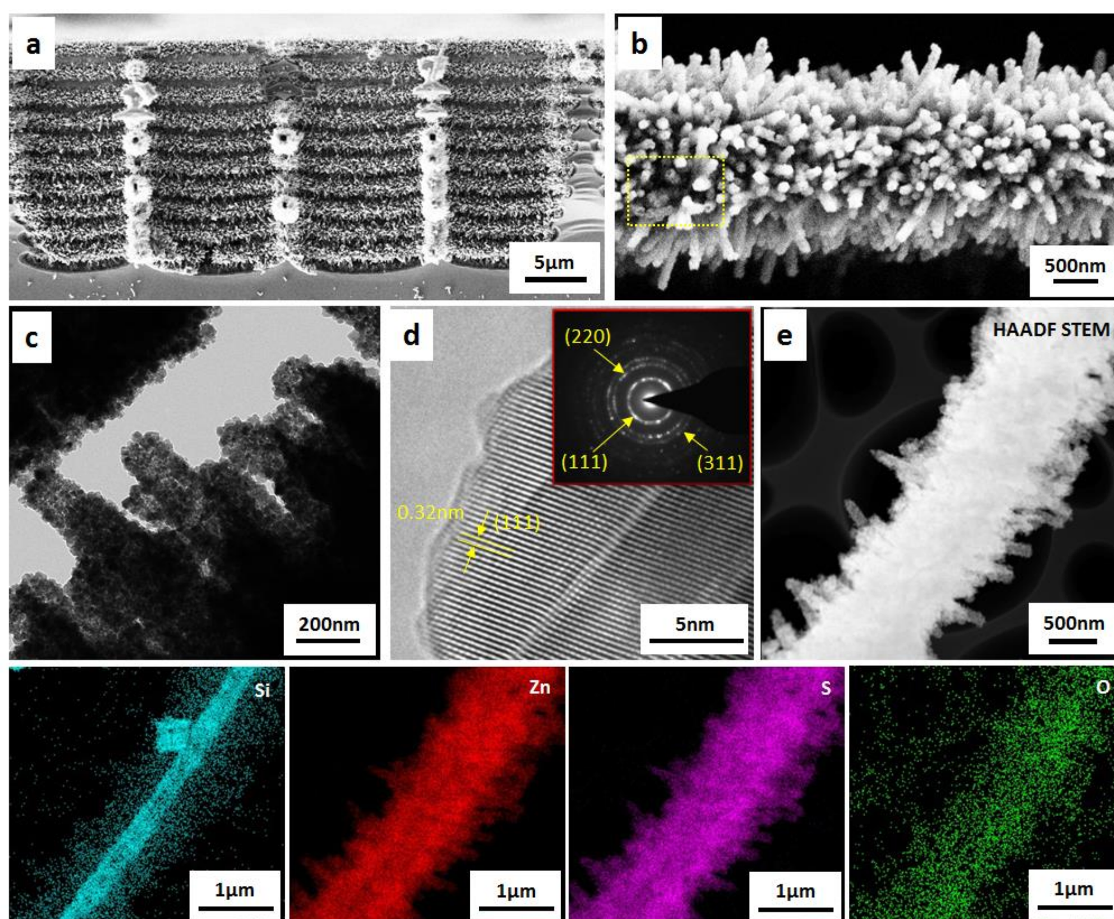


Figure 6.7. (a, b) SEM, (c) TEM, and (d) HRTEM of ZnS NWs/3D silicon microstructures. The inset shows the SAED pattern. (e) HAADF-STEM images and corresponding EDX element mapping.

The other converted material is ZIF-8, which has been studied earlier in chapter 2. Here, a solvothermal reaction was employed to convert the ZnO NWs into ZIF-8 structures on the 3D Si substrate (the growth methods and parameters are the same compared with chapter

2). **Figure 6.8a-c** shows the SEM images of the transformed structures. It can be seen that ZIF-8 crystals cover the 3D silicon structures in a uniform manner. An enlarged view implies that there are still underlying ZnO NWs remaining on silicon substrates, and the ZIF-8 crystals filled the gaps between ZnO NWs. This is expected as each Zn atom from the the ZnO gives a 102 times larger ZIF-8 unit cell (4913 $Å^3$) than the ZnO unit cell (48 $Å^3$). HAADF-STEM (figure 6.8d) and TEM images (figure 6.8e-f) also show the porous morphology of ZIF-8 crystals, and residual ZnO NWs exist in the core of ZIF NWs, thus forming ZnO@ZIF-8 NWs/3D silicon microstructures. EDX element mapping on a section of ZnO@ZIF-8 NWs/3D silicon microstructures confirms the existence of N, O and C elements and verifies the formation of ZIF-8 structures on the surface of ZnO NWs (figure 6.8g). Compared with the traditional powder-like ZIF-8 crystals, the obtained ZIF-8 NWs /3D silicon microstructures can serve as a reusable and mechanically robust substrate, and an improved performance is expected for applications as catalysis and gas adsorption.

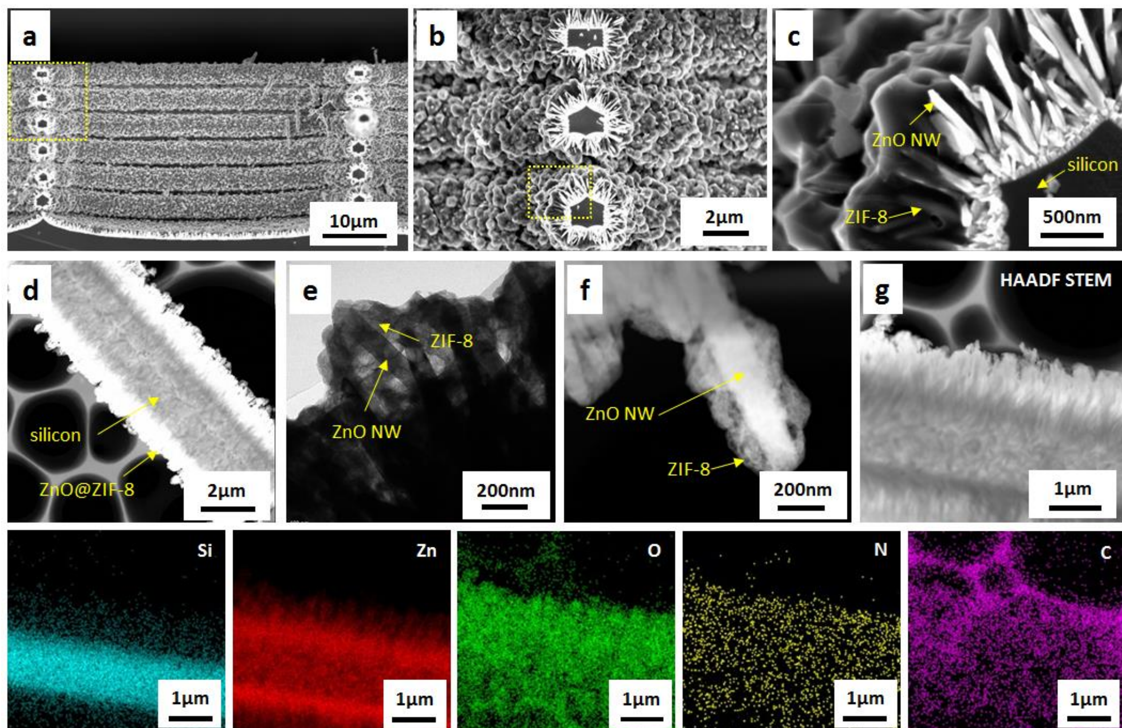


Figure 6.8. (a-c) SEM, (d) HAADF-STEM, and (e, f) TEM images of ZnO@ZIF-8 NWs/3D silicon microstructures; (g) HAADF STEM image and corresponding EDX element mapping results of the ZnO@ZIF-8 NWs/3D silicon microstructures.

In summary, DREM process can be used to fabricate a highly ordered 3D silicon micro-mesh structure, which is a robust substrate to significantly increase the surface area of different materials. By integrating ZnO NWs with the 3D silicon substrates, both photocatalytic and photocurrent generation performances were improved in a large scale compared with 2D plane substrate grown ZnO NWs. The fabricated ZnO NWs can also be converted to other functional materials including ZnS and ZIF-8, while the ordered structure and morphology remain intact, showing the flexibility and potential of other applications. The whole fabrication process is easy to control and less time consuming compared with traditional multiple-time growth method. It is also promising to integrate other low dimensional materials onto the 3D silicon substrates with MEMS designs, allowing for a range of advanced applications and on-chip applications.

6.2 3D SILICON PHOTONIC CRYSTAL MEMBRANES

In this section we will demonstrate another application with 3D silicon structures fabricated with a modified DREM process. We will show how 3D photonic crystals (3D PhCs) can be fabricated with much less costs compared with previous studies. The etch processes can be easily programmed so that planar defects can be embedded, enabling practical applications in solvent sensing and optical filters.

6.2.1 Background introduction

3D PhCs are structures with periodic modulations of dielectric constants in three dimensions, possess a modified dispersion relation and a photonic band gap (PBG). This results in a range of wavelength, where electromagnetic propagating modes are forbidden, and is an optical analog to the electronic band gap structures of atomic lattices. By incorporating defects with 3D PhCs, a localized optical resonance mode can be realized in the defect region, and more advanced functionalities can be demonstrated. PhCs with lower dimensions have already been widely used in various fields, such as optical waveguides and sensors. However, 3D PhCs, which enable light manipulations in full three spatial dimensions, are still faced with fabrication challenges. A lot of efforts have been invested in previous studies, and various fabrication methods have been proposed, most of which are limited by fabrication complexity and cost. The classical 3D PhC configurations, such as woodpile structures [219, 220] and inverse opal structures [221, 222] enable a large band gap ratio (band gap width over mid gap position) and flexibilities to manipulate photons with embedded cavities. [223-225] However, these bottom-up strategies require multiple complex fabrication steps and are not suitable for large scale production. Some top-down methods have been proposed using plasma etching [226] or modulated electrochemical etching. [227] However, there is still a need for feasible fabrication methods for large scale 3D PhCs and embedded cavities.

The idea to fabricate large scale 3D PhCs simply by using the plasma etching was first proposed by S. Venkataraman et. al. [228] A similar study was later reported by A. Vlad et. al., both of them made use of the scallops generated during the Bosch and can give a ripple-like sidewall profile to create the necessary modulation of the refractive index. Thus, a 2D pattern from a traditional lithography can be transferred into 3D PhCs in a top-down manner. This method has the advantage of high fabrication efficiency and low cost. However, there are some technical limitations. Firstly, the size and the shape of the scallops are difficult to control precisely, since the Bosch process is limited intrinsically by IAD and effects such as ARDE, which will influence not only the etch rate but also the sidewall profile along the etch depth in the silicon, generating nonuniformities affecting the periodicity of the structure. Secondly, the simple cubic lattice type of 3D PhCs have a relatively small band gap ratio of less than 10%, [229] thus geometric distortions or nonuniformity of lattices can close the bandgap in certain directions of Brillouin zone, and the stop band can only exhibit in certain angles of incidence (termed as pseudo photonic band gaps). Thirdly, to achieve a complete band gap that is incident angle independent with a high attenuation rat of around 20 dB in mid gap position, a large contrast of refractive index is necessary, thus a strong structural shape modulation of the scallops is necessary, which will at the same time reduces the mechanical stability of the structures. All of the disadvantages mentioned above will limit the capabilities and flexibilities of the fabricated structures. Besides, the total number of repeated layers will be limited and the

precise introduction of defects will be difficult, ultimately limiting the functionalities of the fabricated structures.

In this study DREM process is used to create the 3D periodic structures. Compared with the scallops created directly by Bosch process, a large refractive index contrast can be realized due to the strongly modulated etch profile. The fabricated 3D PhCs also show excellent mechanical properties, which enable the structures to be lifted of the substrate and be transferred as a membrane onto other substrates. Moreover, by infiltrating the air voids in 3D PhC membranes with polymer, a self-supported flexible hybrid film can be fabricated, with 3D silicon structure embedded, while the features of band gap still preserved. To enable optical functionalities of the fabricated 3D PhCs, planar defects are introduced directly during the modified etch process, which results in a resonance mode coupled to PBG at a wavelength of around 1100 nm, with a linewidth of around 30 nm. The fabricated 3D PhC membrane with embedded planar cavity can be used as a sensor for organic solvents with a good sensitivity of around 400 nm RIU^{-1} (RIU, refractive index unit). By transferring the 3D PhC membranes onto n-doped black silicon, the near infrared photoluminescence of the black silicon [230] could be filtered efficiently with an attenuation ratio of around 20 dB.

6.2.2 Fabrication and characterization

DUV stepper lithography has been used to define the patterns on silicon wafers, 65 nm thick BARC layer and 360 nm thick DUV resist were coated on the substrate. Patterns were exposed with a DUV stepper system (FPA-3000EX4, Canon) with dose 21 mJ/cm^2 and focus depth 0.17 µm. The DREM process was performed with DRIE Pegasus system (SPTS). The process flow is shown in **figure 6.9**. The diameter of patterned hole structures is around 250 nm. Each scallop during the DREM process has the size of around 20 nm, which is much smaller than the scallop sizes from the traditional Bosch process, which is typically around a few hundred nanometers. Isotropic etch was performed with SF_6 gas without platen power to maximize the isotropicity, thus generating a large shape modulation. Since the structures are strengthened by the anisotropic part of the etch profile, the sequences can be repeat for at least 8 times (limited by the thickness of DUV resist), and the fabricated 3D periodic structures can be released from silicon substrate by a final isotropic etch step with a longer etch time (figure 6.9(4)).

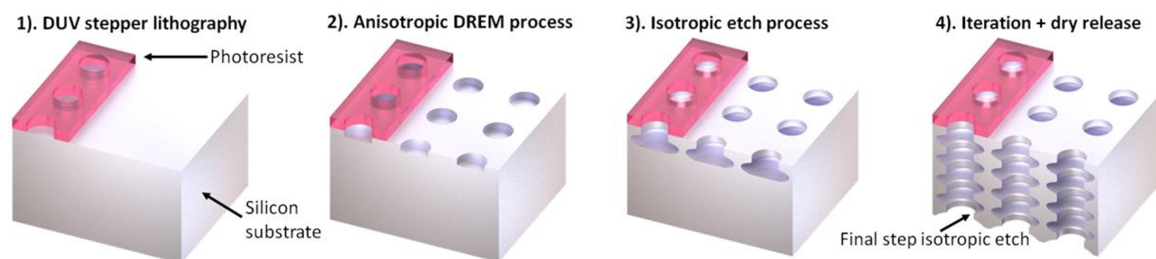


Figure 6.9. Process flow to create 3D PhC membranes with modified DREM process.

The fabrication process is CMOS compatible and based on the standard fabrication techniques. The etch process takes only a few minutes and the sequence and timing is easy to control be programming the plasma etch tool, so that the period and the size of void can be tuned in a reasonable wide range. The total thickness of the fabricated membranes is around 2 µm, and area can be several square millimeters. In **figure 6.10a4**, we can see that the fabricated 3D PhCs can be peeled off by a tweezer and transferred to a piece of quartz

wafer. The fabricated 3D PhC membranes can also be infiltrated with polymer: firstly, Efiron PC-404 (Lucantix, South Korean) was applied onto the membranes (with a silicon wafer treated with an anti stiction layer of 1H,1H,2H,2H-Perfluorodecyltrichlorosilane as a substrate), then the sample was cured under UV lamp for 5 min (13.5 mW/cm^2 at 365 nm), finally, the hardened resist was released together with 3D PhC membranes from the silicon wafer (as shown in figure 6.10a5). The silicon structures could then be supported by the soft polymer, and a good flexibility can be achieved resulting in a polymer membrane integrated with a 3D PhCs membrane (figure 16.10a6), which can be promising for flexible photonic devices. SEM images show the 3D PhCs fabricated on the silicon substrate before final release (figure 6.10b) and in the membrane form (figure 6.10c), it can be seen that the structure of membrane remains intact after peeling off from silicon substrate.

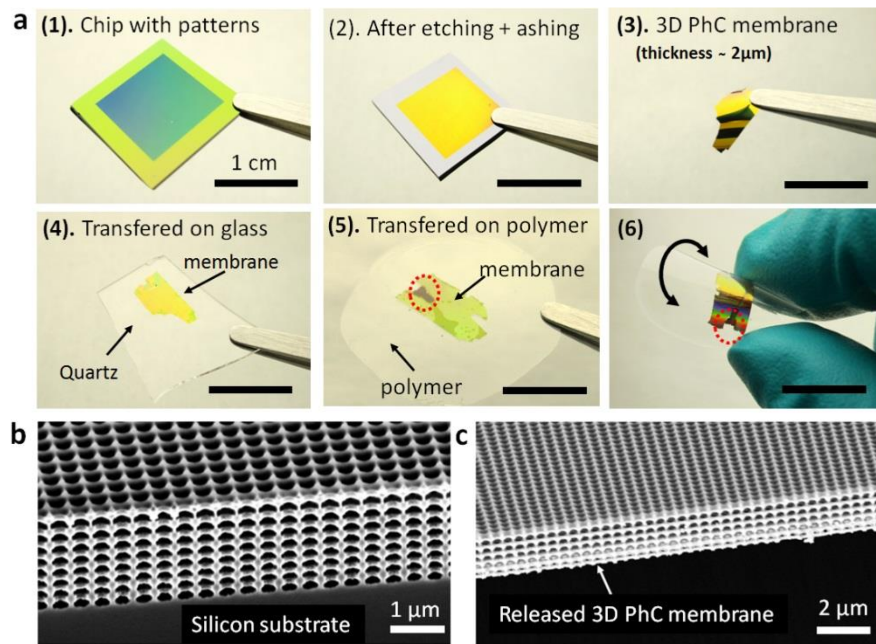


Figure 6.10. Photographic illustration of the process flow: (a1) Chips with patterns defined by DUV stepper lithography; (a2) Chips after modified DREM etch process and plasma ashing to remove the DUV resist; (a3) Freestanding 3D PhC membranes peeled off by tweezer; (a4) Membranes transferred on a piece of quartz; (a5) Membranes infiltrated and transferred on a piece of flexible polymer plate; (a6) Bendable 3D PhC membrane infiltrated with polymer. (b) SEM image of 3D PhCs with 8 periods before last step of dry release; (d) SEM image of freestanding 3D PhC membranes with 6 periods after dry release.

There are several technical challenges that we had to address during the fabrication process. The first is that the silicon-to-air volume ratio during the isotropic etch step can reduce to less than 10%, thus a proper isotropic etch time should be chosen, otherwise the layers can delaminate from each other (as shown in **figure 6.11a-c**). Another effect that needs to be considered is the ARDE for hole-like structures, which can cause a decreased etch rate when the aspect ratio increases. In the fabrication process, both the etch step during DREM process and the isotropic etch step are ramped along with the process time (which has been introduced earlier in chapter 5), so the possible shape nonuniformity is compensated and precise periodicity can be achieved (a comparison of etched profiles with and without parameter ramping is shown in figure 6.11d).

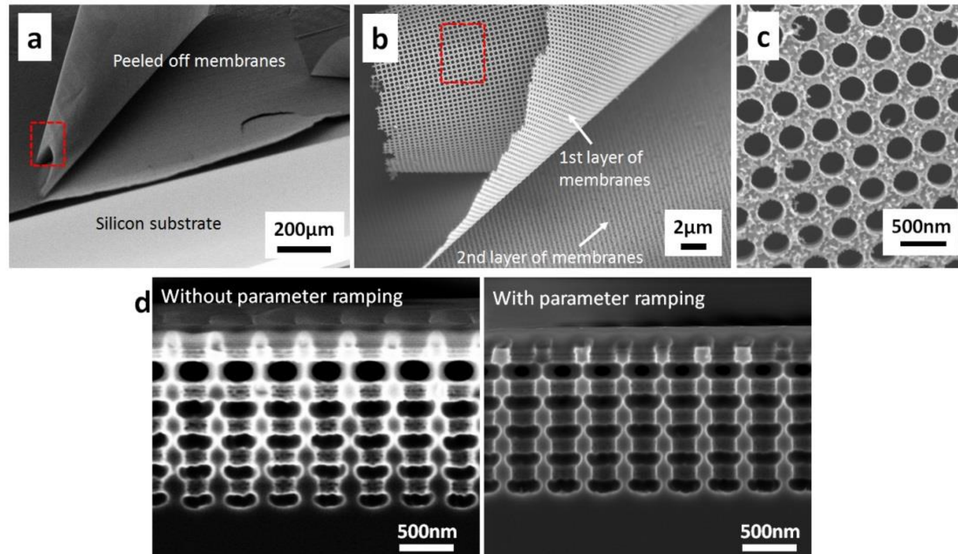


Figure 6.11. Etching defects for fabricating 3D PhC membranes: (a-c) Delaminated single layer of 3D PhC membranes, with the thickness of around 200 nm; (d) ARDE and its compensation with a parameter ramping procedure.

6.2.3 Characterization of optical properties

The fabricated 3D PhCs membranes have a well-defined SC structure as shown in **figure 6.12a**, in which a unit cell is also labeled. The width of the cubic cell is 400 nm, and the diameter d of the lithography patterns is around 250 nm. A void with diameter larger than 400 nm is created during the isotropic etch step, such that each unit cell is connected with its neighbouring cells, resulting in a strong shape modulation. Based on the volume proportion of silicon in different layers, a large refractive index contrast of around 1.53 is estimated along the direction of the holes. In some cases silicon single crystalline structures could be damaged during the plasma etching process due to UV irradiations or ion bombardments, thus the refractive index, especially the absorption coefficient, could change. To rule out this effect, X-ray diffraction (XRD) measurements were performed for both a silicon dummy wafer and a 3D PhC membrane on top of glass, the spectra are shown in figure 6.12b. We can clearly see the sharp diffraction peak of (400) silicon crystalline plane at around 69.24˚, which suggest a good single crystalline quality after plasma etching process (the peak with lower intensity at around 61˚ corresponds to the Cu Kβ radiation source). The XRD measurement was performed with a high-resolution X-ray diffractometer system (SmartLab, Rigaku), which is equipped with a Cu Kα radiation source (1.54 Å).

The band diagram was calculated numerically with FDTD method, assuming the 3D PhC membrane has SC structures with vacuum as substrate (figure 6.12c). A complete band gap with a gap ratio of around 8% can be observed between the 5th and 6th band. The reflection spectrum of fabricated 3D PhC membranes on glass substrate was measured at incident angles of 7.5˚, 15˚ and 30˚ (as shown in figure 6.12d). A strong reflection peak at λ = 1100 nm is present, which fits well with the band edge position as shown in the band diagram. The gap to mid gap ratio is estimated to be $\Delta\lambda/\ \lambda$ = 18%. The system used for reflection measurement was a goniometer stage (Gon360 from Instrument systems) and a broadband optical spectrometer (Spectro320 from Instrument Systems) with a wavelength range from 400 nm to 1600nm. Reflectance measurement of a silver coated mirror was used as a reference. A broadband light from a Xenon lamp (HPX2000 from Ocean Optics) is used as a source for the reflectance measurements.

Reflection and transmission spectrum were also measured with an ellipsometer (Vase, J.A. Woollam Co., Inc.) as shown in figure 6.12e, displaying a low transmittance in the PBG region. The reflectance was measured with 45˚ incident angle, while the transmittance was measured with 0˚ incident angle, the spot size was 1 mm by 1 mm, and the wavelength ranges from 200 nm to 1600 nm, the reference sample was a silicon wafer deposited with 25 nm SiO_2.

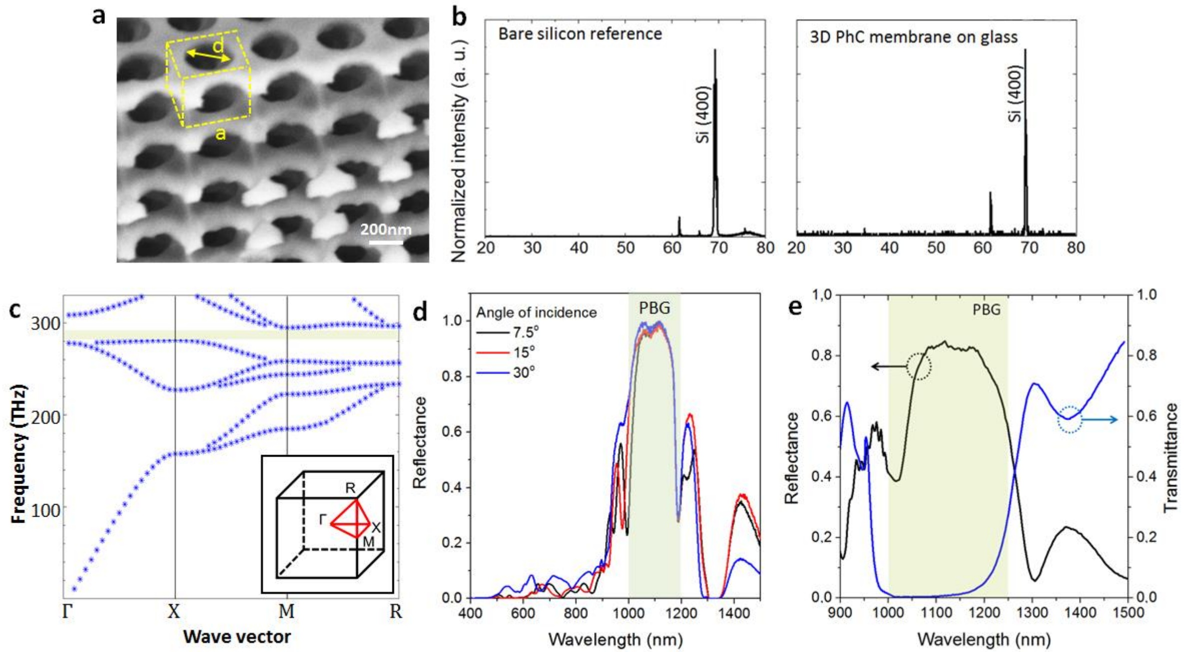


Figure 6.12. (a) SEM image showing the SC structure of fabricated 3D PhC membrane; (b) XRD measurements of a bare silicon wafer and 3D PhC membranes on top of glass substrate; (c) Caculated band diagram showing the existence of a complete band gap; (d) Reflection spectrum of 3D PhC membranes on glass measured with three different angles of incidence using goniometer stage and an optical spectrometer; (d) reflection and transmission spectrum of 3D PhC membranes on glass measured by ellipsometry (incident angle of 45 for reflection measurement).

Since the fabricated 3D PhC membranes have the advantage of large surface area, the reflectance spectrum can be easily measured by a compact spectroscopic ellipsometer without focused probes. To proof the fabricated 3D PhC membranes is a complete 3D PhCs, the reflectance spectrum was measured with varying incident angles θ in a large range from 45˚ to 75˚, and the incoming angle φ as 0˚ and 45˚. To demonstrate both sides of the membranes have the same optical properties, we also measured the reflection spectrum from both top side and bottom side of the 3D PhCs membranes on top of glass, as shown in **figure 6.13a**. The measured spectrum agrees with the measurement made using a standard spectrometer in figure 6.12d, showing a significant reflectance peak in the band gap region. The reflection spectrums along the (110) plane for 3D PhC membranes on different substrates are compared in figure 6.13b. The reflection maxima and the band edge position coincide well with each other for 3D PhC membranes on glass and on silicon, while for the membranes infiltrated with a low refractive index polymer (Efiron, refractive index n = 1.404 at λ = 852nm after curing by UV light) the band edge was redshifted by around 80 nm, which is expected., Since the void in the structures is replaced by polymer with a higher refractive index, the mean refractive index will increase and position of band edge will shift to a lower frequency range. Besides, the SC structures might be distorted due to the strain introduced by polymer infiltration, thus the reflection spectrum might be altered compared

with a free standing membrane on glass or silicon. When increasing the number of periods for 3D PhCs from 4 layers to 8 layers, we could clearly see the development of the PBG, as the reflection in mid gap position increases by around 60%.

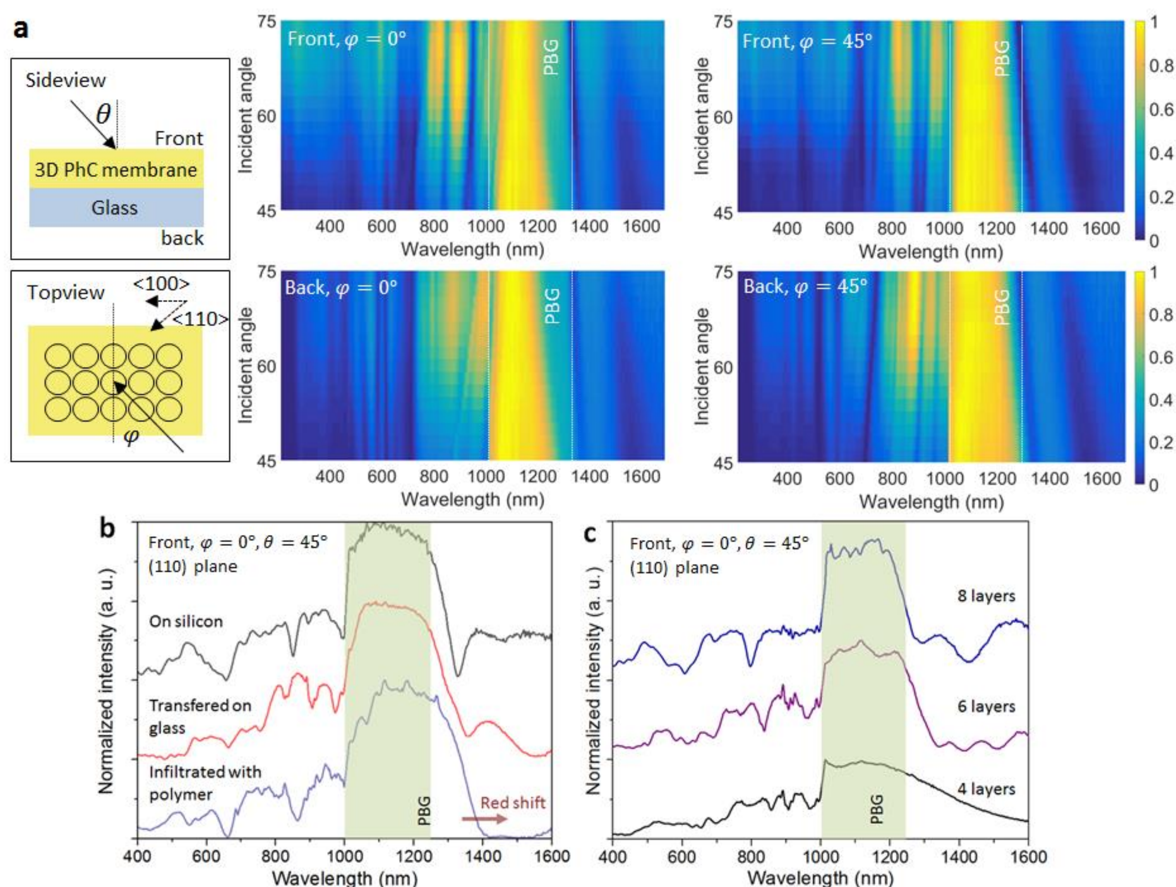


Figure 6.13. Reflection spectra measured by ellipsometry. (a) a schematic view of the 3D PhC membranes on glass substrate, and measured reflection spectrum from both the front and back side of the sample with different incident angles, which show a clear bandgap region at around 1100nm; (b) reflection spectrums of 3D PhC membrane on different kinds substrates: silicon, glass and polymer; (c) reflection spectrums with different numbers of repeating layers of 3D PhC membranes on glass substrate.

Since the fabricated 3D PhC membranes could be easily infiltrated by polymer, the integrated 3D PhC membranes on the polymer possess mechanical flexibility and can be bent in a large scale without collapse, which implies the potential for flexible and wearable photonic devices. It should also be noticed that shear strain can be introduced in 3D PhC structures when the polymer membrane is bended, thus the SC geometry will be distorted as shown in **figure 6.14a**, where the shear strain can be as large as 0.48. The band structures will also be modified, thus realizing tunable and flexible photonic devices that are biocompatible, [231, 232] which will be interesting to investigate in the future study. Apart from polymers, some high refractive index materials could also be infiltrated and coated conformally on the 3D PhC membranes by ALD. Figure 6.14b is a 3D PhC membrane coated with TiO_2 on a glass substrate. EDX element mapping shows a uniform coating of TiO_2 on the membrane. When the thickness of TiO_2 increases from 10 nm to 15 nm, the band edge is red shifted due to the increased average refractive index, while the reflection intensity decreases significantly, which is supposed to be caused by the increased volume ratio of high refractive index materials, thus the complete PBG closes. However, it should be mentioned that in order to achieve a better optical performance of fabricated PhCs, it is

an efficient method to coat 3D PhC structures with materials with better thermal or optical properties, [233] or creating inverse structures and replicas with other materials. [234, 235] By carefully choosing the dimensions of the 3D PhC membranes, it should be possible to make inverse 3D PhCs with other materials.

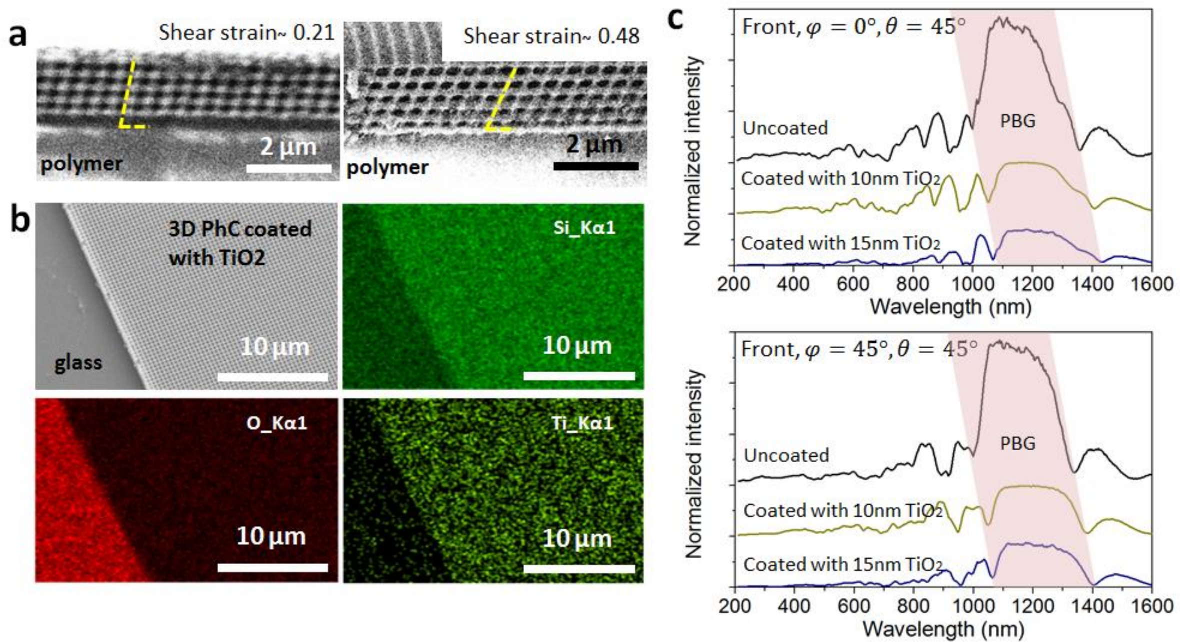


Figure 6.14. a) 3D PhC membranes infiltrated with polymer under shear stress (scale bare 2 μm); (b) SEM image and EDX mapping of 3D PhC membrane coated with 15 nm TiO2 by ALD (scale bars 10 μm); (c) reflection spectra of 3D PhC membranes coated with different thickness of TiO2, with glass as substrate.

6.2.4 Applications with embedded planar cavities

To enable the functionalities of 3D PhCs for the purpose of light manipulation, defects are introduced into the structures, such as planar cavities, single point defect, or even complex 3D waveguides which can guide the light in three dimensions. [236] Planar defects have been studied mostly for different configurations of 3D PhC. [237 -239] Here we will show how a planar cavity could be introduced into 3D PhC membranes for different applications. **Figure 6.15a** is a free standing 3D PhC membrane with 6 periods; the cross section view shows a good size uniformity for 6 layers. Figure 6.15b is a free standing 3D PhC membrane with 7 layers, with a defect layer embedded in the middle with a thickness of around 300 nm. The planar defect was introduced simply by increasing the number of DREM cycles for the fourth layer, while the other layers remain the same. The reflection spectrums for 3D PhC membranes on glass substrate with and without embedded planar defects are shown in **figure 6.16a** and figure 6.16d. Since photonic states are introduced in the stop band by the planar defects, a resonance could be clearly seen in the PBG region, which should otherwise be free from photon propagations. The resonance has a linewidth of around 30 nm, and can be observed with incident angles from 45˚ to 75˚ from both the top side and the bottom side of the membranes. It should be addressed that there are several resonance dips near the bandgap position on the spectra, this is possibly due to the high volume ratio of silicon dielectric defect, which can host multiple localized resonance modes, [240, 241] while for silica planar defects or air defects, only a single resonance dip can be observed which is generated by the basic dipole resonance state or monopole state. To further increase the quality factor of the planar cavity resonance mode, the effective cavity length should be increased, e.g. by increasing the number of repeated defect-free layers to achieve a better

confinement of resonance states in the cavity region. A thermal annealing process should also be considered to reduce the roughness on structure surfaces, thus less scattering loss is generated and the quality factor can be increased for a sharper resonance dip.

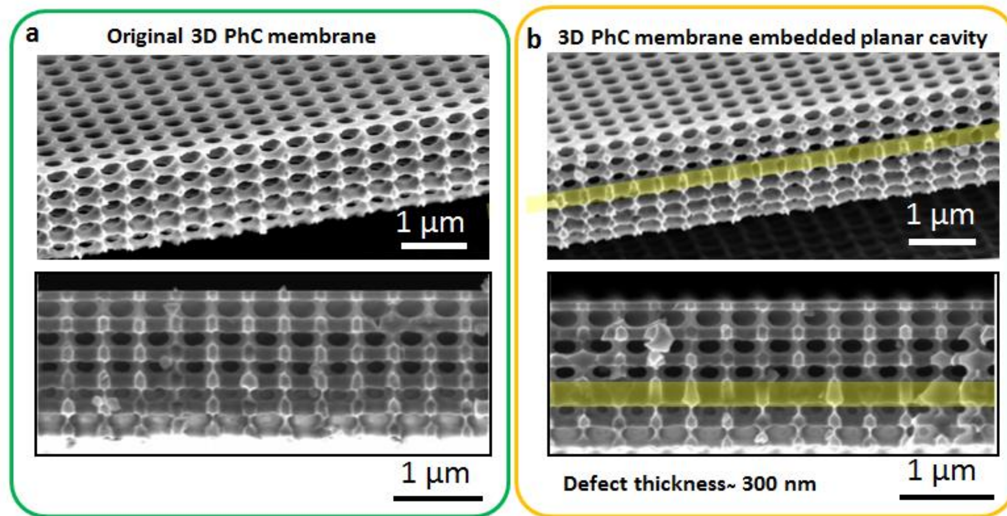


Figure 6.15. SEM images of 3D PhC membranes with and without a planar defect.

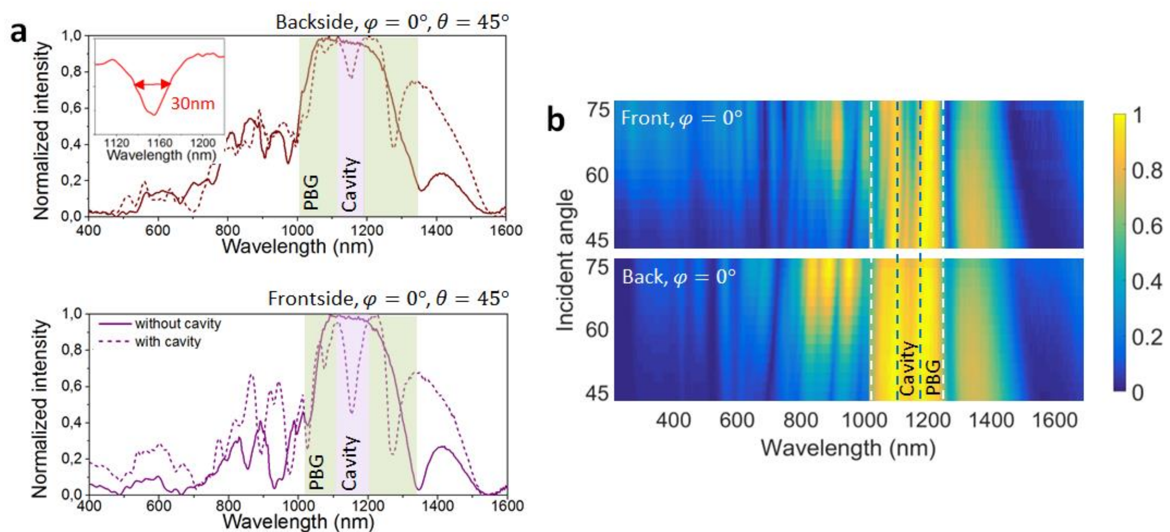


Figure 6.16. Reflection spectra of 3D PhC membranes with an embedded planar defect: (a) Comparison with reflection spectra without planar cavity from both front and back side; (b) Reflection spectra when the incident angle is tuned from 45˚ to 75˚.

The porous structure of fabricated 3D PhC membranes enables solvents and gases to easily infiltrate, thus the refractive index can be tuned in a controllable manner. Here we applied ethanol with different concentrations (in DIW) onto the 3D PhC membranes with glass as the substrate. The reflection spectrum was then measured using an ellipsometer at an incident angle of 45˚. A red shift could be observed both for the band edge of the reflection peak and the resonance mode of the planar cavity as shown in **figure 6.17a**. This can be explained as the electromagnetic confinement in the silicon cavity region started to leak inside the surrounding medium of solvent with a higher refractive index than air, and both the air band and dielectric band will be suppressed to a lower frequency level. The correspondence between the center wavelength of the resonance mode and the refractive

index of infiltrated solvent is recorded and shown in figure 6.17b, which suggested a sensitivity of around 397 nm RIU^{-1}. This is comparable with the result from silk inverse opal structures. [242, 243] After each measurement, the sample can be soft baked to let the solvents fully evaporate from the porous structures, thus multiple usage can be possible for sensing gases or solvents.

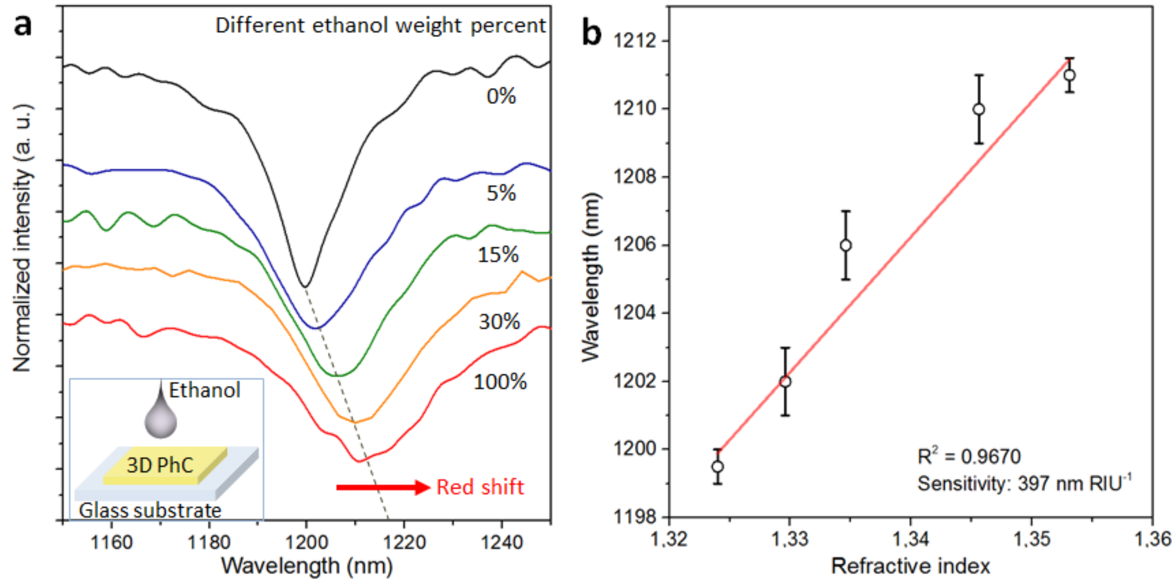


Figure 6.17. (a) Observed red shift of resonance dip, when ethonal solevent is dispensed on the 3D PhC membrane with a planar cavity; (b) The relation between center wavelength position of resonance dip and the refractive index of ethonal solution.

Fabricated 3D PhC membranes can also be transferred onto substrates with engineered surfaces as shown in figure **6.18a**, which can be difficult with traditional 3D PhC structures. The substrates that have been used were highly doped black silicon (antimony doped, resistivity < 0.25 Ohm·cm, doping concentration around 2×1028 cm^{-3}) created by DREM etch process, which has been discussed earlier in chapter 5 and is known to exhibit room temperature band-edge photoluminescence (PL) near infrared wavelengths. In the experiment, photoexcitation was performed with a 532 nm continuous wave (CW) laser (with the power of around 7.11 mW) on a RPM2000 Rapid Photoluminescence Mapper (Nanometrics). An InGaAs detector was used to detect the PL signals. When the surface of the black silicon was covered with a 3D photonic crystal membrane (with 6 periods, thickness of around 2 μm), the PL intensity in the PBG region was suppressed with an attenuation rate of around 20 dB as shown in figure 6.18b, while the PL signal could still be detected in the wavelength away from PBG region. When a membrane with a planar cavity was transferred on top of black silicon, the PL intensity in the band gap region was still low, but had a noticable peak at the wavelength of cavity resonance mode, which in this case act as an optical bandpass filter. However, due to the optical absorption of the silicon material at the excitation wavelength of 532 nm, the PL intensity at resonance wavelength was also reduced. Nevertheless, this demonstrates the possibility to apply the 3D photonic crystal membranes as an optical bandpass filter that is adaptable for different substrates.

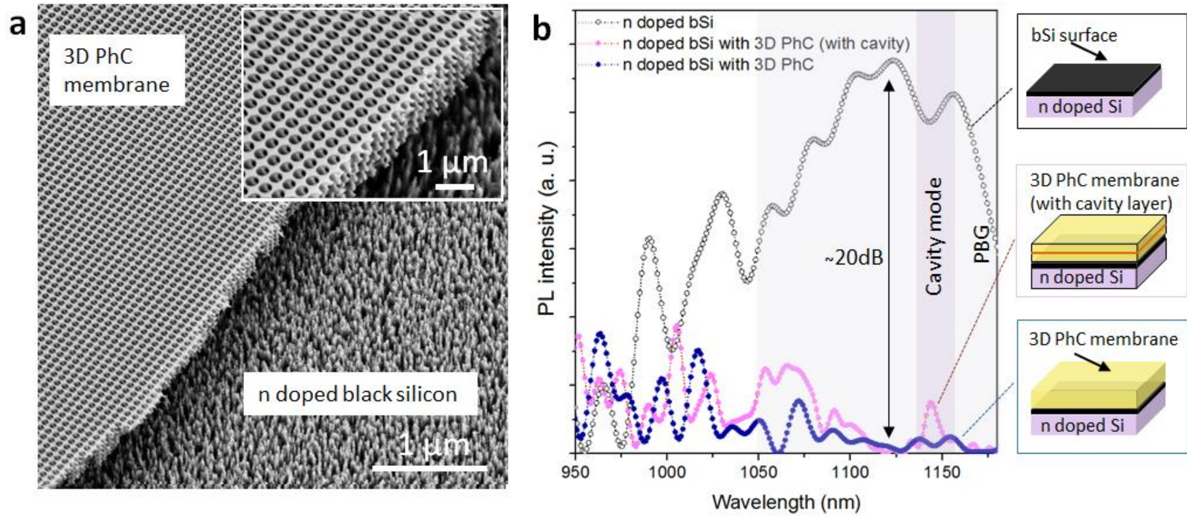


Figure 6.18. (a) SEM image of transferred 3D PhC membrane on a black silicon surface; (b) 3D PhC membrane as an optical filter of PL signal from black silicon substrates.

As a summary, modified DREM process has been demonstrated to be an effective method to fabricate 3D PhC structures. The fabricated membranes have a thickness of around 2μm with excellent mechanical stability. Reflectance spectra were recorded at different angles of incidence from 7.5° to 75°, suggesting a complete photonic band gap structure with a peak reflection at around 1100 nm. The fabricated membranes can be transferred manually onto different substrates, such as glass or black silicon surfaces. A soft 3D PhC membrane could also be achieved by infiltrating the structures with polymer. In addition a planar defect can also be conveniently introduced into the 3D PhC structures during the fabrication process, giving an optical resonance mode coupled with the stop band. The narrow resonance peak of around 30 nm linewidth can be used for sensing the concentrations of organic solvents. The PL from black silicon could be filtered effectively by 3D PhC membranes with the incoperated planar defect. Thus a convenient strategy is provided for large scale fabrication of flexible 3D PhC membrane structures with the feasibility to introduce planar cavities and possibilities for integration on different photonic devices. Other obvious application areas include biological sensors (e.g. in connection with bacteria/cell growth) as well as optical communications and lasers. The whole fabrication process is performed by standard fabrication technologies in the semiconductor industry and is CMOS compatible.

7 Conclusion and Outlook

As a conclusion of the thesis, we will summarize the achievements that have been made in this project. Further technological improvement and potential applications will also be discussed briefly.

Firstly, several technological developments have been achieved, especially in deep reactive ion etching processes for silicon micro- and nanostructures:

- The resolution limit of electron beam lithography has been improved. By optimizing process parameters of HSQ resist, patterns with sub-10 nm feature size can be produced on a silicon substrate. Since HSQ resist is well known to be highly sensitive and has a short shelf lifetime, a robust lithography process with a good repeatability has been developed;

- Real time monitoring systems for plasma etching processes have been installed to realize a more precise process control and a deeper understanding of etching processes: oscilloscope is used to monitor etching parameters with high temporal resolution; OES is used for analysis of plasma chemistry and endpoint detection; OEI is used for real time monitoring of etch rates of both masks and silicon;

- A 3-step modified Bosch process, named DREM process, has been proposed and developed. Compared with standard Bosch processes, several advantages of DREM processes have been demonstrated, e.g. easy to be programmed, a high etch selectivity, a precise control of etch profiles, etc. An aspect ratio of 50 has been achieved for microstructures with feature size of 1 μm; an aspect ratio of 20 has been achieved for nanostructures with minimized sidewall roughness. Based on DREM process, a 4-step modified Bosch process, named DREAM process, has also been proposed, which has shown its potential for fabrication of HAR structures;

- 3D silicon structures in both micro- and nanoscale have been fabricated successfully based on a modified DREM process, combining both anisotropic etch sequences and isotropic etch processes to create suspended structures. For microstructures, more than 10 vertically stacked layers of structures can be fabricated with one single process run; for nanostructures, 5 layers of stacked silicon nanowires (with linewidth of 20 nm) can be fabricated.

Owing to the technological developments as summarized above, some novel devices and applications can be designed and realized:

- By coating ZnO seed layer on 3D silicon micro-mesh structures with ALD, ZnO nanowires can be grown conformally on the 3D silicon surface. Because of the large surface area of 3D silicon substrate, the number density of ZnO can be increased by around one order of magnitude, leading to a significantly improved photocatalytic efficiency and photocurrent density. The ZnO NWs/3D silicon mesh hybrid structures can also be transformed into ZnS NWs/3D silicon mesh or ZIF-8@ZnO/3D silicon mesh, while the whole structures maintain intact;

- 3D silicon photonic crystal membranes can be fabricated with a thickness of around 2 μm and size of a few square millimeters. The periodic structures give a photonic stopband at around 1100 nm, where a strong reflection peak can be observed in a large range of incident angles from 7.5° to 75°, suggesting the existence of a complete photonic band gap. A planar defect can be embedded conveniently, which gives a resonant mode on top of the stop band. The fabricated membranes can be used as a sensor for organic solvent with a sensitivity of 397 nm RIU^{-1}. The fabricated membrane is also demonstrated to be a good optical bandpass filter with attenuation ratio of around 20 dB.

- Polarization-dependent, enhanced subwavelength optical resonance has been observed for stacked silicon nanowires with linewidths much smaller than visible wavelength. Vivid structural colors has been demonstrated with a spatial resolution of ~ 25000 dpi;

- ZIF-8 novel material has been explored. By using ALD grown ZnO as a seed layer, and gold nanoparticles as growth inhibitors, isolated ZIF-8 nanocrystals can be grown in a confined manner, and size-dependent optical resonance is then studied.

Based on these achievements in both fabrication technologies and applications, some research directions can be worth exploring in the future study, and some techniques need to be further improved to enable more freedom and possibilities for device fabrications. Firstly, from a technical point of view, there is still plenty of space to improve some of the some fabrication techniques, e.g.

- By performing an annealing procedure with H_2 or Ar, sidewall roughness on the silicon structures can be reduced significantly according to some previous studies. Preliminary tests will be performed with the coming annealing system in DTU Danchip;

- DREAM process will be further optimized. Since the resist corrosion can be avoided by using a thin hard mask, DREAM process will be a good candidate for HAR micro- and nanostructures;

- A deeper understanding of plasma process and etching apparatus should be achieved. For example, electron temperatures and plasma densities can be studied by installing a Langmuir probe, and the etching products can be analyzed by a downstream plasma chamber equipped with a separate OES system;

- 3D silicon micro- and nanostructures can be used as a mold to create 3D structures of other materials. For example, a replica of TiO_2 can be created by conformal ALD process,

3D polymer structures can also be created by nanoimprinting followed by silicon removal with KOH, etc.

When the fabrication techniques are further developed, some devices and applications will be further explored, for example,

- Sub-10 nm silicon structures with well-defined geometry and small sidewall roughness can have some interesting properties for quantum electronics, e.g. coulomb blockade or spin related effect;

- There are still many possibilities for 3D silicon structures, e.g. vertically stacked silicon nanowires can be promising for fabricating FET devices; arrays of 3D silicon nanostructures can be used for 3D metasurfaces or optical topological insulators;

- 3D silicon structures can also be used to integrate with novel materials (e.g. perovskite crystals or MOF particles) for heterostructures and related applications like solar cells, photocatalysis, etc.

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Appendix A. Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ALE	Atomic Layer Etching
ANOVA	Analysis of Variance
AR	Aspect Ratio
ARDE	Aspect Ratio Dependent Etching
BARC	Bottom-Anti-Reflective Coating
C_4F_8	Octafluorocyclobutane (or perfluorocyclobutane)
CD	Critical Dimension
CMOS	Complementary Metal–Oxide–Semiconductor
CPA	Control Performance Analyzer
DEZ	Diethylzinc
DIW	Deionized Water
DMF	Dimethylformamide
DREM	Deposit-Remove-Etch Method
DREAM	Deposit-Remove-Etch-Ashing Method
DRIE	Deep Reactive Ion Etching
DUV	Deep Ultraviolet
EBL	Electron Beam Lithography
EDX	Energy-dispersive X-ray Spectroscopy
ESC	Electrostatic Chuck
FDTD	Finite-Difference Time-Domain
FET	Field Effect Transistor
HAADF	High-angle annular dark-field
HAR	High Aspect Ratio
HMDS	Hexamethyldisilazane
HMTA	Hexamethylenetetramine
HRTEM	High Resolution Transmission Electron Microscopy
HSQ	Hydrogen Silsesquioxane

IAD	Ion Angular Distribution
IED	Ion Energy Distribution
LER	Line Edge Roughness
LSV	Line Sweep Voltammogram
LWR	Line Width Roughness
MeIm	Methylimidazolate
MFC	Mass Flow Controller
MIBK	Methyl Isobutyl Ketone
MOF	Metal Organic Frameworks
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
OEI	Optical Emission Interferometry
OES	Optical Emission Spectroscopy
PBG	Photonic Band Gap
PCA	Principal Component Analysis
PECVD	Plasma-enhanced Chemical Vapor Deposition
PGMEA	Propylene Glycol Methyl Ether Acetate
PhC	Photonic Crystals
PL	Photoluminescence
PSD	Power Spectral Density
PSF	Point Spread Function
RCA	Radio Corporation of America
RF	Radio Frequency
RhB	rhodamine B
RIE	Reactive Ion Etching
SC	Simple Cubic
SCE	Saturated Calomel Electrode
SEM	Scanning Electron Microscopy
SF_6	Sulfur Hexafluoride
SOI	Silicon-on-Insulator
STEM	Scanning Transmission Electron Microscopy
TEM	Transmission Electron Microscopy
TMA	Trimethylaluminium
TMAH	Tetramethylammonium Hydroxide
UV	Ultraviolet
VLSI	Very Large Scale Integration
XRD	X-ray Diffractometry
ZIF	Zeolitic Imidazolate Framework

Appendix B. List of Published Journal Articles

Published (as first author):

- **Chang, B.**, Leussink, P., Jensen, F., Hübner, J. and Jansen, H., (2018) DREM: Infinite etch selectivity and optimized scallop size distribution with conventional photoresists in an adapted multiplexed Bosch DRIE process. *Microelectronic Engineering*, 191, pp.77-83. https://doi.org/10.1016/j.mee.2018.01.034
- **Chang, B**., Jensen, F., Hübner, J. and Jansen, H., (2018) DREM2: a facile fabrication strategy for freestanding three dimensional silicon micro-and nanostructures by a modified Bosch etch process. *Journal of Micromechanics and Microengineering*, 28(10), p.105012. https://doi.org/10.1088/1361-6439/aad0c4
- **Chang, B.**, Yang, Y., Jansen, H., Ding, F., Mølhave, K. and Sun, H., (2018) Confined Growth of ZIF-8 Nanocrystals with Tunable Structural Colors. *Advanced Materials Interfaces*, 5(9), p.1701270. https://doi.org/10.1002/admi.201701270
- **Chang, B.**, Tang, Y., Liang, M., Jansen, H., Jensen, F., Wang, B., Mølhave, K., Hübner, J. and Sun, H., (2018) Highly Ordered 3D Silicon Micro-Mesh Structures Integrated with Nanowire Arrays: A Multifunctional Platform for Photodegradation, Photocurrent Generation, and Materials Conversion. *ChemNanoMat*. https://doi.org/10.1002/cnma.201800371
- **Chang, B.**, Zhou, C., Tarekegne, A., Yang, Y., Zhao, D., Jensen, F., Hübner, J. and Jansen, H., Large area three dimensional photonic crystal membranes: single-run fabrication and applications with embedded planar defects. (accepted by *Advanced Optical Materials*)

Published (as second author):

- Han, A., **Chang, B.,** Todeschini, M., Le, H. T., Tiddi, W., and Keil, M. (2018). Inductively coupled plasma nanoetching of atomic layer deposition alumina. *Microelectronic Engineering*. https://doi.org/10.1016/j.mee.2018.02.023

Submitted (as co-author):

- Zheng, Y., Yi. A., **Chang, B.,** You, T., Huang, K., Ou, X., Pu, M., and Ou, H., High-Confinement, High-Q Silicon Carbide-On-Insulator (SiCOI) Microring Resonators. (submitted to Asia Communications and Photonics Conference 2018)

Appendix C. Conference Contributions

Conference contributions

43rd International conference on Micro and Nano Engineering
Braga, Portugal, 2017

- **Chang, B.,** Leussink, P., Jensen, F., Hübner, J. and Jansen, H. (2017). RIE-lag "Correction" in Bosch Etch Process of Silicon to Enable Profile Straightness and Improved Scallop Size Distribution. (*poster presentation*)
- **Chang, B**., Leussink, P., Jensen, F., Hübner, J. and Jansen, H. (2017). Infinite Etching Selectivity with Conventional Photoresist in a Bosch Process. (*poster presentation*)
- Silvestre, C., **Chang, B.,** Jansen, H., & Hansen, O. (2017). Microfabrication of X-Ray grating for Talbot Interferometry.
- Han, A., **Chang, B.,** Todeschini, M., Le, H. T., Tiddi, W., and Keil, M. (2017). Inductively Coupled plasma nanoetching of alumina made by atomic layer deposition.

44th International conference on Micro and Nano Engineering
Copenhagen, Denmark, 2018

- **Chang, B**., Jensen, F., Hübner, J. and Jansen, H. Three dimensional engineering of silicon micro- and nanostructures. (*oral presentation*)

Appendix D. Journal Articles

Microelectronic Engineering 191 (2018) 77–83

Contents lists available at ScienceDirect

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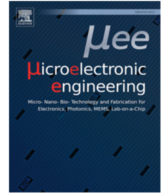
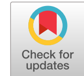


DREM: Infinite etch selectivity and optimized scallop size distribution with conventional photoresists in an adapted multiplexed Bosch DRIE process



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ABSTRACT

The quest to sculpture materials as small and deep as possible is an ongoing topic in micro- and nanofabrication. For this, the Bosch process has been widely used to achieve anisotropic silicon microstructures with high aspect ratio. Reactive ion etching (RIE) lag is a phenomenon in which etch rate depends on the opening areas of patterns, aspect ratio of the trenches and other geometrical factors. The lag not only gives a non-uniform distribution of scallop size, but it also sets a limit for the maximum achievable aspect ratio. The latter since the mask suffers from persistent erosion. While different kinds of hard masks have been suggested to ensure a longer total etch time, here we report a correctly tuned 3-steps Bosch process – called DREM (Deposit, Remove, Etch, Multistep) – without mask erosion. The erosion-free feature is independent of the type of mask. For example, an aspect ratio of more than 50 is achieved for trenches with 1 μm linewidths, while no erosion is observed for 360 nm thin standard photoresists. The mechanism behind this extraordinary infinite selectivity is mainly due to the depletion of C_4F_8 deposition species. Furthermore, a linear ramping of the etch step duration is performed to achieve a uniform distribution of scallop sizes along the etch profile. This outperforms the usual broad scallop size distribution when no parameter ramping is performed and improves the straightness of the etch profile considerably, in addition, it allows an easier way to control periodic sidewall shaping. e.g., a sausage-chain-like feature is demonstrated with an almost perfect periodicity.

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1. Introduction

Etching silicon is one of the key technologies in mainstream semiconductor industry and dry plasma etching has become indispensable to transfer patterns anisotropically (i.e. directionally). The current trend is to sculpture the silicon as deep and precise as possible while preserving the critical dimension of the original photoresist pattern; i.e. to achieve extreme high aspect ratios. Two perfect examples are the creation of deep silicon pores to create highly area-efficient trench capacitors and the structuring of high-raised silicon pillars useful in the fast evolving photonic crystal discipline. By performing a pulsed process in so-called deep reactive ion etching (DRIE; e.g. the Bosch sequence), the sidewall of trenches can be protected during an etch process and the etch depth can be significant with minimal undercut. However, the achievement of extremely high aspect ratios, e.g. larger than 50, remains challenging. The main reason is that, when etch depth increases, the silicon etch rate slows down due to the notorious reactive ion etching (RIE) lag [1], while the mask erosion continues at the same speed. This means that the selectivity (etch rate of silicon divided by the erosion rate of mask) drops drastically when the aspect ratio increases and the etching should be halted before the mask is totally eroded away. This issue sets a limit for high aspect ratio etching and a lot of efforts have been undertaken to find a "hard" mask with sufficient high selectivity, e.g. Al [2], Cr [3], SiO_2 [4], or Al_2O_3 [5]. However, a hard mask can be sputtered during etching and creates roughness [6]. Furthermore, the transfer of resist patterns into the hard mask will increase fabrication complexity.

Another issue to consider in Bosch sequences is the non-uniform distribution of scallops [7]. While the scallops are generated during the isotopic silicon etch steps, due to RIE lag the scallop size decreases while the Bosch process continues. This non-uniformity in scallop size is pronounced especially in devices with high aspect ratio. Furthermore, this aspect ratio dependent scallop size distribution will not only change the sidewall profile, but it will also generate difficulties for post-etch sidewall smoothening procedures.

A third important high aspect ratio feature is sidewall corrosion due to off-normal ionic bombardment. It can be due to the not always perfectly straight trajectory of ions leaving the plasma boundary, some

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collisions inside the plasma sheath, or deflection of the charged species by an image force [14]. Although this issue can be very problematic, it has not been truly pronounced in the present work and will therefore not be addressed in detail.

Here we propose a correctly tuned 3-steps cyclic Bosch process (step 1 – C_4F_8 deposition, step 2 – Ar bottom removal, and step 3 – SF_6 isotropic silicon etch) as suggested in previous literature [8]. From now on we will call this procedure DREM (**D**eposit, **R**emove, **E**tch, **M**ultistep). By carefully tuning the balance between deposition and bottom removal, the mask can stay fully intact and an infinite etch selectivity is achieved. Furthermore, a linear time ramping of the etch step is employed to counteract the decreasing etch rate caused by RIE lag. By combining these two techniques, it is possible to etch silicon trenches (1 μm linewidth, 10 μm pitch) with an aspect ratio of more than 50 without degradation of a conventional photoresist while keeping all the scallops downwards the trench almost identical in size rendering the sidewall almost perfectly straight.

2. Materials and methods

Silicon wafers (150 mm diameter, single side polished) were given a 65 nm (60 s at 4700 rpm) thick bottom antireflective coating (BARC, DUV42s-6, Brewer Science) in a robot system (Gamma 2 M, Süss) with a soft baking temperature of 60 s at 175 °C. On top of the BARC layer, a 360 nm thick deep ultraviolet (DUV) resist (JSR KRF M230Y, JSR-Micro) was coated (60 s at 2500 rpm) with a 90s soft baking temperature at 130 °C. Afterwards trenches with 1 μm linewidth and 10 μm pitch were patterned by a DUV stepper system (FPA-3000EX4, Canon), which was equipped with a 248 nm KrF excimer laser (intensity 280 mW/cm^2, dose 21 mJ/cm^2 and focus depth 0.17 μm). The samples were baked right after exposure for 60 s at 130 °C, and developed in AZ726 (AZ Electronic Materials) for 60 s, rinsed in DI water and dried by spin coating in a gentle nitrogen stream.

The thickness of both the BARC layer (65 nm) and resist (355 nm) were determined by a spectroscopic ellipsometer (Vase, J.A. Woollam Co., Inc.), with a standard deviation of 1 nm. To verify the critical dimension of exposed patterns, scanning electron microscopy (SEM, Supra V60, Zeiss) images were taken both from a top view and cross-sectional view. The results show an average linewidth of 0.95 μm across the wafer, with standard deviation of 0.02 μm. The sidewall angle of the resist was measured to be around 82°.

The plasma etching process was performed in a dual source etching system (DRIE Pegasus, SPTS) from which the settings will be discussed in the next section. The samples were cleaved manually into pieces of around 2 cm by 2 cm and attached to a carrier wafer with Fomblin oil (Solvay Solexis S.P.A.). To ensure sufficient process reproducibility, the silicon carrier wafers (100 mm, single side polished) were coated with 100 nm Al_2O_3 (alumina) passivation coating by atomic layer deposition (ALD, Picosun R200 ALD system). These carrier wafers have been found to be relatively undisturbed by the plasma and could be reused throughout the experiments.

After etching, the sample pieces were cleaved manually and analyzed by SEM. The analysis of scallop size distribution was performed by Matlab (R2015b, MathWorks), which could extract coordinates of scallop edges from the SEM images.

3. Results and discussions

3.1. Infinite etch selectivity

The basic parameter setting for the 3-steps DREM process with an illustrative diagram is shown in Fig. 1. A full tool recipe is presented in the supplementary section. In the first **1.8 s deposition step**, C_4F_8 plasma is used to passivate the wafer with a fluorocarbon (FC) layer. A minimum of platen power is applied to ensure low mask erosion [9]. The processing temperature was chosen to be approximate minimum of −19 °C allowed by the tool. Also the pressure is optimized with respect to the 3000 W coil power for maximum FC deposition rate. In the second **1.9 s removal step**, low pressure (5mTorr) argon plasma with high bias power (75 W, with DC bias of around 325 V) is used for 1.0 s to clear the FC film from the bottom of the trenches. By taking rise time of mass flow controllers (MFC) and delay time caused by the reactor residence time into consideration, the process synchronization is established for optimal performance as suggested in [8]. It is easier to maintain low pressure plasma with argon than with e.g. SF_6, because argon is an electropositive gas (it provides electrons) whereas SF_6 is electronegative (it scavenges electrons). To minimize the coil reflective power, the argon gas flow was chosen to be 200sccm during deposition, and 250sccm during bottom removal and etching. The lowest possible pressure during bottom removal is needed to sharpen the ion angular distribution as much as possible, thus ensure a maximum straight profile. In the third **time-ramped etching step**, SF_6 based plasma is used to etch silicon isotropically at the cleared bottom of the trenches. Again a minimum platen power is applied, to preserve the mask. By using time ramping during this SF_6 step, the scallop sizes can be tuned to be almost identical along the trench. The initial etch step duration was chosen to be 0.6 s to ensure correct initial etches and the final etch step duration t_{end} was carefully tuned as discussed in the next section. We should notice that switching off the SF_6 flow abruptly after the etch step is bad news for the coil reflected power as the sudden change in plasma chemistry will cause sharp harmful peaks in the reflected power. We have improved this issue by smoothing the gas flow changes

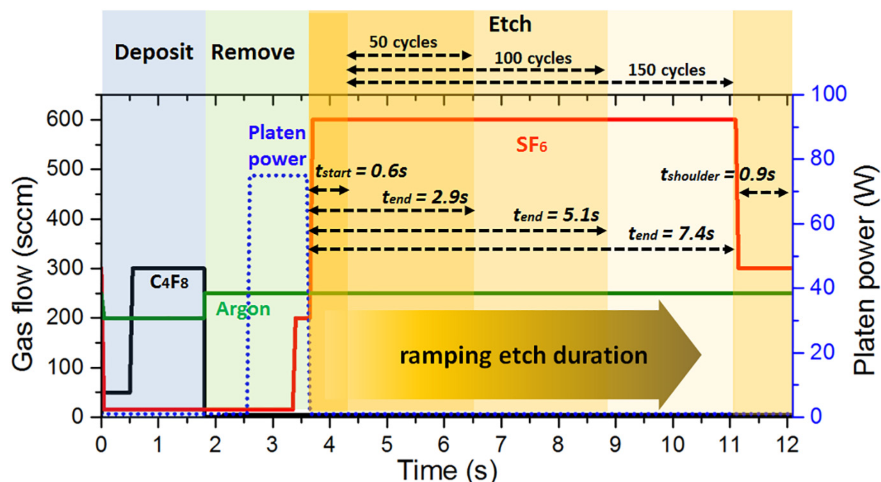

Fig. 1. DRIE parameters and etch sequence.

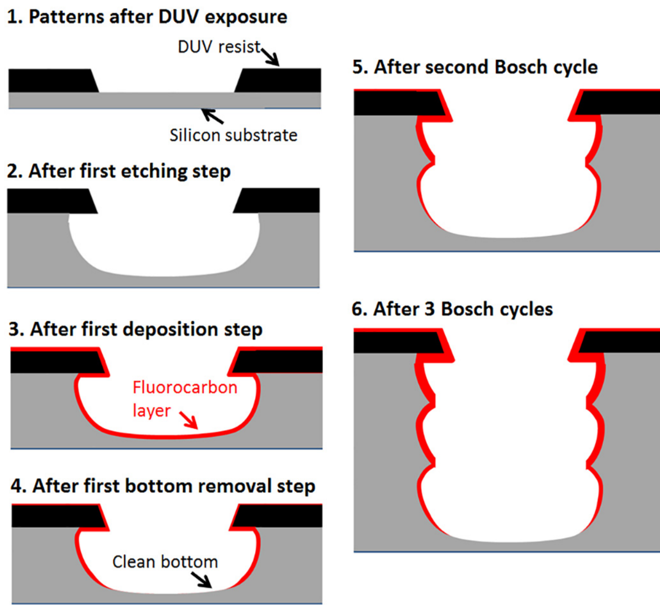

Fig. 2. Schematic of the first DREM cycles showing that silicon is etched without photoresist attack.

with what we call 'shoulders'. For the SF6 flow, the flow starts with a 0.3 s at 200sccm shoulder and then it goes to 600sccm and it stops the flow with a 1 s at 300sccm shoulder. For the 300sccm C_4F_8 flow we did the same with a 50sccm shoulder. Using the gas flow shoulders, we could maintain a very high power without matching problems.

The reason why an infinite selectivity is achieved is not because of intrinsic properties of a specifically selected photoresist. Most resist-types have selectivities around 100 or less [10]. Instead, the extraordinary high selectivity is caused by the non-conformal FC deposition inside etched structures. This layer protects not only the features sidewalls, as well as the mask. The mechanism is shown briefly in Fig. 2. Firstly, silicon is etched isotropically using SF_6 plasma (Fig. 2.1 and 2.2). Secondly, C_4F_8 is applied for FC passivation (Fig. 2.3). Importantly, due to depletion of species inside the trenches, the thickness of the FC film is thicker on top of the resist pattern compared with the bottom of the etching trench. Then, the FC film is removed directionally with a bias during the Ar bottom removal step. If the applied bias is just enough for clearing the bottom of the trench, the resist will still be covered by some added FC film residue (Fig. 2.4). Thus, when the etch process goes on to next cycles, the resist (or any other mask material) will always be protected (Fig. 2.5 and 2.6).

The etch profiles of the 1 μm wide trenches are shown in Fig. 3. After etching the BARC layer, 50 cycles were performed to reach an etch depth of 18.8 μm (Fig. 3.a1), while the 360 nm resist remained intact (Fig.3.b1). After 100 cycles, the etch depth was doubled and the resist was still undisturbed (Fig. 3.a2/b2). Noticeably, a rather thick FC layer started to grow at the topside of the etched structure narrowing the trench opening of the flowing gases (Fig. 3.b2). This effect is a direct result from the non-uniform step coverage due to the lack of surface migration. So, the downside of the infinite selectivity (which is based on the non-uniform coating characteristic) is that the smaller openings tend to close while etching proceeds. When we increased the number of cycles further to 150, the etch depth was around 58.1 μm, which implied an aspect ratio of more than 50, while the sidewall of the trench started to be slightly corroded (Fig. 3.a3). Furthermore, the trenches have the tendency to become a slightly more positive tapered towards

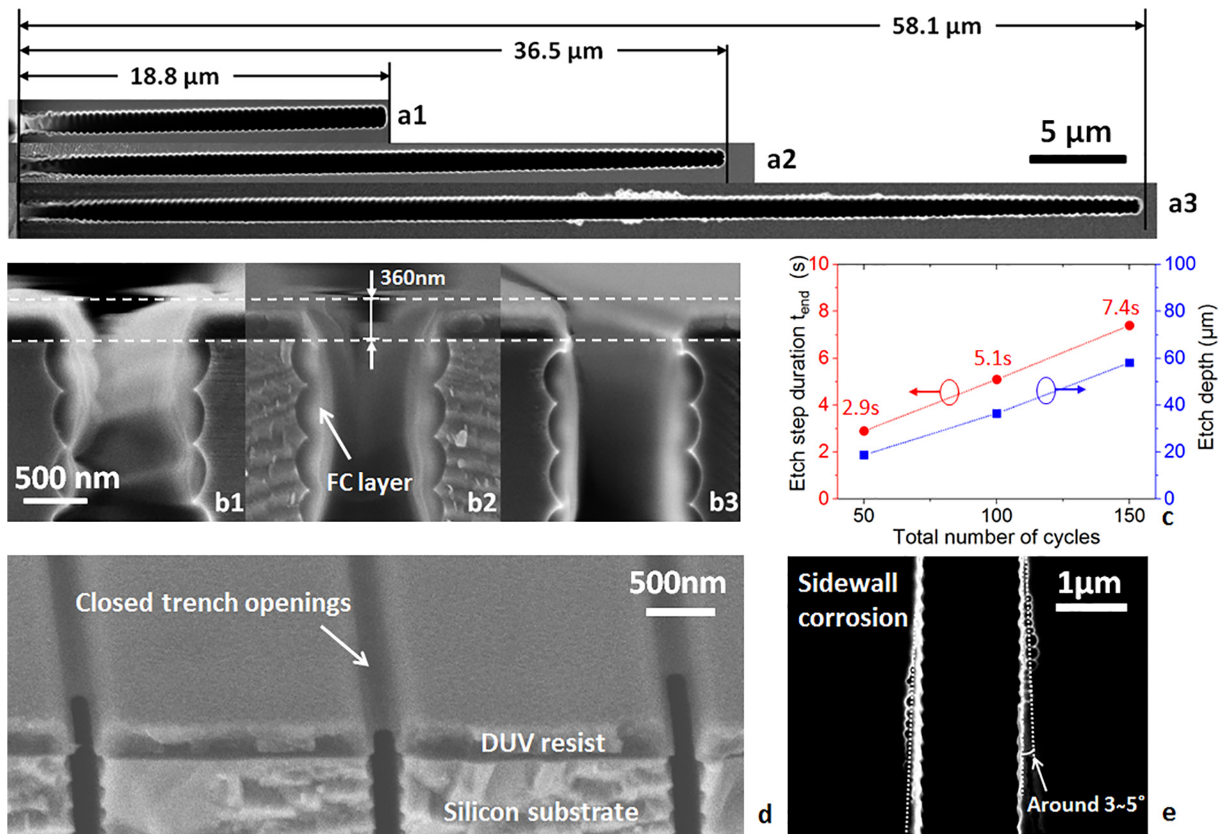

Fig. 3. Etch profile evolution during DREM a1) 50 cycles; a2) 100 cycles; a3) 150 cycles. And the corresponding top parts of the trenches b1) 50 cycles; b2) 100 cycles; b3) 150 cycles. The linearly increasing etching depths for these three processes are shown in (c), with different etching step durations t_{end} at the end of etch. For trenches with linewidth of 200 nm, the openings are closed as shown in (d). For trenches with high aspect ratio, slight sidewall corrosion can be observed as shown in (e).

the bottom of the trench. This is most likely the result of the slowly closing trench entrance while etching proceeds. The total etch depths and the duration of etch step in the last cycle t_{end} are shown in Fig. 3.c, which suggests a linear relation between etch depths and total number of cycles, this is due to the identical scallop sizes given by parameter ramping. Thus, by carefully tuning DREM, silicon can be etched directionally with identical scallops and infinite selectivity with respect to conventional photoresists; i.e. resist is not consumed at all. Obviously any mask (e.g. Cr, SiO_2 or Si_3N_4), even though not demonstrated here, will be able to perform this task as well. Therefore, DREM is believed to be the key to realize ultrahigh aspect ratio structures with a free choice in masking material.

There are two issues that should be addressed regarding this process. The first is the closing trench most likely due to the lack of surface migration of the growing FC film. On the one hand the FC film will provide the top part of the trench sufficient protection against erosion, but on the other hand the non-conformal layer will limit the incoming etching species and influence the ion angular distribution (IAD), both of which will cause non-uniformity in the etch process. When the process continues the trench will even be fully closed and the etch process will not be able to continue. This effect is especially pronounced for trenches with a very small linewidth (as shown in Fig. 3.d), in which the top part of a 200 nm wide trench is totally closed by the FC layer. The method to solve this problem is to add an oxygen plasma pulse after every SF6 etch step. Thus the trench can be opened again and DREM can continue. So, in total there will be 4 steps during this process, which the authors have called the DREAM process (Deposition with C_4F_8, Removal bottom with Ar, Etching with SF_6, Ashing with O_2, Multistep). Clearly, due to the constant removal of FC polymer, the photoresist will also erode quickly and the infinite selectivity with respect to photoresist is lost, thus in this paper, a DREM process (that is to say, a DREAM process without the O_2 ashing step) was performed, which results in a straight profile with a relatively high aspect ratio. Nevertheless, for hard mask materials DREAM is a viable option.

Another issue is the sidewall corrosion, which can be clearly seen when the aspect ratio is more than 50 (as shown in midsection in Fig. 3.a3 and a close up view in Fig. 3.e). The authors noticed that this sidewall corrosion is closely related to the sidewall angle of the profile. We already discussed that the passivation of ion inhibitors is increasingly limited with increasing aspect ratio and, therefore, the lower region of the sidewall will be less FC protected. However, during the bottom removal step the accelerated argon ions can be transported down to the bottom of trenches virtually unchanged in number. But, due to the non-ideal Ion Angular Distribution (IAD), also the sidewall will be continuously exposed to off-normal incoming energetic ions. Thus when the etching depth increases, the off-normal argon ions will start to corrode the passivation layer and create weak points in the sidewall protection [11]. Since the middle part of the trench has less sidewall protection compared with the top part, and is exposed to the ion bombardment for a longer time than the bottom part, the sidewall corrosion is most pronounced in the middle of the trench. One way to solve this issue is to tune the profile to a slightly negative tapered angle, either by increasing the platen power during bottom removal steps, or by reducing the passivation during the deposition steps. With the profile slightly negatively tapered, the sidewall will suffer less off-normal ion bombardment. The downside of this method is that the infinite selectivity might get lost.

3.2. Optimized scallop size distributions

As mentioned in the previous section, parameter ramping was used to achieve uniformly distributed scallop sizes. The direct measurement of scallop sizes along the sidewall, however, can be difficult or cumbersome, and several techniques have been reported before, e.g. using a

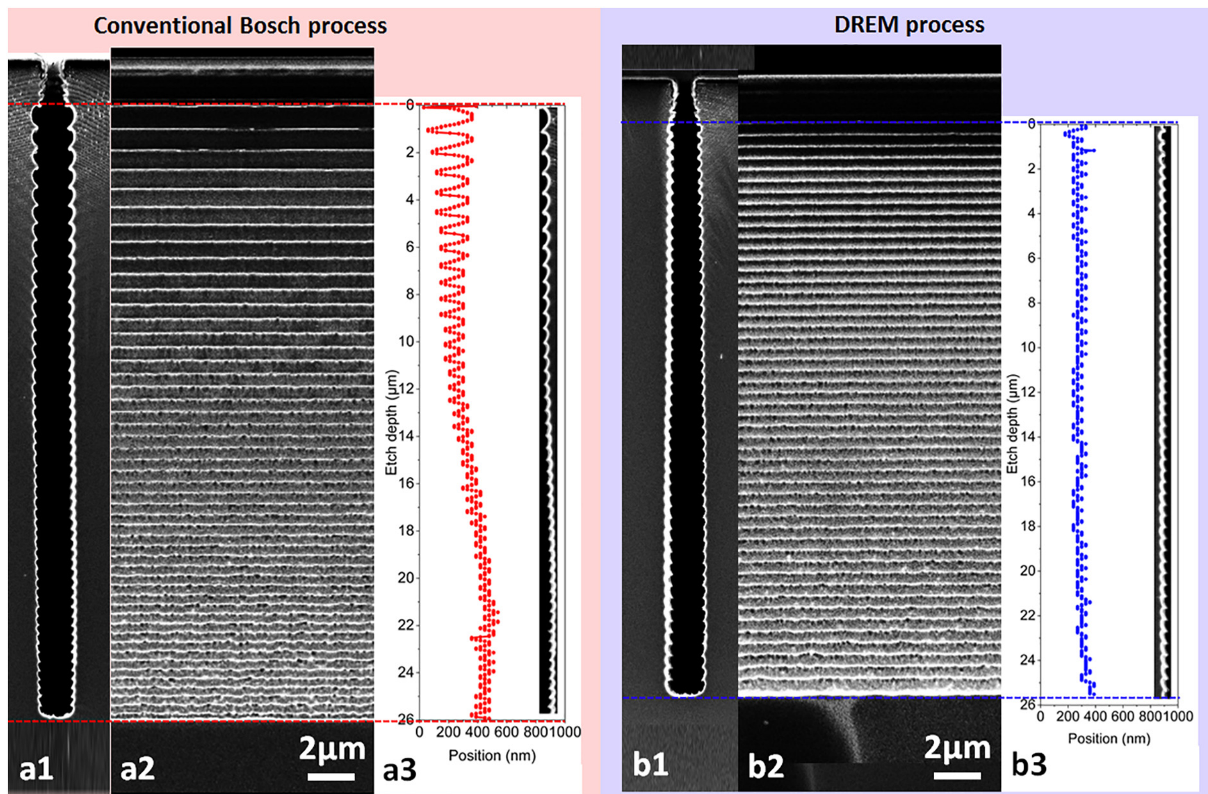

Fig. 4. Etching profile of experiment a (a1) without time ramping, and experiment b (b1) with time ramping. A 2-dimensional view of sidewall surface of exp.1 (a2) and exp.2 (b2). Extracted etch profile from exp.1 (a3) and from exp.2 (b3).

specially built atomic force microscopy (AFM) system as in [12,13], or using a conventional AFM system to scan the surface of a replica from the trench structures [14]. In our experiment, in order to quickly get a quantitative analysis for process optimization, the samples were first manually cleaved and pictured with SEM and further studied by Matlab. Based on the pixel size and coordinates of sidewall edges, the scallop sizes can be calculated and analyzed.

Two experiments were performed to prove the increased uniformity of scallop size distribution. In the first experiment, we performed 'standard' 50 Bosch cycles with a 1.5 s deposition step and a fixed 6.0 s etch step. The etch depth was 29.4 μm (Fig. 4.a1). In the second experiment, to counteract the effect of changing scallop size and profile straightness due to RIE-lag, the SF_6 time was linearly ramped from 3.5 s to 8.5 s during 50 DREM cycles. The other parameters were unchanged. The etch depth was 27.5 μm (Fig. 4.b1). Although the etch depth of exp.1 is slightly larger than in exp.2, the scallop sizes can be observed to be more uniform when etch-time ramping is performed. The samples were also cleaved manually along the trench openings, which gave a direct view of 2-dimensional sidewall surface as in Fig. 4.a2 and Fig. 4.b2. The etch profiles of both experiments were extracted from SEM images

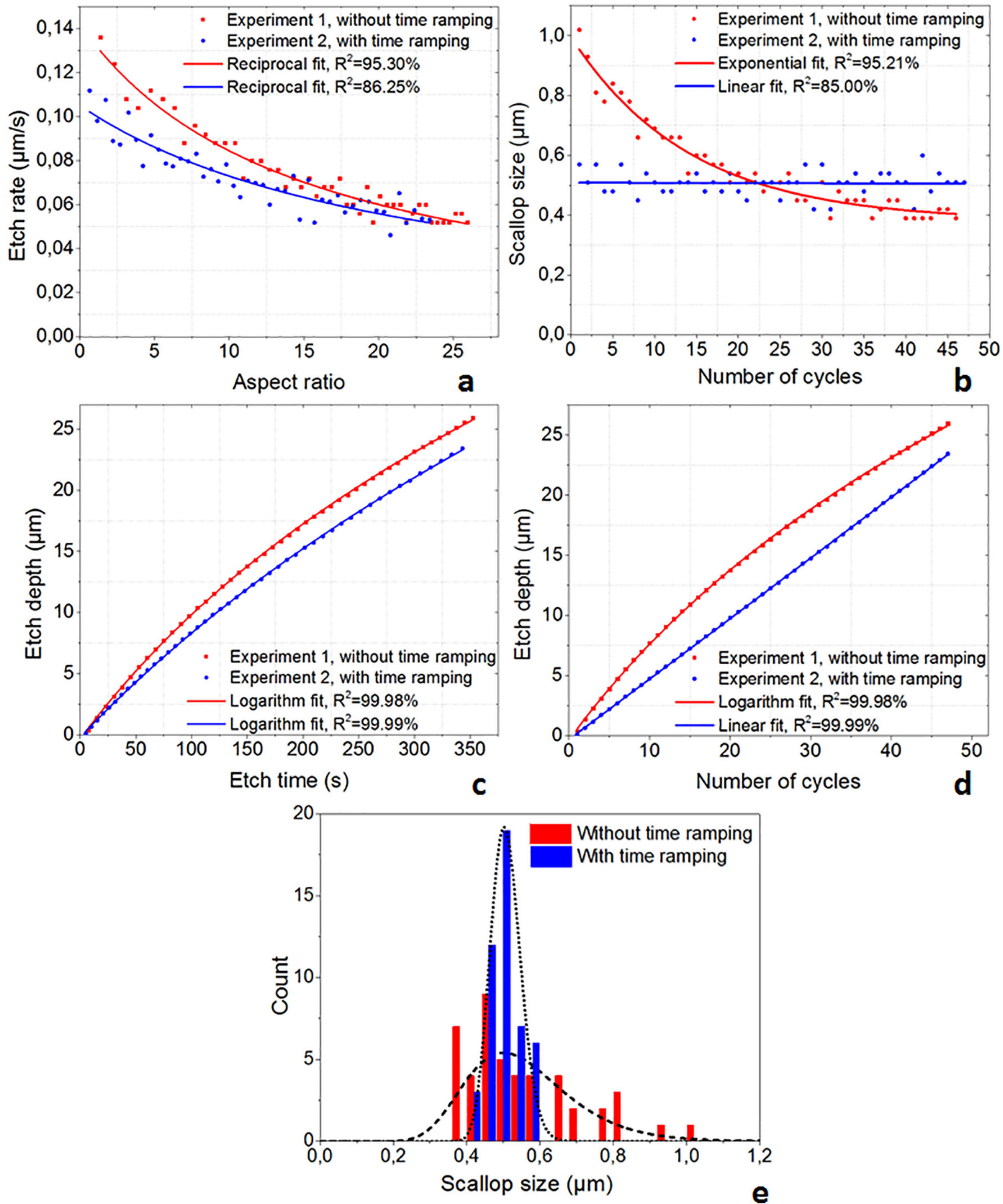

Fig. 5. Etch rate as a function of aspect ratio for both experiment 1 and experiment 2 (a); scallop sizes as a function of number of cycles for both experiment 1 and experiment 2 (b). Etch depth as a function of etch time for both experiment 1 and experiment 2 (c); etch depth as a function of number of cycles for both experiment 1 and experiment 2 (d); scallop size distributions for both experiment 1 and experiment 2 (e).

using Matlab (Fig. 4.a3 and 4.b3), from which we can clearly see an increased uniformity of scallop sizes and profile straightness when performing time ramping.

RIE lag is a phenomenon in which etch rate depends on the opening areas of patterns, aspect ratio of the trenches and other geometrical factors [1]. Some studies explain this by ion angular distribution, which will cause depletion of ions and radicals along the trench and slow down the etch process [15]. Other studies suggest attenuated neutral transport along the trench passage to be the reason [16]. Whatever is the actual cause, when aspect ratio increases the etch rate (scallop size divided by cycle time) for both experiments decreases (Fig. 5.a). Nevertheless, while in exp.1 the average scallop size decreases monotonically (Fig. 5.b), the scallop sizes for exp.2 remains roughly identical (507 nm with 40 nm standard deviation). Of course, the etch depth as a function of time is still nonlinear for both experiments (Fig. 5.c), which also suggests a decreasing etch rate (slope of the curve). However, the etch depth as a function of number of cycles (Fig. 4.d) is linear for exp.2. A qualitative explanation of this linear relation can be, that in our experiments the linearly increasing etch time can compensate for the decreasing average etch rate, which can be approximated as a quadratic function of aspect ratio [17]. However, depending on different models, the relation between the average etch rate and aspect ratio can be more complicated [18] [19], and for higher aspect ratio etching, a quadratic fitting will deviate from the real average etch rate, thus a linearly increasing etch time will not be sufficient to compensate for the drop of average etch rate.

From the results above, we can see that by performing a parameter ramping during a Bosch process, we can counteract the effect of RIE-lag on the usual non-uniformity of scallop sizes. Since the variance of scallop sizes has a detrimental effect on overall sidewall roughness and sidewall straightness, a higher uniformity of scallop size distribution will make the sidewall much straighter. At the same time it is also

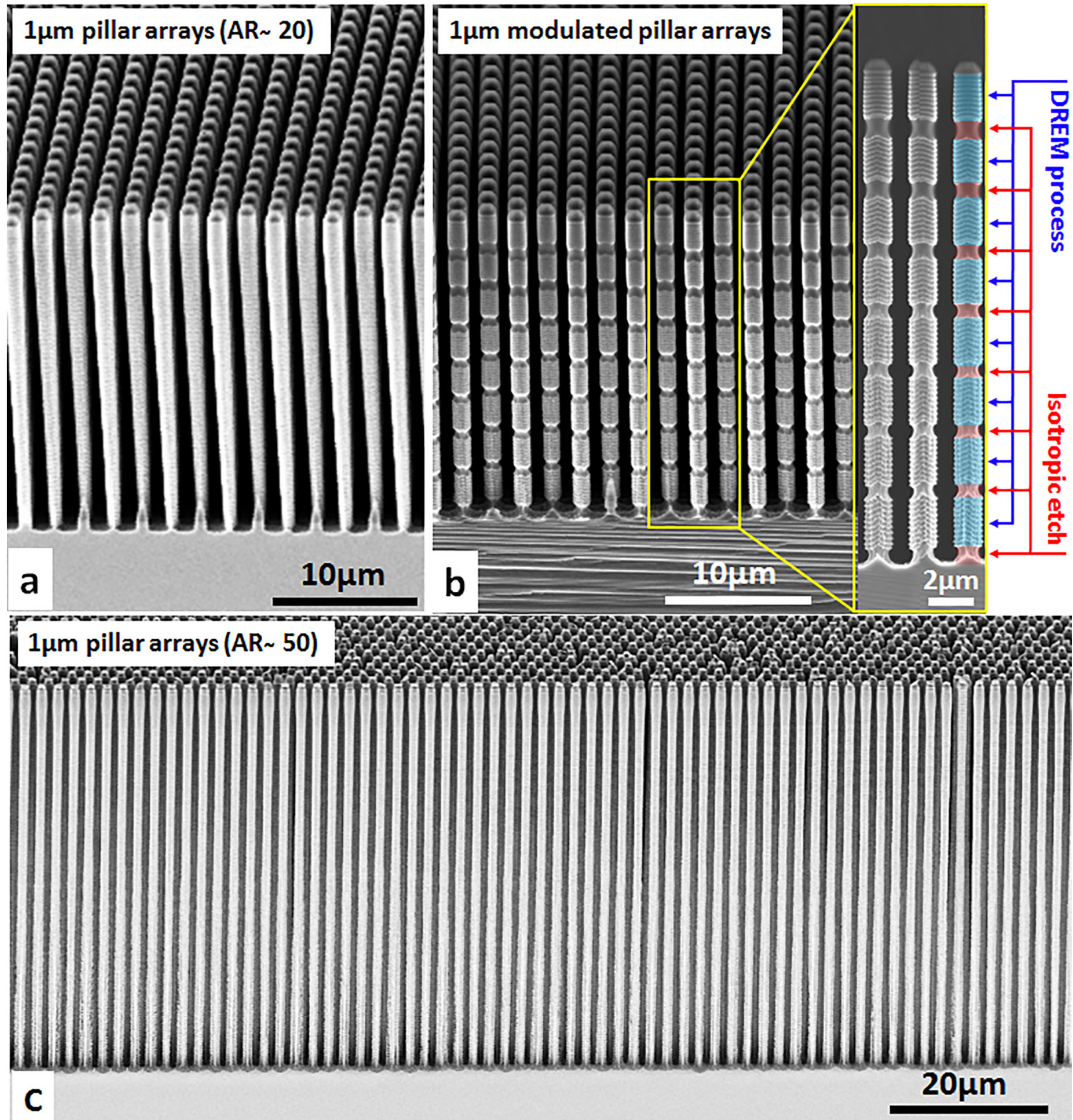

Fig. 6. 1 µm pillars after 100 DREM cycles (a); the same DREM process but repeatedly interrupted by time-controlled isotropic etches that creates sausage-chain-like features (b); 1 µm pillars after 175 DREM cycles (c). (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

a promising method for high aspect ratio etching as for very high aspect ratios, any deviation from a straight profile will limit the maximum achievable aspect ratio.

The strategies discussed above have been successfully applied to pillar structures with diameters of 1 μm. Firstly, 100 cycles of DREM process were applied resulting in an etch depth of 23 μm (Fig. 6.a). Secondly, a combination of DREM process and isotropic etch process was performed, in such a way that every 10 cycles of DREM process were followed by isotropic etch (200sccm SF_6, 3000 W coil power, 0 W platen power, the time was ramped up at the same rate as the Bosch cycles), 80 DREM process cycles were performed in total. This specially modified etch process can achieve a modulated etch profile (Fig. 6.b), which consists of straight etch profiles (labeled by blue false color in Fig. 6.b) separated by "nodes" with isotropic profiles (labeled by red false color in Fig.5.b). We can notice that there is still plenty of photoresist left, and the distance between each 'nodes' is very similar (2.5 μm). These special features couldn't be achieved without the high etch selectivity and an accurate control of etch profiles. As a consequence, DREM can open pathways to manufacture periodic 3D structures beneficial for example in next generation photonics or electronics. Besides, by applying 175 cycles DREM cycles, a high aspect ratio of 50 could be achieved for pillar structures with diameter of 1 μm (Fig. 6.c).

4. Conclusions

A DREM procedure is reported to improve and optimize a conventional DRIE process (Bosch). An aspect ratio of 50 is achieved for 1 μm wide trenches with identical scallops down the trench and without any consumption of conventional photoresist during the etch process. We have achieved a plasma etch process with infinite selectivity. This procedure is promising to etch deep silicon structures without using hard masks, which will not only get rid of sputtering issues, but also simplify the process flow. The reported process can be beneficial for industrial productions, since less materials and less time needs to be invested. The scallop size distribution is optimized using a parameter ramping strategy, which can "correct" the effect of RIE-lag. This process can be favorable for applications as microbattery [20], photonic devices [21], through silicon vias [22], X-ray gratings [23], etc. For post etch processes such as sidewall smoothening by oxidation [24], this uniform distribution of scallops and a straight profile are also favorable, since scallops will be oxidized at almost the same oxidation rate.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mee.2018.01.034.

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PAPER

DREM2: a facile fabrication strategy for freestanding three dimensional silicon micro- and nanostructures by a modified Bosch etch process

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DREM2: a facile fabrication strategy for freestanding three dimensional silicon micro- and nanostructures by a modified Bosch etch process

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Abstract

Three dimensional (3D) silicon micro- and nanostructures enable novel functionalities and better device performances in various fields. Fabrication of real 3D structures in a larger scale and wider applications has been proven to be limited by the technical difficulties during the fabrication process, which normally requires multiple process steps and techniques. Direct top-down fabrication processes by modifying a plasma etch process have been proposed and studied in previous studies. However, the repeatability, size uniformity and the maximal number of stacked layers were limited. Here we report a facile single run fabrication strategy for three dimensional silicon micro- and nanostructures. A good uniformity of suspended layer thickness has to be achieved and up to 10 stacked layers have been fabricated in a single run without other additional steps or post-process procedures. This is enabled by a modified multiplexed Bosch etch process, so called DREM (deposit, remove, etch, multistep), while the DREM etch is used to transfer the patterns into silicon, an extra isotropic etch creates a complete undercut and thus freestanding structures come into form. This method is easy to program and provides well-controlled etch profiles.

Keywords: DRIE, DREM, silicon, plasma etching, Bosch process, three dimensional structures

(Some figures may appear in colour only in the online journal)

1. Introduction

Three dimensional (3D) silicon micro- and nanomachining has attracted a lot of interest in recent years for both research and industrial uses, and several promising applications have been proposed and demonstrated, e.g. vertically stacked silicon nanowires for field effect transistors (FET) [1], unified memory [2] and biosensors [3], shape-modified silicon nanopillars for quantum transport study [4] and FET [5], 3D silicon single cubic structures for 3D photonic crystal structures [6], etc. However, to easily fabricate 3D micro- and nanostructures, and simultaneously obtain a good size and shape control of the fabricated structures, is still considered to be difficult.

Bottom-up methods can create single crystalline silicon nanostructures, and the morphology can be encoded [6], however, this method is difficult to be integrated in traditional complementary metal-oxide-semiconductor (CMOS) industries. Top-down approaches, which can transfer the 2D lithography patterns into silicon in a 3D structure have been studied extensively before, e.g. using wet etching [7, 8], or more commonly, plasma etching (also called dry etching). Some of the dry etching methods reported before rely on an additional oxidation procedure to protect the sidewall of the structures during the dry release step [9, 10], however, the oxidation step and bottom opening step add extra fabrication complexity. Some other studies make use of the scallops

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generated during a Bosch process and the self-limited oxidation process [3], however, the removal of the oxide layer after the etching process requires special techniques, such as vapor release or critical drying release, especially for nanostructures, which are easily collapse under capillary forces.

Here we report an improved fabrication method for 3D silicon micro- and nanostructures based on a previous paper by the authors [11], which require only one single plasma run without additional oxidation procedure or post-process steps. The 2D patterns are first defined with traditional ultraviolet (UV) lithography or electron beam lithography. Afterwards, the patterns are transferred into silicon with a modified plasma process, which consists of a DREM (deposit, remove, etch, multistep) process to sculpture structures and an extra isotropic etch step to release the structures. Instead of oxide, a fluorocarbon (FC) layer is used to protect the sidewall during the dry release step. The FC layer is generated directly during the same run by octafluorocyclobutane (C_4F_8) gases, which is a widely used as a passivation gas for Bosch etch processes. Thus, by tuning the etch process parameters during a single run, 3D structures can be created conveniently. This strategy has been tested for both micro- and nanostructures with different pattern designs, e.g. ultralong microcantilever (width of 1.5 μm, thickness of 500 nm and length of 400 μm) and multilayer silicon nanobeams (width of 20 nm, thickness of 50 nm and length of 2 μm) could be fabricated with this method. Besides, up to 10 stacked layers could be achieved showing good size uniformity and mechanical stability. Our approach allows for relatively low fabrication cost and high structure quality, which will open possibilities for novel device designs and applications.

2. Method

The patterns were defined by UV lithography for microstructures and electron beam lithography for nanostructures, and then transferred into silicon by deep reactive ion etching (DRIE). The technical details of the process flow are described as below.

The UV lithography was carried out with maskless lithography (MLA100, Heidelberg Instruments), which is a direct writing system with a high power LED light source (10 W at 365 nm). Different patterns were designed, and the negative photoresist AZ nLOF 2020 (MicroChemicals) was used, resulting in a resolution of resolution of around 1 μm. The thickness of the resist was 1.5 μm, and the dose during the exposure was 220 mJ cm^{-2}.

The electron beam lithography was performed with an electron beam writer (Jeol JBX-9500FS, JEOL) and the resist used was hydrogen silsesquioxane (HSQ, XR 1541 002 from Dow Corning). The thickness of the resist was around 100 nm, the acceleration voltage during exposure was 100 kV and the beam current was set to be 10 nA, which allows a small spot size (below 5 nm) and thus high resolution. The dose was around 20 000 μC cm^{-2}. The HSQ pattern is in many ways similar to silicon oxide and therefor can serve as a hard mask for the subsequent etch process. To verify the critical dimension of the exposed patterns, the samples were characterized by scanning electron microscopy (SEM, Supra V60, Zeiss).

The etching process was performed in an inductively coupled plasma (ICP) etching system (DRIE Pegasus, SPTS), and the processing details will be discussed in details in next section. The sample chips were attached on a carrier wafer, which is a 150 mm single side polished silicon wafer coated with 100 nm thick alumina by atomic layer deposition (R200 ALD system, Picosun). After etching, the samples were cleaned with oxygen plasma in a plasma asher system (TePla 300, PVA TePla).

3. Results and discussions

3.1. 3D silicon microstructures

The basic principle to fabricate 3D silicon micro- and nanostructures is based on the DREM process as introduced in [12]. Briefly speaking, a DREM process is a three-step Bosch process, which enables a better control of etch process [13]. Compared with typical two-step Bosch process with deposition step and etch step, the DREM process introduces a bottom removal step as shown in figure 1(a). During deposition step, C_4F_8 gas is applied without bias to create an almost conformal coating on both sidewalls and the bottom. Subsequently, in the 'removing' step, argon is used with high bias to clean the FC layer in the bottom. Since this step is performed in at low pressure, a high anisotropicity can be achieved and the FC layer on the sidewall remains unaffected. Then SF_6 gas is used to etch the silicon, this step is performed without bias, resulting in a small scallop size limiting sidewall roughness. This special three-step DREM process provides excellent sidewall protection, and, while keeping the scallop size small, a highly anisotropic etch profile can be achieved for freestanding structures.

Having the DREM process, to sculpture anisotropic etch profiles with high sidewall protection, we can now create 3D structures by adding an extra isotropic etch in the total sequence as introduced before in [14–16]. The process flow is shown in figure 1(b). First the patterns were defined by traditional UV lithography, afterwards an anisotropic etch profile was created by a number of DREM cycles, then an isotropic etch was applied to provide an undercut to the anisotropic structures. These structures will then be freestanding and act as a mask for the second round of DREM process steps and another isotropic etch. Since the sidewalls of the anisotropic structures are well protected, the iteration of DREM processes followed by an isotropic etch could be repeated several times, thus more freestanding layers (each layer is defined by one DREM cycle) could be fabricated without collapse of the structure. A technical challenge during the process is the precise control of the geometry of the structures, e.g. to fabricate all the the layers with an identical thickness (i.e. exact same etch depth per cycle independent of the aspect ratio). This is crucial for the fabrication of 3D structures that suitable for practical applications. In our study, this technical issue is solved by applying a process parameter ramping technique.

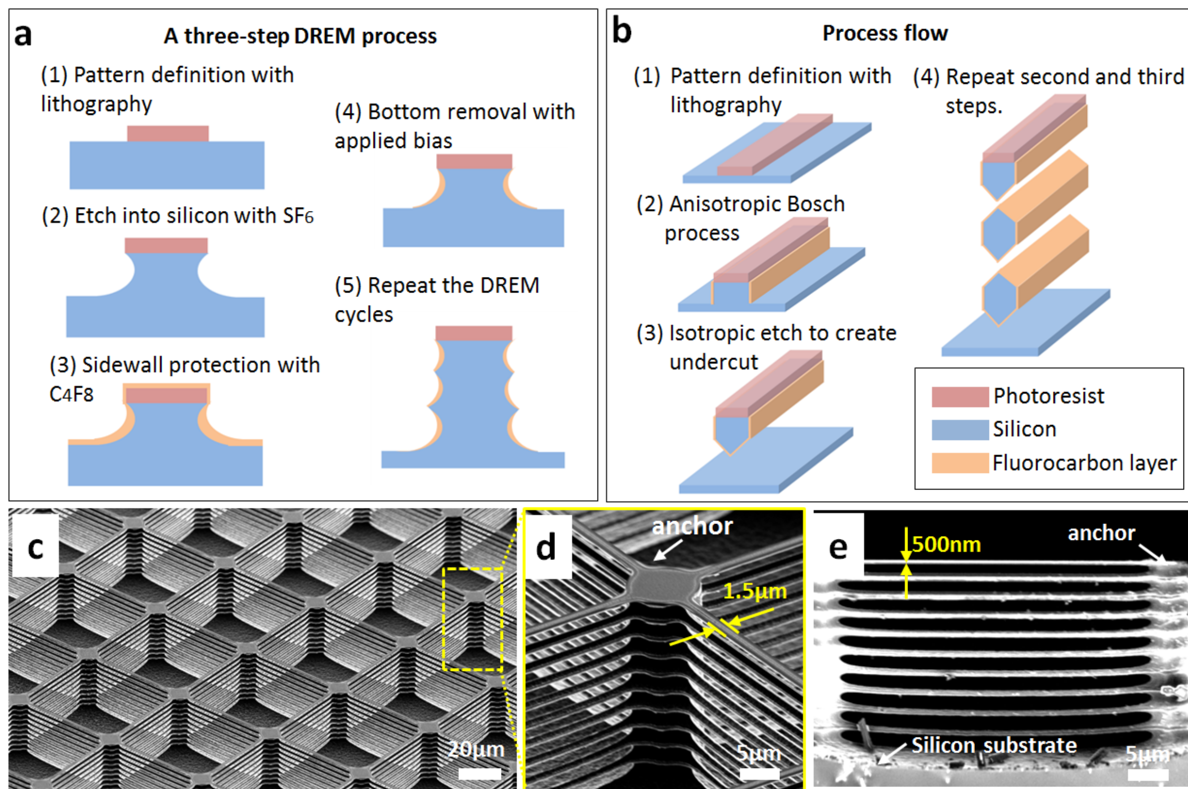

Figure 1. (a) A schematic view of a three step DREM process; (b) process flow for fabrication of 3D silicon structures; (c) SEM image of a 3D silicon microstructures with 10 isolated stacked layers, (d) zoom in of the region in (c), which shows the anchor part that holds 10 stacked silicon beams, (e) a cross section view of the 3D silicon structures.

The process parameter ramping technique has been introduced in a previous paper [12], in which a sausage-chain-like micropillar structures were fabricated. It is well known that the etch rate of silicon is aspect ratio dependent, the effect is known under ARDE (aspect ratio dependent etch rate) or sometimes just referred to RIE lag [17, 18]. In our case, both the etch rate during each cycle of the DREM process and the isotropic etch rate will slowly decrease as the etch process progresses down into the silicon. This causes a decreasing size of the scallops, which we documented in a previous study [12]. This issue becomes particularly significant when we want to create a number of suspended (freestanding) layers. To compensate for this effect, we slowly increase the time of the etch cycle in our DREM process, so the scallop size will be constant down into the silicon, and an excellent thickness uniformity of the different suspended layers can be achieved. At the same time, the duration of the isotropic etch cycle is also increasesed, thus the size of the gap between each two suspended layers is identical. This parameter ramping procedure is crucial in order to have precise size control of the fabricated 3D structures, which is otherwise difficult and cumbersome with alternative fabrication techniques. All the parameter settings are shown in table 1.

Figure 1(c) is a SEM image of a 3D silicon microstructure fabricated with the presented DREM, and isotropic etch process, consisting of 10 suspended layers of beam structures supported by pillars, which are larger in size and act as anchors, so the isotropic etch step will not undercut and release the whole structure. An enlarged view is shown in figure 1(d), where we can clearly see the suspended beams (with a width of 1.5 μm, and length of 50 μm), and the vertical supporting anchors (with a diameter of 10 μm). A cross section view is shown in figure 1(e), where we can see the suspended beams, which have a uniform thickness of around 500 nm, and the gaps between each two suspended layers also have a uniform size of around 2.5 μm.

By applying the fabrication technologies discussed above, different kinds of freestanding structures can be fabricated. In figure 2 there are three kinds of structures etched from the same mask design, which is a double spiral structure with anchors and beams (with a linewidth of 2 μm). Three different fabrication sequences were applied as shown in figure 2(d). Figure 2(a) shows a cantilever like beam structure, which is fabricated by 10 cycles of the DREM process followed by an isotropic etch release. Figure 2(b) shows capacitor-like structures, which are etched by 50 cycles followed by a final isotropic etch step. Figure 2(c) shows five isolated structures, each layer is etched with 10 cycles of the DREM process followed by an isotropic etch, giving a thickness of around 2 μm for each isolated layer. From the results we can see the flexibility of this approach, which makes fabrication easy to program for different applications. However, it should be noted that, in order to have a uniform size distribution of different suspended layers, the etch speed should be controlled precisely, so the scallop size distribution is uniform (as shown in figure 3(e)). This is accomplished by the parameter ramping technique discussed earlier.

By designing the patterns properly, different structures with complicated pattern designs can be fabricated as presented in

Table 1. An overview of parameter settings to create 3D silicon microstructures.

	DREM process step			
	Deposition	Bottom removal	Etch	Isotropic etch step
Time (s)	1.0	0.5	Ramping up from 2.5 s ramping rate: 0.5 s/cycle	Ramping up from 10 s ramping rate: 0.5 s/cycle
C_4F_8 gas flow (sccm)	400	5	5	5
SF_6 gas flow (sccm)	15	15	600	600
Argon gas flow (sccm)	250	75	250	250
Coil power (W)	3000	3000	3000	3000
Platen power (W)	0	300	0	0
Pressure (mTorr)	20	5	20	20
Temperature (°C)	−19	−19	−19	−19

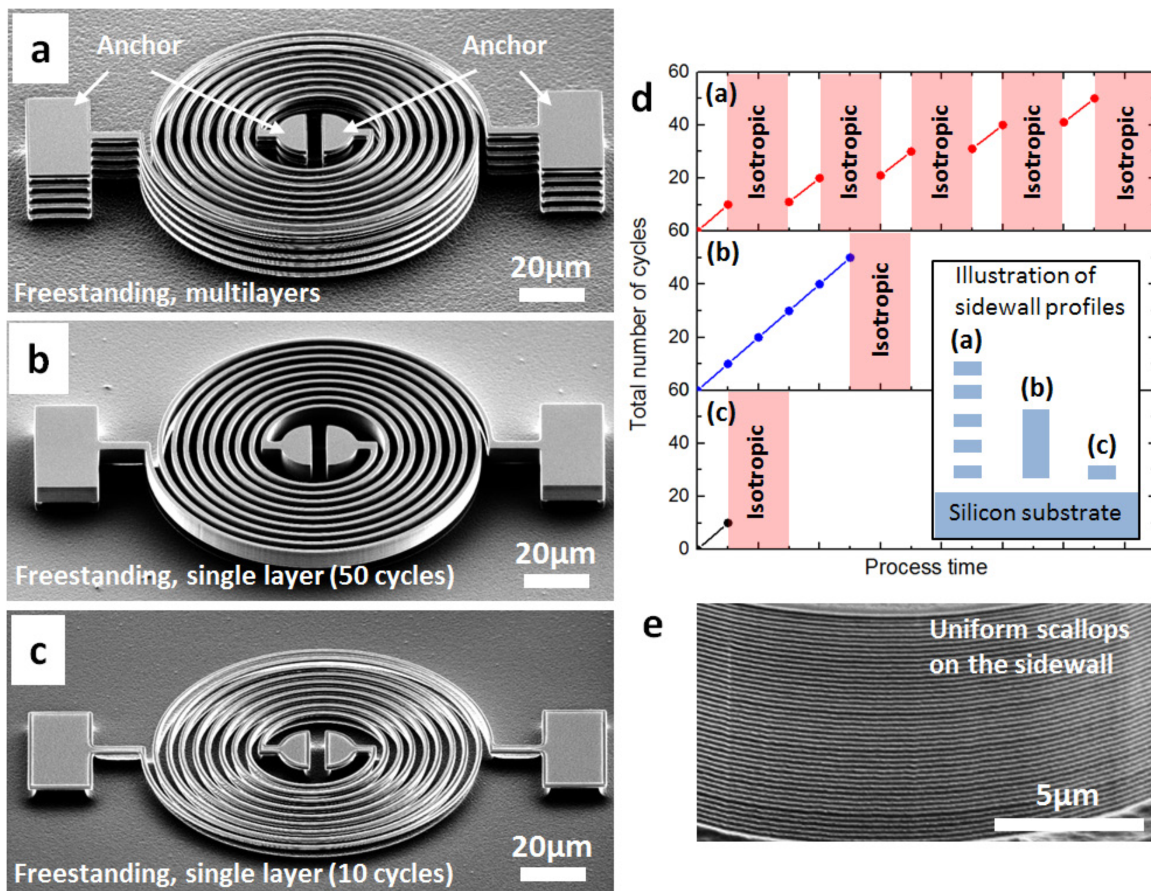

Figure 2. Different strategies to create freestanding structures: (a) one suspended layer which consists of 10 Bosch cycles; (b) one suspended layer which consists of 50 Bosch cycles; (c) five suspended layers, each layer consists of ten Bosch cycles; (d) a schematic view of the processes in (a)–(c), and an illustration of cross section view of the structures in the inset; (e) a zoom in view of the scallops on the sidewall of structures in (b).

figure 3. Five sequences of ten DREM cycles each followed by an isotropic etch were performed in (a)–(c). Figure 3(a) shows arrays of spiral-like structures with the anchor in the middle, the linewidth of the suspended beams is 2 μm, and the gap between the beams is 2 μm. Figure 3(b) shows arrays of stacked ring resonator-like structures with different diameters, the linewidth of the ring is 2 μm. Figure 3(c) shows arrays of tuning fork-like structures with different length from 20 μm to 200 μm, the linewidth of the suspended beams is 2 μm. An enlarged section of the image is shown for each structure, which gives more details regarding the isolated layers. In figure 3(d) we show a 3D photonic crystal-like structure, which is created by six sequences of five DREM cycles each followed by an isotropic etch. The fabricated structure has six stacked layers of holes with a square lattice type, the diameter of the holes is 3 μm and the periodicity is 4 μm (an enlarged view of the structures are shown in figures 3(e) and (f)). A simple illustration is also shown in the bottom left corner of the image to show the anchors (blue) and suspended structures (yellow). This figure shows the flexibility of our fabrication

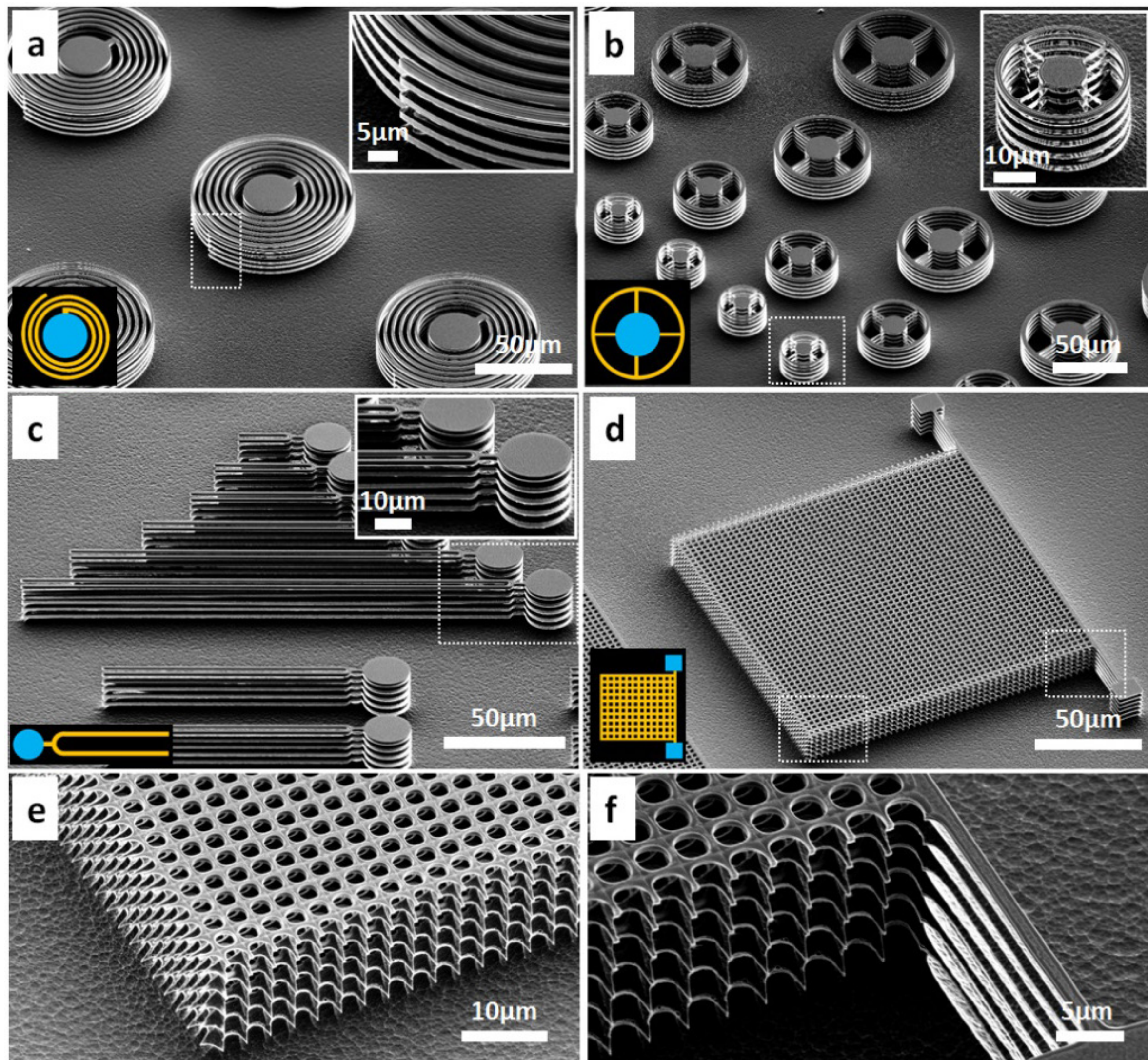

Figure 3. SEM images of different complex 3D microstructures (from (a) to (d)). A schematic view (bottom-left corner in each image) shows the anchor parts (blue) and the stacked layer parts (yellow). Zoomed in images are shown in the insets (top right corner) in (a)–(c), which show the details of the parts in dashed squares in the SEM images. Figures (e) and (f) are zoom in images from two regions labeled in (d).

technique, it also implies possibilities for various applications in photonics [19], micromechanics [20], etc.

It should be noted that the bottom part of anisotropic structures will be consumed slowly upwards during the isotropic etch step, which will change the thickness of the suspended structure and additional calculations are thus needed to have a precise size control of these structures. To illustrate the demolishing effect of isotropic etch on anisotropic structures, a wheel-like pattern with diameter of 500 μm is designed as shown in figure 4(c). The rim of the wheel and the 'spokes' have a linewidth of around 2 μm, and the whole structure is supported by an anchor in the center, which has a diameter of 15 μm. In the experiments, 20 DREM cycles were first applied to create anisotropic structures, and then an isotropic etch was applied with different durations of 10 s, 20 s and 30 s. It is found that the number of remaining scallops on the anisotropic structures decrease linearly with increased isotropic etch time (figures 4(a) and (b)), which suggested a constant isotropic etch rate into the structures of 60 nm s^{-1} (in the anchor region) and 80 nm s^{-1} (in the rim region) as shown in figure 4(d). This phenomenon canbe explained qualitatively as follows: while the sidewall of the anisotropic structures is well protected by the FC layer, SF_6 based etching species will etch isotropically and undercut structures, thus the bottom of the structure is exposed to fluorine radicals and slowly gets thinner. This process is geometry (shape) dependent, resulting in the fact that the spokes and rims will be attacked from different directions after being released, thus the etch rate into structures will be higher than in the central support, where the isotropic etch can only attack the structure from one side. This phenomenon is important, since it will determine both the thickness of suspended structures and the size of the gap between two adjacent suspended layers, which are two important parameters to design 3D structure based devices. The anisotropic structures will be slowly etched away from the bottom, this will give a contribution to the final size of the

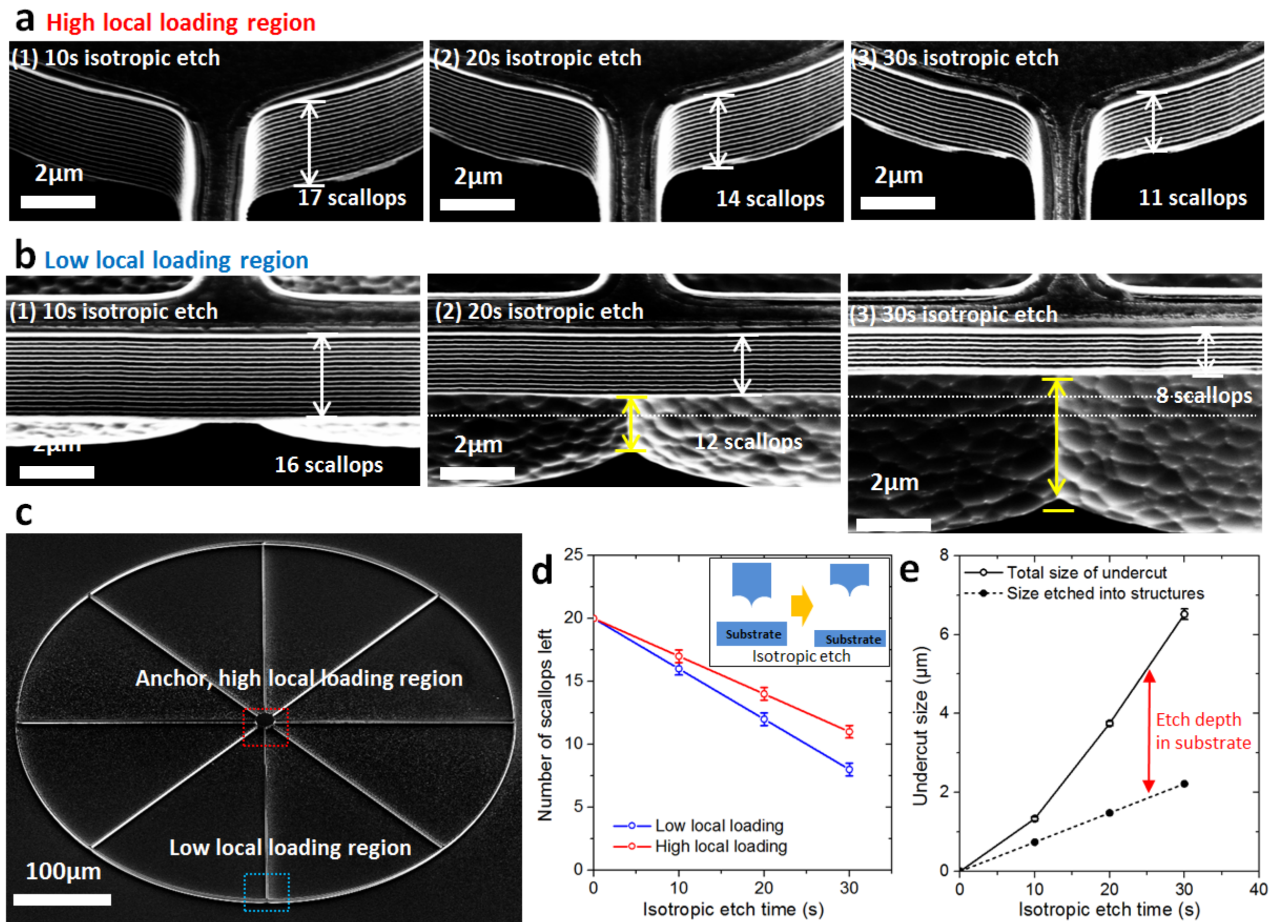

Figure 4. The influence of isotropic etch on freestanding structures. For regions with single-side isotropic undercut (a) and double-side isotropic undercut (b) with different isotropic etch time. The regions in (a) and (b) correspond to regions in the structure as shown in (c). The isotropic etch rates of the scallops being etched are shown in (d), with a schematic view of the structure change after isotropic etch process. The gap size between freestanding structures and the substrate is shown in (e).

gap (figure 4(e)) and thus should be considered during design. To give a practical example, in some cases a large gap size is favored, to achieve this, we should not just increase the isotropic etch time, since it will totally demolish the anisotropic structures. A more proper way, however, is to increase the number of cycles during the Bosch process, and in the same time increase the isotropic etch time.

By precisely controlling the isotropic etch step, we can fabricate some ultralong cantilever-like structures, which normally require silicon on insulator (SOI) wafers. In the latter the buried oxide layer is removed after the plasma etch. To prevent the structures from collapse due to the capillary force [21], some special techniques are needed, e.g. critical point drying after hydrofluoric (HF) solution removal [22], XeF_2 etching [23], vapor phase HF etching [24], or a C_xF_y-based plasma chemistry removal [25]. In our experiments, the undercut is created directly during the plasma etching process, thus the stiction effect can be avoided. Figure 5(a) shows two sets of cantilever structures, which were fabricated by 20 cycles of DREM followed by 22 s of isotropic etch. The width of the cantilever is around 1.5 μm (figure 5(b)), and the thickness of the cantilevers is around 300 nm, the lengths of the cantilevers are from 50 μm up to 500 μm, and they are completely free-hanging above from the substrate (figure 5(c)). The tips of fabricated cantilever beams are also observed to clamp on the substrate during the scanning with SEM (figures 5(d) and (e)), which can be explained as the electrostatic attraction force caused by the charge accumulation on beams and substrates. This implies potential applications for switches and electrostatic actuations [26, 27]. This type of long cantilevers with thin thickness have also been demonstrated to have small spring constants to detect small forces [28] or to measure the mechanical properties of thin films coated on silicon [29]. This strategy is also promising to be fabricate free standing electronic devices, e.g. transformers and inductors [30].

3.2. 3D silicon nanostructures

While 3D microstructures can already bring new possibilities and applications in micromechanics, microelectronics, microfluidics, etc, to shrink the size further and create 3D nanostructures can give us novel insights into fundamental phenomena. This becomes very relevant when the CD of the structures is comparable to or below the wavelength of light, the mean free path of electrons or the electron phase coherence lengths. Compared with the methods to fabricate 3D silicon microstructures as discussed above, some additional technical issues need to be addressed for nanoscale, and the

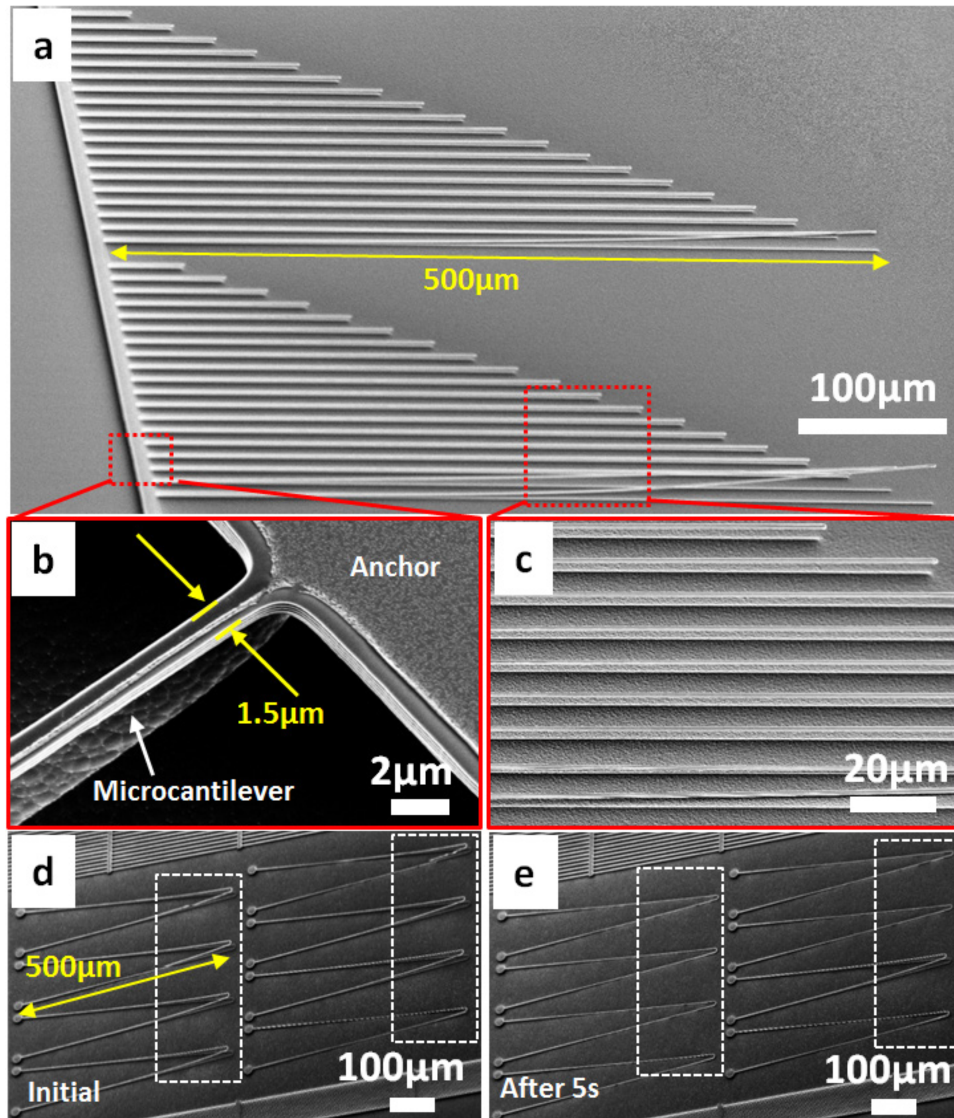

Figure 5. Ultralong silicon micocantilevers created with 20 DREM cycles followed by 22 s isotropic etch. (a) Cantilevers with length up to 500 μm; (b) an enlarged view of the anchor region of the cantilevers; (c) an enlarged view of the center of the cantilevers. Attaching phenomena for ultralong silicon microcantilevers under SEM, the initial morphology (d) and after 5 s (e).

major challenge is to have a profile control with higher precision, which is limited by the plasma etch process. Since the CD of the nanostructures can be below 100 nm,which is even smaller than the scallop size for already presented microstructures, the recipe has to be adapted to the these dimensions. Should the same recipe be applied as used for the microstructures, the large scallops and undercut will completely dissolve the nanostructures. In order to produce 3D nanostructures with this approach the etch rate needs to be significantly reduced, so that the sizes of scallops and undercuts can be minimized.

In table 2 we can see the parameter settings to create 3D nanostructures. In order to reduce the etch rate, the density of radicals should be decreased, thus a smaller coil power of 500 W is applied, and the gas flow ratio of SF_6 is also reduced [13]. By doing so a scallop size of around 15 nm could be achieved (compared with the large scallop size of around 200 nm for microstructures). The platen power is also reduced during the bottom removal step of DREM process, which helps to reduce the roughness caused by resputtering, which is more crucial for nanostructures. The parameter ramping technique was not performed for the nanostructure etching, since

Table 2. An overview of parameter settings to create 3D silicon nanostructures.

	DREM process step			
	Deposition	Bottom removal	Etch	Isotropic etch step
Time (s)	0.4	1.0	2.5	1
C_4F_8 gas flow (sccm)	40	5	5	5
SF_6 gas flow (sccm)	10	10	30	30
Argon gas flow (sccm)	100	75	100	100
Coil power (W)	500	500	500	500
Platen power (W)	0	80	0	0
Pressure (mTorr)	6	3	6	6
Temperature (°C)	−19	−19	−19	−19

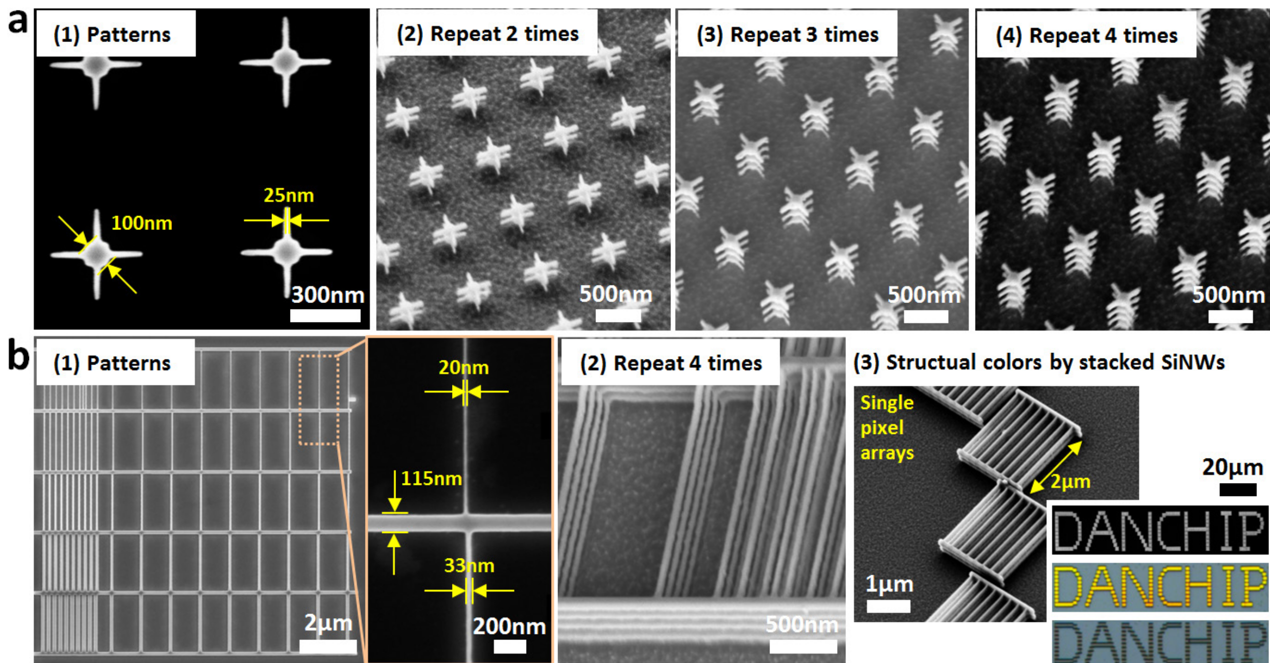

Figure 6. Fabrication of 3D silicon nanostructures: (a) cross-like structures defined by electron beam lithography (1), after plasma etching to create different number of stacked layers as shown in (2)–(4); (b) SEM images of SiNWs structures patterned by electron beam lithography (1), four stacked layers of SiNWs after etching (2), and single pixels made by two stack layers of SiNWs in (3), which can be used to make a graph that gives structural colors as shown in the bottom right corner, from top to bottom: SEM images, optical microscopic graph when the incident light polarization is perpendicular to the direction of SiNWs, and the optical microscopic graph when the incident light polarization is along the direction of SiNWs.

for nanostructures the aspect ratio is not as large as for the microstructures, thus the ARDE or RIE-lag is less prominent.

Some 3D silicon nanostructures are shown in figure 6. Electron beam lithography was used to define the high resolution patterns, which include cross-like structures (figure 6(a)(1)) and nanowire structures (figure 6(b)(1)), the smallest size of the patterns is around 20–25 nm, and larger patterns are defined to act as anchors for the suspended 3D structures. After several iterations of DREM and isotropic etch, 3D nanostructures are created from cross-like patterns (two stacked layers in figure 6(a)(2), three stacked layers in figure 6(a)(3), four stacked layers in figure 6(a)(4)), and nanowire patterns with four stacked layers in figure 6(b)(2). Five DREM cycles were applied during each anisotropic etch part, thus giving a height of around 50–60 nm for each layer of nanostructures, and the size of the gap between each two layers is around 50 nm. The line edge roughness (LER) of the HSQ patterns is measured to be below 3 nm, and the sidewall roughness is minimized by reducing the etch rate, thus the fabricated silicon nanowires (SiNWs) arrays in figure 6(b)(2) show a very good size uniformity, which is favorable for applications in nanophotonics and nanoelectronics, where the exact geometry of the structures is crucial. To briefly demonstrate one possible application of the 3D SiNWs, pixels were written (with pixel size of 2 μm by 2 μm) to form a graph, each pixel is composed of two stacked layers of SiNWs with linewidth of 50 nm, height of 50 nm, length of 2 μm and pitch of 300 nm as in figure 6(b)(3).These SiNWs have been shown previously to possess size and polarization dependent light scattering properties, which can give enhanced light scattering intensity in certain wavelength regions [31, 32, 33]. In figure 6(b)(3), we can see such pixels could be used to write patterns with a high spatial resolution of around 10 000 dpi (dots per inch), which can give bright yellow structural colors when the polarization of light is perpendicular to the direction of SiNWs. When the polarization is rotated by 90°, the resonance mode is not active and thus no structural colors can be observed. Compared with previous studies on structural colors induced by light scattering of SiNWs [28, 29], our method does not rely on a complicated SOI structure, and the coupling of resonance mode from adjacent SiNWs could be extended to an extra dimension. Technical details of these light scattering properties of 3D SiNWs, however, is out of the scope of this paper and will be reported elsewhere.

4. Conclusion

3D silicon freestanding structures have been fabricated with a modified DREM (deposit, remove, etch, multistep) etch process without additional steps such as oxidation or wet releasing. Micro- and nanostructures were fabricated with excellent control of size uniformity and a maximum number of 10 stacked suspended layers. The process is reproducible and easy to program for different kinds of freestanding structures. Technical issues have been addressed and a three-step DREM process combined with parameter ramping, has been introduced. Some potential devices and applications have

been demonstrated, more practical applications based on this technique are under investigation.

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Confined Growth of ZIF-8 Nanocrystals with Tunable Structural Colors

*Bingdong Chang, Yuanqing Yang, Henri Jansen, Fei Ding, Kristian Mølhave, and Hongyu Sun**

Zeolitic imidazolate frameworks (ZIF-8) have promising applications as sensors or catalysts due to their highly porous crystalline structures. While most of the previous studies are based on ZIF-8 crystals either in isolated particles in aqueous environments or in a compact colloidal form, here a facile method is reported to achieve wafer-based isolated ZIF-8 nanocrystals to facilitate their integration in microsystems and as surface coatings for catalysis. The fabrication process includes the growth of compact zinc oxide film by atomic layer deposition that functions as the Zn source for the ZIF-8 synthesis, and the dispersion of gold nanoparticles as inhibitors for the following crystallization transformation of ZIF-8 crystals. By choosing the concentration of gold nanoparticles, the density of ZIF-8 nanocrystals can be controlled and the sizes of individual ZIF-8 crystals can be scaled down to ≈100 nm. A wide range of structural colors generated by the ZIF-8 nanocrystals is also observed, which can be attributed to the size-dependent resonant scattering as verified by finite-difference time-domain simulations and classical Mie theory. The scalable fabrication of wafer-based ZIF-8 nanocrystals empowered with tunable optical properties paves a new way to explore the promising applications in nanophotonics and bionanotechnology.

1. Introduction

Metal–organic frameworks (MOFs) have been widely studied in recent years due to their unique structures and applications in environment and energy. As a typical MOF, zeolitic imidazolate framework-8 (ZIF-8) possesses a 3D zeolite crystal structure which is constructed by bridging zinc ions with methylimidazolate (MeIm) ligands. Compared with other ZIF structures, ZIF-8 crystals have a large cavity size (11.6 Å), small connecting apertures (3.4 Å), and high thermal/chemical stability, which makes them outperform other MOF structures in a wide range of applications, including heterocatalysis,[1,2] low-κ dielectrics microelectronic devices,[3] and gas adsorption.[4]

The crystallization of ZIF-8 requires both zinc ion sources and imidazolate linkers. Traditional bulk synthesis methods have been well studied and established.[5–9] In the synthesis, soluble zinc salts ($Zn(NO_3)_2$, $ZnSO_4$, $ZnCl_2$, etc.) are used to provide zinc ions. But the produced powder ZIF-8 crystals are difficult to integrate into micro- or nano-electromechanical systems (MEMS or NEMS), where a mechanically robust structure is preferred. Recent studies show that ZnO nanostructures (nanoparticles, nanowires, or nanofilms) can also be used as zinc ion sources to direct the growth of ZIF-8 crystals, which inherit the initial morphology of ZnO nanostructures. For example, polycrystal ZIF-8 thin films can be fabricated by converting ZnO layer grown either by atomic layer deposition (ALD) or sputtering.[10] By combining metal oxide vapor deposition and consecutive vapor solid reaction, ZIF-8 thin films with high quality can also be deposited using only gas phase reactions.[11] Based on the compact ZIF-8 films, traditional top-down micro- and nanofabrication techniques (such as standard photolithography[12] and nanoimprint lithography[13]) can be employed to pattern the ZIF-8 crystals in a regular manner.

It has been shown that a photochemical sensor can be created by integrating ZIF-8 nanofilms with plasmonic materials, e.g., gold or silver nanostructures, the plasmonic adsorption can be modulated.[14] A large optical nonlinearity of ZIF-8 materials has also been demonstrated,[15] making it a promising candidate for many emerging optical applications. In this paper, we explored the resonant optical properties of wafer-based isolated ZIF-8 crystals with nanoscale dimensions. The ZIF-8 structures were synthesized from ZnO films deposited using ALD, and gold nanoparticles (Au NPs) were used to confine the crystallization of ZIF-8 structures, thus in a way "patterning" the ZIF-8 structures and thereby resulting in isolated ZIF-8 nanocrystals. The smallest size of the fabricated ZIF-8 crystals can be controlled down to ≈100 nm with well-defined rhombohedral or

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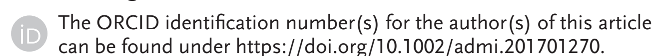
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rhombic dodecahedron morphologies. The synthesized ZIF-8 nanocrystals exhibited broadband scattering resonances in visible wavelengths, which gave prominent structural colors. Besides, an evident redshift of structural colors was observed to be correlated with increasing sizes of single ZIF-8 nanocrystals. Such size-dependent resonant scattering behavior is of central importance for the applications in nanophotonics and bionanotechnology.[16–20] By presenting a facile fabrication method of wafer-based ZIF-8 nanocrystals and revealing their fundamental light scattering properties, we believe our work can provide new possibilities for dielectric ZIF-8 nanostructures functionalized to have favorable optical properties.

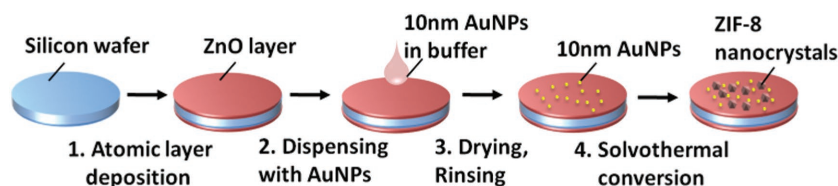

Figure 1. Schematic illustration of converting ZIF-8 nanocrystals from ALD grown ZnO layer, with steps of ALD, Au NPs dispensing and solvothermal synthesis.

2. Results and Discussion

Figure 1 shows a schematic illustration of the process flow in which three steps are included to fabricate ZIF-8 nanocrystals, i.e., growth of ZnO film via ALD, dispersion of Au NPs, and subsequent solvothermal conversion. The representative scanning electron microscopy (SEM) images of the samples are shown in **Figure 2**. SEM measurement of the thickness of the initial ZnO film was determined to be 157 nm (Figure S2, Supporting Information) after 1000 cycles of deposition, and the atomic force microscopy (AFM) measured root mean squared (RMS) roughness was ≈6 nm (Figure 2a, and Figure S1a in the Supporting Information). Without the addition of Au NPs, the surface of ZnO was fully transformed into a ZIF-8 colloidal film, with a normal size distribution and an average grain size

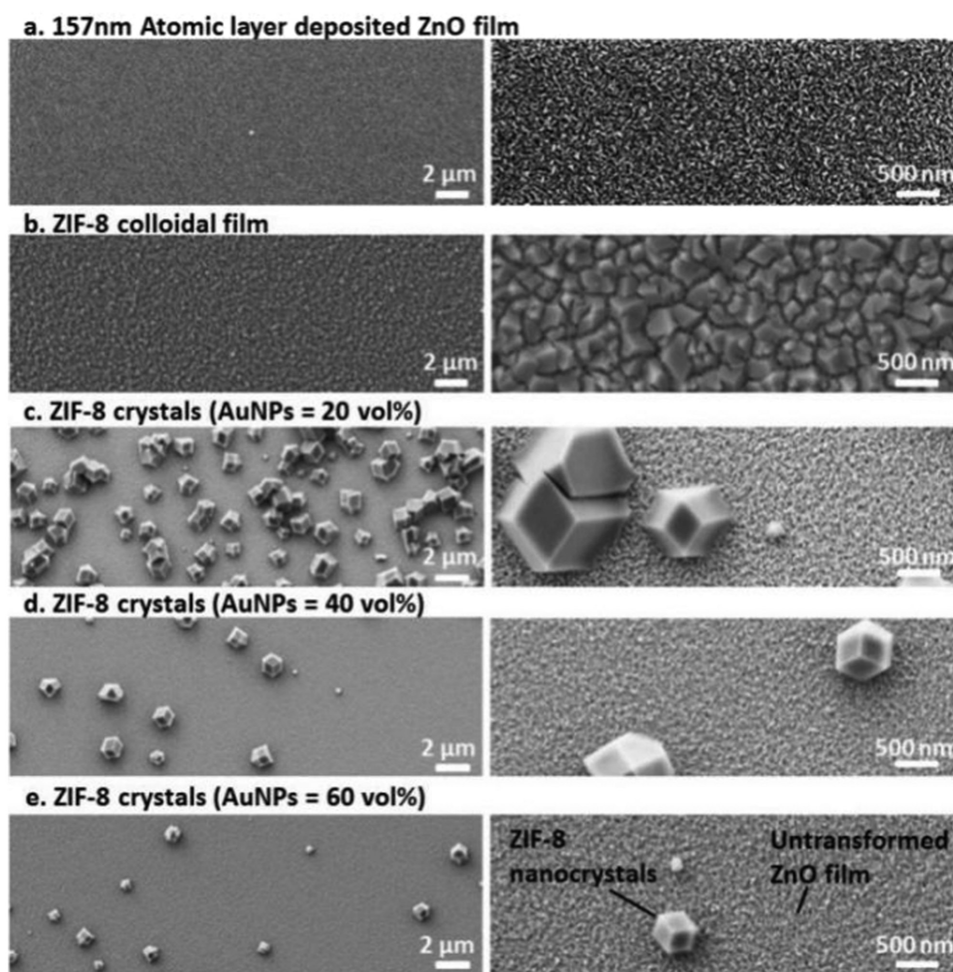

Figure 2. Low-magnification (left column) and high-magnification (right column) SEM images of the samples. a) 157 nm ZnO layer deposited by ALD on silicon substrate; b) fully transformed ZIF-8 nanocrystals from ZnO film without the addition of Au NPs; partially transformed ZIF-8 crystals from ZnO film with different Au NPs concentrations: c) 20 vol%, d) 40 vol%, and e) 60 vol%.

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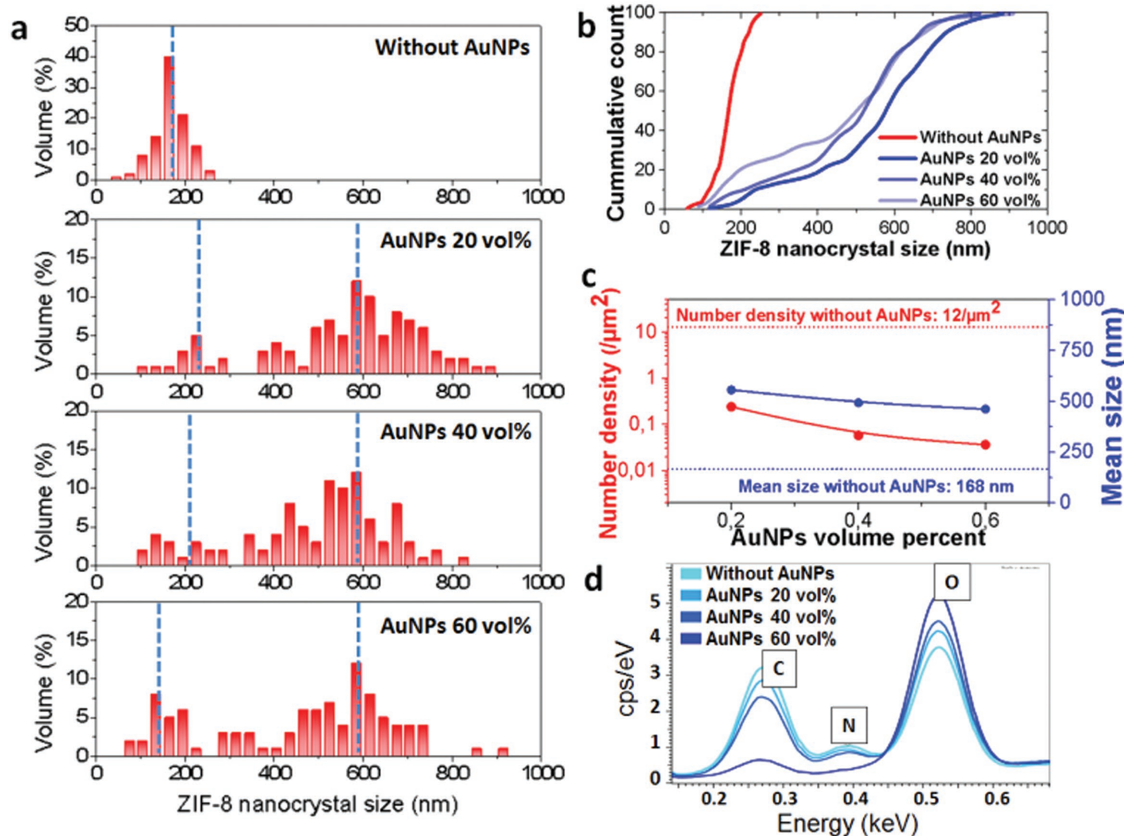

Figure 3. a) Particle size distributions for ZIF-8 nanocrystals with different concentrations of Au NPs; b) cumulative plot for different concentrations of Au NPs, which shows a size reduction when the concentration of Au NPs increases; c) spatial densities and average sizes of ZIF-8 nanocrystals; d) EDX element analysis of C, N, and O, which shows a decreasing density of ZIF-8 nanocrystals when increasing the Au NPs concentrations.

of ≈168 nm as shown in **Figure 3**a. Here, the size of ZIF-8 nanocrystals is defined as the side length in our discussions and following simulations. The surface and cross-section morphology of ZIF-8 colloidal film was directly mapped with AFM (Figure S1b, Supporting Information) and SEM (Figure S2b, Supporting Information). The transformation from the pristine ZnO to ZIF-8 colloidal film was also confirmed by both surface sensitive X-ray photoelectron spectroscopy (XPS) element analysis (Figure S3, Supporting Information) and energy dispersive X-ray spectroscopy (EDX) measurements (Figure S2c, Supporting Information). The XPS results suggest the existence of carbonates and water/hydroxyl groups on the film surface, and the EDX spectra verify the existence of carbon and nitrogen elements in the converted sample. The elemental analysis is in good agreement with previous studies.[21] When Au NPs with different concentrations (20, 40, and 60 vol%) were predispersed on ZnO film, the sizes of ZIF-8 nanocrystals exhibited a bipolar distribution, which consists of larger crystals with average size of ≈600 nm and smaller ones with mean size of ≈200 nm (Figure 3a and the detailed description in the Supporting Information). Moreover, the proportion of smaller crystals is slightly increased with increasing Au NPs concentration (Figure 3b). The similar results can also be found in different ZIF-8 samples that obtained by changing the thickness of initial ZnO film or substrates (Figure S4, Supporting Information). The number density of ZIF-8 nanocrystals decreases with a higher concentration of Au NPs as shown in Figure 3c, and this decreasing spatial density is verified by EDX analysis, which suggested a decreasing proportion of nitrogen and carbon elements when Au NPs with higher concentration were used (Figure 3d). The confined growth of ZIF-8 nanocrystals is further confirmed by AFM measurements (Figure S5, Supporting Information). The results show that the concentration and coverage of Au NPs on ZnO film are crucial for the subsequent conversion of ZIF-8 nanocrystals. For comparison, we discussed the distribution of Au NPs before solvothermal reactions (Figure S6, Supporting Information).

This variation of size distribution of ZIF-8 nanocrystals is related to surface nucleation and spreading growth process.[22] The interaction between ZnO film and solvents facilitates the deprotonation of MeIm ligands and thus reduces the pH value in solution.[23] The solvated zinc ions, together with $MeIm^-$ are two basic monomeric building units, which will be added sequentially in a metastable manner and crystallize into an enclosed framework structure. When the citrate stabilized Au NPs are introduced, the hydrogen bond donation ability of the solvent is assumed to be limited, which prevents the coordination between Zn ions and nitrogen from imidazole groups.[23] Thus the crystallization of ZIF-8 is inhibited where Au NPs are present, and the nucleation and spreading process are confined in specific regions, where the influence of Au NPs is less pronounced. The particle size distributions show a

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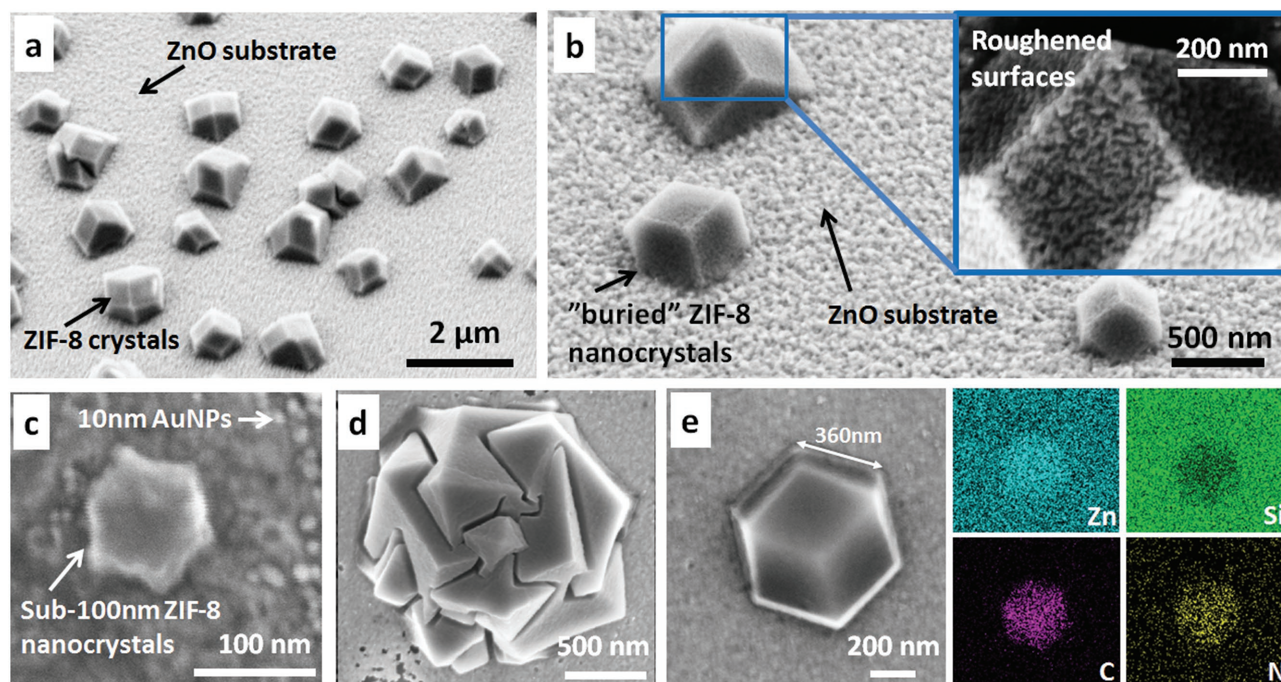

Figure 4. Surface morphology of isolated ZIF-8 nanocrystals with a) 45° tilted view of ZIF-8 crystals on the surface of ZnO; b) a closer view of ZIF-8 nanocrystals shows a roughened surface; c) an isolated sub-100 nm ZIF-8 nanocrystal and 10 nm Au NPs; d) coalescence of multiple ZIF-8 crystals; e) asymmetric rhombic dodecahedron caused by truncated growth in [–110] direction. The EDX element mapping of a typical ZIF-8 single nanocrystal in (e), which shows the distribution of Zn, Si, C, and N elements. The concentration of Au NPs is 60 vol%.

defocusing trend with the increasing of Au NPs concentration (Figure 3a). This nonuniform size distribution can be explained by a focusing of size distribution in the early stage of crystal growth, followed by defocusing of size distributions caused by the further growth of larger ZIF-8 crystals in later stage.[24] In our experiments, the crystal growth and coalescence processes are confined by Au NPs, which "define" the sizes of ZIF-8 nanocrystals. Since the Au NPs were manually dispersed on the ZnO film, the particle distribution is not perfectly uniform, which affects the growth of ZIF-8 nanocrystals and results in a broad size distribution. Therefore, by precisely controlling the size and location of Au NPs via the methods such as Langmuir–Blodgett assembly or spin coating, might be a way to further tune the dimension of ZIF-8 crystals.

For a high concentration of Au NPs of 60 vol%, isolated single ZIF-8 nanocrystals are formed and embedded in the substrate (**Figure 4**a), and the surface roughness can be clearly distinguished (Figure 4b). These nanocrystals exhibit a well-defined rhombohedral or rhombic dodecahedron morphology (Figure 4a,b), and sizes below 100 nm were presented (Figure 4c). The crystallization of ZIF-8 crystals starts with a higher growth rate on {111} crystalline planes as compared with {110} and {100} planes, thus giving a cubic shape exposed with {100} facets.[24,25] Then the growth rate on {100} planes dominates on the other two planes, resulting in the transformation from the initial cubic form into twofold symmetric rhombic dodecahedra structures with a higher thermal stability.[24,25] Since ZnO layer deposited by ALD is polycrystalline, some clusters of ZIF-8 crystals could also be found (Figure 4d), indicating a coalescence-growth process of smaller ZIF-8 crystals. EDX elemental mapping analysis confirms the uniform distribution of both N and C elements inside the region of rhombic dodecahedron structures (Figure 4e). The appearance of Au NPs in the converted ZIF-8 colloidal film is examined. When the concentration of Au NPs is 20 vol%, the EDX signal from Au NPs is difficult to be detected, while for a high concentration of 60 vol%, ZIF-8 nanocrystal and Au NPs coexist as shown in Figure S7 (Supporting Information). Besides Au NPs, we also studied the role of silver nanoparticles (Ag NPs, average diameter 10 nm) on the conversion of ZnO to ZIF-8 crystal. Different from Au NPs, the initial ZnO films transformed uniformly into ZIF-8 crystals with the addition of Ag NPs (Figure S8, Supporting Information), i.e., no confined growth is observed in the case of Ag NPs, which may arise from the different affinity between the metal NPs and zinc–nitrogen coordination. In the future, more experiments should be performed to determine the effect and mechanism of metal NPs addition in the ZIF-8 synthesis.

Next, we study the optical properties of the synthesized ZIF-8 nanocrystals by investigating their light scattering properties with dark field optical microscope. A fused silica wafer was used as the substrate, which is transparent in the ultraviolet and visible spectral ranges. A silicon carrier wafer (150 mm) was used to prevent the conformal growth of ZnO on backside of fused silica wafer. A thinner ZnO layer with a thickness of 60 nm was deposited in order to make sure that all the ZnO was reacted and the substrate was purely optically transparent silica. The surface was mapped by EDX analysis after solvothermal reaction, which shows ZIF-8 crystals and silica substrate (Figure S9, Supporting Information). A typical direct dark field image (**Figure 5**a) shows a variety of colors that are produced

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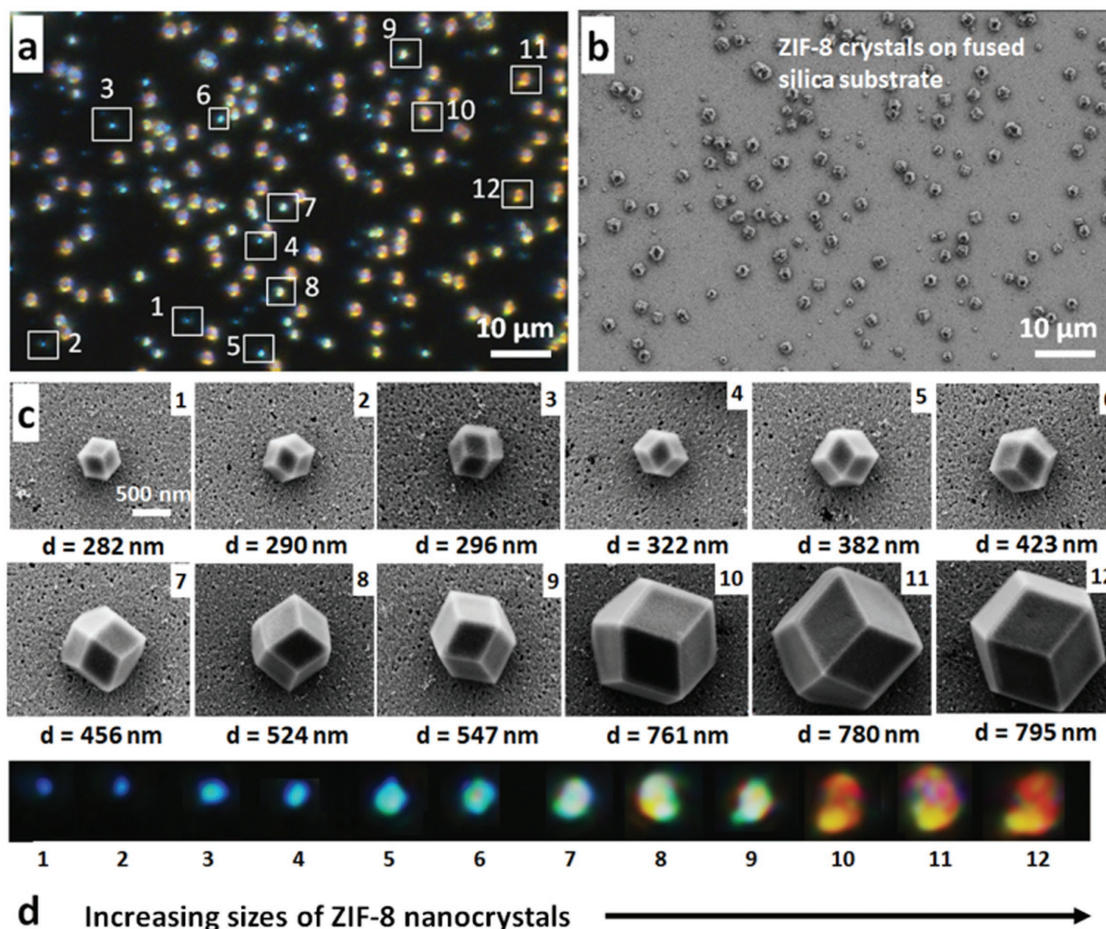

Figure 5. Light scattering and structural color of ZIF-8 crystals fabricated with the addition of 60 vol% Au NPs. a) Dark-field optical microscope images of ZIF-8 nanocrystals on a fused silica wafer; b) SEM image of the corresponding area in (a); c) SEM images of ZIF-8 nanocrystals with different size; d) structure colors of ZIF-8 crystals corresponding to (c).

by the ZIF-8 crystals. Corresponding SEM image (Figure 5b) demonstrates the specific dimensions and orientations of the crystals, indicating a strong dependence of the different colors on the particle geometry. To verify this relation, dark field scattering of individual ZIF-8 nanocrystal with different size was studied as illustrated in Figure 5c,d. One can clearly see that the scattered light is shifted from deep blue color to red color with the increasing sizes of the ZIF-8 nanocrystals.

To fully analyze the progressive color evolution with the crystal size, we performed finite-difference time-domain (FDTD) simulations to calculate the optical response of individual ZIF-8 nanocrystals (**Figure 6**). A total-field scattered-field method was exploited to reduce computation effort and provide both near field profiles and far-field scattering spectra. A refractive index of 1.59 was adopted for ZIF-8 nanocrystals in our simulation.[15,26,27] Scattering response of rhombic dodecahedral and cubic nanocrystals are studied with different side lengths ranging from 300 to 800 nm. We would like to note that these two shapes were chosen because the fabricated ZIF-8 crystals actually possess transitional morphologies between them. Given the high rotational symmetry of these two shapes, only specific orientations are considered for simplicity, as shown in Figure 6a. In Figure 6b,e, scattering efficiency Q_{scat} is defined as the ratio of the scattering cross section to the geometric cross section. When $Q_{scat} > 1$, it indicates an enhanced scattering process induced by an efficient light-matter interaction. This enhanced scattering phenomenon can be found in most spectral regions of ZIF-8 nanocrystals with sizes larger than 300 nm, covering the entire visible range. Substantial red shifts of scattering peaks with increasing crystal size can also be readily seen in these scattering spectra, which is in good accordance with the above dark-field observations. To further prove the tunable optical resonances supported by the ZIF-8 nanocrystals, we performed a proof-of-principle experiment to measure the spectroscopic response of certain regions of ZIF-8 crystals with relatively uniform size. Reflection and transmission spectra were measured by using ellipsometry and linear spectroscopy respectively, as shown in Figure S10 (Supporting Information). Due to the spatial resolution of the incident beam size, all these spectra reflect the collective response of a cluster of ZIF-8 crystals. The variations in particle size, orientations, and morphologies of the crystals would largely broaden the spectra, thereby leading to only one pronounced peak that can be readily seen. Nevertheless, all measured spectra show clear optical resonances in the UV–visible range and substantial size dependence, confirming the tunability of structural colors produced by the ZIF-8 crystals.

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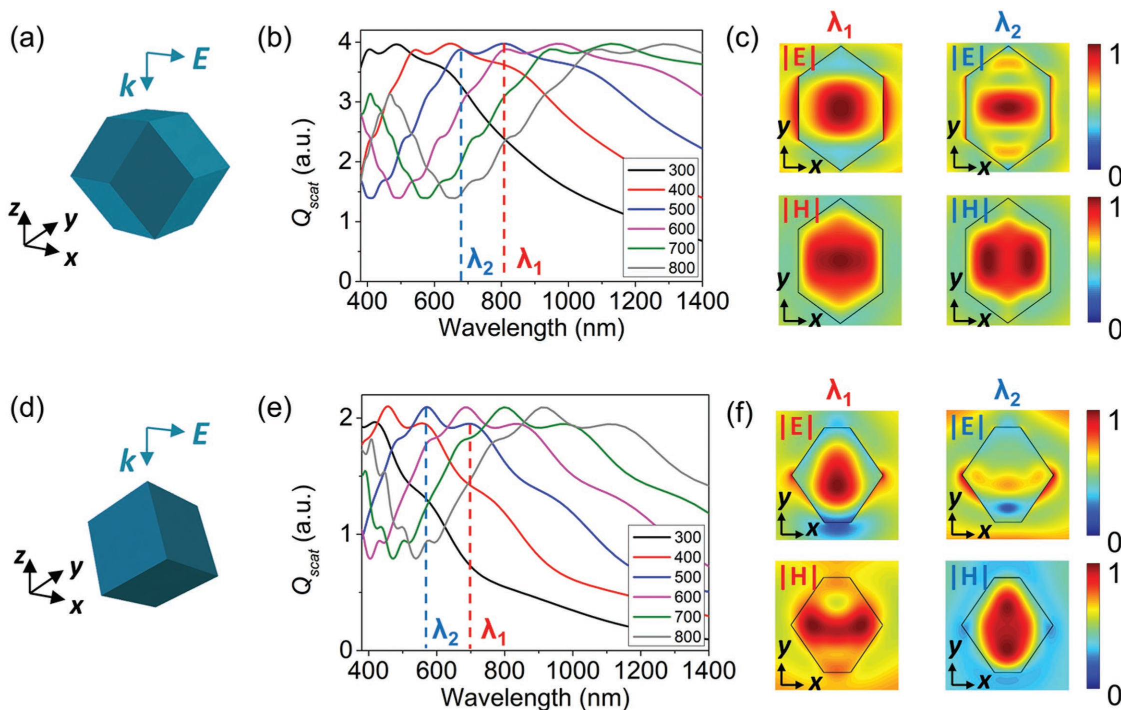

Figure 6. Calculated light scattering of rhombic dodecahedral (upper) and cubic (lower) ZIF-8 nanocrystals. a,d) Schematic illustrations of the nanocrystals and the coordinate system. The incident polarization is in the *x* direction. b,e) Spectral scattering efficiency of nanocrystals with different side length *d* ranging from 100 nm to 500 nm. c,f) Electric and magnetic near-field distributions at scattering resonances of ZIF-8 nanocrystals with a side length $d = 500$ nm. The *xy* profiles are taken in the middle cross section of the nanocrystals. Corresponding resonant wavelengths are labeled in panels (b) and (e).

It is also worth mentioning that, whereas scattering and associated colors are conventional optical phenomena for many nanoparticles, they are also one of the most fundamental and significant physical processes which can provide an effective measure to investigate the fundamental optical properties of nanomaterials. Scattering behaviors of nanoparticles have thus simulated the development of a diverse set of applications ranging from biosensing and thermos-therapy to optical antennas and information storage.[16–20,28–31] During the past few decades, the physics of light scattering by subwavelength nanoparticles were commonly associated with Rayleigh scattering or surface–plasmon interactions supported by metallic materials such as gold or silver. For nonmetallic nanoparticles, it is only until very recently that people started to investigate their scattering properties and relevant optical resonances.[29] A multitude of intriguing scattering properties of various dielectric nanoparticles have been unveiled, opening up unique possibilities for many novel applications such as color filtering, color printing, and quantum information technology.[30,31] In this context, Mie theory[28] provides a fundamental physical framework to understand the size-dependent scattering response of the ZIF-8 nanocrystals. The broadband scattering feature of the ZIF-8 nanocrystals is due to the low permittivity contrast between the crystal and the surrounding environment, which leads to a slightly dispersive polarization current inside the particles and further results in the Mie resonances and associated scattering colors. The noticeable scattering peaks can be attributed to the optically induced electric and magnetic dipolar or multipolar resonances. Figure 6c shows the near-field electric and magnetic distributions at first two peak wavelengths for rhombic dodecahedral ZIF-8 nanocrystals with $d = 500$ nm. At the first scattering resonance ($\lambda_1 = 820$ nm), the electric field shows a clear electric dipolar behavior with two hot spots at both ends of the crystal along with the incident polarization in the x direction while the magnetic profile demonstrates an evident magnetic dipolar response with a strong concentration of the magnetic field inside the particle. Such a confined magnetic dipolar contribution also contributes to the shoulder (≈1020 nm) appeared on the long-wavelength side of the peak, reverifying the broadband optical response of the ZIF-8 nanocrystals. The coexistence of the electric and magnetic dipolar resonances has recently given rise to a variety of interesting applications such as the directional scattering, enhanced Raman spectroscopy and Huygens metasurfaces.[32–34] Differently, at the second scattering peak ($\lambda_2 = 680$ nm), higher-order electric and magnetic multipolar responses can be seen with more complicated field distributions. The electric standing wave and two separate magnetic maxima imply the excitation of a hybrid Fabry–Perot–Mie resonance.[35,36]

Similar electric and magnetic-type Mie resonances are also possessed by the cubic nanocrystals (Figure 6d–f), with relatively smaller magnitudes and blueshifted spectra. We also plot 2D maps of the scattering efficiency as a function of the incident wavelength and the crystal size for both morphological nanocrystals (see Figure S11, Supporting Information). The scattering peak wavelengths exhibit a linear redshift tendency with respect to the increasing crystal size. Given the wide range of the crystal size that we can obtain, we may expect that

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the intriguing scattering resonances of the ZIF-8 crystals can be further extended from the visible spectrum to the infrared region. The influence of the incident polarization is additionally studied. As shown in Figure S12 (Supporting Information), there is only a slight difference between two orthogonal polarizations due to the high-rotational symmetry of the synthesized crystals.

The presented structural color and the fascinating scattering properties provide a credible new pathway for ZIF-8 crystals to be used in a range of nanophotonic applications. For example, the broadband and efficient light-matter interactions and the induced optical magnetism make the ZIF-8 a promising low-index optical material that can be applied in the visible metasurfaces and planar optics.[37–40] It is also worth re-emphasizing the significant chemical features of ZIF-8 material, including thermal stability, chemical tolerability and selective-sorption properties. We believe that the combination of such remarkable chemical properties and its unique optical characteristics can further bring entirely novel and unexplored possibilities in a diverse set of interdisciplinary applications such as photochemical catalysis, chemical sensing, and spectral imaging.

3. Conclusions

In summary, we have demonstrated a wafer-based fabrication method for isolated ZIF-8 nanocrystals, and the zinc source was provided by zinc oxide thin film deposited by ALD. To selectively convert zinc oxide thin film into isolated ZIF-8 nanocrystals, we used Au NPs as an inhibitor for the crystallization process, which could confine the particle number density and with also some effect on size of ZIF-8 nanocrystals depending on the concentration of Au NPs. The light scattering properties of ZIF-8 nanocrystals in visible wavelengths and size induced redshift of resonance were observed directly by dark field optical microscope. This resonant optical response was verified by FDTD simulation, which further suggested a broadband resonance of ZIF-8 nanocrystals in both visible and infrared wavelengths depending on geometry and sizes. The fabrication method we proposed provides new possibilities not only to study ZIF-8 crystals, but also to integrate this potential material with various micro and nanofabrication techniques. The structural colors induced by Mie resonances also suggest ZIF-8 as a promising dielectric material for nanophotonics research, which can be combined with chemical or biological applications.

4. Experimental Section

Deposition of ZnO Film: ZnO films were deposited with a thermal ALD system (Picosun R200). The substrates used were (100) silicon wafers (100 mm, single side polished, with native oxide) or fused silica wafers (100 mm, double side polished). The layer by layer ALD was realized by subsequently applying two precursors—diethylzinc ($Zn(C_2H_5)_2$, DEZ) and deionized water, with carrier gas (N_2) flows of 150 and 200 sccm, respectively. The pulse times of both precursors were 0.1 s, the purge time for water was 0.5 s, while the purge time for DEZ was set to be 20 s to remove any reaction byproducts and unreacted precursors. Since a low deposition temperature can give better structural and optical qualities of ZnO thin film,[41] the reaction temperature was set to be 200 °C, under which the deposition rate was suggested to be 0.15 nm per cycle.[42]

Synthesis of ZIF-8 Crystals from ZnO Films: Au NPs (OD1; average diameter 10 nm, stabilized suspension in 0.1×10^{-3} M PBS, Sigma-Aldrich) was mixed with deionized water (DIW) with volume concentrations of 20, 40, and 60 vol%, and dispensed (20 µL) on the top of deposited ZnO layer. The samples were dried and cleaved into small pieces with size of around 1 cm × 1 cm. After that DIW was used to rinse the sample surface for 1–2 min to remove possible potassium chloride residues in the PBS buffer solution. The distribution of Au NPs was analyzed with SEM and an image processing procedure as discussed in Figure S6 (Supporting Information). The ZnO thin film was transformed into ZIF-8 crystals through solvothermal reaction. In a typical process, dimethylformamide (45 mL) was mixed with 2-methylimidazole (0.2 g) and DIW (15 mL) in a Teflon lined autoclave. ZnO thin films were put into the container, sealed, and placed inside a convection oven for 20 h at 75 °C. After the reaction, the samples were rinsed with DIW several times and dried for further characterizations.

Characterization and Simulation: The sample thickness was measured by spectroscopic ellipsometry (Ellipsometer VASE, J.A.Woolam). The morphology and surface roughness were studied by SEM (Supra 60VP, Zeiss, 3 kV) and AFM (ICON PT, Bruker). The elemental composition was analyzed by EDX (the acceleration voltage of 10 kV was used) and XPS (ThermoScientific). The light scattering properties were studied by employing dark field optical microscope (Nikon ECLIPSE L200N), randomly polarized white light was used to illuminate the sample and the scattered light was collected normally to the substrate through a 20 × dark field objective lens (NA = 0.8). The optical response was calculated by FDTD simulations (Lumerical FDTD Solutions, version 8.11).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

atomic layer deposition, gold nanoparticles, structural colors, ZIF-8

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Photocatalysis

Highly Ordered 3D Silicon Micro-Mesh Structures Integrated with Nanowire Arrays: A Multifunctional Platform for Photodegradation, Photocurrent Generation, and Materials Conversion

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Abstract: Hierarchical three dimensional (3D) microstructures integrated with low-dimensional nanomaterials can realize novel properties or improved performance. We report a unique conductive and highly ordered 3D silicon micro-mesh structure, which is fabricated by standard lithography using a modified plasma etch process. Zinc oxide (ZnO) nanowires are then integrated with the micro-mesh, and the density of ZnO nanowires (NWs) can be increased by around one order of magnitude compared with ZnO NWs on a 2D substrate. Owing to the high spatial density of ZnO NWs on the robust 3D silicon micro-mesh structures, improved photocatalytic activity and stability can be achieved. A remarkable enhancement of photocurrent response is also observed. The ZnO can be converted into ZnS NWs and ZnO@ZIF-8 as on the micromesh. This method is low-cost and compatible with traditional complementary metal–oxide–semiconductor industries, and provides new possibilities for a wide range of devices based on micro-nano-electro-mechanical and chemical systems.

Introduction

Materials with 3D structures and well-defined geometries can give performance improvements in applications within the fields of photonics[1] and electronics.[2] First, intrinsic properties of the microstructured materials can be tuned in 3D structures, such as microporosity, and photonic bandgaps. Second, these 3D structures can be integrated with functional low-dimensional building blocks, e.g. nanoparticles or nanowires (NW), to achieve an improved performance of their desired functions. Although the potential of 3D structures is attractive, a reliable fabrication strategy is considered to be technically difficult. Bottom up synthesis of 3D foams constituted by metals (Cu, Ni, Al, etc.) or graphene are widely used, however, the geometry and morphology of the 3D structures are difficult to control. Another category of top-down fabricated 3D structures employs traditional micro- and nanofabrication techniques from the semiconductor industry, which show the superiority for on-chip integration and mass production, albeit often at higher cost that will require a considerable performance improvements compared to bottom up systems.

To functionalize 3D microstructures, as a typical direct wide band gap (Eg = 3.37 eV) semiconductor, zinc oxide (ZnO) can generate free carriers by incident photons and be utilized for a wide range of purposes, e.g. dye sensitized solar cells (DSSC),[3] photocatalytic reactions,[4] supercapacitors,[5] etc. Besides, the notable piezoelectric properties in ZnO nanostructures also makes it a good candidate for applications as electric generators[6] and piezo-phototronic devices.[7] Apart from the intrinsic physical and chemical properties, the geometry and morphology of ZnO nanostructures are important parameters that influence the above mentioned applications. By adjusting the nucleation and growth during the materials synthesis, ZnO nanostructures with a wide range of morphologies have been successfully achieved.[8–11] Among these, ZnO NWs show unique advantages due to the facile fabrication process and the high spatial density, making ZnO NWs outperform other nanoscale counterparts in different applications, such as sensors[12] and field electron emission.[13]

To further improve the materials usage and performance of ZnO NWs, increasing the spatial density of ZnO NWs on a device will facilitate the full contact of the NWs with the surrounding reaction medium, but also accelerate mass and ion

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transportation during device working. For example, Ko et al developed a repeated seed deposition-hydrothermal growth method to prepare long branched “treelike” multigeneration hierarchical ZnO NWs. Compared to the conventional ZnO NWs without branches, the 3D ZnO nanotrees show a density increasement of 1–2 orders of magnitude, and 5 times improvement of the overall light-conversion efficiency for dye-sensitized solar cell.[14] Another strategy is to use different 3D structures, i.e., graphene foams,[15,16] nickel foams,[17] or silicon NW arrays,[18] as substrates for the growth of ZnO NWs, but often with low microstructure control mentioned above and process compatibility difficulties if on-chip integration is wanted.

Here we report a highly ordered 3D silicon micro-mesh structure, which is low cost and can be easily designed and fabricated, by being created in a single reactive ion etch run by a novel plasma etching technique. The fabricated silicon substrate has a mesh-like microstructure and can increase the surface area by around one order of magnitude compared to a 2D planar substrate. Importantly, the 3D silicon micro-mesh structures can be integrated with low-dimensional structures and become a promising platform for diverse applications. In this work, ZnO NWs were used as typical model system to demonstrate the usage of 3D silicon micro-mesh structures. Specifically, atomic layer deposition (ALD) was used to grow a ZnO layer conformally on the surface of the 3D silicon structures, to act as the seed layer for the following hydrothermal reaction, during which ZnO NWs were grown perpendicularly to the 3D mesh, forming a high density of ZnO NWs. The functionality was tested by photocatalytic degradation of rhodamine B (RhB) and photocurrent response properties of the obtained ZnO NWs/3D silicon structures and compared with that of ZnO NWs on 2D silicon substrates. A significant increase of degradation rate of RhB was observed under UV light irradiation, and the enhancement of light induced photocurrent was achieved. Thanks to the chemically and mechanically stable silicon substrate, the ZnO NWs can be used as self-sacrificed templates and chemically converted into other zinc-based compounds with tunable composition, such as zinc sulfide (ZnS) and zeolitic imidazolate frameworks (ZIF-8), while the original 3D NW morphology can still be inherited. Our results demonstrate the flexibility and multifunctionality of the fabricated NW arrays/3D silicon structures. It should be noted that the whole process is carried out at a relatively low temperature of below 200 °C, which is within the process limit of complementary metal oxide semiconductor (CMOS) circuits and most of the polymer materials,[19] thus enabling flexibility and freedom for different applications. When integrating with CMOS devices, the proposed NW arrays/3D silicon structures are expected to show potentials in on-chip detection, power storage and conversion, and devices for in-situ thermal or electric modulations.

2. Results and Discussion

2.1. Fabrication and Characterization

A schematic view of the fabrication process flow is shown in Figure 1a, which includes pattern definition with conventional UV lithography, creation of 3D silicon microstructures with a new plasma etching process, ZnO layer coating with ALD, and the final step of hydrothermal reactions to grow ZnO NWs onto the 3D silicon structures. As a crucial step of the fabrication, highly ordered 3D silicon micro-mesh substrate was fabricated by the DREM (Deposit, Remove, Etch Multistep) method, which has been reported in our previous work.[20,21] Briefly, DREM is a modified time multiplexed Bosch etch process, but employs well defined three steps and a parameter ramping technique, resulting in a straight profile of silicon structures. Meanwhile, sidewalls of the structure could be well protected by the fluorocarbon (FC) layer, which is generated by the passivation of octafluorocyclobutane (C_4F_8) gas. During the process, a few DREM cycles were first applied as in Figure 1a(2), thus an anisotropic silicon structure was fabricated. To make the structure isolated from substrate, an isotropic etch was applied as in Figure 1a(3), during which the FC layer on the sidewall could protect the structure from being corroded by the etch gas sulfur hexafluoride (SF_6). By repeating DREM cycles and isotropic etch, 3D multiple suspended layers could be fabricated as shown in Figure 1a(4), and the FC layer protected silicon structures acted as the etch mask for the next layer of suspended silicon structures. To prevent the isolated layers from collapse, some larger support structures were designed beforehand, which could survive the isotropic etch step and support the suspended silicon beams. After plasma ashing, the remaining photoresist layer and the FC layer on the silicon structures were removed, thus a clean highly ordered 3D silicon micro-mesh substrate was prepared for the subsequent ALD process, during which a ZnO layer with 50 nm thickness was deposited conformally as shown in Figure 1a(5). The ALD deposited ZnO thin film is polycrystalline with a major orientation of (002),[22] and it will serve as the seed layer for the ZnO NWs growth via a hydrothermal reaction (Figure 1a(6)).[23,24] Since ALD process is conformal, ZnO NWs would grow following the 3D silicon substrate, also on the bottom part of the suspended silicon structures. Thus ZnO NWs/3D silicon structures were fabricated, and the density of ZnO NWs could be increased compared with ZnO NWs on a 2D planar substrate.

The morphology of the highly ordered 3D silicon micro-mesh substrate and ZnO NWs/3D silicon structures were studied by scanning electronic microscope (SEM). Figure 1b shows the cross section view of 10 layered silicon microbeam structures, and the thickness of each beam is around 1 μm. The sample was cleaved and a tilted view is shown in Figure 1e. The length of the silicon microbeams is 10 μm and the width is 2 μm, anchored on large pillars with 10 μm diameter. After depositing ZnO seed layer and hydrothermal reactions, ZnO NWs can grow conformally following the surface of the silicon structures (Figure 1c, f). The length of ZnO NWs is controlled by

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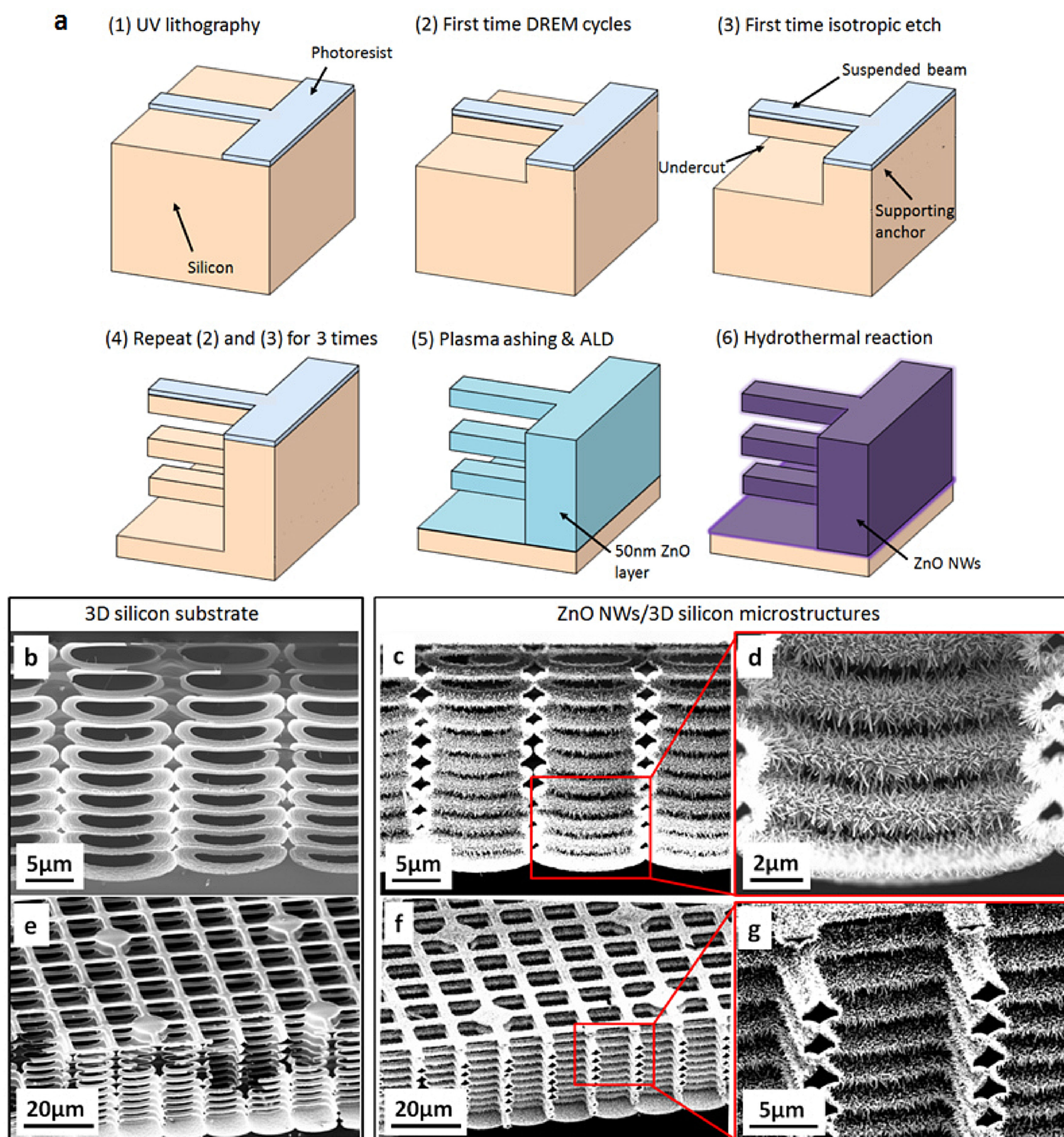

Figure 1. (a) Process flow to fabricate ZnO NWs/3D silicon structures: (1) UV lithography; (2) first DREM cycle to create structures; (3) first isotropic etch to create suspended structures; (4) repeat DREM cycles followed by isotropic etch for 3 times; (5) plasma ashing to clean the polymers and deposit ZnO with ALD; (6) hydrothermal reaction to grow ZnO NWs; SEM images of 3D silicon substrate in (b) cross section view and (e) tilted view. SEM images of ZnO NWs/3D silicon structures in (c, d) cross section view and (f, g) tilted view.

the hydrothermal reaction time. The reaction time was carefully controlled to avoid the overlap of ZnO NWs between each two layers of silicon structures (Figure 1d, g).

Figure 2a shows a magnified SEM image of a single silicon microbeam covered by ZnO NWs. It can be seen that high density of ZnO NWs grow on the suspended silicon microbeam. Transmission electron microscope (TEM) image of the sample is shown in Figure 2b. The average length of the ZnO NWs is around 1 µm, and the diameter is ~60 nm. The crystalline and phase of the sample was determined by X-ray diffraction (XRD) as shown in Figure 2c. All the diffraction peaks are well matched with the wurtzite ZnO according to the standard diffraction card (JCPDS number: 36-1451). A strong (002) diffraction peak is observed, indicating the growth of ZnO NWs follows the crystalline orientation of ALD ZnO thin film. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image and elemental mapping (Figure 2d) performed by electron dispersive x-ray (EDX) spectroscopy show the spatial distribution of Zn, O, and Si elements in the products. Additional structural characterizations with EDX, XRD, TEM and photoluminescence measurements can be found in Figure S1–S4.

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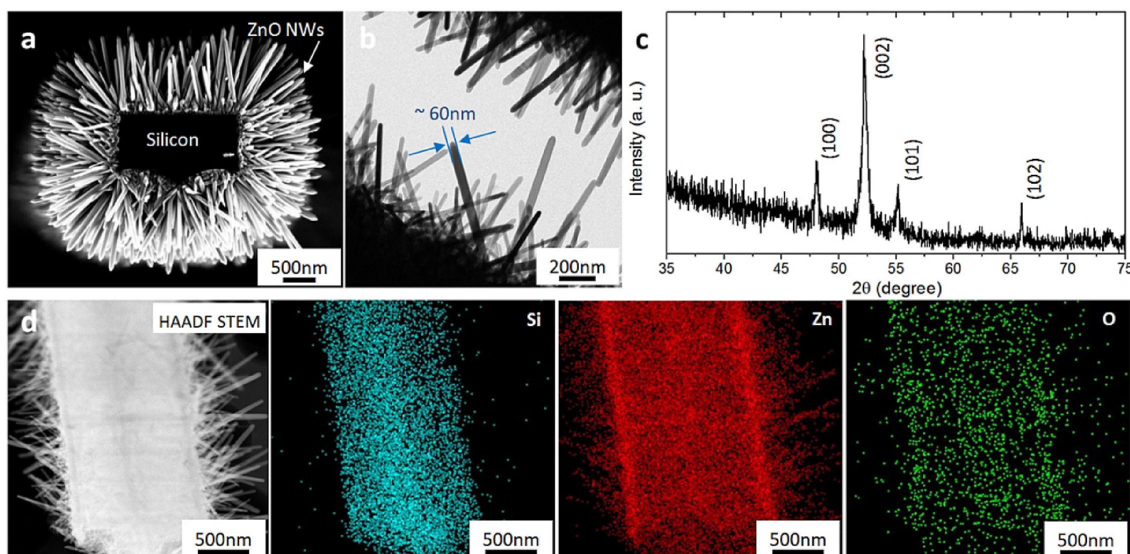

Figure 2. (a) SEM image of silicon microbeam covered with ZnO NWs; (b) TEM image of ZnO NWs; (c) XRD pattern of ZnO NWs/3D silicon structures; (d) HAADF-STEM image and element mapping of a silicon microbeam covered with ZnO NWs.

2.2. Photocatalytic Performance

When irradiating ZnO materials with light with photon energy larger than the band gap of ZnO, electron-hole pairs will be generated, and the unpaired holes react with water to form hydroxyl radicals, which is a strong oxidizers and can degrade organic dyes into simple organics and finally into carbon dioxide.[25] This process has been widely studied for the purpose of decontamination and purification of polluted water. Many strategies have been proposed to increase the photocatalytic degradation efficiency, e.g. by modifying the morphology,[9,26] introducing dopants,[27,28] integrating ZnO with other substrates,[29,30] etc. Here we demonstrate that the ZnO NWs/3D silicon microstructures possess high photocatalytic activities towards the degradation of organic dye RhB.

For comparison, three different samples were prepared using different silicon substrates, including 3D silicon with large 2 μm beam size (ZnO NWs/3D Si–L), 3D silicon with smaller 1 μm beam size (ZnO NWs/3D Si–S), and planar silicon (ZnO NWs/2D Si). The typical morphology of the three samples are shown in Figure 3a–c. Figure 3d shows a series of UV-vis absorption spectra of the aqueous solution of RhB with ZnO NWs/3D Si–L as the photocatalyst exposed to UV light for different times. The characteristic absorption peak of RhB dye centered at 554 nm decreases rapidly with increasing exposure time. Figure 3e shows the comparison of the photocatalytic activity of the three samples under the same experimental conditions. The blank experiment without the addition of photocatalyst shows almost no degradation of RhB under UV light illumination. While with the presence of different photocatalysts, the degradation of RhB is observed. The degradation of RhB follows the order of ZnO NWs/3D Si–L > ZnO NWs/3D Si–S > ZnO NWs/2D Si. Figure 3f shows the linear relationship between $\ln(C_t/C_0)$ and illumination time t, indicating the photocatalytic reaction follows first-order kinetics, $\ln(C_t/C_0) = -kt$, here C_0 and C_t are the initial concentration and the concentration at reaction time *t* of the RhB solution, respectively, and the slope k is the apparent reaction rate. The calculated rate constant for ZnO NWs/3D Si–L is 0.047 min^{-1}, which is 1.5 times faster than ZnO NWs/3D Si–S (0.031 min^{-1}), and 8 times faster than ZnO NWs/2D Si (0.006 min^{-1}). The results confirm that the ZnO NWs/3D Si–L sample is superior in degrading RhB dye, and a comparison between ZnO NWs/3D Si–L and other reported hybrid structures is shown in Table S1. The enhancement of photodegradation efficiency is attributed to the significant increase of ZnO NWs density, thus more photocatalytic reactions can take place in the same unit area. Figure S5 shows the relation between photodegradation rate k and the number density of ZnO NWs. To test the stability of the photocatalytic performance, ZnO NWs/3D Si–L was rinsed after each photocatalytic process and a new process was repeated afterwards, and the same degradation rate could be observed for 3 processes as shown in Figure 3g. This demonstrates the good reusability of ZnO NWs/3D Si microstructures for photocatalytic applications.

2.3. Photocurrent Generation

The semiconductor nature of ZnO material makes it a favorable material for photosensitive devices, e.g. photovoltaics and solar cells.[31] To improve the efficiency of the free charge migration, conductive substrates such as graphene are used to form into heterostructures with ZnO.[32,33] This strategy, however, increases the economic cost for the fabrication process, thus hinders the large scale applications. Here we demonstrate that a significant enhancement of photocurrent response can be achieved by integrating ZnO NWs with the 3D silicon microstructures.

The photoresponse performances of ZnO NWs/3D Si–L, ZnO NWs/2D Si, and ZnO film/2D Si were investigated by

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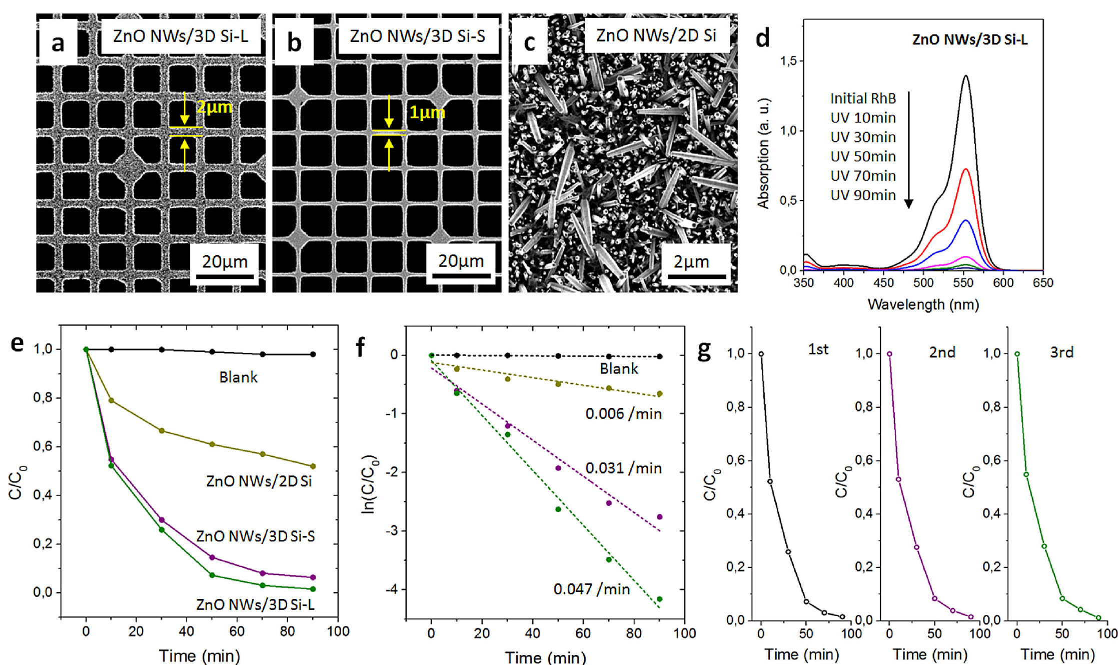

Figure 3. Photocatalytic performance of ZnO NWs/3D silicon structures. (a-c) SEM images (top view) of ZnO NWs/3D Si–L, ZnO NWs/3D Si–S, and ZnO NWs/2D Si; (d) Time dependent UV-visible spectra of RhB solutions with presence of NWs/3D Si–L; (e), (f) Degradation curves for different photocatalysts under UV light illumination; (g) Time profile of the change in concentration of RhB aqueous solution for the first three cycles in the presence of ZnO NWs/3D Si–L.

running the line sweep voltammograms (LSV) with and without UV light irradiation ($\lambda \sim 365$ nm) and an electrolyte, under ambient conditions). The bias potential was ranging from -0.5 to $+1.0$ V vs. saturated calomel electrode (SCE). As shown in Figure 4a, ZnO NWs/2D Si and ZnO film/2D Si show negligible current in the dark. When illuminated with UV light, the two samples exhibit non-zero current densities. For ZnO NWs/3D Si sample, it is interesting to find that an obvious current is generated even without UV light illumination. A prominent photocurrent response can be observed with the UV irradiation. Specifically, a current density of ~0.18 mA/cm^2 can be achieved at a bias of 1.0 V, which is around one magnitude larger than the photocurrent density for ZnO NWs/2D Si and ZnO film/2D Si, respectively. This photocurrent enhancement is related to the high density of ZnO NWs and more free charge carriers generated in a unit area, and the relationship between photocurrent amplitude at a bias of 0.5 V vs. SCE and the density of ZnO NWs is shown in Figure S6. The amperometric I–t curves with the chopped illumination at the bias potential of 0.5 V vs. SCE were measured for the three samples as shown in Figure 5b. A photoresponse with a stable photocurrent for all the samples was observed. The current returned to the original values immediately as the light was switched off. Figure 5c compares the photocurrent density at the bias of 0.5 V vs. SCE for the different samples. The results of bare silicon and ZnO NWs/3D Si (beam size of 1 µm) are also shown for comparison. It can be seen that ZnO NWs/3D Si–L (beam size of 2 µm) gives a higher current density compared with ZnO NWs/3D Si–S

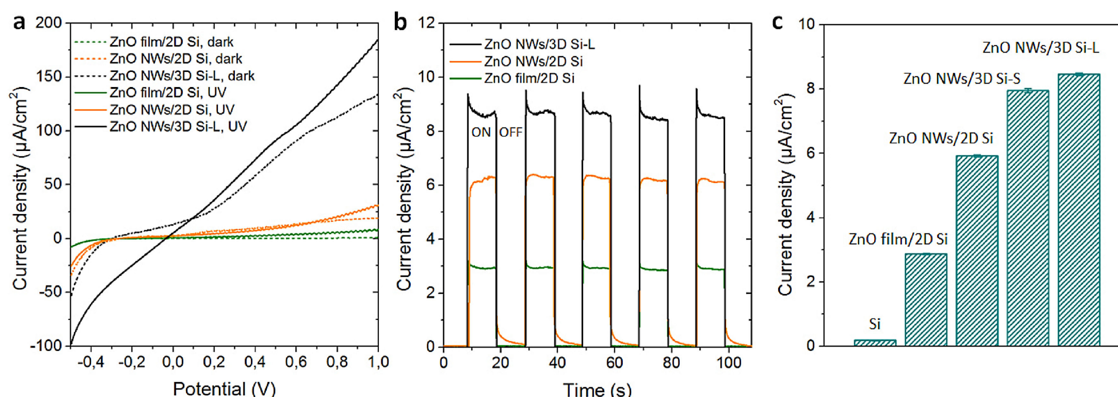

Figure 4. (a) Line sweep voltammograms; (b) photocurrent responses with UV light five on/off cycles at a bias of 0.5 V vs. SCE; (c) average photocurrents for different samples at a bias of 0.5 V vs. SCE.

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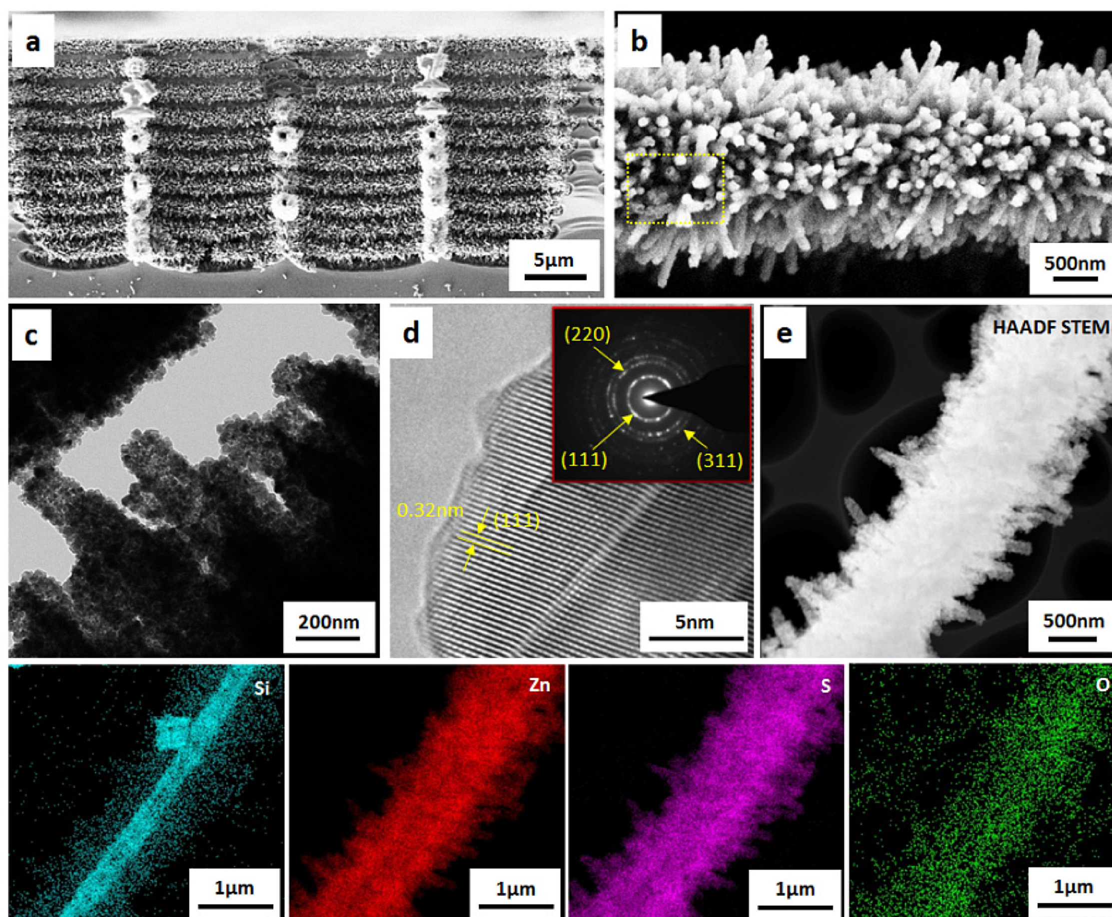

Figure 5. (a, b) SEM, (c) TEM, and (d) HRTEM of ZnS NWs/3D silicon microstructures. The inset shows the SAED pattern. (e) HAADF-STEM images and corresponding EDX element mapping.

(beam size of 1 µm), both are significantly higher than ZnO NWs/2D Si, ZnO film/2D Si, and bare Si. The remarkable improvement of photocurrent response demonstrates the ZnO NWs/3D silicon microstructures as efficient alternative structures for photoelectric applications. It should be mentioned that by increasing the number of isolated layers, the photocatalytic and photocurrent performance could also be improved, however, this is determined by the fabrication process, thus a maximum number of 15 layers can be achieved and the highest photodegradation rate and photocurrent density are limited.

2.4. Beyond ZnO – Other Materials

ZnO is a versatile material that can be conveniently transformed into other functional materials, e.g. ZnS and ZIF-8 structures, which show a broader range of applications. By using a simple hydrothermal or solvothermal reaction, the present ZnO NWs/3D silicon microstructures can be converted into ZnS NWs/3D silicon and ZnO@ZIF-8 NWs/3D silicon microstructures, while the original 3D morphology can still be preserved.

ZnS is a typical semiconductor with a bandgap of 3.67 eV, and has been for photoelectric,[34] and photovoltaics[35] applications. A hydrothermal growth process was performed to convert ZnO NWs to ZnS nanostructures, during which a nanoscale Kirkendall effect happens inducing the formation of hollow structures.[36,37] In Figure 5a, we can see that the structures remain intact after hydrothermal reactions, with "tubular" nanostructures covering the whole 3D substrate. From an enlarged view of one microbeam, the tube-like morphology can be distinguished (see the yellow square area in Figure 5b), and the hollow structure can also be confirmed by additional TEM and HAADF-STEM images as shown in Figure S7. The rough surface of the ZnS NWs indicates the converted sample is polycrystalline (Figure 5c), which is further confirmed by the selected area electron diffraction pattern (Figure 5d inset). The diffraction rings can be identified and indexed to (111), (311) and (220) planes of zinc-blend ZnS. Figure 5d shows a typical high-resolution TEM (HRTEM) image, and the lattice spacing was calculated to be 0.32 nm, which corresponds to the (111) crystalline plane of a cubic ZnS crystal. HAADF-STEM image and elemental mapping results show a uniform distribution of Zn and S over the Si microbeam. The

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observation of some weak O signals suggests the coexistence of ZnO residues.

The other converted material is ZIF-8, which is a typical metal-organic framework (MOF) with a porous 3D zeolite crystal structure. ZIF-8 has been studied extensively and shows a great potential in catalysis,[38] gas adsorption,[39] and optics.[40,41] Herein, solvothermal reaction was employed to convert the ZnO NWs into ZIF-8 structures on the 3D Si substrate. Figure 6a–c shows the SEM images of the transformed structures. It can be seen that ZIF-8 crystals cover the 3D silicon structures in a uniform manner. An enlarged view implies that there are still underlying ZnO NWs remaining on silicon substrates, and the ZIF-8 crystals filled the gaps between ZnO NWs. This is expected as each Zn atom from the the ZnO gives a 102 times larger ZIF-8 unit cell (4913 $Å^3$) than the ZnO unit cell (48 $Å^3$). HAADF-STEM (Figure 5d, Figure S8) and TEM images (Figure 5e,f) also show the porous morphology of ZIF-8 crystals, and residual ZnO NWs exist in the core of ZIF NWs, thus forming ZnO@ZIF-8 NWs/3D silicon microstructures. EDX element mapping on a section of ZnO@ZIF-8 NWs/3D silicon microstructures confirms the existence of N, O and C elements and verifies the formation of ZIF-8 structures on the surface of ZnO NWs (Figure 5g). Compared with the traditional powder-like ZIF-8 crystals, the obtained ZIF-8 NWs /3D silicon microstructures can serve as a reusable and mechanically robust substrate. Meanwhile, the spatial density of ZIF-8 NWs can also be modulated on the 3D structure geometry. Therefore, an improved performance can be expected for applications as catalysis and gas adsorption. Further studies on the applications of these 3D nanostructures are in progress.

Conclusions

In summary, a novel highly ordered 3D silicon micro-mesh structure is presented as a robust substrate to significantly increase the surface area of different materials. By integrating ZnO NWs with the 3D silicon substrates, both photocatalytic and photocurrent generation performances were improved in a large scale compared with 2D plane substrate grown ZnO NWs. The fabricated ZnO NWs can also be converted to other functional materials including ZnS and ZIF-8, while the ordered structure and morphology remain intact, showing the flexibility and potential of 3D structures for other applications. The whole fabrication process is easy to control and less time consuming compared with traditional multiple-time growth method. Since the 3D silicon substrate was fabricated with standard techniques in semiconductor industries, it is promising to integrate the funtionalities of different NW structures onto 3D silicon substrates with micro-electro-mechanical and chemical system designs, to optimize yields in complicated range of applications especially for on-chip applications.

Experimental Section

Fabrication of 3D silicon micro-mesh structures: Double side polished silicon wafer (100 mm, *n*-doped, 1–20 Ω cm) was used to fabricate

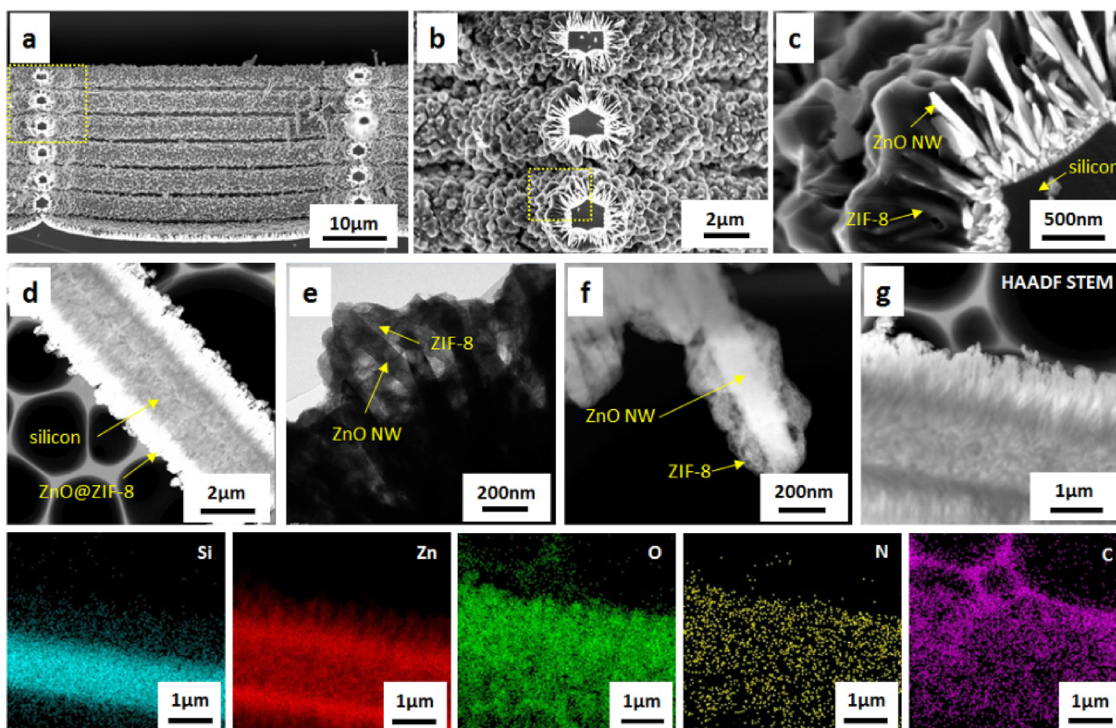

Figure 6. (a–c) SEM, (d) HAADF-STEM, and (e, f) TEM images of ZnO@ZIF-8 NWs/3D silicon microstructures; (g) HAADF STEM image and corresponding EDX element mapping results of the ZnO@ZIF-8 NWs/3D silicon microstructures.

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3D silicon micro-mesh structures. Patterns were defined with a direct exposure maskless lithography system (tabletop maskless aligner MLA100, Heidelberg), and a negative tone resist (AZ nLOF 2020, MicroChemicals) was used. Plasma etching was performed in a dual source etching system (DRIE Pegasus, SPTS). After etching, the samples were cleaved into pieces with size of 1.2 cm by 1.2 cm, and cleaned with a plasma ashing system (PVA TePla 300).

ZnO coating and hydrothermal synthesis: The ZnO seed layer was deposited with a thermal ALD system (Picosun R200). Diethylzinc ($Zn(C_2H_5)_2$, DEZ) and deionized water were used as precursors, with N_2 as carrier gas. The chamber temperature was set to be 200 °C and the deposition rate was around 0.15 nm per cycle. The ZnO NWs were then synthesized by a hydrothermal reaction. Typically, hexamethylenetetramine (HMTA, 0.1 g) and zinc nitrate hexahydrate ($Zn(NO_3)_2$, 0.22 g) were mixed and dissolved in 60 mL of deionized water (DIW). The mixture was then transferred into a Teflon-lined stainless-steel autoclave with 100 mL capacity. The 3D Si micro-mesh structures with ZnO seed layer were put upside down in the solutions, then the autoclave was sealed for solution reaction at 90 °C for 20 h. After the autoclave cooled down to room temperature naturally, the samples were pick up by tweezers, washed with distilled water and dried in air.

Materials characterization: The thickness of ALD grown ZnO layer was measured by spectroscopic ellipsometry (Ellipsometer VASE, J. A. Woolam). PL spectra were measured with a PL mapping system (Accent RPM 2000 series), with excitation wavelength at 404 nm and energy of 20 mW. The morphology of the samples were characterized with scanning electron microscopy (SEM Supra 60VP, 3 keV, Zeiss), transmission electron microscopy (TEM, Tecnai G^2 T20, 200 keV, FEI) coupled with an EDS X-ray spectrometer (Oxford Instrument). Crystallographic information for the samples was collected using a Bruker Model D8 Advanced powder X-ray diffractometer (XRD) with Cr Ka irradiation (2.08 Å). Transmission electron microscopy (TEM), high resolution transmission electron microscopy (HRTEM), high angle annular dark-field scanning transmission electron microscopy (HAADF-STEM), and energy dispersive X-ray spectroscopy mapping analysis were performed on Tecnai G^2 T20 microscope (200 keV, FEI).

Photocatalytic performance test: The photocatalytic activity of the sample was evaluated by the degradation of rhodamine B (RhB, 1.0×10^{-5} M) aqueous solution under UV light (365 nm), using a 300 W Xe arc lamp (CEL-HXF 300) equipped with an UV cutoff filter as a light source. The samples were put into 100 mL of RhB solution. The aqueous solution was stirred in the dark for 1 h to reach a complete adsorption-desorption equilibrium. The reaction system was placed in a sealed black box with the top opened, and was maintained a distance of 15 cm from the light source. After initiation of the reaction by irradiation, a 5 mL sample of the suspension was taken out at regular intervals (~20 min). In order to measure the RhB degradation, UV-visible spectra of the solution was recorded by using UV-2550 UV-visible spectrophotometer (Shimadzu, Japan).

Photocurrent measurement: Standard three-electrode system, including Pt wire as counter electrode, saturated calomel electrode (SCE) as reference electrode, and ZnO/Si samples as working electrodes, was used throughout the measurements. Aqueous solution of Na_2SO_4 (0.5 M, pH = 7.0) was prepared as the electrolyte. The working electrodes with half area of the sample were dipped into the electrolyte, and irradiated from the front side under a UV light (λ~365 nm). The distance from the light source to sample was around 10 cm. The linear sweep voltammetry (LSV; I–V) curves with a scan rate of 5 $mV\,s^{-1}$ at the bias potential (vs. SCE) range from −0.5 to +1.0 V and the amperometric I–t curves with the chopped illumination at the bias potential of 0.5 V vs. SCE were measured for the different working electrodes to compare their photocurrent outputs and photoresponse switching behavior. All the measurements were performed at room temperature. The TAA amount was estimated to be sufficient for a maximum conversion of ZnO nanowires.

Conversion to ZnS: ZnO NWs were converted to ZnS by a hydrothermal reaction. In a typical process, ZnO/Si samples were put into a Teflon lined autoclave (100 mL capacity) containing 50 mL of thioacetamide (TAA, 0.2 M, Sigma-Aldrich), and then kept at 120 °C for 10 hours. After that, the samples were washed with distilled water and dried in air.

Conversion to ZIF-8 structures: The ZnO NWs were converted into ZIF-8 structures by a solvothermal reaction. Typically, dimethylformamide (45 mL) was mixed with 2-methylimidazole (0.2 g) and deionized water (15 mL) in a Teflon lined autoclave with 100 mL capacity, ZnO/Si samples were put into the container, sealed, and placed inside a convection oven for 20 h at 75 °C. After the reaction, the samples were rinsed with deionized water several times and dried in air.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords: three dimensional structures · nanowire arrays · photocatalytic · photocurrent · materials conversion

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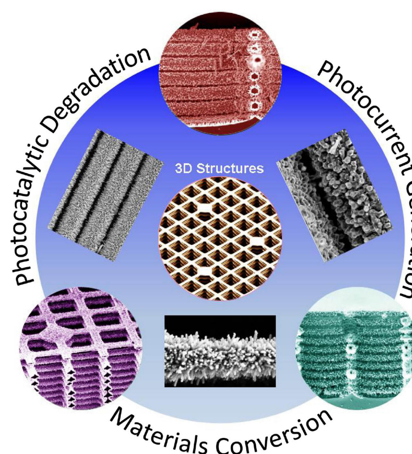
FULL PAPER

Highly ordered 3D silicon micro-mesh structures are used as a substrate for growth of different nanowire arrays. The density of nanowires is increased by one magnitude compared to the 2D substrates, which gives a significant improvement of photodegradation efficiency and photocurrent generation.



Photocatalysis

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1 – 10

Highly Ordered 3D Silicon Micro-Mesh Structures Integrated with Nanowire Arrays: A Multifunctional Platform for Photodegradation, Photocurrent Generation, and Materials Conversion

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Large Area Three-Dimensional Photonic Crystal Membranes: Single-Run Fabrication and Applications with Embedded Planar Defects

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Three-dimensional photonic crystals (3D PhCs) enable light manipulations in all three spatial dimensions, however, real world applications are still faced with challenges in fabrication. Here, a facile fabrication strategy for 3D silicon PhCs with a simple cubic (SC) lattice structure is presented, which exhibits a complete photonic bandgap at near-infrared wavelengths of around 1100 nm. The fabrication process is composed of standard deep ultra-violet stepper lithography, followed by a single-run modified plasma etch process. By applying a direct dry etch release step at the end of the 3D structural etch process, the fabricated 3D PhCs can be released and transferred in the form of a membrane onto other substrates such as glass, polymers, or even substrates with engineered surface. The thickness of the demonstrated membranes is around 2 µm and the size can be up to a few millimeters. A high reflectivity is observed at the stop band frequency, and a planar defect is introduced during the etching process resulting in an optical resonance mode with a small linewidth of around 30 nm. The structure constitutes an optical bandpass filter and can be used as a sensor for organic solvents.

1. Introduction

Three dimensional photonic crystals (3D PhCs), with periodic modulations of dielectric constants in three dimensions, possess a modified dispersion relation and a photonic bandgap (PBG). This results in a range of wavelength, where electromagnetic propagating modes are forbidden, and is an optical analog to the electronic bandgap structures of atomic lattices. By incorporating defects with 3D PhCs, a localized optical resonance mode can be realized in the defect region, and more advanced functionalities can be demonstrated. PhCs with lower dimensions have already been widely used in various fields such as optical waveguides and sensors. However, 3D PhCs, which enable light manipulations in full three spatial dimensions, are still faced with fabrication challenges. A lot of effort has been invested in previous studies, and various fabrication methods have been proposed, most of which are limited by fabrication complexity and cost. The classical 3D PhC configurations such as woodpile structures[1,2] and inverse opal structures[3,4] enable a large bandgap ratio (bandgap width over mid gap position) and flexibilities to manipulate photons with embedded cavities.[5–7] However, these bottom-up strategies require multiple complex fabrication steps and are not suitable for large scale production. Some top-down methods have been proposed to fabricate 3D PhC in a convenient manner, but they do need nonstandard fabrication instruments.[8–12] Fabrication of 3D PhC in a large scale can be realized by plasma etching[13] or modulated electrochemical etching.[14] However, there is still a need for feasible fabrication methods for large scale 3D PhCs and embedded cavities.

The idea to fabricate large scale 3D PhCs simply by using the plasma etching was first proposed by Venkataraman et al.[15] A similar study was later reported by Vlad et al.,[13] both of them made use of the so called "scallops," which are generated during the Bosch process etch cycles and can give a ripple-like sidewall profile to create the necessary modulation of the refractive index. Thus, a 2D pattern from a traditional lithography can be transferred into 3D PhC in a top-down manner. This method has the advantage of high fabrication efficiency and low cost. However, there are some technical limitations. First, the size and the shape of the scallops are difficult to control precisely, since the Bosch process is limited intrinsically by ion angular distribution (IAD) and effects such as aspect ratio dependent etching (ARDE).[16,17] All of them will influence not only the

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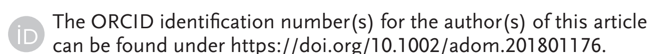
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etch rate, but also the sidewall profile along the etch depth in the silicon, generating nonuniformities affecting the periodicity of the structure. Second, the simple cubic (SC) lattice type of 3D PhCs have a relatively small bandgap ratio of less than 10%,[18] thus geometric distortions or nonuniformity of lattices can close the bandgap in certain directions of Brillouin zone, and the stop band can only exhibit in certain angles of incidence (referred to as pseudo PBGs[19]). Third, to achieve a complete bandgap that is incident angle independent with a high attenuation rate of around 20 dB in mid gap position, a large contrast of refractive index is necessary, thus a strong structural shape modulation of the scallops is necessary, which will at the same time reduce the mechanical stability of the structures.[13,15] All of the disadvantages mentioned above will limit the capabilities and flexibilities of the fabricated structures. Besides, the total number of repeated layers will be limited and the precise introduction of defects will be difficult, ultimately limiting the functionalities of the fabricated structures.

Here, we report a novel multistep one-run fabrication process for 3D PhCs with a SC configuration. The 2D patterns were defined with standard deep ultra-violet (DUV) stepper lithography, and a modified DREM (deposit, remove, etch, multistep) etch process was then performed to transfer the patterns into silicon in such a manner that a 3D shaped structure is realized.[20,21] Compared with the scallops created directly by Bosch process,[13] a large refractive index contrast can be realized due to the strongly modulated etch profile. The fabricated 3D PhCs also show excellent mechanical properties, which enable the structures to be lifted off the substrate and be transferred as a membrane onto other substrates, or to be infiltrated by polymers. Moreover, by infiltrating the air voids in 3D PhC membranes with polymer, a self-supported flexible hybrid film can be fabricated, with 3D silicon structure embedded, while the features of bandgap still preserved. To enable optical functionalities of the fabricated 3D PhCs, planar defects are introduced directly during the modified etch process, which results in a resonance mode coupled to PBG at a wavelength of around 1100 nm, with a linewidth of around 30 nm. We have demonstrated that the fabricated 3D PhC membrane with embedded planar cavity can be used as a sensor for organic solvents with a good sensitivity of around 400 nm RIU^{-1} (RIU, refractive index unit). By transferring the 3D PhC membranes onto n-doped black silicon, the near-infrared (NIR) photoluminescence (PL) of the black silicon[22] could be filtered efficiently with an attenuation ratio of around 20 dB.

2. Results and Discussion

2.1. Fabrication Process

The time multiplexed Bosch process is a standard plasma etching technique in conventional complementary metal-oxide semiconductor (CMOS) micro- and nanofabrication industries. By applying a passivation step with inhibitors (such as CF_2 from C_4F_8), some ion bombardment using a radiofrequency platen power source, and a step with isotropic etching species (such F from as SF_6) sequentially, the sidewall can be protected, and the etch process can proceed in an anisotropic manner. Since the etch step with SF_6 is isotropic, the sidewall has normally a “rippled” profile with shape modulations known as scallops, which has been suggested before for fabrication of 3D PhCs.[13,15] In order to have a large modulation of the etch profile, the amplitude of the scallop needs to be maximized. This, however, might delaminate and destroy the structures. To have a better profile control of the structures and more flexibility in fabrication, we applied a modified DREM etch process as introduced in our previous studies.[20,21] A schematic view to compare the Bosch process and the modified DREM process can be seen in Figures S1 and S2 in the Supporting Information. We will show later that this technique enables a better mechanical stability of the fabricated structures and a large modulation of the refractive index. More importantly, planar cavities can be embedded conveniently and are easily introduced by programming the etching sequence during the fabrication process. The fabricated 3D PhCs were then released into freestanding membranes by a final dry release step. The details of the fabrication process will be introduced below.

In a DREM process, the bottom removal of the passivation layer and the isotropic etch of silicon are fully decoupled, thus the size of scallops can be minimized, at the same time, a straight profile can be achieved and the sidewall can be well protected from ion bombardment.[20] A process flow of the modified DREM process[21] is shown in **Figure 1**a. First, DUV stepper lithography was performed to define the patterns (see Figure 1a1). Second, 5 DREM cycles were applied to etch into silicon and create straight hole structures (see Figure 1a2). Each scallop has the size of around 20 nm, which is much smaller than the scallop sizes from the traditional Bosch process, which is typically around a few hundred nanometers.[13,15] In the next step, an isotropic etch was performed with SF_6 gas without platen power to maximize the isotropicity (Figure 1a3), thus generating a large shape modulation. By repeating these two steps subsequently, 3D periodic structures have been fabricated. Since the structures are strengthened by the anisotropic part of the etch profile, the sequences can be repeated for at least eight times (limited by the thickness of photoresist), and the fabricated 3D periodic structures can be released from silicon substrate by a final isotropic etch step with a longer etch time not resulting into structural collapse (Figure 1a4). The fabrication process is CMOS compatible and based on the standard fabrication techniques. The etch process takes only a few minutes, and the sequence is easy to be programmed, so that the period and the size of void can be tuned in a reasonable wide range.

The total thickness of the fabricated membranes is around 2 µm, and area can be several square millimeters. In Figure 1b, we can see that the fabricated 3D PhCs can be peeled off by tweezers and transferred to a piece of quartz wafer (Figure 1b4). The membranes can also be infiltrated by polymer, thus a flexible film can be fabricated with 3D PhCs embedded (Figure 1b5) (for membranes with even larger area, other transfer methods might be necessary, since the membranes will break at the contact point with tweezers). It should be noticed that the 3D PhCs membranes are porous and can be infiltrated with liquids, e.g., polymer, thus the silicon structures could be supported by the soft polymer, and a good flexibility

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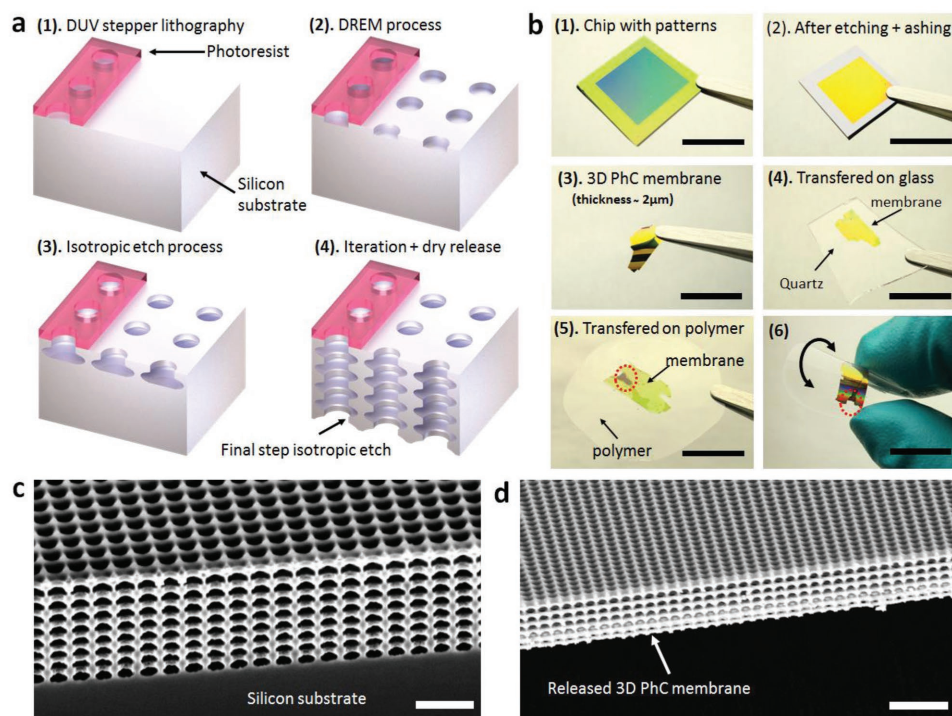

Figure 1. a) Fabrication process of 3D photonic crystal membranes, which includes pattern definition with DUV stepper lithography (1), iterative DREM process (2) and isotropic etch (3), and final step of dry release to detach the membrane from silicon substrate (4). b) Photographic illustration of the process flow, which shows the chip with pattern area of 1×1 cm^2 (1), chips after etching process and plasma ashing to remove the photoresist (2), freestanding 3D photonic crystal membranes (3), membranes transferred on a piece of quartz (4), membranes infiltrated and transferred on a piece of flexible polymer plate (5), and the sample from (5) being bent (6), scale bars 1 cm. c) SEM image of 3D PhCs with eight periods before last step of dry release, scale bar 1 μm. d) SEM image of freestanding 3D photonic crystal membranes with six periods after dry release, scale bar 2 μm.

can be achieved resulting in a polymer membrane integrated with a 3D PhCs membrane (Figure 1b6), to fabricate flexible photonic devices. The scanning electron microscopy (SEM) images show the 3D PhCs fabricated on the silicon substrate before final release (Figure 1c) and in the membrane form (Figure 1d). After peeling off from silicon substrate, the structure of membrane remains intact.

There are several technical challenges that we had to address during the fabrication process. The first is that the silicon-to-air volume ratio during the isotropic etch step can reduce to less than 10%, thus a proper isotropic etch time should be chosen. Otherwise, the layers can delaminate from each other (as shown in Figure S3, Supporting Information). Another effect that needs to be considered is the ARDE, which is especially prominent for hole-like structures, due to ion shadowing[16] and the poor depletion of etching reactants in a confined space, and the etch rate can drop significantly when the aspect ratio increases. When the etch process goes deeper into the structures, the etch rate will be aspect ratio dependent and the etch process will slow down gradually, thus the periodicity of the structures will be compromised. In our process, both the etch step during DREM process and the isotropic etch step are ramped along with the process time (a technique we call parameter ramping), so the possible shape nonuniformity is compensated and precise periodicity can be achieved (a comparison of profiles with and without parameter ramping is shown in Figure S4, Supporting Information).

2.2. Characterization of 3D Photonic Crystal Membranes

The fabricated 3D PhCs membranes have a well-defined SC structure as shown in **Figure 2**a, in which a unit cell is also labeled. The width a of the cubic cell is 400 nm, and the diameter d of the lithography patterns is around 250 nm. A void with diameter larger than 400 nm is created during the isotropic etch step, such that each unit cell is connected with its neighboring cells, resulting in a strong shape modulation. Based on the volume proportion of silicon in different layers, a large refractive index contrast of around 1.53 is estimated along the direction of the holes. In some cases, silicon single crystalline structures could be damaged during the plasma etching process due to UV irradiations or ion bombardments, thus the refractive index, especially the absorption coefficient, could change. To rule out this effect, X-ray diffraction (XRD) measurements were performed for both a silicon dummy wafer and a 3D PhC membrane on top of glass; the spectra are shown in Figure 2b. We can clearly see the sharp diffraction peak of (400) silicon crystalline plane at around 69.24°, which suggest a good single crystalline quality after plasma etching process (the peak with lower intensity at around 61° corresponds to the Cu Kβ radiation source). We measured the reflection spectrum of fabricated 3D PhC membranes on glass substrate at incident angles of 7.5°, 15°, and 30° with a goniometer stage and broadband optical spectrometer as shown in Figure 2c. A strong reflection peak at $\lambda = 1100$ nm is present, which fits well with

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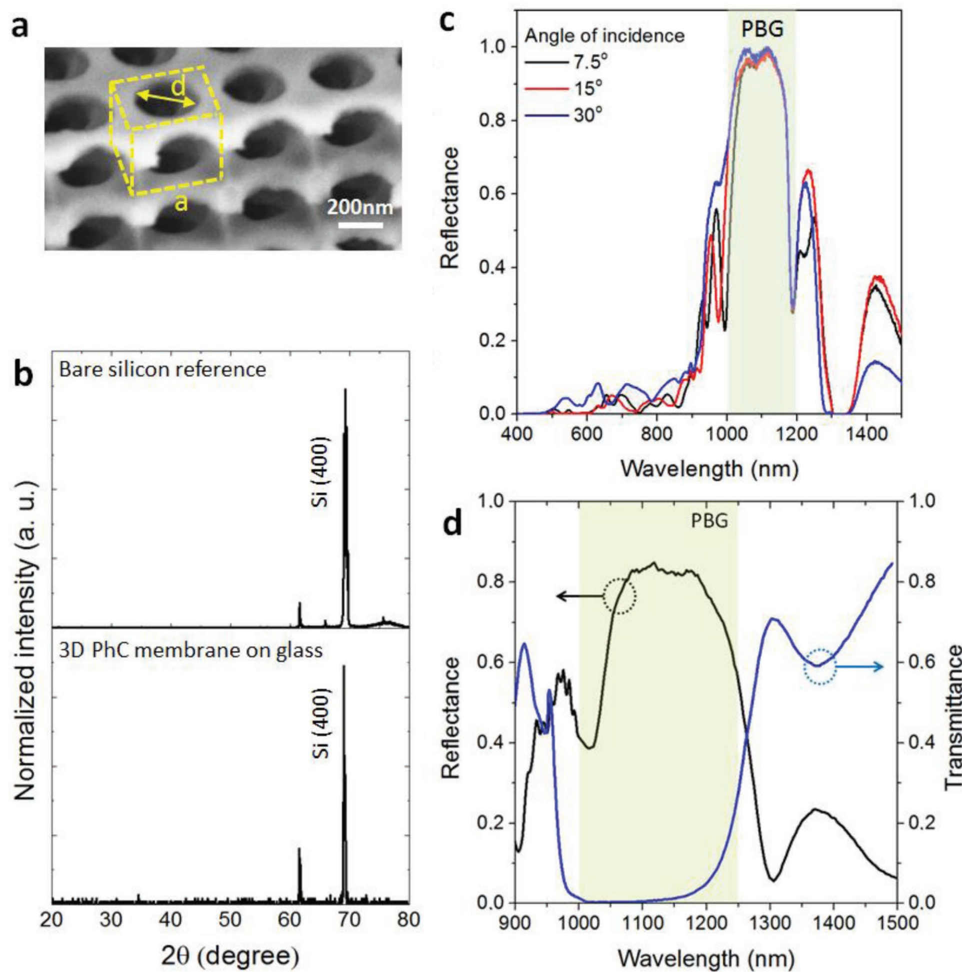

Figure 2. a) SEM image of fabricated 3D PhC structures, in which a unit cell is labeled with yellow lines; b) XRD measurements of a bare silicon wafer and 3D PhC membranes on top of glass substrate; c) reflection spectrum of 3D PhC membranes on glass measured with three different angles of incidence using goniometer stage and an optical spectrometer; d) reflection and transmission spectrum of 3D PhC membranes on glass measured by ellipsometry (incident angle of 45° for reflection measurement).

the band-edge position as in previous studies for 3D PhCs with SC geometry.[14] The gap to mid gap ratio $\Delta\lambda/\lambda = 18\%$. Reflection and transmission spectrum were also measured with an ellipsometer as shown in Figure 2d, displaying the low transmittance in the PBG region (the reflectance was measured with 45° incident angle, while the transmittance was measured with 0° incident angle).

Since the fabricated 3D PhC membranes have the advantage of large surface area, the reflectance spectrum can be easily measured by a compact spectroscopic ellipsometer without focused probes. To prove the fabricated 3D PhC membranes have complete PBG, the reflectance spectrum was measured with varying incident angles θ in a large range from 45° to 75°, and the incoming angle φ as 0° and 45°. To demonstrate both sides of the membranes have the same optical properties, we also measured the reflection spectrum from both top side and bottom side of the 3D PhCs membranes on top of glass, as shown in **Figure 3**a. The measured spectrum agrees with the measurement made using a standard spectrometer in Figure 2c, showing a significant reflectance peak in the bandgap region. The band diagram is also calculated by finite-difference time-domain (FDTD) simulation (Figure S5, Supporting Information), suggesting a complete bandgap, and the position of measured reflectance peak fits nicely with the calculated bandgap position. The reflection spectrums along the (110) plane for 3D PhC membranes on different substrates are compared in Figure 3b. The reflection maxima and the band-edge position coincide well with each other for 3D PhC membranes on glass and on silicon, while for the membranes infiltrated with a low refractive index polymer (Efiron, refractive index $n = 1.404$ at $\lambda = 852$ nm after curing by UV light), the band edge was redshifted by around 80 nm, which is expected. Since the void in the structures is replaced by polymer with a higher refractive index of around 1.3, the mean refractive index will increase and position of band edge will shift to a lower frequency range. Besides, the SC structures might be distorted due to the strain introduced by polymer infiltration, thus the reflection spectrum might be altered compared with a free standing membrane on glass or silicon. When increasing the number of periods for 3D PhCs from four layers to eight layers, we could

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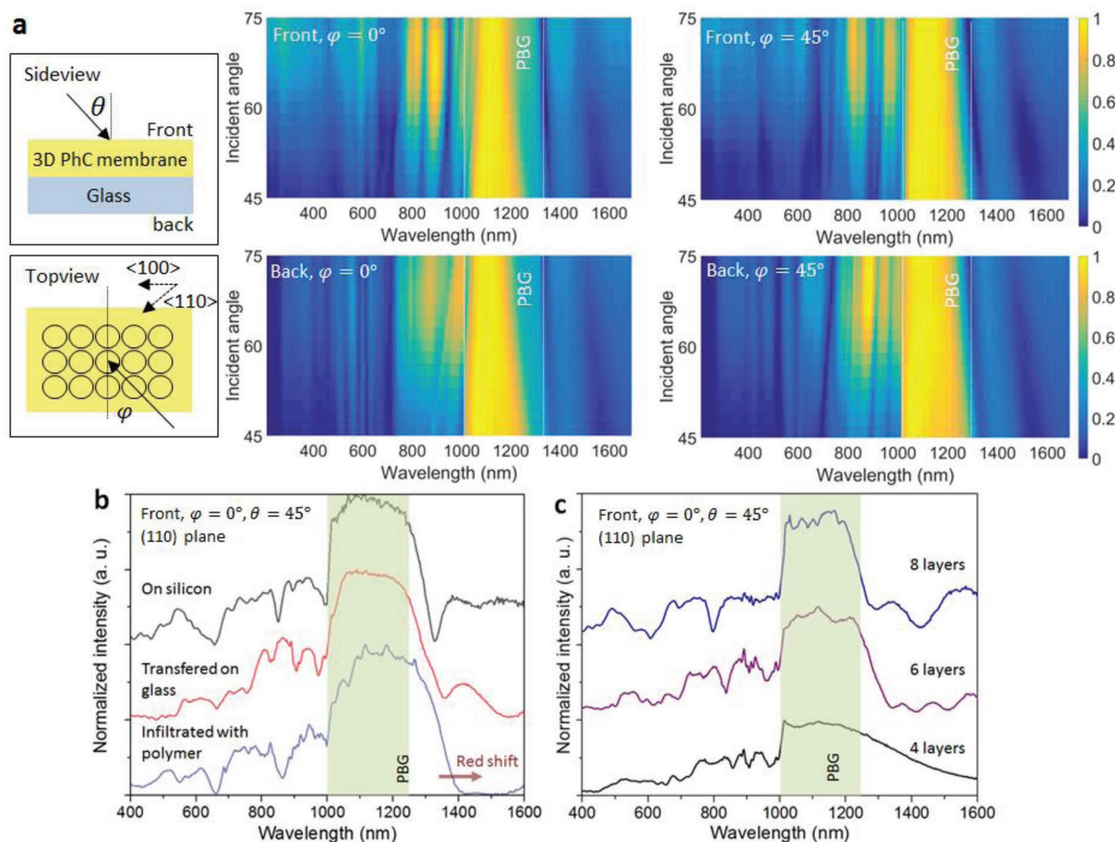

Figure 3. Reflection spectra measured by ellipsometry. a) A schematic view of the 3D PhC membranes on glass substrate, and measured reflection spectrum from both the front and back side of the sample with different incident angles, which show a clear bandgap region at around 1100 nm; b) reflection spectrums of 3D PhC membrane on different kinds substrates: silicon, glass, and polymer; c) reflection spectrums with different numbers of repeating layers of 3D PhC membranes on glass substrate.

clearly see the development of the PBG, as the reflection in mid gap position increases by around 60%.

As already shown in Figure 1b5, the fabricated 3D PhC membranes could be easily infiltrated by polymer, and the integrated 3D PhC membranes on the polymer possess mechanical flexibility and can be bent in a large scale without collapse, which implies the potential for flexible and wearable photonic devices. It should also be noticed that shear strain can be introduced in 3D PhC structures when the polymer membrane is bend, thus the SC geometry will be distorted as shown in **Figure 4**a, where the shear strain can be as large as 0.48. The band structures will also be modified, thus realizing tunable and flexible photonic devices that can be compatible with biological systems,[23,24] which will be interesting to investigate, but are not within the scope of this article. Apart from polymers, some high refractive index materials could also be infiltrated and coated conformally on the 3D PhC membranes by atomic layer deposition (ALD) method. Figure 4b is a 3D PhC membrane coated with titanium dioxide (TiO_2) on a glass as substrate. The energy dispersive X-ray (EDX) mapping shows a uniform coating of TiO_2 on the membrane. When the thickness of TiO_2 increases from 10 to 15 nm, the band edge is redshifted due to the increased average refractive index, while the reflection intensity decreases significantly, which is supposed to be caused by the increased volume ratio of high refractive index materials, thus the complete PBG closes. However, it should be mentioned that in order to achieve a better optical performance of fabricated PhCs, it is an efficient method to coat 3D PhC structures with materials with better thermal or optical properties,[25] or creating inverse structures and replicas with other materials.[26,27] By carefully choosing the dimensions of the 3D PhC membranes, it should be possible to make inverse 3D PhCs with other materials, which is a subject of future study.

2.3. Embedded Planar Cavities and Applications

To enable the functionalities of 3D PhCs for the purpose of light manipulation, defects are introduced into the structures, such as planar cavities, single point defect, or even complex 3D waveguides which can guide the light in three dimensions.[28] Planar defects have been studied mostly for different configurations of 3D PhC.[29–31] Here, we will show how a planar cavity could be introduced into our 3D PhC membranes for different applications. **Figure 5**a is a free standing 3D PhC membrane with six periods; the cross section shows a good size uniformity for six layers. Figure 5b is a free standing 3D PhC membrane with seven layers, with a defect layer embedded in the middle with a thickness of around 300 nm. The planar defect was introduced simply by increasing the number of DREM cycles

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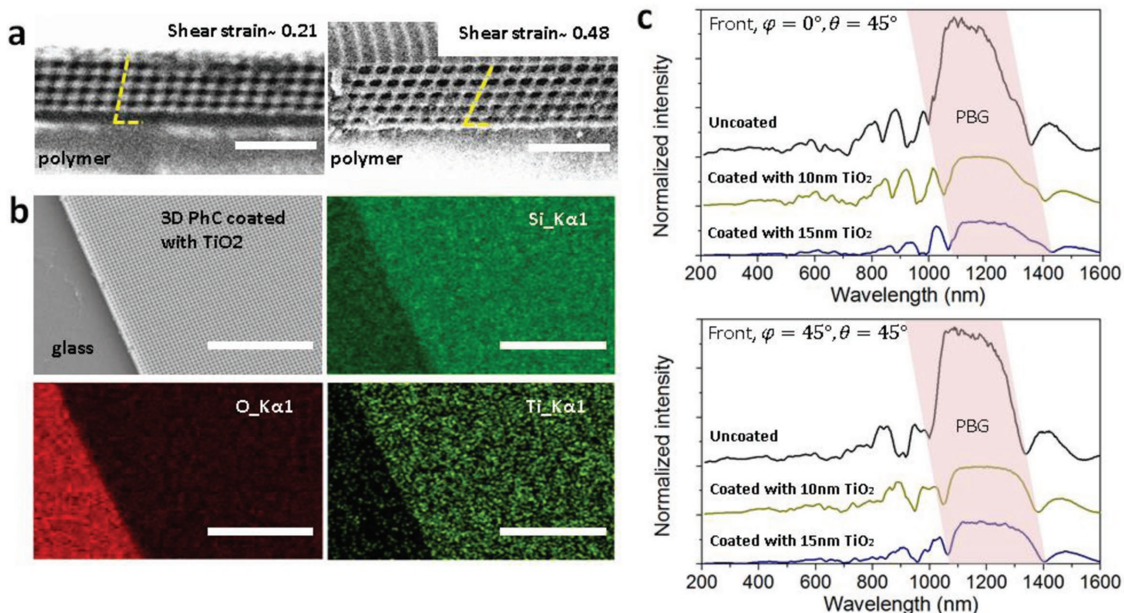

Figure 4. a) 3D PhC membranes infiltrated with polymer under shear stress (scale bars 2 µm); b) SEM image and EDX mapping of 3D PhC membrane coated with 15 nm TiO_2 by ALD (scale bars 10 µm); c) reflection spectra of 3D PhC membranes coated with different thickness of TiO_2, with glass as substrate.

for the fourth layer, while the other layers remain in good size uniformity. The reflection spectrums for 3D PhC membranes on glass substrate with and without embedded planar defects are shown in Figure 5c,d. Since photonic states are introduced in the stop band by the planar defects, a resonance could be clearly seen in the PBG region, which should otherwise be free from photon propagations. The resonance has a linewidth of around 30 nm, and can be observed with incident angles from

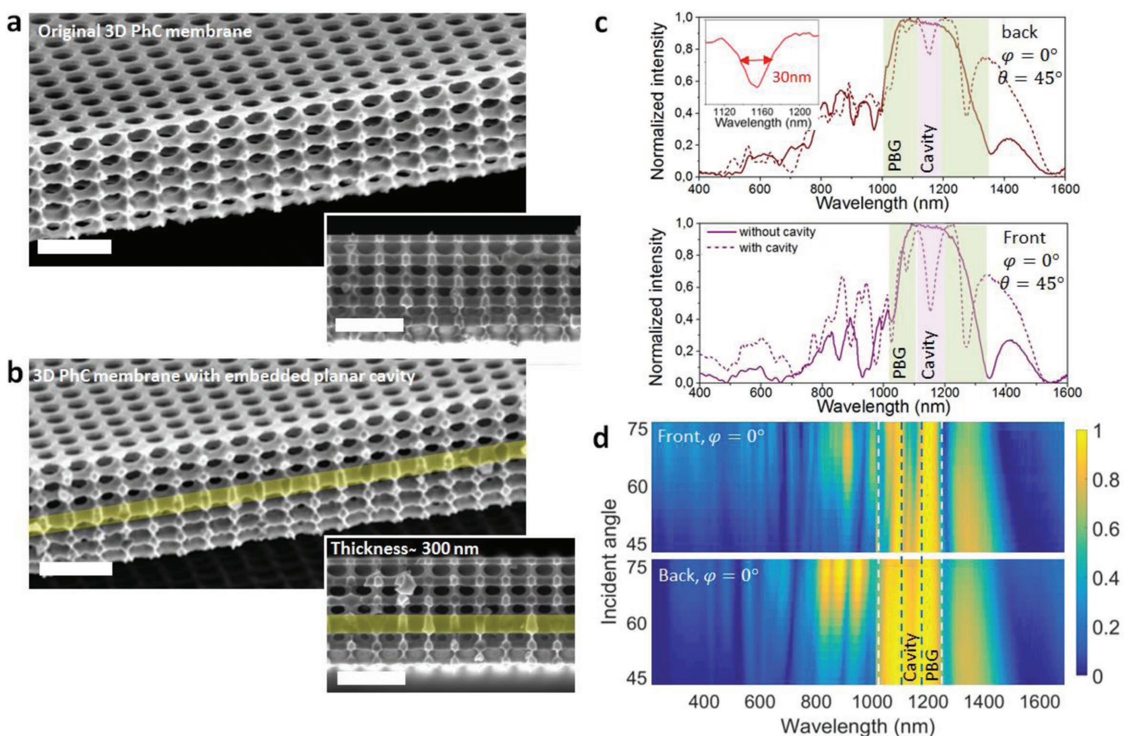

Figure 5. 3D PhC membranes with embedded planar cavity. SEM image of freestanding 3D PhC membranes a) without cavity and b) with planar cavity, scale bars 1 µm; c) the comparison of reflection spectra, which shows a cavity resonance mode in the PBG with a linewidth of 30 nm; d) the reflection spectrum of a 3D PhC membrane (with cavity) on glass, with different incident angles.

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45° to 75° from both the top side and the bottom side of the membranes. It should be addressed that there are several resonance dips near the bandgap position on the spectra. This is possibly due to the high volume ratio of silicon dielectric defect, which can host multiple localized resonance modes,[32,33] while for silica planar defects[30,31] or air defects,[7] only a single resonance dip can be observed, which is generated by the basic dipole resonance state or monopole state. To further increase the quality factor of the planar cavity resonance mode, the effective cavity length should be increased, e.g., by increasing the number of repeated defect-free layers to achieve a better confinement of states in the cavity region. A thermal annealing process is also promising to reduce the roughness on structure surfaces, thus less scattering loss is generated and the quality factor can be increased for a sharper resonance dip.

The porous structure of fabricated 3D PhC membranes enables solvents and gases to easily infiltrate, thus the refractive index can be tuned in a controllable manner. Here, we applied ethanol with different concentrations (in deionized water) onto the 3D PhC membrane with glass as the substrate. The reflection spectrum was then measured using an ellipsometer at an incident angle of 45°. A redshift could be observed both for the band edge of the reflection peak and the resonance mode of the planar cavity as shown in **Figure 6**a. This can be explained as the electromagnetic confinement in the silicon cavity region started to leak inside the surrounding medium of the solvent with a higher refractive index than air, and both the air band and dielectric band will be suppressed to a lower frequency level. The correspondence between the center wavelength of the resonance mode and the refractive index of infiltrated solvent is recorded and shown in Figure 6b, which suggested a sensitivity of around 397 nm RIU^{-1}. This is comparable with the result from silk inverse opal structures.[34,35] After each measurement, the sample can be soft baked to let the solvents fully evaporate from the porous structures, thus making it suitable for multiple usage for sensing gases or solvents.

We also transferred the fabricated 3D PhC membranes onto substrates with engineered surfaces as shown in Figure 6c (more SEM images with details is in Figure S6, Supporting Information), which can be difficult with traditional 3D PhC structures. The substrates we used were highly-doped black silicon created by Bosch etch process, which is known to exhibit room

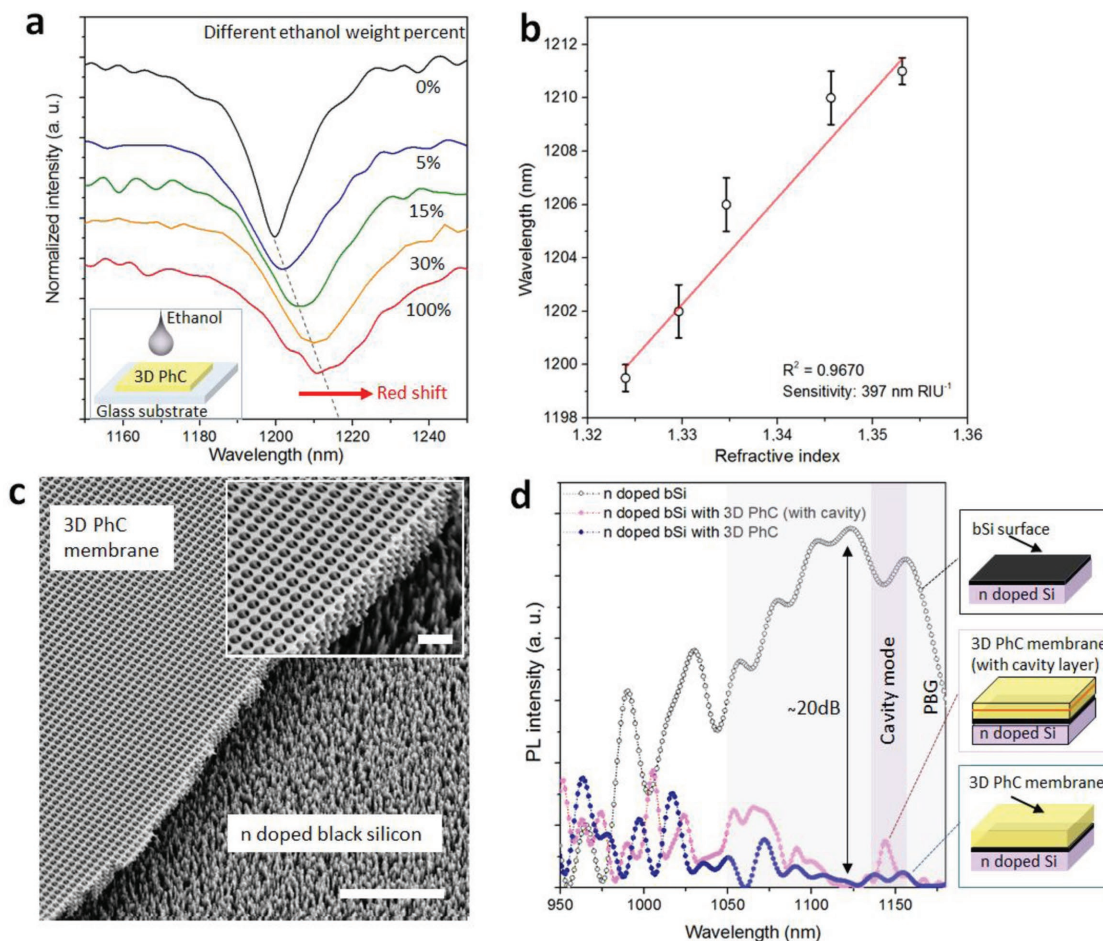

Figure 6. Applications of 3D PhC membranes with embedded planar cavities. a) The redshift of the resonance peak when ethanol solution with different concentrations (in deionized water) is applied on the membrane. b) The relation between the resonance peak wavelength and refractive index of ethanol solutions. c) SEM images of transferred 3D PhC membranes on n-doped black silicon substrate, scale bars 5 µm, with a close up view in the inset, scale bars 1 µm; d) the PL intensity with a black silicon reference sample, black silicon sample covered with 3D PhC membranes, and black silicon sample covered with 3D PhC membrane with an embedded planar cavity.

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temperature band-edge PL NIR wavelengths.[22] Photoexcitation was performed with a 532 nm continuous wave (CW) laser, allowing detection of the PL signals with an InGaAs detector. When the surface of the black silicon was covered with a 3D photonic crystal membrane (with six periods, thickness of around 2 µm), the PL intensity in the PBG region was suppressed with an attenuation rate of around 20 dB as shown in Figure 6d, while the PL signal could still be detected in the wavelength away from PBG region. When a membrane with a planar cavity was transferred on top of black silicon, the PL intensity in the bandgap region was still low, but had a noticeable peak at the wavelength of cavity resonance mode, which in this case acted as an optical bandpass filter. However, due to the optical absorption of the silicon material at 532 nm, the PL intensity at resonance wavelength was also reduced. Nevertheless, this demonstrates the possibility to apply the 3D photonic crystal membranes as an optical bandpass filter that is adaptable for different substrates.

3. Conclusions

In this work, we have demonstrated a one-step fabrication process for 3D photonic crystal membranes. The fabricated membranes have a thickness of around 2 µm with excellent mechanical stability. Reflectance spectra were recorded at different angles of incidence from 7.5° to 75°, suggesting a complete PBG structure with a peak reflection at around 1100 nm. We transferred the fabricated membranes (manually, using tweezers) onto different substrates such as glass or black silicon surfaces. A soft 3D PhC membrane could be achieved by infiltrating the structures with polymer. In addition, we demonstrated that a planar defect can be conveniently introduced into the 3D PhC structures during the fabrication process, giving an optical resonance mode coupled with the stop band. The narrow resonance peak of around 30 nm linewidth can be used for sensing the concentrations of organic solvents. The PL from black silicon could be filtered effectively by 3D PhC membranes with the incorporated planar defect. Our study provides a convenient strategy for large scale fabrication of flexible 3D PhC membrane structures with the feasibility to introduce planar cavities and possibilities for integration on different photonic devices. We have shown the feasibility of some practical applications within optics and chemical sensing. Other obvious application areas include biological sensors (e.g., in connection with bacteria/cell growth) as well as optical communications and lasers. The whole fabrication process is performed by standard fabrication technologies in the semiconductor industry and is CMOS compatible.

4. Experimental Section

DUV Stepper Lithography: Silicon wafers (150 mm, n-doped, <100> orientation) were first coated with 65 nm thick bottom antireflective coating (BARC, DUV42s-6, Brewer Science) layer in a spin coating system (Gamma 2M, Süss). Afterwards, a 360 nm thick DUV resist (JSR KRF M230Y, JSR-Micro) was coated on top of the BARC layer. Patterns were exposed with a DUV stepper lithography system (FPA-3000EX4, Canon), which was equipped with a 248 nm KrF excimer laser (intensity 280 mW cm^{-2}, dose 21 mJ cm^{-2}, and focus depth 0.17 µm). Finally, the samples were developed in AZ726 (AZ Electronic Materials).

Plasma Etching: The plasma etching process was performed in a dual source inductively coupled plasma (ICP) etching system (DRIE Pegasus, SPTS). Samples with patterns after lithography were diced manually into pieces (around 1.5 cm × 1.5 cm) and attached on an alumina coated silicon carrier wafer using a small amount of Fomblin oil (Solvay Solexis S.P.A.), a kind of chemically inert perfluoropolyether vacuum oil with good thermal conductivity. The alumina was coated by a R200 ALD system (Picosun), the thickness was measured to be 100 nm.

Transfer of 3D PhC Membranes: 3D PhC membranes were released from bulk silicon substrate during etch process, which could be easily peeled off using tweezers and then manually transferred onto glass substrates. To transfer and infiltrate the 3D PhC membranes with polymer, Efiron PC-404 (Lucantix, South Korean) was first applied onto the membranes (with a silicon wafer treated with an anti-stiction layer of 1H,1H,2H,2H-Perfluorodecyltrichlorosilane as a substrate), and then cured under UV lamp for 5 min (13.5 mW cm^{-2} at 365 nm); afterwards, the hardened resist was released together with 3D PhC membranes from the silicon wafer.

Characterizations of Structures: The thickness of the BARC layer and resist were measured by a spectroscopic ellipsometer (Vase, J.A. Woollam Co., Inc.). SEM (Supra V60, Zeiss) images were taken to characterize the dimension and morphology of the structures. Crystallographic information of fabricated samples was collected with a high-resolution X-ray diffractometer system (SmartLab, Rigaku), which was equipped with a Cu Kα radiation source (1.54 Å).

Characterizations of Optical Properties: The reflection and transmission spectrums were measured by a spectroscopic ellipsometer (Vase, J.A. Woollam Co., Inc.) with incidence angle from 45° to 75°, the spot size was 1 mm × 1 mm, and the wavelength ranges from 200 to 1600 nm. The reference sample was a silicon wafer deposited with 25 nm SiO_2. To confirm the result of measurements over broader angles of incidence, the reflection spectrum was also measured at incident angles of 7.5°, 15°, and 30° using a goniometer stage (Gon360 from Instrument systems) and a broadband optical spectrometer (Spectro320 from Instrument Systems) with a wavelength range from 400 to 1600 nm. Reflectance measurement of a silver-coated mirror was used as a reference. A broadband light from a Xenon lamp (HPX2000 from Ocean Optics) was used as a source for the reflectance measurements.

PL Measurement: The PL measurement was carried out on RPM2000 Rapid Photoluminescence Mapper (Nanometrics). The black silicon reference samples were fabricated with a Bosch etch process from an n-doped silicon wafer (antimony doped, resistivity <0.25 Ohm cm, doping concentration around 2 × 1028 cm^{-3}). The samples were then cleaned with plasma ashing (400 sccm O_2, 70 sccm N_2, with coil power of 1000 W). A CW laser source of 532 nm (with the power of 7.11 mW) and an InGaAs detector were used.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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