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InGaN/(GaN)/AlGaN/GaN normally-off metal-oxide-semiconductor high-electron mobility transistors with etched access region

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The proposal and processing aspects of the prove-of-concept InGaN/GaN/AlGaN/GaN metal-oxide-semiconductor (MOS) high-electron mobility transistor with etched access regions are addressed. Full strain and decent quality of the epitaxial system comprising 4 nm $In_{0.16}Ga_{0.84}N$/3 nm GaN/5 nm $Al_{0.27}Ga_{0.73}N$ are observed using a high-resolution transmission-electron microscopy and by deformation profile extractions. Large negative polarization charge in the MOS gate stack provides the HEMT normally-off operation, while free electrons are populated at access regions after etching. Consecutive passivation by 10 nm Al_2O_3 together with annealing at 300 °C improved the Al_2O_3/semiconductor interface, with the threshold voltage (V_T) reaching 1 V. Improvements of the present concept in comparison to the previous one with a gate recess were proved by showing the decreased drain leakage current and increased breakdown voltage.

1. Introduction

Increase of a positive threshold voltage (V_T) in GaN-based transistors is needed for safe operation of high-performance switches and logic circuits.[1–9] Several methods were successfully applied to manipulate V_T in true high-electron mobility transistors (HEMTs) without removing a quantum well (QW) high-mobility channel. Among them are fluoride implantation to barrier,[1)] p-GaN capping,[2,3)] gate stack polarization engineering,[4–6)] or reduction of a surface donors density.[7,8)] In these concepts an additional negative charge is introduced in a gate region and consequently an energetic band structure is raised while electrons are depleted from the QW. Among these methods, taking into account a high negative polarization charge at possible hetero-junctions such as InGaN/GaN,[10)] surprisingly less effort was invested in exploring polarization engineering. In contrast, in a more matured concept of p-GaN capping, only limited activation of Mg could be expected.[11,12)] As pointed out by us recently, setting a high V_T can be achieved by combining polarization engineering and increasing the oxide thickness in the metal-oxide-semiconductor (MOS) gate stack.[6)] Still, several issues remain to be solved in the reported gate-recessed polarization-engineered n^+ GaN/InGaN/AlGaN/GaN normally-off MOS HEMT: the need for supplemental p-doping, and testing of the alternative InGaN/(GaN)/AlGaN/GaN heterostructure with access region etching.[6)] In this way, by combining polarization and p-doping,[13)] an unprecedented hole concentration and predictive V_T scalability above +5 V can be expected.[6)] On the other hand, avoiding gate recess may provide a less spoiled MOS interface with more stable V_T,[14)] while removing InGaN at access regions may lead to lower drain leakage and higher breakdown voltage.[6,15)] However, carefully controlled removal of the capping layer with consecutive surface passivation of the AlGaN surface is needed to provide HEMT low access resistance, similarly as in conventional p-GaN/AlGaN/GaN HEMTs.[16)] Special concerns may arise also due to possible leakage current along the etched sidewalls of the gate region.[17)] Moreover, proper design of the InGaN/(GaN)/AlGaN/GaN heterostructure must avoid possible relaxation of the strained InGaN layer.[18)]

In the present work, we study InGaN/GaN/AlGaN/GaN normally-off MOS HEMTs with etched access region. 3 nm thin GaN is introduced between InGaN and AlGaN to provide a tolerance for the etch termination, and for better control of the composition. The heterostructure is grown using metal-organic-chemical-vapor deposition (MOCVD), while high-resolution transmission-electron microscopy (HRTEM) is used to monitor strain evolution in the stack. No p-doping is applied in the present study; focus is given to processing steps. In particular, the Al_2O_3 passivation layer is introduced at access regions after the etching, which is followed by rapid thermal annealing (RTA) to remove the plasma-induced damage.[13,19)] Devices and sequential processing steps are studied using *dc* current–voltage characterizations.

2. Experimental methods

The epi-structure was grown by MOCVD using a AIXTRON 3×2 CCS system on a sapphire substrate starting with a low-temperature GaN nucleation layer, 1.6 μm thick C-doped GaN buffer and 200 nm un-doped GaN channel layers. Following QW growth was set to provide a 1 nm AlN spike, 5 nm $Al_{0.27}Ga_{0.73}N$, 3 nm GaN, and 4 nm $In_{0.16}Ga_{0.84}N$ on top. The calculated energy band diagram using a Schrödinger–Poisson equation solver[20)] and the device schematic view are shown in Fig. 1. The channel is fully depleted under the gate as the energy diagram is raised up by the high-density negative polarisation charge reaching $\sim 4 \times 10^{13}\,cm^{-2}$ combining both interfaces of the InGaN/GaN/AlGaN system, see Fig. 1(a). On the other hand, after the etching as theoretically predicted in Fig. 1(b), access regions become fully populated with free electron density reaching $\sim 1 \times 10^{13}\,cm^{-2}$. Thus, this will minimise access resistances and calculated sheet resistance was about 610 Ω/□. Moreover, removing the low-band gap InGaN at access regions, see Fig. 1(c), may have also additional positive consequences, by increasing the device breakdown voltage

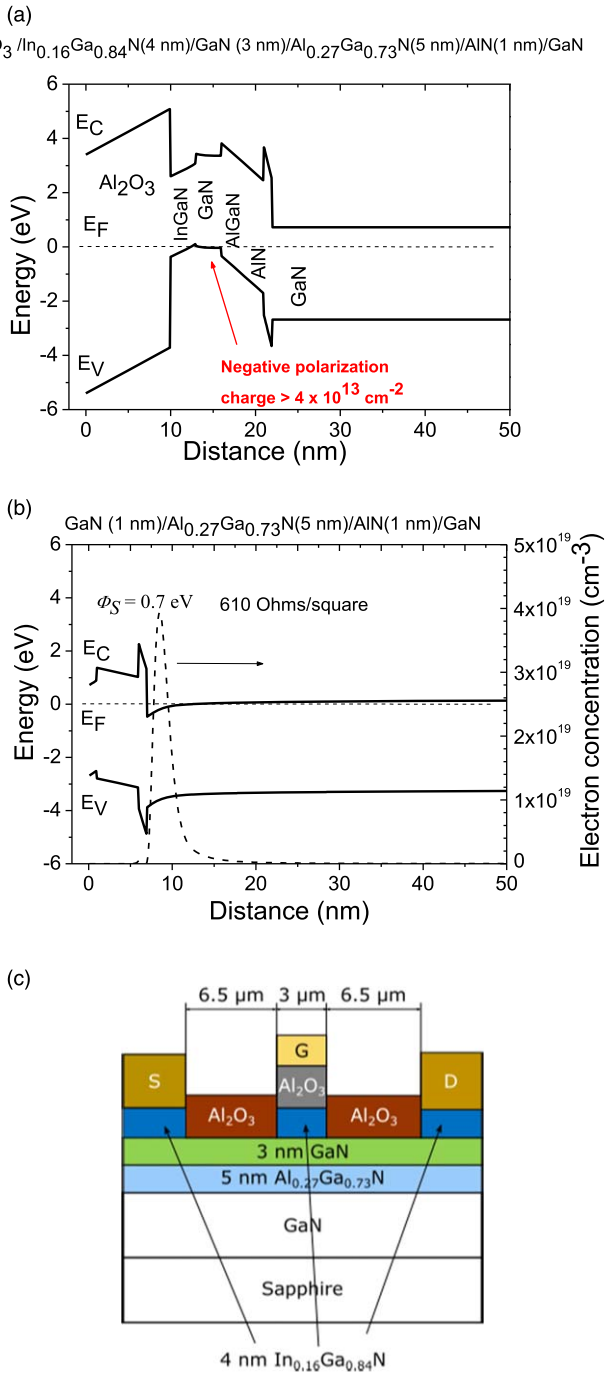

Fig. 1. (Color online) Calculated energy band diagram in the (a) gate stack cross-section and (b) cross-section of the etched access region, together with the electron density in populated QW. (c) Schematic view of the processed HEMT. Arrow in (a) points to the calculated density of the negative polarization charge ($\sim 4 \times 10^{13}$ cm^{-2}).

and by decreasing the possibility for detrimental drain leakage current. This will be studied in our following experiments. As a reference sample, also an uncapped $Al_{0.27}Ga_{0.73}N$(5 nm)/AlN(1 nm)/GaN QW has been grown and characterised by Hall experiment.

For structural and strain analysis, after the cross sectional preparation, the Ar ion milled specimens were studied in a HRTEM (JEOL 3010) as well as in an aberration corrected TEM (FEI Themis). The obtained HRTEM images were analysed by the method of Refs. 21,22 to quantitatively determine the strain field in the heteroepitaxial structure. Phase images were calculated from the raw HRTEM image using the signed reflections on the FFT image and using a reference area in the GaN layer. Elemental composition of studied samples was obtained by energy dispersive spectroscopy (EDS).

By device processing, mesa definition was performed by $SiCl_4$-based plasma etching, Ti/Al/Ni/Au ohmic contacts were formed 16 μm apart and annealed at 750 °C. 3 μm long and 60 μm wide photoresist mask was applied by depositing a 10 nm thick Al_2O_3 gate insulation in an atomic-layer deposition (ALD) system using trimethylaluminium and water at 100 °C. No particular InGaN surface treatment was applied prior to ALD. Next, Ni/Au metal together with the oxide was lifted-off to form the self-aligned MOS gates.[8,9] Access region etching was performed using $SiCl_4$:SF_6 (4:1) gas mixture in the inductive-coupled plasma reactive-ion etching (ICP RIE) system at 2.7 Pa keeping self-induced bias of about 75 V. The etching process (InGaN removal and reaching of the AlGaN surface) was calibrated by measuring the heterostructure sheet resistance using the transmission-line method (TLM) structure and/or by measuring the etching depth by AFM. Passivating 10 nm thick Al_2O_3 was again grown by ALD. RTA at 300 °C for 10 min finalized the processing. *dc I–V* characterizations were performed using a Keithley 4200 SCS.

3. Results and discussion

While a normally-off heterostructure was too resistive for the Hall experiment, the reference $Al_{0.27}Ga_{0.73}N$(5 nm)/AlN(1 nm)/GaN QW showed free electron concentration of 1×10^{13} cm^{-2} and mobility of 650 cm^2 V^{-1} s^{-1}. We assume that also in this case the data are influenced by the vicinity of the surface.

As shown in Fig. 2, the structure of the InGaN/GaN/AlGAN/GaN layer stack was found epitaxial with no lattice defects observed except some threading dislocations originated at the GaN/sapphire interface. The low-temperature deposited ALD oxide film under the gate was amorphous but rapidly crystallized under the focused electron beam.

The deformation maps of Fig. 2(a) were calculated by GPA software implemented into Digital Micrograph.[23] It is shown that the in-plane deformation profile does not change relative to the GaN (ε_{xx} of the strain tensor) but significant strain is observed in the normal direction (ε_{yy}). The lattice of the InGaN layer was extended by 3%–4%, while that of AlGaN is shrunken by about 2%. That finding proves fully strained layers are needed for our concept. The profile of the thin AlN spike between GaN and AlGaN was found to be sharper in the aberration corrected microscope because of its better resolution and less delocalization. About 2 nm wide transitions were observed at the interfaces. The deformation profile gained from GPA in the vertical direction follows the chemical variations of the EDS profile of the grown layers shown in Fig. 2(b).

As expected, Fig. 3 shows TLM sheet resistance dropping from $\sim$10 MΩ/□ of the virgin structure down to $\sim$10 kΩ/□ after removing InGaN. The sheet resistance dropped further down to $\sim$3 kΩ/□ after passivation and annealing, but was still inferior to $\sim$1.2 kΩ/□ of the reference un-passivated AlGaN/GaN. This may be a consequence of an un-sufficient duration of etching, leaving some GaN (or even InGaN) still in place. In future, the ambiguity of the etching may be

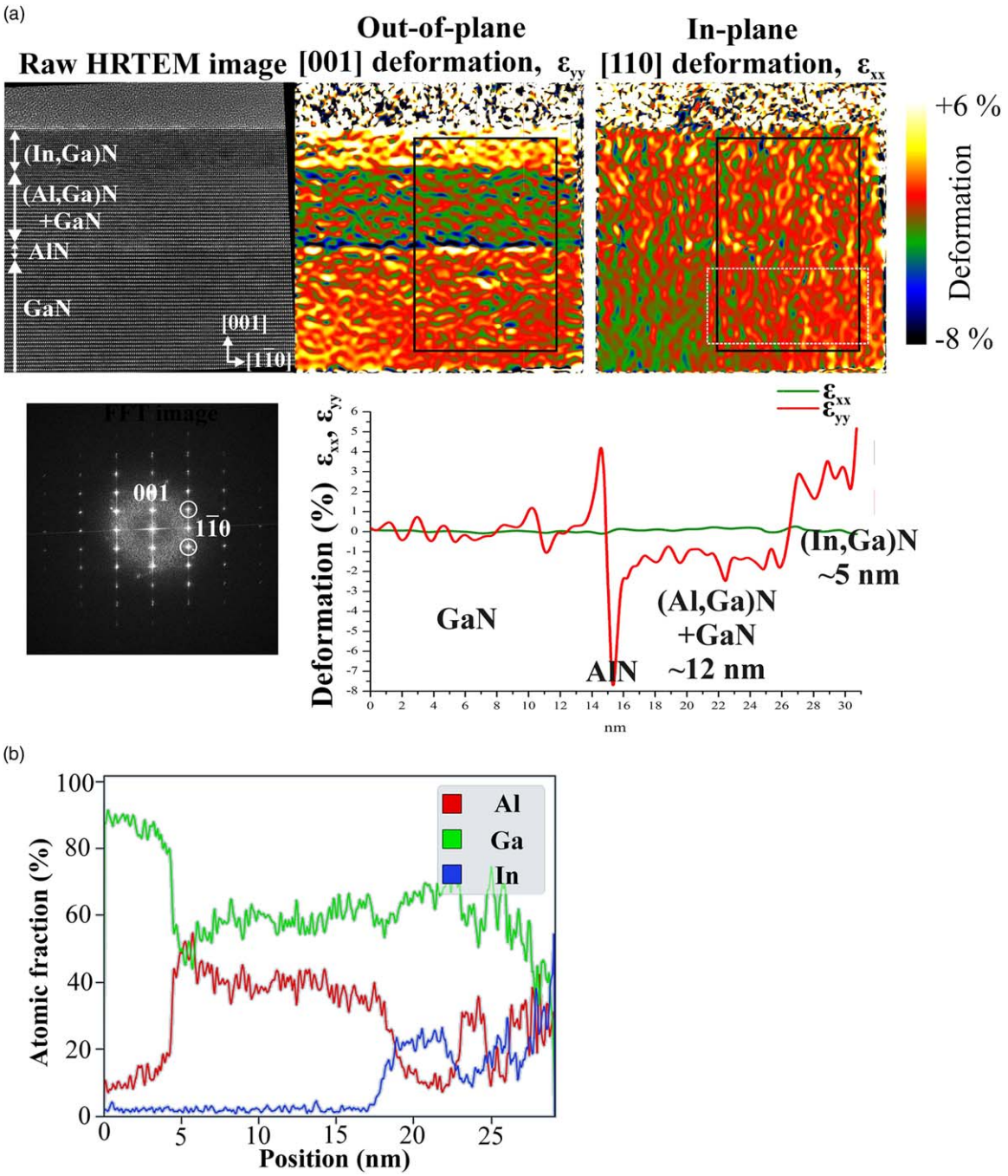

Fig. 2. (Color online) (a) A HRTEM image in the [11–20] crystallographic zone taken from the top of the sample with corresponding FFT image and deformations maps. (b) EDS elemental analysis. The local strain/deformation variations are obtained with GPA (resolution: about 1 nm). The colored figures show the two main components of the strain tensor, ε_{yy} (out-of-plane [001] deformation) and ε_{xx} (in-plane [1–10] deformation), respectively, calculated using phase images. Phase images (not presented here) were calculated from raw HRTEM image using the signed reflections on FFT image and using a reference area in the GaN layer (signed with white stripped rectangles in the in-plane deformation map).

solved by introducing an AlN etch-stop layer;[24] nevertheless present data are fully sufficient for testing the viability of the proposed new concept.

Figure 4 shows evolution of transfer characteristics after consecutive processing steps, by sweeping *I–Vs* from the off-state to on-state and back, with $V_{DS} = 8$ V. In all cases, a right-hand shift in I_{DS} was observed during the backward sweep towards the off-state. A particularly large I_{DS} hysteresis and $V_T \sim 0$ V was observed after the etching, which was the HEMT initial vital stage, after only marginal current of the virgin (un-etched) device. Large hysteresis is often a consequence of deep levels and trapping in the MOS gate stack, particularly in normally-off HEMTs,[25,26] and increases with applied V_{GS}.[27–29] After the passivation hysteresis was largely eliminated, most likely because of decreased V_T and low V_{GS} of the normally-on operation.[25] Still after the post-deposition RTA, HEMTs become normally-off again (V_T reached ~ 1 V), while hysteresis remained marginal. Low trapping indicated that RTA at 300 °C was successful by forming the gate MOS interface even though low-temperature ALD may leave more traps.[30] On the other hand, increased gate leakage after RTA may be responsible for a less effective controllability of the HEMT and decreased maximal drain current. Also of interest is the evolution of V_T,

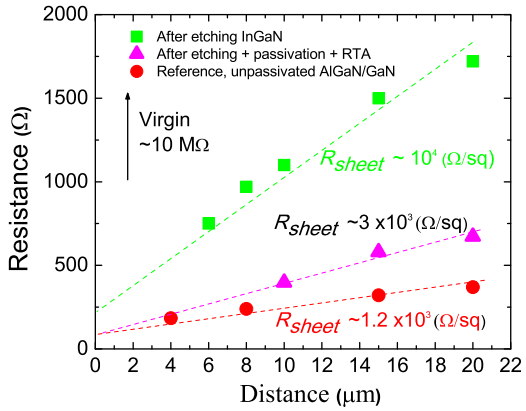

Fig. 3. (Color online) TLM data of the reference un-passivated D-mode AlGaN/GaN HEMT, E-mode InGaN/GaN/AlGaN/GaN MOS HEMT after etching InGaN at access regions and after passivation and annealing.

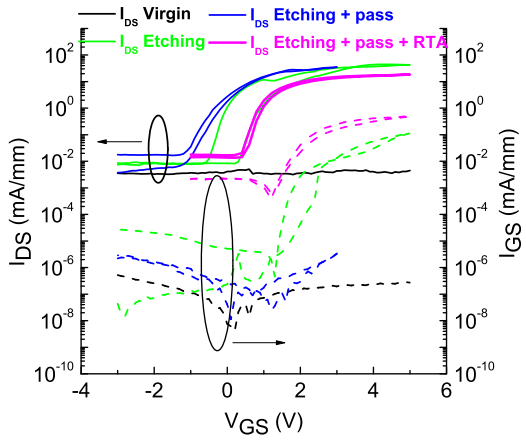

Fig. 4. (Color online) Transfer and gate characteristics of the InGaN/GaN/AlGaN/GaN MOS HEMT at different processing steps: virgin epi-structure, after etching InGaN, after passivation and after passivation and annealing.

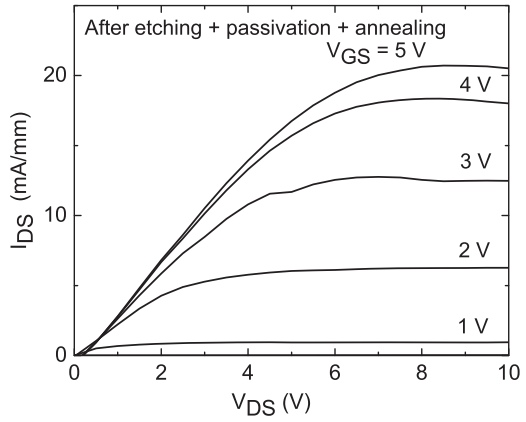

Fig. 5. (Color online) InGaN/GaN/AlGaN/GaN MOS HEMT output characteristics after passivation and annealing.

which may follow the state of the vertical walls of the etched/passivated gate island, similarly as observed in p-GaN HEMTs.[16,17] Obviously, the passivation process of the present devices is of great importance and different recipes may be needed for optimized passivation and gate insulation. This was also observed by measuring the three-terminal I_{GS} characteristics during our processing sequence, when the lowest leakage current did not necessarily mean the best

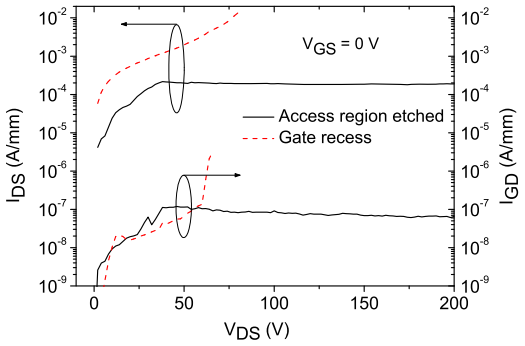

Fig. 6. (Color online) Off-state characteristics (with grounded gate) of the InGaN/GaN/AlGaN/GaN MOS HEMT with etched access region compared with gate-recessed HEMT.

HEMT sub-threshold characteristics with less trapping and the highest V_T.

Finally, in Figs. 5 and 6 we show output and off state (with grounded gate) characteristics of the processed normally-off InGaN/GaN/AlGaN/GaN HEMTs with the etched access region. Devices show decent output characteristics which however were limited with still high sheet resistance at access regions. On the other hand, fair improvements in the drain leakage current and the breakdown voltage (beyond the measuring range of Keithley 4200 SCS) if compared with the analogous gate-recessed HEMT has been recorded, proving viability of the present concept.

4. Conclusions

In conclusion we demonstrated a prove-off-concept of the normally-off InGaN/GaN/AlGaN/GaN MOS HEMTs with etched access region. Advancement in respect to the previous gate-recess concept is explained and verified. We have pointed to different technological aspects which need further optimization.

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