ACS APPLIED MATERIALS & INTERFACES

Research Article

Cite This: ACS Appl. Mater. Interfaces 2017, 9, 43993−44000

www.acsami.org

Engineering the Photoresponse of InAs Nanowires

Jack A. Alexander-Webber,*[,†] Catherine K. Groschner,[†,∥] Abhay A. Sagade,[†,⊥] Gregory Tainter,[†] M. Fernando Gonzalez-Zalba,[‡] Riccardo Di Pietro,[‡] Jennifer Wong-Leung,[§] H. Hoe Tan,[§] Chennupati Jagadish,[§] Stephan Hofmann,[†] and Hannah J. Joyce*[,†]

[†]Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, United Kingdom

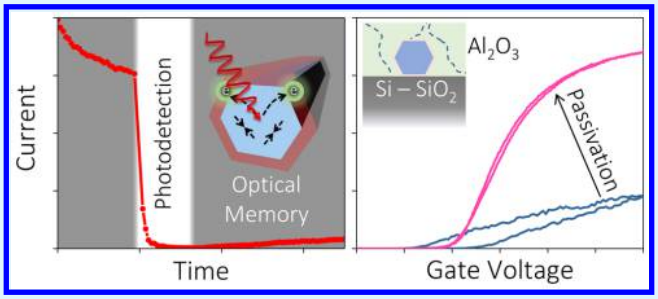
[⊥]SRM Research Institute, Department of Physics & Nanotechnology, SRM University, Kattankulathur 603 203, India

[‡]Hitachi Cambridge Laboratory, JJ Thomson Avenue, Cambridge CB3 0HE, United Kingdom

[§]Department of Electronic Materials Engineering, Research School of Physics and Engineering, The Australian National University, Canberra, ACT 2601, Australia

S *Supporting Information*

ABSTRACT: We report on individual-InAs nanowire optoelectronic devices which can be tailored to exhibit either negative or positive photoconductivity (NPC or PPC). The NPC photoresponse time and magnitude is found to be highly tunable by varying the nanowire diameter under controlled growth conditions. Using hysteresis characterization, we decouple the observed photoexcitation-induced hot electron trapping from conventional electric field-induced trapping to gain a fundamental insight into the interface trap states responsible for NPC. Furthermore, we demonstrate surface passivation without chemical etching which both enhances the field-effect mobility of the nanowires by approximately an order of magnitude and effectively eliminates the hot carrier trapping found to be responsible for NPC, thus restoring an "intrinsic" positive photoresponse. This opens pathways toward engineering semiconductor nanowires for novel optical-memory and photodetector applications.



KEYWORDS: *indium arsenide, photodetector, negative photoconductivity, optical memory, surface state, hysteresis, passivation, atomic layer deposition*

INTRODUCTION

InAs nanowires have great potential in electronics[1] and optoelectronics[2−4] due to their exceptionally high room temperature mobility,[5] narrow band gap[6,7] (ranging from 0.35 eV in bulk InAs to 0.477 eV in wurtzite nanowires[8]), and ability to host exotic quasiparticle excitations.[9] As the dimensionality of InAs is reduced, the role of surface states in determining the (opto)electronic properties becomes increasingly more important.[10−13] This is due to a combination of strong charge accumulation at the surface of InAs,[10] which enables comparatively easy Ohmic contact formation,[14] and the presence of electron trapping sites which lie in the native oxide, i.e., in very close proximity to the active channel.

In most semiconductors, photoexcitation promotes an increase in the density of mobile charge carriers, leading to an increase in conductivity, i.e., a positive photoconductivity (PPC). However, surface effects in InAs nanowires have been shown to cause an unconventional negative photoconductivity (NPC), i.e., a drop in conductivity under visible light irradiation.[15−20] After photoexcitation with a photon energy significantly above the band gap (≥1 eV),[17] free carriers in the nanowire can be promoted into above-gap charge trapping sites which lie in the native surface oxide. This trapping of photoexcited (hot) carriers can occur on the time scales of ms or less, leading to the development of fast photodetectors.[15,17] Conversely, due to a thermally activated relaxation process, NPC can be remarkably long-lived, over tens of seconds at room temperature and orders of magnitude longer at 77 K,[17−19] which may be applicable to novel nonvolatile optical-memory devices.[21] Recently, it was shown that NPC, following visible light excitation, can be used to improve greatly the sensitivity of InAs nanowire devices to infrared light.[19] The tuning of these surface states is vital in controlling the (opto)electronic performance of InAs nanowire devices. Some efforts have been made to treat the surface of InAs nanowires to either enhance or investigate the mechanisms of NPC. This has included the growth of a highly defective "photogating" shell to induce a greater trap density,[15] embedding in polymer to determine atmospheric effects,[18] and passivating the native oxide through wet chemical processing, followed by atomic layer deposition (ALD).[20]

Received: September 22, 2017
Accepted: November 24, 2017
Published: November 24, 2017

DOI: 10.1021/acsami.7b14415
ACS Appl. Mater. Interfaces 2017, 9, 43993−44000

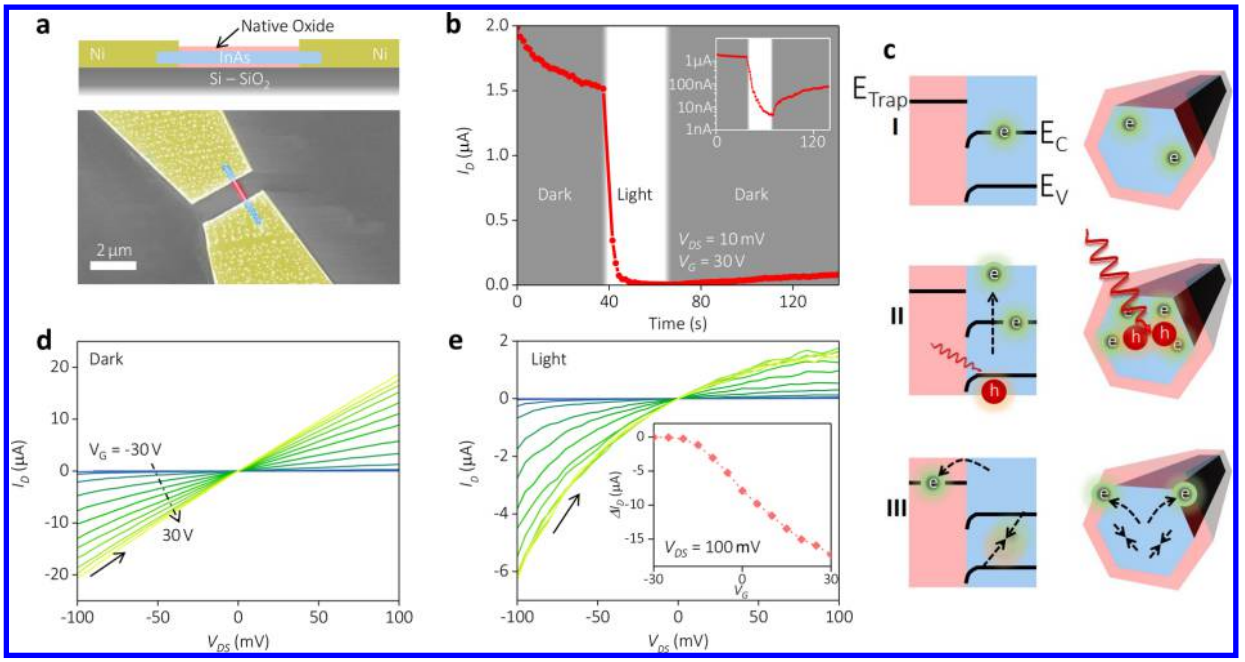


Figure 1. (a) A false color SEM image of a typical InAs nanowire (blue) device on Si/SiO_2 (gray), where the native oxide (red) is removed under the Ni electrodes (yellow). (b) Time dependent NPC observed during photoexcitation (white) in a 40 nm diameter InAs nanowire device plotting the drain current I_D on a linear or log scale (inset). (c) Proposed mechanism for NPC as described in the main text. Output characteristics under dark (d) and photoexcited (e) conditions for a series of gate voltages from −30 to 30 V in 5 V steps measured on the same nanowire device shown in (b). The solid arrow represents the voltage sweep direction. The time between setting V_G and starting to sweep V_{DS} was set at 50 ms, and $dV_{DS}/dt = 0.1$ V s^{-1}. The inset of (e) shows the total change in current after illumination, extracted from the difference between (d) and (e) ($\Delta I_D = I_{ph} - I_{dark}$) at V_{DS} = 100 mV.

It is clear therefore that an improved understanding of the material dependent properties of NPC in InAs nanowires is crucial for a range of potential applications. Signatures of NPC have been observed previously in InAs nanowires with a range of diameters[16,18] from 20 nm up to 475 nm, and we present here the first systematic study of the diameter dependence of NPC. By linking the observed photoresponse to electrical measurements of the photoinduced charge trap density, we gain insights vital for rational materials design toward novel photodetector and optical-memory devices. Furthermore, we have used ALD of Al_2O_3 to achieve effective surface passivation, without chemical etching, in individual-InAs nanowire devices. We have found that this results in devices with negligible gate hysteresis, due to a significant decrease in interfacial charge trap density; a greatly increased carrier mobility, due to decreased scattering; and a complete reversal in behavior from NPC to PPC under visible light illumination.

RESULTS AND DISCUSSION

Figure 1a shows the schematic and scanning electron microscopy (SEM) of a fabricated phototransistor. All the devices studied show n-type conduction where a positive gate voltage bias is required to "turn on" the conduction,[13] and were measured at room temperature under ambient conditions unless otherwise specified. A typical transfer curve (see the Supporting Information, Figure S1) shows large hysteresis between the forward and backward gate voltage sweeps, indicating a large number of trap states. To demonstrate the transient response of the nanowire to illumination, Figure 1b shows the variation of current at an applied back gate voltage of V_G = 30 V, and a source-drain bias V_{DS} = 10 mV. For an individual nanowire of d = 40 nm, a dark on-state current of I_{dark} = 2 μA is observed. An initial decrease in current indicates the population of interface trap states[11] reducing conductivity, even in dark conditions (as mentioned above). Under photoexcitation, a reduction in conductivity of almost 3 orders of magnitude is seen and the current reaches a minimum value of I_{ph} = 4 nA after 30 s. Previous studies[17,20] have reported that, as the intensity of illumination increases beyond 100 mW cm^{-2}, the gate voltage dependent NPC saturates and ultimately the photoresponse returns to conventional PPC, due to a finite density of charge traps. In our study, the illumination power density was limited to 30 mW cm^{-2}. The decrease in conductivity can be assigned to hot carrier trapping into above-gap states excited by the halogen lamp source which has a peak intensity at a wavelength of 906 nm (1.37 eV). Once the illumination is switched off, the current begins to steadily increase, as highlighted by the inset of Figure 1b. We note that, even after a further 75 s in dark conditions, the current still remains less than 5% of the original current. This indicates the long lifetime of charge carriers in the hot electron trap states, analogous to an optical-memory state. A proposed mechanism[17,20] for NPC is shown schematically in Figure 1c. (I) In dark conditions, highly mobile electrons, predominantly associated with the surface accumulation layer,[10] contribute to conduction along the channel. (II) Following photoexcitation, an electron hole pair is created. (III) If the photoexcited hot electron reaches the surface trap sites before thermalization occurs, it is trapped. The trapped electron will not contribute to conduction until thermal activation allows it to be released back into the conduction band. The trapped electrons electrostatically reduce the electron density in the channel, thereby contributing to NPC and shifting the threshold voltage as described below. The photoexcited holes recombine with equilibrium electrons, further depleting free electrons in the channel and giving rise to NPC.

DOI: 10.1021/acsami.7b14415
ACS Appl. Mater. Interfaces 2017, 9, 43993−44000

Figure 1d,e shows output characteristics to highlight the effect of gate voltage on NPC. In dark conditions for $V_G > 0$ V, a large on-state current is observed which varies linearly with V_{DS}, indicating good Ohmic contacts. After illumination, NPC causes a strong nonlinearity in the output characteristics. Despite the hot electron trapping, it is interesting to see that a good current modulation with V_G still remains. The gate dependent negative photocurrent $\Delta I_D = I_{ph} - I_{dark}$ is also found to increase in magnitude up to $\Delta I_D = -17.2$ μA at $V_{DS} = 100$ mV and $V_G = 30$ V (Figure 1e, inset). Due to the time constants of NPC, the output characteristics are shown to be strongly dependent on timing conditions, as shown in Figure S2.

At first glance, the slow recovery observed in Figure 1b appears to hinder any possibility of using the nanowires as a photodetector with repeatable operation. By applying a short gate pulse (~50 ms), we are able to electrostatically return the trapped charges into the nanowire to restore current flow.[17,19] Figure 2a shows the transient response of a nanowire device ($d = 30$ nm) where the gate voltage is kept at a constant value from $V_G = 10$ to 40 V, except where the gate is pulsed to $V_G = 0$ V to free trapped electrons. At $V_G = 10$ V, upon 15 s of illumination, the current drops to $I_{ph} \sim 100$ pA and shows no significant recovery within the noise level of the measurement after a further 15 s in the dark. Once the 0 V gate pulse is applied, the current increases but to only ~15% of the initial dark current. This may indicate that a change of −10 V for the gate voltage pulse is insufficient to completely release the trapped charges. As V_G is increased, the initial dark current increases in line with n-type field-effect behavior. All measurements at higher gate voltages also exhibit NPC. However, as V_G is increased, I_{ph} gradually increases, indicating that mobile carriers are still present in the nanowire after illumination. NPC can be overcome using high gate voltages due to the finite density of trap sites available at the nanowire surface which causes the NPC effect to saturate as the traps are completely filled, discussed in detail below. A similar trend is observed in the current recovered in the dark, I_{rec}. The proportion of current recovered after the 0 V gate pulse, i.e., over successive measurement cycles, also increases as V_G increases, suggesting that a change of −40 V for the gate voltage pulse is suitable for freeing the majority of trapped charges.

The proposed surface dominated NPC mechanism can be studied through a systematic study of nanowire diameter dependent characteristics. Several nanowire devices were fabricated for each diameter, all showed NPC, and typical devices were selected for further study. Figure 2b shows repeated dark − light − dark − reset measurement cycles at $V_G = 30$ V, as described above, for selected nanowire devices with diameters of 30, 40, 65, and 110 nm, respectively (see the Materials and Methods section and Figure S3 for more details). The 30 and 40 nm diameter nanowires show very similar NPC behavior with a low $I_{ph} < 1$ nA after 15 s of illumination (Figure 2c), each resulting in an "on−off" ratio of $I_{dark}/I_{ph} \sim 300$. Comparable values for I_{rec} are also observed for these two diameters and both exhibit very long recovery time constants, many times greater than the measurement time. When the nanowire diameter is increased to 65 nm, photoexcitation using the same power density can no longer completely turn off the current in the device, where an average $I_{ph} = 7$ nA ($I_{dark}/I_{ph} \sim 36$) is measured. An even greater difference in behavior is seen with the 110 nm diameter nanowire, where $I_{ph} > 100$ nA, and an average $I_{dark}/I_{ph} \sim 2.6$. This strongly indicates the role of the nanowire diameter in tuning the NPC switching ratio by 2 orders of magnitude. It is found that, as the diameter is increased, the recovery of current after photoexcitation becomes more efficient.

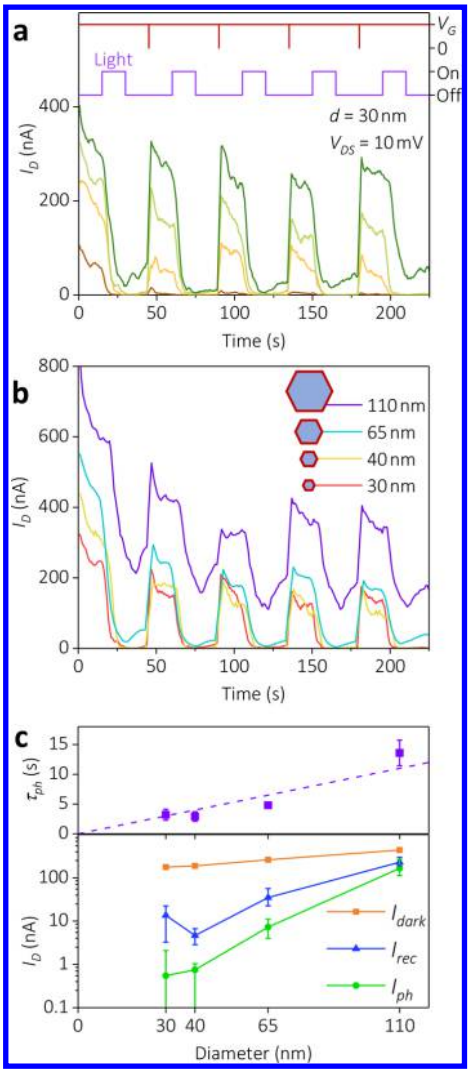


Figure 2. (a) Transient photoresponse during repeated cycling of a nanowire ($d = 30$ nm) following a dark − light − dark − reset test at $V_{DS} = 10$ mV for $V_G = 10$ V (dark orange), 20 V (yellow), 30 V (light green), and 40 V (dark green). The photoexcitation and gate voltage pulse sequence are also shown (top). (b) The same test performed for a series of devices with $d = 30$, 40, 65, and 110 nm at $V_G = 30$ V. (c) Extracted current values (bottom) and photoresponse time τ_{ph} (top) as a function of nanowire diameter for $V_G = 30$ V. The average value of 5 measurements is shown with minimum and maximum represented by the error bars. The dashed line represents a linear dependence of τ_{ph} on d.

To investigate the diameter dependence of the characteristic time constant of the photoresponse τ_{ph}, we fitted the data with a time dependent current decay during photoexcitation using $I(t - t_0) = I_{ph}(1 + A \exp(-t/\tau_{ph}))$, where $A > 0$. The results are summarized in Figure 2c. Narrow diameter nanowires with large values of I_{dark}/I_{ph} show relatively fast decay times of $\tau_{ph} \sim 3$ s for 30 and 40 nm diameter devices. Wider diameter nanowires show a slower response to photoexcitation where $\tau_{ph} = 5$ and 14 s for 65 and 110 nm diameter devices, respectively. In high mobility nanowires, the rate of trapping at the surface is known to be inversely proportional to the nanowire

DOI: 10.1021/acsami.7b14415
ACS Appl. Mater. Interfaces 2017, 9, 43993−44000

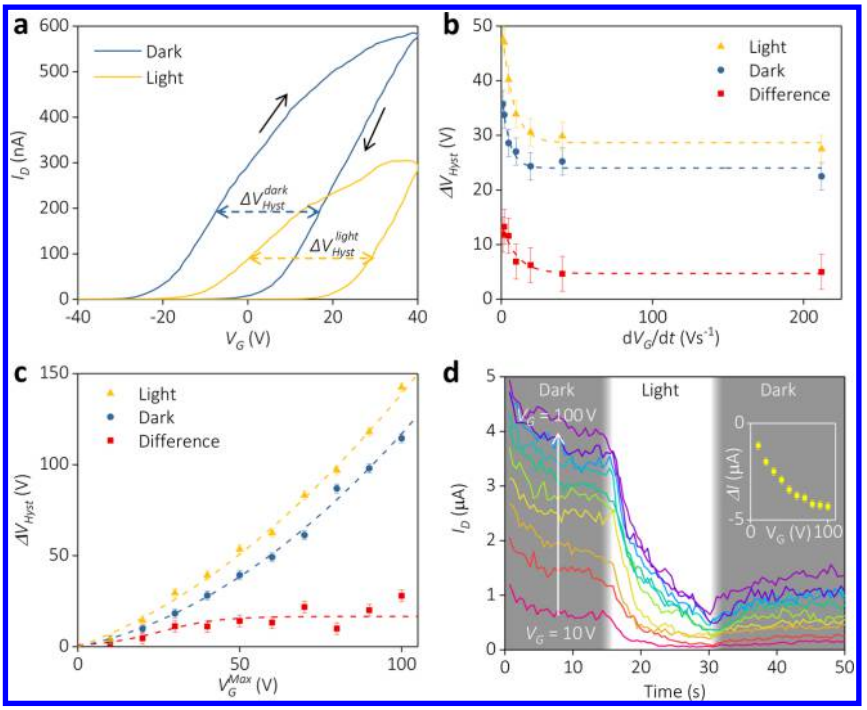


Figure 3. Correlated electronic and photoresponse properties of the same 65 nm diameter InAs nanowire device. (a) Transfer characteristics under dark and illuminated conditions at a constant sweep rate of 40 V s^{-1}. Arrows represent the gate voltage sweep direction. (b) Sweep rate dependence of hysteresis under dark and illuminated conditions where V_G was swept from V_G^{Min} to V_G^{Max} and back again ($V_G^{Max} = -V_G^{Min} = 40$ V). The difference represents the contribution of hot electron trapping. Dashed lines represent fits to monoexponential decays. (c) Sweep magnitude dependence of hysteresis where V_G was swept at a constant rate of 2 V s^{-1}. Dashed lines are guides to the eye. (d) Transient photoresponse from the same device at different gate voltages showing a saturation in NPC (inset) in line with the saturation of hot electron trapping shown in (c).

diameter.[22,23] Therefore, we expect $1/\tau_{ph} \propto 1/d$ if the negative photoresponse arises from traps at the surface. Indeed, we observe a similar dependency in our study. We can conclude that the magnitude of NPC is larger for narrower diameter nanowires ($d \leq 40$ nm) which also exhibit a faster NPC response with a larger on−off ratio and hence represent a better choice for optical-memory devices operating at room temperature.

Field-effect devices using low dimensional materials can suffer from substantial gate hysteresis, instability, reduced mobility, and degradation over time in the presence of charge trap states at the dielectric−semiconductor interface.[24−26] As we have shown, the effects of charge traps are not limited to electronic characteristics but, in particular for InAs nanowire devices, extend to optoelectronics. A greater understanding of the interplay between gate hysteresis and NPC could offer many new insights. Gate hysteresis is characterized by a change in transfer characteristics depending on the gate voltage sweep direction. Gate hysteresis is sensitive to the region of the nanowire in the vicinity of the dielectric interface, so hysteresis characterization is a useful tool to reveal the properties of electronic interface states. The magnitude of hysteresis (ΔV_{Hyst}) is highly dependent on the magnitude or range of the voltage sweep, between the maximum and minimum values ($V_G^{Max} - V_G^{Min}$), as well as the sweep rate dV_G/dt.

Figure 3a shows the transfer characteristics for a 65 nm diameter InAs nanowire device, both in the dark and illuminated for $V_G^{Max} = -V_G^{Min} = 40$ V, and $V_{DS} = 10$ mV. The gate voltage is swept from negative to positive values (up sweep) and back again (down sweep), at a constant sweep rate of 40 V s^{-1}. We observe n-type behavior and a substantial hysteresis between up and down sweeps. To define the hysteresis, we measure the width of the hysteresis loop between the up sweep and the down sweep, intersecting the point of the up sweep at which the device shows peak field-effect mobility. We define hysteresis as positive if the transfer curve shifts to more positive V_G on the down sweep, and negative if the transfer curve shifts to a more negative V_G on the down sweep. There are two clearly discernible contributions to the gate hysteresis, namely, trapping in the vicinity of the SiO_2 dielectric interface, and hot electron trapping that occurs under photoexcitation within the native oxide on the InAs NW surface. We observe a positive ΔV_{Hyst}, which indicates the predominantly electron-trapping nature of each type of interface trap site.[27] An intuitive explanation of this positive hysteresis is that traps charge upon the up sweep, and that once the traps are occupied by negatively charged electrons, a more positive V_G is required to achieve a given current I_D. Without photoexcitation, charge trapping can be attributed largely to the charging and discharging of silanol, SiOH, groups present in the SiO_2 dielectric.[26,28] It is worth noting that, by changing the dielectric material to one with donor-type charge traps,[11] a "negative" ΔV_{Hyst} has also been observed in InAs nanowire field-effect devices. We observe a number of noticeable changes between the dark and illuminated transfer characteristics. In line with the previous measurements, the maximum current is reduced under photoexcitation. The field-effect mobility, given by[29] $(dI_D/dV_G)L^2/C_{ox}V_{DS}$, where $L = 1$ μm is the channel length and C_{ox} is the back-gate capacitance,[30] is decreased from $\mu_{dark} = 230$ cm^2 V^{-1} s^{-1} to $\mu_{ph} = 140$ cm^2 V^{-1} s^{-1} due to charge scattering by an increased number of trapped charges. The threshold voltage on the up sweep shifts toward less negative values, indicating a decrease in the mobile carrier density under illumination. We also observe an increase in the hysteresis

DOI: 10.1021/acsami.7b14415
ACS Appl. Mater. Interfaces 2017, 9, 43993−44000

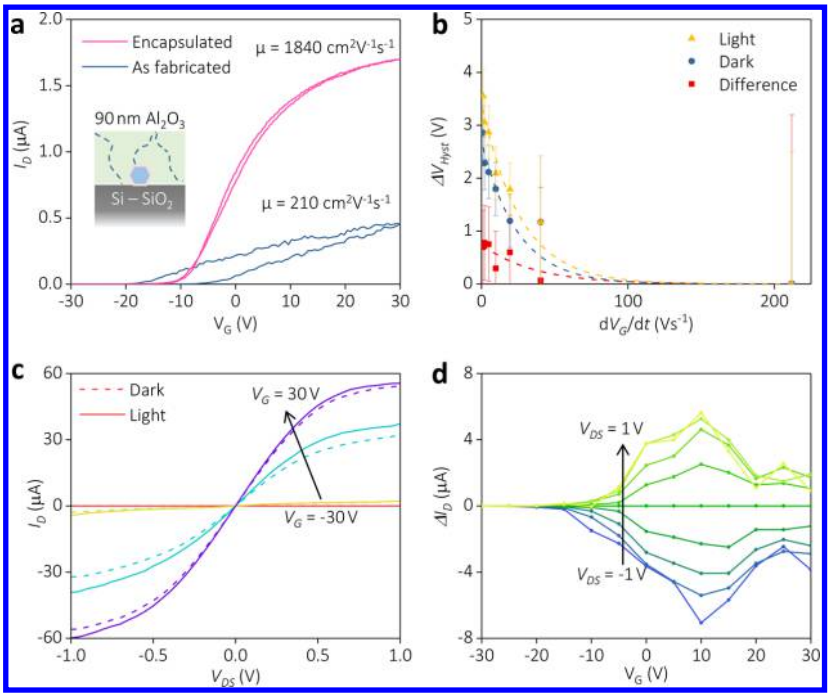


Figure 4. (a) Transfer characteristics of a 40 nm diameter InAs nanowire device before and after passivation with 90 nm of ALD Al_2O_3. The inset shows the schematic cross section where dashed lines represent possible pinhole defects within the amorphous Al_2O_3 layer. (b) Gate voltage sweep rate dependent hysteresis characterization for a device after ALD passivation. (c) Output characteristics of an ALD passivated 40 nm diameter InAs nanowire device as a function of V_G, with 20 V steps. (d) Positive photocurrent $\Delta I_D = I_D^{light} - I_D^{dark}$, extracted from the output characteristics (c) as a function of V_G for $V_{DS} = -1$ V to 1 V, with 250 mV steps.

which indicates that a greater number of charge traps are populated and is consistent with the hot electron trapping mechanism described above. The density of trapped hot electrons can be estimated using $C_{ox}\Delta V_{Hyst}/eA$, where e is the electronic charge and A is the surface area of the nanowire, assuming a uniform distribution of charge traps around the surface. We obtain a value of 1×10^{12} cm^{-2} at high sweep rates, rising to 3×10^{12} cm^{-2} at low sweep rates, which is comparable to previous estimates.[17] Similar behavior was observed for all nanowire diameters as shown in the Figure S4.

Figure 3b shows the gate voltage sweep rate dependence of the hysteresis for the same 65 nm diameter nanowire device for $V_G^{Max} = -V_G^{Min} = 40$ V. At very high sweep rates, between 20 and 210 V s^{-1}, the level of hysteresis is very weakly rate dependent under both dark and illuminated conditions. As the rate is decreased toward 1 V s^{-1} and the measurement time approaches the characteristic charging/discharging time constants of the interface states, ΔV_{Hyst} increases as an increasing proportion of the traps are filled. By taking the difference between the dark and illuminated measurements, we can obtain the contribution to ΔV_{Hyst} due to hot electron trapping. Hot electron trapping consistently raises ΔV_{Hyst} and becomes steadily more important as the sweep rate is reduced. Using a relatively low sweep rate of 2 V s^{-1}, where a significant contribution of hot electron trapping is expected, we study the V_G dependence of ΔV_{Hyst} as we increase V_G^{Max} from 10 to 100 V. Figure 3c shows that the total hysteresis increases quadratically under dark conditions. As higher gate voltages are applied, more trap sites within the SiO_2 are charged. A very different behavior is observed for the hot electron traps which, after rapidly increasing at lower gate voltages, then plateaus for $V_G \geq 40$ V. The photoresponse of the same nanowire is measured at constant V_G, in the same range as V_G^{Max} for the hysteresis measurements, as shown in Figure 3d. At low V_G, the current is almost completely switched off under illumination, and as V_G increases, I_{ph} also increases and ΔI_D plateaus. At the same time, the optical-memory effect decreases as a larger current is recovered after the dark conditions are returned. These results are consistent with the complete filling of hot electron traps at high V_G. This in turn results in a plateau of both the NPC and optical-memory effects for $V_G \geq 40$ V, thus providing a useful guide for the operating point of NPC based photodetectors and optical-memory devices.

While this is of great interest for the development of novel negative-photoconductivity based photodetectors, for many other electronic and optoelectronic devices, where the high mobility and conductivity of InAs are exploited, this photosensitivity to visible light would constitute a major barrier in the route toward these applications. As this effect is mediated by surface states, we explore surface passivation to mitigate this effect. One approach to nanowire surface passivation is to overcoat with a larger band gap shell to obtain "core−shell" structures, although strain due to lattice mismatch must be taken into careful consideration.[31−34] Alternatively, etching the native oxide from an InAs nanowire, followed by ALD of HfO_2, can recover positive photoconductivity.[20] Indeed, our measurements demonstrated that NPC and hot carrier trapping are eliminated by the removal of the native oxide by wet chemical etching (Figure S5). However, we found that wet etching was detrimental to the ultimate device performance, consistent with previous reports.[35] Our improved approach avoids strain effects and etching damage, and instead exploits the reactivity of III−V oxides to metalorganic precursors. In particular, during the deposition of Al_2O_3 by ALD, trimethylaluminum (TMA) precursors can drive chemical (redox) reduction of the native oxide at III−V surfaces.[36−44] Due to the industrial importance

DOI: 10.1021/acsami.7b14415
ACS Appl. Mater. Interfaces 2017, 9, 43993−44000

of ALD growth of Al_2O_3, the reaction pathways of TMA with a variety of materials have been extensively studied both theoretically[42,45] and experimentally. The reaction of TMA with the native oxide of InAs is a complex process due to the presence of As-, In-, and mixed-oxides, each present in different oxidation states. For InAs, the deposition of just 2 nm of Al_2O_3 using TMA and H_2O has been shown, using X-ray photoelectron spectroscopy (XPS), to reduce over 90% of the native As-oxides, and up to 90% of the native In-oxides.[39] The specific reactions are numerous,[42] but generally within the first few ALD cycles, the native oxide acts as an additional source of oxygen to react with the TMA. For specific reaction pathways, As−O and In−O can be replaced with Al−O bonds and result in volatile As- and In-containing species which are removed during purging between pulses. Furthermore, there are additional defect states such as As−As dimers present at the interface, and known to create above gap states in InAs,[46] which are passivated by the TMA reaction.[47] We find here that ALD of Al_2O_3, without an additional etching process, is sufficient to remove NPC effects in InAs nanowires and return devices to an "intrinsic" positive photoconductivity.

Despite the previous observation that even a single pulse of TMA is suitable to reduce the native oxide,[38] we apply a thicker (90 nm) layer which has the added benefit of acting as a gas diffusion barrier to prevent reoxidation and other unwanted atmospheric effects.[48] Figure 4a shows the transfer characteristics of the same 40 nm diameter nanowire device tested before and after ALD passivation under dark conditions. A number of dramatic changes are observed. The on-state current at V_{DS} = 10 mV increases from 450 nA before passivation to 1.7 μA afterward. The field-effect mobility increases by almost an order of magnitude from 210 to 1840 $cm^2\ V^{-1}\ s^{-1}$. We see an almost 10 times drop in dark hysteresis and a 20 times decrease in hysteresis due to hot electron trapping relative to unpassivated nanowires (Figure 4b).

The ALD process has two separate effects on the chemistry of the interface. First, it chemically reduces the native oxide, as described above. This has a direct effect on the trapping of photoexcited hot carriers. Second, charge traps within the SiO_2 gate dielectric are passivated during ALD. This has little or no effect on hot carrier trapping or NPC but significantly lowers the total (nonphotoexcited) charge trap density, giving low hysteresis and enhanced mobility due to a decrease in charge carrier scattering. Specifically, during ALD, hydrogen from SiOH at the surface of SiO_2 is transferred to a methyl group from the TMA and extracted as CH_4, thus passivating the surface.[45,49] As the SiOH groups account for the majority of charge traps in the gate dielectric,[28] this is the dominant reaction responsible for reducing hysteresis. It is important to make clear that this overall reduction in hysteresis after ALD passivation is due to chemical reactions occurring at the gate dielectric and nanowire surfaces during the ALD process. It is not simply due to the removal of atmospheric adsorbates, the effects of which have been studied in detail previously.[50,51] To verify the role of atmospheric adsorbates, we studied unpassivated nanowires in vacuum (10^{-4} mbar) and N_2. Under vacuum and N_2, the majority of the gate hysteresis remained in unpassivated nanowires, as detailed in Figure S6, indicating that adsorbed gases are not the primary origin of the gate hysteresis.

Due to the complexity of the ALD reaction processes, described above, the exact chemical origin of the ALD passivation of hot carrier traps is less clear. Nevertheless, an empirical model has arisen from previous experimental studies. It consists of a trap state which lies between approximately 0.5[17] and 0.8 eV[20] above the bottom of conduction band. One plausible origin of the hot electron traps is the As−As dimer which is predicted to generate states ~0.7 eV above the bottom of the conduction band in InAs.[46] During ALD, the TMA reaction at the nanowire surface would passivate As−As dimers,[47] reducing the density of above gap states. Because the traps lie significantly above the conduction band minimum for both zinc-blende and wurtzite InAs, we expect NPC and hysteresis to affect both zinc-blende and wurtzite nanowires, and that these effects can be mitigated by ALD passivation in both cases.

By measuring the output characteristics as a function of gate voltage, we can see that, under photoexcitation, a positive photoconductivity can be observed throughout the gate voltage range (Figure 4c,d). The transient response time for PPC is comparable to previous reports of PPC in etched InAs nanowires,[20] where $\tau_{ph,PPC} \sim 10$ s, as shown in Figure S7.

CONCLUSIONS

We have demonstrated photodetectors based on negative photoconductivity in individual MOCVD grown, wurtzite InAs nanowires. At room temperature under ambient conditions, hot electron trapping can cause a substantial depletion of mobile carriers, effectively switching off the devices. Such devices show a pronounced and long-lived "optical-memory" effect. For larger diameter nanowires, the magnitude of NPC diminishes because of reduced surface area to volume ratio. Hence, the contribution of surface states to the photoresponse is less important while bulklike conduction through the core of the nanowire becomes more significant. At high gate voltages, we observe a saturation of NPC attributed to a complete filling of available hot electron traps, which is confirmed through hysteresis characterization. By passivating the devices with atomic layer deposited Al_2O_3, we achieve an order of magnitude reduction in charge trap density, accompanied by almost an order of magnitude increase in field-effect mobility. Without additional surface etching steps, we find that ALD is sufficient to achieve a positive photoconductivity in InAs nanowires. Thus, our approach, based on fine control over nanowire diameter, and subsequent surface-state engineering treatments offer scalable techniques to develop a broad range of nanowire devices with an application specific tailored photoresponse.

MATERIALS AND METHODS

InAs nanowires were grown by metal−organic chemical vapor deposition (MOCVD). The growth conditions were chosen to grow wurtzite crystal structures with minimal stacking faults, minimal tapering, and hexagonal cross sections with $\{1\bar{1}00\}$ side facets,[52] as confirmed by transmission electron microscopy (TEM) shown in Figure S8. The nanowire diameter was tightly controlled by selecting the diameter of the Au catalyst. Nanowire diameters, inclusive of surface oxide, of 30 ± 5 nm, 40 ± 5 nm, 65 ± 5 nm, and 110 ± 5 nm, respectively, were obtained, as confirmed by SEM (Figure S3). For TEM measurements, nanowires were mechanically transferred to a holey carbon grid. TEM was performed using a JEOL 2100F instrument operated at 200 keV. The nanowires were transferred to a doped Si wafer with 300 nm of thermally grown SiO_2 which served as a global back gate. Contacts with a separation of 1 μm (Figure 1a) were patterned using e-beam lithography and sputter deposition of 70 nm Ni, followed by lift-off. To obtain low contact resistivity, prior to Ni deposition, the contact region of the nanowire was etched in 2% aqueous $(NH_4)_2S$ solution at 40 °C for 10 min. Electrical

DOI: 10.1021/acsami.7b14415
ACS Appl. Mater. Interfaces 2017, 9, 43993−44000

measurements were carried out using a probe station connected to a Keithley 4200-SCS semiconductor characterization system. Illumination of the samples to measure the photoresponse was applied using a 3200 K halogen lamp with a power density of 30 mW cm^{-2}. All measurements were carried out at room temperature under ambient conditions unless otherwise specified. For ALD passivation, after device fabrication, a 90 nm capping layer of Al_2O_3 was deposited using a Cambridge NanoTech ALD system at 120 °C using trimethylaluminum and H_2O precursors. The probe pads were then exposed by etching through the Al_2O_3 with phosphoric acid.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b14415.

SEM images of as-grown InAs nanowires. HRTEM images of nanowire crystal structure and oxide thickness. Transfer characteristics from the device in Figure 1b. Sweep delay dependent output characteristics. Sweep rate dependent hysteresis for different nanowire diameters. Device characteristics of bare nanowires after wet etching the native oxide. Transfer characteristics and sweep rate dependent hysteresis for ambient atmosphere, N_2 and 10^{-4} bar vacuum. Transient positive photoresponse (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

*E-mail: jaa59@cam.ac.uk (J.A.A.-W.).
*E-mail: hjj28@cam.ac.uk (H.J.J.).

ORCID

Jack A. Alexander-Webber: 0000-0002-9374-7423
Riccardo Di Pietro: 0000-0002-5526-0120
Stephan Hofmann: 0000-0001-6375-1459
Hannah J. Joyce: 0000-0002-9737-680X

Present Address

[‖]Materials Science and Engineering Department, University of California, Berkeley, CA 94720, United States.

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

Data sets related to this publication are available from the Cambridge University data repository at https://doi.org/10.17863/CAM.16773.

■ ACKNOWLEDGMENTS

We acknowledge funding from the EPSRC (Grant No. EP/M009505/1) and the ERC (Grant No. 716471, ACrossWire). S.H. acknowledges funding from the EPSRC (Grant No. EP/P005152/1). This work was also supported by the Australian Research Council, Australian National Fabrication Facility and Australian Microscopy & Microanalysis Research Facility. J.A.A.-W. acknowledges the support of his Research Fellowships from the Royal Commission for the Exhibition of 1851 and Churchill College, Cambridge. C.K.G acknowledges the support of her scholarship from The Winston Churchill Foundation of the United States. We would like to thank Prof John Robertson for useful discussions regarding III−V interfaces.

■ REFERENCES

(1) Dayeh, S. A. Electron Transport in Indium Arsenide Nanowires. *Semicond. Sci. Technol.* **2010**, *25* (2), 024004.
(2) Joyce, H. J.; Gao, Q.; Hoe Tan, H.; Jagadish, C.; Kim, Y.; Zou, J.; Smith, L. M.; Jackson, H. E.; Yarrison-Rice, J. M.; Parkinson, P.; Johnston, M. B. III−V Semiconductor Nanowires for Optoelectronic Device Applications. *Prog. Quantum Electron.* **2011**, *35* (2−3), 23−75.
(3) Joyce, H. J.; Gao, Q.; Wong-Leung, J.; Kim, Y.; Tan, H. H.; Jagadish, C. Tailoring GaAs, InAs, and InGaAs Nanowires for Optoelectronic Device Applications. *IEEE J. Sel. Top. Quantum Electron.* **2011**, *17* (4), 766−778.
(4) Logeeswaran, V. J.; Oh, J.; Nayak, A. P.; Katzenmeyer, A. M.; Gilchrist, K. H.; Grego, S.; Kobayashi, N. P.; Wang, S.-Y.; Talin, A. A.; Dhar, N. K.; Islam, M. S. A Perspective on Nanowire Photodetectors: Current Status, Future Challenges, and Opportunities. *IEEE J. Sel. Top. Quantum Electron.* **2011**, *17* (4), 1002−1032.
(5) Dayeh, S. A.; Aplin, D. P. R.; Zhou, X.; Yu, P. K. L.; Yu, E. T.; Wang, D. High Electron Mobility InAs Nanowire Field-Effect Transistors. *Small* **2007**, *3* (2), 326−332.
(6) Miao, J.; Hu, W.; Guo, N.; Lu, Z.; Zou, X.; Liao, L.; Shi, S.; Chen, P.; Fan, Z.; Ho, J. C.; Li, T. X.; Chen, X. S.; Lu, W. Single InAs Nanowire Room-Temperature near-Infrared Photodetectors. *ACS Nano* **2014**, *8* (4), 3628−3635.
(7) LaPierre, R. R.; Robson, M.; Azizur-Rahman, K. M.; Kuyanov, P. A Review of III−V Nanowire Infrared Photodetectors and Sensors. *J. Phys. D: Appl. Phys.* **2017**, *50* (12), 123001.
(8) Rota, M. B.; Ameruddin, A. S.; Fonseka, H. A.; Gao, Q.; Mura, F.; Polimeni, A.; Miriametro, A.; Tan, H. H.; Jagadish, C.; Capizzi, M. Bandgap Energy of Wurtzite InAs Nanowires. *Nano Lett.* **2016**, *16* (8), 5197−5203.
(9) Das, A.; Ronen, Y.; Most, Y.; Oreg, Y.; Heiblum, M.; Shtrikman, H. Zero-Bias Peaks and Splitting in an Al-InAs Nanowire Topological Superconductor as a Signature of Majorana Fermions. *Nat. Phys.* **2012**, *8* (12), 887−895.
(10) Olsson, L.; Andersson, C.; Håkansson, M.; Kanski, J.; Ilver, L.; Karlsson, U. Charge Accumulation at InAs Surfaces. *Phys. Rev. Lett.* **1996**, *76* (19), 3626−3629.
(11) Dayeh, S. A.; Soci, C.; Yu, P. K. L.; Yu, E. T.; Wang, D. Transport Properties of InAs Nanowire Field Effect Transistors: The Effects of Surface States. *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.* **2007**, *25* (4), 1432.
(12) Sun, M. H.; Joyce, H. J.; Gao, Q.; Tan, H. H.; Jagadish, C.; Ning, C. Z. Removal of Surface States and Recovery of Band-Edge Emission in InAs Nanowires through Surface Passivation. *Nano Lett.* **2012**, *12* (7), 3378−3384.
(13) Heedt, S.; Otto, I.; Sladek, K.; Hardtdegen, H.; Schubert, J.; Demarina, N.; Lüth, H.; Grützmacher, D.; SchäPers, T. Resolving Ambiguities in Nanowire Field-Effect Transistor Characterization. *Nanoscale* **2015**, *7* (43), 18188−18197.
(14) Suyatin, D. B.; Thelander, C.; Björk, M. T.; Maximov, I.; Samuelson, L. Sulfur Passivation for Ohmic Contact Formation to InAs Nanowires. *Nanotechnology* **2007**, *18* (10), 105307.
(15) Guo, N.; Hu, W.; Liao, L.; Yip, S.; Ho, J. C.; Miao, J.; Zhang, Z.; Zou, J.; Jiang, T.; Wu, S.; Chen, X.; Lu, W. Anomalous and Highly Efficient InAs Nanowire Phototransistors Based on Majority Carrier Transport at Room Temperature. *Adv. Mater.* **2014**, *26* (48), 8203−8209.
(16) Li, J.; Yan, X.; Sun, F.; Zhang, X.; Ren, X. Anomalous Photoconductive Behavior of a Single InAs Nanowire Photodetector. *Appl. Phys. Lett.* **2015**, *107* (26), 263103.
(17) Yang, Y.; Peng, X.; Kim, H. S.; Kim, T.; Jeon, S.; Kang, H. K.; Choi, W.; Song, J.; Doh, Y. J.; Yu, D. Hot Carrier Trapping Induced Negative Photoconductance in InAs Nanowires toward Novel Nonvolatile Memory. *Nano Lett.* **2015**, *15* (9), 5875−5882.
(18) Han, Y.; Zheng, X.; Fu, M.; Pan, D.; Li, X.; Guo, Y.; Zhao, J.; Chen, Q. Negative Photoconductivity of InAs Nanowires. *Phys. Chem. Chem. Phys.* **2016**, *18* (2), 818−826.
(19) Fang, H.; Hu, W.; Wang, P.; Guo, N.; Luo, W.; Zheng, D.; Gong, F.; Luo, M.; Tian, H.; Zhang, X.; Luo, C.; Wu, X.; Chen, P.;

DOI: 10.1021/acsami.7b14415
ACS Appl. Mater. Interfaces 2017, 9, 43993−44000

Liao, L.; Pan, A.; Chen, X.; Lu, W. Visible Light-Assisted High-Performance Mid-Infrared Photodetectors Based on Single InAs Nanowire. *Nano Lett.* **2016**, *16* (10), 6416−6424.
(20) Han, Y.; Fu, M.; Tang, Z.; Zheng, X.; Ji, X.; Wang, X.; Lin, W.; Yang, T.; Chen, Q. Switching from Negative to Positive Photoconductivity toward Intrinsic Photoelectric Response in InAs Nanowire. *ACS Appl. Mater. Interfaces* **2017**, *9* (3), 2867−2874.
(21) Roy, K.; Padmanabhan, M.; Goswami, S.; Sai, T. P.; Ramalingam, G.; Raghavan, S.; Ghosh, A. Graphene-MoS2 Hybrid Structures for Multifunctional Photoresponsive Memory Devices. *Nat. Nanotechnol.* **2013**, *8* (11), 826−830.
(22) Léonard, F.; Talin, A. A.; Swartzentruber, B. S.; Picraux, S. T. Diameter-Dependent Electronic Transport Properties of Au-Catalyst/Ge-Nanowire Schottky Diodes. *Phys. Rev. Lett.* **2009**, *102* (10), 106805.
(23) Joyce, H. J.; Wong-Leung, J.; Yong, C. K.; Docherty, C. J.; Paiman, S.; Gao, Q.; Tan, H. H.; Jagadish, C.; Lloyd-Hughes, J.; Herz, L. M.; Johnston, M. B. Ultralow Surface Recombination Velocity in InP Nanowires Probed by Terahertz Spectroscopy. *Nano Lett.* **2012**, *12* (10), 5325−5330.
(24) Dayeh, S. A.; Soci, C.; Yu, P. K. L.; Yu, E. T.; Wang, D. Influence of Surface States on the Extraction of Transport Parameters from InAs Nanowire Field Effect Transistors. *Appl. Phys. Lett.* **2007**, *90* (16), 162112.
(25) Alexander-Webber, J. A.; Sagade, A. A.; Aria, A. I.; Van Veldhoven, Z. A.; Braeuninger-Weimer, P.; Wang, R.; Cabrero-Vilatela, A.; Martin, M.-B.; Sui, J.; Connolly, M. R.; Hofmann, S. Encapsulation of Graphene Transistors and Vertical Device Integration by Interface Engineering with Atomic Layer Deposited Oxide. *2D Mater.* **2017**, *4* (1), 011008.
(26) Lee, J. S.; Ryu, S.; Yoo, K.; Choi, I. S.; Yun, W. S.; Kim, J. Origin of Gate Hysteresis in Carbon Nanotube Field-Effect Transistors. *J. Phys. Chem. C* **2007**, *111* (34), 12504−12507.
(27) Kaushik, N.; Mackenzie, D. M. A.; Thakar, K.; Goyal, N.; Mukherjee, B.; Boggild, P.; Petersen, D. H.; Lodha, S. Reversible Hysteresis Inversion in MoS2 Field Effect Transistors. *npj 2D Mater. Appl.* **2017**, *1* (1), 34.
(28) Hartstein, A.; Young, D. R. Identification of Electron Traps in Thermal Silicon Dioxide Films. *Appl. Phys. Lett.* **1981**, *38* (8), 631−633.
(29) Ford, A. C.; Ho, J. C.; Chueh, Y. L.; Tseng, Y. C.; Fan, Z. Y.; Guo, J.; Bokor, J.; Javey, A. Diameter-Dependent Electron Mobility of InAs Nanowires. *Nano Lett.* **2009**, *9* (1), 360−365.
(30) Wunnicke, O. Gate Capacitance of Back-Gated Nanowire Field-Effect Transistors. *Appl. Phys. Lett.* **2006**, *89*, 083102.
(31) Parkinson, P.; Joyce, H. J.; Gao, Q.; Tan, H. H.; Zhang, X.; Zou, J.; Jagadish, C.; Herz, L. M.; Johnston, M. B. Carrier Lifetime and Mobility Enhancement in Nearly Defect-Free Core- Shell Nanowires Measured Using Time-Resolved Terahertz Spectroscopy. *Nano Lett.* **2009**, *9* (9), 3349−3353.
(32) van Tilburg, J. W. W.; Algra, R. E.; Immink, W. G. G.; Verheijen, M.; Bakkers, E. P. a M.; Kouwenhoven, L. P. Surface Passivated InAs/InP Core/shell Nanowires. *Semicond. Sci. Technol.* **2010**, *25* (2), 024011.
(33) Joyce, H. J.; Parkinson, P.; Jiang, N.; Docherty, C. J.; Gao, Q.; Tan, H. H.; Jagadish, C.; Herz, L. M.; Johnston, M. B. Electron Mobilities Approaching Bulk Limits In "surface-free" GaAs Nanowires. *Nano Lett.* **2014**, *14* (10), 5989−5994.
(34) Kavanagh, K. L.; Saveliev, I.; Blumin, M.; Swadener, G.; Ruda, H. E. Faster Radial Strain Relaxation in InAs-GaAs Core-Shell Heterowires. *J. Appl. Phys.* **2012**, *111* (4), 044301.
(35) Petrovykh, D. Y.; Yang, M. J.; Whitman, L. J. Chemical and Electronic Properties of Sulfur-Passivated InAs Surfaces. *Surf. Sci.* **2003**, *523* (3), 231−240.
(36) Huang, M. L.; Chang, Y. C.; Chang, C. H.; Lee, Y. J.; Chang, P.; Kwo, J.; Wu, T. B.; Hong, M. Surface Passivation of III-V Compound Semiconductors Using Atomic-Layer-Deposition-Grown Al2O3. *Appl. Phys. Lett.* **2005**, *87* (25), 252104.
(37) Hinkle, C. L.; Sonnet, A. M.; Vogel, E. M.; McDonnell, S.; Hughes, G. J.; Milojevic, M.; Lee, B.; Aguirre-Tostado, F. S.; Choi, K. J.; Kim, H. C.; Kim, J.; Wallace, R. M. GaAs Interfacial Self-Cleaning by Atomic Layer Deposition. *Appl. Phys. Lett.* **2008**, *92* (7), 071901.
(38) Lee, H. D.; Feng, T.; Yu, L.; Mastrogiovanni, D.; Wan, A.; Gustafsson, T.; Garfunkel, E. Reduction of Native Oxides on GaAs during Atomic Layer Growth of Al2O3. *Appl. Phys. Lett.* **2009**, *94* (22), 222108.
(39) Timm, R.; Fian, A.; Hjort, M.; Thelander, C.; Lind, E.; Andersen, J. N.; Wernersson, L. E.; Mikkelsen, A. Reduction of Native Oxides on InAs by Atomic Layer Deposited Al2O3 and HfO2. *Appl. Phys. Lett.* **2010**, *97*, 132904.
(40) Timm, R.; Hjort, M.; Fian, A.; Borg, B. M.; Thelander, C.; Andersen, J. N.; Wernersson, L. E.; Mikkelsen, A. Interface Composition of InAs Nanowires with Al2O3 and HfO2 Thin Films. *Appl. Phys. Lett.* **2011**, *99* (22), 222907.
(41) Hinkle, C. L.; Vogel, E. M.; Ye, P. D.; Wallace, R. M. Interfacial Chemistry of Oxides on InxGa(1-x)As and Implications for MOSFET Applications. *Curr. Opin. Solid State Mater. Sci.* **2011**, *15* (5), 188−207.
(42) Klejna, S.; Elliott, S. D. First Principles Modelling of the "Clean-Up"of Native Oxides during Atomic Layer Deposition onto III-V Substrates. *J. Phys. Chem. C* **2012**, *116* (1), 643−654.
(43) Dey, A. W.; Thelander, C.; Lind, E.; Dick, K. A.; Borg, B. M.; Borgstrom, M.; Nilsson, P.; Wernersson, L. E. High-Performance InAs Nanowire MOSFETs. *IEEE Electron Device Lett.* **2012**, *33* (6), 791−793.
(44) Robertson, J.; Guo, Y.; Lin, L. Defect State Passivation at III-V Oxide Interfaces for Complementary Metal-Oxide-Semiconductor Devices. *J. Appl. Phys.* **2015**, *117* (11), 112806.
(45) Elliott, S. D.; Greer, J. C. Simulating the Atomic Layer Deposition of Alumina from First Principles. *J. Mater. Chem.* **2004**, *14* (21), 3246−3250.
(46) Lin, L.; Robertson, J. Defect States at III-V Semiconductor Oxide Interfaces. *Appl. Phys. Lett.* **2011**, *98* (8), 082903.
(47) Pi, T. W.; Lin, H. Y.; Chiang, T. H.; Liu, Y. T.; Chang, Y. C.; Lin, T. D.; Wertheim, G. K.; Kwo, J.; Hong, M. Surface Atoms Core-Level Shifts in Single Crystal GaAs Surfaces: Interactions with Trimethylaluminum and Water Prepared by Atomic Layer Deposition. *Appl. Surf. Sci.* **2013**, *284*, 601−610.
(48) Carcia, P. F.; McLean, R. S.; Reilly, M. H.; Groner, M. D.; George, S. M. Ca Test of Al2O3 Gas Diffusion Barriers Grown by Atomic Layer Deposition on Polymers. *Appl. Phys. Lett.* **2006**, *89*, 031915.
(49) Puurunen, R. L. Surface Chemistry of Atomic Layer Deposition: A Case Study for the Trimethylaluminum/water Process. *J. Appl. Phys.* **2005**, *97* (12), 121301.
(50) Du, J.; Liang, D.; Tang, H.; Gao, X. P. A. InAs Nanowire Transistors as Gas Sensor and the Response Mechanism. *Nano Lett.* **2009**, *9* (12), 4348−4351.
(51) Ullah, A. R.; Joyce, H. J.; Tan, H. H.; Jagadish, C.; Micolich, A. P. The Influence of Atmosphere on the Performance of Pure-Phase WZ and ZB InAs Nanowire Transistors. *Nanotechnology* **2017**, *28* (45), 454001.
(52) Joyce, H. J.; Wong-Leung, J.; Gao, Q.; Tan, H. H.; Jagadish, C. Phase Perfection in Zinc Blende and Wurtzite III- V Nanowires Using Basic Growth Parameters. *Nano Lett.* **2010**, *10* (3), 908−915.

DOI: 10.1021/acsami.7b14415
ACS Appl. Mater. Interfaces 2017, 9, 43993−44000