Robust Stability Analysis of Active Voltage Control for High-power IGBT Switching by Kharitonov's Theorem

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***Abstract*— The main idea of active voltage control (AVC) is to em- ploy classic feedback-control methods forcing the IGBT collector voltage transient to follow a predefined trajectory. This feedback control of IGBTs has great advantages in guaranteeing that IGBTs remain in safe operating area (SOA), restricting EMI, mitigat- ing the voltage/current stress, minimizing/predicting their power losses, and balancing voltages of IGBTs in series. Inevitably, how- ever, AVC introduces stability issues. Based on the assumption that accurate IGBT small-signal model parameters are available, an analogue proportional-derivative and multiloop feedback control was proposed to achieve stable performance in previous work. Due to nonlinearities and uncertainties in IGBT parameters, previous stability analysis methods have important limitations. This work uses Kharitonov's theorem during the IGBT controlled turn-off to assess the system's stability and guide the AVC design to account for model uncertainties and varying parameters. We conducted ex- periments to investigate the system's robust stability due to these uncertainties in the IGBT parameters, which confirm the validity of the proposed theoretical analysis. With the use of wide bandwidth op-amps, it is shown that the feedback design may be simplified.**

***Index Terms*—Active voltage control (AVC), IGBT gate drive, IGBT parameters uncertainties, Kharitonov's theorem, nonlinear- ity, stability analysis;**

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I. INTRODUCTION

The Active Voltage Control (AVC) method has been proven to be an effective solution for controlling a single IGBT switching [1-3] and series-connected IGBTs switching [4-6]. Feedback control of IGBTs in the active region can be employed to regulate the switching trajectory according to a pre-defined reference. Hence, AVC can guarantee that IGBTs remain in the Sate Operation Area (SOA), minimise/predict their switching losses, mitigate the voltage/current stress, synchronise votlage transients of IGBTs in series and restrict EMI for a wide range of operating conditions.

However, feedback control can inevitably introduce stability issues. An essential question is whether AVC multi-loop feedback control system is prone to instability; as a result itrequires a systematic design process due to its sensitivity to system parameters [5]. Previous work considered internal physics of IGBT-and-diode commutation [2] to optimise the reference design. For stability analysis, several methods used classic control theory. For example, the work in [5] plotted system root loci by sweeping one parameter over an estimated wide range, and while keeping other parameters fixed. This approach, however, is very conservative and, in most cases, is not realistically assumed the full knowledge of the exact values of all other parameters.

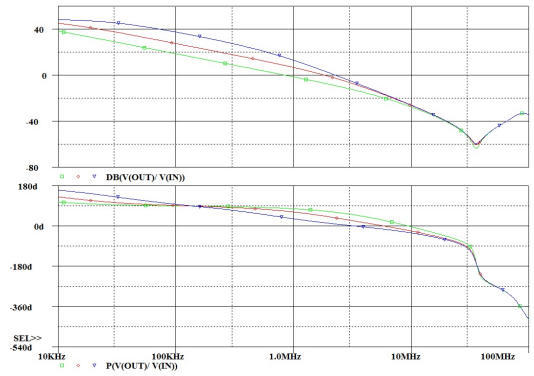

Fig. 1. Bode plots for the system open-loop transfer function at turn-off ramp (Red: C_{GC} and C_{CE} from [4]; Green: C_{GC} and C_{CE} increased by 10%; Purple: C_{GC} and C_{CE} reduced by 10%;).

An better approach is to choose different operating points of interest, derive linearised IGBT models around them and analyse stability correspondingly [4]. Recently, this approach has been further applied to an intelligent close-loop gate drive in [8-9] by carefully considering the important parasitic inductances of different IGBT products. This approach generates a switching profile of major operating points and provides an improved representation of the switching process. On the other hand, it has important limitations. First, the approach requires very accurate system parameters for systen transfer fucntions.

However, the IGBT physical and geometrical parameters are difficult to be extracted accurately. Even with a advanced and time-costly IGBT model parameter optmisation process, deviations might still exist due to assumptions made in the model [7]. IGBT parasitics capaictances that are well known to have great effects on IGBT switching are even harder to model properly without knowing critical geometrical parameters [2,14,21]. A satisfactory accuracy of their values is, therefore, even harder to guarantee. Second, a single analysis result can only be useful for a specific operating condition while IGBT parameters are well known to be dependent on different operating conditions (voltage, current, temperature et. al.). For example, for the previous design and operating point in [4], if C_{GC} and C_{CE} varies by 10%, the open-loop transfer fucntion bode plots will be quite different as shown in Fig. 1. The phase margin for reduecd C_{GC} and C_{CE} will be very close to zero. It can also seen that, Fig. 1, the system bode plot is very sensitive to the uncertainties in the IGBT parameters. If Bode plots are used for robust stability analysis of linearlised transfer functions by considering a proper range of IGBT parameters, it leads to an infinite number of tests (for example, Routh Hurwitz test [17]) by considering all possible combinations of IGBT parameters in the considered range. A sample of the parameter space leads to a finite number of such tests but it cannot guarantee stability.Several other intelligent close-loop schemes proposed to control IGBT switching with similar classic analogue controllers [10-13]. However, they are all based on empirical design processes with numerous tests. The work in [10-11] proposes a mathematical method to describe the IGBT switching behaviours and to assess the system stability. It simplifies IGBT parameters with a few constant values, which undermines its accuracy.

This paper follows similar ideas to [4] by selecting tractable sets of parameters, and improving the computational aspects tremendously while at the same time guaranteeing stability. For the purpose, this paper uses Kharitonov's theorem, which guarantees robust stability of a given transfer function (stability over all possible values of its coefficients in a given range) by analysing the stability of just four polynomials. The advantages are: 1) it is a necessary and sufficient condition, and we can further use this criteria for robust parameter design (Section IV) and 2) it is computationally efficient as it reduces the initial infinite number of tests to only four which makes the robust design problem tractable. Based on practical IGBT behaviours and desired outcomes of control in IGBT collector-to-emitter voltage ramps, three operating points are carefully selected and analysed under different sets of AVC parameters. Experimental results show a high agreement with the proposed theoretical analysis with regard to the robust stability.

II. AVC SCHEME

A. AVC Structure

The idea of AVC is to apply the collector-voltage feedback loop so as to achieve the direct control of the IGBT collector-emitter voltage V_{CE} by comparing the scaled feedback of V_{CE} and a well-defined reference. In order to achieve a stable and fast response, two extra feedbacks were used [4]: gate voltage feedback H_G for faster response and *dv*/*dt* feedback H_R for stability as shown in Fig. 2. But it will be shown later that both feedbacks are optional with the availability of high-performance op amps. By feedbacking the load current I_L, the gating delay becomes predictable.

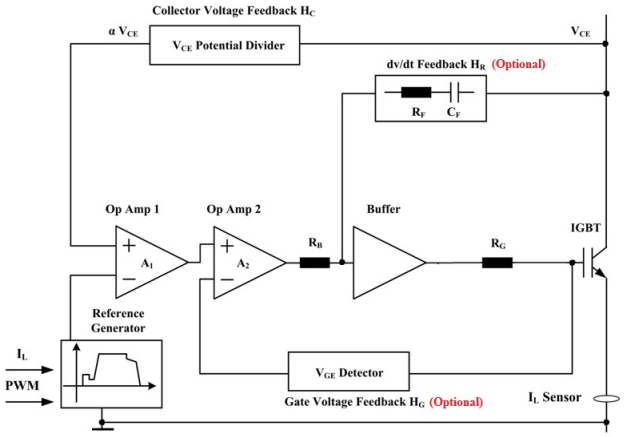

Fig. 2. The schematic of AVC.

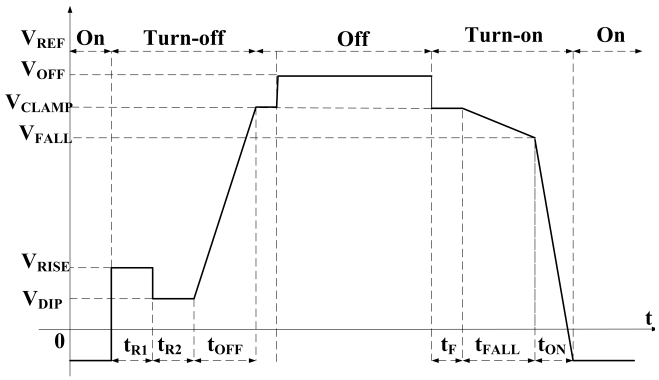

Fig. 3. AVC reference.

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B. AVC Reference

AVC reference is triggered at the edges of PWM signals. Initially proposed for IGBTs connected in series [6], the reference was generated by an simple analogue circuit. Thus, the reference is hard to become a sophiscated shape to cope

with the nonlinear IGBT switching. With an digital FPGA used on the AVC board, the reference generation is improved to better suitthe nonlinear IGBT switching transient as shown in Fig. 3 [19]. For the previous reference, it has some limitations as shown in Fig. 4. An lengthened pre-conditioning step will lead to more power losses, and shortening the step to less than the gating delay will lead to poor controlled switching and possibly oscillations that might cause EMI issues.

This nonlinear transient mainly results from the renowned V_{CE}-dependent Miller capacitance [7, 14-15]. Thus, a better reference solution for IGBT turn-off is to divide the pre-conditioning step into two [3.19]: t_{R1} and t_{R2}. With the first platform, V_{RISE} in t_{R1} overdrives the buffer to charge the IGBT input capacitance. The second platform V_{DIP} with a duration of t_{R2} mitigates the gate current in t_{R2} to cope with the sudden drop of the IGBT Miller capacitance. By applying the two reference steps, V_{DIP} deals with the sharp varying of Miller capacitance nicely in a physics-based IGBT model from Fig. 5. V_{CLAMP} can be used to limit the overshoot voltage. For turn-on, a constant pre-conditioning step is added to deal with the turn-on gating delay. All the reference parameters settings have been carefully discussed in [19] and therefore, are not further discussed here.

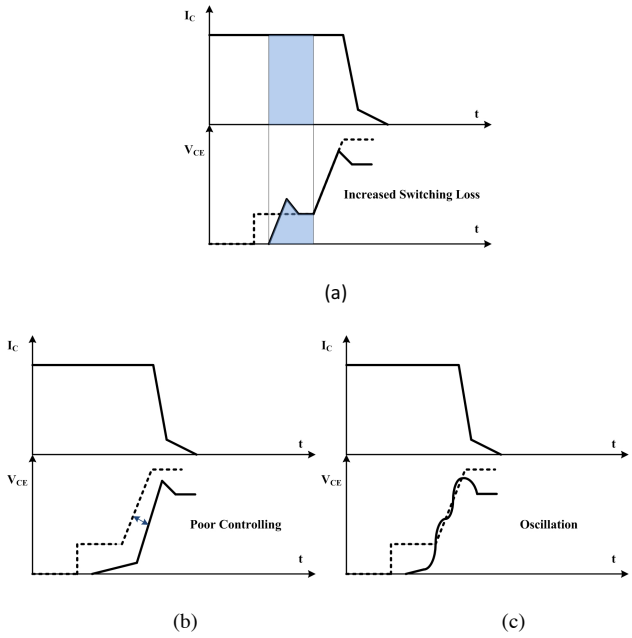

Fig. 4. Illustration of improper pre-conditioning step for a single IGBT switching: (a) increased switching loss; (b) poor control of V_{CE}; (c) oscillation of V_{CE}.

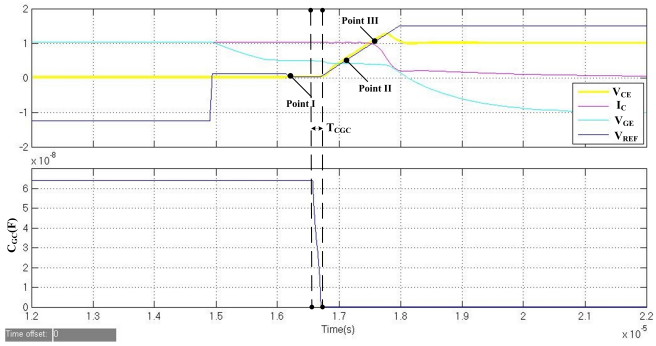

Fig. 5: Normalised SKM400GA173D IGBT **AVC** turn-off waveforms under Palmer-Byrant Model (V_{DC}=800 V, I_L=60 A) and the collector-to-emitter capacitance varying during turn-off.

III. MODELLING AND STABILITY ANALYSIS

The small-signal approach is a suitable perspective to study the system pole-zero distribution; however, it is only valid in the active region of IGBT. In this work, the stability discussion is mainly about turn-off process. From Section II, the nonlinear IGBT turn-off process has been carefully considered divided into two functional linearised sub-sections, which is a common solution to nonlinear control problems. The focus here is on IGBT active region where V_{CE} can be well regulated to even sophisticated "S" shape for EMI reduction [20]. The first step is to derive an accurate system transfer function from a small-signal model. Then, three sample operating points are selected for analysis in the collector voltage rise as shown in Fig. 5. The linearised IGBT parameters (mainly C_{GC}, C_{CE}, g_m) are strongly dependent on the operating conditions (voltage, current, temperature etc) [14]. Typically, there is high uncertainty on IGBT parameters in real applications. Based on a reasonable parameter estimation via the Palmer-Bryant Model, uncertainties on C_{GC}, C_{CE} and g_m are carefully chosen for analysis.

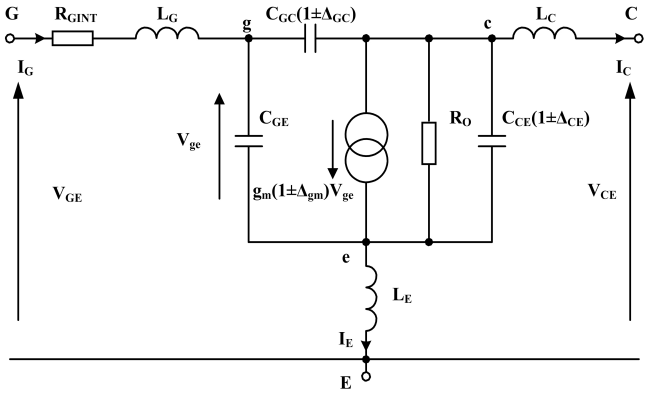

Fig. 6. Small-signal IGBT model with parameters uncertainties.

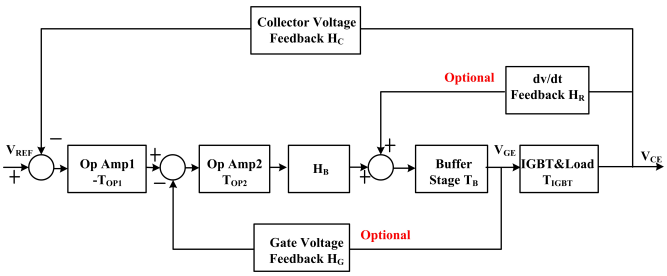

Fig. 7. The control system representation of an IGBT under AVC.

A. Modelling of the IGBT and AVC

A small signal IGBT model based on MOSFET *T* model is employed here with suitable modifications in Fig. 6 [2]. It takes into account the IGBT internal gate resistance R_{GINT} and the terminal stray inductances. Due to the charge stored in the base region, the *dv*/*dt* achievable by an IGBT is smaller than that of a similar MOSFET. The extra charge extraction capacitance C_O [15] in the base region appears in parallel with C_{CE}, and so is incorporated into C_{CE}. The pronounced Early effect can be modelled as an output resistance R_O, which captures the fact that the saturation current increases with the collector voltage in the active region. According to the transfer function derivation in the chopper circuit [4], the transfer function for IGBT turn-off is given by:

$$T_{IGBT} = \frac{V_{CE}}{V_{GE}} = \frac{a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0}{b_3 s^3 + b_2 s^2 + b_1 s^1 + b_0}$$

where the coefficients are:

$$a_0 = -g_m R_O$$
$$a_1 = C_{GC} R_O$$
$$a_2 = L_E (C_{GC} + C_{GE} + g_m C_{GC} R_O)$$
$$a_3 = L_E C_T R_O$$

$$b_0 = 1$$
$$b_1 = R_O (C_{GC} + C_{CE}) + R_{GINT} (C_{GE} + C_{GC} (1 + g_m R_O))$$
$$b_2 = R_O R_{GINT} C_T + (L_G + L_E)(C_{GE} + C_{GC} (1 + g_m R_O))$$
$$b_3 = R_O (L_G + L_E) C_T$$
$$C_T = C_{GC} C_{GE} + C_{GE} C_{CE} + C_{GC} C_{CE}$$

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The AVC control system is shown by a block diagram as shown in Fig. 7. The detailed transfer functions are attached in Appendix. The whole transfer function open-loop T_{OL} and close-loop transfer function T_{CL} are expressed as:

$$T_{OL} = -T_B T_{IGBT} H_R + T_{OP2} T_B H_G - T_{OP1} T_{OP2} T_B T_{IGBT} H_C$$

$$T_{CL} = \frac{-T_{OP1} T_{OP2} T_B T_{IGBT}}{1 + T_{OL}} = \frac{d_6 s^6 + d_5 s^5 + d_4 s^4 + d_3 s^3 + d_2 s^2 + d_1 s^1 + d_0}{c_8 s^8 + c_7 s^7 + c_6 s^6 + c_5 s^5 + c_4 s^4 + c_3 s^3 + c_2 s^2 + c_1 s^1 + c_0}$$

The parameters of the denominator play the most important role in determining the system stability. They are given by :

$$c_0 = (k_0 + y_0 + v_0 + u_0)$$
$$c_1 = (k_1 + y_1 + v_1 + u_1)$$
$$c_2 = (k_2 + y_2 + v_2 + u_2)$$
$$c_3 = (k_3 + y_3 + v_3 + u_3)$$
$$c_4 = (k_4 + y_4 + v_4 + u_4)$$
$$c_5 = (k_5 + y_5 + v_5)$$
$$c_6 = (k_6 + y_6 + v_6)$$
$$c_7 = (k_7 + y_7)$$
$$c_8 = (k_8)$$

Due to the complexity of the system, all the polynomials k_i, y_j, v_m and u_n (i, j, m, n are the indexes) are listed in Appendix.

B. Parameter Values

The IGBT used in this paper is 1700V/650A 2MBI650VXA-170E-50, the latest FS-IGBT. Within this model, some parameters do not change values with switching conditions and can be obtainedby measurement or estimation. The terminal inductances L_C, L_G and L_E were estimated to be 100 nH, 15 nH and 1.0 nH respectively. The IGBT internal gate resistance R_{GINT} is found to be 2.0 Ω by measurement. The default AVC designs are given in Table I. Both of the new AVC designs apply a push-pull emitter-follower that can be used to provide a very high analog bandwidth (the transitional f_T>130 MHz) and satisfactory gate currents (6A continuous current). It is worth to point out that in the new design II, the current-feedback op-amps are used to provide a very high bandwidth. It can be shown later that the AVC speed and performance are much improved compared with the design in [4].

There are some other parameters varying according to the operating conditions. g_m can be roughly estimated from the manufacturer's datasheets. R_O can be obtained from the I-V output characteristics. But manufacturers do not normally provide sufficient data to infer a reasonable value of R_O. A high-power curve tracer was used to measure the IGBT characteristic curves in order to obtain better values of R_O and g_m. The most important parameters, terminal capacitances (C_{CE}, C_{GC} and C_{GE}) are given in the datasheet but these values are measured at zero gate voltage, low collector-to-emitter voltage and zero collector current. Thus, those values cannot represent the actual values during the switching transient.

In practice, however, C_{CE} is much larger due to the charge stored in the wide drift region of the device during the conduction period. C_{GC} is also found to be much larger due to the increased effective doping [21]. The device parameters, mainly C_{GC}, C_{CE}, and g_m, vary greatly throughout the switching. To obtain suitable values at normal room temperature 20°C , an accurate IGBT physical model-the Palmer-Bryant IGBT model [13]- is used to extract a satisfactory degree of parameter

accuracy. They have been listed on the Table II. This set provides a very sensible baseline for IGBT parameter uncertainty consideration. With a reasonable range added on the main parameters of Table II, the IGBT small-signal transfer fucntion will represent the IGBT turn-off process with a high degree of accuracy.

TABLE I. THE DEFAULT DESIGNS OF THE AVC CIRCUIT

	Op-amp 1		**Op-amp 2**		**Buffer Stage**	***dv/dt* Feedback**		**V_{CE} Feedback**	
Device	**LM7171**		**LM7171**		**BUF634**	**RC**		**RC**	
Design I	**A_1**	**f_{OP1}(MHz)**	**A_2**	**f_{op2}(MHz)**	**f_B(MHz)**	**C_F(pF)**	**R_F(Ω)**	**α**	**f_{FB}(MHz)**
	10	20	1	100	180	50	10	1/100	32
Device	**THS3091**		**THS3091**		-	**RC**		**RC**	
Design II	**A_1**	**f_{OP1}(MHz)**	**A_2**	**f_{op2}(MHz)**	-	**C_F(pF)**	**R_F(Ω)**	**α**	**f_{FB}(MHz)**
	10	200	1	220	-	50	10	1/100	32

TABLE II. PARAMETER VALUES OF IGBT DURING AVC SWITCHING (T= 20 ° C)

	V_{CE}(V)	**I_C(A)**	**V_{GE}(V)**	**C_{GC}(nF)**	**C_{GE}(nF)**	**C_{CE}(nF)**	**g_m(S)**	**R_O(Ω)**
Datasheet	15	0	0	4.5	60.0	1.7	-	-
Point I	10	50	7.5	85.1	60.0	35.4	90	55
Point II	400	50	7.5	0.91	60.0	10.1	90	55
Point III	800	45	7.5	0.47	60.0	2.4	140	55

IV. STABILITY ANLYSIS

A. *Theory*

Before presenting our main result, we will first introduce the definition of stability. A dynamical system is stable if its has a bounded output for any bounded input. Mathematically, if all the roots of a polynomial p(s) have negative real parts, we say that the polynomial is stable (sometimes the term Hurwitz is used). For a linear system, if its transfer function G(s) has a stable denominator, then the system is stable.

A root of p(s) on the left-half plane is called a stable pole of G(s). Otherwise, it is called an unstable pole. It then follows that a transfer function with only stable poles is stable, and otherwise it is unstable. System time-responses are closed related to the location of the poles in the complex plane.

Next is an example that illustrates the stability of a transfer function: consider the following transfer function

$$G = \frac{a_2 s^2 + a_1 s^1 + a_0}{b_3 s^3 + b_2 s^2 + b_1 s^1 + b_0}$$

with $a_2 = 1, a_1 = 2, a_0 = 1$ and $b_3 = 1, b_2 = 2, b_1 = 2$ and $b_0 = 1$.The stability of this transfer function can be tested by looking at the roots of the denuminator. In this example, the roots are -1, -5+0.866i and -5-0.866i and therefore the system is stable.

However, the computation complexity for finding roots of a given polynomial is high and typically includes numerical issues for large polynomial degrees. Luckily, there is an alternative effective test for determining stability that does not require an explicit solution of the algebraic equation. The Routh-Hurwitz Stability Criterion only involves computing the determinants of some low-dimensional matrices [16]. Still, this low computation complexity criterion is only applicable to fixed transfer functions, i.e. all the parameters must be determined and time-invariant, which is not suitable for our analysis.

In this section, we shall investigate the robust stability when the system is approximately known. We shall introduce the Kharitonov's theorem, a powerful generalization of the Routh-Hurwitz test to polynomials whose coefficients vary within known intervals. It is simple and efficient method, as it involves the Routh-Hurwitz test of only four polynomials. Basically, it gurantees the stability of all possible values of its coefficients in the above intervals.

Theorem 1[Kharitonov's Theorem][17]: Consider a polynomial

$p(s) = a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + \ldots + a_n s^n$, where

$l_i \leq a_i \leq u_i$, for all i, and the leading coefficient $0 \notin [l_n, u_n]$.An interval polynomial is stable (i.e. all members of the family are stable) if and only if the four Kharitonov polynomials

K1: $l_0 + l_1 s + u_2 s^2 + u_3 s^3 + l_4 s^4 + l_5 s^5 + \cdots$

K2: $u_0 + u_1 s + l_2 s^2 + l_3 s^3 + u_4 s^4 + u_5 s^5 + \cdots$

K3: $l_0 + u_1 s + u_2 s^2 + l_3 s^3 + l_4 s^4 + u_5 s^5 + \cdots$

K4: $u_0 + l_1 s + l_2 s^2 + u_3 s^3 + u_4 s^4 + l_5 s^5 + \cdots$

ar stable.

Remark: What is remarkable about Kharitonov's result is that we need to test only four polynomials for stability to verify an infinite number of them. In addition, each of the four polynomials can be tested for stability using efficient methods such as the Routh-Hurwitz criterium. Hence, it only takes four times more work to check stability of an interval polynomial than it takes to test one ordinary polynomial.

As an example, consider the following transfer function

$$G = \frac{a_2 s^2 + a_1 s^1 + a_0}{b_3 s^3 + b_2 s^2 + b_1 s^1 + b_0}$$

with $a_2 = 1, a_1 = 2, a_0 = 1$ and $b_3 \in [1,2], b_2 \in [0,1], b_1 \in [3,4]$ and $b_0 \in [-1,2]$.

From Kharitonov's theorem, the stability of G can be checked by simply testing the stability of the following four polynomials:

K1: $-1 + 3s + 1s^2 + 2s^3$

K2: $2 + 4s + 0s^2 + 1s^3$

K3: $-1 + 4s + 1s^2 + 1s^3$

K4: $2 + 3s + 0s^2 + 2s^3$

Which can be done using the Routh-Hurwitz criterium.

B. Internal Stability

Now we consider the internal stability of the closed loop system. Unlike the input-output stability we have discussed above, internal stability concerns the stability of internal states. A system is called internally stable, if the internal state of the system is bounded for bounded inputs. That is, we treat V_{REF} still as input but V_{GE} as output. The transfer function has the following form $T_{INT} = \frac{-T_{OP1} T_{OP2} T_B}{1 + T_{OL}}$. We can apply Routh-Hurwitz criteria to T_{INT} to test the internal stability and similarly, we can study the robust internal stabiity using Kharitonov theorem when there exist parameter uncertainties in the model. In this particular example, we found that the pole of T_{INT} have the same pole as T_{CL} and there are no unstable pole-zero cancellation;

since the cancelled term $b_3s^3 + b_2s^2 + b_1s^1 + b_0$ of T_{IGBT} is stable (This can be checked since for any third order system $p(s) = c_0 + c_1s + c_2s^2 + c_3s^3$, where $c_i>0$, the Routh-Hurwitz stability test is $c_2c_1 > c_3c_0$, we can verify this for T_{IGBT} by substituting the expressions for b_i by using values in Table II). Therefore, the internal stability for the system we study here is equivalent to the input-output stability. The system stability can be judged by the appearance of V_{GE} with V_{REF} as input.

C. Analysis

During a single turn-off transient, IGBT variables V_{CE} and I_C go through a very large range. This means that the IGBT will experience a wide range of operating points. As a consequence, it is difficult to analyse the system stability at every operating point. Also, it is also of little nececessity given the switching transient is normally very short.

In order to assess the system stability, appropriate to the switching process adopted here, a small number of sampled operating points may be selected to investigate the system stability. As the reference signal is carefully chosen to deal with the initial delay stage, we do not need to analyse the stability for the operating points during the delay stage. However, the early stage of the ramp time immediately follows the delay and it is possible that the response remains slow. Once the voltage has risen, the response is fast and a further sample point is therefore needed. The high voltage response is also important as the current drops again leading to a poor response, so a third sample is necessary. The three operating points (Points I, II and III) are shown in Fig. 5. They are able to depict a reasonably good general profile of the whole voltage ramp.

With the assumptions in the Palmer-Bryant IGBT model, even with an advanced time-costly optimisation process, there are still parameter deviations from the real values that were not taken into account. For example, some IGBT parameters are strongly temperature-dependent [14]. Both factors leads some uncertainties in the IGBT parameters, mainly C_{GC}, C_{CE} and g_m. In practice, instead of finding the exact parameter values, a proper estimation about the parameter uncertainty is much more feasible and reasonable. In Fig. 6, Δ_{CE}, Δ_{GC}, and Δ_{gm} represent the uncertainty percentages of $C_{CE,}$ C_{GC} and g_m respectively. We will consider the uncertainties in all three parameters. From [14], C_{CE} has around 10% variance from 20 to 100 ^oC. Therefore, a range of 10% uncertainty is applied on C_{CE} for the system robustness investigation. For C_{GC}, a similar 10% uncertainty is considered. Due to the large nonlinearity at low currents, g_m's uncertain range is considered to be around 20%. If the method in [4] were employed for analysis, there would be a infinite number of bode plots that are needed to be analysed by taking into account of every combination in the range of $[C_{CE}-\Delta_{CE,}C_{CE}+\Delta_{CE}]$, $[C_{GC}-\Delta_{GC,}C_{GC}+\Delta_{GC}]$ and $[g_m -\Delta_{gm,}g_m +\Delta_{gm}]$, which is practically impossible. Therefore, Kharitonov's therom must be applied.

The whole system has been described in terms of transfer functions. The performance is studied using Matlab. By considering the IGBT parameter uncertainties, Design I is unstable at operating Points II and III except Point I. Increasing R_G can stablise the system but at the expense of more power losses and longer gating delay. Therefore, it cannot provide an ideal solution for the AVC design. R_G for both designs are chosen to be 2 Ω. Taking off the two extra feedback loops, the situtaion does not become better for Design I.

V. THERE ARE SOME OTHER DEGREES OF FREEDOM IN AVC DESIGN: THE BANDWIDTHS OF OP AMPS, THE COLLECTOR VOLTAGE FEEDBACK H_C AND THE BUFFER. THE SECOND OP AMP'S BANDWIDTH F_{OP2} AND THE BUFFER BANDWIDTH F_B HAVE LITTLE EFFECT ON THE SYSTEM STABILITY. BY COMPARISON, THE FIRST OP AMP BANDWIDTH F_{OP1} AND THE COLLECTOR VOLTAGE FEEDBACK H_C BANDWIDTH F_{FB} ARE VERY IMPORTANT. INCREASING F_{OP1} AND F_{FB} ABOVE 50 MHZ CAN BOTH STABLISE THE SYSTEM. THEREFORE, DESIGN II WITH A VERY HIGH OP-AMP BANDWIDTH BECOMES A VERY PROMISING SOLUTION FOR STABILITY WITHOUT INCREASING THE GATE RESISTOR. THE GATE VOLTAGE FEEDBACK H_G IS KNOWN TO INCREASE THE RESPONSE OF THE SYSTEM [4]. HOWEVER, ONLY WITHOUT THE GATE VOLTAGE FEEDBACK H_G, DESIGN II BECOMES STABLE. *DV/DT* FEEDBACK PREVIOUSLY IS KNOW TO BE CRUCIAL TO STABLISE THE SYSTEM. BUT FOR DESIGN II, EVEN IF THE *DV/DT* FEEDBACK H_R IS MISSING BY SETTING R_F TO INFINITE, DESIGN II IS STILL STABLE.THE STRAY INDUCTANCE L_G ALSO PLAYS AN IMPORTANT ROLE IN THE SYSTEM STABILITY. IF THERE IS NO GATE STRAY INDUCTANCE, THE SYSTEM COULD BE STABLE AND TOLERANT OF SLIGHTLY LARGER UNCERTAINTIES ON THE THREE NONLINEAR PARAMETERS (A 2% INCREASE IN THE ABSOLUTE VALUE). EXPERIMENTAL RESULTS

Double pulse tests have been performed to obtain the following experimental results. The experimental circuit is a boost converter used as a clamped inductive load test circuit that has a very similar small-signal model as a stanard chopper cell as shown in Fig. 8. The leg under test is set to operate at 800V and 50 A. In this work, we will investigate the IGBT at comparatively low currents since the nonlinearity in the IGBT characteristics is significantly greater at lower currents [14]. For example, g_m is nonlinear with current, becoming almost constant at high currents.

As we discussed in Section III, the system stability can be judged by the appearance of V_{GE} that has a well-scaled transients instead of the large-scaled V_{CE} trace. The controller performance can be well observed from the V_{GE} appearance. For design I with all the feedback added, high-frequency noises that is spotted as similar as in [4] on V_{GE} become very large. Taking it off can kill the high-frequency noices on V_{GE}. From our theoretical analysis, design I without V_{GE} feedback is unstable. The corresponding experimental result is shown in Fig. 9. Oscillation is also clearly observed in V_{GE}, and in phase with the V_{CE} oscillation, with an approximate frequency of 3 MHz. Without *dv/dt* feedback, the oscillation becomes worse with an increased amplitude as shown in Fig. 10.

From our analysis, it would be of great interest to test Design II as even without *dv/dt* feedback added Design II is stable. The result is plotted in Fig. 11. It can be seen that V_{GE} is well damped and V_{CE} is well contolled to follow the reference ramp with slight errors on Point III. When *dv/dt* feedback is added, there is little difference to observe. In order to test the robustness of Design II, we continue the tests using Design II. This design should be stable through a large temperature range from 20 to 100 ºC. In From Figs. 11 to 13, Design II is tested at different temperatures 20, 60 and 100 ºC respectively. In order to observe the appearances of V_{GE}, the reference *dv/dt* ramps in Figs 12 and 13 are lengthened intentionally. Also, with the increase of temperature, the maximal *dv/dt* that can be driven by AVC is slower [14]. It can be seen that the system is robustly stable as expected and no oscillation is identified. V_{CE} is under damped at the start and follows V_{REF} nicely afterwards.

To better test the stability and robustness of AVC, another experiment is set up. A high-frequency disturbance signal, which is a small triangular waveform (frequency f_{REF}, amplitude Δ_{REF}=0.1 V), is added to the V_{REF} ramp as shown in Fig. 8. The small disturbance signal will cause about 10 V disturbances on V_{CE} trace. This is a very effective way to test the system stability. Therefore, f_{REF} is chosen to be 1.67 MHz, 3.33 MHz, 5 MHz and 10 MHz respectively, Figs. 15 to 18. These experiments are carried out at 20 ºC. In Figs. 15 to 18, the system stays stable. V_{CE} still tracks V_{REF} well. V_{GE} is also well damped. More importantly, with such a disturbance signal, V_{GE} is still stable. The disturbance signal's effects on V_{GE} are well constricted. According to the results in Fig. 11, Design II, V_{CE} oscillates at around 3 MHz. Therefore, a triangular disturbance signal of 3.33 MHz is used to test Design I with *dv/dt* feedback as shown in Fig. 19. V_{GE} oscillation amplitude is increased due to the disturbances compared with Fig. 9. The turn-on switching under both designs are shown in Fig. 20 and 21. Although both designs constrain the current overshoots well compared with hard-switching, the ringing for Design II without *dv/dt* feedback would cause EMI issues. On the other hand, V_{GE} in Fig. 20 is well damped even with a fast reference.

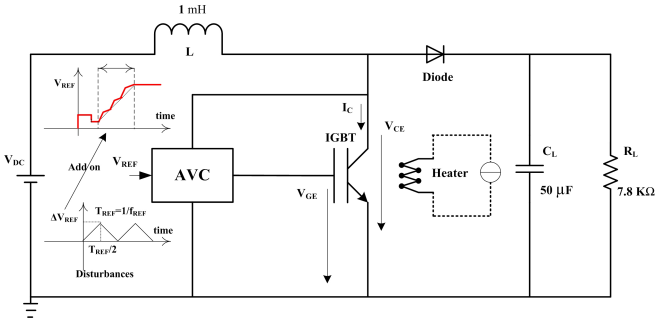

Fig. 8. Experimental boost converter as a clamped inductive load test circuit with a triangular disturbance signal on AVC reference input.

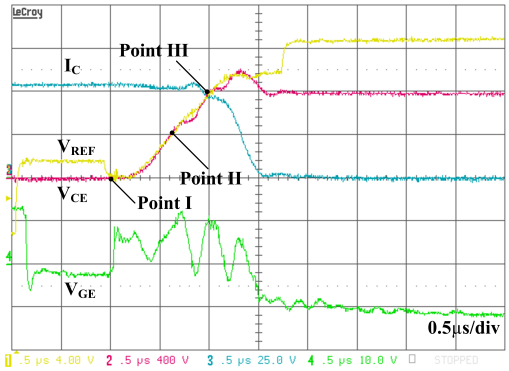

Fig. 9. IGBT turn-off under AVC Design I without V_{GE} feedback.

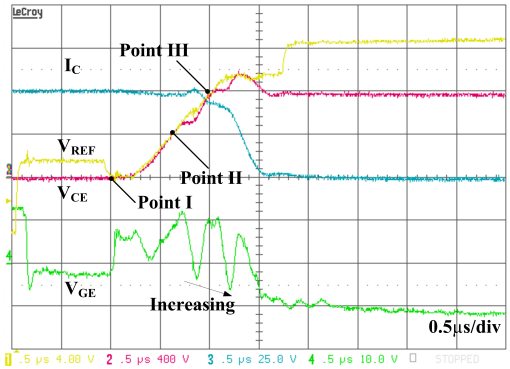

Fig. 10. IGBT turn-off under AVC Design I without V_{GE} feedback and *dv/dt* feedback.

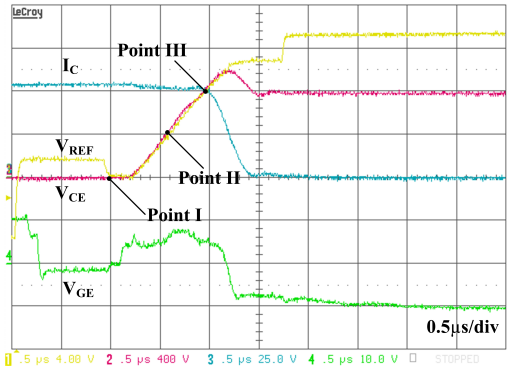

Fig. 11. IGBT turn-off under AVC Design II without V_{GE} feedback and *dv/dt* feedback at **T= 20 ºC**.

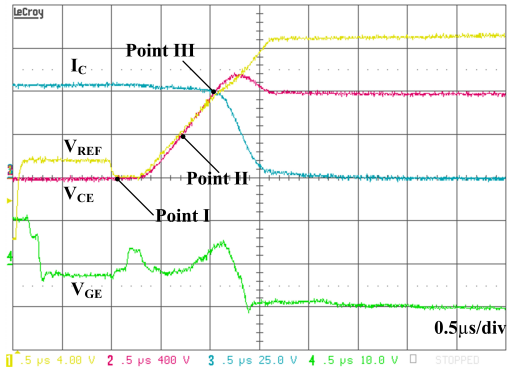

Fig. 12. IGBT turn-off under AVC Design II without V_{GE} feedback and *dv/dt* feedback at **T= 60 ºC**.

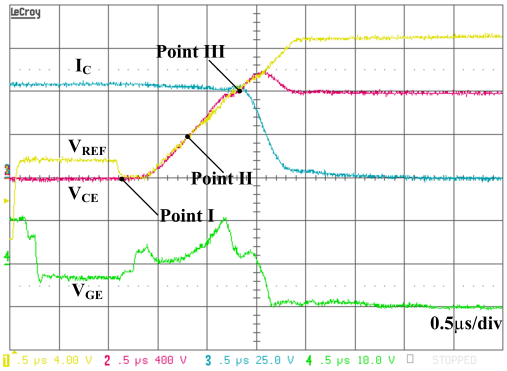

Fig. 13. IGBT turn-off under AVC Design II without V_{GE} feedback and *dv/dt* feedback at **T= 100 ºC**.

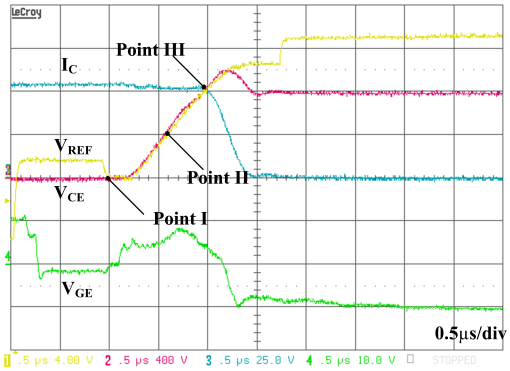

Fig. 15. IGBT turn-off under AVC Design II without V_{GE} feedback and *dv/dt* feedback under a triangular disturbances of **f_{REF}=1.67 MHz**.

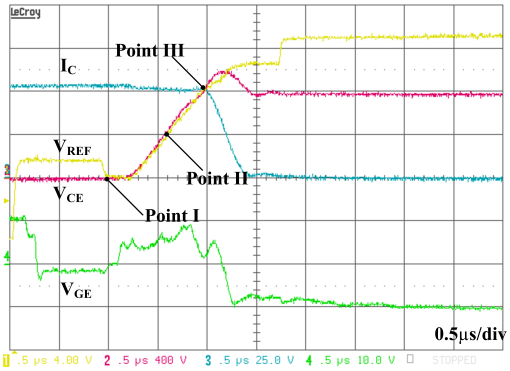

Fig. 16. IGBT turn-off under AVC Design II without V_{GE} feedback and *dv/dt* feedback under a triangular disturbances of **f_{REF}=3.3 MHz**.

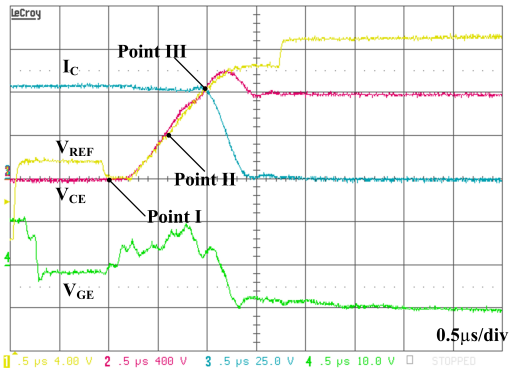

Fig. 17. IGBT turn-off under AVC Design II without V_{GE} feedback and *dv/dt* feedback under a triangular disturbances of **f_{REF}=5 MHz**.

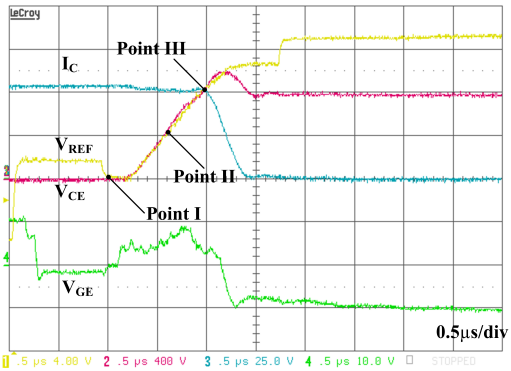

Fig. 18. IGBT turn-off under AVC Design II without V_{GE} feedback and *dv/dt* feedback under a triangular disturbances of **f_{REF}=10 MHz**.

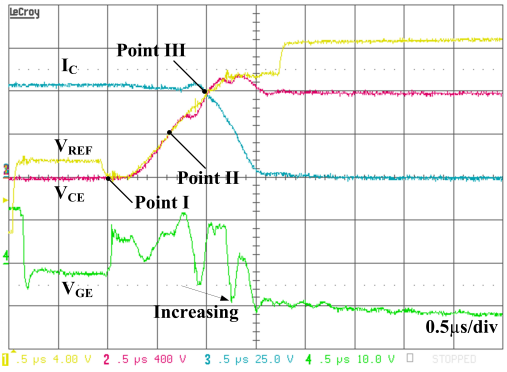

Fig. 19. IGBT turn-off under AVC Design I without V_{GE} feedback and *dv/dt* feedback under a triangular disturbances of **f_{REF}=3.3 MHz**.

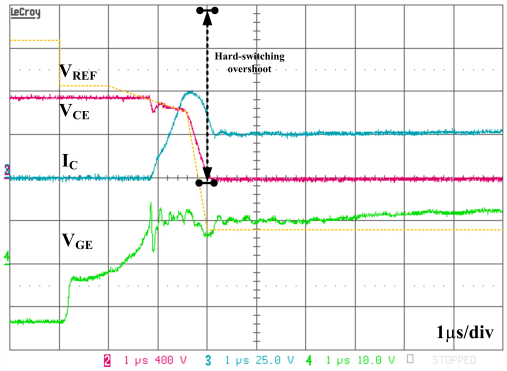

Fig. 20. IGBT turn-on under AVC Design II without V_{GE} feedback and *dv/dt* feedback

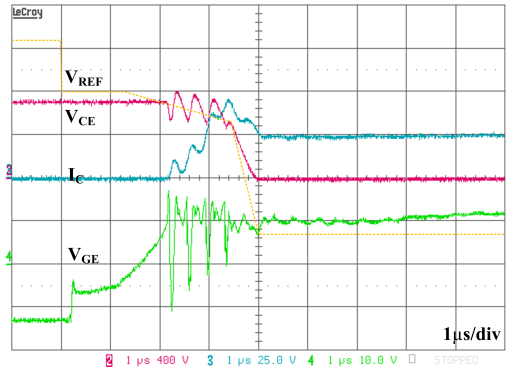

Fig. 21. IGBT turn-on under AVC Design I without V_{GE} feedback but with *dv/dt* feedback.

VI. DISCUSSION

The whole system investigated in this paper is a popular chopper cell circuit, composed of AVC gate drives, IGBTs and diodes. Its modelling complexity lies the factor that both the high-frequency signal processing (AVC controller part) and low-frequency as conventionally operated power processing (IGBT-and-diode commutation) co-exist in the system. Each part has a significant impact on the whole system and no obvious simplification is possible. This leads to an eigth-order transfer function as it is shown in Section III. This transfer function is based on circuit analysis and has been used for the system stability analysis [4-5, 8]. It seems that by selecting several operation points with derived linearised IGBT parameters, a practical guideline for IGBT close-loop gate drive design can be achieved. However, the parameter uncertainty of our control target IGBT undermines this approach. Therefore, Kharitonou's theorem is called for to deal with the parameter uncertainty issue. But an accurate IGBT simulation model with in-depth understanding of IGBT physics [6, 14] is still of great significance for the system modelling and stability. It can provide the system stability analysis with satisfactory IGBT parameter values. Thus, the difficulty of analysis can be reduced and an optimal AVC design is easier to achieve. In our analysis, Points II and III in our work are found to be more prone to instability. Point I, the same with the Pre-conditioning delay point in [4], is more likely to be stable. This conclusion is consistent with that in [4]. The approach adopted here is applicable to turn on, where a similar set of sample points may be chosen. But sharping shifting operating points, three operating points might look insufficient. Considering the fast switching durtaion (microscends based), the controller's stability might be difficult to judge (Oscillation period might be comparable to the swithcing duration). That is why the proposed small signal disturbance signal testing method is significant. This approach can be very effective to test the stability, Fig 19.

However, from our results, it can be seen that a good design that is stable at turn-off seems to perform well at turn-on as well. For different switching conditions (different currents), IGBT parameters would be quite different, scientifically it is imperative to analyse each switching condition in order to achieve a robust stable design. However, it has been found in our experiments that Design II works well for high currents (100A switching in Fig.22 can well represent FS-IGBT high currents operation.) as well. It should be noted that with super fast op-amps and modified references, the current AVC is able to drive IGBT switching *dv/dt* as fast as hard-switching. In our tests for 800V/50A conditions, the maximal hard-switching *dv/dt* is

about 1 kV/μs, which is almost the same as AVC-switching. Therefore, in order to achieve even faster *dv*/*dt* control, a better drive stage needs to be employed.

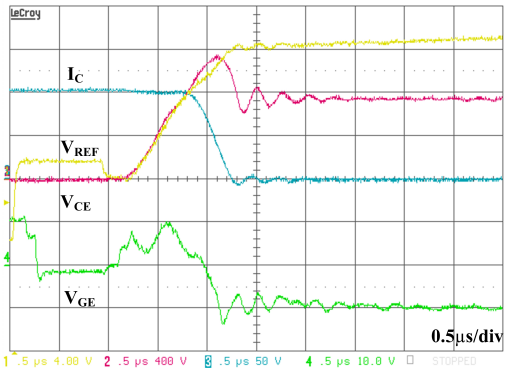

Fig. 22. IGBT turn-off at 100A under AVC Design II without V_{GE} feedback and dv/dt feedback

The gate resistor value is the most important factor in all kinds of gate drive designs [10-13]. Here, it also plays a very important role in achieving AVC robust stability. From a transfer function perspective, the system with a larger gate resistor is more stable. However, there are important trade-offs with a large gate resistor: it will lead to a longer delay and more power losses. In addition, the switching speed is more limited. Therefore, this approach is not ideal.

The stray inductance at the gate L_G has also a strong impact on the system stability.. If no gate stray inductance is included at the gate drive or inside IGBTs, the system becomes more robust stable. This is consistent with the gate drive design principle that the gate stray inductance L_G needs to be eliminated to avoid the LCR oscillation caused by the L_G, R_G and IGBT parasitic capacitances. Achieving this is difficult nonetheless.

A detailed investigation on the parastics inductances' effects on stability has been done in [8] with different IGBT products by the linear time-constant theory (Root locus plots). The work provided a practical approach to make the close-loop gate drive design more "robust" and suitable for the large IGBT market. However, it can be found that the analysis has to be done for each specific IGBT with the exact knowledge of all parameters. Given the uncertainties in IGBT parameters, the approach in [8] cannot guarantee the stability.

Our future work can be to apply the proposed method in this paper to investigate "robustness" in different IGBT products. Given the same rated IGBT from different manufactors, we can find a range for the parasitics inductances and then use the Kharitonov therom. What is more important, such robustness problem can be solved by a computationally efficient algorithm with theoretical stability guarantee. However, given a expanded range, design such an omniponent controller with optimal performances might be demanding as in [8].

In [4], it claims that the extra two feedbacks are all proven to be very effective in improving the system stability and optimising the response. In our analysis above, the *dv*/*dt* feeback H_R is still an important factor in stablising the system when the op amp bandwidth is limited. The gate voltage feedback H_G has been found in experiments to improve the response speed but it also needs better design to avoid the introduction of instability on the gate voltage, which arises from the limited gain

bandwidth product and phase margin of the LM 7171 Op Amp used. According to our analysis and results, the first Op Amp bandwidth and the V_{CE} feedback bandwith play a dominant role in stablising the system. While both factors have been long discussed [1-5], the solution is only feasible as the high-slew-rate and wide-swing Op Amps with high gain-bandwidth become available.

For a theoretically stable AVC gate drive, according to the control analysis, its time-response performance is not always treated as acceptable in practical applications. For example, some damping performance might be considered as stable in the stability perspective. However, in the AVC design of high-power IGBTs, a large damping of V_{CE} would cause high EMI, Fig. 21. ESpecially when close tracking is needed to shape a sophisticated "S" shape for EMI reduction in [20], a very smoothed and limited damping is expected. Furthermore, it also might negatively affect the transient control of series-connected IGBTs due to the differences of charge distribution and depletion region growth in different IGBTs. The desired stable performance of AVC gate drives is that V_{CE} nicely following the reference without any deviation. The voltage overshoot clamping function is proven to be able to be implemented by AVC [1,20], it has to be admitted in [21] that EMI suppresion is limitted at low and middle currents at the expense of more power losses. Furthermore, for high current switching, tracking errors are observed around Point III as shown in Fig. 22. The control around this point is dominated by the rapidly changing IGBT parameters so a tight control (large gain) might be needed. The clamping effects can be observed in Fig. 19 with instable performances at other operating Points. Therefore, the system stability analysis would be the first step in AVC design.

VII. CONCLUSIONS

- The difficulty of designing an IGBT controller in a conventional way arises because the transfer functions of each part have a significant effect, and no obvious simplification is possible. In addition, the characteristics of the IGBT change with current, voltage, temperature and stored charge.
- By practical consideration of the IGBT behaviour and the desired outcome of control in the voltage ramps, three operating points can be selected, and a reasonable parameter estimation range is attached to each. Then, Kharitonov's theorem is applied, thereby judging the overal system stability of IGBT turn-off under AVC.
- The experiments conducted using well charaterised components indicate the agreement with the theoretical analysis regard stability. The robustness has been fully tested by utilising a high-frequency disturbance signal to input V_{REF}.Thus, the Klasnikov approach adopted here has been shown to account for the main variations in the parameters in a convincing manner.
- Thereby, we obtain an accurate transfer function of the IGBT and its AVC controller. Treating the range of parameters as uncertainties in IGBT parameters and in accuracies in the parameter extraction process used, Kharitonov's theorem provides both a necessary and sufficient condition for stability. Such confidence in the stability estimation can then underpin a computationally efficient guideline for high performance AVC design.

ACKNOWLEDGMENT

The authors thank Fuji Electric co. ltd. for the supply of IGBT modules. Xin Yang would like to thank the Henry Lester Trust and the Cambridge Overseas Trust for their generous support during his research life at Cambridge. Ye Yuan and Jorge Goncalves would like to thank EPSRC for the support through project EP/I03210X/1 and EP/G066477/1.

APPENDIX

The V_{CE} potential divider for the collector-voltage feedback is regarded as a low-pass filter with the voltage ratio α and the cut-off frequency f_{FB}

$$H_C = \frac{\alpha}{1 + s/(2\pi f_{FB})}.$$

The high-bandwidth Op Amps can be modelled as low-pass filters

$$T_{OP1} = \frac{-A_{OP1}}{1 + s/(2\pi f_{OP1})}$$

$$T_{OP2} = \frac{A_{OP2}}{1 + s/(2\pi f_{OP2})}.$$

The resistor R_B is employed at the input of the buffer stage while the dv/dt feedback H_R is directly connected to the input. The transfer functions for the buffer T_B and H_R are:

$$H_R = \frac{sC_F R_B}{sC_F(R_F + R_B) + 1}$$

$$T_B = \frac{2\pi f_B}{s + 2\pi f_B} \frac{sC_F R_F + 1}{sC_F(R_F + R_B) + 1}.$$

As the *dv/dt* feedback H_R plays an important in stabilising the system, no simplications on the transfer function has been made. From Fig.1, the buffer is actually a line diver, i.e. voltage follower. It can also be modelled as a low-pass filter as well.

By putting all these transfer function into the close-loop system transfer fucntion, it can be obtained that:

$$
\begin{aligned}
k_8 &= C_F(R_F + R_B)h_7 \\
k_7 &= h_7 + C_F(R_F + R_B)h_6 \\
k_6 &= h_6 + C_F(R_F + R_B)h_5 \\
k_5 &= h_5 + C_F(R_F + R_B)h_4 \\
k_4 &= h_4 + C_F(R_F + R_B)h_3 \\
k_3 &= h_3 + C_F(R_F + R_B)h_2 \\
k_2 &= h_2 + C_F(R_F + R_B)h_1 \\
k_1 &= h_1 + C_F(R_F + R_B)h_0 \\
k_0 &= h_0
\end{aligned}
$$

$$
\begin{aligned}
y_7 &= -2\pi f_B C_F R_B x_6 \\
y_6 &= -2\pi f_B C_F R_B x_5 \\
y_5 &= -2\pi f_B C_F R_B x_4 \\
y_4 &= -2\pi f_B C_F R_B x_3 \\
y_3 &= -2\pi f_B C_F R_B x_2 \\
y_2 &= -2\pi f_B C_F R_B x_1 \\
y_1 &= -2\pi f_B C_F R_B x_0 \\
y_0 &= 0
\end{aligned}
$$

$$
\begin{aligned}
v_6 &= 4\pi^2 f_{OP2} f_B A_{OP2} C_F R_F z_5 \\
v_5 &= 4\pi^2 f_{OP2} f_B A_{OP2} [C_F R_F z_4 + z_5] \\
v_4 &= 4\pi^2 f_{OP2} f_B A_{OP2} [C_F R_F z_3 + z_4] \\
v_3 &= 4\pi^2 f_{OP2} f_B A_{OP2} [C_F R_F z_2 + z_3] \\
v_2 &= 4\pi^2 f_{OP2} f_B A_{OP2} [C_F R_F z_1 + z_2] \\
v_1 &= 4\pi^2 f_{OP2} f_B A_{OP2} [C_F R_F z_0 + z_1] \\
v_0 &= 4\pi^2 f_{OP2} f_B A_{OP2} z_0
\end{aligned}
$$

$$
\begin{aligned}
u_4 &= -16\alpha\pi^4 A_{OP1} A_{OP2} f_{OP1} f_{OP2} f_B f_{FB} C_F R_F a_3 \\
u_3 &= -16\alpha\pi^4 A_{OP1} A_{OP2} f_{OP1} f_{OP2} f_B f_{FB} [C_F R_F a_2 + a_3] \\
u_2 &= -16\alpha\pi^4 A_{OP1} A_{OP2} f_{OP1} f_{OP2} f_B f_{FB} [C_F R_F a_1 + a_2] \\
u_1 &= -16\alpha\pi^4 A_{OP1} A_{OP2} f_{OP1} f_{OP2} f_B f_{FB} [C_F R_F a_0 + a_1] \\
u_0 &= -16\alpha\pi^4 A_{OP1} A_{OP2} f_{OP1} f_{OP2} f_B f_{FB} a_0
\end{aligned}
$$

.

The parameters can be further expressed as follows:

$$
\begin{aligned}
h_7 &= b_3 \\
h_6 &= [2\pi(f_{OP1} + f_{OP2} + f_{FB} + f_B)b_3 + b_2] \\
h_5 &= [(4\pi^2 f_{OP1} f_{OP2} + 4\pi^2 f_{FB} f_B + 4\pi^2 (f_{FB} + f_B)(f_{OP1} + f_{OP2}))b_3 \\
&\quad +2\pi(f_{OP1} + f_{OP2} + f_{FB} + f_B)b_2 + b_1] \\
h_4 &= [(8\pi^3 f_{FB} f_B (f_{OP1} + f_{OP2}) + 8\pi^3 f_{OP1} f_{OP2} (f_{FB} + f_B))b_3 \\
&\quad +(4\pi^2 f_{OP1} f_{OP2} + 4\pi^2 f_{FB} f_B + 4\pi^2 (f_{FB} + f_B)(f_{OP1} + f_{OP2}))b_2 \\
&\quad +2\pi(f_{OP1} + f_{OP2} + f_{FB} + f_B)b_1 + b_0] \\
h_3 &= [16\pi^4 f_{OP1} f_{OP2} f_{FB} f_B b_3 + (8\pi^3 f_{FB} f_B (f_{OP1} + f_{OP2}) + 8\pi^3 f_{OP1} f_{OP2} (f_{FB} + f_B))b_2 \\
&\quad +(4\pi^2 f_{OP1} f_{OP2} + 4\pi^2 f_{FB} f_B + 4\pi^2 (f_{FB} + f_B)(f_{OP1} + f_{OP2}))b_1 \\
&\quad +2\pi(f_{OP1} + f_{OP2} + f_{FB} + f_B)b_0] \\
h_2 &= [16\pi^4 f_{OP1} f_{OP2} f_{FB} f_B b_2 + (8\pi^3 f_{FB} f_B (f_{OP1} + f_{OP2}) + 8\pi^3 f_{OP1} f_{OP2} (f_{FB} + f_B))b_1 \\
&\quad +(4\pi^2 f_{OP1} f_{OP2} + 4\pi^2 f_{FB} f_B + 4\pi^2 (f_{FB} + f_B)(f_{OP1} + f_{OP2}))b_0] \\
h_1 &= [16\pi^4 f_{OP1} f_{OP2} f_{FB} f_B b_1 + (8\pi^3 f_{FB} f_B (f_{OP1} + f_{OP2}) + 8\pi^3 f_{OP1} f_{OP2} (f_{FB} + f_B))b_0] \\
h_0 &= 16\pi^4 f_{OP1} f_{OP2} f_{FB} f_B b_0
\end{aligned}
$$

$$
\begin{aligned}
z_5 &= b_3 \\
z_4 &= [2\pi(f_{OP1} + f_{FB})b_3 + b_2] \\
z_3 &= [4\pi^2 f_{OP1} f_{FB} b_3 + 2\pi(f_{OP1} + f_{FB})b_2 + b_1] \\
z_2 &= [4\pi^2 f_{OP1} f_{FB} b_2 + 2\pi(f_{OP1} + f_{FB})b_1 + b_0] \\
z_1 &= [4\pi^2 f_{OP1} f_{FB} b_1 + 2\pi(f_{OP1} + f_{FB})b_0] \\
z_0 &= 4\pi^2 f_{OP1} f_{FB} b_0
\end{aligned}
$$

$$
\begin{aligned}
x_6 &= a_3 \\
x_5 &= [2\pi(f_{OP1}+f_{OP2})a_3 + a_2 + 2\pi f_{FB}a_3] \\
x_4 &= [4\pi^2 f_{OP1}f_{OP2}a_3 + 2\pi(f_{OP1}+f_{OP2})a_2 + a_1 \\
&\quad +4\pi^2 f_{FB}(f_{OP1}+f_{OP2})a_3 + 2\pi f_{FB}a_2] \\
x_3 &= [4\pi^2 f_{OP1}f_{OP2}a_2 + 2\pi(f_{OP1}+f_{OP2})a_1 + a_0 \\
&\quad +(8\pi^3 f_{FB}f_{OP1}f_{OP2}a_3 + 4\pi^2 f_{FB}(f_{OP1}+f_{OP2})a_2 + 2\pi f_{FB}a_1)] \\
x_2 &= [4\pi^2 f_{OP1}f_{OP2}a_1 + 2\pi(f_{OP1}+f_{OP2})a_0 \\
&\quad +(8\pi^3 f_{FB}f_{OP1}f_{OP2}a_2 + 4\pi^2 f_{FB}(f_{OP1}+f_{OP2})a_1 + 2\pi f_{FB}a_0)] \\
x_1 &= [4\pi^2 f_{OP1}f_{OP2}a_0 \\
&\quad +8\pi^3 f_{OP1}f_{OP2}f_{FB}a_1 + 4\pi^2 f_{FB}(f_{OP1}+f_{OP2})a_0] \\
x_0 &= 8\pi^3 f_{OP1}f_{OP2}f_{FB}a_0
\end{aligned}
$$

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REFERENCES

[1] Palmer, P.R.; Rajamani, H.S.; , "Active Voltage control of IGBTs for high power applications," Power Electronics, IEEE Transactions on , vol.19, no.4, pp. 894, 901, Jul. 2004.

[2] Bryant, A.T.; Yalan Wang; Finney, S.J.; Tee Chong Lim; Palmer, P.R., "Numerical Optimization of an Active Voltage Controller for High-Power IGBT Converters," Power Electronics, IEEE Transactions on , vol.22, no.2, pp.374,383, Mar. 2007.

[3] Yang, Xin; Palmer, Patrick R., "Optimised IGBT turn-off under active voltage control in PEBB applications," Power Electronics and Applications (EPE), 2013 15th European Conference on , vol., no., pp.1,10, 2-6 Sep. 2013.

[4] Y. Wang, P. R. Palmer, A. T. Bryant, S. J. Finney, M. S. Abu-Khaizaran,and G. Li, "An analysis of high-power IGBT switching under cascadeactive voltage control," Industry Applications,IEEE Transactions on, vol. 45, no.2, pp. 861,870, Mar./Apr. 2009.

[5] Palmer, P.R.; Wang, Y.; Abu-Khaizaran, M.; Finney, S., "Design of the active voltage controller for series IGBTs," Power Electronics Specialists Conference (PESC), 2004 IEEE 35th Annual , vol.4, no., pp.3248,3254 , 2004.

[6] Lim, T.C.; Williams, B.W.; Finney, S.J.; Palmer, P.R., "Series-Connected IGBTs Using Active Voltage Control Technique," Power Electronics, IEEE Transactions on , vol.28, no.8, pp.4083,4103, Aug. 2013.

[7] A. Bryant, X. Kang, E. Santi, P. Palmer, and J. Hudgins, "Two-step parameter extraction procedure with formal optimization for physics-based circuit simulator IGBT and PIN diode models," Power Electronics, IEEE Transactions on, vol.21, no.2, pp. 295,309, Mar. 2006.

[8] Lobsiger, Y.; Kolar, J.W., "Stability and robustness analysis of d/dt-closed-loop IGBT gate drive," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.2682,2689, 17-21 Mar. 2013.

[9] Lobsiger, Yanick; Kolar, Johann W.; , "Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control," Energy Conversion Congress and Exposition (ECCE), 2012 IEEE , vol., no., pp.4754,4761, 15-20 Sep. 2012.

[10] Wittig, B.; Fuchs, F.W., "Analysis and Comparison of Turn-off Active Gate Control Methods for Low-Voltage Power MOSFETs With High Current Ratings," Power Electronics, IEEE Transactions on , vol.27, no.3, pp.1632,1640, Mar. 2012.

[11] Lihua Chen; Baoming Ge; Peng, F.Z., "Modeling and analysis of closed-loop gate drive," Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE , vol., no., pp.1124,1130, 21-25 Feb. 2010.

[12] Grbovic, P.J., "An IGBT Gate Driver for Feed-Forward Control of Turn-on Losses and Reverse Recovery Current," Power Electronics, IEEE Transactions on , vol.23, no.2, pp.643,652, Mar. 2008.

[13] N. Idir, R. Bausiere, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," Power Electronics, IEEE Transactions on , vol.21, no.4, pp. 849,855, Jul. 2006.

[14] Bryant, A.; Shaoyong Yang; Mawby, P.; Dawei Xiang; Li Ran; Tavner, P.; Palmer, P.; , "Investigation Into IGBT dV/dt During Turn-Off and Its Temperature Dependence," Power Electronics, IEEE Transactions on , vol.26, no.10, pp.3019,3031, Oct. 2011.

[15] P.R. Palmer, P.Y. Eng, J.C. Joyce, J. Hudgins, E. Santi and R.Dougal, "Circuit simulator models for the diode and IGBT with full temperature dependent features", Power Electronics, IEEE Transactions on, vol.18, no.5, pp. 1220,1229, Sep. 2003.

[16] B. J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWS-Kent, 1996.

[17] Routh, E. J. , *A Treatise on the Stability of a Given State of Motion: Particularly Steady Motion*: Macmillan and co. 1877.

[18] V. L. Kharitonov, *Asymptotic stability of an equilibrium position of a family of systems of differential equations*: Differentsialnye uravneniya, 1978. (Russian).

[19] Xin Yang; Xueqiang Zhang; Jin Zhang; Palmer, P.R., "Predictive optimisation of high-power IGBT switching under Active Voltage Control," Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE , vol., no., pp.1169,1174, 10-13 Nov. 2013.

[20] Xin Yang; Palmer, P.R., "Shaping pulse transitions by active voltage control for reduced EMI generation," *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE* , vol., no., pp.1682,1687, 15-19 Sept. 2013.

[21] Tominaga, S.; Urushibata, H.; Fujita, H.; Akagi, H.; Horiguchi, T.; Kinouchi, S.; Oi, T., "Modeling of IGBTs with focus on voltage dependency of terminal capacitances," Power Electronics and Applications (EPE 2011), Proceedings of the 14th European Conference on , vol., no., pp.1,9, Aug. 30-Sep. 1 2011.

[22]