THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Medium Voltage Generation System with Five-level NPC Converters for Kite Tidal Power

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To my family and friends

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Abstract

Offshore power generation has emerged as a prominent source of energy and the installed capacity of new plants has been steadily increasing in recent years. Tidal power specifically is a promising renewable energy source which has not been highly exploited yet, despite its distinctive advantages of being predictable and independent of weather conditions. The main objective of this Licentiate thesis is to analyze and propose solutions for two common problems in offshore power production, which are the power variations due to the non-steady speed profile of the water speed flowing through the turbine and the efficient transportation of the produced power to the shore.

The tidal power application utilized in this thesis is the subsea kite, which is a recently developed tidal energy conversion technology that can increase the generated power compared to a traditional static tidal turbine. A turbine is mounted on a submerged kite and the kite moves inside the sea following a predefined trajectory and generating electric power from the tidal currents. The speed and torque of the turbine varies periodically due to the periodic movement of the kite in the sea and, therefore, the control of the generator needs to be able to handle this variable generated power. The kite studied in this thesis has rated active power of 500 kW.

In the first part of the thesis, the power generation system of the subsea kite is modelled and the profile of the generated power is extracted given a specific tidal current and turbine geometry. The control of the power converters is described and tested for the specific profile of the generated power. The speed of the generator is controlled by a properly designed Maximum Power Point Tracking algorithm, which ensures that the generator extracts the maximum power from the tidal stream. Experimental verification of the model of this innovative system is also conducted on a laboratory 35 kVA emulator of the tidal power generator.

The second part of the thesis deals with the design of a medium voltage generator

drive. The use of medium voltage in the power generation system is highly advantageous for the tidal kite application, since it can reduce the current flowing through the undersea cables connecting the tidal plant to the local grid. Therefore, the size of the cables can be reduced. The drive proposed here uses two 5-level Neutral Point Clamped (NPC) converters connected back-to-back. The 5-level NPC converters can operate with high voltage, while using multiple low-voltage-rated power switches. Contrarily, the typical 2-Level converters have limited voltage capability, since they would require more expensive high-voltage-rated power switches. The increased operating voltage of the power conversion system results to lower current and losses in the cables. Another advantage of the NPC converter is the low harmonics at the ac side, which reduces the requirements for passive grid filters. However, the voltage balancing of the dc-link capacitors in this converter topology is a challenge which has not been effectively solved in previous studies. Therefore, a novel voltage balancing strategy is proposed here that uses advanced Space-Vector-Modulation techniques and hardware-based voltage balancing schemes with reduced number of components and lower power losses. Finally, a laboratory prototype of the NPC-converter-based power conversion system is developed with rated power 50 kVA. SiC MOSFETs are used on the converters to further increase the system's efficiency and voltage capability.

This thesis presents the model, control and laboratory emulator of a kite-based tidal power generator. The experimental set-up can be utilized for conducting research on other renewable sources, such as wind power, that have similar performance. Also, the developed multilevel drive is suitable for various applications where medium voltage grid-connected drives are used and particularly in distributed renewable power generation.

Index Terms: Maximum Power Point Tracking (MPPT), Medium Voltage Converters, Multilevel Space-Vector-Modulation, Neutral point clamped converter (NPC), Subsea kite, Tidal power, Voltage balancing.

Acknowledgements

Firstly, I would like to express my gratitude to my supervisor Prof. Yujing Liu for his guidance and support throughout the course of this project. Thank you very much for believing in my ideas and encouraging me to investigate the areas that I enjoyed mostly and at the same time for providing me with comments that helped me to improve myself as a person and as a future researcher. I thank also my examiner Prof. Ola Carlson for his feedback on my thesis and on the planning of my PhD studies.

I would also like to thank Assoc. Prof. Peiyuan Chen for the excellent collaboration that we had during most of my experimental work on this project. My gratitude goes also to my co-supervisor Dr. Stefan Lundberg and to Robert Karlsson for their great assistance in solving any major problems that I faced in the prototyping of the laboratory set-up. I would like to mention that I am thankful for the contribution of Dr. Nima Saadat during the initial phase of the project.

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Γεώργιος Μαδεμλής / Georgios Mademlis
Gothenburg, Sweden
March, 2019

List of Acronyms

2LC	2-level Converter
ADC	Analog-to-Digital Converter
ANPC	Active Neutral Point Clamped
B2B	Back-to-Back
DTC	Direct Torque Control
EMF	Electromotive Force
EMI	Electromagnetic Interference
ePWM	enhanced Pulse Width Modulator
FFT	Fast Fourier Transform
FC	Flying Capacitor
FOC	Field Oriented Control
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IGBT	Insulated-gate bipolar transistor
IM	Induction Motor
LPF	Low-Pass-Filter
L2L	Line-to-line
MCU	Microcontroller Unit
MMC	Modular-Multilevel-Converter
MOSFET	Metal oxide semiconductor field effect transistor
MPPT	Maximum Power Point Tracking
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
POC	Point of Common Coupling
PI	Proportional-plus-Integral

PLL	Phase-Locked Loop
PMSG	Permanent Magnet Synchronous Generator
pu	Per Unit
PWM	Pulse-Width Modulation
RES	Renewable Energy Sources
rms	Root mean square
rpm	revolutions per minute
SG	Synchronous Generator
SMD	Surface-mount device
STATCOM	Static synchronous Compensator
SPWM	Sinusoidal Pulse-Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
TSR	Tip Speed Ratio
TUSK	Tethered UnderSea Kite
VSC	Voltage Source Converter

List of Symbols

Each variable symbol has *italic* font and is defined in the text where it is first mentioned. The basic variables of the thesis defined below are sorted alphabetically:

*	reference signal
$\dot{\gamma}$	angular velocity matrix of the kite
θ	voltage angle
τ	time constant [s]
ω_{gen}	rotor speed of the generator [rad/s]
ω_{turb}	turbine rotational speed [rad/s]
a_c	generator current controller bandwidth [rad/s]
a_ω	generator speed controller bandwidth [rad/s]
a_{cs}	grid current controller bandwidth [rad/s]
a_{PLL}	grid PLL bandwidth [rad/s]
a_{DClink}	grid dc-link controller bandwidth [rad/s]
B_a	active damping term
C_P	performance coefficient [%]
D	altitude angle [°]
d_T	duty cycle of the power switch T
f_{sw}	switching frequency [Hz]
i	trajectory position of the kite
i_{bl}	ac current used for voltage balancing [A]
I_{d1} ... I_{d5}	dc currents at the clamping points of a 5-level NPC converter
I_{gen}	generator stator current [V]
I_s	grid current [V]
J	moment of inertia [kg·m^2]
K_I	integral gain
K_P	proportional gain
L_d	stator inductance in the d-axis [H]

L_f	Grid filter inductance [H]
L_q	stator inductance in the q-axis [H]
L_1 ... L_3	Balancing converter inductance [H]
$\hat{m}$	modulation index [%]
N	number of levels of the phase voltage of a VSC
n_{gen}	rotor speed of the generator [rpm]
P	number of machine's pole pairs
$\vec{P}(x, y, z)$	parametric equation of the Viviani's Curve in space coordinates
P_{loss_i}	power losses at the trajectory point i owed to the drag of the kite [W]
P_m	turbine mechanical power [W]
P_{grid}	active power at the PCC [W]
PRT	error signal of the overcurrent/overvoltage detection board [V]
Q_{grid}	reactive power at the PCC [W]
r	cylinder radium of the Viviani's Curve [m]
R	sphere radium of the Viviani's Curve [m]
R_S	stator resistance [Ω]
R_T	turbine radius [m]
t	time [s]
T_{grid}	electrical torque at the PCC [Nm]
T_m	turbine mechanical torque [Nm]
t_r	rise time [s]
T_{sw}	switching period [s]
t_D ... t_G	dwell times of the switching states in the SVM
v^*	normalized reference voltage of a VSC
V_a	effective water speed [m/s]
V_{C1} ... V_{C4}	dc capacitor voltages of a 5-level NPC converter
V_{CC}	supply voltage for electronic circuits [V]
V_{dc}	voltage of each dc-link capacitor bank [V]
$V_{dc\ tot}$	total dc-link voltage of a drive [V]
V_D ... V_G	space vectors of the SVM in (α', β') coordinates
V'_D ... V'_G	three-phase switching vectors of the SVM
V_{gen}	generator terminal voltage [V]
V_{GS}	MOSFET gate-source voltage [V]
V_s	grid voltage [V]
V_{tide}	tidal free stream speed [m/s]
V_{tr}	voltage of the triangular carrier in SPWM
$\hat{V}^*_{ph}$	reference converter phase voltage [V]

Contents

Chapter 1

Introduction

1.1 Background and Motivation

Kite-based Tidal Power Generation System

Offshore power plants producing energy from the sea tides have attracted significant research interest in the recent years, since this can be a renewable energy source with large potential [1–4] and an alternative to the wind and solar energy sources. Especially the United Kingdom and France cover almost 90% of the European tidal resource with 48GW of power, when considering the available tidal generation technology, as reported in [1,2]. Tidal energy has considerable advantages compared to the other renewable energy sources, such as the fully predictable nature of the tidal movements and its robustness against climatic changes, such as the wind, rain, snow, clouds and fog [5].

Up to now, tidal power has been largely unexploited, although attempts to harness the energy of the sea tides date back from 1966, when the oldest application was installed in France [6]. Most of the traditional tidal power plants required the construction of large dams and static undersea constructions, which had a large investment cost as well as a high environmental impact for the local communities, and this hindered further development of tidal power projects in large scale. An emerging hydrokinetic energy technology named "Tethered UnderSea Kite" (TUSK) proposes a new more efficient way to produce electrical energy from the sea tides using axial-flow water turbines mounted on a kite which can move freely

inside the sea following the motions of the sea currents [7]. This type of technology can increase the power production of a specific tidal turbine, when compared to a traditional static tidal turbines of the same size. Therefore, the potential resources of tidal power can be increased by using the TUSK-based systems. Also, the environmental impact of the plant's installation is limited. A recent application of the TUSK system is the Deep Green [8, 9] concept which has been developed by Minesto AB and is under development in various projects, such as the PowerKite project [10]. The undersea kites can be installed either standalone or they can build arrays, as shown in Fig. 1.1.

The concept of using a moving kite for producing power has initially been proposed for airborne systems that would increase the power density of existing wind power turbines, as cited in [11–16]. As described there, the turbine is mounted on the kite, which is attached to the ground through a tether. While the kite is travelling on the air (in the case of airborne kites) or in the sea (for the undersea kites) following a predefined trajectory, the relative speed of the air or water flowing through the turbine becomes higher compared to a traditional static turbine. The kite is moving fast following a trajectory that resembles to the "∞" symbol. Since the power generated from the turbine is proportional to the third-power of the relative wind/water speed, the electric power produced by the generator is highly increased, as well, increasing also the power density of the whole power generation system.

The increase of the power density is a distinctive advantage for TUSK systems compared to fixed marine turbine technologies [7] and this is one of the character-

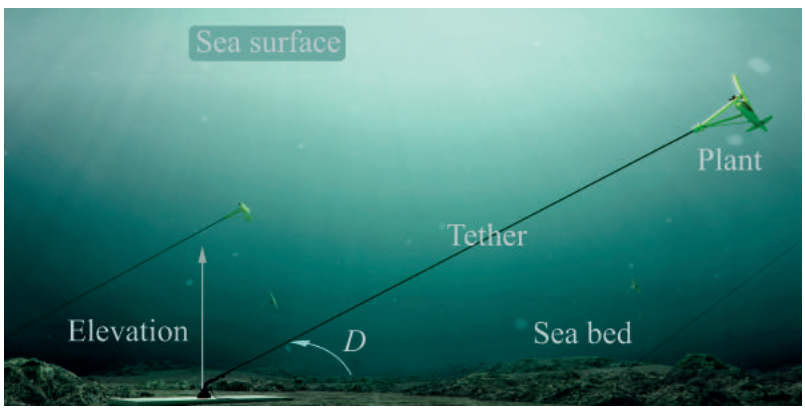


Fig. 1.1: TUSK plant schematic into the sea showing the tether connecting the kite to the sea bed [Property of Minesto AB]

istics that would make tidal power competitive against other renewable energy sources. Additionally, the increased relative speed of the fluid flowing through the plant's turbine, allows TUSK-based tidal plants to operate at places with medium or low tidal streams, which may not be cost-effective using the traditional fixed tidal turbines that require high-speed tidal streams [8].

The TUSK-based plants, however, have some special requirements for the design and control of the power generation subsystem, which are going to be further analyzed in this thesis. Firstly, the speed of water flowing through the kite's turbine experiences fluctuations which depend on the trajectory of the TUSK in the sea. These speed fluctuations are periodic and cause variations in the output electrical torque of the plant's generator and of the produced power at the grid side of the system [17]. The speed and power variations can be estimated using analytical calculations, if the trajectory of the kite is known. A special design of the controllers for the power conversion system should be made in order to ensure stability under this highly dynamic operation. Verifying the effectiveness of the power converters' control in laboratory conditions is necessary and, therefore, a laboratory emulator of the kite's power generation system is needed which will represent the dynamics of the kite's tidal turbine. Laboratory emulators of wind power systems have been presented in [18–22], where the wind turbine has been emulated by a motor and the control of the real wind power generator has been tested. A similar experimental set-up can be used to emulate the operation of the TUSK-based tidal generator.

The Maximum Power Point Tracking (MPPT) algorithm of the kite's tidal generator is another topic that has not been investigated. MPPT strategies used in wind power plants can be applied also in the tidal power generation [23–27], since the operational conditions are similar. However, due to the highly dynamic operation of the kite and the constantly variating flow speed of the water through its turbine, these methods should be compared and their effectiveness should be evaluated experimentally. The turbine inertia is also a factor that can influence the effectiveness of the MPPT control of the kite's generator. The inertia of the system will create a error between the actual rotational speed of the generator and the reference speed which is calculated by the MPPT control. Therefore, improvements should be proposed to properly adjust the generator speed control for the specific needs of the examined application.

Medium Voltage Multilevel Generator Drives

An additional constraint of the TUSK systems is the limited available space inside the nacelle of the kite for the generator and the power converters which makes the design of the power conversion system a challenging task. Therefore, power equipment of high power density is a requirement for this application. Also, the tether of the kite provides both mechanical coupling of the system with the sea bed and electrical connection to the grid. The weight and diameter of the electrical cables inside the tether should be kept as low as possible in order to reduce the drag that the tether creates while the kite is moving inside the sea. This makes the efficient transportation of the produced active power from the kite to the grid challenging, since the power of the system is high.

Increasing the operating voltage of the kite's power generation system can increase the efficiency of the power transportation though the subsea cables, since this results to reduced current and ohmic losses. The 2-level converters (2LC) can still be used in medium voltage applications by having high-voltage semiconductors or multiple series-connected low-voltage power switches in each switch position. However, problems with the voltage balancing of these switches during the switching transient are the main disadvantages of this solution [28, 29]. Therefore, the use of multilevel VSCs is a preferable solution for this case.

The main advantage of multilevel converters is the possibility to utilize power semiconductors of low voltage ratings which have lower cost and are more easily available [30, 31]. Another important advantage is the reduction of the harmonic distortion at the point of common coupling (PCC) of the kite, which eliminates the need for large passive filters at the grid-side of the system [30] that contribute a lot to the total weight and size of the drive mounted inside the kite. An improvement of the converter's efficiency has also been reported in [32] when using multilevel converters compared to 2LC of the same operating voltage and power. Multilevel converters can also reduce the voltage stress of the power switches dv/dt during the switching transients of the converters, as stated in [33], which decreases drastically the EMI and voltage oscillations produced by the converters.

The available multilevel topologies need to be compared in order to select the most suitable converter for the power conversion system of the undersea kite. A comparative study based on literature review for multilevel converters suitable for drive applications is made in Section 3.2 of the thesis where the 5-level Neutral Point Clamped (NPC) converter is finally chosen. The 5-level NPC converter can increase the operating voltage of the drive system up to 4 kV (peak), in case power

switches with voltage rating of 1.2 kV are used. The 5-level converter has four series-connected capacitor banks at the dc side and a well known problem of this topology is the imbalance of the individual capacitor voltages. This imbalance would create overvoltage in some of the power switches of the converter and low frequency harmonics at the ac side of the system. Special control and/or hardware is required to balance the capacitor voltages, which may increase the complexity and cost of the system. Thus, several methods have been proposed to alleviate this drawback and they can be divided into two types, the software and the hardware based techniques.

The software-based balancing method is based on the modification of the standard space vector modulator of the NPC converter, as suggested in [34–42]. However, most of the solutions proposed in these studies require some limitations in the operation of the drive, such as the difficulty to operate under unity power factor, which is usually the preferred operation mode for the grid-side converter of the drive. Some studies propose also the operation of the 5-level converter in a 3-level mode only in order to avoid specific switching combinations that create unbalances of the dc-link voltages. However, this method would increase the harmonics at the ac side of the NPC converters and the need for grid filters and this characteristic is not preferable in a generator drive, such as the one designed for the TUSK where the available space for the drive is limited.

Another option for balancing the capacitor voltages of the dc-link is by employing dc/dc converters that can actively distribute the voltage across the four series-connected capacitors, as proposed in [43–48]. This technique has several advantages; however, the cost and the losses of the extra power devices for the dc/dc converters is a serious drawback. From the above it is concluded that further investigation should be made to develop a new technique of the capacitor voltage balancing in a drive with 5-level NPC converters without the previously mentioned disadvantages.

1.2 Aim of the Thesis

The aim of the work presented in this thesis is the development of the power generation subsystem in a TUSK-based power plant. The control of the power converters of the generator drive should be designed considering the highly dynamic operation of the kite due to the periodic variations in the active power and rotor speed.

An additional goal of this thesis is to propose techniques for increasing the

operational voltage of the power conversion system in order to reduce the current at the output of the kite and increase the power density of the power equipment. Multilevel power converter topologies are needed in order to meet the voltage requirements of this application and reduce the need for passive filters at the grid-side of the drive. The 5-level NPC converter is selected as a suitable converter for this project; however, the issue of the dc-link voltage balancing in this converter needs to be solved by developing suitable voltage balancing control techniques.

1.3 Contributions

The key contributions of the thesis can be identified as follows:

- Modelling of TUSK power generation: The power generation of a novel TUSK plant has been described with analytical calculations showing how the periodic trajectory of the kite inside the sea can affect the power extracted by the tidal turbine. A properly designed MPPT controller for the generator is implemented highlighting the key factors that should be considered when designing such a system. The effectiveness of the developed controllers has been experimentally verified on a laboratory set-up where the operation of the turbine is emulated by an induction motor (IM).

  The laboratory emulator can be further utilized in future research projects to emulate the operation of other renewable energy sources, like wind power which uses power conversion system with similar structure [49].

- Development of a prototype medium voltage drive: A generator drive with 5-level NPC converters has been developed, which is used for the first time as the power conversion system of a TUSK plant. A laboratory prototype of the generator drive with maximum designed dc voltage up to 4 kV has been firstly simulated and then designed and built during this project. The system is tested experimentally with dc-link voltage up to 670 V.

  The power converter PCBs, measurement devices and control platforms of the prototype system are specially designed to have low EMI and ringing on the power switches. Also, the use of SiC MOSFETs and diodes in the converters allows the further increase of the operating voltage while keeping the switching losses low. Suitable gate driver boards for the SiC MOSFETs have been designed, which utilize fiber optic cables for the communication with the microcontrollers in order to achieve high voltage insulation and low

EMI on the control signals. An advanced overvoltage/overcurrent hardware protection scheme of the prototype with multiple layers of protection has been developed for keeping the converters safe in case of faults.

- DC-link Voltage balancing algorithms: The challenging problem of balancing the capacitor voltages in the dc-link of a generator drive with 5-level NPC converters has been solved in this thesis by proposing three new voltage balancing techniques. A control method of the voltages that utilize the redundant states of a modified Space Vector Modulation (SVM) is shown, as well as hardware-based balancing techniques. The capacitor voltages are verified to remain balanced under every operating condition in both of the proposed control techniques. A combined SVM-based and hardware-controlled voltage balancing technique is also developed in order to reduce the number of components and the losses introduced by the additional balancing converter, minimizing the cost of the system.

  The use of the developed NPC-based generator drive can be extended into further medium voltage grid-connected drives, such as distributed wind power generation and various other offshore generator or motor drives.

1.4 Thesis Outline

The thesis is organized into six chapters:

- Chapter 1 is the introduction and describes the motivation, the aim and the main contributions of this study.
- In Chapter 2 an overview of the background application of this project, the TUSK tidal generator, is presented. The modelling procedure of the tidal power system and the design of the control structure for both converters of the drive are described. Experimental results from the tidal power emulator are also shown.
- Chapter 3 starts with an analysis of the most well-known multilevel converter topologies for drive applications. Modulation strategies for N-level multilevel converters are later presented.
- Capacitor voltage balancing methods using modified Space Vector Modulation and dc/dc converters are presented in Chapter 4. A literature review of the available balancing techniques is provided in Section 4.2 and the new control schemes are described. The theoretical analysis of the proposed

control techniques is supported with simulation results.

- Experimental verification of some of these control techniques is made in Chapter 5, where the design process of a medium voltage prototype multilevel drive is given.
- The conclusions of the thesis and plans for future work are included in Chapter 6 of the thesis.

1.5 List of Publications

The publications originating from this thesis are:

I. **G. Mademlis**, Y. Liu, and N. Saadat, "Combined voltage balancing techniques of the DC link in five-level medium voltage NPC back-to-back converters for offshore renewable generation", in *Proc. 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017.

II. **G. Mademlis**, Y. Liu, and J. Zhao, "Comparative Study of the Torque Ripple and Iron Losses of a Permanent Magnet Synchronous Generator Driven by Multilevel Converters", in *Proc. 23rd International Conference on Electrical Machines (ICEM)*, September 3-6, 2018.

III. **G. Mademlis**, Y. Liu, P. Chen, and E. Singhroy, "Generator Speed Control and Experimental Verification of Tidal Undersea Kite Systems", in *Proc. 23rd International Conference on Electrical Machines (ICEM)*, September 3-6, 2018.

IV. **G. Mademlis** and Y. Liu, "DC Link Voltage Balancing Technique Utilizing Space Vector Control in SiC-based Five-Level Back-to-Back-Connected NPC Converters", in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, September 23-27, 2018.

V. **G. Mademlis** and Y. Liu, "Feed-forward Control of Active Voltage Balancing Converter in Electric Drive with Five-Level NPC Converters", in *Proc. of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, September 23-27, 2018.

VI. C. Larsson, A. Rydgård, **G. Mademlis**, Y. Liu, and M. Fredriksson, "Overvoltage Mitigation of Medium Voltage Electric Drives with Long Cables using Multilevel-Converters and Passive Filters", to be presented in *the 21st European Conference on Power Electronics and Applications (EPE'19 ECCE*

Europe), 2019.

VII. **G. Mademlis**, Y. Liu, P. Chen, and E. Singhroy, "Design of Maximum Power Point Tracking for Dynamic Power Response of Tidal Undersea Kite Systems", submitted to *IEEE Trans. Industry Applications*, May 2019.

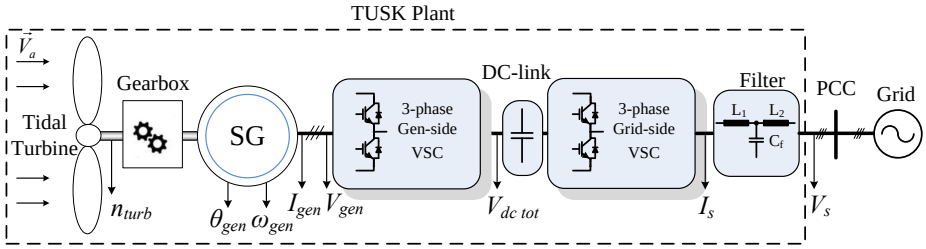
Chapter 2

Modelling and Control of Kite-based Tidal Power Generator Systems

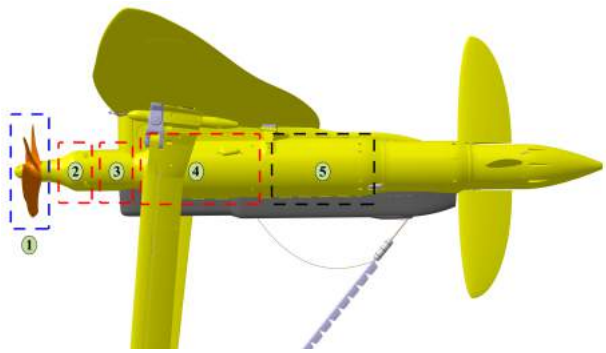
2.1 Introduction to Control Techniques of the Kite

The power conversion system of the kite is mounted inside the nacelle and consists of a generator, two B2B connected VSCs and a passive LCL filter at the point of connection to the grid. A synchronous generator (SG) has been used for the purpose of this study. A block diagram of the kite can be seen in Fig. 2.1(a). The MPPT algorithm of the TUSK is an essential part of the generator control system. The speed of the water flowing though the turbine is constantly changing, because of the kite's crosscurrent motion into the sea. The optimum reference generator speed should be evaluated in order to extract the maximum electric power from the water.

The MPPT algorithms presented in [23, 24] have as input the calculated active power at the terminals of a permanent magnet synchronous generator (PMSG) and calculates the reference speed of the rotor which serves as input of the generator's speed controller. Loss minimization control of the generator can also be applied in parallel. Another type of MPPT algorithm is described in [25–27], which receives as input the measured rotational speed of the generator and generates the optimal reference electrical torque that the current controller of the machine needs to create. The speed of the rotor is controlled indirectly here, since the rotational speed and the mechanical torque of the rotor will settle down to an equilibrium with an optimal torque point, where the turbine operates at the maximum power



(a)



(b)

Fig. 2.1: (a) Block diagram of the power conversion subsystem in a TUSK tidal plant; (b) CAD-drawing of an early-concept kite for the DG500 project [53]: 1) tidal turbine, 2) gearbox, 3) generator, 4) power conversion subsystem and grid filters, 5) auxiliary equipment [Property of Minesto AB]

point. The speed control strategy of the kite's generator is designed in this chapter based on these two MPPT control schemes and their performance is compared experimentally.

The rotational inertia of the tidal power system may affect the accuracy of the applied MPPT control, since the generator speed controller gains are selected based on the inertia of the mechanical drivetrain. This characteristic has a positive influence at the wind turbine drives, where the wind fluctuations are stochastic and cannot be predicted. The large wind turbine inertia has been utilized to smooth out the power fluctuations caused by sudden changes of the wind speed [50, 51] or to filter the highly fluctuating power output of wave generators in [52].

The TUSK tidal system experiences also power fluctuations; however, contrarily to the wind and wave power plants these power fluctuations are periodic, highly predictable and dependent mainly on the predefined movement of the kite in the sea. It is possible to smooth out the power fluctuations of a TUSK farm by

combining the power output of multiple kites, as shown in the Master thesis of [17]. Therefore, it is not necessary anymore to utilize the turbine shaft inertia in order to limit these power variations of the individual kites and the maximum power should be extracted by the tidal generator at any time instant. The inertia of the TUSK turbine shaft will still affect the transient response of the generator speed controller, which could hinder it from following the optimal MPPT curve. A speed control strategy needs to be applied on the TUSK tidal power generator that has fast dynamic performance, so that the turbine of the kite can follow the MPPT curve with the least possible error. A further analysis of the shaft inertia influence is conducted at the experimental results of this chapter.

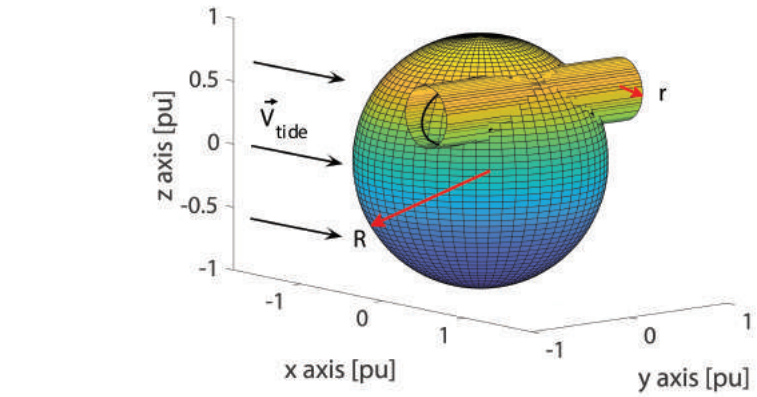
2.2 Tidal Power Plant System Modeling

The TUSK plant is controlled to undergo periodic movements into the water and the orbit is eight-shaped. Water flows through the turbine blades of the kite and creates a rotational torque that generates electric power at the output of the generator. The generator is attached to back-to-back-connected VSCs which control the generator speed and the synchronization to the grid at the electrical output of the topology. In order to calculate the produced electric power of the topology, a mathematical model of the kite's trajectory is needed.

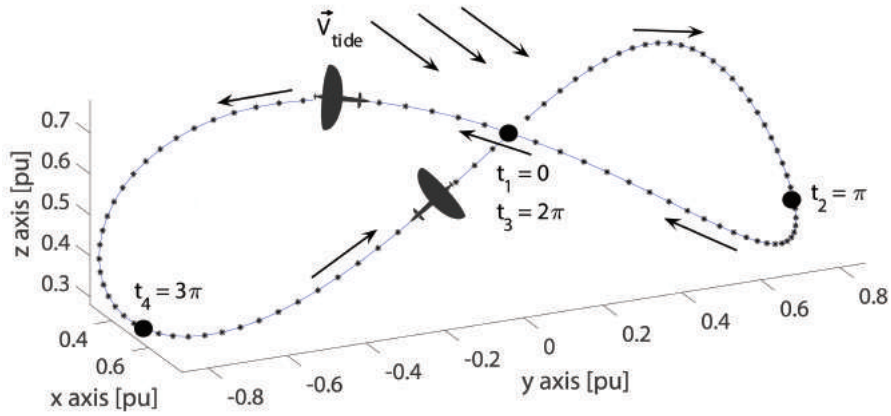
A detailed analysis of the kite's hydrodynamics can be found in the Master Thesis report in [17]. The model presented here is simplified and is utilized only for the modelling of the electrical installation and the control of the power conversion system. The exact geometry of the kite and its hydrodynamic performance have not been modelled and the kite's trajectory is considered to be unaffected by the operation of the electrical generator. Also, the kite is considered to follow its trajectory without error and the control mechanisms for that are not studied here.

2.2.1 Modeling of Kite's Trajectory and Power Generation

The three-dimensional depiction of the kite's trajectory can be mathematically described by the Viviani's Curve, which is defined as the intersection between a cylinder and a sphere, as shown in Fig. 2.2. The Viviani's curve offers the minimum curvature and maximizes power production compared to other trajectories, such as the circle. The parametric equation of the Viviani's Curve in the xyz-coordinate system is given by



(a)



(b)

Fig. 2.2: Three-dimensional drawing of (a) the Viviani's curve used as the trajectory of the kite and (b) the TUSK plant following its trajectory $\vec{P}_r$ with the arrows showing the direction of the kite's movement after applying the rotation matrix in (2.2)

$$\vec{P}\big(x(t), y(t), z(t)\big) = \left\{ \begin{array}{l} x(t) = (R - r) + r \cdot \cos(t) \\ y(t) = 2 \cdot \sqrt{(R - r) \cdot r} \cdot \sin(\frac{t}{2}) \\ z(t) = r \cdot \sin(t) \end{array} \right\} \tag{2.1}$$

where r is the cylinder radius, and R is the sphere radius. The parameter t varies from 0 to 4π and some characteristic values of t on the Viviani's curve can be seen in Fig. 2.2(b). The x-axis of the graph is in-line with the tidal current flow.

The TUSK plant is elevated from the sea floor. Also, the tether of the TUSK and the sea floor have an altitude angle D, as can be observed in Fig. 1.1. Therefore,

the position vector $\vec{P_r}$ can be rotated by multiplying with the following matrix

$$\vec{P_r} = \begin{bmatrix} \cos(D) & 0 & -\sin(D) \\ 0 & 1 & 1 \\ \sin(D) & 0 & \cos(D) \end{bmatrix} \cdot \vec{P} \tag{2.2}$$

The partial derivative vector of the rotated position vector $\vec{P_r}$ can be defined as

$$\frac{\partial \vec{P_r}}{\partial x \partial y \partial z} = \frac{\partial P_r}{\partial x}\vec{i} + \frac{\partial P_r}{\partial y}\vec{j} + \frac{\partial P_r}{\partial z}\vec{k} \tag{2.3}$$

The kite's trajectory is discretized into a definite number of points and each trajectory point is named with the variable i. The partial derivatives of the position vector are used to define the angular velocity matrix $\dot{\gamma_i}$, which describes the rate of change of the kite's pitch, roll and yaw on each point i of the trajectory

$$\dot{\gamma_i} = \begin{bmatrix} \Delta Pitch_i & \Delta Roll_i & \Delta Yaw_i \end{bmatrix} \tag{2.4}$$

A more detailed analysis of the mathematical movement equations can be found in [54].

The mechanical power extracted by the tidal turbine can be calculated as [51]

$$P_{m_i} = \frac{1}{2}\rho A_T C_p V_{a_i}^3 - P_{loss_i} \tag{2.5}$$

where $\rho = 1025\ \mathrm{kg/m^3}$ is the salt water density, C_P is the coefficient of performance of the turbine, $A_T = \pi R_T^2$ the swept area, R_T is the turbine radius and V_a the effective water speed flowing through the turbine in m/s. The last term P_{loss_i} describes the power losses at each trajectory point i owed to the motion of the kite and can be calculated by

$$P_{loss_i} = L_i \dot{\gamma_i} \tag{2.6}$$

where L_i is a torque coefficient matrix dependent on the kite geometry. The following coefficients have been used for the analysis of this study and have been empirically chosen

$$\dot{L_i} = \begin{bmatrix} 1500 & 2000 & 1000 \end{bmatrix} \tag{2.7}$$

The torque coefficients depend mainly on the design of the whole tidal kite system and the empirical choice of these parameters could introduce some error, which is not considered during this study. The tip speed ratio TSR_i of the tidal turbine at each trajectory point i is defined as

$$TSR_i = \frac{\omega_{turb_i} R_T}{V_{a_i}} \tag{2.8}$$

where ω_{turb_i} is the turbine rotational speed in rad/s. By using (2.5) and (2.8)

$$P_{m_i} = \frac{\rho C_P \pi R_T^5}{2 \cdot TSR_i^3} \omega_{turb_i}^3 - P_{loss_i} \tag{2.9}$$

The active power at the point of connection to the grid can also be expressed as follows

$$P_{grid_i} = \frac{\rho C_P \pi R_T^5}{2 \cdot TSR_i^3} \omega_{turb_i}^3 - P_{loss_i} - P_{e\,loss_i} \tag{2.10}$$

where $P_{e\,loss_i}$ is the power losses (mechanical and electrical) between the generator shaft and the connection to the grid. The turbine torque T_{m_i} and the electrical torque at the grid output of the kite T_{grid_i} are defined as

$$T_{m_i} = \frac{P_{m_i}}{\omega_{turb_i}} = \frac{\rho C_P \pi R_T^5}{2 \cdot TSR_i^3} \omega_{turb_i}^2 - \frac{P_{loss_i}}{\omega_{turb_i}} \tag{2.11}$$

$$T_{grid_i} = \frac{P_{grid_i}}{\omega_{turb_i}} = \frac{\rho C_P \pi R_T^5}{2 \cdot TSR_i^3} \omega_{turb_i}^2 - \frac{P_{loss_i}}{\omega_{turb_i}} - \frac{P_{e\,loss_i}}{\omega_{turb_i}} \tag{2.12}$$

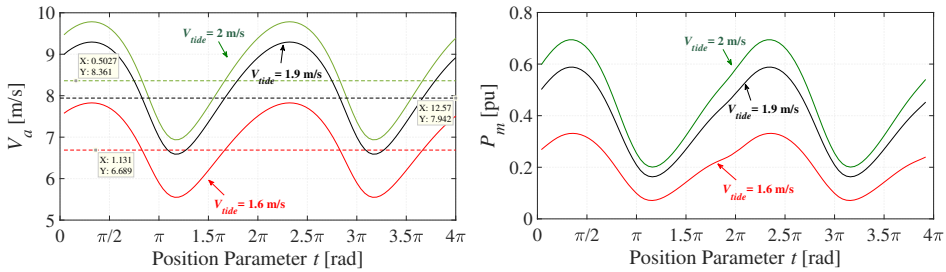
The effective water speed V_a depends on the lift and drag of the kite and varies within one trajectory period. The kite's speed is controlled with fixed angle of attack and variable angle of inclination, which provides the optimum performance, based on the analysis presented in Sections 5.13 and 5.16 of [17]. Therefore, the average value of the water speed V_a can be calculated as follows [11]

$$V_{a_{mean}} = \frac{2}{3} \frac{L}{D_k} V_{tide} \tag{2.13}$$

where L is the kite lift coefficient, D_k is the drag coefficient and V_{tide} is the free stream speed of the tide, which is considered unaffected by the operation of the kite. The V_{tide} varies based of the lunar cycle, as described in Section 2 of [17]. In case the kite's trajectory in the sea is controlled with fixed angle of attack and variable speed of inclination, the optimal lift to drag ratio is equal to $\frac{L}{D_k} = 6.512$, as stated in Fig. 36 of [17], and the water speed speed in (2.13) becomes

$$V_{a_{mean}} \overset{[17]}{=\!=} \frac{2}{3} \cdot 6.512 \cdot V_{tide} = 4.34 \cdot V_{tide} \tag{2.14}$$

The effective water speed V_a will vary periodically around its calculated mean value, since the kite is moving in some time instants with or against the tidal current, shown in Fig. 2.3(a). These water speed fluctuations create a variation of the extracted mechanical power, as well, since in (2.5) it can be seen that the mechanical power is a function of the water speed. Therefore, the turbine rotational speed ω_{turb} and shaft torque vary also periodically based on (2.10) and (2.12), when the turbine has constant TSR and C_P.



(a) (b)

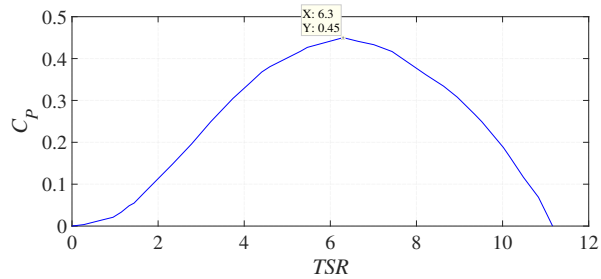
Fig. 2.3: (a) Effective water speed in m/s and (b) turbine power in pu for maximum C_P as a function of the kite's position on the Viviani's curve

Experimental measurements of the C_P and the TSR for the turbine used in the TUSK plant are not available. Therefore, the curve shown in Fig. 2.4(a) is used for the analysis of this chapter, which is referenced from [54–56] where marine current turbines are studied. When optimal $TSR_{opt} = 6.3$ and maximum $C_{Pmax} = 0.45$ are considered, the equations (2.10) and (2.12) are converted into

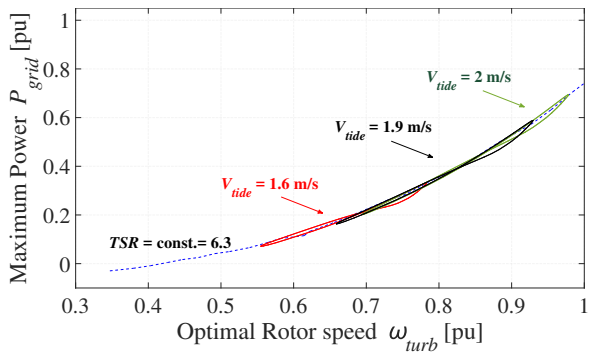
$$\begin{aligned} P_{grid\ max_i} &= k_1 \cdot \omega_{turb_i}^3 - P_{loss_i} - P_{e\,loss_i} \\ T_{grid\ max_i} &= k_2 \cdot \omega_{turb_i}^2 - \frac{P_{loss_i}}{\omega_{turb_i}} - \frac{P_{e\,loss_i}}{\omega_{turb_i}} \end{aligned} \tag{2.15}$$

The TUSK plant's design characteristics of Table 2.1 are used as base model for the power calculations of Fig. 2.3 and Fig. 2.4. A sample plant with 500 kW nominal turbine power has been chosen for the analysis of this section. Fig. 2.3(a) shows the fluctuation of V_a and Fig. 2.3(b) shows P_m during one period of the kite's motion for tidal stream speeds equal to 1.6 m/s, 1.9 m/s and 2 m/s. The dashed lines in Fig. 2.3(a) show the average effective water speed of the tidal stream speed. The average extracted power is higher, when the tidal stream increases; however, the ripple in the extracted power increases, as well. Fig. 2.4(b) shows a graphic depiction of (2.15), the grid power. For a given tidal stream speed V_{tide} the extracted power varies around a middle point, since the kite's speed is changing based on its periodic movement.

The operating region for turbine speed ω_{turb} higher than the nominal value of 1pu has not been considered at this study, due to mechanical constraints of the experimental set-up in Section 2.3. In the real-life kite system the turbine speed would be limited by the pitch controllers, after it exceeds the nominal value.



(a)



(b)

Fig. 2.4: (a) C_P curve for marine current turbine as referenced from [54–56]; (b) Grid power in pu as a function of the turbine rotational speed for optimal $TSR_{opt} = 6.3$ and maximum $C_{Pmax} = 0.45$

Table 2.1: TUSK Design Parameters

Parameter	Value	Unit
Cylinder radius r	25	m
Sphere radius R	100	m
Turbine radius R_T	0.75	m
Altitude angle D	45	°
Maximum C_{Pmax}	0.45	-
Optimal TSR_{opt}	6.3	-
Power plant base power S_b	500	kVA
Turbine base speed $\omega_{turb\,b}$	84	rad/s
Maximum effective water speed $V_{a\,max}$	10	m/s

2.2.2 MPPT with Active Control of Generator Rotor Speed

The control structure of the SG is based on the FOC strategy and can be seen in Fig. 2.5. There is an outer speed controller loop and an inner current controller, which generates the modulation index m_{gen} for the generator-side VSC. The reference rotor speed ω^*_{gen} in rad/s is provided by the MPPT block of the tidal turbine, as seen in Fig. 2.5. More details about the speed controller of the generator are given in Subsection 2.3.2. The MPPT algorithm presented in [49], which is widely used in wind power plants, has been adopted here in order to develop a suitable control scheme for TUSK power plants.

More specifically, the active power at the grid side of the drive is measured and the optimal rotor speed is calculated though (2.10) for $TSR = TSR_{opt}$ and $C_P = C_{Pmax}$ in order to maximize the power production of the plant. A low-pass filter is applied on the reference rotor speed to filter out high frequency harmonics that come from the grid power measurement.

The TSR_{opt} and C_{Pmax} in (2.10) depend on the geometry of the turbine and are obtained through experimental results in practical applications. In this study, the tidal turbine optimal TSR_{opt} and maximum C_{Pmax} are equal to the values provided in Table 2.1, which have been referenced from [54–56].

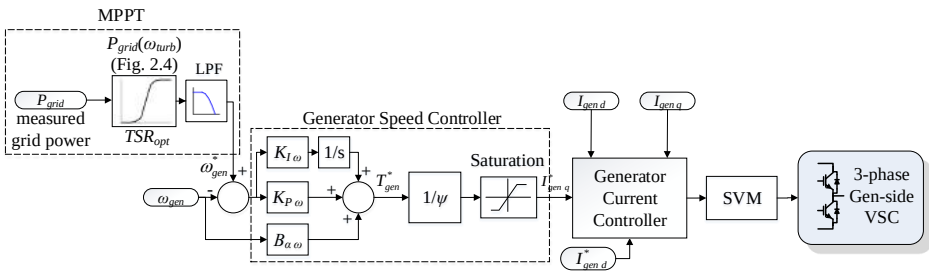


Fig. 2.5: Block diagram of the synchronous generator FOC-based control system with separate speed control loop

2.2.3 MPPT with Torque Control of the Generator

Another way of operating the turbine on the maximum power point is by generating directly the necessary electrical reference torque without the use of any speed controller loop, as referenced from [57]. There is no active control of the shaft speed, since the speed is only a result of the balancing between the generator

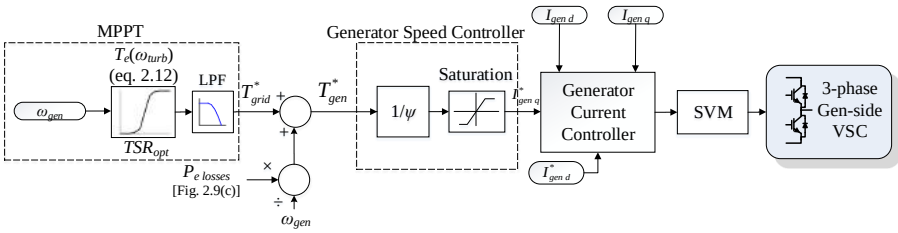


Fig. 2.6: Block diagram of the synchronous generator FOC-based control system with generator torque control

electrical torque and the mechanical torque of the turbine. The main advantage of this MPPT algorithm is the simplicity of the generator control, since only the current controller is needed. An analytical comparison of both MPPT methods is described in Subsection 2.4.2.

Input of the MPPT control algorithm is the measured rotor speed and the optimal electrical torque is calculated based on the torque-speed equation in (2.12) for $TSR = TSR_{opt}$ and $C_P = C_{Pmax}$, so that the turbine can operate under MPPT. The torque given by (2.12) is the electrical torque at the grid side of the kite and, therefore, the losses of the system have to be added in order to calculate the reference torque of the generator.

$$T^*_{gen} = T^*_{grid} + \frac{P_{electrical\,loss}}{\omega_{gen}} \tag{2.16}$$

The losses $P_{electrical\,loss}$ include the stator losses of the generator, the B2B converter and the grid filter losses and are shown in Fig. 2.9(c). The reference current I^*_q is calculated by dividing the reference torque with the flux of the generator and the reference current is fed to the generator current controller. The block diagram of the control system for the generator-side converter is shown in Fig. 2.6, when the generator is controlled in torque control mode.

2.3 Tidal Power Laboratory Emulator

A tidal kite emulator was designed in order to test the system model described in Section 2.2 and the control strategy of the SG. Fig. 2.7 shows the structure of the experimental set-up, which consists of an IM and an externally excited synchronous generator. The SG is driven by B2B-connected VSCs, which operate similarly to the generator drive of a real tidal power plant. The generator-side

VSC controls the generator voltage and speed using the field-oriented control scheme [58] and voltage-oriented control is used for the grid-side VSC [59]. There is a grid filter L_f at the output of the grid-side VSC and a resistor bank R_{init} for soft-charging the dc link capacitors at the initial start-up of the system. The dc link of the generator drive is protected from overvoltage with a braking chopper R_{dc}.

The IM is supplied by a VSC and a passive diode rectifier and emulates the behavior of the TUSK tidal turbine. The control system of the SG power converters is implemented on the dSPACE 1005 control board. The design parameters of the experimental emulator and the base of the experimental analysis per-unit system are presented in Table 2.2. An overview picture of the laboratory set-up is shown in Fig. 2.8(a).

In order to emulate the turbine shaft inertia of a real TUSK tidal plant, a flywheel has been installed in the machine set-up as shown in Fig. 2.8(b). The flywheel has the shape of a circular disc and a mass of approximately 90 kg. The additional inertia that the flywheel adds on the shaft of the electrical machines is equal to 5.74 kg $\cdot$ m^2.

2.3.1 Design Process of the Emulator

The IM of the experimental set-up is controlled in Direct Torque Control (DTC) mode by an ACS600 ABB drive [60]. The rated rotational speed of the IM is 1445 rpm. The electromagnetic torque reference T^*_{eIM} is calculated by the tidal turbine model, which has been presented in Section 2.2.

Inputs of the model are the design characteristics of the TUSK trajectory and turbine geometry, while outputs of the model are the optimal power-rotor speed

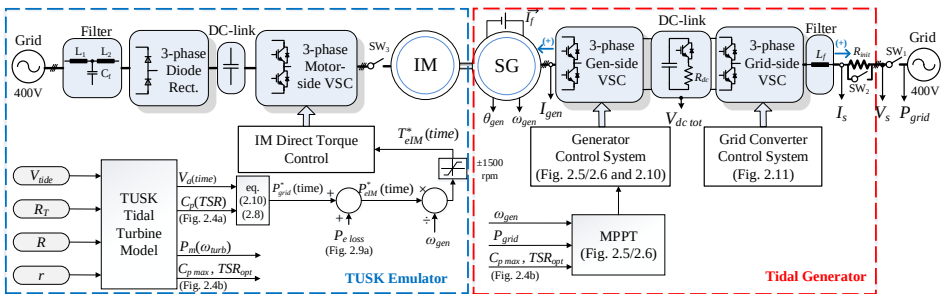
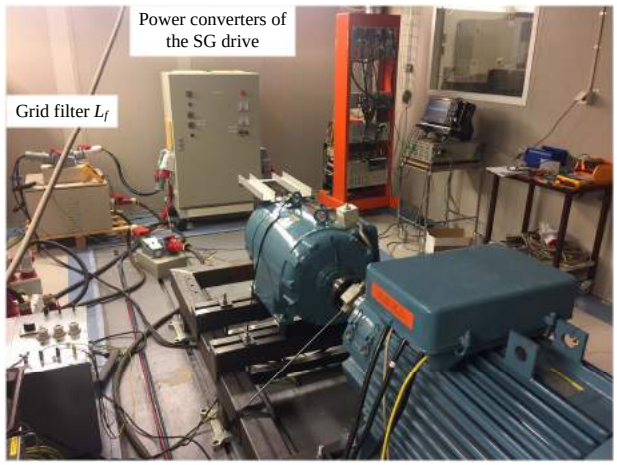
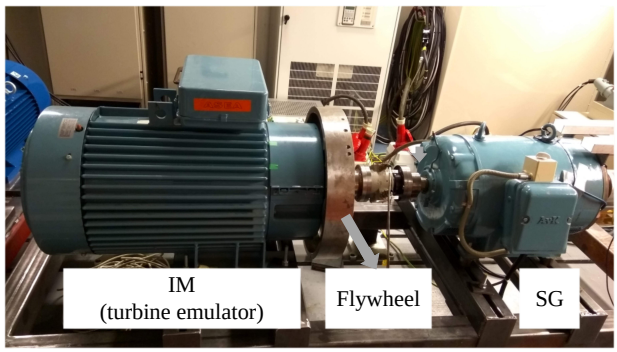


Fig. 2.7: Power circuit and control system diagram of the TUSK tidal plant emulator



(a)



(b)

Fig. 2.8: Laboratory set-up of a 35 kVA converter-driven TUSK tidal plant emulator: (a) overview of the set-up and (b) the electrical machines test bench with the flywheel installed

curve (Fig. 2.4), the maximum C_{Pmax}, optimal TSR_{opt} and a time series of the effective water speed V_a. Then, the active power of the TUSK plant is calculated based on (2.10). The losses of the laboratory emulator have been added to the reference grid power $P^*_{grid}(time)$, so that the output power of the set-up P_{grid} is equal to the power calculated through the TUSK tidal turbine model through equation (2.10). Finally, the reference electromagnetic torque of the IM T^*_{eIM} is calculated by dividing the active power with the rotor speed.

The losses of the laboratory emulator have been measured with the oscilloscope and are shown in Fig. 2.9 for many different operational points of the SG. Specifically,

Table 2.2: Tidal Power Emulator Design Parameters

Parameter	Value	Unit
Base rotor speed n_b	1500	rpm
Base power S_b	35	kVA
Base current I_b	71.7	A
SG number of pole pairs P	2	-
Shaft inertia (without the flywheel) J	2.04	kg·m^2
Shaft inertia (with the flywheel) J'	7.78	kg·m^2
SG friction constant b	0.073	Nm/rad·s
SG excitation I_f	22	A
SG Stator resistance R_s	60	mΩ
SG Stator inductance L_d	10.8	mH
SG Stator inductance L_q	6.2	mH
SG d-axis mutual inductance (for rated I_f) L_{md}	10.4	mH
Power converters' switching freq. f_{sw}	5	kHz
Grid filter inductance L_f	2	mH
DC-link capacitance	6.08	mF
Nominal dc-link voltage of the SG drive $V_{dc\ tot}$	670	V
Nominal L2L grid voltage (rms) V_s	400	V

the measured losses in Fig. 2.9(a)-(b) include the mechanical losses of the IM and SG, the core and copper losses of the SG, the generator and grid VSC losses and the grid filter L_f losses. Fig. 2.9(c)-(d) shows only the converter and grid filter losses of the SG drive.

2.3.2 Generator Speed Controller Design

A schematic of the SG speed controller is shown in Fig. 2.5. It consists of a proportional-integral (PI) control loop and an active damping term $B_{a\omega}$. The gains of the PI loop are chosen based on the Loop Shaping Method [61] and are defined as

$$K_{P\omega} = a_\omega \cdot J \tag{2.17}$$

$$K_{I\omega} = a_\omega \cdot (b + B_{a\omega}) \tag{2.18}$$

where a_ω is the closed-loop bandwidth of the speed controller, J is the inertia of the system and b is the friction constant of the SG. Various values of the a_ω are

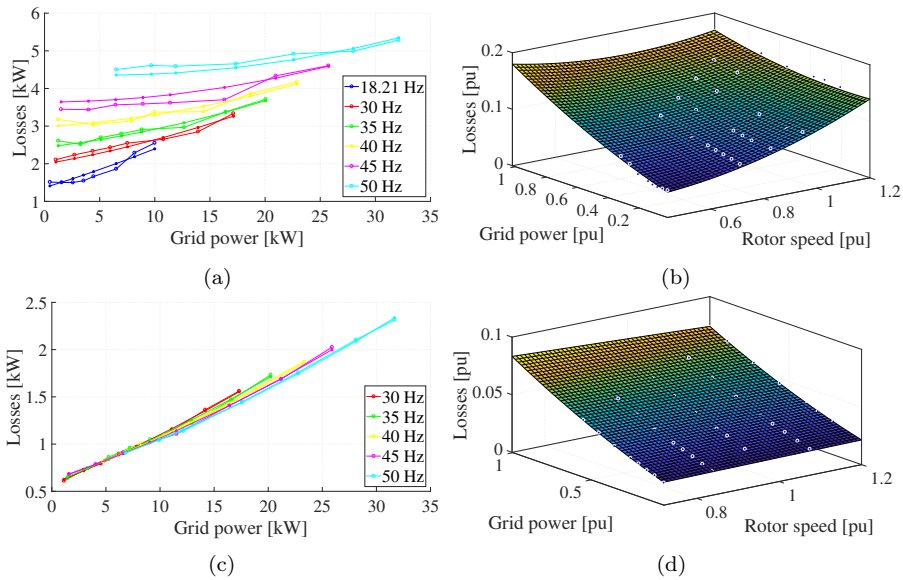


Fig. 2.9: Curve-fitted diagram of the TUSK tidal power emulator losses including the (a)-(b) total SG drive losses and the IM mechanical losses and (c)-(d) the electrical losses of the power converters and grid filter in the SG drive

tested later in Subsection 2.4.1. The active damping term $B_{a\omega}$ is selected as

$$B_{a\omega} = a_\omega \cdot J - b \tag{2.19}$$

in order to increase the robustness of the controller against estimation errors of the system parameters.

The output of the speed controller is the reference current $I^*_{gen\ q}$ which is limited up to its rated value of 71.7 A by a saturation block. Anti-reset windup is also implemented, which is not shown in the block diagram of Fig. 2.5.

2.3.3 Generator Current Controller Design

The schematic of the generator current controller is shown in Fig. 2.10. The current controller diagram is split between the d and q axis control blocks. Inputs of the controller are the current reference and actual values in both d and q axis. The gains and the active damping term of the d-axis PI controller are selected

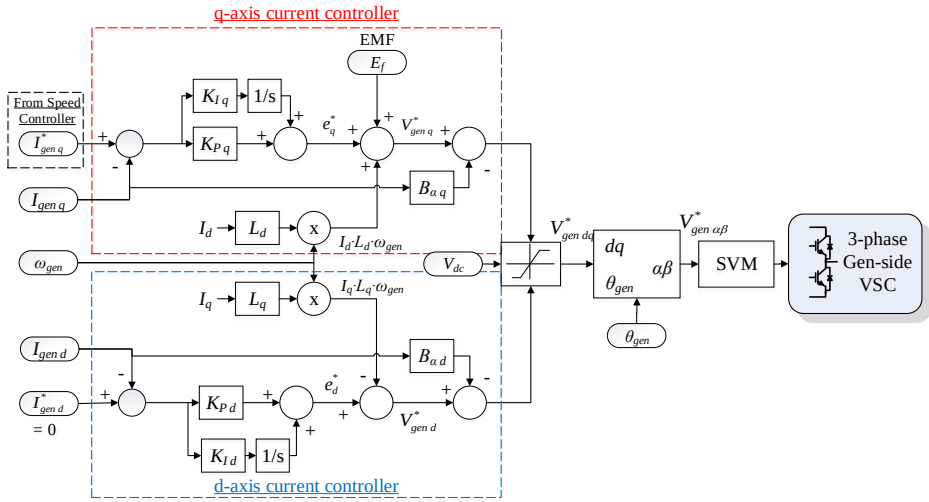


Fig. 2.10: Block diagram of the SG current controller in dq-frame

based on the Loop Shaping Method as follows

$$K_{Pd} = L_d \cdot a_c \tag{2.20}$$

$$K_{Id} = a_c \cdot (R_S + B_{ad}) \tag{2.21}$$

$$B_{ad} = L_d \cdot a_c - R_S \tag{2.22}$$

Similar equations define the parameters of the q-axis PI controller. The switching frequency of the SG power converters is set to 5kHz. Therefore, the closed-loop bandwidth of the generator current controller is chosen to be equal to $a_c = 2\pi \frac{f_{sw}}{50} = 2\pi \cdot 100\text{rad/s}$ in order to have a stable system during dynamic and steady-state operation. The peak value of the SG EMF voltage is calculated as

$$E_f = L_{md} I_f \omega_e \tag{2.23}$$

Output of the generator current controller is the generator reference dq-voltage $V^*_{gen\ dq}$, which is limited by a saturation block in order to avoid overmodulation. Anti-reset windup is also implemented, which is not shown in the block diagram of Fig. 2.10.

2.3.4 Grid-side VSC Control System Design

The block diagrams of the controllers for the grid-side VSC are shown in Fig. 2.11. More specifically, the current controller in dq-frame [59] is shown in Fig. 2.11(a).

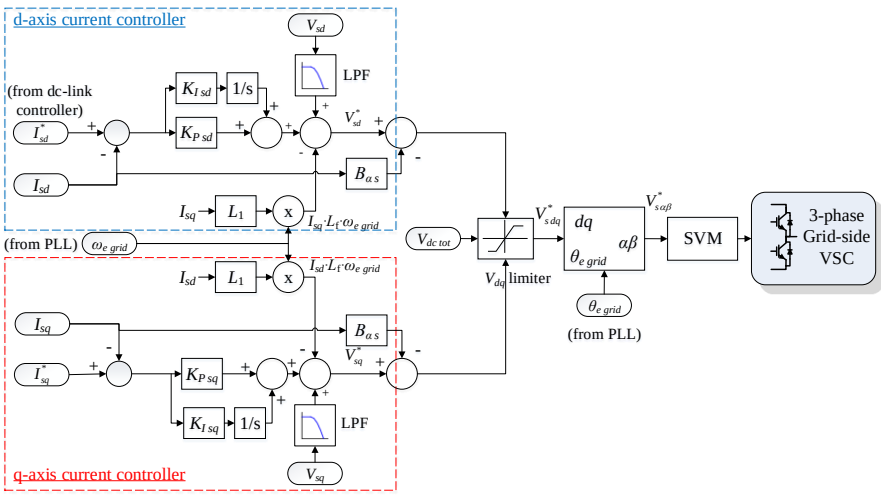
The gains are defined as follows

$$K_{Psd} = K_{Psq} = L_f \cdot a_{cs} \tag{2.24}$$

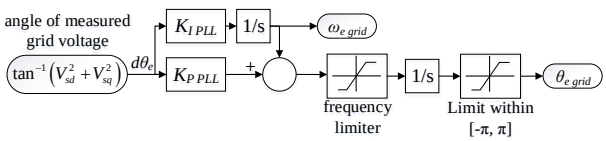
$$K_{Id} = a_{cs} \cdot (R_f + B_{as}) \tag{2.25}$$

$$B_{as} = L_f \cdot a_{cs} - R_f \tag{2.26}$$

where L_f and R_f are the grid filter parameters. The grid current controller bandwidth for the laboratory set-up of the emulator is equal to $a_{cs} = 2\pi \frac{f_{sw}}{10} =$



(a)



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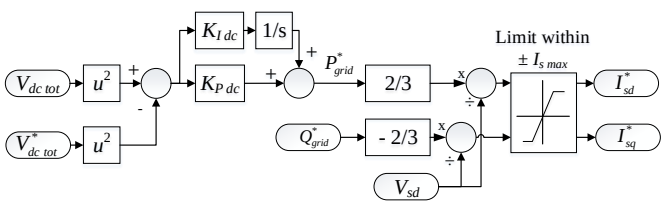


(c)

Fig. 2.11: Block diagram of the grid-side VSC (a) current controller, (b) PLL and (c) dc-link controller

$2\pi \cdot 500$ rad/s.

The phase-locked-loop (PLL) of the grid-side converter is shown in Fig. 2.11(b) and its task is to track the angle and calculate the frequency of the grid voltage V_s. The PI controller of the PLL aligns the space vector of the V_s with the d-axis in the dq-frame by keeping the angle and the q-axis component of the grid voltage equal to zero. The gains of the controller are selected as described in [62, 63]

$$K_{PPLL} = 2 \cdot a_{PLL} \tag{2.27}$$

$$K_{IPLL} = a_{PLL}^2 \tag{2.28}$$

where a_{PLL} is the bandwidth of the PI controller and in this case it is chosen equal to $2\pi \cdot 5$ rad/s.

The dc-link controller, shown in Fig. 2.11(c), keeps the dc-link voltage close to its reference value $V_{dc\ tot}^*$. The power balance at the dc-link is described by

$$\frac{C_{dc\ tot}}{2} \frac{dV_{dc\ tot}^2}{dt} = P_{gen} - P_{grid} - P_{loss} \tag{2.29}$$

The left part of the above equation corresponds to the rate of change in the energy of the dc-bus capacitors and the second power of the dc voltage $V_{dc\ tot}^2$ is regulated by the dc-link controller. The $C_{dc\ tot}$ is the dc-link capacitance of the drive and is equal to 6.08 mF. The proportional gain of the controller is selected as

$$K_{P\ dc} = a_{DClink} \cdot C_{dc\ tot} \tag{2.30}$$

where a_{DClink} is the bandwidth of the controller and is chosen to be 10 times slower than the grid current controller bandwidth, namely $a_{DClink} = a_{cs}/10 = 2\pi \cdot 50$ rad/s. The dc-link PI-controller is selected to have dynamic response with time constant of 0.03 sec/rad and, therefore, the integrator of the controller is

$$K_{I\ dc} = \frac{K_{P\ dc}}{0.03} \tag{2.31}$$

Output of the controller is the reference active power of the grid converter P_{grid}^*.

$$P_{grid}^* = \frac{3}{2}\left[V_{sd} \cdot i_{sd}^* + V_{sq} \cdot i_{sq}^*\right] \overset{V_{sq}=0}{=\!=} \frac{3}{2} \cdot V_{sd} \cdot i_{sd}^* \tag{2.32}$$

The power exiting the converter has positive sign and the current direction is indicated with arrows in Fig. 2.7.

2.4 Experimental Results of the Laboratory Emulator

The experimental results of this section are divided into two parts. In Subsection 2.4.1 an analysis of the bandwidth of the speed controller is made and its effect on the kite's power generation is shown. Experimental results from the TUSK plant emulator are presented, while in this case the flywheel shown in Fig. 2.8(b) is not installed in the set-up in order to allow faster responses of the speed control. In Subsection 2.4.2 a comparison of the MPPT algorithms from Subsections 2.2.2 and 2.2.3 is made for different operating conditions of the TUSK. The flywheel is installed in this case on the shaft of the machine system, in order to study also the effect of the inertia on the response of the system and to point out any possible problems that can arise.

2.4.1 Effect of the Speed Controller's Response Time on the kite's Power Generation

The transient response experimental results of the SG speed controller are shown in Fig. 2.12(a)-(b), where a step-change of the speed reference is performed from 0.6pu (corresponding to 900rpm) to the nominal speed of 1pu (which is equal to 1500rpm). As can be seen in the figure, the rise time t_r is 0.31s, when the speed controller bandwidth is $a_\omega = 2\pi$ rad/s. The reference q-axis current of the generator I^*_{genq} reaches also its maximum positive value of 71.7A, while the machine is accelerating. Due to the fast acceleration applied in this test, the SG operates temporarily in motor operation and the current becomes positive. A slower speed controller with bandwidth equal to $a_\omega = 2\pi \cdot 0.1$ rad/s has also been tested in Fig. 2.12(c)-(d), which has a rise time t_r of 3.66s. The t_r is defined as the response time of the generator between 10% and 90% of the final value of the reference speed.

The TUSK tidal plant model shown in Subsection 2.2.1 is tested experimentally on the laboratory emulator and the power curves of Fig. 2.13 are imported into the dSPACE control platform. The power and speed calculations have been converted into the per-unit system in order to scale down the real 500kW tidal turbine (Table 2.1) into the 35kVA electric drive of the emulator (Table 2.2). Aim of this test is to investigate if the generator speed controller can follow effectively the speed reference given by the MPPT block. The MPPT control algorithm with separate

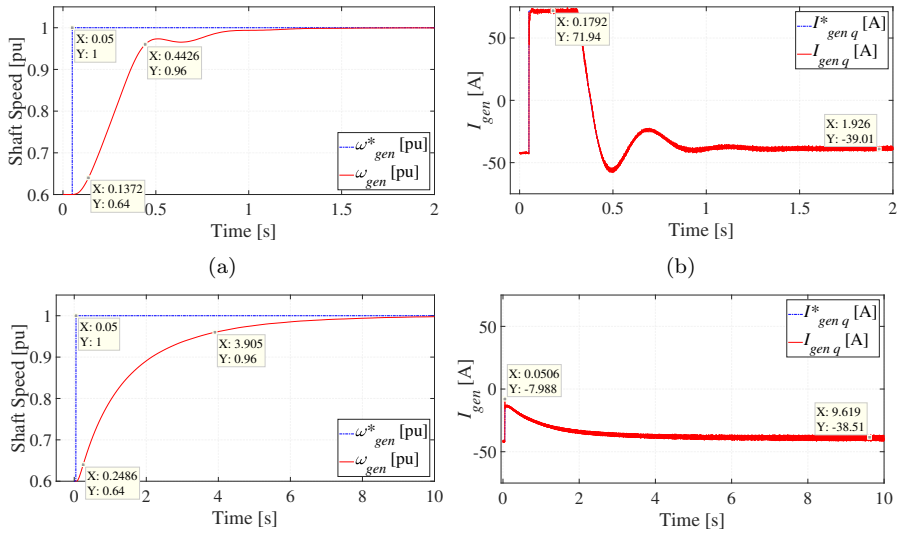


Fig. 2.12: Experimental results of the SG in a step-change of the reference speed from 0.9pu (900rpm) to 1pu (1500rpm) with speed controller bandwidth equal to (a)-(b) $a_\omega = 2\pi$ rad/s and (c)-(d) $a_\omega = 2\pi \cdot 0.1$ rad/s

speed control loop of the generator (Fig. 2.5) is used in this subsection. As can be seen in Fig. 2.13, a decrease of the Viviani's curve r radius results to faster turbine power variations and faster variations of the generator speed reference, since the system is controlled with TSR_{opt} and C_{Pmax}. More specifically, $r = 25$ m results to a power variation with period 22.9 s, while at $r = 5$ m the period of the power

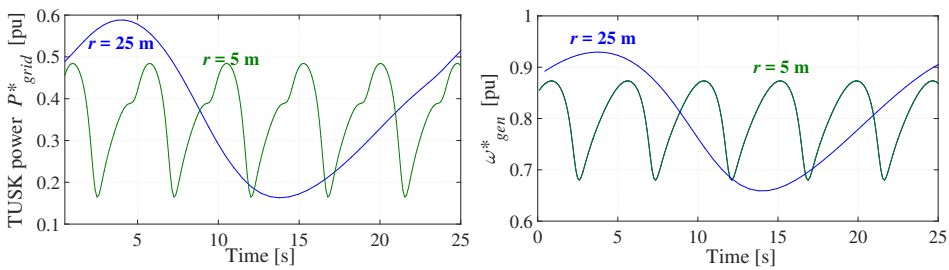
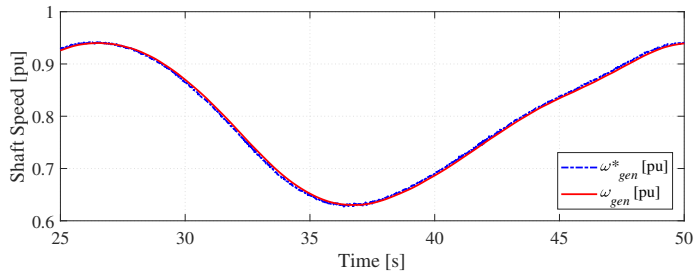
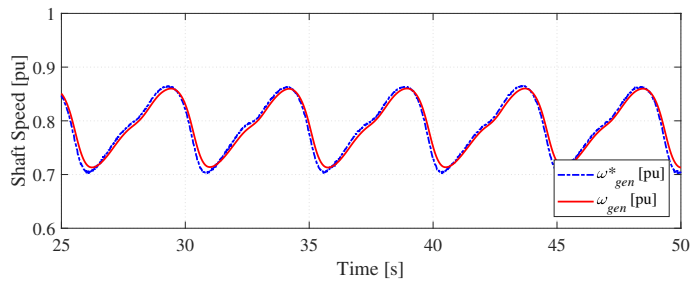


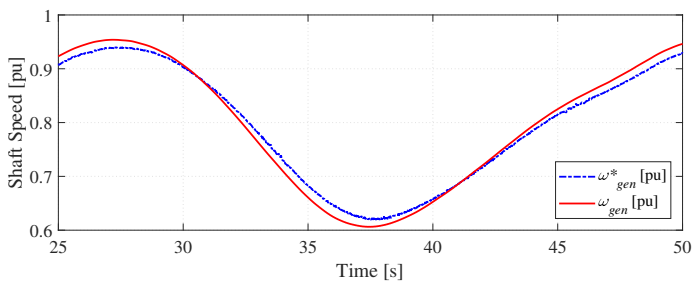
Fig. 2.13: (a) Reference grid power and (b) shaft speed of the tidal power emulator for modelling a TUSK tidal power plant with tidal stream speed $V_{tide} = 1.9$ m/s and Viviani's curve radius $r_1 = 25$ m and $r_2 = 5$ m.



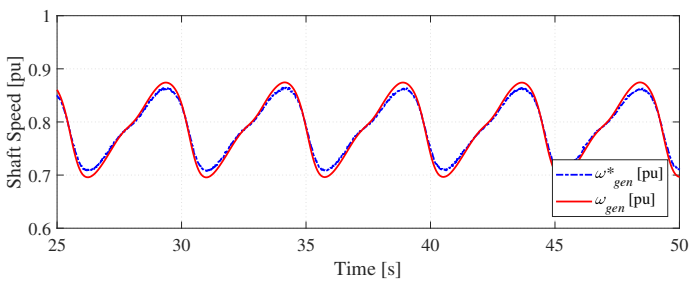
(a) $a_\omega = 2\pi$ rad/s, $r = 25$ m



(b) $a_\omega = 2\pi$ rad/s, $r = 5$ m

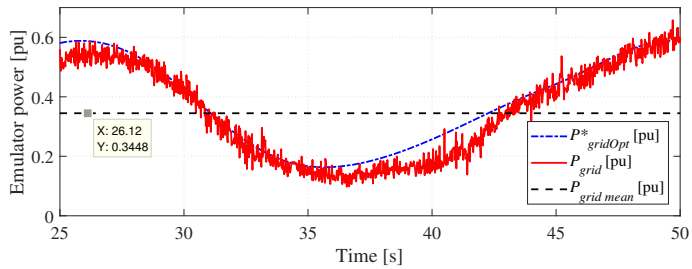


(c) $a_\omega = 0.2\pi$ rad/s, $r = 25$ m

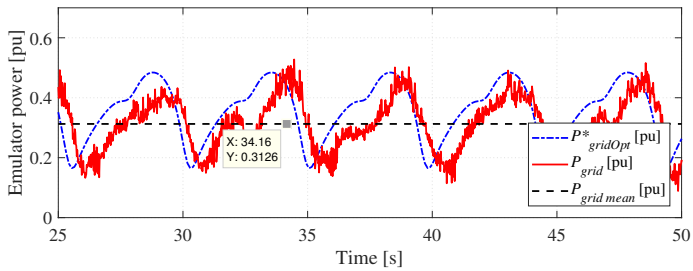


(d) $a_\omega = 0.2\pi$ rad/s, $r = 5$ m

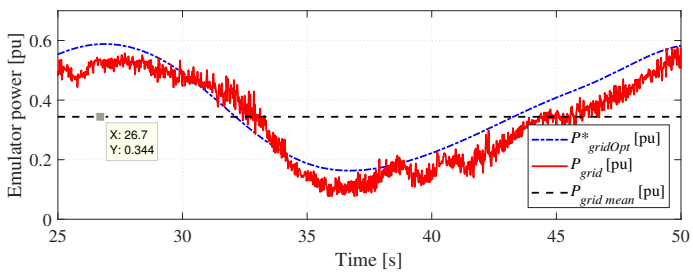
Fig. 2.14: Experimental results of the tidal power emulator reference and actual shaft speed with different profiles of the TUSK trajectory and different generator speed controller bandwidths



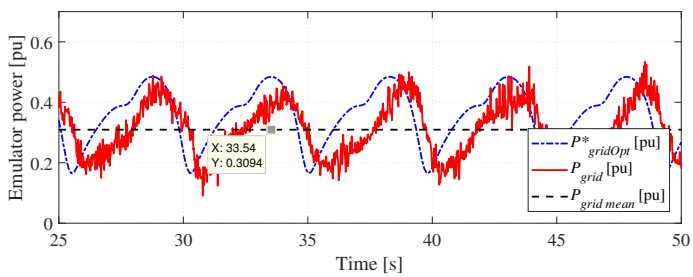
(a) $a_\omega = 2\pi$ rad/s, $r = 25$ m



(b) $a_\omega = 2\pi$ rad/s, $r = 5$ m



(c) $a_\omega = 0.2\pi$ rad/s, $r = 25$ m



(d) $a_\omega = 0.2\pi$ rad/s, $r = 5$ m

Fig. 2.15: Experimental results of the tidal power emulator reference and actual grid power with different profiles of the TUSK trajectory and different generator speed controller bandwidths.

is 4.6 s.

The experimental results of the emulator for Viviani's curve radius equal to $r_1 = 25$ m and $r_2 = 5$ m are shown in Fig. 2.14. The generator actual speed ω_{gen} follows the reference shaft speed given by the MPPT control block with small error, when the bandwidth of the speed controller is equal to $a_w = 2\pi$ rad/s and the radius of the trajectory is $r_1 = 25$ m [Fig. 2.14(a)]. However, when the tidal kite's motion becomes faster at $r_2 = 5$ m, the error between the reference speed and the actual shaft speed becomes larger. This error increases even more when the bandwidth of the speed controller is equal to $a_w = 0.2\pi$ rad/s.

The error between the reference rotor speed and the actual speed causes the emulated power plant to operate with TSR different from the optimal value, which also results to a decrease in the produced power. Fig. 2.15 shows with dashed blue line the active power at the grid side that the emulator would produce, if it could always operate with optimal TSR and maximum C_p. The actual power P_{grid} produced by the emulated plant is also shown with red line and the average actual power is shown with black dashed line. It can be seen that the produced power of Fig. 2.15(a) is the closest to the optimal case, while in all the other cases the actual power is a little lower than the optimal power. There is also a time shift between the $P_{gridOpt}$ and P_{grid}, which is more visible in Fig. 2.15(b) and Fig. 2.15(d). This delay is introduced by the PI controller of the generator speed control loop and by the LPF at the output of the MPPT block (Fig. 2.5).

2.4.2 MPPT Algorithm Comparison Study

The MPPT algorithms described in Subsections 2.2.2 and 2.2.3 are now compared experimentally on the tidal power emulator. The flywheel is installed in this case on the shaft of the machine system and the inertia of the mechanical system increases compared to the previous study and is equal to $J' = 7.78\text{kg}m^2$. The transient response of the SG speed controller is shown in Fig. 2.16, where a step-change of the speed reference is performed from 0.6pu (corresponding to 900rpm) to the nominal speed of 1pu (which is equal to 1500rpm). Bandwidths of $a_\omega = 2\pi$ rad/s and of $a_\omega = 2\pi \cdot 0.1$ rad/s are tested, similarly to Subsection 2.4.1.

As can be seen in Fig. 2.16(a), the rise time t_r is 1.07s, when the speed controller bandwidth is $a_\omega = 2\pi$ rad/s, which is as expected more than three times higher than in the case without the flywheel. The rise time becomes equal to $t_r = 3.46$ s, when the slower speed controller $a_\omega = 2\pi \cdot 0.1$ rad/s is tested [Fig. 2.16(c)].

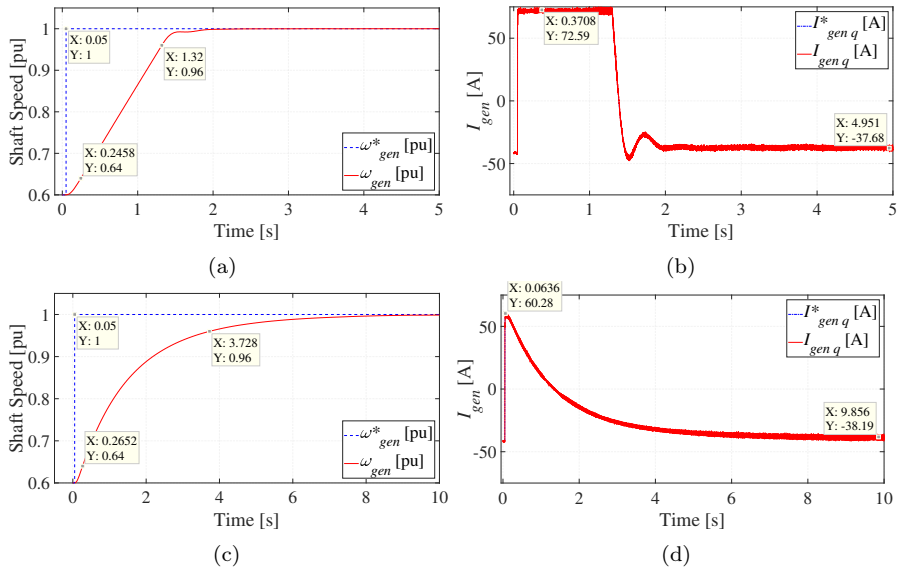
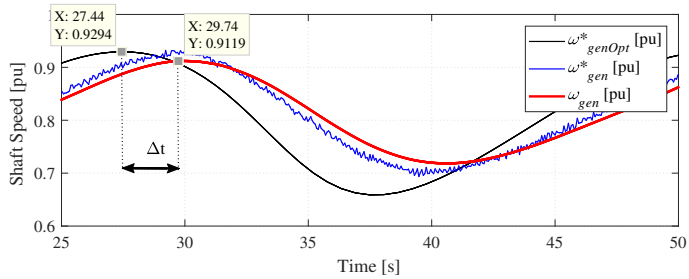


Fig. 2.16: Experimental results of the SG with the flywheel installed on the shaft in a step-change of the reference speed from 0.9pu (900rpm) to 1pu (1500rpm) with speed controller bandwidth equal to (a)-(b) $a_\omega = 2\pi$ rad/s and (c)-(d) $a_\omega = 2\pi \cdot 0.1$ rad/s

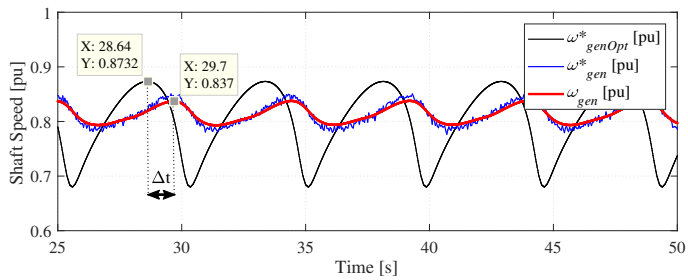
The TUSK tidal plant model is tested experimentally on the laboratory emulator and the power curves of Fig. 2.13 are imported into the dSPACE control platform. The MPPT control algorithm with speed control loop (Fig. 2.5) is compared with the algorithm with torque control of the generator (Fig. 2.6) in the following figures in order to identify which control structure has the best performance.

The experimental results of the shaft speed for Viviani's curve radius equal to $r_1 = 25$ m and $r_2 = 5$ m are shown in Fig. 2.17. The blue curve shows the reference speed ω^*_{gen} which is generated by the MPPT block, when the generator is controlled with speed controller and bandwidth equal to 0.2π rad/s. The black curve shows the optimal reference speed ω^*_{genOpt}, which is the reference speed that the emulator would have if it operated with constant $C_{Pmax} = 0.45$. Fig. 2.17(a)-(b) show the experimental results of the generator when the speed controller is used, while in Fig. 2.17(c)-(d) the torque control mode is used.

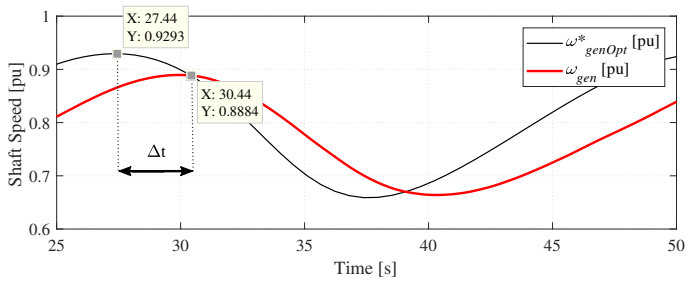
As can be seen in Fig. 2.17, there is a delay Δt between the actual shaft speed ω_{gen} and the ω^*_{genOpt}. The delay is higher in the case of the torque control mode compared to the speed control mode by 0.7s, when the Viviani's curve radius is



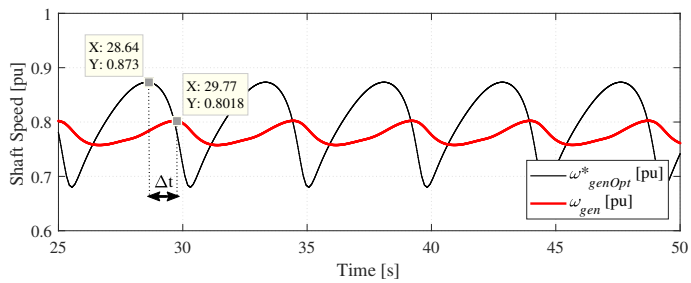
(a) $a_\omega = 0.2\pi$ rad/s, $r = 25$ m



(b) $a_\omega = 0.2\pi$ rad/s, $r = 5$ m



(c) Torque control, $r = 25$ m



(d) Torque control, $r = 5$ m

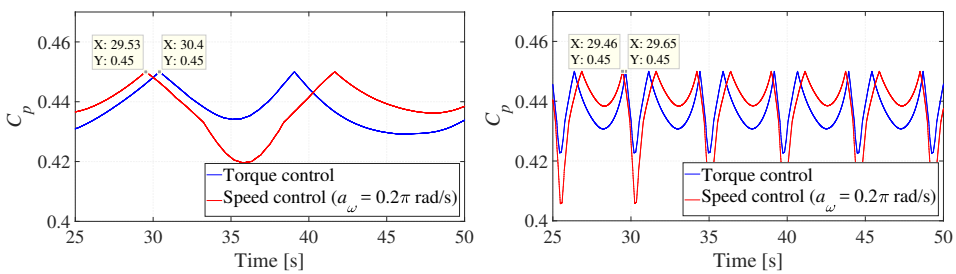
Fig. 2.17: Experimental results of the tidal power emulator reference and actual shaft speed with different profiles of the TUSK trajectory and different MPPT methods

equal to $r_1 = 25$ m [Figs. 2.17(a) and 2.17(c)] and higher by 0.07s when $r_2 = 5$ m [Figs. 2.17(b) and 2.17(d)]. Due to this delay Δt the active power produced by the emulated tidal turbine is expected to be lower in the case of the torque control mode, as will be shown later. Fig. 2.18 shows the C_P curves of the emulator for all the four operating conditions. In all the graphs the C_P curve reaches the peak point of 0.45 when the shaft speed ω_{gen} overlaps with the ω^*_{genOpt}. However, the slower response of the generator operating in torque control mode is also visible here.

Fig. 2.19 shows the generated active power at the grid side of the emulator. The red solid line shows the actual power of the grid P_{grid}, the dashed blue line is the reference grid power P^*_{grid} and the dashed black line represents the optimal reference power $P^*_{gridOpt}$ that the emulator would produce with constant TSR_{opt} and C_{Pmax}. The average power $P_{gridmean}$ is shown with dashed red line and is higher when the MPPT with speed control is used in Figs. 2.19(a)-(b) compared to the results in Figs. 2.19(c)-(d).

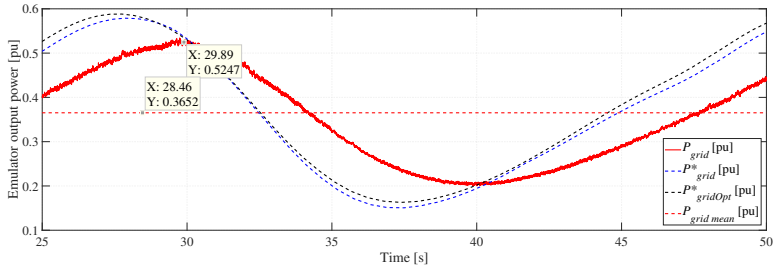
Fig. 2.20 shows a closer look of the reference grid powers, where the peak values of the reference active power can be seen. Higher reference power can be seen here as well for the MPPT with speed control.

It can be concluded that the generator has a faster dynamic response when the MPPT algorithm with speed control loop is used compared to the MPPT scheme with torque control. The result of this faster response is that the generator can produce higher power at the peak points as well as in average in one cycle of the kite's trajectory. The advantageous performance of the generator speed controller can be explained by considering the time constant of the mechanical model of the generator. The time constant of the generator when there is no active speed

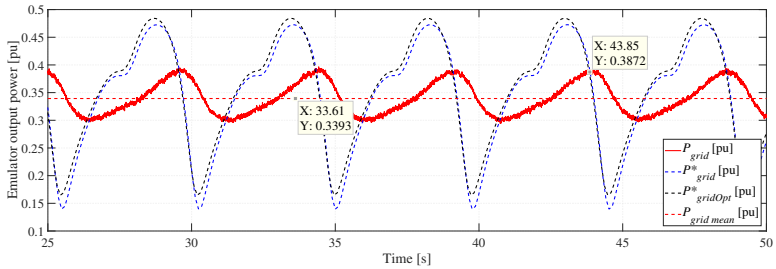


(a) $r = 25$ m (b) $r = 5$ m

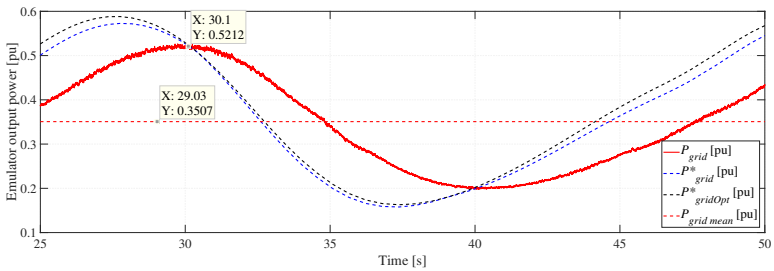
Fig. 2.18: Experimental results of the tidal power emulator power coefficient C_P with different profiles of the TUSK trajectory and different MPPT methods.



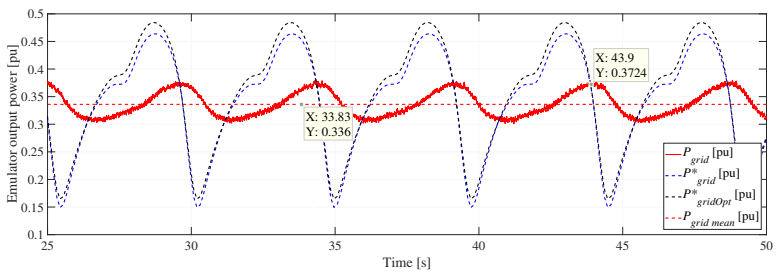
(a) $a_\omega = 0.2\pi$ rad/s, $r = 25$ m



(b) $a_\omega = 0.2\pi$ rad/s, $r = 5$ m

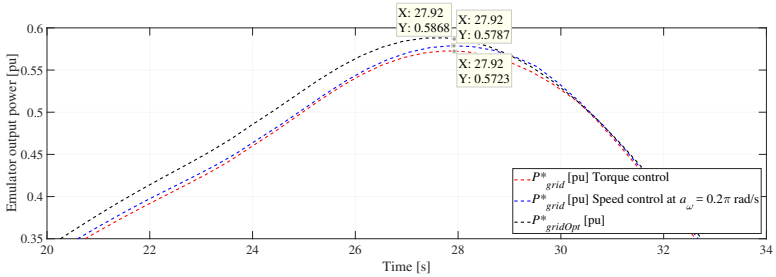


(c) Torque control, $r = 25$ m

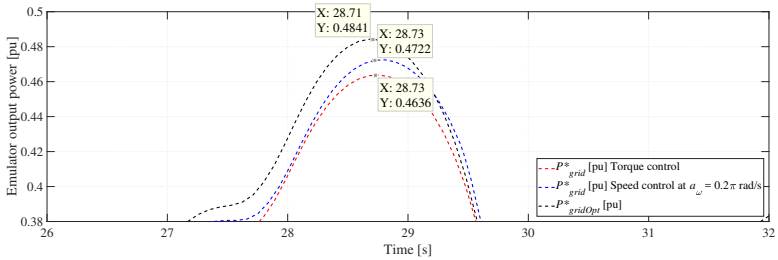


(d) Torque control, $r = 5$ m

Fig. 2.19: Experimental results of the tidal power emulator reference and actual grid power with different profiles of the TUSK trajectory and different MPPT methods



(a) $r = 25$ m



(b) $r = 5$ m

Fig. 2.20: Experimental results of the tidal power emulator reference grid power

control loop and when torque control mode is used is equal to

$$\tau_{Tctrl} = \frac{J'}{b} \tag{2.33}$$

The time constant of the generator when the speed controller is used, which is described in Subsection 2.2.2, is equal to

$$\tau_{Sctrl} = \frac{K_{P\omega}}{K_{I\omega}} = \frac{J'}{b + B_{a\omega}} \tag{2.34}$$

It is clear that $\tau_{Tctrl} > \tau_{Sctrl}$, which explains the previously presented experimental results.

2.4.3 Summary

Chapter 2 presents the model of a TUSK tidal power generator unit describing the kite's trajectory and the produced electric power. It has been shown that the tidal turbine produces fluctuating electrical power due to the motion of the TUSK into the sea. Two different algorithms of MPPT have also been presented, one with closed loop speed control and the second method with torque control of the generator. A laboratory emulator of the TUSK has been constructed for

reproducing the performance of the tidal system in laboratory conditions. The accuracy of the shaft speed control has been evaluated with measurements on the emulator for different trajectories of the TUSK and gains of the speed controller.

The experimental results are divided into two parts. The first part in Subsection 2.4.1 analyzes the effect of the speed controller bandwidth on the performance of the MPPT. Specifically, Fig. 2.15 shows that an increase of 10 times of the PI controller gains results to an increase of the average produced power of up to 1%, since the speed controller of the generator converter can follow the reference rotor speed with smaller error. Therefore, a better design of the PI controllers regulating the converters and a fast speed controller can increase the power produced by the TUSK tidal power system.

The second part of the experimental results in Subsection 2.4.2 compares two MPPT control schemes, the MPPT with torque control of the generator which is simpler and easier to design and the control scheme with active speed control. The speed control method has advantageous dynamic response which results to a higher power production of the tidal turbine, although the difference in the performance of both methods is quite small in some cases. Specifically, the average power production of the generator $P_{grid\ mean}$ is approximately 4% higher when using active speed control compared to the MPPT with torque control, as shown in the Figs. 2.19(a) and 2.19(c) where it increases from 0.3507pu to 0.3652pu.

The results of this chapter can be utilized to improve the power production of tethered kites. The advantages and disadvantages of each MPPT control scheme need to be considered in order to evaluate if the more efficient, but also more complicated, speed control method should be used or the torque control method is better due to its simplicity. The experimental set-up of the tidal power emulator can also be used for modelling the power generation from other renewable energy sources, such as the wind power. The wind speed variations are stochastic, contrarily to the kite tidal speed variations which have been studied here. Therefore, emulating wind speed variations with the IM of the current experimental set-up could be of high value in order to investigate and optimize the performance of the generator.

Chapter 3

Multilevel Converter Topologies and Modulation Techniques

3.1 Motivation towards Medium Voltage Drives

Increasing the operating voltage of the power generation system has attracted interest in offshore applications, since it leads to higher power density. Electrical machine drives with higher voltage have lower current flow in the cables and the power converters, which leads to reduced copper loss and to a possible reduction of the cables size. Medium voltage drives are particularly popular in power generation from renewable energy sources (RES), including wind and tidal/wave power systems, where the high power density can lead to a decrease of the system level cost. Large power generation units (e.g. 10MW or even higher) suffer from high current on the cables and on the semiconductors of the converters [64], whereas by increasing the operating voltage of the system, the conduction losses can be considerably reduced.

Especially in the case of the TUSK, the power cables, which are installed inside the tether of the kite, can hinder its movement inside the sea and create additional drag which is reflected in the power production equation (2.5). Therefore, it is of high importance to decrease the cables' size and weight as much as possible. Also, the kite is connected to the onshore PCC through long cables which lay on the sea-bed. The power losses and the voltage drop through these cables need to be kept at minimum level in order to connect to the local grid. Increasing the operating voltage of the power generation system helps either to increase the

efficiency of the power cables and to keep the voltage drop low (in case the copper area of the cables is kept constant) or to reduce the cable size and make the kite system more compact.

3.2 Multilevel Converter Topologies

The above issues can be effectively addressed by using medium voltage multilevel converters in the generator drive. The basic concept of these topologies is the interconnection of many low-voltage-rated power switches. A simple series connection of power switches may increase the operating voltage of the converter as that shown in the traditional 2-level converter (2LC) of Fig. 3.1(a). However, this type of converter faces the serious problem of unbalanced voltage sharing among the power switches due to the system parasitic components and the uneven characteristics of the power switches. This problem can be solved by using balancing circuits or special designed gate drivers that ensure synchronous turn on/off of the switches [28, 29]. The losses of the medium voltage 2LC are also higher than in the multilevel topologies described later [29].

Multilevel converters can be defined as the inverters that generate at least three voltage levels at their ac side. Multiple low-voltage-rated power switches are used in these topologies, so that the converter is able to operate with high voltage. This topology also attains reduced total harmonic distortion at the ac side, compared to the 2-level VSC. This is a further advantage in the case of the undersea kites because the passive filters placed inside the kite at the grid-side of the generator drive can be drastically minimized saving space and weight. Another advantage of the multilevel converters is the reduced $\frac{dV}{dt}$ of their generated ac voltage [1] , which is not further studied in this thesis.

Modular converters, such as the Cascaded H-Bridge (CHB) converter or the Modular-Multilevel-Converter (MMC) [65], are commonly used topologies in high-voltage applications. These converters due to their modular structure can have large number of levels handling many tens to hundreds kVs of voltage and, therefore, they are commonly used in grid applications for improving power flow control and grid voltage stability, such as in parallel connection to the transmission lines as STATCOMs [66] and in HVDC applications [67]. One disadvantage of these

[1] C. Larsson, A. Rydgård, G. Mademlis, Y. Liu, and M. Fredriksson, "Overvoltage Mitigation of Medium Voltage Electric Drives with Long Cables using Multilevel-Converters and Passive Filters", to be presented in *the 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*, 2019

topologies is the lack of a common dc-link at their dc-side, since each converter module has its own capacitor. Therefore, they are used less frequently in electric drives where two of these converters need to be connected back-to-back (B2B), because disturbances at the machine-side can affect more easily other control variables at the grid-side of the system and vice versa [68]. Also, the need for many passive components, such as capacitors at each converter module and inductors for each converter leg, can make the converter bulky.

The Neutral-Point-Clamped (NPC) (also known as Diode-Clamped) converter, originally introduced in [69], and the Flying-Capacitor (FC) converter are two of the main multilevel VSC types with a controllable dc-link at their dc-side. Their 3-level [Fig. 3.1(b)] variant has already been used in industrial applications, such as in [70, 71] for the NPC converter. Both the FC and the NPC converters are limited up to 5-levels in practical applications, because their structure becomes too complicated for higher number of levels. The power switches used in these converters are rated to 1/4 of the total dc-link voltage. Therefore, by using power switches of 1.2kV rated voltage, dc-link voltage of up to 4 kV can be obtained in their 5-level version, depending on the safety voltage margin that we choose to have for the power semiconductors. The schematics of 5-level FC and NPC converters are shown in Fig. 3.1(c)-(d).

The main advantage of the FC converter compared to the NPC is the reduced number of semiconductor components. They have equal number of power switches, but the NPC converter has also got clamping diodes. This makes the structure of the FC much simpler compared to the NPC. However, a large number of capacitors are needed for the FC converter, which becomes even larger in the 5-level version and increases a lot the size of the power conversion system. Proper balancing of these flying capacitor voltages and precharging them during the system initialization is needed making the operation of the converter more complicated [72].

On the other hand, the NPC converter requires the highest number of semiconductors due to the extra clamping diodes that it has, which also do not have equal reverse voltage rating. For this reason, series connection of two diodes are needed in some points, as can be seen in Fig. 3.1(d). However, the NPC converter has the lowest number of capacitors [73], which keeps the volume of the converter small, if a high-power-density design is implemented with low loss semiconductor devices. Since the size of the power conversion system is of high importance for the TUSK application, the 5-level NPC inverter is chosen as the preferred VSC topology studied in the rest of the thesis.

Another serious issue of the NPC converter is the control of its dc-link capacitors. In general, an N-level NPC converter uses a single dc-bus which is subdivided into $N-1$ series connected capacitors, whose voltages should be monitored and properly controlled in order to be balanced in every operating condition. A more detailed study of the control of the dc-link capacitor voltages is made in Chapter 4.

Unequal loss distribution among the switches of the NPC converter is also a serious drawback of the NPC converter. This problem can result to asymmetrical loss distribution and junction temperatures of the semiconductors [72, 74]. The semiconductor losses can be balanced by replacing the clamping diodes with active

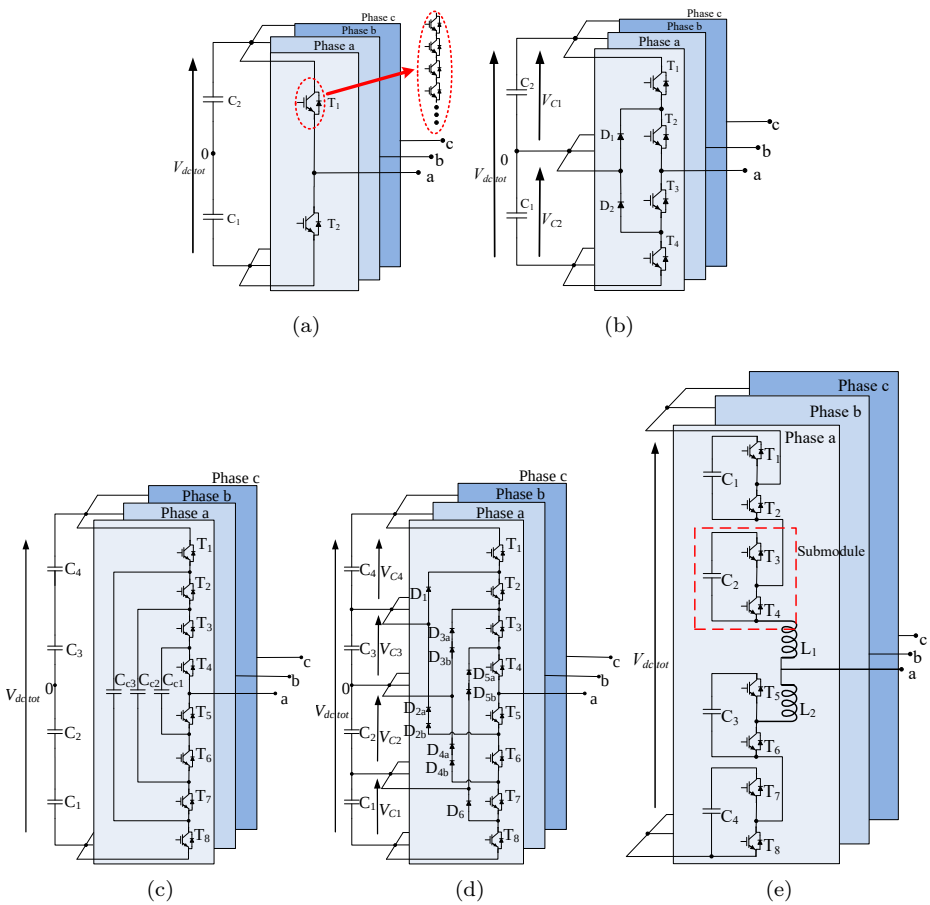


Fig. 3.1: Schematic of (a) 2-level VSC with multiple series connected switches, (b) 3-level NPC, (c) 5-level FC, (d) 5-level NPC and (e) 5-level MMC converters

switches and this modified NPC converter is called active NPC (ANPC) [75]. However, the loss distribution issue has not been covered in this thesis.

3.3 Multilevel PWM Modulation Strategies

The PWM modulator of a three-phase DC/AC converter is responsible for translating the reference voltage signal created by the controller, which can be either open-loop or closed-loop similar to the ones presented previously in Section 2.3, into the corresponding switching function for each active switch of the converter. The most commonly used modulation strategies for the 2LC are the sinusoidal PWM (SPWM) and the Space Vector modulation (SVM). These two methods can be extended for multilevel converters, as described in the following subsections for 5-level and N-level NPC converters.

3.3.1 Sinusoidal PWM

The SPWM technique is built with a sinusoidal reference signal for each phase of the converter running with fundamental frequency which is being compared to a high-frequency triangular carrier. For the 2LC, when the reference signal is higher than the triangular carrier, the upper switch of the corresponding phase leg is conducting, whereas the lower switch is off. Oppositely, when the reference signal is lower than the triangular carrier, the lower switch is conducting and the upper switch is turned off.

This concept can be extended for an N-level converter by using $N-1$ carriers

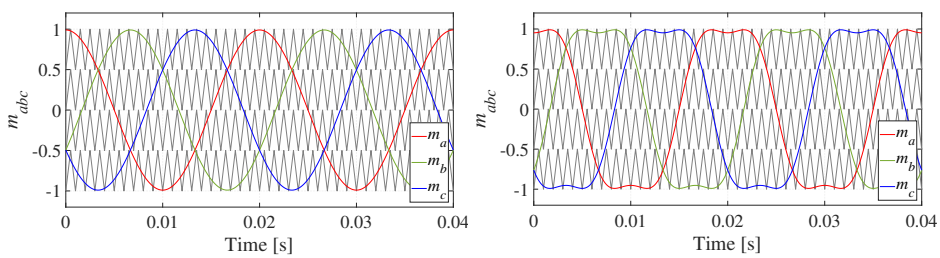


Fig. 3.2: Modulating signals corresponding to (a) conventional 5-level SPWM and (b) third-harmonic injected 5-level SPWM

shifted in amplitude instead of a single triangular carrier. This means that for a 5-level converter 4 carriers are needed, as shown in Fig. 3.2. There are many methods of placing the different carriers depending on their phase sequence, as presented in [76, 77]. The case shown in Fig. 3.2, where all the carriers are in phase is called PH-disposition [76].

The three-phase reference signal is the voltage reference $m_{abc}(t)$ and its peak value is called modulation index and is limited to $\hat{m} \leq 1$. The voltage reference equations are defined as

$$m_a(t) = \hat{m} \cdot \cos(\omega t) \tag{3.1}$$

$$m_b(t) = \hat{m} \cdot \cos(\omega t - \frac{2\pi}{3}) \tag{3.2}$$

$$m_c(t) = \hat{m} \cdot \cos(\omega t - \frac{4\pi}{3}) \tag{3.3}$$

where ω is the fundamental frequency of the converter. The maximum amplitude of the reference phase voltage of the converter for this specific modulation technique is equal to

$$\hat{V}^*_{phmax} = \frac{V_{dc} \cdot (N-1)}{2} \tag{3.4}$$

where V_{dc} is the mean dc voltage of the capacitor cells, which is defined as

$$V_{dc\ tot} = V_{dc} \cdot (N-1) \tag{3.5}$$

and $V_{dc\ tot}$ is the total dc-link voltage of the N-level NPC converter.

It is possible to extend the range of the voltage and utilize better the dc-link by injecting third-harmonic components in the voltage reference. The voltage reference is defined then as [59]

$$m'_a(t) = \frac{3}{2}\hat{m} \cdot \cos(\omega t) - \frac{2}{3}\hat{m} \cdot \cos(\omega t)^3 \tag{3.6}$$

The term at the right side of the above equation is the third-harmonic component of the voltage, which is cancelled out in the L2L voltage. However, the maximum amplitude of the voltage is now extended by almost 15% and the modulation index in (3.6) can get values within $\hat{m} \in [0, \frac{2}{\sqrt{3}}]$ without reaching overmodulation. Therefore, the maximum amplitude of the reference phase voltage of the converter becomes

$$\hat{V}^*_{phmax} = \frac{V_{dc} \cdot (N-1)}{\sqrt{3}} \tag{3.7}$$

The switching sequence for the switches of the 5-level NPC converter shown in Fig. 3.1(d) can be generated based on the algorithm in Table 3.1.

Table 3.1: Switching States for phase A of 5-level NPC Converter with SPWM

Condition	State	Pulses*
$m_a > V_{tr1} \wedge m_a > V_{tr2} \wedge m_a > V_{tr3} \wedge m_a > V_{tr4}$	4	[1 1 1 1 0 0 0 0]
$m_a < V_{tr1} \wedge m_a > V_{tr2} \wedge m_a > V_{tr3} \wedge m_a > V_{tr4}$	3	[0 1 1 1 1 0 0 0]
$m_a < V_{tr1} \wedge m_a < V_{tr2} \wedge m_a > V_{tr3} \wedge m_a > V_{tr4}$	2	[0 0 1 1 1 1 0 0]
$m_a < V_{tr1} \wedge m_a < V_{tr2} \wedge m_a < V_{tr3} \wedge m_a > V_{tr4}$	1	[0 0 0 1 1 1 1 0]
$m_a < V_{tr1} \wedge m_a < V_{tr2} \wedge m_a < V_{tr3} \wedge m_a < V_{tr4}$	0	[0 0 0 0 1 1 1 1]

* for the power switches [T_1 T_2 T_3 T_4 T_5 T_6 T_7 T_8], where 1 = closed, 0 = open

The multicarrier SPWM has the main advantage of being simple and easy to use. However, the main issue with this modulation strategy is the difficulty to obtain the multiple carriers with this specific amplitude shift using a regular MCU. It might be necessary to have an external customized control board which creates the required carriers and generates the suitable switching signal for each power switch of the converter. Also, the Space Vector Modulation (SVM) shown in the next subsection allows more freedom in choosing the switching states, than the SPWM, which can be utilized for control purposes.

3.3.2 Space Vector Modulation

The SVM allows the direct calculation of the switching state for all the switches of the converter having as input the amplitude and the angle of the ac voltage reference. The SVM diagram for a 5-level converter can be derived from the conventional 2-level space vector plane, as can be seen in Figs. 3.3(a)-(b). The N-level SVM has $6(N-1)^2$ triangles and $N^3-(N-1)^3$ voltage vectors [78]. In many points of the space vector plane there are multiple switching states noted the one underneath each other, which are equivalent and create the same L2L voltage. These states are called redundant states and can be utilized for control purposes, such as for balancing the dc-link voltage for the NPC converter.

The switching states can be translated into switching pulses and the conversion is unique for each converter topology. The conversion table for the 5-level NPC converter has been shown in Table 3.1.

The modulation index $\hat{m}$ is defined as follows

$$\hat{m} = \frac{\hat{V}_{ph}^{*}\sqrt{3}}{(N-1)V_{dc}} \overset{N=5}{\Longrightarrow} \hat{m} = \frac{\hat{V}_{ph}^{*}\sqrt{3}}{4V_{dc}} \tag{3.8}$$

It can be seen from the above equation that the maximum voltage obtained by the SVM without overmodulation is equal to the voltage calculated by (3.7) for the SPWM with third-harmonic injection. The vector plane of the SPWM without third-harmonic injection and SVM are shown in Fig. 3.3(c), as well as the overmodulation region for voltages exceeding $\hat{m} = 1$ in (3.8) [79]. The overmodulation region of the SVM has not been studied in this thesis.

The space vector plane is divided into six sectors depending on the angle $\theta \in [0, 2\pi]$ of the reference voltage $\hat{V}^*_{ph}$, as seen in Figs. 3.3(b)-(c). The sector number is determined by

$$Sector = ceil(\theta \cdot 3/\pi) \tag{3.9}$$

The angle θ is rotated based on the sector number as described in Table 3.2, so that the voltage vector is converted into an equivalent vector of Sector 1.

The normalized value of the voltage $\hat{V}^*_{ph}$ can be calculated by

$$v^* = \frac{3\hat{V}^*_{ph}}{2V_{dc}} \tag{3.10}$$

and then it can be transformed into a 60°-coordinate system ($\alpha'\beta'$), as can be seen in Fig. 3.4 [78]

$$\begin{aligned} v^*_{\alpha'} &= v^* \cos\theta' - v^* \sin\theta'/\sqrt{3} \\ v^*_{\beta'} &= v^* \sin\theta' \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{3.11}$$

The space vector $\begin{bmatrix} v^*_{\alpha'} & v^*_{\beta'} \end{bmatrix}$ is now decomposed into the following vectors

$$\begin{bmatrix} V_D \\ V_E \\ V_F \\ V_G \end{bmatrix} = \begin{bmatrix} \text{floor}(v^*_{\alpha'}) & \text{floor}(v^*_{\beta'}) \\ \text{ceil}(v^*_{\alpha'}) & \text{floor}(v^*_{\beta'}) \\ \text{floor}(v^*_{\alpha'}) & \text{ceil}(v^*_{\beta'}) \\ \text{ceil}(v^*_{\alpha'}) & \text{ceil}(v^*_{\beta'}) \end{bmatrix} \tag{3.12}$$

Table 3.2: Sector Selection of SVM

Sector	Angle θ	New θ'	Basic Vector u_a [Phase$_a$ Phase$_b$ Phase$_c$]	Basic Vector u_b [Phase$_a$ Phase$_b$ Phase$_c$]
1	$(0, \pi/3]$	$\theta' = \theta$	[1 0 0]	[1 1 0]
2	$(\pi/3, 2\pi/3]$	$\theta' = -\theta + 2\pi/3$	[1 1 0]	[1 1 0]
3	$(2\pi/3, \pi]$	$\theta' = \theta - 2\pi/3$	[0 1 0]	[0 1 1]
4	$(\pi, 4\pi/3]$	$\theta' = -\theta - 2\pi/3$	[0 0 1]	[0 1 1]
5	$(4\pi/3, 5\pi/3]$	$\theta' = \theta + 2\pi/3$	[0 0 1]	[1 0 1]
6	$(5\pi/3, 2\pi]$	$\theta' = -\theta$	[1 0 0]	[1 0 1]

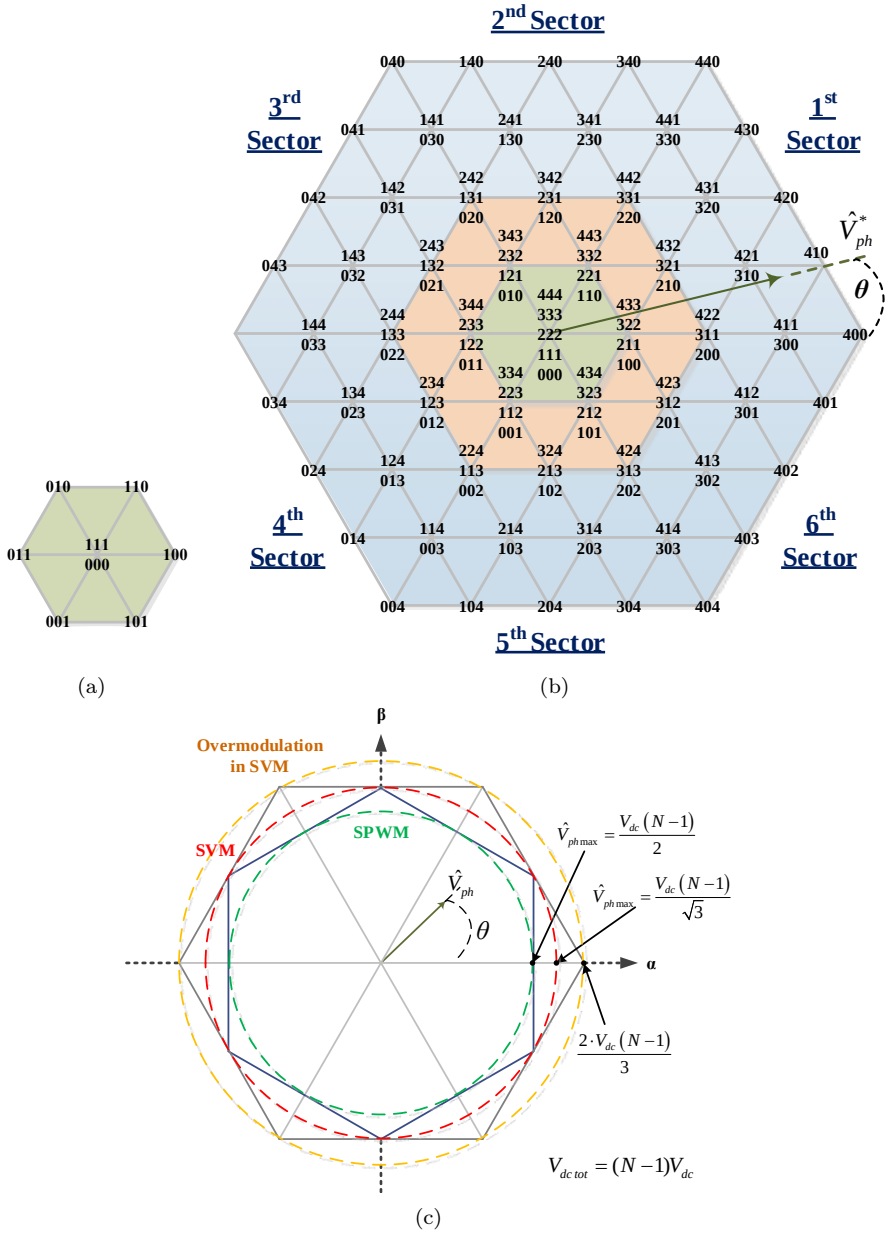
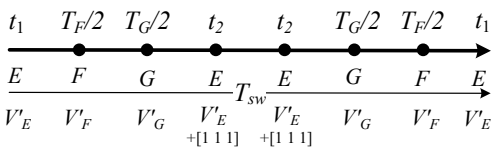


Fig. 3.3: Space vector plane for (a) 2LC and for (b) 5-level VSC; (c) Voltage vector plane indicating the maximum voltage reference for SPWM without third-harmonic injection and SVM

The vectors of (3.12) are multiplied with the basic vectors $[u_a \; u_b]$ of Table 3.2 in order to convert them back into their original sector

$$\begin{bmatrix} V'_D \\ V'_E \\ V'_F \\ V'_G \end{bmatrix} = \begin{bmatrix} V_D \\ V_E \\ V_F \\ V_G \end{bmatrix} \cdot \begin{bmatrix} u_a \\ u_b \end{bmatrix} \tag{3.13}$$

Each edge of the triangles on the space vector plane seen in Fig. 3.3 corresponds to a switching state of the converter in the format $[Phase_A \; Phase_B \; Phase_C]$. The triangles can be divided into lower triangles and upper triangles depending on their orientation and their switching sequence, as shown in Fig. 3.4 where the lower triangle $\overset{\triangle}{DEF}$ is marked with "L" and the upper triangle $\overset{\triangle}{DEF}$ is marked with "U". During each switching period T_{sw}, the triangle within which the voltage vector is located, as defined by the $\alpha'\beta'$-coordinates in (3.11), becomes active. Then, its switching states vary in the sequence which is marked with red arrows in Fig. 3.4. More specifically, for the upper triangles the switching sequence will be



(3.14)

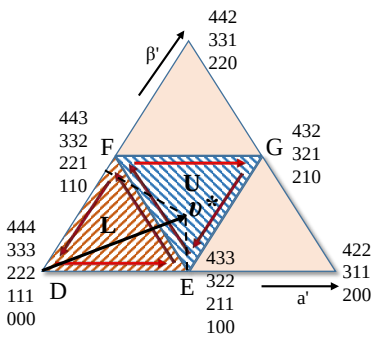
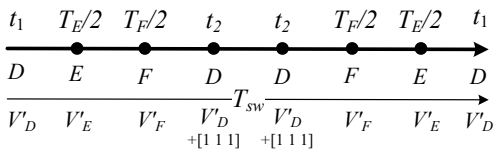


Fig. 3.4: First sector of regions 0 and I indicating the switching states of the lower and upper triangles

and for the lower triangles



(3.15)

SVM - Version 1: There are now two ways to continue with the generation of the PWM pulses for the switches of the N-level converter. The first way is to calculate the the dwell times of each switching state (which is the percentage during the switching period when the specific state is active). For the upper triangle, the dwell times are given by [78]

$$\begin{aligned} T_E &= \big(ceil(v^*_{\beta'}) - v^*_{\beta'}\big)T_{sw} \\ T_F &= \big(ceil(v^*_{\alpha'}) - v^*_{\alpha'}\big)T_{sw} \\ T_G &= T_{sw} - T_E - T_F \end{aligned} \tag{3.16}$$

and for the lower triangles they are

$$\begin{aligned} T_E &= \big(v^*_{\alpha'} - floor(v^*_{\alpha'})\big)T_{sw} \\ T_F &= \big(v^*_{\beta'} - floor(v^*_{\beta'})\big)T_{sw} \\ T_D &= T_{sw} - T_E - T_F \end{aligned} \tag{3.17}$$

$Ceil(x)$ and $floor(x)$ are mathematical operators for rounding towards up and down, respectively. The dwell times t_1 and t_2 in (3.14) and (3.15) are distributed among the redundant states V'_E for the upper and V'_D for the lower triangles

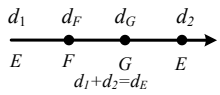
$$\begin{aligned} t_1 + t_2 &= T_E \text{ (for upper triangles)} \\ t_1 + t_2 &= T_D \text{ (for lower triangles)} \end{aligned} \tag{3.18}$$

Since now the dwell times for each switching state of the converter is known, the final step is to translate these switching states into pulses for each switch of the converter. Table 3.1 can be used for that in the case of the 5-level NPC converter.

The main disadvantage of this SVM method is that the final PWM pulses of the switches are calculated directly from the modulation algorithm, which is difficult to be implemented on a standard MCU board. Therefore, this version of the SVM algorithm can be used mainly for computer simulations.

SVM - Version 2: Another version of the N-level SVM is to calculate the duty cycle of the switches instead of the dwell times of each voltage vector. The duty cycles for the switching states of the upper triangles are

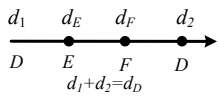
$$\begin{aligned} d_E &= ceil(v^*_{\beta'}) - v^*_{\beta'} \\ d_F &= ceil(v^*_{\alpha'}) - v^*_{\alpha'} \\ d_G &= 1 - d_E - d_F \end{aligned} \tag{3.19}$$



(3.20)

and for the lower triangles

$$\begin{aligned} d_E &= v^*_{\alpha'} - floor(v^*_{\alpha'}) \\ d_F &= v^*_{\beta'} - floor(v^*_{\beta'}) \\ d_D &= 1 - d_E - d_F \end{aligned} \tag{3.21}$$



(3.22)

By using (3.12) and (3.19)-(3.22) the following matrices can be generated for the duty cycle of each converter state

$$d_{state} = \begin{bmatrix} d_{PhaseA\ State1} & d_{PhaseB\ State1} & d_{PhaseC\ State1} \\ d_{PhaseA\ State2} & d_{PhaseB\ State1} & d_{PhaseC\ State1} \\ d_{PhaseA\ State3} & d_{PhaseB\ State1} & d_{PhaseC\ State1} \\ ... & ... & ... \\ d_{PhaseA\ State(N-1)} & d_{PhaseB\ State(N-1)} & d_{PhaseC\ State(N-1)} \end{bmatrix} \tag{3.23}$$

and for the duty cycle of each switch for the upper-leg of an N-level NPC converter

$$d_{sw} = \begin{bmatrix} d_{PhaseA\ switch1} & d_{PhaseB\ switch1} & d_{PhaseC\ switch1} \\ d_{PhaseA\ switch2} & d_{PhaseB\ switch2} & d_{PhaseC\ switch2} \\ d_{PhaseA\ switch3} & d_{PhaseB\ switch3} & d_{PhaseC\ switch3} \\ ... & ... & ... \\ d_{PhaseA\ switch(N-1)} & d_{PhaseB\ switch(N-1)} & d_{PhaseC\ switch(N-1)} \end{bmatrix} \tag{3.24}$$

The switches of the lower-leg of each converter phase are complimentary to the upper switches. The detailed code for generating (3.23) and (3.24) is included in Appendix A.

The duty cycle d_{sw} of (3.24) is sent to the ePWM module of the MCU, as shown in Fig. 3.5, which generates the corresponding PWM signal by comparing the duty cycle with a triangular carrier. For a 3-phase N-level NPC converter $3 \cdot (N-1)$ ePWM modules are needed.

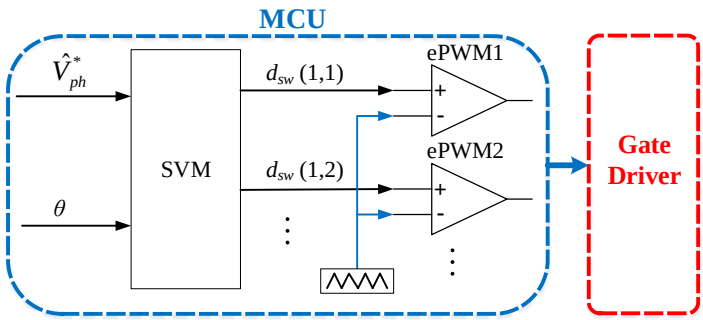


Fig. 3.5: Block diagram of the N-level SVM and the ePWM module of the MCU

Chapter 4

DC-Link Capacitor Voltage Balancing Techniques

The voltage balancing of the dc-link capacitors is a common issue in the NPC converter topologies. Specifically, the 3-level NPC converter has two dc-link capacitors which have normally balanced voltages, when a symmetrical three-phase load is connected at the ac side. They tend to unbalance only at asymmetrical loads and faults. Many control techniques have been proposed in the technical literature for alleviating successfully the above drawback of the 3-level NPC converter and the majority uses zero-sequence voltage for balancing these voltages [42, 59].

The 5-level NPC converter presented in Fig. 3.1(d) may be applied in higher operating voltage applications and the harmonic distortion at the ac output is lower compared to that of the 3-level NPC. However, conventional modulation techniques such as SVM and SPWM cannot be used in this multilevel topology, because the dc capacitor voltage drift is more apparent here, due to the voltage unbalance in the four capacitors that may be observed even with symmetrical three-phase loads. Therefore, a more advanced control method of the dc-link capacitor voltages needs to be implemented as will be shown in the following sections.

This chapter presents simulation results from generator drives with 3-level converters and with 5-level NPC converters for the same operating voltage. The generator of the system is a PMSG, which is controlled with field-oriented control, similarly to Subsection 2.3.3. The grid-side converter uses the voltage-oriented

control scheme of Subsection 2.3.4. The available methods for balancing the dc-link capacitor voltage in the 5-level drives are also presented. A comparison of the performance of the different designs of the generator drives is made in terms of simulated efficiency and voltage/current quality, as well as number of components required for manufacturing the power converters in each case. The design characteristics of the converters are shown in Table 4.1

Table 4.1: Parameters of the simulated 3- and 5-level generator drive

Parameter	Value	Unit
Nominal Power P_{nom}	50	kW
Total dc link voltage	4	kV
Maximum ac L2L voltage V_{gen} (rms)	2.8	kV
Number of MOSFETs (each NPC converter)	24	(3-level drive)
	24	(5-level drive)
Number of clamping diodes (each NPC converter)	12	(3-level drive)
	30	(5-level drive)
V_{DSmax} (SCH2080KE MOSFET)	1.2	kV
I_{Dmax} (for the MOSFET at 25°C)	40	A
R_{DSon} (MOSFET)	80	mΩ
Peak Reverse Voltage V_{RRM} (C3D10170H diode)	1.7	kV
Continuous forward current I_F (for the diode at 25°C)	29	A
Total dc link capacitance	100	μF
Switching frequency f_{sw}	20	kHz

4.1 Electric Drive Design using 3-level NPC Converters

An electric drive design with 3-level NPC converters is described in this section and the schematic diagram of the system is shown in Fig. 4.1. The model and the simulation results of the power converters have been implemented on Matlab/Simulink and PLECS.

The power switches of the converters are the SiC MOSFETs SCH2080KE with breakdown voltage $V_{DSmax} = 1.2$ kV and the clamping diodes are the SiC schottky diodes C3D10170H with peak reverse voltage $V_{RRM} = 1.7$ kV. In order to be able to operate the VSC at the required voltage level, two MOSFETs connected in

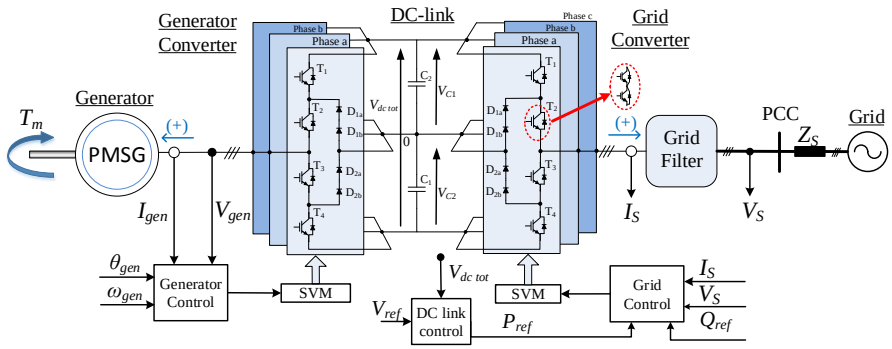


Fig. 4.1: Schematic of 3-level generator drive

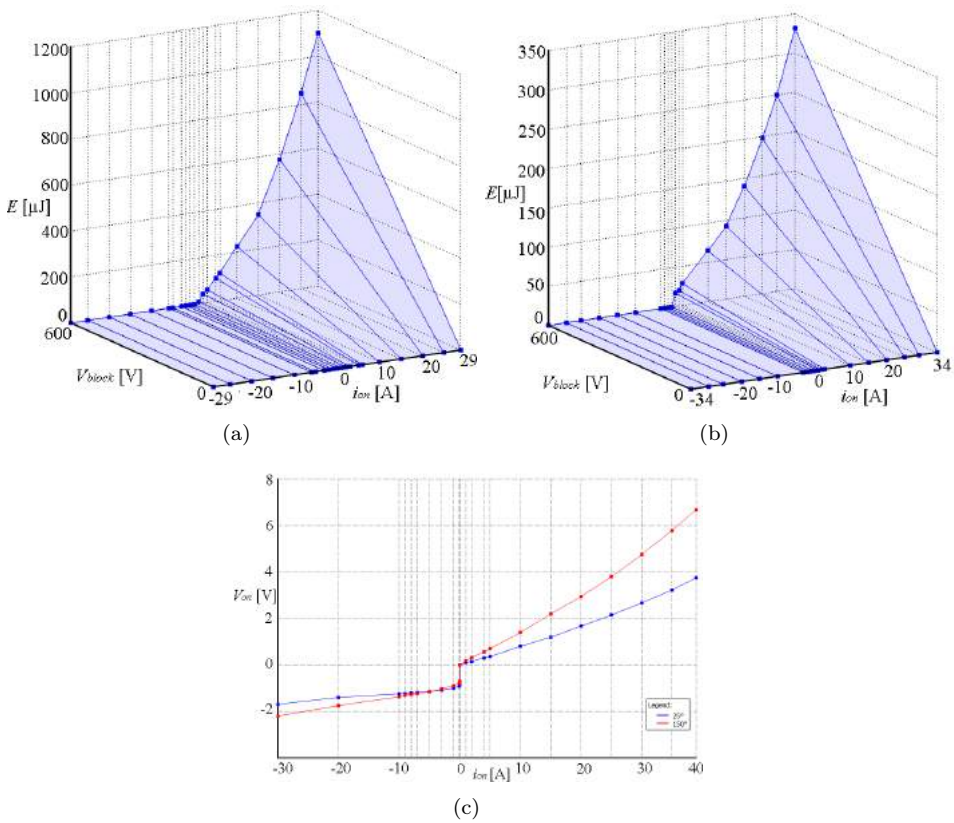


Fig. 4.2: (a) Turn-on losses, (b) turn-off losses and (c) conduction losses of the MOSFET SCH2080KE, as modelled on PLECS

series are used for each power-switch-block and two series-connected clamping diodes for each diode-block of the converter. SiC power switches have been chosen for the simulation analysis of this study, because they have higher voltage capabilities compared to Si switches and also lower losses. The losses of the MOSFETs SCH2080KE and the diodes C3D10170H are modelled according to the information given in their datasheets. The model on PLECS of the switching and conduction losses for the SCH2080KE can be seen in Fig. 4.2.

The following figures present the simulation results of the electric drive. Three operating points of the generator are chosen in order to test the steady-state drive performance at low, medium and high power, as shown in Fig. 4.3(a). These three operating points are at 500rpm/1.5kW, at 2000rpm/10.5kW and at 4000rpm/46kW. The dc-link voltages and the generator current and voltage at the third operating point are shown in Fig. 4.3(c)-(d).

The harmonics of the PMSG terminal voltage and current are analyzed in Fig. 4.4, while the system operates at rated power (operating point 3). The total harmonic distortion of the PMSG current (THD_{IGen}) is equal to 1.8% and the THD of the phase voltage THD_{VphGen} is 54.7%.

The efficiency of the two 3-level VSCs is evaluated on PLECS and the simulation

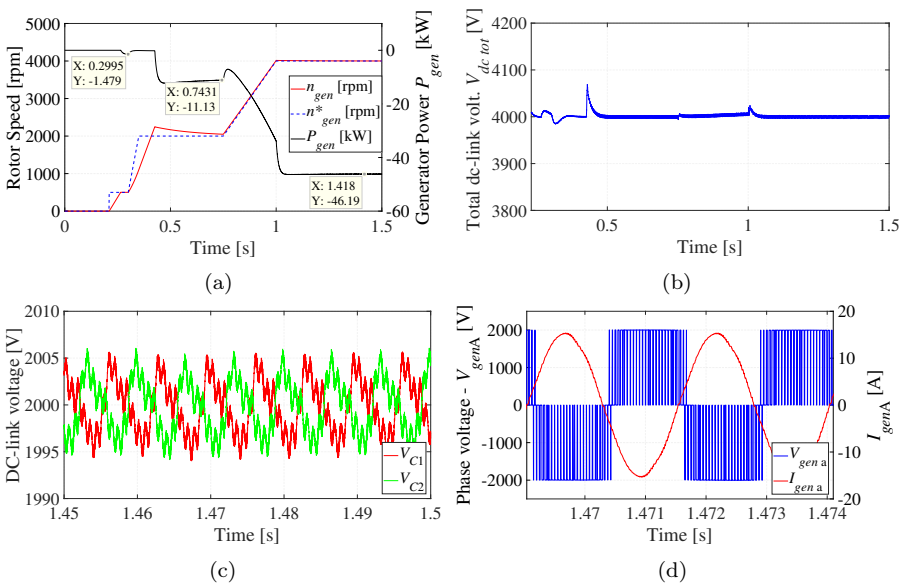


Fig. 4.3: Simulation results of the 3-level generator drive: (a) rotor speed and generator power, (b) total dc-link voltage, (c) dc-link capacitor voltages and (d) phase voltage and current at the generator-side converter

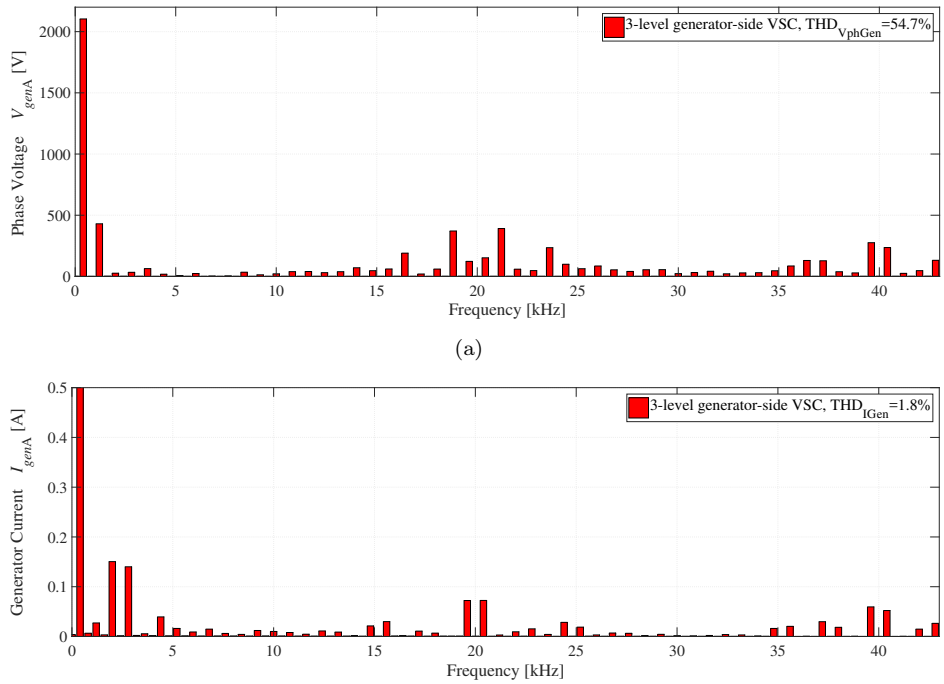


Fig. 4.4: Simulation results of the 3-level generator drive at rated power (4000rpm/46kW): (a) FFT of the PMSG phase voltage and (b) current

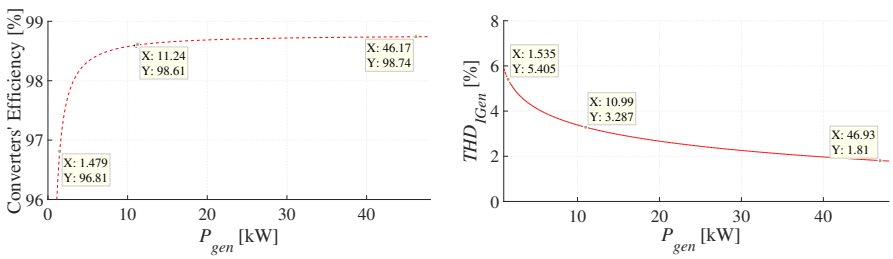


Fig. 4.5: Simulation results of the 3-level (a) power converters' efficiency and (b) THD of the stator current

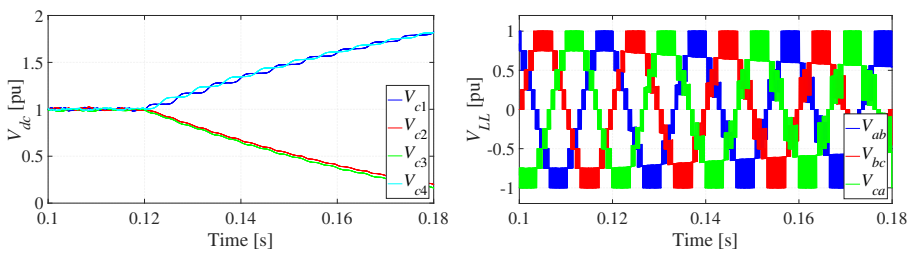
result can be seen in Fig. 4.5. The system efficiency is simulated at these three operating points and the efficiency plot is extracted through curve-fitting.

4.2 Electric Drive Design using 5-level NPC Converters

The electric drive design with 5-level NPC converters is presented in this section. The same power switches and diodes with the ones mentioned in the previous section are used for this drive, namely the 1.2kV SCH2080KE SiC MOSFETs and the 1.7kV C3D10170H SiC diodes.

The main challenge in the control of the 5-level NPC converter is the fact that the converter is naturally unbalanced at the dc-side and, therefore, without any special control of its four dc-link capacitors, their voltage will variate a lot from its set-point [Fig. 4.6(a)]. As can be seen on the right side of Fig. 4.6(b), the unbalancing of the dc link capacitor voltages can create distortions on the ac voltage of the converter and additional harmonics on the ac current. It can also cause the capacitors of the dc-link and the power switches of the converter to exceed their maximum voltage capabilities.

The available methods for balancing the dc link capacitor voltages in a drive with 5-level NPC converters are divided into two types, the software and the hardware based methods. Many control techniques have been developed based on a modified version of the SVM by utilizing the redundant states of the 5-level space vector plane. The control of the redundant states in the SVM can affect the dc link capacitor voltages and at the same time, the requested line-to-line voltage at the ac side is created. However, the effectiveness of purely software based control techniques is limited, since they cannot provide voltage balancing when the converter is operating with resistive power factor and high modulation index,



(a) (b)

Fig. 4.6: 5-Level NPC converter without dc-link balancing control: (a) the four dc-link capacitor voltages and (b) the L2L output voltages

as described in [80]. Therefore, some modifications and operational limitations should be applied on the NPC converter. Specifically, a voltage balancing method in a 5-level NPC converter used in active filters has been proposed in [34]. Similar modulation techniques have been proposed in [35, 36]; however, special design of the passive filter is required in [36] and the balanced operation can be accomplished only with capacitive or inductive power factor in [35]. An SVM-based control strategy for HVDC systems with two B2B-connected 5-level NPC converters has been presented in [37], where the capacitor voltages are balanced effectively. However, the modulation index of both NPC converters has to be the same and this is not possible in an electric drive system with a variable speed generator.

Hardware based voltage balancing techniques usually employ multistage dc/dc converters at the dc-link. These dc/dc converters are bidirectional buck-boost converters that control usually the voltage of the four capacitors in pairs. Various control techniques have been developed, such as in [43–45], which can provide effective voltage balancing in every operational condition of the electric drive. However, their main disadvantages are the increased installation cost and size of the system due to the additional hardware, as well as the reduced system efficiency because of the losses on the dc/dc converter. A balancing converter with reduced number of passive components was proposed in [46], but it requires more power switches and the control is more complicated than the previously mentioned topologies.

This sections presents three alternative ways of balancing the dc-link capacitor voltages:

- A purely software-based balancing control is presented in Subsection 4.2.1, where a new modified SVM algorithm is used for controlling the four capacitor voltages.
- Hardware-based voltage balancing is shown in Subsection 4.2.2 where different types of control for the balancing converter are presented.
- A combination of the hardware and software-based balancing is analyzed in Subsection 4.2.3, which proposes a balancing converter with reduced number of components, utilizing also the SVM for balancing the voltages under certain operating conditions.

4.2.1 SVM-based DC-Link Voltage Balancing [1]

The multilevel SVM has got redundant states at many points of the space vector plane. These redundant states create the same L2L voltage at the ac side of the converter. However, each state has different effect on the capacitor voltages of the dc-side, which can be utilized to balance their voltages. The 5-level SVM diagram of Fig. 3.3 can be divided into three regions depending on the modulation index $\hat{m}$:

- Region 0 ($0 \leq \hat{m} < 0.25$): The modulation index at this region is low and the 5-level NPC converter generates 2-level L2L voltage at the ac side. There are four different redundant states that can control the voltage level of the four dc-link capacitors.
- Region I ($0.25 \leq \hat{m} < 0.5$): The 5-level NPC converter has 3-level L2L voltage at the ac side. As can be seen in Fig. 3.4, there are four different redundant states to be chosen for controlling the switches.
- Region II ($0.5 \leq \hat{m} \leq 1$): The converter has 4-level voltage between $0.5 \leq \hat{m} < 0.75$ and 5-level voltage for $\hat{m} \geq 0.75$. The redundant states in this region are not enough to ensure balanced condition with every load of the converter [80]. Therefore, the switching sequence of the SVM will be modified, as described later in this section.

The structure of an generator drive with two 5-level NPC converters and a PMSG is illustrated in Fig. 4.7. In this subsection a fully software-based voltage balancing technique is shown and the first step is to split the dc-link capacitors between the two converters, as shown in Fig. 4.7. The NPC converters are connected to each other only at the top and the bottom joint-points (points 5 and 1, respectively) of the dc-link. The parallel connection of the two groups of capacitors (C_a and C_b) will ensure that they will have the same voltage. The middle point of the two converters can be connected to the ground or the neutral point of the system. The two converters operate at different modulation indexes and a common dc-link capacitor bank would have caused interferences that would have affected the balancing of the dc-link voltages. The configuration presented here decouples the generator-side converter of the drive from the grid-side converter allowing individual voltage balancing of the two groups C_a and C_b of the dc capacitors. The

[1] More details can be found:
G. Mademlis and Y. Liu, "DC Link Voltage Balancing Technique Utilizing Space Vector Control in SiC-based Five-Level Back-to-Back-Connected NPC Converters", in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, September 23-27, 2018.

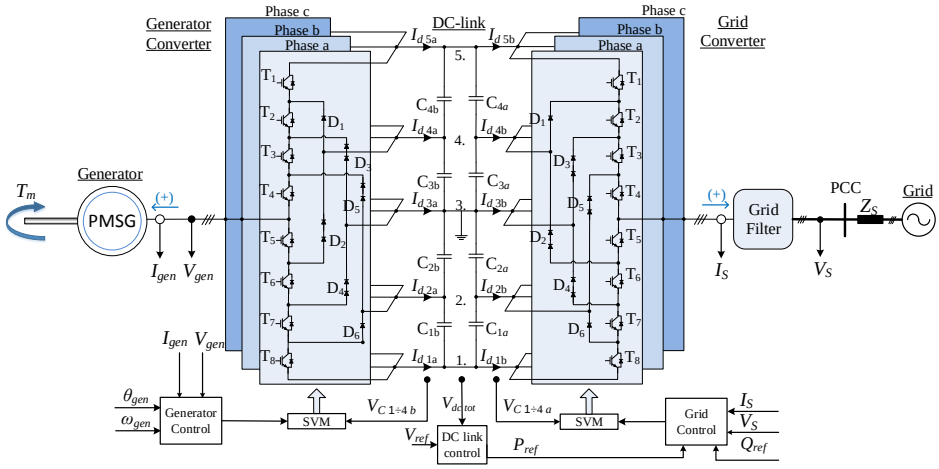


Fig. 4.7: Structure of a generator drive with two 5-level NPC converters connected B2B using modified SVM for voltage balancing of the dc-link

total dc-link voltage of the drive $V_{dc\ tot}$ is still controlled by the dc-link controller of the grid converter (Subsection 2.3.4).

The SVM diagram for a 5-level converter can be seen in Fig. 4.8(a) and the modulation strategy described in this section is identical for controlling both NPC converters of the electrical machine drive. The grid-side converter operates at an almost constant modulation index $\hat{m}_{grid} \leq 1$ in region II, whereas, the generator-side converter has variable modulation index $\hat{m}_{gen}$, since the speed and the voltage of the generator are changing. The variable v^* in Fig. 4.8 is the normalized reference voltage of the converter, as calculated by (3.10), and for a 5-level converter it varies from 0 to 4.

Voltage balancing algorithm for regions 0 & I: The switching states and the switching sequence of the SVM on the triangles of the space vector plane are indicated with arrows in Fig. 4.8(b). When the NPC converter operates in regions 0 and I, there are four available redundant switching states in each switching cycle that can easily be assigned to each of the four dc-link capacitors in order to charge them or discharge them whenever it is necessary.

An example is shown in Fig. 4.9, where the effect of the redundant states on the state of charge of the dc-link capacitors is demonstrated. The circuit diagram of the NPC converter is shown there, when the redundant states {100}/{211}/{322}/{433} from Sector 1 of the SVM plane are active. The switches which are active in each

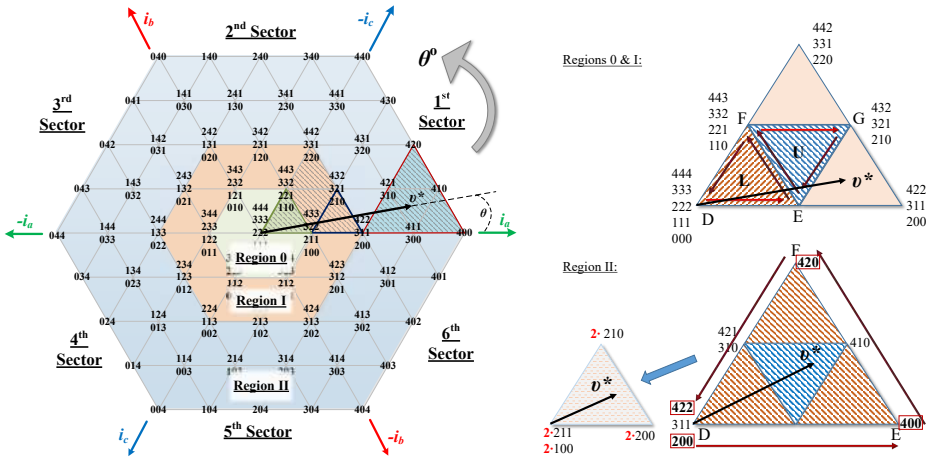


Fig. 4.8: Five-level SVM diagram: (a) space vector plane indicating the regions and sectors; (b) first sector of of the SVM plane indicating the switching sequence

case are shown with thick black lines, while the inactive switches are marked with grey line. Specifically, when the instantaneous phase A current i_a is positive in Fig. 4.9(a), the state {100} discharges the capacitor C_1. Oppositely, if the current i_A is negative, the capacitor C_1 gets charged. Similarly, in Fig. 4.9(b) the state {211} discharges the capacitor C_2 when $i_a > 0$. In Fig. 4.9(c) the state {322} discharges the capacitor C_3 and in Fig. 4.9(d) the state {433} discharges the capacitor C_4. The L2L voltage at the ac side of the NPC converter is the same in all the four cases.

The three-phase current at the ac side of the NPC converters and the four capacitor voltages are measured and compared with each other in order to choose the correct redundant states from the space vector diagram. The sign of the ac current affects also the charging state of the dc-link capacitors, as has been shown in Fig. 4.9. The current that affects the capacitor voltages at each time instant depends on the angle θ of the reference voltage v^* and the proper balancing current i_{bl} is chosen according to Table 4.2, as referenced from [40].

It was mentioned in (3.18) that the dwell times t_1 and t_2 are distributed among the redundant states V'_E for the upper and V'_D for the lower triangles. The standard way is to distribute them evenly, in order to minimize the switching losses of the converter and this method from now on will be called as "standard SVM" [78]. However, it is possible by varying these variables to control the capacitor voltages,

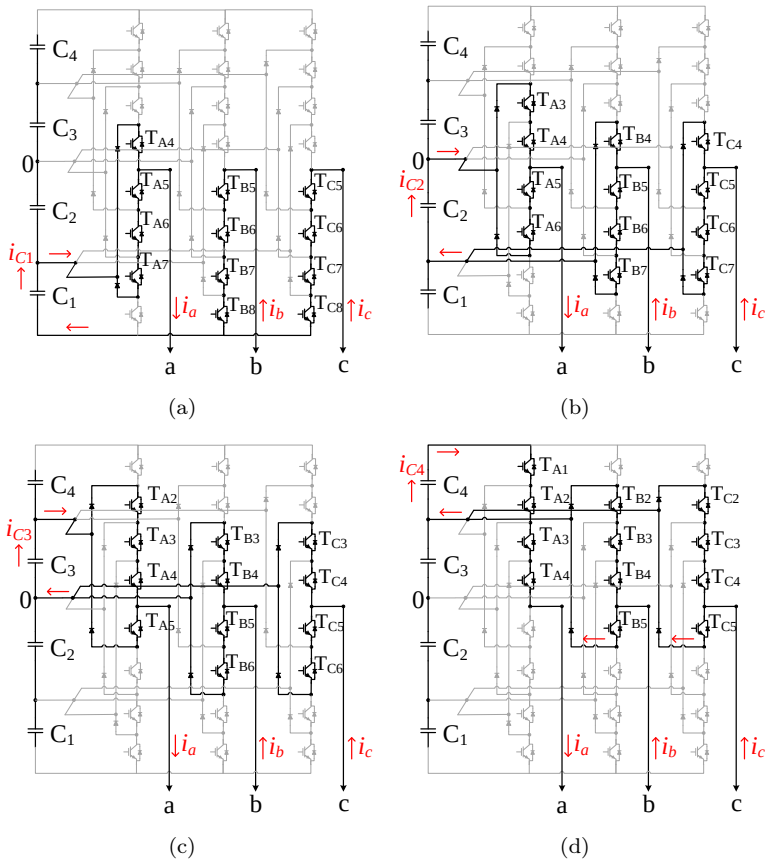


Fig. 4.9: Circuit diagram of the 5-level NPC converter when the switching state (a) {100}, (b) {211}, (c) {322} and (d) {433} is active

Table 4.2: Balancing Current [40]

Angle θ	Balanc. current i_{bl}
(-$\pi/6$, $\pi/6$]	i_a
($\pi/6$, $\pi/2$]	$-i_c$
($\pi/2$, $5\pi/6$]	i_b
($5\pi/6$, $7\pi/6$]	$-i_a$
($7\pi/6$, $3\pi/2$]	i_c
($3\pi/2$, $11\pi/6$]	$-i_b$

Table 4.3: Voltage balancing algorithm for region 0 (lower triangles)

i_{bl}	Condition	Switching sequence	t_1	t_2
>0	$V_{Cmax} = V_{C1}$	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/4$	$T_D/4$
>0	$V_{Cmax} = V_{C2}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/4$	$T_D/4$
>0	$V_{Cmax} = V_{C3}$	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/4$	$T_D/4$
>0	$V_{Cmax} = V_{C4}$	$\{V_D + [3\ 3\ 3]; V_E + [3\ 3\ 3]; V_F + [3\ 3\ 3]; V_D + [4\ 4\ 4]\}$	$T_D/4$	$T_D/4$
<0	$V_{Cmin} = V_{C1}$	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/4$	$T_D/4$
<0	$V_{Cmin} = V_{C2}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/4$	$T_D/4$
<0	$V_{Cmin} = V_{C3}$	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/4$	$T_D/4$
<0	$V_{Cmin} = V_{C4}$	$\{V_D + [3\ 3\ 3]; V_E + [3\ 3\ 3]; V_F + [3\ 3\ 3]; V_D + [4\ 4\ 4]\}$	$T_D/4$	$T_D/4$

* V_{Cmax}, V_{Cmin} are the maximum and minimum capacitor voltage, respectively

Table 4.4: Voltage balancing algorithm for region I (lower triangles) [34]

i_{bl}	Condition 1	Condition 2	Switching sequence	t_1	t_2
>0	$V_{Cmax1} = V_{C1}$	-	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/3$	$T_D/6$
>0	$V_{Cmax1} = V_{C2}$	$V_{Cmax2} = V_{C1}$	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/6$	$T_D/3$
>0	$V_{Cmax1} = V_{C2}$	$V_{Cmax2} = V_{C3}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/3$	$T_D/6$
>0	$V_{Cmax1} = V_{C3}$	$V_{Cmax2} = V_{C2}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/6$	$T_D/3$
>0	$V_{Cmax1} = V_{C3}$	$V_{Cmax2} = V_{C4}$	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/3$	$T_D/6$
>0	$V_{Cmax1} = V_{C4}$	-	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/6$	$T_D/3$
<0	$V_{Cmin1} = V_{C1}$	-	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/3$	$T_D/6$
<0	$V_{Cmin1} = V_{C2}$	$V_{Cmin2} = V_{C1}$	$\{V_D; V_E; V_F; V_D + [1\ 1\ 1]\}$	$T_D/6$	$T_D/3$
<0	$V_{Cmin1} = V_{C2}$	$V_{Cmin2} = V_{C3}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/3$	$T_D/6$
<0	$V_{Cmin1} = V_{C3}$	$V_{Cmin2} = V_{C2}$	$\{V_D + [1\ 1\ 1]; V_E + [1\ 1\ 1]; V_F + [1\ 1\ 1]; V_D + [2\ 2\ 2]\}$	$T_D/6$	$T_D/3$
<0	$V_{Cmin1} = V_{C3}$	$V_{Cmin2} = V_{C4}$	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/3$	$T_D/6$
<0	$V_{Cmin1} = V_{C4}$	-	$\{V_D + [2\ 2\ 2]; V_E + [2\ 2\ 2]; V_F + [2\ 2\ 2]; V_D + [3\ 3\ 3]\}$	$T_D/6$	$T_D/3$

* V_{Cmax1}, V_{Cmax2} are the highest and the second highest capacitor voltage.
* V_{Cmin1}, V_{Cmin2} are the lowest and the second lowest capacitor voltage.

as shown in Table 4.3 for the lower triangles of region 0 and in Table 4.4 for region I (which is referenced from [34]). Similar methodology is followed for deriving the switching states for the upper triangles.

Voltage balancing algorithm for region II: The redundant states in the triangles of region II are not enough to keep all the capacitor voltages balanced, as can be seen in Fig. 4.8(b). More specifically, there are only two available redundant states on the D edge of the outer lower triangles in region II, the {300}

Table 4.5: Voltage balancing algorithm for region II (lower triangles)

i_{bl}	Condition	Switching sequence	t_1	t_2
>0	$V_{C1}+V_{C2}>V_{C3}+V_{C4}$	2·{$V_D;V_E;V_F;V_D+[1\ 1\ 1]$}	$T_D/3$	$T_D/6$
>0	$V_{C1}+V_{C2}<V_{C3}+V_{C4}$	2·{$V_D;V_E;V_F;V_D+[1\ 1\ 1]$}	$T_D/6$	$T_D/3$
>0	$V_{C1}+V_{C2}>V_{C3}+V_{C4}$	2·{$V_D;V_E;V_F;V_D+[1\ 1\ 1]$}	$T_D/6$	$T_D/3$
>0	$V_{C1}+V_{C2}<V_{C3}+V_{C4}$	2·{$V_D;V_E;V_F;V_D+[1\ 1\ 1]$}	$T_D/3$	$T_D/6$

and {411}, and three redundant states on the D edge of the inner lower triangles, the {200}, {311} and {422}.

One way to overcome this issue is to treat the 5-level NPC converter as if it was a 3-level converter. In this case, the capacitor voltages are controlled in pairs, $V_{C1}+V_{C2}$ and $V_{C3}+V_{C4}$, and the redundant states are enough to balance them effectively. This control strategy has been proposed in [34, 81] for single NPC converters and it is applied here for a drive with two B2B NPC converters. The switching states that generate current at the clamping points 2 and 4 of the NPC converters (Fig. 4.7) are not used in this SVM scheme (such as the states {300}, {311} and {411}) and the currents I_{d2a}, I_{d4a}, I_{d2b} and I_{d4b} are zero. Therefore, there is no voltage drift between the capacitor voltages of each pair. The resultant redundant states marked with a red box in Fig. 4.8(b) are utilized to keep the average current of the middle point 3 equal to zero, in order to balance the two pairs of the capacitor voltages. A more detailed view of the effect of these switching states on the charging state of the dc-link capacitors and the dc-side currents can be seen in Fig. 4.10.

The conversion from 5-level operation into 3-level operation is implemented by converting the large triangle on the bottom side of Fig. 4.8(b) into the equivalent triangle on the left side. Therefore, the reference voltage vector of the SVM in (3.10) is now modified as follows

$$v^{*'}=\frac{v^*}{2}=\frac{3\hat{V}^*_{ph}}{4V_{dc}} \tag{4.1}$$

The modified reference voltage $v^{*'}$ is now used in the rest of the equations (3.11)-(3.13) in order to calculate the space vectors and the dwell times. It can be seen in Fig. 4.8(b) that there are two available redundant states in each triangle, which are selected as shown in Table 4.5.

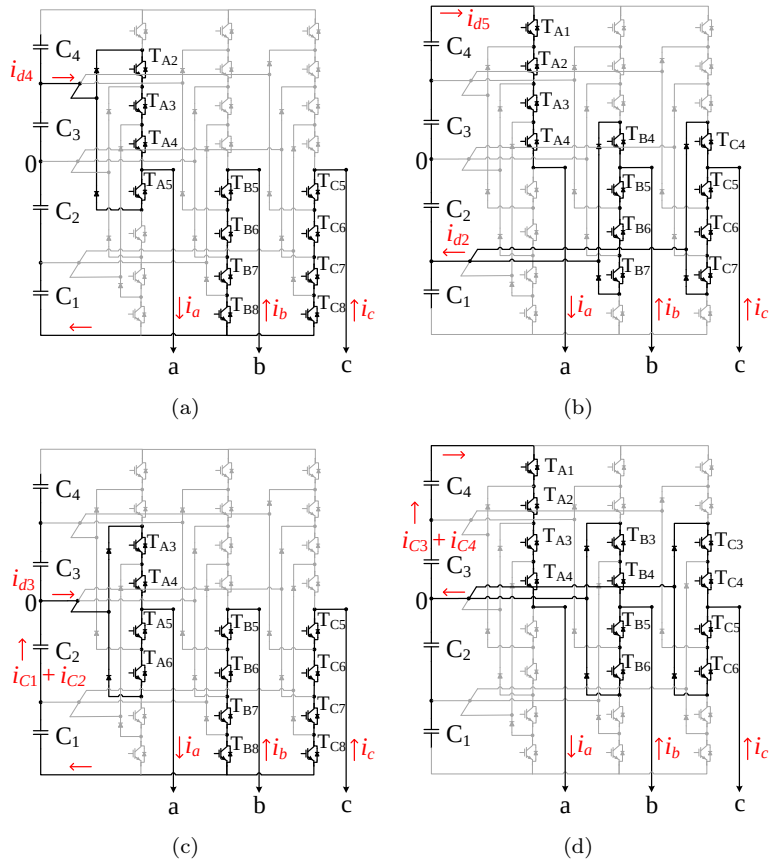
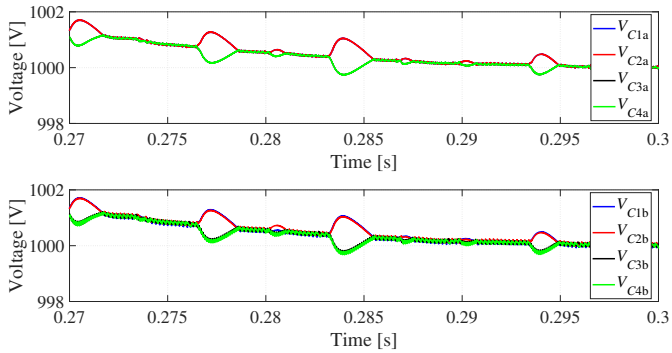
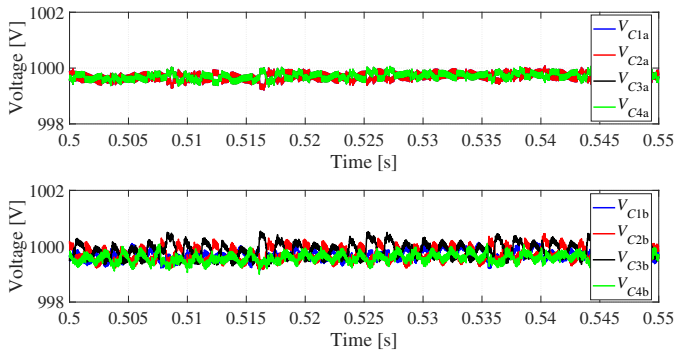


Fig. 4.10: Circuit diagram of the 5-level NPC converter when the following switching states are active: (a) {300}, (b) {411}, (c) {200} (⇒ the C_1 and C_2 are getting discharged) and (d) {422} (⇒ the C_3 and C_4 are getting discharged)

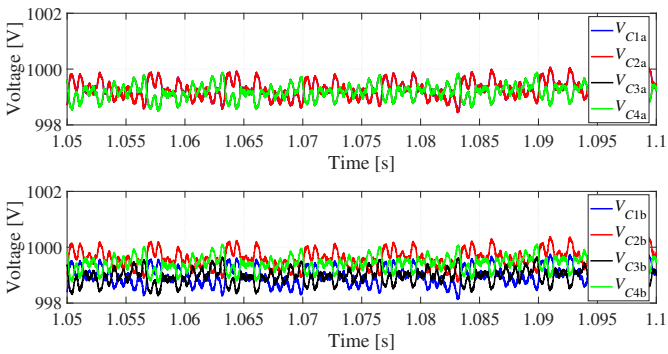
Simulation results: The generator drive of Fig. 4.7 has been simulated on Matlab/Simulink. The parameters of the system are the same with the ones for the 3-level drive reported in Table 4.1. The grid-side converter operates at constant modulation index which is at region II of the SVM diagram. However, many operating points of the generator are simulated in order to investigate all the three regions of the SVM for the generator-side converter. The same three operating points shown in Fig. 4.3(a) (500rpm/1.5kW operating at region 0, 2000rpm/10.5kW at region I and 4000rpm/46kW at region II) have been simulated also here.



(a)



(b)



(c)

Fig. 4.11: Simulation results of the dc-link voltages when the generator-side 5-level NPC converter operates in (a) region 0, (b) region I and (c) region II of the SVM plane

The reference voltage of each capacitor bank is equal to $4000/4 = 1000$V. As can be seen in Fig. 4.11, the capacitor voltages remain balanced in all the operating regions of the system (the blue curve of V_{C1a} is overlapped by the red one of V_{C2a} and the black curve of V_{C3a} is overlapped by the green curve of V_{C4a}). The $V_{c1a} \div V_{c4a}$ are the capacitor voltages of the grid-side NPC converter and the $V_{c1b} \div V_{c4b}$ are at the generator-side. The voltages in Fig. 4.11(a) are slightly declining because the converter has not fully reached steady state yet.

The L2L voltage of the generator terminals can be seen in Fig. 4.12, where the 2-level voltage of region 0 is in Fig. 4.12(a) and the 3-level voltage of regions I and II is in Figs. 4.12(b)-(c). It can be seen here that although the generator-side converter operates with high modulation index in region II, the voltage still has 3 levels, due to the voltage balancing algorithm described previously. This is also the main disadvantage of the SVM-based voltage balancing method, because the converters are not possible to generate 5-level voltage, although the voltage stress on each MOSFET is still equal to $V_{dc\ tot}/4$.

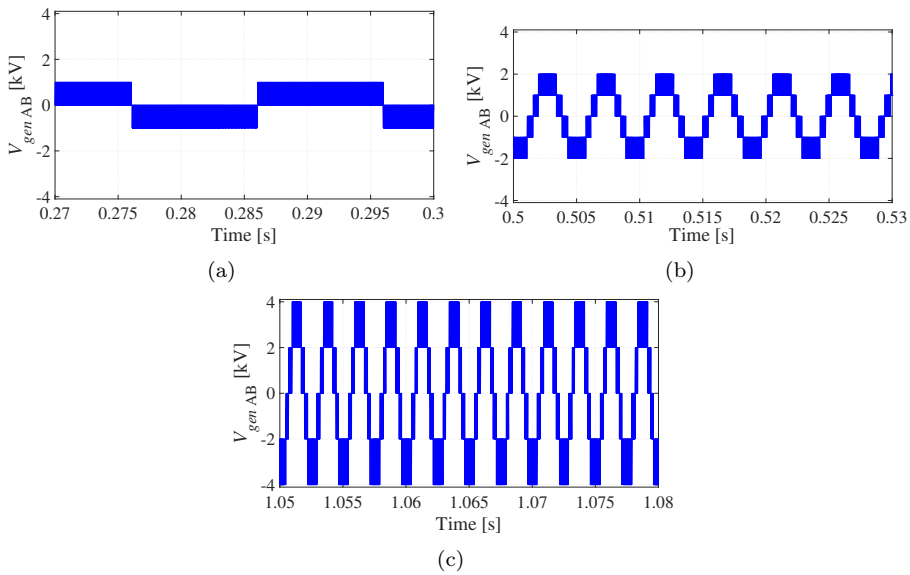


Fig. 4.12: Simulation results of the PMSG L2L voltage when the generator-side 5-level NPC converter operates in (a) region 0, (b) region I and (c) region II of the SVM plane

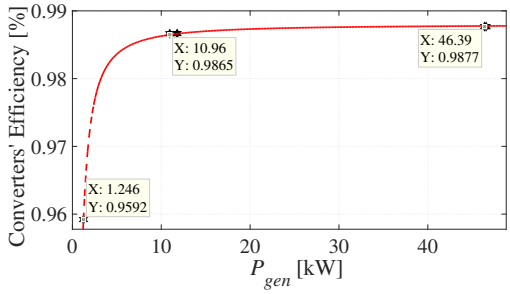


Fig. 4.13: Simulation results of the 5-level power converters' efficiency when SVM-based dc-link voltage balancing is used

4.2.2 Hardware-based DC-Link Voltage Balancing [2]

The dc-link voltage balancing of NPC-based electric drives can be implemented with specially designed dc/dc converters placed in parallel to the dc-link, as described in [44, 48, 82, 83] and shown in Fig. 4.14. The dc/dc converters can be controlled with constant duty cycle in open-loop mode or they can have a closed loop control system. Both ways are described in this subsection.

Open-loop Control of the Balancing Converter

The dc/dc converter balances the capacitor voltages in pairs and, therefore, three stages are needed for a 5-level drive. Each converter stage consists of two power switches with antiparallel diode and an inductor. The maximum instantaneous voltage applied across each switch is equal to

$$v_{T_{bk}} = v_{Ck} + v_{C(k+1)} \tag{4.2}$$

which is two times the rated voltage of the switches of the NPC converter. As can been seen in Fig. 4.14, the dc/dc converter has been modelled here with two series-connected switches in each switch position. Instantaneous currents and voltages are symbolized here with lowercase letters (i and v respectively), while average quantities are shown with capital letters (I and V).

The two switches T_{bk} and $T_{bk'}$ are complimentary to each other and the duty

[2] More details can be found:
G. Mademlis and Y. Liu, "Feed-forward Control of Active Voltage Balancing Converter in Electric Drive with Five-Level NPC Converters", in *Proc. of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, September 23-27, 2018.

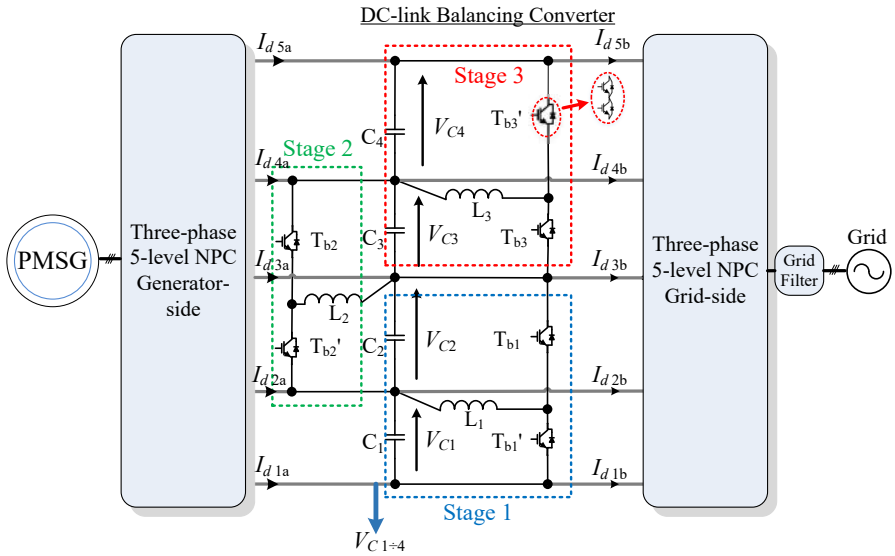


Fig. 4.14: Power circuit of the the dc/dc converter that balances the dc-link of a 5-level drive when only hardware balancing is used

cycle of the k-stage power switch is defined as [84]

$$d'_k = 1 - d_k = \frac{v_{C(k+1)}}{v_{Ck} + v_{C(k+1)}} \tag{4.3}$$

When the capacitor voltages of that converter stage are equal

$$v_{Ck} = v_{C(k+1)} \overset{(4.3)}{\Rightarrow} d_k = d'_k = 0.5 \tag{4.4}$$

Therefore, by applying a constant duty cycle equal to 0.5 on all the power switches, the capacitor voltages will have the same voltage.

The operation of the converter can be explained by the graphs in Fig. 4.15. The first stage of the balancing converter is shown as an example and the other two stages operate similarly:

- When $V_{C1} > V_{C2}$ [Fig. 4.15(a)]
  1. the capacitor C_1 charges the inductor and the current flows through the switch T'_{b1} during half of the switching period.
  2. During the other half period, the switch T'_{b1} is off and the T_{b1} is on. However, the current does not pass through the switch T_{b1} but through its antiparallel diode and the energy of the inductor is finally transferred to the capacitor C_2.

- When $V_{C1} < V_{C2}$ [Fig. 4.15(b)]
  1. the capacitor C_2 charges the inductor and the current flows through the switch T_{b1} during half of the switching period.
  2. During the other half period, the switch T_{b1} is off and the T'_{b1} is on. The current now passes through the antiparallel diode of T'_{b1} and the energy of the inductor is transferred to the capacitor C_1.

The average currents of the switches in Fig. 4.15 are defined as

$$\begin{aligned} I_{TB1} &= I_{L1} d_{b1} \\ I_{TB1'} &= I_{L1}(1 - d_{b1}) \end{aligned} \tag{4.5}$$

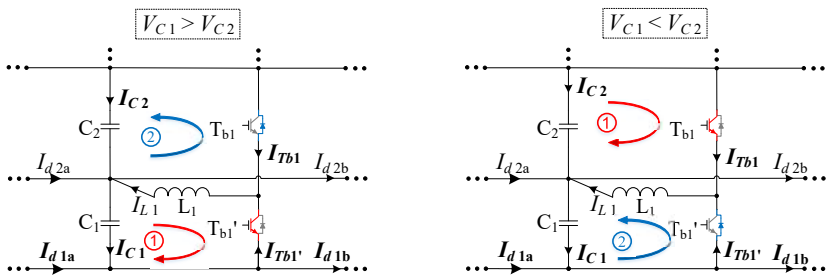
The following current and voltage equations exist in the circuit of Fig. 4.15

$$i_{TB1'} = i_{C1} + i_{d1a} - i_{d1b} \tag{4.6}$$

$$v_{TB1} = v_{C2} - v_{L1} \tag{4.7}$$

Since the antiparallel diodes of the switches conduct almost half of the time, it is recommended to use power MOSFETs for this converter, due to their ability to have reverse conduction current [85]. MOSFETs allow positive, as well as negative current to flow through their N-channel, when the gate-source voltage is positive. The N-channel of the MOSFET has lower conduction and switching losses compared to the antiparallel diode or the body diode. Therefore, by forcing the current to flow always through the switch even when it is negative, the losses of the balancing converter can be reduced.

It is very important to define a large enough dead-time between the two complimentary switches of each stage of the balancing converter. Otherwise, there is the



(a) (b)

Fig. 4.15: Power circuit of the first stage of the dc link balancing converter when (a) the capacitor C_2 and (b) when C_1 are being charged

danger of short-circuiting the dc-link capacitors and creating large current spikes which could destroy the switches.

The open-loop control of the balancing converter offers a simple and effective way of balancing the dc-link capacitor voltages of the 5-level drive. However, since there is no feedback of the actual voltage of the capacitors, there will be steady state error between the four voltages due to the losses and the voltage drop of the system. The most serious drawback of this control method is that there is no active control of the current that flows through the dc inductors and it is actually the resultant of the voltage difference between the capacitors. Therefore, in the case of a step-change of the load of the NPC converters, high current overshoots and oscillations are expected on the inductors, which cannot be suppressed, as seen in Fig. 4.16.

Experimental results of the generator drive, which will be presented in the next Chapter 5, are shown in Fig. 4.16. Specifically, the total dc-link voltage of the system $V_{dc\ tot}$ is 670V and a step-change of the generator's reference speed is applied at 0.49s. The current of the NPC converter I_{gen} increases due to the acceleration of the machine and the sudden current increase creates a larger drift

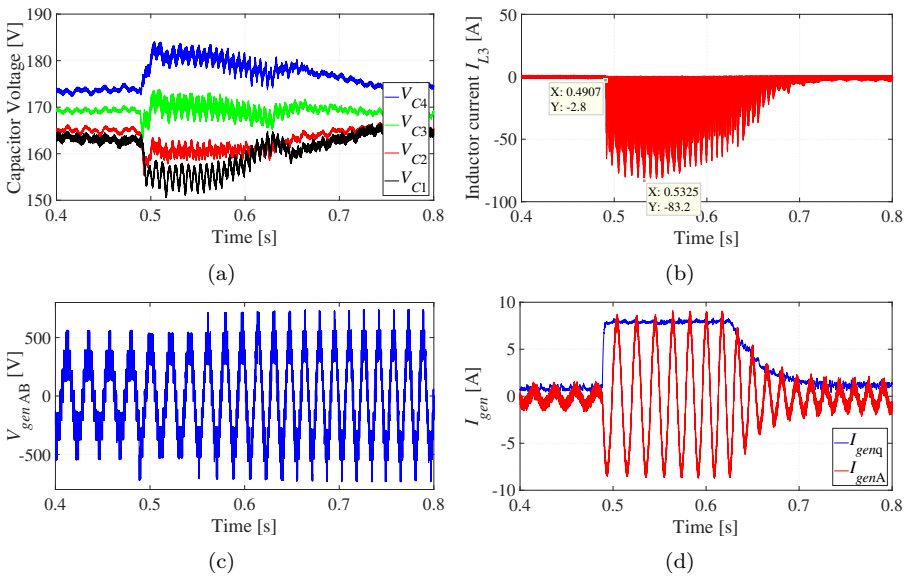


Fig. 4.16: Experimental results of the 5-level generator drive with a step-change of the PMSG speed from 450 rpm to 650 rpm when the dc-link is balanced with open-loop controlled balancing converter and with $V_{dc\ tot} = 670$V

of the capacitor voltages in Fig. 4.16(a). The current of the dc-inductors increases as well trying to eliminate the voltage drift and can reach high values as shown in Fig. 4.16(b) for the I_{L3} which has peak of 83A. In that particular case, the I_{L3} became so high, because the inductor core got saturated.

Feedforward-based Closed-loop Control of the Balancing Converter

Each stage k of the balancing converter is regulated by separate controllers consisting of two cascaded control loops. The primary control loop is the voltage controller which creates the current reference that balances the two capacitor voltages. The secondary control loop is the current controller, which has as output the duty cycle d_k of the balancing converter. The voltage and current control loops can be made of PI controllers, as described in [44]. A feedforward-based control has been developed for the specific dc/dc converter in [83, 84] which uses only proportional controllers and offers faster dynamic response. It has been adapted in this thesis in order to be applied on the balancing converter of a generator drive with B2B-connected NPC converters.

The control structure of the dc/dc converter is presented in Fig. 4.17. The P_V and P_I are the proportional gains of the voltage and current controllers, respectively. The control of the first stage of the dc/dc converter can be described as follows.

The reference capacitor currents of each stage I_C^* are given by the error between the two capacitor voltages, after being amplified by the proportional gain of the voltage controller P_V. The reference current of the switch is calculated by using (4.6), with feed-forward of the dc-link currents. The reference inductor current is finally calculated with (4.5). The d_{b1} in (4.5) is the duty cycle of the switch T_{b1} during obtained from (4.3) during the previous sample period of the controller.

Input of the current controller is the error between the reference and actual inductor current. The current error is amplified by the gain P_I and becomes the reference average voltage of the inductor V_L^*. Then, the reference voltage of the switch V_{TB}^* is calculated by using (4.7). During steady state operation of the balancing converter, the average voltage of the inductor V_{L1} is equal to 0 and, therefore, the (4.7) becomes

$$V_{TB1} \approx V_{C2} \tag{4.8}$$

The reference duty cycle of switches in the fist stage of the converter are calculated with (4.3) and (4.8) as

$$d_{b1}^* \approx \frac{V_{C1}}{V_{TB1}^* + V_{C1}} \tag{4.9}$$

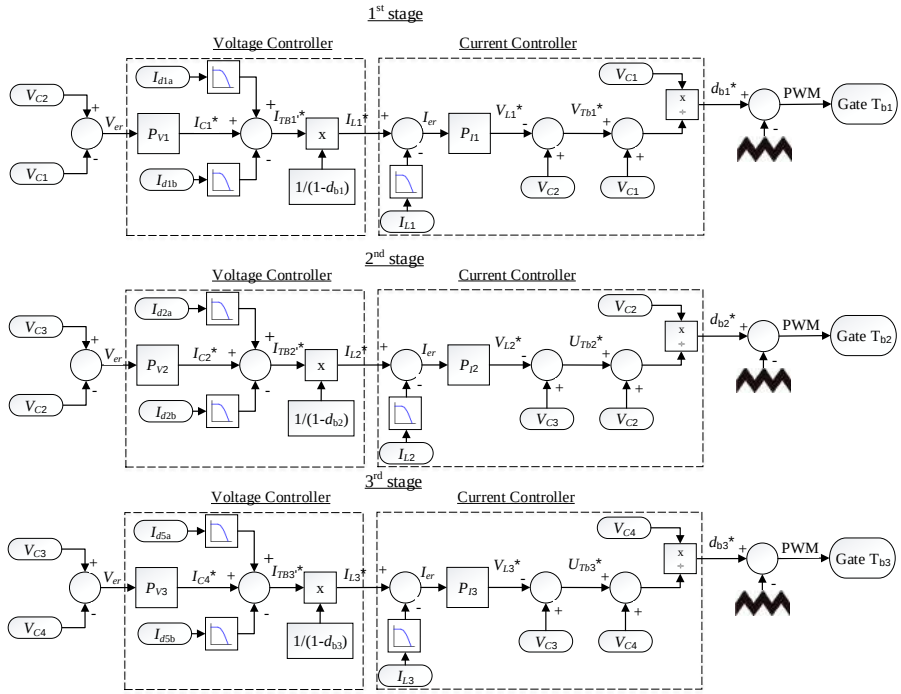


Fig. 4.17: Block diagram of the feed-forward control system of the dc-link balancing converter

For the implementation of the feed-forward control scheme measurements of the four capacitor voltages, the three inductor currents (I_{L1}, I_{L2} and I_{L3}) and the dc-link currents (I_{d1a} up to I_{d5a} and I_{d1b} up to I_{d5b} shown in Fig. 4.7) are required. The current signals are filtered with LPF in order to suppress high order harmonics. It is possible to reduce the number of measurements by estimating the dc currents of the NPC converters. The dc currents are proportional to the ac output currents and the duty cycle of the NPC converters. A similar study has been conducted in [45] for single phase 5-level NPC converter. The dc-current estimation algorithm for a 5-level 3-phase NPC converter can be described as follows for the phase a of the grid-side NPC converter

$$
\begin{aligned}
I_{d5b_a} &= I_{S_\alpha}[d_{G1_\alpha} + d_{G2_\alpha} + d_{G3_\alpha} + d_{G4_\alpha}] \\
I_{d4b_a} &= I_{S_\alpha}[(1 - d_{G1_\alpha}) + d_{G2_\alpha} + d_{G3_\alpha} + d_{G4_\alpha}] \\
I_{d3b_a} &= I_{S_\alpha}[(1 - d_{G1_\alpha}) + (1 - d_{G2_\alpha}) + d_{G3_\alpha} + d_{G4_\alpha}] \\
I_{d2b_a} &= I_{S_\alpha}[(1 - d_{G1_\alpha}) + (1 - d_{G2_\alpha}) + (1 - d_{G3_\alpha}) + d_{G4_\alpha}] \\
I_{d1b_a} &= I_{S_\alpha}[(1 - d_{G1_\alpha}) + (1 - d_{G2_\alpha}) + (1 - d_{G3_\alpha}) + (1 - d_{G4_\alpha})]
\end{aligned}
\tag{4.10}
$$

where I_{S_α} is the grid line current of phase α and d_{G1_α} is the duty cycle of the switch T_{G1} at the phase α of the grid-side NPC converter. The current estimation of the other two phases, b and c, can be obtained by similarly utilizing the (4.10). It should be noted that the currents given by (4.10) are the average values and not the instantaneous currents. The final values of the dc currents are calculated by summing the contributions of the three phases

$$\begin{aligned} I_{d5b} &= I_{d5b_a} + I_{d5b_b} + I_{d5b_c} \\ I_{d4b} &= I_{d4b_a} + I_{d4b_b} + I_{d4b_c} \\ I_{d3b} &= I_{d3b_a} + I_{d3b_b} + I_{d3b_c} \\ I_{d2b} &= I_{d2b_a} + I_{d2b_b} + I_{d2b_c} \\ I_{d1b} &= I_{d1b_a} + I_{d1b_b} + I_{d1b_c} \end{aligned} \tag{4.11}$$

The dc currents of the machine-side NPC converter I_{d1_a} up to I_{d5_a} are calculated similarly to equations (4.10) and (4.11) by using the machine-side line currents I_{gen} instead of the grid current I_S in (4.10).

The system shown in Fig. 4.14 has been simulated using Matlab/Simulink and the simulation results are shown in the following figures. The variation of the dc-link capacitor voltages is shown in Fig. 4.18(a) and they are balanced with small steady state error. This verifies the effectiveness of the control system described in the previous section. The total dc-link voltage is controlled by the grid-side converter and has mainly remained unaffected by the individual capacitor voltages, as can be seen in Fig. 4.18(b). The estimated and measured currents at the dc side of the grid NPC converter are presented in Fig. 4.19. The estimated currents are calculated by (4.10)-(4.11) and are the average values of the measured currents.

The harmonic analysis of the generator phase voltage and current is shown in

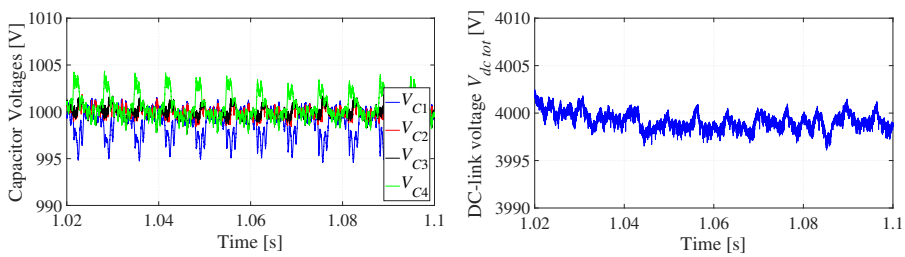


Fig. 4.18: Simulation results of (a) the dc-link capacitor voltages and (b) the total dc-link voltage when feedforward-based voltage balancing is used

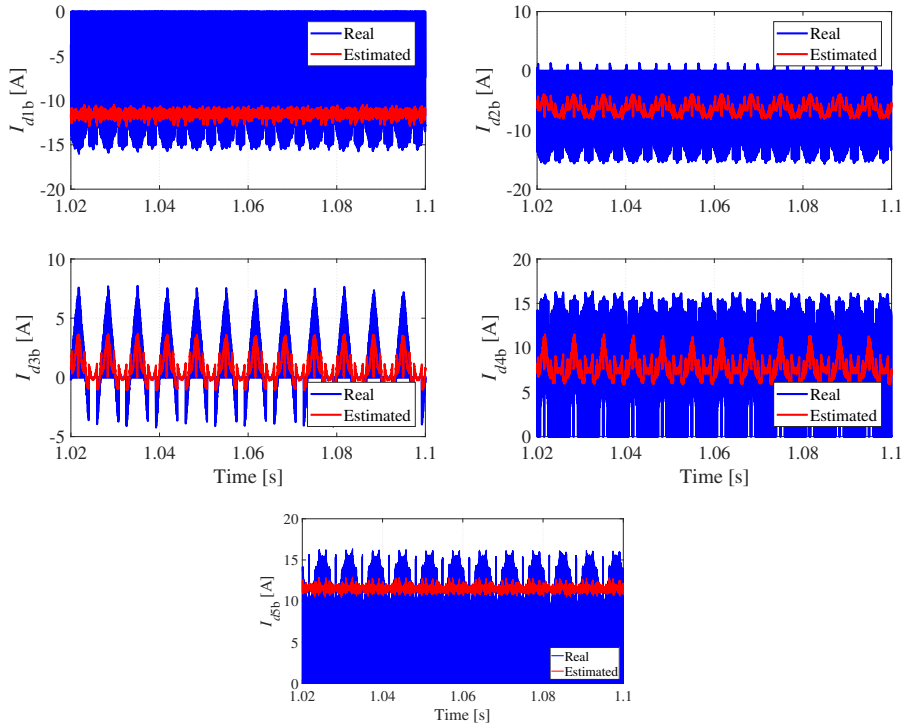
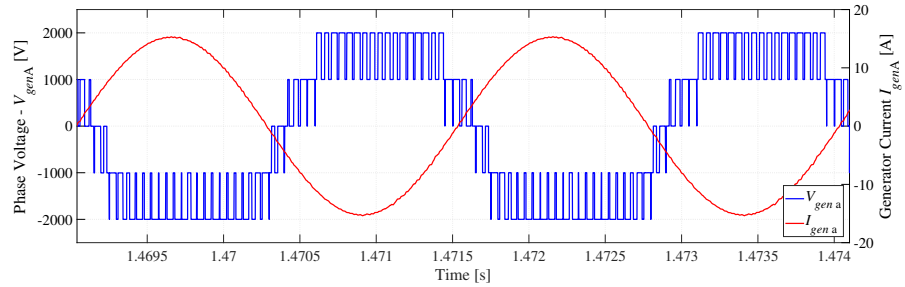
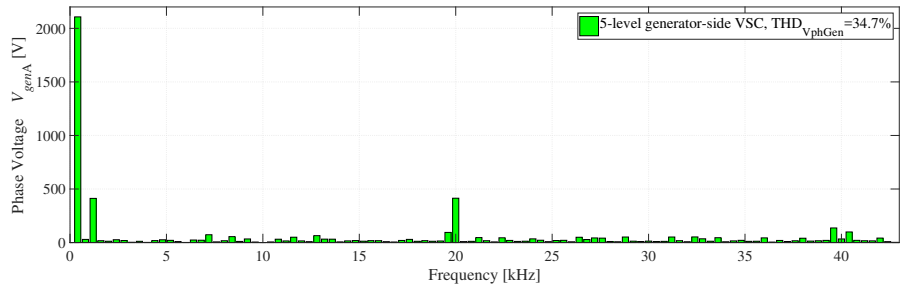


Fig. 4.19: Simulation results of the dc currents of the grid-side NPC converter at rated power of the generator (4000rpm/46kW) when feedforward-based voltage balancing is used

Fig. 4.20, when the system has rated power (4000rpm/46kW). The THD of the voltage is 34.7%, while the THD of the current is 0.6%. Both results are improved compared to the harmonic analysis of the 3-level drive in Fig. 4.4 that has shown a phase voltage THD equal to 54.7% and current THD of 1.8% .



(a)



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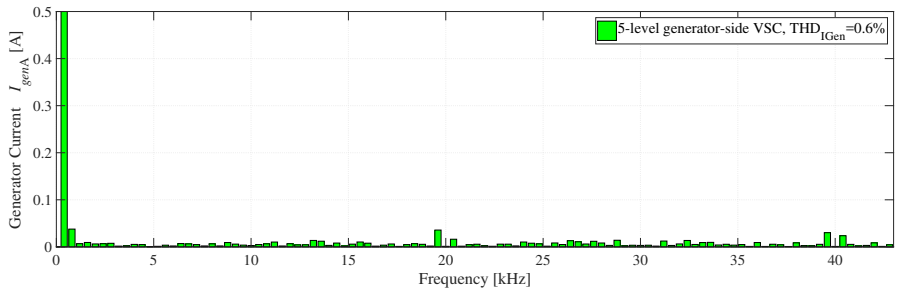


(c)

Fig. 4.20: Simulation results of the 5-level generator voltage and current at rated power (4000rpm/46kW) when hardware voltage balancing is used: (a) time-domain analysis and (b)-(c) FFT of the voltage and current

4.2.3 Combined Hardware and SVM-based Voltage Balancing

The SVM-based voltage balancing method works effectively when the 5-level NPC converters operate at regions 0 and I of the SVM plane and the modulation index is lower than 0.5. For higher modulation index, the SVM algorithms needs to be modified, as shown in Subsection 4.2.1, and the ac output voltage of the

NPC converters cannot have 5-level shape, since some specific switching states of the converter are not used. On the other hand, the hardware-based voltage balancing works effectively under every operating condition, but an additional dc/dc converter needs to be installed.

One solution would be to combine the advantages of both balancing techniques, the hardware- and the SVM-based, and build a new balancing converter with reduced number of components which will operate only when the redundant states of the NPC converter are not enough to keep the dc-link capacitors under control. The circuit diagram of the generator drive studied here is shown in Fig. 4.21. Compared to the diagram in Fig. 4.14, the balancing converter which is used here has only two stages, regulating the capacitors C_1-C_2 and C_3-C_4. The voltage balancing strategy depends on the modulation index. The grid side converter is operating at an almost constant modulation index $\hat{m}_{grid} \geq 0.5$, whereas, the generator side converter has variable modulation index $\hat{m}_{gen}$. The control structure of the whole electric drive system (an NPC converter connected to the grid and another converter at the generator side of the power plant) can be summarized in the flowchart of Fig. 4.22.

When the modulation index $\hat{m}_{gen}$ is at Regions 0 and I, the capacitor voltages

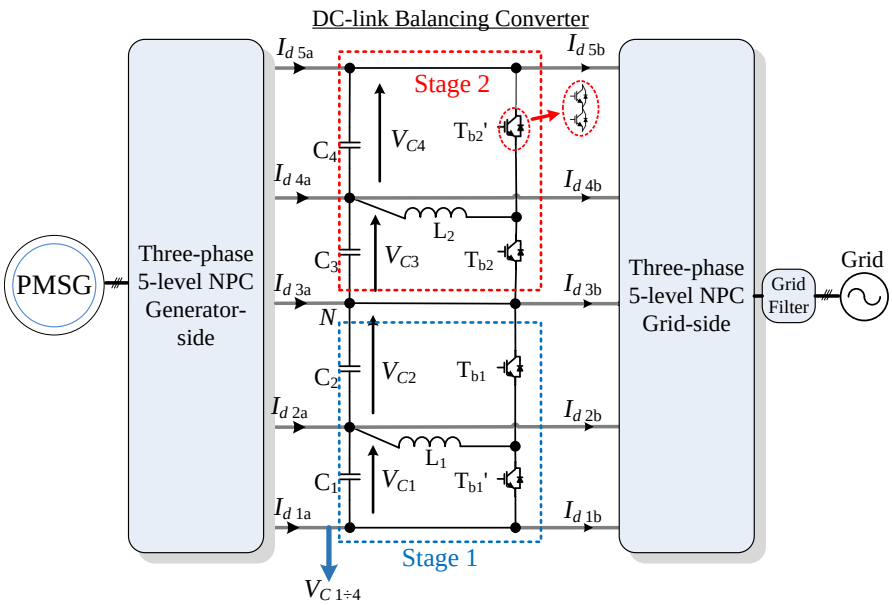


Fig. 4.21: Power circuit of a five-level generator drive with a 2-stage voltage balancing converter at the dc-link

are balanced only from the control system at the generator-side converter and the grid converter is controlled with conventional SVM [78]. The balancing converter does not need to operate during that time.

When the generator-side NPC converter is operating at the Region II of the space vector plane, the redundant states are not enough to control the capacitor voltages and at the same time to keep 5-level voltage. Therefore, the dc/dc converter at the dc link is activated to keep the V_{C1} equal to V_{C2} and the V_{C3} equal to V_{C4}. The voltage potential at the middle of the dc-link is controlled by injecting zero-sequence voltage as follows.

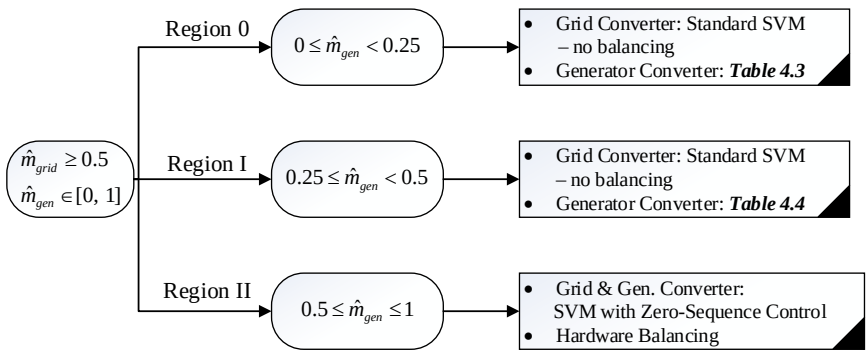


Fig. 4.22: Flowchart of the dc-link voltage balancing algorithm in a 5-level generator drive

Zero-sequence injection control (Region II)

The currents of the middle clamping point I_{d3a} and I_{d3b}, are controlled by the SVM-blocks of both NPC converters using zero-sequence injection. Zero-sequence injection is used in 3-level NPC converters for balancing their capacitor voltages in [59] and can also be applied here using a similar control structure. Fig. 4.23 shows the block diagram of the zero-sequence controller that has been implemented for both space vector modulators of the back-to-back connected NPC converters. Input of the zero-sequence injection controller is the voltage difference between the two upper capacitors C_3 and C_4 and the two lower capacitors C_1 and C_2. This error voltage contains 3rd harmonic components, which are filtered by a notch filter tuned at three times the fundamental frequency. The filtered signal is multiplied with the sign of the active power that goes through the NPC converter. Then, the error voltage goes through a PI controller and the output parameter k is the input of the SVM.

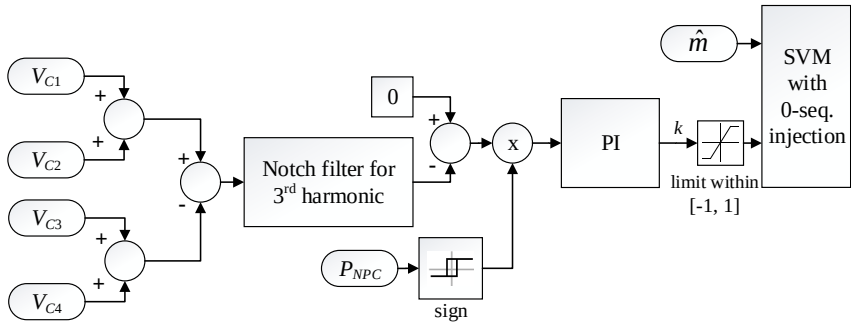
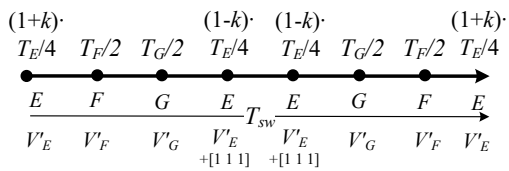


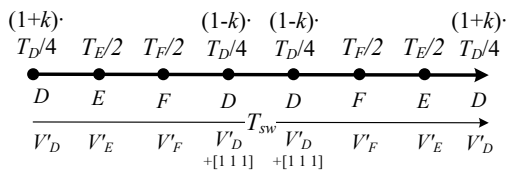
Fig. 4.23: Block diagram of the zero-sequence controller for regulating the potential at the middle point of the dc-link

The switching sequence of the upper triangles from (3.14)-(3.15) for both NPC converters changes to



(4.12)

and for the lower triangles



(4.13)

The combination of software and hardware control techniques presented here ensures that the additional dc/dc converter is used only when the redundant states of the SVM are not enough for effective dc capacitor voltage balancing. Therefore, the efficiency of the whole system will be theoretically improved compared to the fully hardware-based balancing of Subsection 4.2.2. This needs to be verified experimentally, which is planned to be implemented in the future. Also, the number of components at the dc/dc converter is reduced, because zero-sequence injection is used for the control of the middle point current instead of using a 3rd stage of the balancing converter. Four and five-level ac voltage is also created when the NPC converters operate at high modulation index, without the limitations imposed in Subsection 4.2.1, where the voltage has got maximum three levels.

Simulation results of this voltage balancing technique have been presented in [3] .

4.2.4 Summary

This chapter has presented the design process and the simulation analysis of 3-level and 5-level generator drives. Drives with 5-level converters can have operating voltage up to 4 times higher than the systems with 2LCs, without using series-connected power switches. A further advantage of the 5-level converters is the decrease of the voltage and current harmonics at their ac side compared to converters with less number of levels, as shown by the FFT analysis in Figs. 4.4 and 4.20. The generator current and phase voltage THD at the 3-level drive is simulated to be 1.8% and 54.7%. The THD of the current decreases to 0.6% and of the voltage to 34.7% for the same operating conditions. A more detailed comparison of the harmonics and losses in generator drives with 2-, 3- and 5-level converters has been implemented during this thesis work and has been published in [86].

The voltage drift of the dc-link capacitors is a serious problem in electric drives with 5-level NPC converters that can be solved by various voltage balancing strategies. Three effective voltage balancing methods have been described in Section 4.2 providing also simulation results on a sample 50kW generator drive for each of these methods. Each technique has its own advantages and disadvantages, as described below.

Firstly, it has been shown that the redundant states on the 5-level space vector plane of the NPC converter's modulator can be utilized to balance the four dc-link voltages. This method is an extension of a similar control technique that is also applied on the 3-level NPC converters, where zero sequence voltage is used to control the two capacitor voltages of that topology. However, contrarily to the 3-level converter, the redundant states are not enough to control all the four capacitor voltages when the 5-level drive operates at the outer regions of the space vector plane. One way to overcome this problem, is to switch the converter in 3-level mode avoiding the use of some switching states, as shown in Subsection 4.2.1. The capacitor voltages are kept balanced in that case, but the ac voltage of the converter has maximum 3-levels, which results to increased harmonics at the ac side. The main advantage of this balancing technique is that it does not

[3] G. Mademlis, Y. Liu, and N. Saadat, "Combined voltage balancing techniques of the DC link in five-level medium voltage NPC back-to-back converters for offshore renewable generation", in *Proc. 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017.

require any additional hardware for the control of the dc-link voltages, since the suitable selection of the redundant states of the converter regulates them.

Another way of balancing the dc-link voltages is the use of dedicated dc/dc converters. This method is the most expensive, since it requires the use of an additional converter and that increases the cost, losses and complexity of the system. The dc/dc converter can either be controlled open-loop by just switching with constant duty cycle without any feedback of the capacitor voltages or a more complicated feedforward-based control system can be used. The open-loop control has the simplest structure, while the closed-loop controller has better dynamic performance and balances the capacitor voltages with smaller steady state error. The SVM of the NPC converters is not utilized in this case for the dc-link control, which makes the redundant states of the NPC converters available to be used in other control strategies, such as in loss and noise reduction the AC/DC converter [87].

The third method proposed in this thesis is the combination of the two previous voltage balancing techniques. The SVM-based voltage balancing method is clearly advantageous when the converter operates with low modulation index, while it should be avoided when high modulation index is used. The dc/dc balancing converter can be activated in this case, while in all the other cases it can remain idle. Zero-sequence injection can also be used to limit the number of components of the balancing converter, as described in Subsection 4.2.3. This method is the most complicated out of the three previously mentioned, since it includes the control for the additional dc/dc converter as well as the optimal selection of the redundant states of the modified SVM. However, the 5-level drive can operate without any limitation, unlike in the first method. Also, the additional hardware needed is less compared to the second method.

The advantages and disadvantages of the voltage balancing techniques that have been discussed previously are summarized in the following Table 4.6. The comparison of the system complexity in the table refers to the complexity of the control in each voltage balancing scheme. The third method has the most advantages, because it balances successfully the dc-link capacitor voltages, without increasing considerably the cost of the system, while having higher complexity in the control and the hardware design. However, the optimal choice of the voltage balancing technique depends on the needs of the application where the drive is intended to be used.

Table 4.6: Summary of DC-link Voltage Balancing Techniques

Balancing method	Complexity	Cost	AC Harmonics
SVM-based (Subsection 4.2.1)	↗	0	↗ (3-level voltage)
Hardware-based with open-loop control (Subsection 4.2.2)	0	↗↗	0
Hardware-based with closed-loop control (Subsection 4.2.2)	↗	↗↗	0
Combination of SVM and hardware (Subsection 4.2.3)	↗↗	↗	0

Chapter 5

Design and Testing of Medium Voltage Generator Drive

5.1 System Overview

The prototype power conversion system developed during this study has two identical 5-level NPC converters placed at the generator- and the grid-side of the drive and are responsible for controlling the generator and for the synchronization to the grid, respectively (Fig. 5.1). There is a third converter connected in parallel to at the dc link of the whole structure, which is responsible for balancing the voltages of the dc link capacitors. The positive direction of the currents at the output of the converters is marked with blue arrows on the schematic. The connections at the ac side of the converters between the PMSG and the generator-side VSC and between the transformer and the grid-side VSC are implemented using 3.3-4.2kV litz-wire cables from Nexans with conductor cross section 16mm^2 (product code 10148758).

The switches of the power converters are controlled by gate drivers, which send suitable signals to the gate of the switches, when they need to turn on and off. The gate drivers receive that control signal from an MCU, as seen in Fig. 5.1. The MCU and the gate drivers are electrically isolated from each other and this isolation is implemented by transferring the PWM signals to the gate drivers through fibre optic cables.

Measurements of the currents and voltages at various points of the power conversion

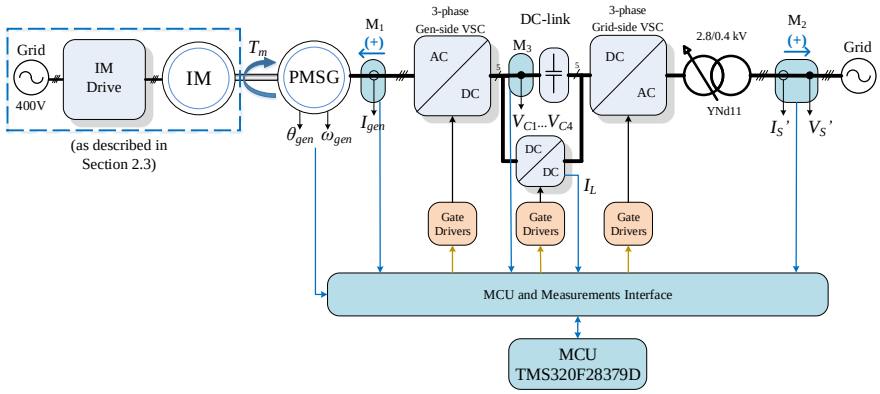


Fig. 5.1: Schematic of the prototype medium voltage power conversion system including the power converters and the control boards

system are needed in order to control the converters. The generator and grid currents and voltages are measured with the measurement boxes M_1 and M_2. The voltage of the capacitors at the dc-link is also measured with another measurement box M_3. The measured signal is sent to the MCU through the "MCU and Measurements Interface". Three MCU boards from Texas Instruments with product code TMS320F28379D are used to control the two NPC converters and the dc-link balancing converter.

The following Section 5.2 describes the design process of the power converters and the measurement devices and Section 5.3 presents experimental results of the multilevel generator drive.

5.2 Prototype PMSG Drive Design

The design parameters of the prototype low-scaled power conversion system is given in Table 5.1. The system described here is a low-power-scaled version, but with higher operating voltage, of the 500 kW TUSK system shown in Table 2.1. The prototype presented in this chapter has been used in the thesis as a proof of concept for the proposed multilevel generator drive and for verifying the developed control strategies described previously in Chapters 3 and 4. The dimensions and the power density of the converters have not been optimized in order to allow easier accessibility and measurements with the oscilloscope.

SiC Power switches are used for the converters of the prototype. SiC has ad-

Table 5.1: Parameters of the developed multilevel power conversion system

Parameter	Value	Unit
Nominal Power P_{nom}	50	kW
Maximum dc-link voltage V_{dctot}	4	kV
DC-link capacitance	295	μF
Inductors of the balancing conv. L_1, L_2, L_3	4	mH
Maximum ac L2L voltage (rms)	2.8	kV
Phase current (rms)	10.31	A
Switching frequency f_{sw}	20	kHz

vantageous performance in terms of lower switching losses and higher operating temperatures compared to the Si power switches [88, 89]. Thus, SiC switches allow the construction of more compact converters due to the higher switching frequency and the resultant decrease of the grid filter size, as well as lower cost for cooling, because of the lower switching losses and higher allowed temperatures. The main disadvantage of these switches is that they have at the moment higher purchase cost compared to the Si IGBTs and MOSFETs. However, their cost is constantly declining, as the SiC technology becomes more mature.

Suitable application regions for each of the available semiconductor devices are shown in Fig. 5.2, namely SiC power switches can substitute IGBTs in applications with power between 1-500 kW and switching frequency higher than 10 kHz. In applications with even higher power the power switches made of Si are expected to

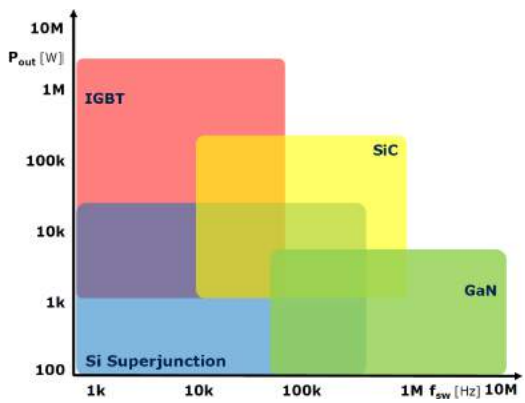


Fig. 5.2: Recommended application ranges for Si, SiC and GaN devices [ISiCPEAW 2016 - presented by Infineon Technologies AG 2016]

(a) (b)

Fig. 5.3: (a) SiC MOSFET SCH2080KE and (b) SiC schottky diode C3D10170H

remain dominant in the future. The graph of Fig. 5.2 was presented by Infineon Technologies AG at the ISiCPEAW workshop in 2016. A proof-of-concept 50kW inverter of Wolfspeed [90] shows that SiC power switches can reduce the total system cost by 15% compared to Si power switches, if the cost of cooling, filters, etc. is considered. More specifically, although the cost of the power devices is much higher compared to a Si-based system, the cost and size of the grid filter inductors and of the cooling system can be reduced in a SiC converter. This is particularly useful in the case of the undersea kite, since a size reduction of the passive filter at the ac side of the power conversion system is highly beneficial.

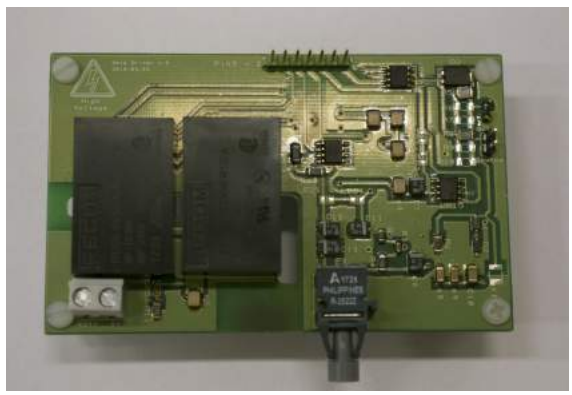
The SiC MOSFETs SCH2080KE of ROHM [Fig. 5.3(a)] are used for the lab prototype of the converters, which have been modelled in the simulation results of Chapter 4. These switches have maximum drain-source voltage 1200V and maximum continuous drain current 40A (at 25°C) / 28A (at 100°C). The clamping diodes of the NPC inverters are the C3D10170H from CREE [Fig. 5.3(b)] with 1700V maximum reverse voltage and 29A (at 25°C) / 14.4A (at 135°C) maximum continuous current.

Voltage overshoots caused by parasitic capacitance and inductance between the switching devices are a serious problem, when designing a power converter. Therefore, the power switches should not operate very close to their absolute rated voltage, but a safety limit of approximately 20% or more should be kept. The exact number of the safety margin depends eventually on the design of the power conversion system. The nominal dc-link voltage of the power conversion system is designed to be equal to 4 kV and, therefore, each switch of the converters will have to withstand 1 kV. In this case, a safety margin of 200 V has been chosen between the nominal operating conditions and the maximum voltage of the switches.

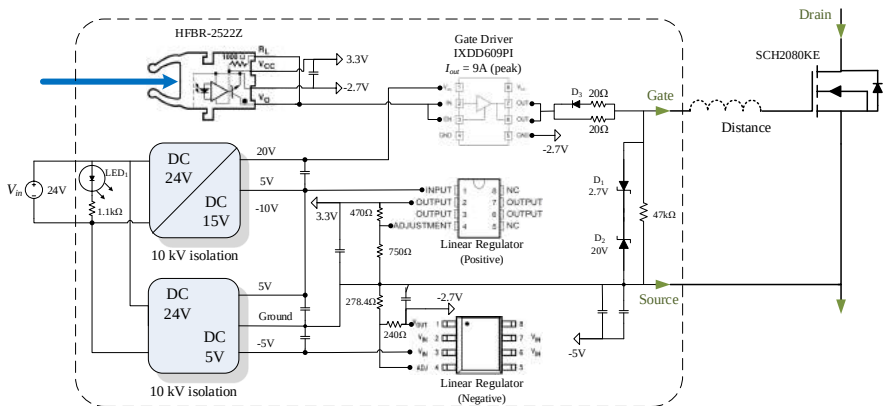
5.2.1 SiC Gate Driver Design

The gate driver is responsible for transferring the control signal from the output of the ePWM peripheral of the MCU to the gate of the MOSFETs. They also provide electrical isolation between the high voltage potential of the switch and the low voltage potential of the microcontroller. The SCH2080KE MOSFET requires a gate-source voltage of 20V in order for the switch to turn on and -2.7V for the switch to turn off.

Fig. 5.4(b) shows the circuit diagram of the gate driver PCB. Two separate dc/dc converters are used for each gate driver board which provide ±15V and ±5V power supplies. The primary side of these converters receives 24V input voltage. The



(a)



(b)

Fig. 5.4: (a) Picture and (b) schematic of the gate driver for the SCH2080 SiC MOSFET

secondary side of the dc/dc converters is floating at the voltage potential of the source of the MOSFET, while the primary side is at the voltage potential of the MCU. Therefore, dc/dc converters with reinforced isolation voltage of 10kV need to be used.

Linear regulators modify the output voltage of the dc/dc converters in order to produce -2.7 V and 3.3 V in respect to the ground, which is the source of the MOSFET. The gate resistor is equal to 20 Ω for turning on the switch and 10 Ω for turning off. Lower resistance is used for the turn-off operation in order to increase the speed of the gate driver. This is implemented by using a schottky antiparallel diode D_3 in parallel to the turn-on resistor [91]. Zener diodes D_1 and D_2 and a large resistor of 47 kΩ are used between the gate and source outputs of the gate driver board in order to protect it from overvoltages.

The distance between the outputs of the gate driver IC up to the gate and source of the switch is very critical for the optimal design of both the gate driver and the inverter PCB. Parasitic inductance occurs due to the loop between the gate driver output and the ground return traces as can be seen on the right side of Fig. 5.4(b), which can create voltage ringing in the gate drive waveform [91]. The voltage ringing is defined as unwanted oscillations during a step change of a voltage signal, because the parasitic inductance does not allow the current flowing on that loop of the system to change rapidly its value. Ringing on the power switch can cause unwanted turn-on and turn-off of the switch, which creates additional switching losses and could eventually destroy the switch if these voltage oscillations surpass its maximum voltage ratings. The longer this distance is, the larger the parasitic inductance becomes and more severe oscillations can occur on the power switch. The voltage oscillations due to the ringing usually have high frequency at MHz level, which create EMI noise that can easily interfere with other sensitive devices of the system, such as measurement devices and the MCU.

In order to decrease these oscillations, the following solutions are available to the designer of the PCBs. First, the distance between the gate driver and the power switch has to be minimized. A wider trace for the gate signal can also limit the parasitic inductance. Surface mounted devices (SMD) are also preferable compared to through-hole devices, since they can deal better with EMI and their reduced physical dimensions can limit the parasitic inductance and allow closer placement of the components [92]. In case the problem cannot be solved, capacitors have to be placed close to the gate pin of the switch and on the gate driver PCB in order to filter out the unwanted oscillations. The filter frequency can be optimized by placing multiple capacitors of different capacitance value, which have different

resonant frequency.

Fig. 5.5(a) shows the experimental measurements of the gate to source voltage V_{GS} at the terminals of the switch with switching frequency of 5 kHz. The switching frequency of the prototype converters used in the experimental results in later sections is equal to 20 kHz. A closer look of the V_{GS} voltage can be seen in Figs. 5.5(b)-(c), which validate that the voltage created by the gate driver is within the recommended range mentioned in the MOSFET datasheet [93], namely maximum $V_{GSS-surge} \in [-10, 26]$ V.

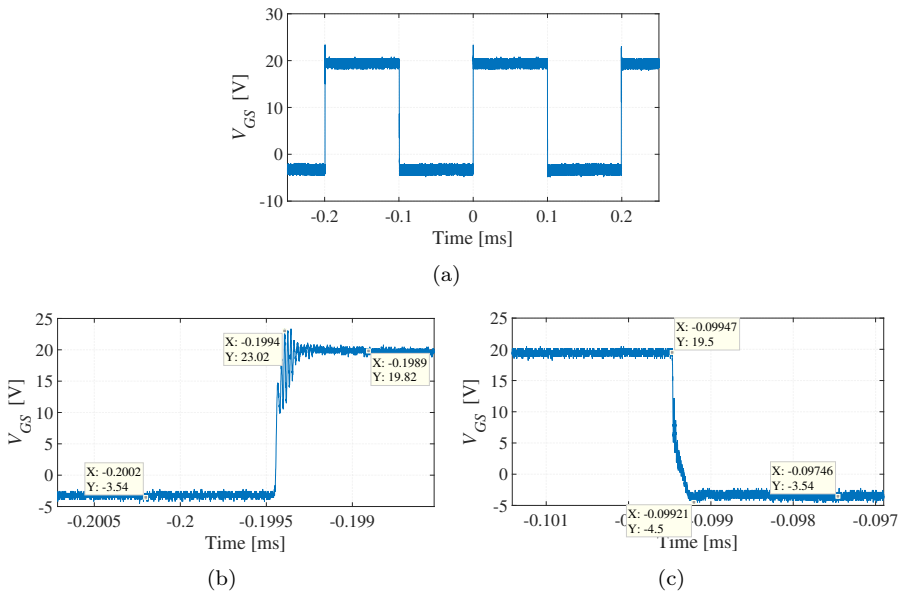


Fig. 5.5: Experimental results of (a) the gate-source voltage of SCH2080KE MOSFET with switching frequency of 5 kHz; zoomed-in gate-source voltage (b) during turn-on and (c) turn-off transient

5.2.2 NPC Converter Board

The developed prototype of the NPC inverter is shown in Fig. 5.7. The inverter has nominal voltage higher than 1.5kV peak voltage and, therefore, some special rules are followed during the design process. The prototype PCBs have been built based on the design guidelines described in [94].

The first thing that needs to be considered is the proper substrate material for the PCB, especially if double-layer PCBs are used (Fig. 5.6). PCBs with more

than two layers are not recommended for high power converters, since they can become fragile due to the large thickness and it is also difficult to dissipate the heat from the inner copper layers [95]. The substrate of the PCB needs to be able to handle the differential voltage between the top and the bottom copper layer. The substrate (prepreg) used on the developed prototype by the manufacturer of the PCBs is the FR-370HR with dielectric strength of 54 kV/mm [96].

Proper design of the traces on the PCB is very important in order to avoid Corona discharges or a direct arc. Sharp edges and corners on the copper traces should be avoided, because high electric field occurs there, which can initiate Corona. Smooth and round curves should be used wherever possible for the traces and the pads of the PCB [94]. Also, the minimum creepage distances should be kept between the components placed on the PCB and between the traces of the same layer. A rule of thumb of 100 V/mm for the creepage distance between the components has been considered for the design of the prototype.

Due to the high operating voltage of the prototype, longer distances are, therefore, required between the power switches of the converters and the dc link capacitors of the system. Since the dc link capacitors operate as a quite stiff voltage source, the parasitic inductance of the PCB traces can cause high frequency voltage oscillations of the switches, which is called ringing. Proper design of the traces in the PCB is very important, as mentioned also in Subsection 5.2.1. The parasitic inductance of the circuit can be reduced in order to limit the ringing by increasing the width of the traces of the PCB as much as possible. Also, the drain and source traces of the power MOSFETs as well as the anode and cathode traces of the schottky diodes should be placed directly over each other, which reduces the parasitic impedance [92]. Resistor-capacitor (RC) snubber circuits are also installed in parallel to each MOSFET and diode of the NPC converter, as can be seen in Fig. 5.7(a). The RC snubber consists of a small capacitor and a small resistor connected in series that suppress the rapid rise in voltage (dV/dt) of the switching device to a value that will not trigger ringing.

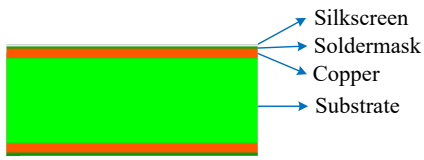
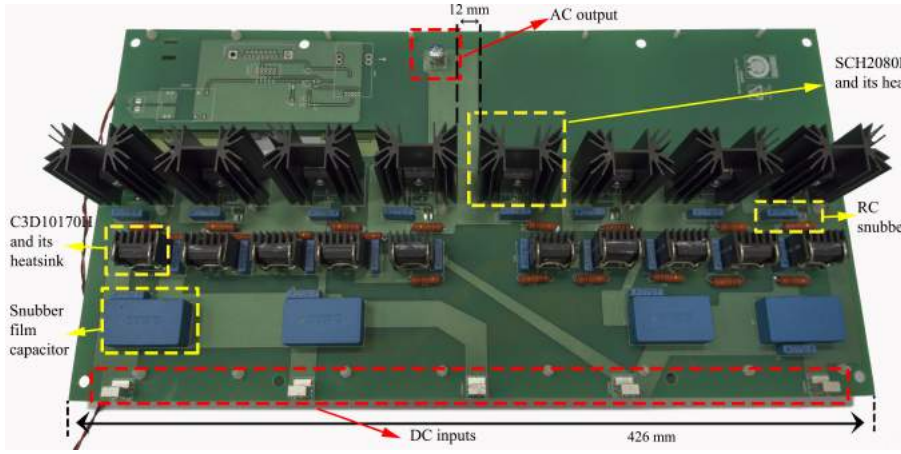


Fig. 5.6: Composition of a two-layer PCB



(a)

(b)

Fig. 5.7: PCB of a single phase 5-level NPC converter with the gate drives connected to the switch terminals: (a) top and (b) bottom view

5.2.3 DC-Link Board

Film capacitors with part number 947D591K132DJRSN are chosen for the prototype power conversion system, which have rated voltage of 1.3 kV and capacitance of 590 μF. Film capacitors are more bulky and expensive compared to electrolytic ones. However, they can handle higher voltage and are, therefore, more commonly used in high voltage drives. Eight capacitors (in two parallel-connected groups of

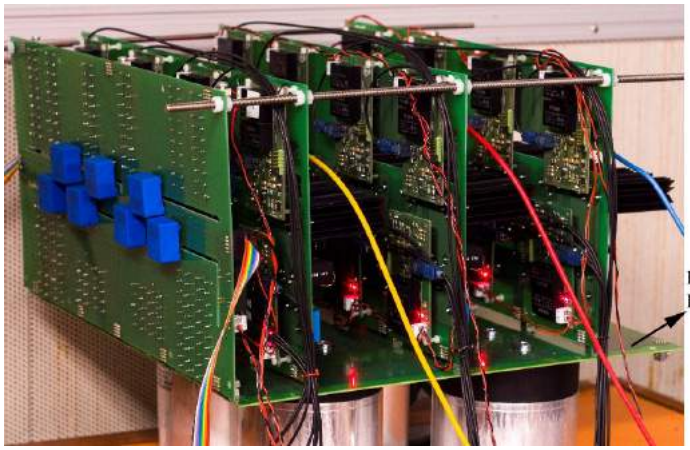


Fig. 5.8: Laboratory prototype of the three-phase 5-level NPC inverter

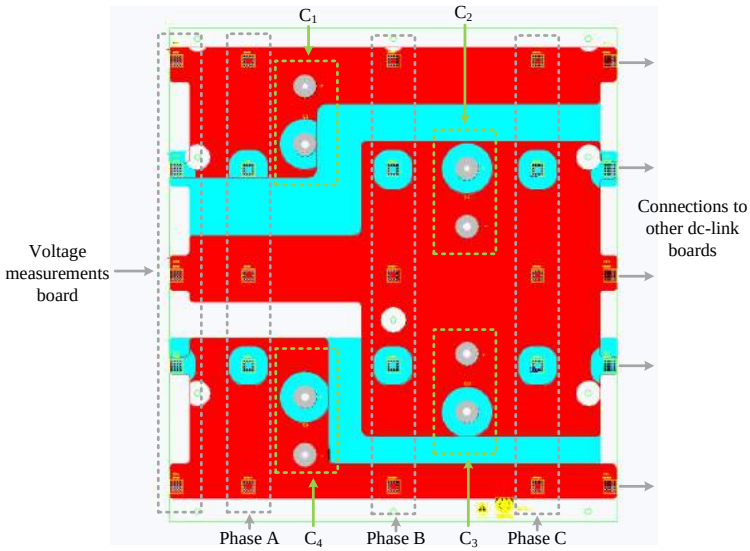


Fig. 5.9: Schematic of the dc link PCB design, red→top copper layer and blue→bottom copper layer

4 capacitors) are installed in total on the PCBs of the power converters through a special board which is shown in Figs. 5.8-5.9. Therefore, the equivalent capacitance of the dc-link becomes $590 \cdot \frac{2}{4} = 295\ \mu$F.

This dc-link PCB serves as the base for connecting the three-phase NPC inverter and the balancing converter to the dc-link of the system. As can be seen in Fig. 5.9, this board has enough connectors for 3 converter boards and 4 capacitors.

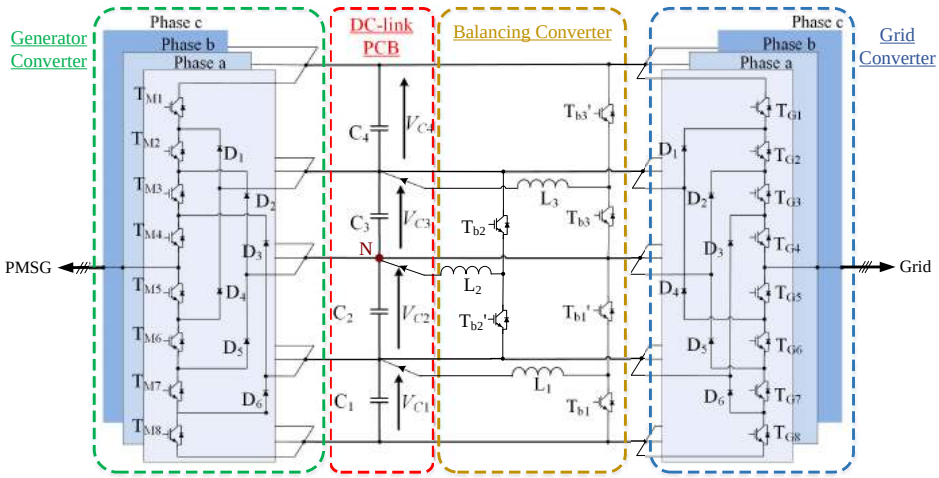


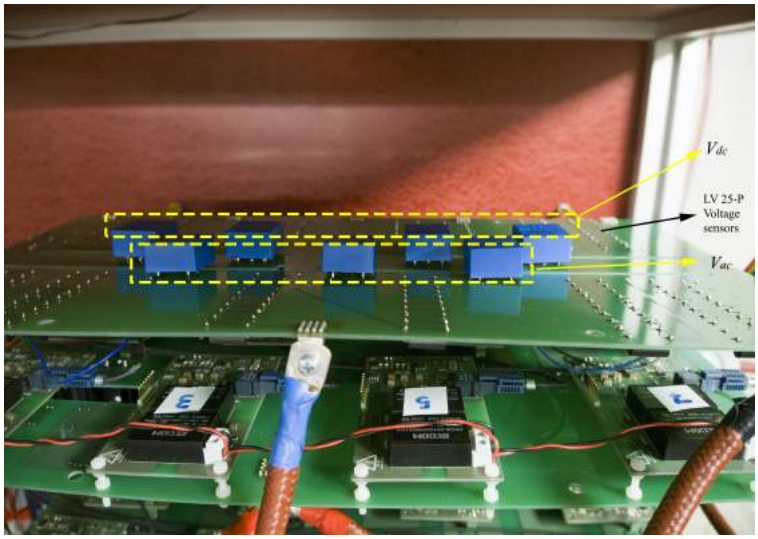
Fig. 5.10: Schematic diagram of the whole prototype power conversion system

Therefore, three of these PCB are needed to accommodate the two B2B-connected NPC converters and the balancing dc/dc converter [Fig. 5.18(b)]. Fig. 5.10 shows also the schematic diagram of the whole power conversion system, which is the same with the schematic of the simulated system in Fig. 4.14.

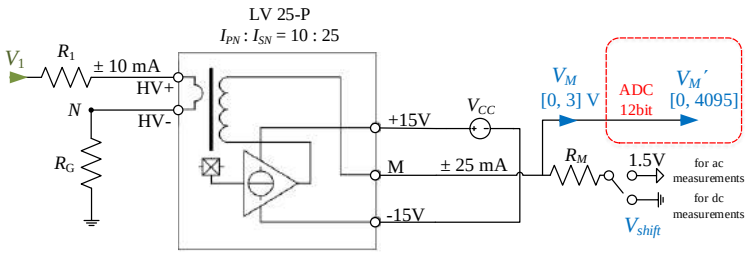
It is important to make sure that the distance between the dc link terminals of the power converters and the pins of the capacitors is the shortest possible and that the traces on the dc link PCB are wide in order to keep the parasitic inductance low. The traces connected to the plus and negative poles of each capacitor are also placed over each other, as explained also in Subsection 5.2.2, which can reduce the parasitic inductance even further.

5.2.4 Measurement Devices

Voltage measurements of the four dc link voltages and of the three phase voltages at the grid output of the converter are needed for the control of the system. The Hall-effect voltage sensors from LEM with product number LV 25-P are used, as can be seen in Fig. 5.11. The voltage to be measured is shown as V_1 in Fig. 5.11(b). The nominal primary current of the sensor is 10mA; therefore, a suitable resistor R_1 is placed between the node V_1 and the input of the sensor HV+. All the required voltages are measured in respect to the neutral point of the dc-link N and, therefore, the negative pole of the sensor HV- is connected to N. The neutral



(a)



(b)

Fig. 5.11: (a) Laboratory prototype and (b) schematic diagram of the dc and ac voltage measurement PCB

point N is grounded though a ground resistor $R_G = 14.1$ kΩ.

The LV 25-P sensor behaves as a current source at its secondary side with nominal secondary current 25mA. The voltage $V_M \in [0, 3]$V across the resistor R_M is the input of the ADC channel of the MCU. When the voltage to be measured V_1 is ac and gets both positive and negative values, the signal V_M needs to be shifted up by 1.5V and the reference of the signal is the 1.5V. In the case of dc voltage measurements, the reference of the V_M is the ground. The R_M is equal to 60Ω, when the measured voltage is ac, and is equal to 120Ω, when measuring dc voltages.

The ADC input of the MCU converts the V_M into a 12bit digital signal and the

original voltage V_1 can be calculated as follows

$$V_1 = \left(\frac{3V'_M}{4095} - V_{shift} \right) \cdot gain + V_{offset} \tag{5.1}$$

where the variable *gain* depends on the ratio between the primary and secondary side of the measurement device and on the resistor R_M.

Similar Hall-effect sensors are used for measuring the currents of the system. More specifically, the following current measurements are needed (see Fig. 5.1): three-phase currents of the PMSG I_{gen}, three-phase grid currents I_s and the current of the three dc inductors I_L . The current transducer LA 25-P from LEM is used for the current measurements and similar methodology to the voltage sensors is used for receiving the measured signal in the MCU.

5.2.5 Overcurrent-Overvoltage Protection Strategy

The signals from all the measurement devices end up on the PCB shown in Fig. 5.12 before being sent to the ADC inputs of the MCU. This PCB converts all the measured signals into the correct voltage level which is required for the ADC inputs. Another use of this board is to disconnect the converter in case an overcurrent/overvoltage is measured in the system. The analog circuit shown in Fig. 5.13 compares each measured signal V_M with a maximum and minimum value $V_{ref\ H}$ and $V_{ref\ L}$, respectively. In case V_M exceeds the predefined operating region, an error signal is created, which turns on also a red LED. The global error signal PRT is the output of this board.

This error signal forces all the power switches of the converters to open, in case of a fault. This is achieved through the trip-zone module of the MCU [97] and also though another PCB marked with red color in Fig. 5.13, whose function is to convert the ePWM outputs of the microcontroller into optical signals, which are sent to the gate drivers. The PRT disables the PWM signals of the gate drivers protecting the converters. The error signal is also connected to a relay coupled to a mechanical switch which switches-off the converters. The detailed schematics of the PCBs shown in Fig. 5.13 can be found in Appendix B.

Therefore, there is a three-layer overcurrent/overvoltage protection strategy of the generator drive. The analog circuit that disconnects the control signals of the gate drivers has the shortest reaction time, since the logical gates have delay in the range of a few μs.

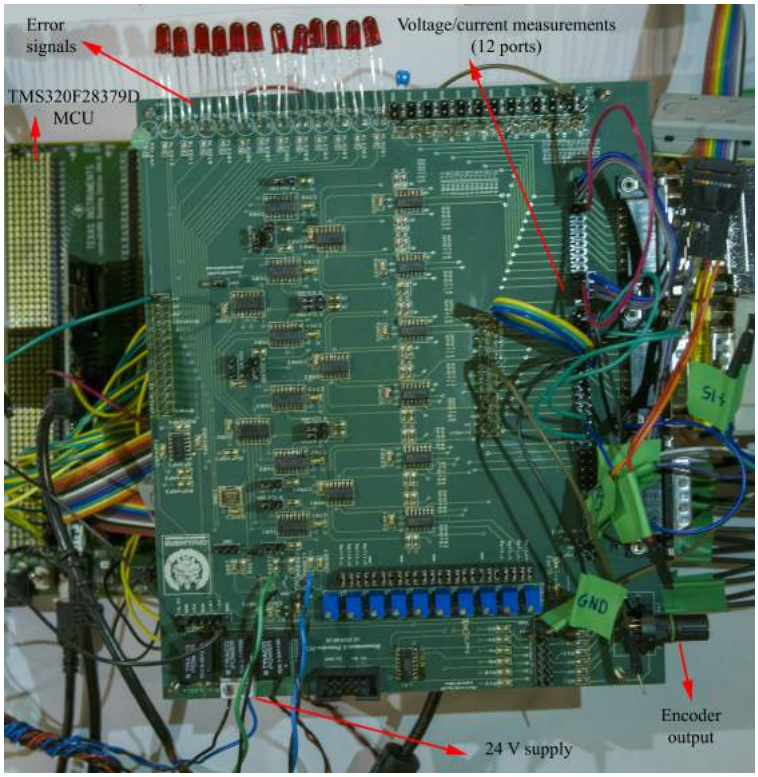


Fig. 5.12: PCB collecting all the measurement signals of the drive before routing them to the MCU

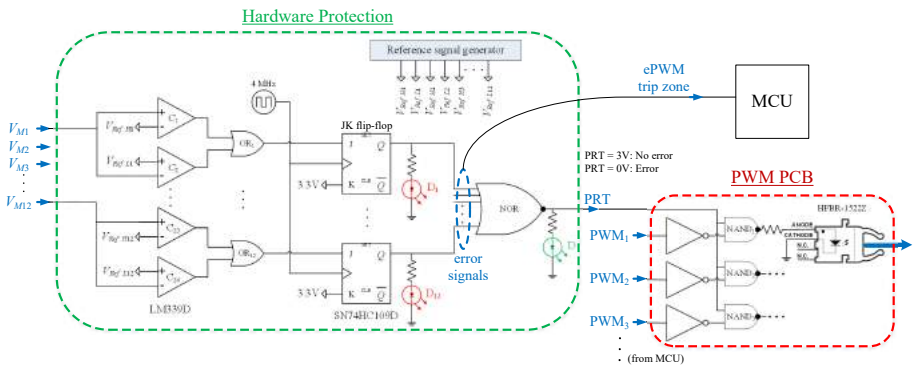


Fig. 5.13: Schematic diagram of the overcurrent/overvoltage protection strategy

5.3 Experimental Results

5.3.1 Medium Voltage PMSG

A medium voltage PMSG has been used within this project and it is tested in this subsection in order to evaluate its performance and measure its parameters. The electrical machine test bench is shown in Fig. 5.14(e), where the PMSG and the driving motor IM are at the right and left side, respectively. Pictures of the generator during its manufacturing phase are shown in Fig. 5.14(a)-(d).

The design of the generator is not part of this thesis.

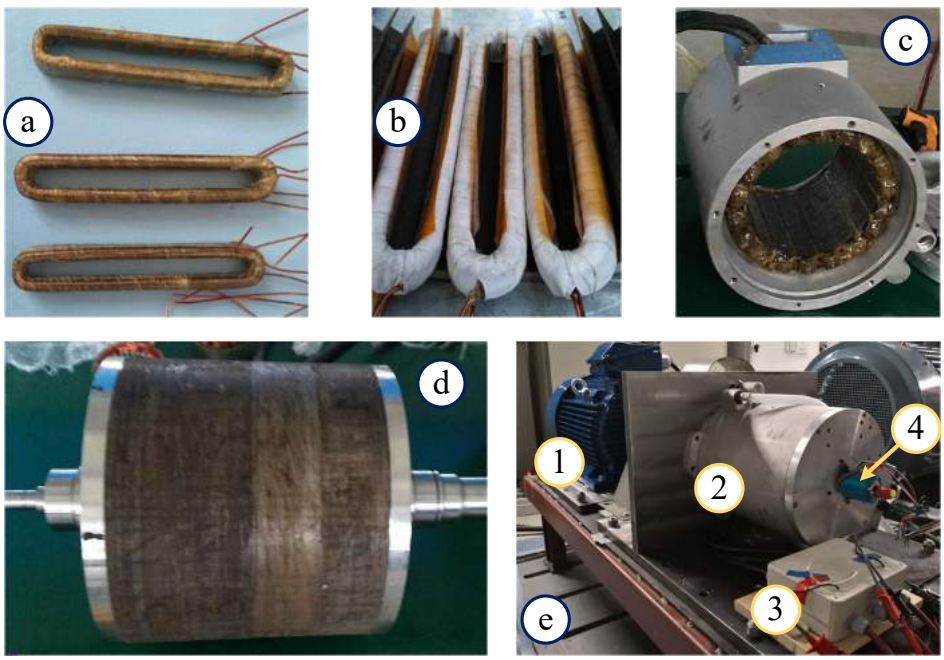


Fig. 5.14: PMSG (a)+(b)Stator windings, (c) stator, (d) rotor and (e) the whole machine test-bench: 1) IM, 2) the medium voltage PMSG mounted on the bench, 3) connection box for the stator cables of the PMSG, 4) terminal for connecting the encoder and temperature sensors of the PMSG

No-load test of the PMSG

The PMSG is tested first at no-load conditions in order to evaluate the back-EMF and the cogging torque, and, afterwards, load-tests are implemented. The following voltage probes are used for the following experiments of this section: the HVD3106A voltage probe with up to 1500 V_{peak} measurement range [7] and the CP150 current probe [8].

No-load test of the PMSG is implemented by having the terminals of the generator open-circuited and operating the IM in motor mode. The measured L2L voltage is equal to the no-load back-EMF of the machine, which is shown in Fig. 5.15(a) for rotor speeds equal to 1600 rpm up to 1200 rpm. Fig. 5.15(b) shows one mechanical period of the no-load EMF voltage and the cogging torque for rotor speed 200 rpm.

The torque waveform has 12 positive and negative peaks in one mechanical period of the PSMG, which is the 12th harmonic generated by the slots and poles of the PMSG. There is also 6th harmonic component in the torque waveform generated by the cogging torque of the IM.

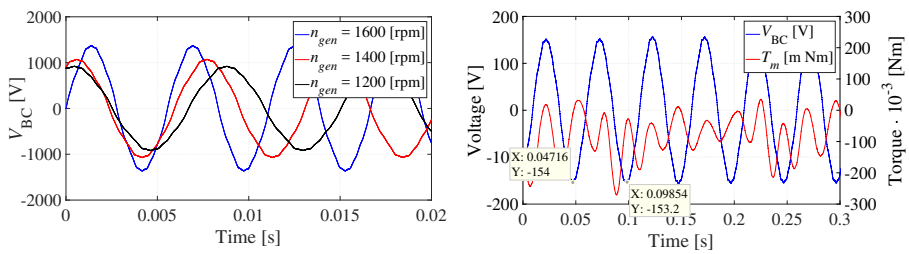


Fig. 5.15: Experimental results of the medium voltage PMSG no-load test: (a) no-load EMF voltage for various rotor speeds and (b) cogging torque for 200 rpm rotational speed

Load test of the PMSG without converter control

The PMSG is tested also with a resistive load R_L, as shown in Fig. 5.16. The load is three resistor banks connected in Y connection and can vary its resistance from 0.4 Ω up to 3 Ω. The PMSG is connected to the resistive load through a step-down transformer and its active and reactive power in each case are determined by the combination of the equivalent resistance and inductance of the load, since it is not

controlled by a converter.

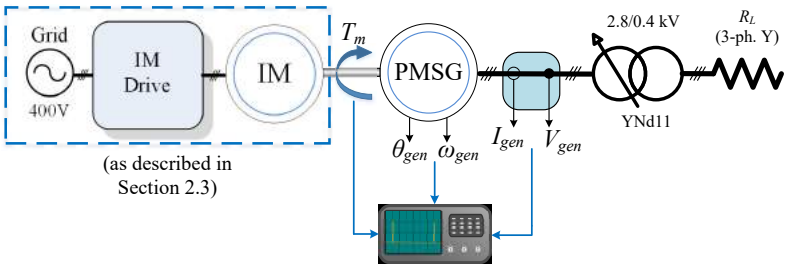
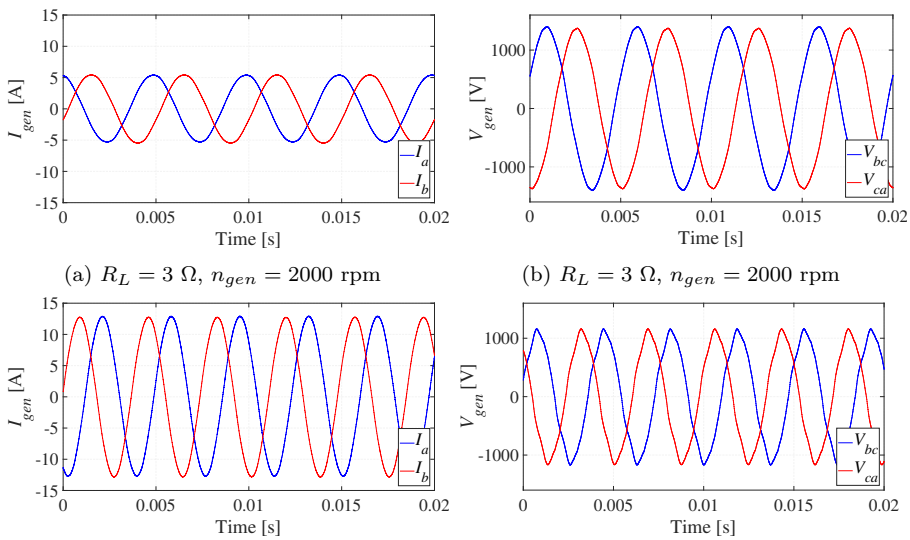


Fig. 5.16: Schematic diagram of the PMSG load test with direct connection of the generator to the resistive-inductive load

Experimental results of this test are presented in Fig. 5.17 for two different operating points. In Figs. 5.17(a)-(b) the load is $R_L = 3\ \Omega$ with $n_{gen} = 2000$ rpm and the apparent power is $S = 6.42$ kVA, while in Figs. 5.17(c)-(d) the load is $R_L = 0.8\ \Omega$ with $n_{gen} = 2700$ rpm and the apparent power is $S = 12.27$ kVA.

The parameters of the PMSG are shown in Table 5.2, where the inductances in the d- and q-axis have been measured based on the method described in [98, 99].



(a) $R_L = 3\ \Omega$, $n_{gen} = 2000$ rpm

(b) $R_L = 3\ \Omega$, $n_{gen} = 2000$ rpm

(c) $R_L = 0.8\ \Omega$ with $n_{gen} = 2700$ rpm

(d) $R_L = 0.8\ \Omega$ with $n_{gen} = 2700$ rpm

Fig. 5.17: Experimental results of the medium voltage PMSG with resistive-inductive load

Table 5.2: Rated values and control parameters of the PMSG and the IM

Parameter	Value	Unit
Nominal Power P_{nom}	50	kW
Nominal rotor speed n_{gen}	4000	rpm
Number of pole pairs P	6	-
Nominal torque T_N	119	Nm
No-load EMF at rated speed (L2L, peak)	2932	V
Stator inductance L_d	18.9	mH
Stator inductance L_q	25	mH
Stator resistance R_S	1.5	Ω
PMSG inertia J_{PMSG}	0.1274367	kg·m^2
IM inertia J_{IM}	0.2	kg·m^2
Torque sensor inertia J_S	$175.8{\cdot}10^{-6}$	kg·m^2
PMSG current controller bandwidth α_c	1500	rad/s
PMSG speed controller bandwidth α_ω	15	rad/s
PMSG converter switching frequency f_{sw}	20	kHz

Specifically, step-change of dc current was applied towards the d- and q-axis of the machine and the inductance was calculated from the response of the current.

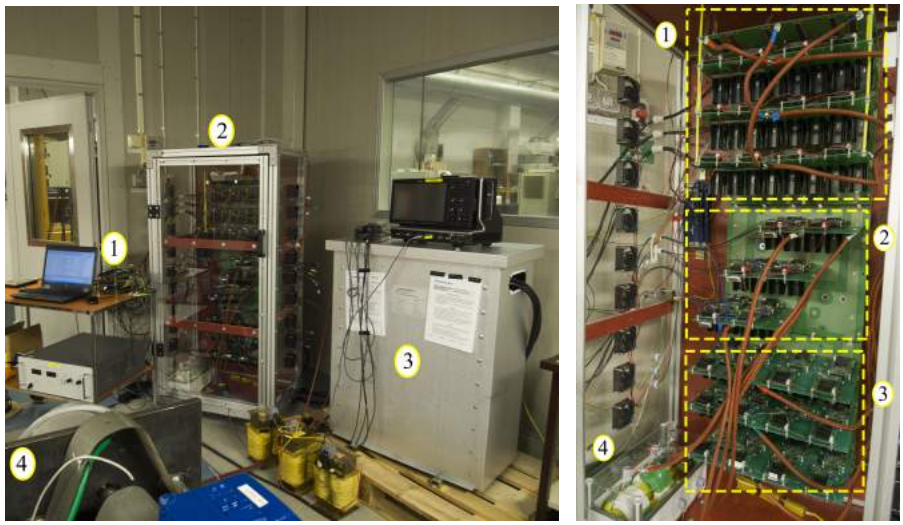
5.3.2 Power Conversion System

The multilevel generator drive is tested in this subsection and the laboratory set-up is shown in Fig. 5.18(a) with the electrical machine test-bench and the power converter cabinet. Fig. 5.18(b) shows a more detailed view of the power converter cabinet. The converters installed inside the cabinet are marked with dashed boxes and are described in the figure caption.

The dc-link voltage balancing strategy of Subsection 4.2.2 is used here, namely the three-stage balancing converter with open-loop control of its duty cycle. The balancing converter has the same switching frequency with the NPC converters, namely 20 kHz.

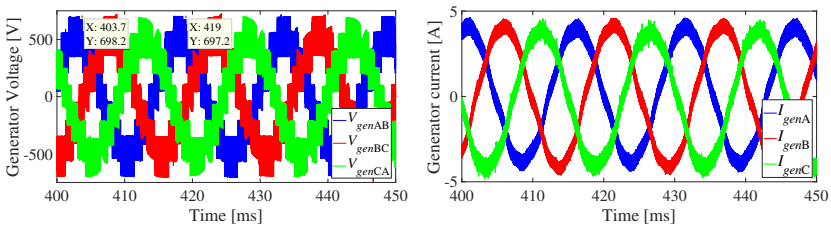
Generator-side Converter

Experimental results of the generator-side NPC converter are shown in Figs. 5.19-5.20. The PMSG operates in generator-mode with 650 rpm and has reference



(a) (b)

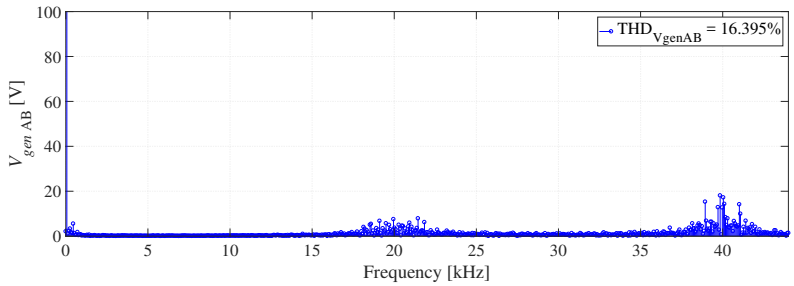
Fig. 5.18: (a) Laboratory set-up of 1) the MCU and measurements board, 2) the power converter cabinet, 3) the 2.8/0.4 kV three-phase transformer 4) the machines test-bench; (b) closer view of the power converter cabinet with 1) the grid side 5-level converter, 2) the dc-link balancing converter, 3) the generator-side 5-level converter and 4) the dc inductors for the balancing converter



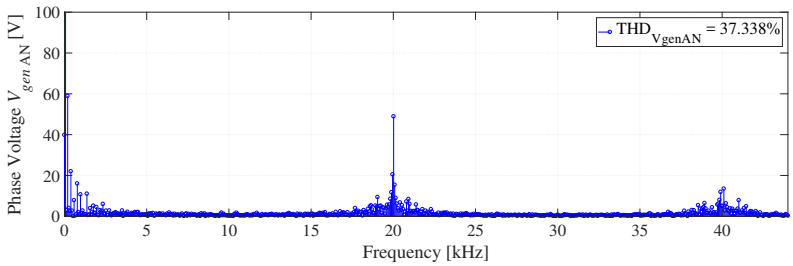
(a) (b)

Fig. 5.19: Experimental results of the generator-side NPC converter when the generator operates at 650rpm and current $I^*_{genq} = -4$ A: (a) three-phase L2L generator voltage and (b) current

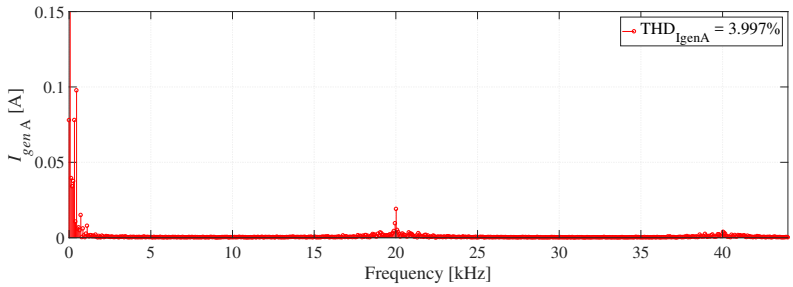
current equal to $I^*_{genq} = -4$ A. The total dc-link voltage is 670 V during this test. The FFT analysis of the voltages and currents is also shown and specifically the THD of the current is 3.997%, while the THD of the phase voltage is 37.338%. When compared to the simulation results of Fig. 4.20 in Subsection 4.2.2, it can be seen that the phase voltage THD is very close to the simulated value. However,



(a)



(b)



(c)

Fig. 5.20: Experimental results of the generator-side NPC converter when the generator operates with 650 rpm and current $I^*_{genq} = -4$ A: FFT analysis of the (a) L2L voltage V_{genAB}, (b) phase voltage V_{genAN} and (c) stator current I_{genA}

the THD of the current is higher at the experimental results and this is explained due to the lower amplitude of the current there.

Grid-side Converter

Experimental results of the grid-side converter are shown in the following figures. The three-phase transformer shown in Fig. 5.1 is not used here, because low voltage tests are implemented. Instead, the grid converter is connected to the

400V-grid through a series-connected inductor with inductance $L_f = 2$ mH. The grid-side converter control parameters are shown in Table 5.3.

Table 5.3: Parameters of the Grid-side Converter

Parameter	Value	Unit
Tested L2L grid voltage (rms) V_s	400	V
Fundamental frequency f_n	50	Hz
Grid converter switching frequency f_{sw}	20	kHz
Grid filter inductance L_f	2	mH
Tested total dc-link voltage $V_{dc\ tot}$	670	V
Grid current controller bandwidth α_{cs}	8000	rad/s
PLL bandwidth α_{PLL}	10π	rad/s
DC-link controller bandwidth α_{DClink}	400	rad/s

The current controller of the grid current I_s is tested and experimental results of the phase A current I_{sA} and the phase voltage at the output of the converter $V_{sConvAN}$ are shown in Figs. 5.21-5.22. The grid phase voltage is defined as the differential voltage between a phase of the converter and the middle point of the dc-link, marked as N. Specifically, step-change of the I^*_{sd} is applied and the converter is sending active power to the grid in Fig. 5.21(a)-(b), while it receives power from the grid in Fig. 5.21(c)-(d). Similarly, q-axis current I^*_{sq} is applied in Fig. 5.22 and the grid converter is exchanging reactive power with the grid.

The dc-link controller of the grid-side NPC converter is tested in Fig. 5.23 with a step-change of the reference voltage, which changes from 670 V to 600 V at the time instant 85ms. The individual voltages of the four dc-link capacitors in Fig. 5.23(b) follow the change of the total dc voltage. They remain balanced with each other with a small error during this transient. This error can be explained due to the use of open-loop control for the balancing converter, as mentioned previously. Therefore, larger errors between the capacitor voltages are expected compared to the closed-loop control scheme shown in the simulation results of Subsection 4.2.2.

The amplitude of the L2L grid voltage at the output of the converter $V_{sConvAB}$ changes as well, as can be seen in Fig. 5.23(c), since it varies between $+V_{dc\ tot}$ and $-V_{dc\ tot}$. The converter voltage is approximately 40V higher than the dc-link voltage due to the ringing on the power switches. The grid voltage V_{sAB} is also shown in the same figure, which is in phase with the converter voltage. The d-axis grid current I_{sd} in Fig. 5.23(d) is calculated by the dc-link PI controller. A limiter of 6 A is applied on the reference d-current, which is reflected on the

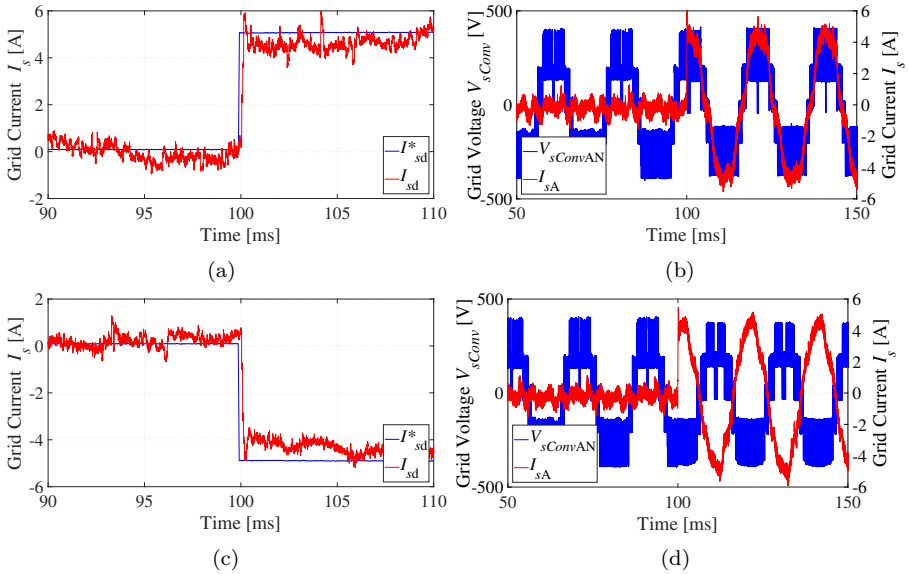


Fig. 5.21: Experimental results of the grid-side NPC converter with a step-change of the I^*_{sd} reference current (a)-(b) from 0 to 5 A and (c)-(d) from 0 to -5 A

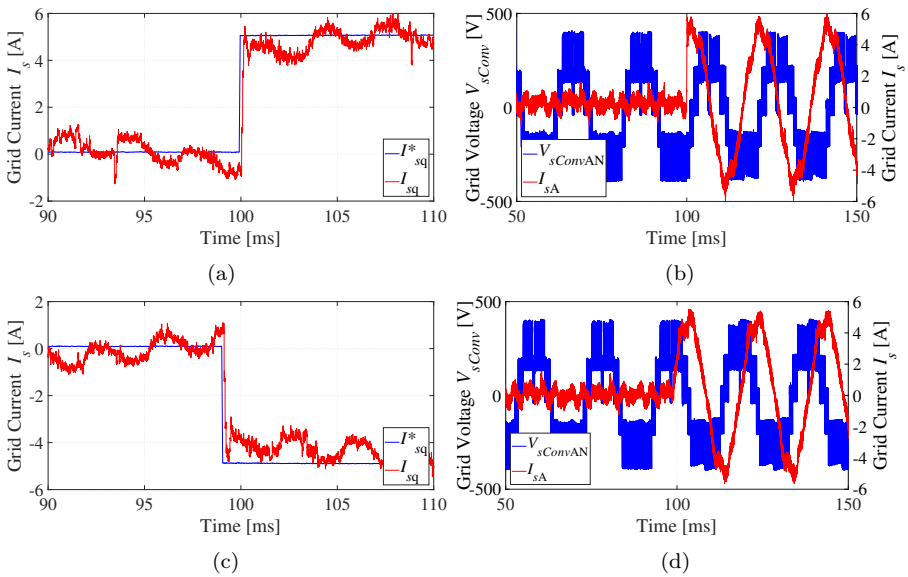


Fig. 5.22: Experimental results of the grid-side NPC converter with a step-change of the I^*_{sq} reference current (a)-(b) from 0 to 5 A and (c)-(d) from 0 to -5 A

actual current.

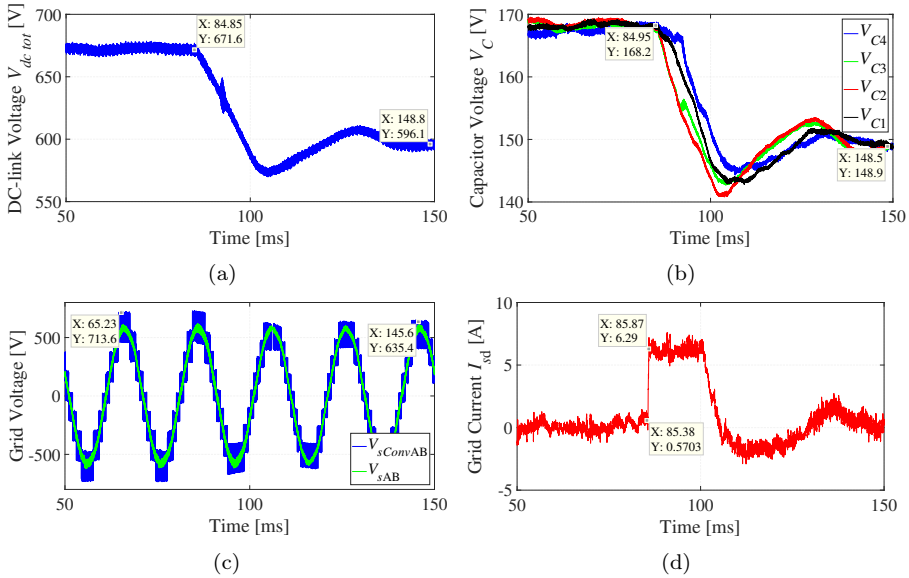


Fig. 5.23: Experimental results of the grid-side NPC converter with a step-change of the dc-link voltage $V_{dc\ tot}$ from 670 V to 600 V: (a) dc-link voltage, (b) dc-link capacitor voltages, (c) grid voltage and (d) d-axis grid current

5.4 Summary

This chapter has presented the design process and test results of a novel 5-level NPC-based PMSG drive. Firstly, the hardware design and component selection of the NPC converters and the balancing circuit are described. Special care has been taken so that the power converters can operate at medium voltage level, with maximum 3 to 4 kV at the dc side. Therefore, large creepage distance has been kept between the power components in order to avoid failures due to the high operating voltage and the control and measurement boards are highly insulated from the power circuit of the converters. The parasitic inductance on the converter boards is also minimized and snubber circuits are used in parallel to some of the power switches to further reduce their voltage overshoot during the switching transient. The prototype multilevel drive uses SiC power switches in order to decrease the converter losses and to increase the maximum operating voltage of the system. Suitable gate drive boards have been designed for the specific switches.

Experimental results of both converters of the drive are shown in order to demonstrate the functionality of the system under various operating conditions. DC-link voltage up to 670 V and current of 5 A have been tested in this chapter. More tests closer to the rated parameters of the system are planned to be implemented in the future.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This thesis investigates the design and control of the power conversion system in a subsea kite-based tidal power generator. This tidal power generation technology is a rather new concept and the design of the converters' control as well as the suitable selection of the converter topology and hardware is challenging. An important initial step to deal with this topic is to understand the operation of the tidal power generator system and to model its power and torque profile. The controllers that regulate the converters of the system are analyzed in detail and tested experimentally. The second step of the thesis is the design and manufacturing of a medium voltage multilevel power conversion system which can improve the performance of the kite due to the increase of the system's operating voltage.

The operation of the kite's power conversion system has been modelled in Chapter 2 in order to study the power and speed dynamics of the generator. Two MPPT control schemes for maximizing the power production of the tidal power system are presented and compared. The first method controls directly the electrical torque of the generator without any feedback of the rotor speed, while in the second technique a separate speed control loop with a PI controller generates the reference current of the generator. The second method has shown better dynamic performance, although the control structure is more complicated. Therefore, the tidal generator operates closer to the reference Maximum Power Point. This results to a higher average power production by the generator of up to 4%. The presented control systems have been verified on a novel 35 kW / 400 V (ac-L2L) laboratory

emulator, where the dynamics of the kite's turbine are reproduced by a properly controlled induction motor. The effect of the speed controller's bandwidth on the accuracy of the MPPT technique has also been studied in Subsection 2.4.1. Specifically, it has been shown that an increase of 10 times of the PI controller gains results to an increase of the average produced power of up to 1%. Therefore, a better design of the PI controllers regulating the converters can increase the power produced by the TUSK tidal power system.

The increase of the kite's operating voltage is highly motivated by the resultant decrease of the ac current flowing through the undersea cables that connect the kite to the local grid, since the use of a 5-level-based drives can increase the voltage more than 4 times compared to the standard design with 2LCs. Therefore, undersea cables with smaller diameter can be used reducing the total weight and drag of the kite system. In case the copper area of the undersea cables is kept the same, the ohmic losses of the cables will be decreased. Therefore, a medium voltage multilevel generator drive has been proposed in Chapter 4 that consists of two B2B-connected 5-level NPC converters and a medium voltage PMSG. The 5-level NPC converter is a suitable topology for medium voltage machine drives and its main advantages compared to other multilevel topologies are the common dc bus and the reduced number of passive components. Conventional control schemes can be used for controlling the PMSG, such as field-oriented-control, and voltage-oriented control for the grid-side of the drive.

The main drawback of this converter topology is the balancing of the dc-link capacitor voltages, which has been thoroughly studied in this thesis. Four alternative ways of balancing the dc-link voltages have been developed utilizing a modified version of the SVM or dc/dc converters connected in parallel to the dc-link. The advantages and disadvantages of each proposed balancing method have been summarized in Table 4.6 and the conclusions mentioned there are based on simulation results implemented on Matlab/Simulink. PLECS has also been used for modelling the physical system of the power converters.

The harmonics of the ac current and voltage are also highly improved when using drives with 5-level converters instead of 2-level drives, as shown by the simulation results of Chapter 4. Specifically, FFT analysis of the current and voltage has shown that the THD of the generator current reduces by 66% and the generator phase voltage by 58%, when 5-level instead of 3-level converters are used. The harmonic analysis of the simulated generator-side converter has also been verified experimentally in Chapter 5 showing similar results. Similar results are expected for the grid-side voltage and current harmonics, which are not shown in the thesis.

Finally, a prototype generator drive with 5-level NPC converters and a PMSG has been designed and manufactured. The system is designed to have 50kW rated power and dc-link with up to 4 kV peak dc voltage. Experimental results with the system connected to the grid are shown in Chapter 5, where the generator-side NPC converter controls effectively the speed of the PMSG and the grid-side converter sends the produced active power to the grid. The dc-link voltage balancing method with a dc/dc balancing converter controlled in open-loop mode is used here.

6.2 Future Work

The hardware-based open-loop controlled voltage balancing technique has been used with the laboratory prototype, which is the simplest out of the four methods shown in Chapter 4. It has been shown in Figs. 4.16 and 5.23 that it controls the capacitor voltages effectively under steady-state operation, but its dynamic performance is not satisfactory. Therefore, the voltage balancing with SVM and closed-loop control of the balancing converter needs to be tested experimentally in order to improve the performance of the prototype system.

It is also interesting to operate the prototype NPC converters with power and voltage closer to their rated values in order to test the effectiveness of the design. More detailed measurements of the system's losses can be implemented in order to demonstrate the improved efficiency of the converters due to the use of SiC power switches.

The use of medium voltage NPC-based drives can be expanded into more applications where the increase of the operating voltage is beneficial. The automotive applications could also be an interesting research topic where SiC-based multilevel converters can be applied to increase the power density and efficiency of the system.

Another suitable application for multilevel power conversion systems is the wind power sector, where NPC converters with IGBTs or IGCTs are already used in large wind turbines. Medium voltage is necessary there to decrease the current of the power converters. SiC-based converters similar to the prototype system developed in this thesis can be used there to increase the efficiency of that system even more.

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Appendix A

The following C-code is used for generating the matrices of the SVM algorithm in (3.23) and (3.24).

The variables from the following C-code are defined as $N\_layer = N - 1$ and the vectors V_D_abc, V_E_abc, V_F_abc and V_G_abc are calculated from (3.13):

```
if ((u_ref_a_SVPWM + u_ref_b_SVPWM) >
            (floor(u_ref_a_SVPWM) + floor(u_ref_b_SVPWM) + 1))
{
    // upper triangle sequence: | E F G E | E G F E |
    duty_E = V_G_ab[1] - u_ref_b_SVPWM;
    duty_F = V_G_ab[0] - u_ref_a_SVPWM;
    duty_G = 1 - duty_E - duty_F;
    duty[0]   = duty_E/2;
    duty[1]   = duty_F;
    duty[2]   = duty_G;
    duty[3]   = duty_E/2;

    //[V_E_abc;V_F_abc;V_G_abc;V_E_abc+[1 1 1]];
    vector[0][0] = V_E_abc[0];
    vector[0][1] = V_E_abc[1];
    vector[0][2] = V_E_abc[2];

    vector[1][0] = V_F_abc[0];
    vector[1][1] = V_F_abc[1];
    vector[1][2] = V_F_abc[2];

    vector[2][0] = V_G_abc[0];
    vector[2][1] = V_G_abc[1];
    vector[2][2] = V_G_abc[2];

    vector[3][0] = V_E_abc[0]+1;
    vector[3][1] = V_E_abc[1]+1;
    vector[3][2] = V_E_abc[2]+1;
```

```
29
30  }
31  else
32  {
33      // lower triangle sequence: | D E F D | D F E D |
34      duty_E = u_ref_a_SVPWM - V_D_ab[0];
35      duty_F = u_ref_b_SVPWM - V_D_ab[1];
36      duty_D = 1 - duty_E - duty_F;
37      duty[0]   = duty_D/2;
38      duty[1]   = duty_E;
39      duty[2]   = duty_F;
40      duty[3]   = duty_D/2;
41
42      //[V_D_abc;V_E_abc;V_F_abc;V_D_abc+[1 1 1]];
43      vector[0][0] = V_D_abc[0];
44      vector[0][1] = V_D_abc[1];
45      vector[0][2] = V_D_abc[2];
46
47      vector[1][0] = V_E_abc[0];
48      vector[1][1] = V_E_abc[1];
49      vector[1][2] = V_E_abc[2];
50
51      vector[2][0] = V_F_abc[0];
52      vector[2][1] = V_F_abc[1];
53      vector[2][2] = V_F_abc[2];
54
55      vector[3][0] = V_D_abc[0]+1;
56      vector[3][1] = V_D_abc[1]+1;
57      vector[3][2] = V_D_abc[2]+1;
58  }
59
60  // duty cycle of each phase and each state
61  //              A                B                C
62  //      1   duty_phA_state1   duty_phB_state1  duty_phC_state1
63  //      2   duty_phA_state2   duty_phB_state2  duty_phC_state2
64  //      3   duty_phA_state3   duty_phB_state3  duty_phC_state3
65  //     ...
66  //N_layer  duty_phA_stateN   duty_phB_stateN  duty_phC_stateN
67
68  for (i = 0; i<=2; i++)            // 3 phases
69    {
70        for (j = 0; j<=3; j++)      // 4 time intervals
71        {
72           duty_state[j][i] = 0;
73        }
74    }
75
76  for (i = 0; i<=2; i++)          // 3 phases
```

```
77  {
78      for (j = 0; j<=3; j++)      // 4 time intervals
79      {
80          for (k = 0; k<N_layer; k++)   // check the state
81          {
82              if (vector[j][i] == k+1)
83              {
84                  duty_state[k][i] = duty_state[k][i] + duty[j];
85                  break;
86            }
87          }
88      }
89  }
90
91  // duty cycle of each switch
92  // sw1 is the top switch of the upper-leg ... sw_N is the bottom
      switch of the upper-leg
93  //                A               B               C
94  // sw1  duty_phA_sw1  duty_phB_sw1  duty_phC_sw1
95  // sw2  duty_phA_sw2  duty_phB_sw2    duty_phC_sw2
96  // sw3  duty_phA_sw3  duty_phB_sw3    duty_phC_sw3
97  // ...
98  // swN  duty_phA_swN  duty_phB_swN    duty_phC_swN
99
100 // sum up the duty cycles for each switch
101
102 for (i=0; i<3; i++)           // 3 phase
103 {
104     for (j=0; j<N_layer; j++)
105     // switch index. "j = 0" corresponds to top switch.
106     {
107       duty_sw[j][i] = 0;
108       for(k=0; k<=j; k++)
109       // sum up the duty cycle from state N_layer until state 1
110       {
111         duty_sw[j][i] += duty_state[N_layer-1-k][i];
112       }
113     }
114 }
```

The matrix *duty_sw* is the final output of the modulator and contains the duty cycle of each switch of the 3-phase 5-level NPC converter.

Appendix B

The PCB layout of the basic boards of the medium voltage generator drive described in Chapter 5 are attached here.

- In Fig. 1 the PCB that receives the current, voltage and encoder measurement signals from the measurement devices of the drive is shown. This PCB has got four copper layers, with the top and bottom layers being available for connecting the components on the board and the middle two layers being occupied with the $V_{CC} = 3$V and the ground potential, respectively. A picture of this board is shown in Fig. 5.12.
- The PCB in Fig. 2 converts the electrical PWM signal from the microcontroller into optical signal through fiber optic transmitters. It is also made of four copper layers and its schematic has been shown in Fig. 5.13.
- The PCB layout of the gate driver described in Subsection 5.2.1 is shown in Fig. 3. This board, like all the power PCBs of the system, is made of two copper layers.

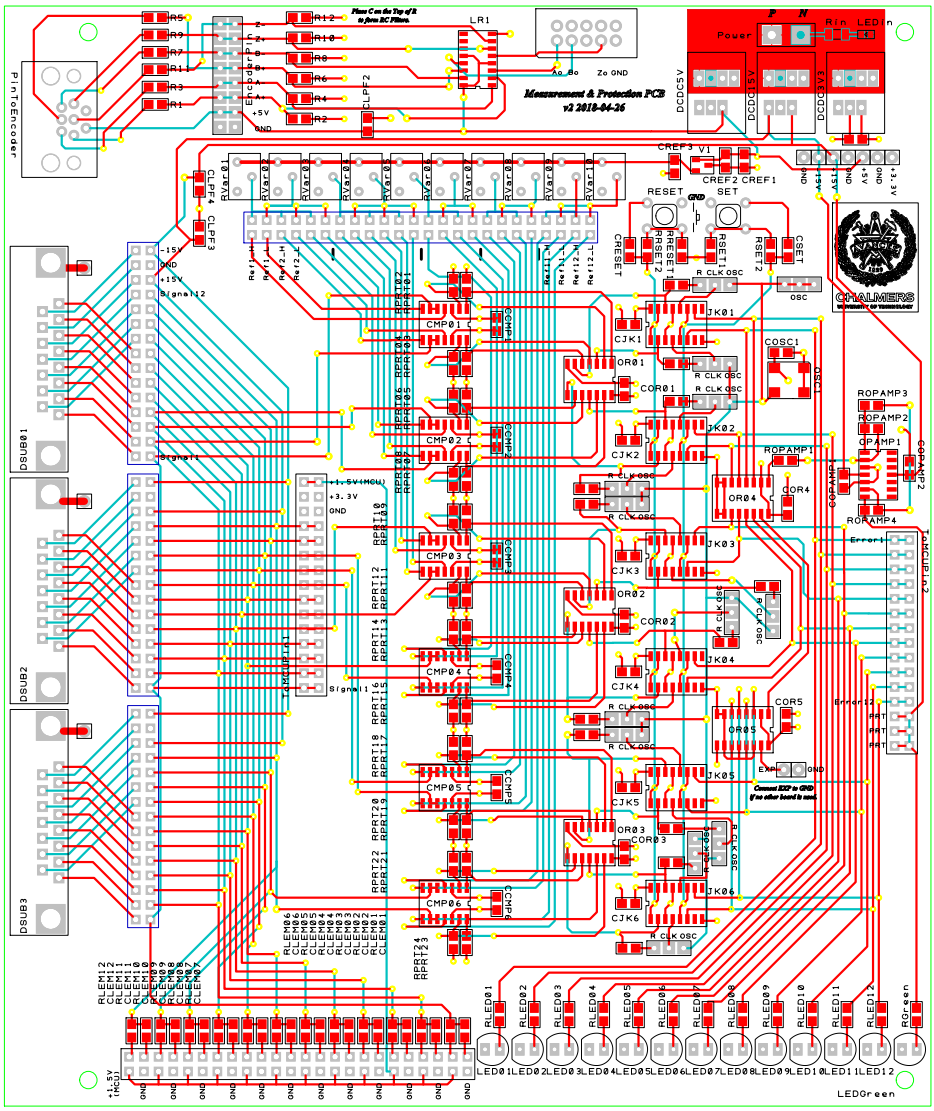


Fig. 1: PCB layout of the measurements and hardware protection board: red and blue lines show the traces of the top and bottom copper layers, respectively

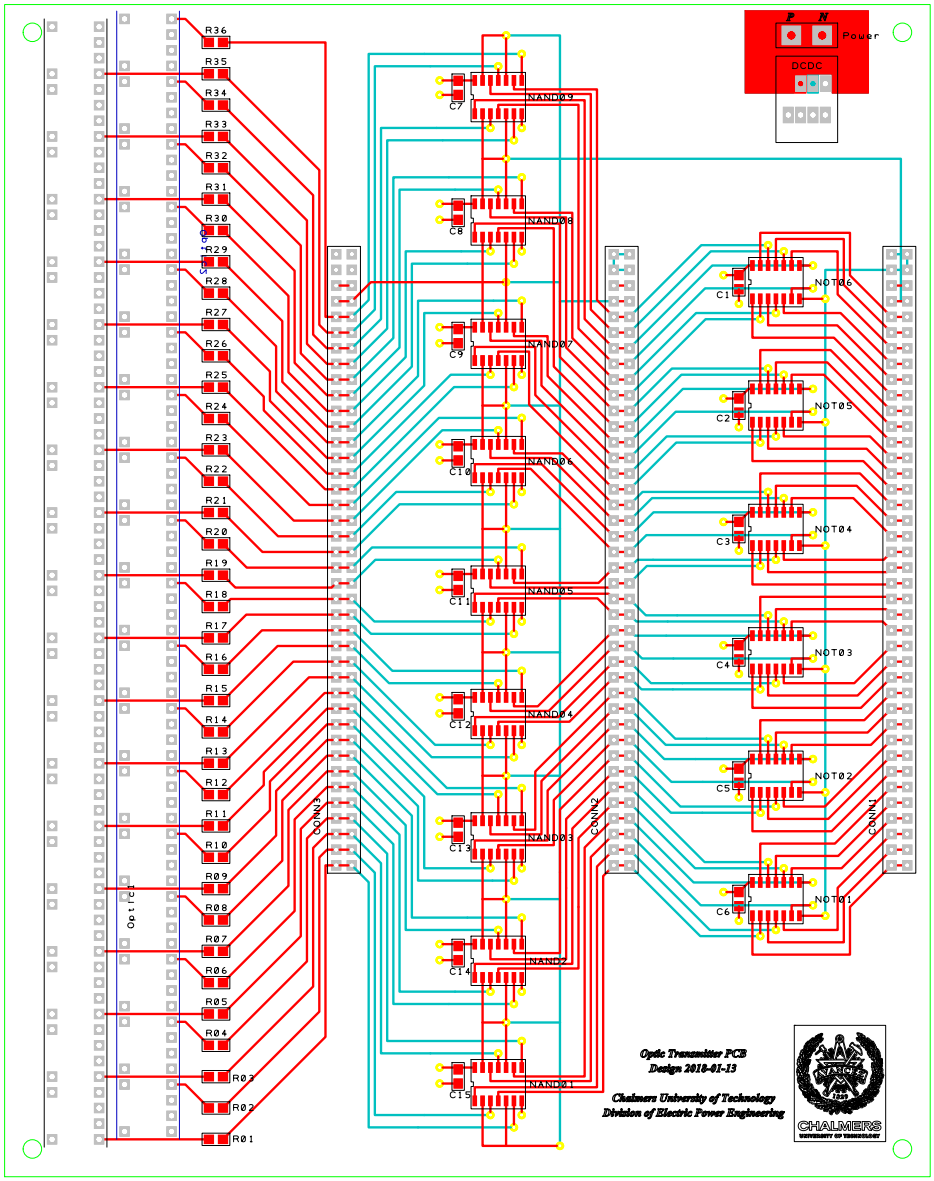
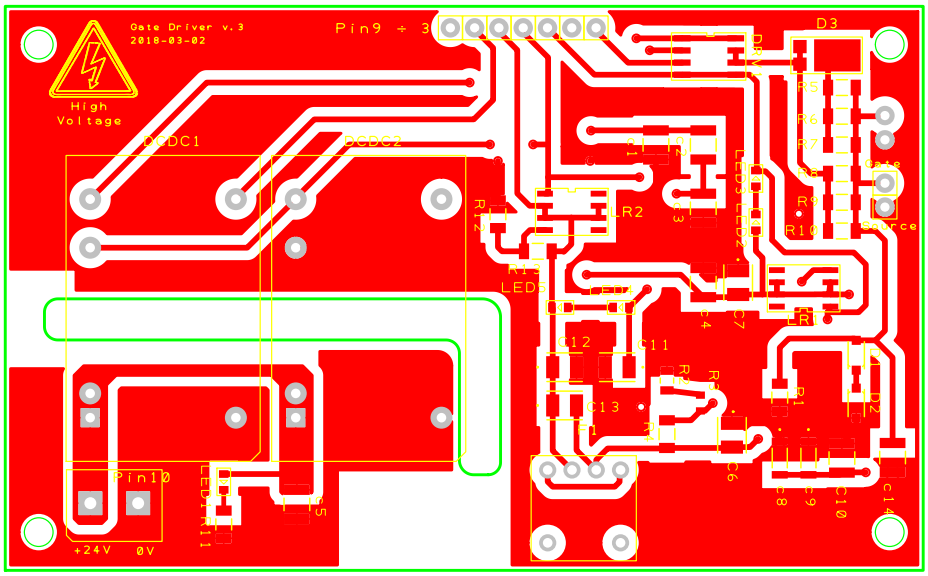
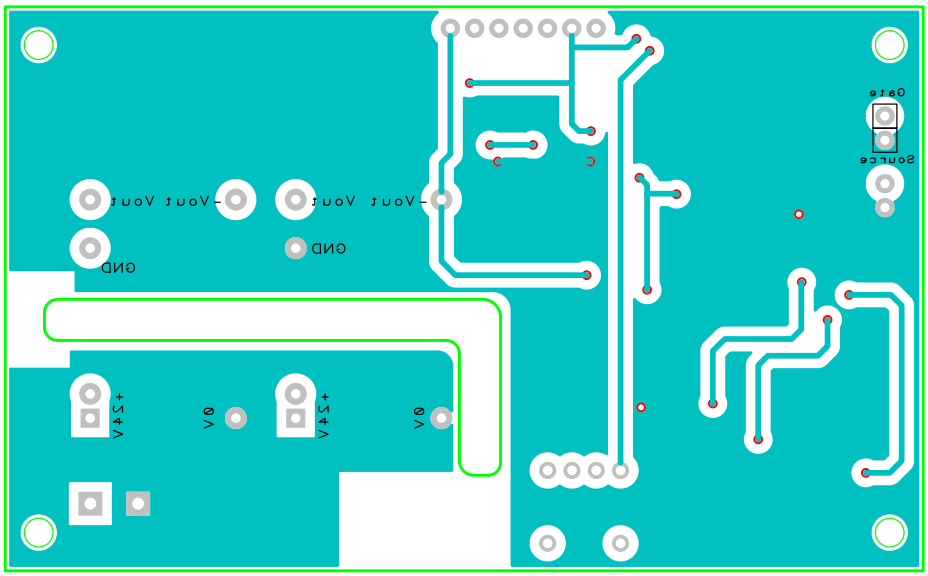


Fig. 2: PCB layout of the PWM board: red and blue lines show the traces of the top and bottom copper layers, respectively



(a)



(b)

Fig. 3: PCB layout of the Gate driver for the SCH2080KE SiC MOSFET: (a) top and (b) bottom copper layer