High-hole mobility Si1-xGex (0.1 x 1) on an insulator formed by advanced solid-phase crystallization

著者（英）	D. Takahara, R. Yoshimine, Takashi SUEMASU, Kaoru TOKO
journal or publication title	Journal of alloys and compounds
volume	766
page range	417-420
year	2018-10
権利	(C) 2018. This manuscript version is made available under the CC-BY-NC-ND 4.0 license http://creativecommons.org/licenses/by-nc-nd/4.0/
URL	http://hdl.handle.net/2241/00155056

doi: 10.1016/j.jallcom.2018.06.357

High-hole mobility $Si_{1-x}Ge_x$ ($0.1 \leq x \leq 1$) on an insulator formed by advanced solid-phase crystallization

D. Takahara[1], R. Yoshimine[1], T. Suemasu[1], and K. Toko[1,2,a)]

[1] Institute of Applied Physics, University of Tsukuba, 1-1-1 Tennodai, Tsukuba, Ibaraki 305-8573, Japan

[2] PRESTO, Japan Science and Technology Agency, 4-1-8 Honcho, Kawaguchi, Saitama 332-0012, Japan

[a)] Author to whom correspondence should be addressed.
Electronic mail: toko@bk.tsukuba.ac.jp

The grain size and hole mobility of polycrystalline $Si_{1-x}Ge_x$ thin films formed on glass by solid-phase crystallization were significantly improved after preparing the amorphous precursors by heating the substrate. By just controlling the deposition temperature of the precursors (50–350 °C) for each SiGe composition, the grain size reached over 2 μm across the whole composition range. Reflecting the enlargement of the grain size, the hole mobility values were improved by approximately one order of magnitude. These values are comparable to those of single-crystal SiGe formed by Ge condensation and are the highest among SiGe on insulators synthesized at low temperature (<900 °C). The SiGe on insulator technology obtained in this study will greatly contribute to the development of SiGe-based electronic and optical devices.

Keywords: SiGe-on-insulator; Solid phase crystallization; Polycrystalline film; Large grain; High carrier mobility

I. INTRODUCTION

Tuning the composition SiGe alloys, an all proportional solid solution, enables a higher carrier mobility than Si[1–5] and results in a large light absorption coefficient at a given wavelength.[5,6] Therefore, SiGe-on-insulator (SGOI) structures have been widely investigated for their use in thin-film transistors,[7,8] thin-film solar cells,[9,10] and on-chip optical interconnects.[11,12] A large number of SGOI-forming methods have been developed: layer transfer,[13] Ge condensation,[4,14–16] laser annealing,[7,10] rapid-melting growth,[8,12] chemical-vapor deposition (CVD),[2,17,18] sputtering,[9] solid-phase crystallization (SPC),[3,19–22] and metal-induced crystallization[23,24] including layer exchange.[25–30] Despite the variety of methodologies, it is still difficult to obtain a large-area SGOI with excellent crystallinity and electrical characteristics by a simple method, suitable for practical applications.

SPC is one of the simplest techniques; it consists on the deposition and heat treatment of amorphous (a-) SiGe layers on insulators.[3,19–22] In addition, because Ge vacancies in polycrystalline (poly-) SiGe produce holes, auto doping to p-type is possible.[3] In recent years, the SPC of a-Ge has been actively investigated.[30–36] Very recently, we have dramatically improved the hole mobility of SPC-Ge from 140 to 340 cm^2/Vs by controlling the deposition temperature of an a-Ge precursor.[37] Furthermore, we achieved a Ge hole mobility of 450 cm^2/Vs by thickening the Ge film and post-annealing at 500 °C.[38] This hole mobility is the highest reported for a thin film formed on insulators at temperatures below the melting point of Ge (937 °C). In this study, we used the same technique for SiGe to fabricate SGOI structures and achieved high quality via a simple process. Moreover, we demonstrate that the grain size and hole mobility of SiGe can be greatly improved by controlling the deposition temperature of the a-SiGe precursors over a wide composition range.

II. EXPERIMENT

Figure 1(a) shows the process of sample preparation. The 200-nm-thick SiGe precursors were deposited on SiO_2 glass substrates using a Knudsen cell for Ge and an electron beam gun for Si in a molecular beam deposition system (base pressure: 5×10^{-7} Pa). The Ge composition, x, in the $Si_{1-x}Ge_x$ precursors was 0.1, 0.25, 0.5, 0.75, and 1; it was controlled by changing the deposition rate of Si and Ge up to 1.0 nm/min, respectively. We note that a pure Si sample ($x = 0$) was excluded because its sheet resistance was too high to measure the electrical properties unless impurity doping. The temperature of the substrate during deposition, T_d, ranged from 50 °C to 350 °C. T_d spontaneously increased from room temperature to 50 °C even though the substrate was not heated; this was due to the heat radiation from the Knudsen cell and the electron beam gun. The samples were then loaded into a conventional tube furnace under a N_2 (99.9%) atmosphere and annealed for 30 h at 450 °C for $x = 0.75$, 550 °C for $x = 0.5$, 600 °C for $x = 0.25$, and 650 °C for $x = 0.1$. All resulting samples were 1 cm^2 square size as representatively shown in Fig. 1(b).

III. RESULTS AND DISCUSSION

Figure 2(a) shows the Raman spectra obtained for $T_d = 50$ °C samples after annealing. The peaks corresponding to the Ge–Ge, Si–Ge, and Si–Si vibration modes are, respectively, located at around 300, 400, and 500 cm^{-1}. These spectra indicate that the SiGe layers were crystallized for every composition under each annealing condition. Considering that the growth rate improves as T_d increases,[37] the samples with $T_d > 50$ °C should be sufficiently crystallized at these annealing conditions. The experimentally obtained SiGe compositions, calculated from the Raman spectra using the equation proposed by Mooney *et al.*,[39] were very close to the expected compositions and independent of the measurement position and T_d. Figure 2(b) shows the scanning electron microscopy (SEM) image of the $Si_{0.5}Ge_{0.5}$ layer surface after annealing obtained at $T_d = 200$ °C. The contrast in the SEM image likely

corresponds to the crystal orientation visualized due to the electron channeling effects, which is characterized by SPC-Ge with large crystal grains and excellent carrier mobility.[37] Figure 2(c) shows the Ge elemental map of the $Si_{0.5}Ge_{0.5}$ layer obtained using the energy dispersive X-ray (EDX) spectrometer. The Ge distribution is uniform, suggesting that the in-plane composition of SiGe is also uniform.

The electron backscattering diffraction (EBSD) images in Fig. 3(a) show that the grains are randomly oriented and that the grain size strongly depends on T_d over the whole composition range. Figure 3(b) shows that, for every composition, the average grain size reaches a maximum at a certain T_d and then decreases again. This behavior possibly arises from the precursor conditions, determined by three regimes: the low-density, high-density, and nucleation regimes.[37,38] The grain is the largest at the high-density regime because of the elevated growth rate of SiGe crystals. As x decreases, the T_d at which the grain size becomes maximum rises. This result reflects the fact that the temperature required for crystallization increases as x in $Si_{1-x}Ge_x$ decreases.[19–21,23] Generally, in SPC, the grain size tends to diminish as x increases.[20] This is attributed to the difference in the activation energies of Si and Ge required for nucleation and growth.[21,30] Here, we observed that large grains can be obtained even for Ge-rich SiGe by controlling T_d. The window at which T_d has an effect of increasing the grain size narrows as x increases, though $x = 0.1$ does not follow this trend. The cause is yet to be understood, but it is possibly related to the growth temperature. Thus, crystal grains of more than 2 μm were obtained for all of the compositions by controlling T_d.

The electrical properties of the resulting poly-SiGe layers were evaluated via Hall effect measurements. The $Si_{0.9}Ge_{0.1}$ sample with $T_d = 50$ °C could not be measured because of the high sheet resistance. All of the other samples showed p-type conduction, similar to conventional non-doped SPC-SiGe.[3] Figure 4(a) shows that the hole concentration remains practically constant with T_d at each x and is dramatically reduced with decreasing x. Because

dangling bonds in Ge provide shallow acceptor levels and then generate holes at room temperature,[40] the decrease in the hole concentration with decreasing x likely reflects the reduction in hole-generating Ge vacancies. Figure 4(b) shows that hole mobility strongly depends on both x and T_d. For each Ge composition, the mobility reaches a maximum in the vicinity of the T_d at which the crystal grain size is the largest. The maximum value of hole mobility decreases as x decreases. This behavior is the same as that of bulk SiGe[1] and is attributed to the fact that Si has a lower hole mobility and a higher grain boundary potential than Ge.[7,37,41]

The hole mobility for each x with the optimum T_d is plotted in Fig. 5. For comparison, the carrier mobility of poly-SiGe prepared by conventional SPC, CVD, and Ge condensation is presented. The hole mobility of SPC-SiGe with no heating deposition (T_d = 50 °C) obtained in this study is close to those previously reported.[3] Some deviation, especially in Si-rich compositions, may reflect the differences in the deposition method, growth temperature, and hole concentration affecting the grain boundary potential. The results demonstrate that the hole mobility can be dramatically improved over a wide composition range by optimizing T_d. The mobility values obtained in this study significantly exceed the carrier mobilities of CVD-SiGe.[5] This mainly reflects the difference in grain size; however, the comparison may not be adequate considering that CVD-SiGe is obtained at low temperature (200 °C) to achieve low carrier concentrations. Furthermore, these mobility values are comparable to those of single-crystal SiGe obtained from a Ge condensation process (≥900 °C), which are the highest SGOI's Hall hole mobility.[4] Among the SiGe alloys formed on glass at low temperature (<900 °C), the current SiGe layers are of the highest quality reported.

IV. CONCLUSION

The deposition temperature T_d of the precursor for SPC strongly influenced the crystal

quality and electrical properties of the resulting poly-SiGe layers on glass. By controlling T_d for each SiGe composition, the grain size was dramatically enlarged, reaching 2 μm or more over the whole composition range. The hole concentration decreased as the Si composition increased probably because of the reduction of Ge vacancies. Reflecting the large crystal grain size, the high hole mobility values were achieved as Ge-rich SGOIs were synthesized at low temperature (<900 °C). The technique used to obtain SGOIs is quite simple, allowing for the practical application of SiGe-based electronic and optical devices.

ACKNOWLEDGEMENTS

This work was financially supported by the Asahi Glass Foundation, the Kato Foundation for Promotion of Science, and the JST PRESTO (No. JPMJPR17R7). The authors are grateful to Prof. T. Sakurai for the Hall effect measurements. Some experiments were performed at the International Center for Young Scientists in NIMS and the Nanotechnology Platform in the University of Tsukuba.

REFERENCES

[1] M. Fischetti and S. Laux, J. Appl. Phys. **80**, (1996).

[2] J.A. Tsai, A.J. Tang, T. Noguchi, and R. Reif, J. Electrochem. Soc. **142**, 3220 (1995).

[3] Y. Aya, K. Takeda, K. Wakisaka, and K. Nishio, Jpn. J. Appl. Phys. **42**, L1308 (2003).

[4] N. Hirashita, Y. Moriyama, S. Nakaharai, T. Irisawa, N. Sugiyama, and S.I. Takagi, Appl. Phys. Express **1**, 1014011 (2008).

[5] T. Matsui, M. Kondo, K. Ogata, T. Ozawa, and M. Isomura, Appl. Phys. Lett. **89**, 142115 (2006).

[6] N. Usami, W. Pan, K. Fujiwara, M. Tayanagi, K. Ohdaira, and K. Nakajima, Sol. Energy Mater. Sol. Cells **91**, 123 (2007).

[7] H. Watakabe, T. Sameshima, H. Kanno, T. Sadoh, and M. Miyao, J. Appl. Phys. **95**, 6457 (2004).

[8] Y. Tojo, R. Matsumura, H. Yokoyama, M. Kurosawa, K. Toko, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **102**, 092102 (2013).

[9] C.-Y. Tsao, Z. Liu, X. Hao, and M.A. Green, Appl. Surf. Sci. **257**, 4354 (2011).

[10] Z. Liu, S. Noh, X. Hao, J. Huang, A. Ho-Baillie, and M.A. Green, J. Alloys Compd. **744**, 679 (2018).

[11] Y. Kim, M. Takenaka, T. Osada, M. Hata, and S. Takagi, Sci. Rep. **4**, 4683 (2014).

[12] C.G. Littlejohns, M. Nedeljkovic, C.F. Mallinson, J.F. Watts, G.Z. Mashanovich, G.T. Reed, and F.Y. Gardes, Sci. Rep. **5**, 8288 (2015).

[13] G. Taraschi, A.J. Pitera, and E.A. Fitzgerald, Solid. State. Electron. **48**, 1297 (2004).

[14] T. Tezuka, N. Sugiyama, and S. Takagi, Appl. Phys. Lett. **79**, 1798 (2001).

[15] M. Mitsui, K. Arimoto, J. Yamanaka, K. Nakagawa, K. Sawano, and Y. Shiraki, Appl. Phys. Lett. **89**, 21 (2006).

[16] H. Yang, D. Wang, and H. Nakashima, Appl. Phys. Lett. **95**, 1 (2009).

[17] A.A. Shklyaev, V.I. Vdovin, V.A. Volodin, D.V.Gulyaev, A.S. Kozhukhov, M. Sakuraba, and J. Murota, Thin Solid Films **579**, 131 (2015).

[18] K. Tao, J.Wang, R. Jia, Y. Sun, Z. Jin, and X. Lin, Scr. Mater. **107**, 100 (2015).

[19] S. Park, S. Yamaguchi, N. Sugii, K. Nakagawa, and M. Miyao, Appl. Surf. Sci. **159-160**, 116 (2000).

[20] J. Olivares, A. Rodríguez, J. Sangrador, T. Rodríguez, C. Ballesteros, and A. Kling, Thin Solid Films **337**, 51 (1999).

[21] K. Toko, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **94**, 192106 (2009).

[22] M. Tada, J.-H. Park, J.R. Jain, and K.C. Saraswat, J. Electrochem. Soc. **156**, D23 (2009).

[23] K. Toko, H. Kanno, A. Kenjo, T. Sadoh, T. Asano, and M. Miyao, Appl. Phys. Lett. **91**, 042111 (2007).

[24] S. Peng, X. Shen, Z. Tang, and D. He, Mater. Chem. Phys. **107**, 431 (2008).

[25] M. Gjukic, M. Buschbeck, R. Lechner, and M. Stutzmann, Appl. Phys. Lett. **85**, 2134 (2004).

[26] M. Kurosawa, N. Kawabata, T. Sadoh, and M. Miyao, ECS J. Solid State Sci. and Tech. **1**, 144 (2012).

[27] T. Zhang, F. Ma, and W. Zhang, Appl. Phys. Lett. **100**, 071908 (2012).

[28] C.A. Niedermeier, Z. Wang, and E.J. Mittemeijer, Acta Mater. **72**, 211 (2014).

[29] M. Nakata, K. Toko, N. Saitoh, N. Yoshizawa, and T. Suemasu, Scr. Mater. **122**, 86 (2016).

[30] K. Toko, K. Kusano, M. Nakata, and T. Suemasu, J. Appl. Phys. **122**, 155305 (2017).

[31] K. Toko, I. Nakao, T. Sadoh, T. Noguchi, and M. Miyao, Solid. State. Electron. **53**, 1159 (2009).

[32] C.-Y. Tsao, J. Huang, X. Hao, P. Campbell, and M. A. Green, Sol. Energy Mater. Sol. Cells **95**, 981 (2011).

[33] H.-W. Jung, W.-S. Jung, H.-Y. Yu, and J.-H. Park, J. Alloys Compd. **561**, 231 (2013).

[34] S. Kabuyanagi, T. Nishimura, K. Nagashio, and A. Toriumi, Thin Solid Films **557**, 334 (2014).

[35] W. Takeuchi, N. Taoka, M. Kurosawa, M. Sakashita, O. Nakatsuka, and S. Zaima, Appl. Phys. Lett. **107**, 22103 (2015).

[36] T. Sadoh, Y. Kai, R. Matsumura, K. Moto, and M. Miyao, Appl. Phys. Lett. **109**, 232106 (2016).

[37] K. Toko, R. Yoshimine, K. Moto, and T. Suemasu, Sci. Rep. **7**, 16981 (2017).

[38] R. Yoshimine, K. Moto, T. Suemasu, and K. Toko, Appl. Phys. Exp. **11** (2018).

[39] P.M. Mooney, F.H. Dacol, J.C. Tsang, and J.O. Chu, Appl. Phys. Lett. **62**, 2069 (1993).

[40] H. Haesslein, R. Sielemann, and C. Zistl, Phys. Rev. Lett. **80**, 2626 (1998).

[41] J.W.Y. Seto, J. Appl. Phys. **46**, 5247 (1975).

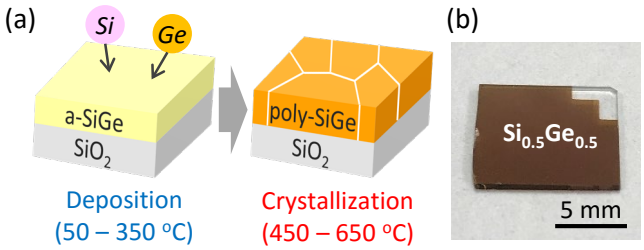

FIG. 1. (a) Schematic image of the sample preparation procedure. (b) Photograph of a sample with $x = 0.5$ and $T_d = 200$ °C after annealing at 550 °C for 30 h.

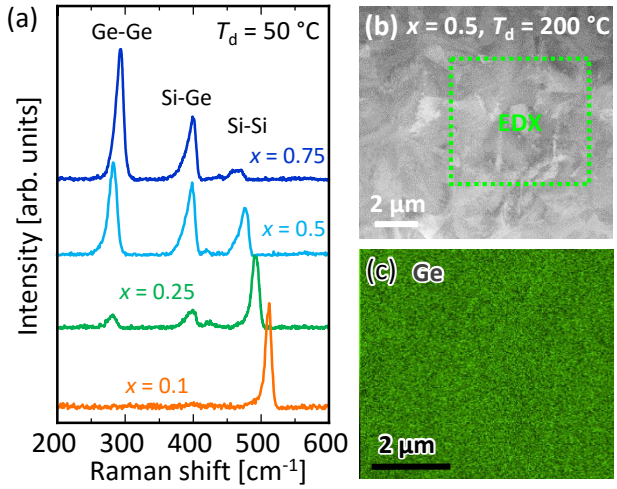

FIG. 2. (a) Raman spectra of the samples with T_d = 50 °C after annealing for SPC. (b) SEM image and (c) EDX elemental map of Ge for the sample with x = 0.5 and T_d = 200 °C after annealing at 550 °C for 30 h.

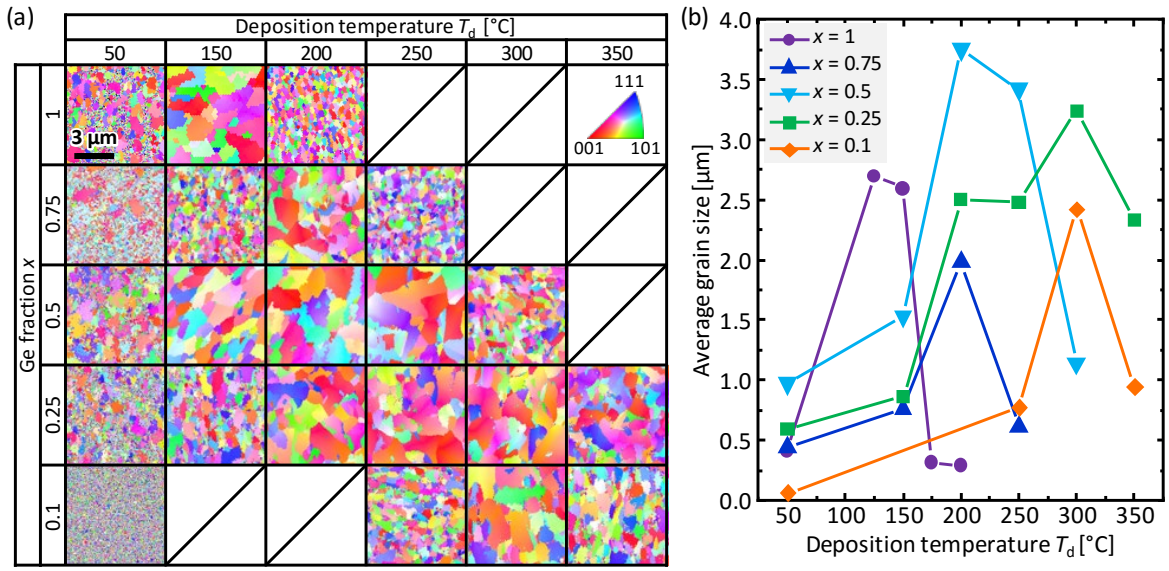

FIG. 3. Grain size of the SPC-$Si_{1-x}Ge_x$ layers. (a) EBSD images of SPC-$Si_{1-x}Ge_x$ summarized as the matrix composed of T_d (50 °C, 150 °C, 200 °C, 250 °C, 300 °C, and 350 °C) and x (1, 0.75, 0.5, 0.25, and 0.1). The colors indicate the crystal orientation according to the inserted color key. (b) T_d dependence of the average grain size calculated from the EBSD images for x = 0.1–1.

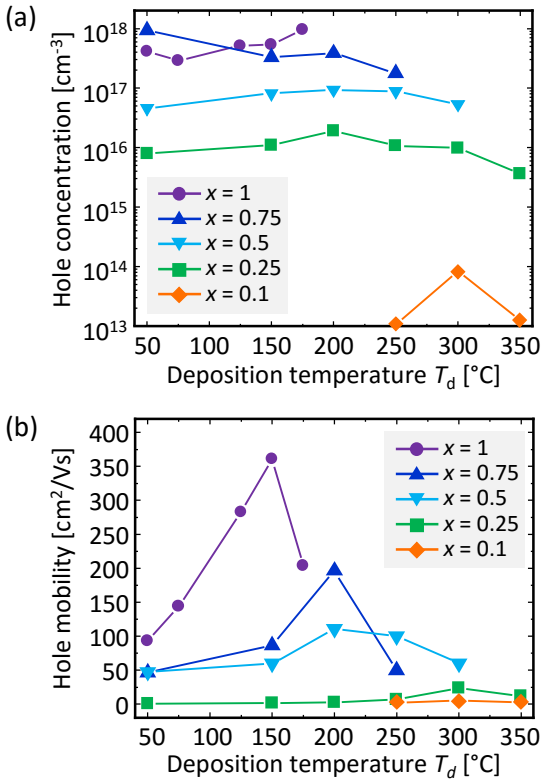

FIG. 4. Electrical properties of the SPC-$Si_{1-x}Ge_x$ layers for x = 0.1–1, obtained from Hall effect measurements with the Van der Pauw method. (a) Hole concentration and (b) hole mobility as a function of T_d. These values were averaged over five measurements for each sample.

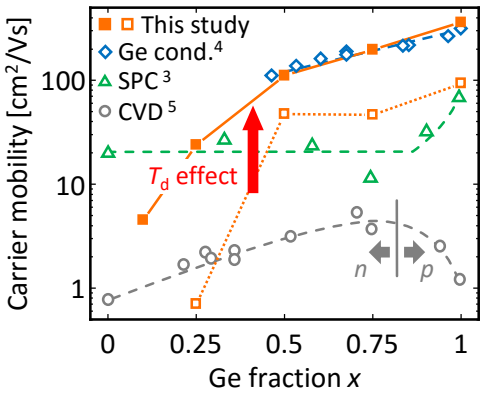

FIG. 5. Hole mobility of SPC-$Si_{1-x}Ge_x$ as a function of x, where the precursors were prepared with heating (closed squares: T_d = 150 °C for x = 1, 200 °C for x = 0.75 and 0.5, and 300 °C for x = 0.25 and 0.1) and without heating (open squares: T_d = 50 °C) during deposition. The data of conventional $Si_{1-x}Ge_x$ obtained by SPC,[3] CVD,[5] and Ge condensation[4] are shown for comparison. The carrier type is electron for CVD-$Si_{1-x}Ge_x$ ($x \leq 0.75$) and hole for the others.