# A Noise Immune Technique to Suppress the Temporal Noise for Wide Dynamic Range CMOS Sensors

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## Abstract

A CMOS image sensor architecture is presented that uses an extra level of parallelism and thermal and 1/f noise suppression techniques to achieve both low-light detection and a high frame rate. By adding the row-parallel readout ADCs, the conversion speed is improved by more than twice compared to the conventional top-bottom parallel ADC structure. The thermal and 1/f noise is reduced by combining the intrinsic oversampling of the incremental sigma-delta ADCs and the 1/f noise suppression through the source-follower inversion-to accumulation method. The chip contains 164 pads, including 24 LVDS drivers. Rows and columns follow the same readout paths. The pixels are surrounded by the pixel-bias circuits and by the switches for cycling the source follower of the pixels from inversion to accumulation for low-frequency noise reduction. The ADC is the key building block of the designed imager.

## Introduction

IN CMOS image sensors, the continuous increase of the spatial resolution directly affects the frame rate of the sensor. However, a narrow bandwidth readout circuit for low noise purpose conflicts with the frame rate desire. Therefore, the increase in parallelism is a very effective way to improve the frame rate without raising the noise level. A high parallelism with multiple stacked column ADCs sharing the same column pitch, however, introduces cross-coupling issues and layout challenges [1]. Recently, the stacking architecture has been a trend of image sensors to improve the readout parallelism [2]. Nevertheless, the high cost, the technology complexity, and the heat issue prevent the stacked image sensors from being popular. Therefore, a simple monolithic architecture to improve both the frame rate and the noise performance by enhancing the parallelism is highly desired. Regarding the CMOS image sensor noise, high-gain column amplifiers [3], have been shown to be effective in narrowing the noise spectrum bandwidth and suppressing the noise of following stages in the signal readout chain. However, the amplifying analog circuitry suffers from the nonlinearity and the variation among columns. Furthermore, the amplifiers and the buffers to drive the column ADCs also take a significant amount of power and area. As a result, a better noise performance of the column amplification approach is achieved with unpleasant costs in the calibration processing, and power and area consumption. Meanwhile, incremental sigma-delta (ISD) ADCs [4] have been recently proven to be effective in reducing the pixel thermal noise by multiple sampling without using a high-gain column amplifier. However, the 1/f noise is almost not affected by either the oversampling conversion or the amplification. The inversion-to-accumulation technique [5] has been shown to reduce the 1/f noise by cycling alternatively a NMOS from inversion to accumulation mode. However, a single cycling operation as in [5] is only effective if the ADC conversion time is short enough such that the traps are not numerously generated during the inversion phase of the pixel source follower (SF).

## The Quadrant Architecture of CMOS Image Sensors

The increase of pixels per column directly affects the frame rate of the sensor. For instance, a 33MPixel image sensor [6] has a column resolution of 4320 pixels, all to be read by the same ADC. If a frame rate of 240fps is required, the total pixel readout time should be below 1μs, which requires a huge design effort, especially when a high-resolution conversion with the digital correlated double sampling (DCDS) are simultaneously to be achieved. And, even such a pixel readout time has been reached, the noise level could not fall below 5e- due to the noisy high-bandwidth readout [6]. Therefore, to achieve high frame rate combined with a low-bandwidth, a higher level of parallelism is needed.

In order to improve the parallelism, an approach with two column-shared ADCs [1] was proposed to fit two column ADCs in one side of the focal plane array (FPA). However, there may be problems with layout of power, reference, clocks, analog and digital signals because the column ADCs are monolithically arranged in two layers posing a high mismatching potential. Fig. 1 shows the overall architecture of the proposed quadrant CMOS image sensor. The focal plane array is divided into four quadrants, each having their own ADCs and control blocks, which can work independently. In addition to column ADCs, row ADCs are placed to enhance the readout speed. As a result, ADCs are arranged symmetrically in all four edges of the FPA.

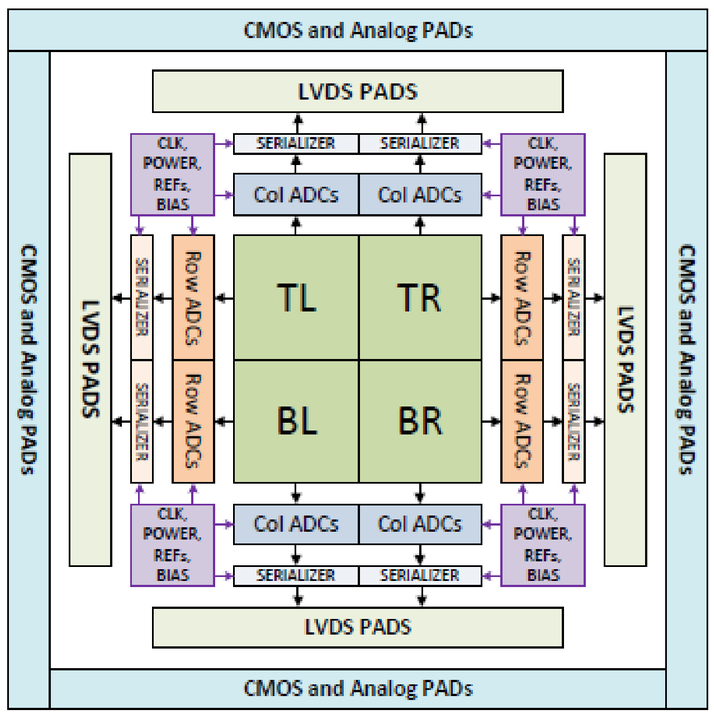


Figure 1:The quadrant architecture for CMOS image sensors

The serializers and digital I/O pads are accordingly placed in series with ADCs. The clock, power, reference, and bias lines are distributed from all four corners of the FPA. A highly symmetrical and short routing layout of power, reference, analog and digital signals is hence obtained. This advantage is very important for CISs, especially for those with large FPA, in which the power drop is a serious problem.

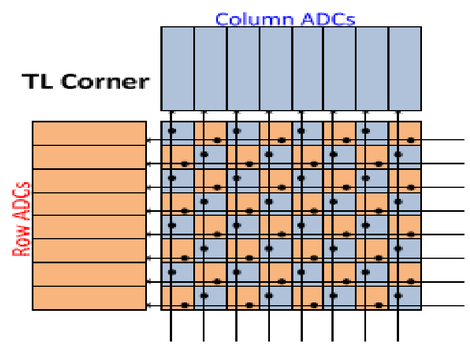


Figure 2:The top-left quadrant with column and row ADCs,

## Conclusion

By increasing the parallelism, techniques have been presented to improve the frame rate by a factor of two, in addition to improving the low light detection through the intrinsic oversampling of incremental sigma-delta ADCs combined with a 1/f noise reduction technique.. Furthermore, it is obvious that this methodology of noise analysis can be extended and used for more complex architectures.

## References

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