Feasibility of Geiger-mode avalanche photodiodes in CMOS standard technologies for tracker detectors

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Preface and organization

Each generation of particle colliders is built with the purpose to perform a series of HEP (High Energy Physics) experiments so as to explore a specific area of particle physics. The experiments conducted at the LHC (Large Hadron Collider), the most powerful particle collider ever built, confirmed the existence of a new particle, presumably the Higgs boson, in 2012. Nevertheless, to determine the properties of the new particle with high precision, refine measurements need to be done. Despite the extraordinary capabilities of the LHC, this machine is not suited for such a target since its precision is intrinsically limited by its proton synchrotron nature.

To solve this issue, the HEP community has already started to look at the post LHC-era. There is a global consensus that it will be characterized by linear lepton colliders, where the collisions between electrons and positrons will allow to probe deeply into the new particle. At present time, there are two alternative projects underway, namely the ILC (International Linear Collider) and CLIC (Compact LInear Collider). From the detector point of view, the physics aims at these particle colliders impose such extreme requirements, that there is no sensor technology available in the market that can fulfill all of them. As a result, several new detector systems are being developed in parallel with the accelerator. The concept of the ILC and CLIC machines is reviewed in Chapter 1, together with a summary of the requirements on tracking detector systems and the main features of the tracking detector candidates proposed so far. Other potential applications apart from particle tracking at future linear colliders, such as the TOTEM experiment at LHC and biomedical imaging, are also outlined in Chapter 1.

This thesis presents the development of a GAPD (Geiger-mode Avalanche PhotoDiode) pixel detector aimed mostly at particle tracking at future linear colliders. GAPDs offer outstanding qualities to meet the challenging requirements of ILC and CLIC, such as an extraordinary high sensitivity, virtually infinite gain and ultra-fast response time, apart from compatibility with standard CMOS technologies. In particular, GAPD detectors enable the direct conversion of a single particle event onto a CMOS digital pulse in the sub-nanosecond time scale without the utilization of either preamplifiers or pulse shapers. As a result, GAPDs can be read out after each single bunch crossing, a unique quality that none of its competitors can offer at the moment. In spite of all these advantages, GAPD detectors suffer from two main problems. On the one side, there exist noise phenomena inherent to the sensor, which induce noise pulses that cannot be distinguished from real particle events and also worsen the detector occupancy to unacceptable levels. On the other side, the fill-factor is too low and gives rise to a

reduced detection efficiency. The most important aspects of the GAPD technology are reviewed in Chapter 2.

Solutions to the two problems commented that are compliant with the severe specifications of the next generation of particle colliders have been thoroughly investigated. Chapter 3 presents the design and characterization of several single pixels and small arrays that incorporate some elements to reduce the intrinsic noise generated by the sensor. The sensors and the readout circuits have been monolithically integrated in a conventional HV-CMOS 0.35 μm process. Concerning the readout circuits, both voltage-mode and current-mode options have been considered. Moreover, the time-gated operation has also been explored as an alternative to reduce the detected sensor noise. Chapter 4 deals about the design and characterization of a prototype GAPD array, also monolithically integrated in a conventional 0.35 μm HV-CMOS process. The detector consists of 10 rows x 43 columns of pixels, with a total sensitive area of 1 mm x 1 mm. The array is operated in a time-gated mode and read out sequentially by rows. The efficiency of the proposed technique to reduce the detected noise is shown with a wide variety of measurements. Further improved results are obtained with the reduction of the working temperature. Finally, the suitability of the proposed detector array for particle detection is shown with the results of a beam-test campaign conducted at CERN-SPS (European Organization for Nuclear Research-Super Proton Synchrotron). In Chapter 5, a series of additional approaches to improve the performance of the GAPD technology are proposed. The benefits of integrating a GAPD pixel array in a 3D process in terms of overcoming the fill-factor limitation are examined first. The design of a GAPD detector in the Global Foundries 130 nm/Tezzaron 3D process is also presented. Moreover, the possibility to obtain better results in light detection applications by means of the time-gated operation or correction techniques is analyzed too.

Finally, the conclusion section summarizes the most significant results presented over the different chapters of this thesis.

Key words: Geiger-mode avalanche photodiode, APD, afterpulsing, beam-test, CLIC, CMOS, crosstalk, dark count rate, fill-factor, future linear lepton colliders, GAPD array, ILC, image sensor, low-noise, non-uniformities correction techniques, readout circuit, SiPM, SPAD, time-gated operation, tracker detector, 3D technologies.

Chapter 1

Future linear lepton colliders and other potential applications

A linear lepton collider operating in the TeV energy scale is needed to study in great detail the underlying physics of the discoveries made at the LHC (Large Hadron Collider) just recently. To fully exploit the physics potential of this endeavor, detector systems capable of unprecedented performance are required. Amongst other technology options, sensors based on APDs (Avalanche PhotoDiodes) and aimed at particle tracking at the next generation of particle colliders are being developed. An APD is implemented as a photodiode reverse biased near or above the breakdown voltage of the junction. When an APD is biased below breakdown, it is known as proportional or linear APD. Linear APDs show a limited optical gain and therefore they can be used to detect only clusters of photons or particles. In contrast, when biased above breakdown, the optical gain of these sensors becomes virtually infinite and they are capable to detect single photons and particles. APDs operating in this regime, known as Geiger-mode, are called GAPDs (Geiger-mode Avalanche PhotoDiodes) or SPADs (Sinlge-Photon Avalanche Diodes).

This chapter reviews the current state of particle colliders and also introduces the proposals for the future linear lepton colliders, namely ILC (International Linear Collider) and CLIC (Compact LInear Collider). Special attention is paid to the requirements demanded on tracking detector systems. Moreover, the several tracking technology options proposed so far are examined, detailing in each case the extent of fulfillment of the demanded requirements. Finally, other potential applications such as experiments at other particle colliders and biomedical imaging are also outlined.

1.1 Current state of particle colliders

HEP (High Energy Physics) is the branch of science that seeks the understanding of the smallest constituents of Nature. In particular, the SM (Standard Model) of particle physics provides a good description of the fundamental particles as well as the interactions between them [1-3]. A fundamental or elementary particle is a particle not known to have any substructure, then it is one of the building blocks of the Universe from which all other particles

are made. According to the SM, there are 6 quarks (known as the flavors up, down, charm, strange, top and bottom), 6 leptons (known as the flavors electron, muon, tau, electron neutrino, muon neutrino and tau neutrino), 4 gauge bosons (photon, gluon, W and Z) and 1 Higgs boson, which together with the quarks, leptons and W boson antiparticles as well as the quarks and gluon colors make a total of 61 elementary particles. The fundamental interactions described by this theory are the electromagnetic, weak and strong forces. The SM was developed in the early 1970's and today it is a well tested model thanks to the large variety of HEP experiments that have been carried out since then.

HEP experiments are conducted using particle accelerators and detectors. Accelerators boost beams of particles to GeV energies before they are made to collide with each other. Detectors observe and record the results of these collisions. At present time, there exist two types of high energy accelerators. On the one hand, synchrotrons, where the accelerated particles follow a high energy constant radius in a time varying magnetic field. On the other hand, linear accelerators, where particles have a linear motion. The accelerated beams of particles are made to collide in the detector region. Usually, the detector, which is composed of several subdetectors performing different purposes, presents a cylindrical symmetry.

Currently, the world's most powerful particle accelerator is the LHC, which is located at CERN (European Organization for Nuclear Research) near Geneva (Switzerland) [4]. In this machine, two beams of hadrons (either protons or heavy ions) are accelerated in opposite directions in a 27 km ring buried underground. The beams are guided around the accelerator ring by a strong magnetic field, achieved using superconducting electromagnets. In the final state of the LHC, the accelerated beams of hadrons will reach the unprecedented energy of 7 TeV each at a nominal luminosity (i.e. the number of particles per unit area per unit time) of $1 \cdot 10^{34}$ $cm^{-2}s^{-1}$. The collisions take place inside the four main detectors placed over ring, which are ATLAS, CMS, ALICE and LHCb. Three further experiments, TOTEM, LHCf and MoEDAL, are respectively positioned near the CMS, ATLAS and LHCb detectors. Amongst other discoveries and findings, experiments conducted at the LHC confirmed the existence of a new particle in 2012. The new particle is presumably the Higgs boson, the last missing piece of the SM model that is responsible for the intrinsic mass of particles [5, 6], and it needs to be studied in great detail to precisely determine its properties. However, despite the extraordinary capabilities of the LHC, the precision of this machine is intrinsically limited because it collides hadrons against hadrons. Hadrons are not fundamental particles. Instead, they are made up of quarks, antiquarks and the gluons that hold them together. In these non-fundamental particles, the energy is shared out between its partons in a constantly changing way. Therefore, the initial energy of the two colliding beams in an hadron collider such as the LHC cannot be determined very accurately. Moreover, due to strong interactions, the signal to background ratio is very low.

In order to provide a better description of the discoveries performed at the LHC, refiner measurements need to be done at a new particle collider. Steps towards the post-LHC era have already started. At the beginning of the millennium, the HEP community reached the consensus that a new lepton collider should be the next major facility for HEP experiments. In lepton colliders the accelerated particles are fundamental particles, basically electrons and positrons. Therefore, the energy of each particle is known. Precision measurements of interactions in a detector are possible, balancing the energy before the event with the energy observed afterwards. Hadrons and lepton machines compliment each other. Hadron colliders are useful for discovering new physics or searching for new particles. Differently, lepton colliders can be used for precision measurements of particles after having probed their existence.

However, building a circular lepton machine is not an option. When a particle is accelerated in a circular path, it suffers from energy losses in the form of electromagnetic radiation. These energy losses are known as synchrotron radiation. The synchrotron radiation is inversely proportional to the fourth power of the particle mass and the bending radius of the accelerator. As a proton is a heavy particle (~1836 times heavier than an electron), it is almost not affected by the synchrotron radiation. However, because the electron is so light, circular electron accelerators of only a few hundred GeV would suffer such large synchrotron radiation losses, that unfeasible energy compensations would be necessary to reach the nominal center-of-mass energy. For instance, the old LEP (Large Electron-Positron Collider), a circular lepton collider built at CERN that was operative from 1989 to 2000, precised an extra energy of 0.4 GeV to supply the 104 GeV nominal center-of-mass energy. By extension, a 500 GeV circular lepton collider with the same size as LEP would require an extra energy higher than 200 GeV. The severe increase of the orbit radius of the ring is also unviable due to the costs of such a civil engineering.

For all these reasons, the HEP community has chosen an e^+e^- linear collider as the next accelerator-based facility to complement and expand the discoveries emerged from the LHC. Moreover, it is also agreed that the nominal center-of-mass energy of this collider has to be in the TeV scale. Regarding the only experience with linear colliders operated so far, the 100 GeV SLAC (Stanford Linear Accelerator Center) National Accelerator Laboratory, researchers have now carried out more than two decades of research to study various solutions. At present time, there are two alternative proposals underway that could fulfill the requirements envisaged for future linear colliders: ILC and CLIC. The HEP community set up a new organization under the umbrella of ICFA (International Committee for Future Accelerators) in February 2013, the LCC (Linear Collider Collaboration), the aim of which is to coordinate the efforts towards the realization of a linear collider. Both machine concepts, ILC and CLIC, are represented in this new organization.

1.2 Proposals for future linear lepton colliders

A linear collider mainly consists of two opposing linear accelerators, which are named linacs. The particles are accelerated following a straight path in each linac, since they are extracted from the particle sources until they are smashed at the center-of-mass energy in the central IP (Interaction Point) located inside the detector. The particles reach their final energy in one go, and therefore very high accelerating gradients of several MeV/m are required in order to limit the length of the collider. Following the acceleration, the two beams collide only once. The particles are grouped together in the so-called bunches of particles. Then, each collision is typically referred as bunch crossing or BX. Several BXs separated by a short temporal gap form a bunch train.

The required luminosity for the target particle physics experiments can be reached only through the appropriate repetition rate (i.e. the frequency of the BXs), number of BXs in a bunch train, number of particles on each of the two colliding bunches, beam cross-section at the IP and mutual beam-beam interaction (i.e. each bunch is affected by the magnetic field created by the other one). In an e+e− collision, both particles feel attraction to each other because of the opposite charge, which enhances the luminosity. However, this attraction provokes a deflection in the trajectory of the particles, which causes them to radiate photons in a phenomenon known as beamstrahlung process. The beamstrahlung photons increase the beam-induced background hits, which are not related to particles created in genuine e+e− physics events and therefore unwanted. The beam-induced hits lead to high occupancies in the inner layers and must be coped with readout techniques or small area pixels.

A brief description of the ILC and CLIC proposals is provided in the following paragraphs. In Table 1.1, a summary of the main beam parameters for the ILC and CLIC colliders is presented.

1.2.1 The International Linear Collider

The ILC accelerator is designed to collide electrons and positrons towards each other at a nominal center-of-mass energy of 500 GeV, which could be increased to 1 TeV in a second phase. This accelerator covers a total length of 31 km, extendable to 50 km in the machine upgrade. The ILC project foresees a linear collider consisting of two sources of electrons and positrons, two damping rings with a circumference of 6.7 km each to pre-accelerate the particles, two 11 km long linacs and a 4.5 km beam delivery system to focus the beams to their final sizes and to bring them to collision [7]. The overall layout of ILC is shown in Fig. 1.1. The linacs are based on 1.3 GHz SCRF (SuperConducting Radio-Frequency) accelerating cavities

Beam parameters	ILC	CLIC
Center-of-mass energy	500GeV (1TeV)	500GeV (3TeV)
Luminosity ($\cdot 10^{34}$cm^{-2}s^{-1})	1.49 (2.70)	2.3 (5.9)
Train repetition rate (Hz)	5	50
Bunches/train	2820	354 (312)
Bunch separation (ns)	337	0.5
Number of particles/bunch ($\cdot 10^9$)	7.5	6.8 (3.72)
Horizontal beam size (nm)	640	200 (40)
Vertical beam size (nm)	5.7	2.26 (1)

Table 1.1 Comparison between the ILC and CLIC machines.

working at 2 K, which provides an average accelerating gradient of 31.5 MeV/m with an energy spread less than 0.1% [8]. The SCRF cavities are hollow structures that are filled with an electric field, the voltage of which changes from plus to minus with a certain frequency (the radio-frequency) to maximize the electric field while maintaining the power consumption within reasonable limits. The luminosity goal is around $2 \cdot 10^{34}$ cm^{-2}s^{-1}. ILC will operate in a pulsed mode: 0.95 ms long bunch trains of electrons and positrons will collide every 200 ms. At a value of 2820 bunches per train, BXs will occur every 337 ns. The bunch structure of the beam is plotted in Fig. 1.2. At the IP the bunches will have horizontal and vertical sizes of 640 nm and 5.7 nm, respectively.

ILC is currently the most advanced linear collider project, both in terms of advanced and tested acceleration technology as well as from an organizational point of view. In parallel to the machine design, an international study group has prepared the DBD (Detailed Baseline Design), explaining the physics capability of the machine and describing the detector concepts [7]. Although the host country has not been decided yet, the Japanese physics community has presented an initiative to host the ILC collider in Japan. If a positive decision is made within a few years, ILC could be ready for data taking before 2030.

1.2.2 The Compact Linear Collider

CLIC is a much more challenging project that proposes to collide electrons and positrons at a nominal center-of-mass energy of 500 GeV, which is intended to be later upgraded to 3 TeV. In order to reach this energy in a realistic and cost efficient way, an accelerating gradient of 100 MeV/m has to be applied. However, such a high value is outside the reach of any available SCRF technology. As a solution, the CLIC project proposes a novel two-beam acceleration technique in which 12 GHz RF (Radio-Frequency) pulses are extracted from a high current low

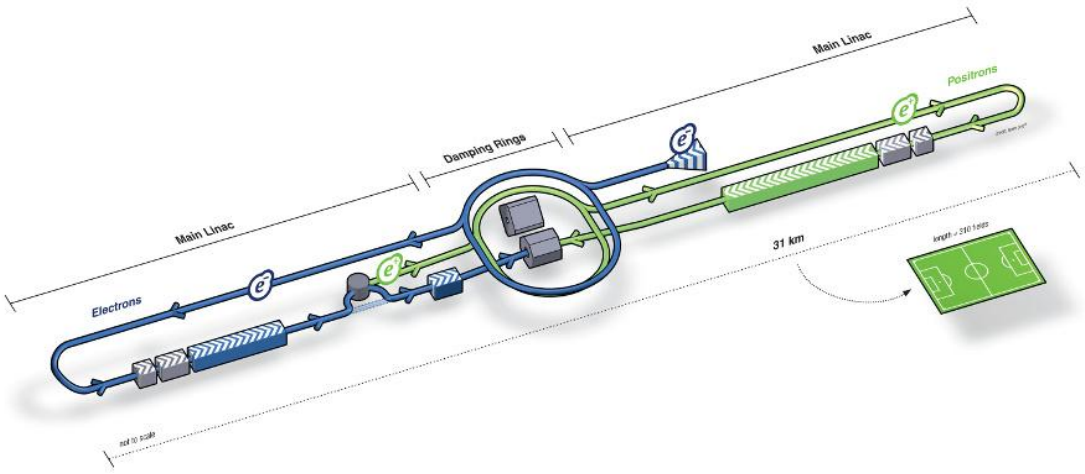

Figure 1.1 Overall layout of the ILC collider [7].

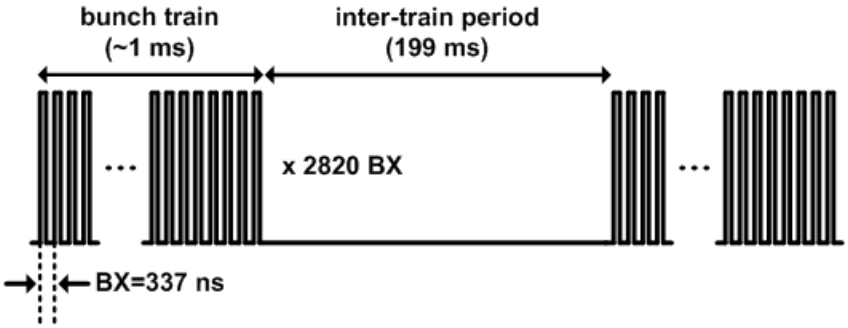

Figure 1.2 ILC beam structure.

energy electron beam (named drive beam) running parallel to the main linac [9]. The drive beam is decelerated in special PETS (Power Extraction and Transfer Structures), producing an RF power that is transferred to the main beam. It is planned that a single drive beam will provide about 70 GeV to the main beam, which means that 22 drive beams will be needed to achieve a beam energy of 3 TeV. This concept leads to a quite simple tunnel, which covers a total length of up to 48 km. Two IPs are foreseen, one for e+e− collisions and another one for γ-γ collisions. A schematic layout of the CLIC accelerator is shown in Fig. 1.3. The luminosity peak of CLIC is around $2 \cdot 10^{34}$ $cm^{-2}s^{-1}$ during the first stage and increased to almost $6 \cdot 10^{34}$ $cm^{-2}s^{-1}$ after the upgrade. The CLIC machine will also operate in a pulsed mode: 156 ns long bunch trains of electrons and positrons will collide every 20 ms. With 312 bunches per train, BXs will occur every 0.5 ns. The beam has the bunch structure plotted in Fig. 1.4. This bunch structure, together with the higher center-of-mass energy, puts additional demands on future detectors. After the upgrade, at the IP the bunches will have horizontal and vertical sizes of 40 nm and 1 nm, respectively.

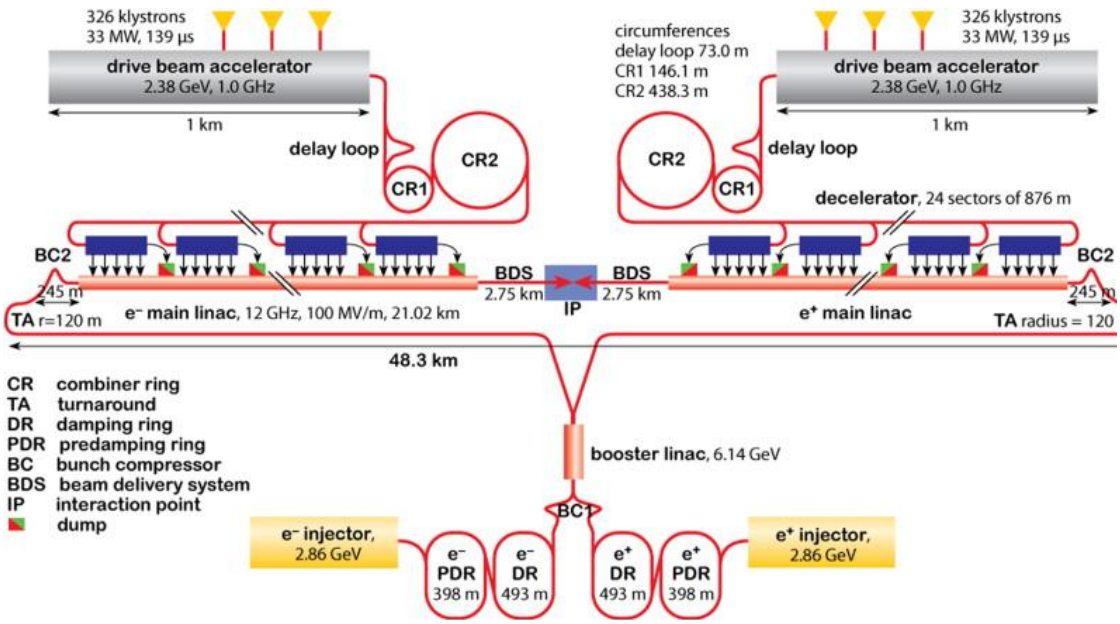

Figure 1.3 Overall layout of the CLIC collider at a center-of-mass energy of 3 TeV [10].

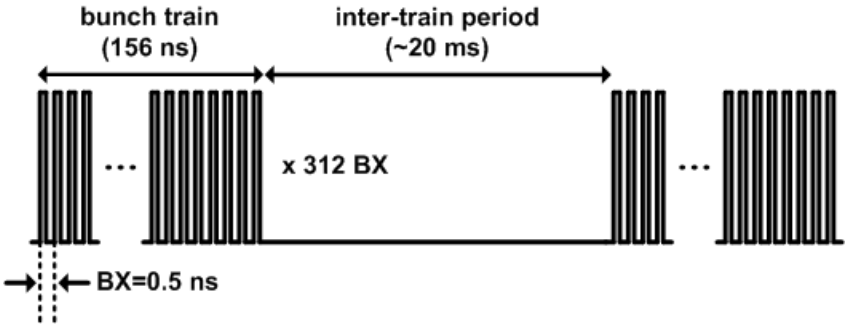

Figure 1.4 CLIC beam structure.

A CDR (Conceptual Design Report) describing the detector and physics issues of the CLIC accelerator was published in 2012 [10]. A decision for the final location has not been made yet, however site studies have shown that CLIC could be constructed underground in the CERN area. The construction of first stage could be accomplished in the years 2023-30, with commissioning starting in 2030.

1.3 Detector systems in future linear colliders

Physics aims at the ILC and CLIC projects put highly challenging requirements on detector systems, which are intended to the reconstruction of the generated events. Particularly complex areas are the impact parameter resolution, track momentum measurement, jet flavor identification and jet energy reconstruction. These issues have been addressed for ILC in two

detector proposals based on a common structure but complementary technologies, the validated ILD (International Linear Detector) [11] and SiD (Silicon Detector) [12]. Fig. 1.5 shows the two detector prototypes. A detailed view of the SiD detector system can be seen in Fig. 1.6. Although the CLIC accelerator is based on a more ambitious concept, it also requires suitable detectors for the particular environment of a TeV scale e+e− collider. Therefore, CLIC has adopted the ILD and SiD detector proposals as well. Nevertheless, these have been modified to meet the more demanding specifications of CLIC.

Both ILD and SiD detectors are composed of several sub-systems, which proceed as follows. The innermost detector is the vertex detector, which consists of a multilayer barrel section of silicon pixels surrounding the beam pipe. The vertex detector is aimed to measure the displaced vertices (i.e. the charged particles coming out from a secondary vertex) of the heavy flavor particles and help in the track reconstruction. It is complemented by forward and backward silicon pixel disks to ensure tracking down to small angles. Then, the tracker detector, based on a gaseous TPC (Time Projection Chamber) surrounded by silicon strip and pixel layers for ILD and an all-silicon system for SiD, reconstructs the tracks of the charged particles and measures their momentum. The electromagnetic and hadronic calorimeters, located outside the tracker detector, are dedicated to energy measurements through the PFA (Particle Flow Algorithm) approach [13]. This precise but complicated technique involves the identification of energy deposits in the calorimeter and the association of these deposits with the charged particle tracks measured in the tracker detector. Both ILD and SiD proposals are also equipped with muon systems to identify isolated muons from the interaction point. Table 1.2 summarizes the technologies of the several sub-systems of ILD and SiD proposals.

1.3.1 Tracking system requirements

To record the particle events in presently operating HEP facilities such as the LHC, hybrid pixel detectors are used. The readout circuits are fabricated in commercial CMOS technologies and connected to the sensors via bump bonding techniques. Since most of the present readout chips are built in 0.25 μm CMOS technologies, this architecture sets a lower limit on the pixel cell size, which together with bump bonding constraints prevents a reduction of the pixel pitch below 50 μm. Nevertheless, the goals of the ILC and CLIC physics programs impose such stringent requirements on the tracking detector system that exceed those met by any previous system. These requirements on the tracking system can be categorized as follows:

- A single point resolution (σ_{point}) better than 5 μm

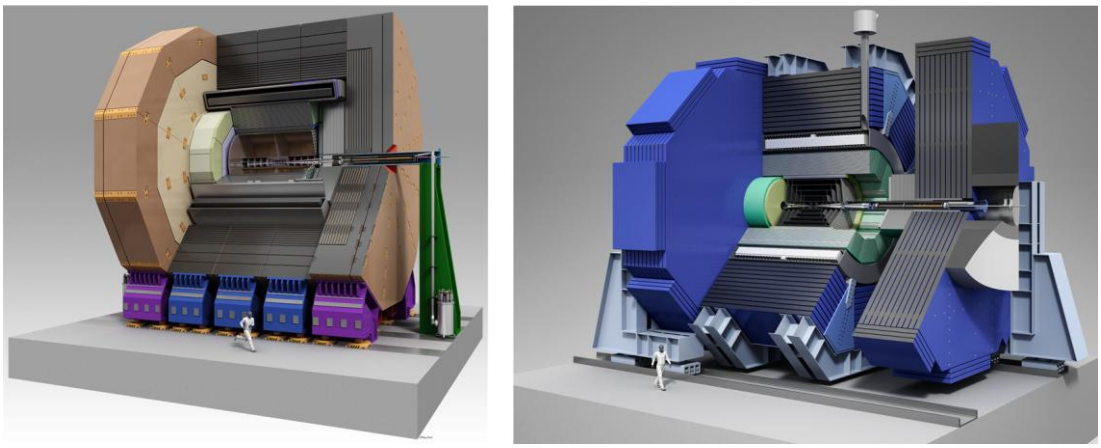

Figure 1.5 ILD (left) [11] and SiD (right) [12] detector prototypes for ILC.

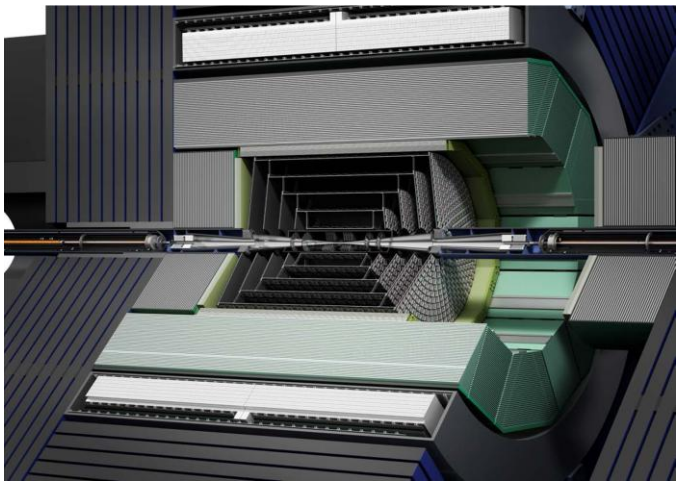

Figure 1.6 Detailed view of the SiD detector system, where it is possible to distinguish the several barrels and disks.

• A material budget below 0.15% (ILD) or 0.30% (SiD) X_0 per layer, where X_0 is the radiation length, to minimize the Coulomb multiple scattering

• A high granularity for good particle separation

• Single bunch crossing resolution

• An occupancy below 1%, including the background hits

• Radiation tolerance

• Average power less than a few mW/cm^2

• EMI (ElectroMagnetic Interference) immunity

• An affordable cost

ILD proposal		SiD proposal	
Sub-system	**Technology**	**Sub-system**	**Technology**
Vertex detector	Silicon pixels	**Vertex detector**	Silicon pixels
	- 3 barrel double layers		- 5 barrel layers - 4 forward disks - 4 backward disks - 3 disks
SIT	Silicon strips	**Tracker detector**	Silicon strips
	- 2 layers		
SET	Silicon strips		- 5 barrel layers - 4 disks
	- 2 layers		
TPC	MPGD readout		
ECAL	W absorber	**ECAL**	Silicon pixels-W
HCAL	Fe absorber	**HCAL**	RPC-steel
Coil	35 T field	**Solenoid**	5 Tesla SC
Muon	Scintillator layers	**Flux return (muon system)**	Scintillator-steel

Table 1.2 Technologies of the different subdetector systems (barrel) of the ILD and SiD proposals. SIT stands for Silicon Internal Tracker, SET for Silicon External Tracker, TPC for Time Projection Chamber, ECAL for Electromagnetic CALorimeter, HCAL for Hadron CALorimeter, MPGD for Micro-Pattern Gas amplification Detectors, RPC for Resistive Plate Chamber and SC for SemiConductor.

These specifications drive the design of the future tracking systems. In particular, the need for an accurate particle track reconstruction implies excellent single point resolution and minimum multiple scattering. Thus, the requirement on a 5 μm single point resolution, set by the multilayer barrel geometry, implies a pixel size of 17 μm as it is inferred from

$$\sigma_{point} \leq pixel\ size / \sqrt{12} \cdot \tag{1.1}$$

To reduce the multiple scattering on the quantity of material crossed by the particles, and hence reduce the uncertainty in the reconstruction of the traces, the overall material budget of the system has to be minimized. Therefore, considering a maximum 0.15-0.30% X_0 per layer in the central region of the tracker, the thickness of the silicon detectors has to be 150 μm or 300 μm at the most. Moreover, because the detector has to be built with the lowest material budget possible to reduce the multiple scattering, no active cooling is allowed inside the acceptance region. Thus, the cooling system relies on forced cold air.

A high granularity is required for good particle separation, i.e. to deal with high particle fluxes and reduce the influence of overlapping events.

Another issue to be handled by the future tracking systems is the timing resolution, which is dictated by the bunch train time structure and the required pixel occupancy. If the detector is not fast enough to read each single bunch crossing, then the signals may be integrated and read out multiple times in one train (technique known as time slicing) to keep the occupancy below 1%. Alternatively, time-stamping can be performed to divide the bunch train into several time-buckets, each of which corresponds to one bunch crossing. The occupancy is mainly generated by beam-induced background events, which are dominated by beamstrahlung photons, and varies with the radius of the layer. According to the studies on ILC performed by the ILD group, the typical background events will range from 0.019 hits/cm^2/BX in the first layer to 0.001 hits/cm^2/BX in the last layer of the tracker detector at a nominal energy of 1 TeV [11]. Thus, at the ILC accelerator, with 2820 bunches/train, 337 ns bunch-spacing and 5 Hz repetition rate, an occupancy low enough not to affect the pattern recognition should be achievable by reading the detector 20 times per bunch train (each 50 μs) for a sensor size of 25 μm x 25 μm. However, the requirement on the occupancy is more challenging at CLIC given the increased background events due to the higher energy of the accelerator and the shorter bunch-spacing. A background level of 0.87 hits/cm^2/BX is foreseen in the tracker detector of CLIC [14]. The CLIC bunch-spacing of 0.5 ns and the train length of 156 ns are too short to achieve a reduction of the backgrounds by fast readout. Instead, time-stamping capabilities need to be available for the tracker detectors. The time-stamping technique could reduce the pile-up from two photon background events to ≤20 bunch crossings.

The required radiation tolerance follows entirely from the beam-induced backgrounds, which is expected to affect predominantly the innermost layer. This way, a maximum TID (Total Ionizing Dose) of up to 1 kGy/year and a neutron fluence or NIEL (Non-Ionizing Energy Loss) of approximately 10^{11} n_{eq}/cm^2/year is expected near the ILC beam pipe. In contrast, the TID and NIEL for CLIC are 200 Gy/year and 10^{10} n_{eq}/cm^2/year, respectively. These data include some safety margin.

The power consumption should be low enough to minimize the material budget of the cooling system inside the detector sensitive volume. An affordable cost should be considered, since large-area detectors are foreseen.

1.3.2 Tracking technology options

The requirements on the tracker detector system of the future linear e+e− collider outlined in the previous section are at least challenging. At present time, there is no mature technology available in the market that can fulfill all of them and new detector systems are being developed

in parallel with the accelerator. The detectors that concentrate most of the R&D (Research and Development) carried out worldwide are based on CMOS pixel technologies, either monolithic, hybrid or 3D. Leading sensor techniques are DEPFETs (DEPleted Field Effect Transistors) [15], MAPS (Monolithic Active Pixel Sensors) [16] and FPCCDs (Fine Pixel Charge Coupled Devices) [17]. Alternative approaches are based on Chronopixels [18], Timepix [19] and GAPDs [20]. Yet another approach is to exploit the new emerging technologies for tracking sensors, which include the SOI (Silicon-On-Insulator) [21] and 3D [22] technologies. The main features of the proposed tracker detectors are summarized in Table 1.3.

1.3.2.1 DEPFETs

The DEPFET concept integrates a pMOS field effect transistor in each pixel of a fully depleted n-substrate to be used as a sensing and amplifying element (Fig. 1.7 for schematic view of the structure). The transistors also incorporate an internal gate, which is accomplished by an additional deep n-doped implantation situated underneath the transistor channel at approximately 1 μm depth. The internal gate creates a local potential minimum for majority carriers (electrons in the case of an n-substrate). If a ionizing particle enters the sensor, electron-hole pairs are created in the depleted substrate. The holes drift to the backside contact of the substrate, but the electrons are collected and stored by the internal gate. The charge collected leads to a change in the potential of the internal gate, which results in a modulation of the drain current at a rate of 400 pA per electron. This constitutes the in-situ amplification of the detector. After readout, the charge collected is removed from the internal gate by applying a positive voltage at a clear contact. The extremely low capacitance (10-20 fF) of the internal gate ensures low noise operation. In addition, a 100% fill-factor (i.e. the ratio between the sensitive area and

Detector	DEPFET	MAPS	FPCCD	Chrono.	Timepix	GAPD	SOI
σ_{point} (μm)	~1	~3	–	~3	2.3	~5	~1
Mat. budg. (μm)	50	50	50	50 - 100	300	250	70
Gran. (μm x μm)	20 x 20	18.4 x 18.4	5 x 5	10 x 10	55 x 55	20 x 100	13.75 x 13.75
Timing	integration	integration	integration	stamping	stamping	single-bunch	integration
Radiation tolerance	10 kGy	10 kGy 10^{13} n_{eq}/cm^2	10^{12} e^-/cm^2	–	4 Mgy	–	1 kGy
Power	5 W	250 mW/cm^2	16 mW/ch	–	886 mW/cm^2	–	–
Fill-factor (%)	100	100	100	100	87	67	100

Table 1.3 Main features of the proposed tracker detectors for the future linear colliders.

the total area occupied by the detector) can be achieved with this detector.

The DEPFET concept was proposed in 1987 by Kemmer and Lutz. Since 2002, intense R&D of this technology has been carried out by an international collaboration named the DEPFET collaboration. As a result, the DEPFET detector has now reached some level of maturity, including their performance in beam-tests at CERN [23] and DESY [24]. The first production of DEPFET sensors took place in 2004 and several generations with different configurations have already been fabricated at the Semiconductor Laboratory of the Max Planck Society. Matrices with up to 64 x 256 pixels and small sensors of 20 μm x 20 μm have been successfully produced in 50 μm thickness wafers. However, the development of larger matrices with the required sensor area is still ongoing. DEPFET prototypes for the future tracker detectors are based on a ladder structure (Fig. 1.7), with the sensitive area placed in the central region and steering and readout ASICs bump bonded at the balconies. The chips, fabricated in three different standard CMOS technologies, are used to operate and read out the DEPFET matrix in a rolling shutter mode with zero suppression and correlated double sampling. Nevertheless, the current readout speed of 80 ns/row has to be improved to achieve a frame readout time of 50 μs and satisfy the ILC requirements. The main results from the DEPFET beam-tests are a SNR (Signal-to-Noise Ratio) better than 110, a detection efficiency of 99.96% and an intrinsic spatial resolution around 1 μm [23]. The power consumption of the active area of the DEPFET sensors is very low since the pixels passively collect the charge and only need power during the readout cycle. A total power consumption of 5 W is foreseen for the whole DEPFET tracker detector. The results from several irradiation campaigns show a remarkable radiation tolerance to 10 kGy. At current time, it is established that the DEPFET technology will

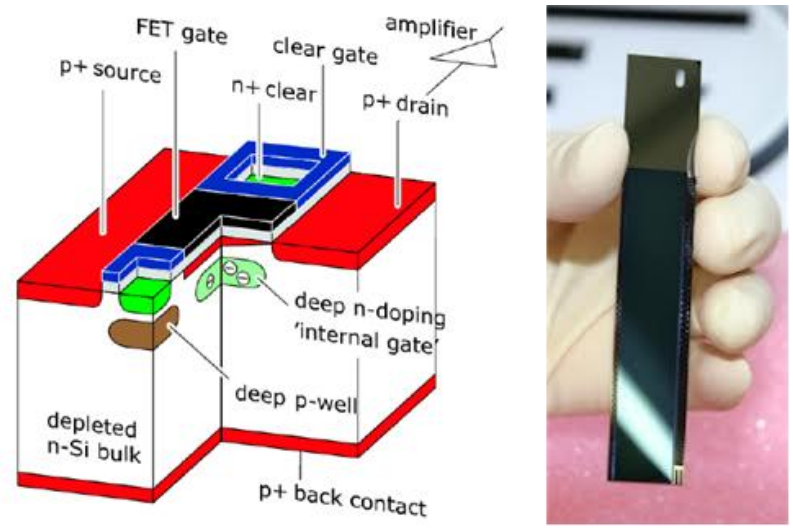

Figure 1.7 Schematic view of a DEPFET pixel structure (left) and mechanical sample of the ladder structure (right).

be used as an inner detector in the Belle II experiment at the Japanese SuperKEKB factory, starting at 2015.

1.3.2.2 MAPS

MAPS sensors are based on an n-well/p-epi diode implemented in a standard CMOS technology (Fig. 1.8). These devices use the lightly doped p-epitaxial layer on a low resistive p-substrate as the active detector volume. The charge generated by the impinging particles in the epitaxial layer reaches the n-well diode contacts by diffusion, which results in long collection times around 100 ns and considerable charge spread over several pixels. The epitaxial layer is thin, and this yields only small signals. Thus, for instance, about 1000 electron-hole pairs produced by a MIP (Minimum Ionizing Particle) are collected with an epitaxial layer of some 10-20 μm thickness. On the other hand, the intrinsic capacitance of these devices is very low and excellent SNRs have been reported [25]. A three-transistor readout circuit does the amplification and row/column selection of the respective pixel. MAPS detectors are usually read out in rolling shutter mode at a typical speed of 200 ns/row. Because the readout circuit is placed on top of the active volume, a 100% fill-factor is possible.

MAPS were re-invented in the early 1990's on both sides of the Atlantic with the establishment of the CMOS process. These sensors have become so far one of the leading technologies in the imaging field. Aimed to particle physics experiments, several MAPS prototypes named MIMOSA (Minimum Ionizing particle MOS Active pixel) have been fabricated since the 2000's. In particular, the MIMOSA-26 [26] sensor equips the final version of the EUDET beam telescope [27], which at present time is an essential part of the beam-test set-ups of novel tracking detector technologies. This chip was fabricated in the AMS (Austrian Micro Systems) 0.35 μm OPTO technology in 2009. The pixel matrix is composed of about 0.7 million pixels distributed in 1152 columns and 576 rows. It has a total sensitive surface of 2.2 cm^2 (pixel size of 18.4 μm x 18.4 μm). Rows are read one by one in a rolling shutter mode while amplification and correlated double sampling are implemented inside each pixel. The chip also incorporates pixel output discrimination for binary readout and zero suppression circuits at the matrix periphery to stream only the fired pixels out. The address and length of consecutive fired pixels is stored in embedded memories. The memories are serially read out with two 80 Mbits/s outputs, which allow to read out the whole pixel matrix in 112 μs. This prototype has shown a 99.5% detection efficiency for an average fake rate below 10^{-4} fake hits per pixel, combined with a spatial resolution close to 3 μm, radiation tolerance of up to 10 kGy of ionizing dose and 10^{13} n_{eq}/cm^2 fluence, and power consumption of 250 mW/cm^2. The MIMOSA-26 is also the sensor of choice for the upgrade of the inner detector in the STAR (Solenoidal Tracker

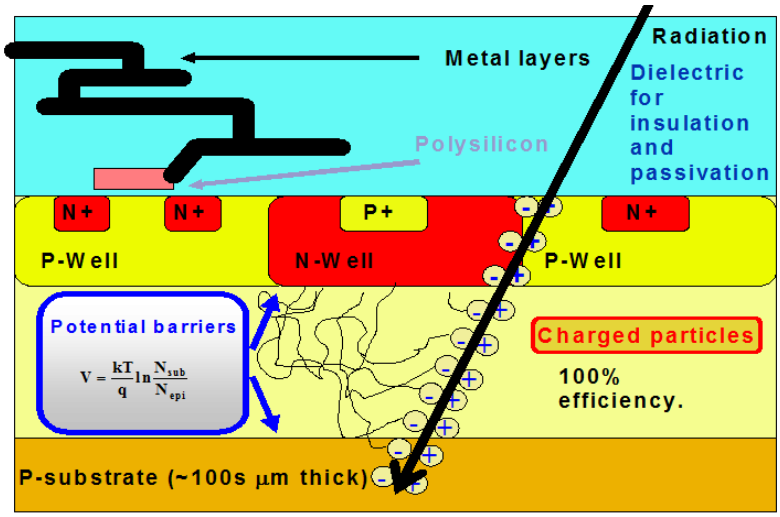

Figure 1.8 Schematic cross-section of a MAPS sensor.

At RHIC) experiment at the RHIC (Relativistic Heavy Ion Collider) accelerator [28], which is the first application of a MAPS detector at a collider.

1.3.2.3 FPCCDs

The fundamental sensing element of CCD pixels is a MOS (Metal Oxide Semiconductor) capacitor, which is implemented by means of a polysilicon gate, a thin film of silicon dioxide (SiO_2) and a weakly doped p-epitaxial layer (~15 μm thickness) laid on top of a highly doped p-substrate. Moreover, an n-type implantation is added to the epitaxial layer in the form of a buried channel at approximately 1 μm beneath the Si/SiO_2 interface to create a potential minimum for minority carriers (electrons in the case of a p-substrate). During the so-called integration time, a positive bias voltage is applied to the gate electrode to create a depletion region in the upper volume of the epitaxial layer. The electrons generated due to the passage of a ionizing particle are transported by drift to the potential minimum. The charge collected is confined within the potential well by means of a superior surrounding potential, which is generated by neighboring gates (termed barriers) biased at a negative voltage. Although there exist several strategies to transfer the charge packets to the readout node, the three-phase CCD clocking approach is the most common. In this configuration, every third electrode of a matrix of CCD pixels is connected to the same voltage. By pulsing the gates in an appropriate sequence through a shift register, the charge packets are transferred in parallel down the detector one row at a time. The lowest line is connected to a serial readout register, which runs orthogonally to the columns of the sensing matrix. The serial register feeds an output amplifier connected to an ADC (Analog to Digital Converter).

CCDs were invented in 1969 by Boyle and Smith at the Bell Telephone Laboratory to be used as computer memories [29], although their huge imaging capabilities were immediately recognized. Today, these devices are regarded as one sensor of choice for both commercial and research applications. Concerning particle physics experiments, CCD detectors also have a large experience. They demonstrated, for instance, a successful performance at the SLAC facilities with the SLD (SLAC Large Detector) experiment [30, 31]. However, this technology cannot fulfill the requirements of the future generation of e+e− colliders, mainly due to its low speed operation and radiation intolerance. To address this issue, several CCD-based approaches are being developed at present time, such as the CPCCD (Column Parallel CCD) [32] and ISIS (In-Situ Storage) [33] by the LCFI (Linear Collider Flavor Identification) collaboration or the FPCCD (Fine Pixel CCD) [17] by the ILC-FPCCD vertex group. In particular, the FPCCD concept makes use of finely segmented sensors of 5 μm x 5 μm to achieve a low hit occupancy below 1% even integrating the detector over a full bunch train. Moreover, the extreme granularity also results in a sub-micron single point resolution and excellent two track separation capability. However, because of the small sensor size, there is a large number of pixels in one channel (20000 x 128). Therefore, the readout speed must be above 10 Mpix/s to read all the pixels in the inter-train time (199 ms). Another inconvenience of using such a small sensor size is the reduced number of electrons (~500) that will be produced if a ionizing particle penetrates the detector horizontally. A total noise level below 50 electrons is desirable. Consequently, this technology requires a low-noise multi-channel readout ASIC, which employs an amplifier, a low pass filter, correlated double sampling circuitry and two ADC converters [34]. The power consumption of the detector should be below 16 mW/ch. In addition, cooling at ~ –40 ºC will be needed to reduce the thermal noise due to the relatively long readout time and suppress the effects of radiation damage. The fabrication of the first sensor and ASIC prototypes took place in 2007 and their development is still ongoing.

1.3.2.4 Chronopixels

The chronopixel technology is based on the same sensing mechanism as MAPS. However, this concept includes additional in-pixel electronics to record the time (i.e. to put a time-stamp) of each hit with enough precision to assign it to one particular bunch crossing of an entire bunch train. Thus, the occupancy is reduced to negligible levels, even reading the chip out during the 199 ms quiet gap between bunch trains.

The development of this detector is being carried out by the Oregon University and Yale University in collaboration with the SARNOFF Corporation since 2004. So far, the chronopixel architecture has been defined and two prototypes have been designed and fabricated [35]. To

store the time of each hit, the in-pixel electronics comprise a voltage comparator, a local counter, a digital memory and a reset transistor. The detector proceeds as follows. After each bunch crossing, the signal of each pixel is compared to a preset calibrated threshold level set at 200 electrons/pixel. If the signal is above the threshold (i.e. a ionizing particle has crossed the sensitive layer), the memory is enabled to latch in its first 14-bit slot the time-stamp data supplied by a global counter. Then, the sensor is reset, the memory pointer is advanced by the local counter and the pixel is ready for the following bunch crossing. Up to a total of four hits per bunch train can be time-stamped in the memory, since the Poisson probability of more than 4 impacts per pixel and train is less than $>10^{-4}$. The stored non-zero time-stamp data of hit pixels is read out in random access mode during the 199 ms gap between bunch trains. To squeeze the 645 transistors that are necessary to operate the chronopixel in a 10 μm x 10 μm pixel (needed to achieve a precision of 3-4 μm), a still extremely expensive 45 nm process technology is required. Instead, the first prototype with 50 μm x 50 μm pixels was fabricated in the TSMC 180 nm technology in 2008 (Fig. 1.9). Alternatively, the second prototype was built on the TSMC 90 nm technology in 2012, which allowed to reduce the pixel size to 25 μm x 25 μm. Although these choices lead to poor efficiency, they have permitted to show that the general concept of the device is working and also to prove the main assumptions on noise level, power consumption and digital circuitry flexibility. Plans for a third prototype are already set. In the final design, the detector will consist of 12500 rows per 2000 columns of pixels, divided into 40 readout regions of 50 columns each. At the end of the bunch train, the 40 regions will be read out in parallel and temporarily stored in a FIFO before leaving the chip, requiring about 8 ms to read out the entire detector. According to estimations, the analog parts of the circuit (i.e. the sensor and the comparator) will consume around 15 mW/mm^2, which represents most of the power. Nevertheless, the average power consumption can be reduced to 0.4 W per chip, or

Figure 1.9 Image of the 645 transistor pixel design [18].

about 100 W for the whole detector, by switching off the analog power between bunch trains.

1.3.2.5 Timepix

The Timepix is a pixel readout chip intended for a TPC, the gaseous main particle tracker of the ILD detector concept. The design of the Timepix chip is derived from the Medipix2 [36], a chip from the Medipix family that was devised for single photon counting in imaging and medical applications in the early 2000's. The idea was to keep the Timepix as similar as possible to the Medipix2 in order to benefit from large prior effort and reduce the risk of chip failure. The development of the Timepix chip took place at CERN by the Medipix2 collaboration with support of the EUDET project.

In very broad terms, the performance of a TPC tracker detector is described next. Similarly to silicon tracker detectors, a charged particle passing through the sensitive gas volume contained in a TPC produces a primary ionization path along its track. Then, the electrons from the ionization drift towards a readout anode plate, where they are collected. Mounted on top of the anode plate typically stands a gain grid system, which is used for charge amplification prior to processing. The Timepix readout chip has been proposed as a novel solution for a pixilated charge collecting anode. It has shown very promising results when coupled to GEM [37] (Gas Electron Multiplier) or Micromegas [38] (MICRO Mesh GASeous detector) gain grids. The Timepix chip consists of an array of 256 rows x 256 columns of 55 μm x 55 μm pixels, with an 87% detection area. Each pixel is equipped with a preamplifier, a discriminator with a globally adjustable threshold, mode control logic and a 14-bit counter. The Timepix chip can be configured in one of four different operation modes: masked, counting, TOT (Time Over Threshold) and TOA (Time Of Arrival). In the masked mode, the pixels are off. In all the others, the pixels are activated by a binary signal called the shutter signal. During the shutter time, the pixel counter is triggered when the signal from the preamplifier crosses the threshold level of the discriminator. The counting mode, also named the medipix mode, is used to count the number of hits. In contrast, in the TOT and TOA modes the counter is used to count the number of clock cycles provided by a reference clock with a frequency of up to 100 MHz. In the TOT mode, the value of the counter is equal to the number of clock cycles elapsed during the time that the signal pulse was above the threshold. The value of the counter is an indication of the total energy deposited. Finally, in the TOA or Timepix mode, the counter records the number of clock cycles counted during the time between the first hit and the end of the shutter time. The TOA mode is used to associate hits to the correct bunch crossing via time-stamping.

The first prototype was fabricated in the IBM 0.25 μm technology in 2006. The entire chip is read out after the shutter signal goes down by means of either on-chip LVDS drivers in ~5 ms or a 32-bit parallel bus in ~300 μs. The power consumption of the analogue and digital parts is respectively 440 mW and 450 mW. A detection efficiency greater than 99.5%, pointing resolution around 2 μm and time resolution in the nanosecond scale have been demonstrated in several beam-test campaigns using 300 μm thick devices. The radiation tolerance has been tested to be 4 Mgy. Moreover, the Timepix chip together with the Medipix2 chip equip a prototype telescope aimed to particle tracking [39]. An improved version of the Timepix chip, the Timepix3 [40], is being developed by the Medipix3 collaboration. It will be fabricated in the IBM 130 nm technology in 2013. This chip will allow simultaneous measurements in the TOT and TOA modes, zero suppression, data driven readout (each hit is time-stamped, labeled and send off-chip immediately) and power pulsing to reduce the consumption to 886 mW/cm^2. The Timepix technology is also being considered for the LHCb VELOpix upgrade [41].

1.3.2.6 GAPDs

In conventional CMOS technologies, GAPD detectors are typically implemented by means of a p^+/n-well junction on a p-substrate, even though n^+/p-well junctions inside a deep n-well for isolation from the substrate are also possible. These photodiodes are reverse biased above the breakdown voltage of the junction to operate the Geiger-mode, condition at which impinging radiation being absorbed by the multiplication region can trigger an avalanche process of generation of electron-hole pairs. As a result, a macroscopic current pulse (gain 10^5-10^6) that can be detected by the readout electronics is generated in a few hundred picoseconds. A simple CMOS inverter is generally used as an avalanche discriminator and digitizer. Preamplifiers or pulse pulse shapers are therefore unnecessary. However, avalanche events are due not only to the absorbed radiation, but also to the noise phenomena generated by the sensor. Since the noise avalanches cannot be distinguished from real events, low SNRs and high occupancies may be anticipated unless power pulsing and/or cooling are applied. On the other hand, GAPD detectors can be read out in a number of different ways, such as random access, sequential by rows or columns, event-driven and pipelined. For a fixed array size, the whole GAPD detector can be read after each bunch crossing if a proper readout strategy is implemented in a fast enough technology process. Given that only the junction area is sensitive to impinging radiation, a 100% fill-factor is not possible with this sensor technology.

Although the first studies on the avalanche multiplication phenomenon in p-n junctions started in the 1960's at the Shockley laboratory [42, 43], it was not until the 1990's that solid-state avalanche detectors became available in a CMOS compatible process [44]. However, only

the monolithic integration of a GAPD sensor and the front-end electronics on a single CMOS die in 2003 [45] opened the way to commercial applications. Since then, intense R&D of this technology has been conducted by several research groups. Good proof of this is the great number of prototype GAPD cameras that have been produced in different standard CMOS technologies in the last ten years, aimed mostly to single-photon detection. In spite of this, the behavior of GAPDs in the detection of high energy particles was not explored until recently. Beam-tests started in 2012 at the SPS (Super Proton Synchrotron) area of CERN and are still ongoing [46]. The radiation tolerance of a GAPD detector fabricated in a HV-AMS 0.35 μm CMOS technology has been tested to be around 1 kGy for gamma rays and around 100 Gy for protons [47]. More details about the characteristics of this sensor technology as well as a complete description and characterization of the first GAPD detector aimed at HEP experiments will be given in the next chapters.

1.3.2.7 SOI

In the SOI technology, a thin buried oxide (BOX) is used to electrically insulate the CMOS readout electronics from the high resistivity charge-collecting substrate (Fig. 1.10). The CMOS electronics is implanted on a 40 nm thin silicon layer, which is fully depleted at typical operational voltages, on top of a 200 nm thick BOX layer. Vias are etched through the buried oxide to contact the transistor layer to the detector substrate, so that topside reverse bias of the n-substrate can be applied and p^+ pixel implantations that collect the charge signal can be contacted. The isolation between the transistor layer and the detector substrate ensures high latch-up immunity as well as a reduced junction capacitance. The substrate can be back-thinned to 70 μm, which together with the low junction capacitance improves the speed and power consumption. However, the reverse bias applied to the detector substrate induces a potential below the CMOS electronics layer, which typically shifts the threshold voltage of the CMOS transistors. This phenomenon, known as back-gating effect, was observed in the first prototypes and limited the charge collection. It has already been addressed by implanting a BPW (Buried P-Well) region beneath the BOX, which screens the potential applied to the substrate.

The SOI pixel detector is developed by the SOIPIX collaboration, the members of which are distributed amongst Asia, America and Europe. A number of prototypes have been designed by different research groups and fabricated by Lapis Semiconductor Co. Ltd. (formerly OKI Semiconductor) in MPW (Multi-Project Wafer) runs since 2006. The first set of prototypes was manufactured in a standard 0.15 μm CMOS technology on fully depleted SOI wafers. However, the shutdown of this process line in 2007 forced migration to a 0.20 μm process. Some examples of the prototypes under development are the INTPIX (INtegration-Type PIXel

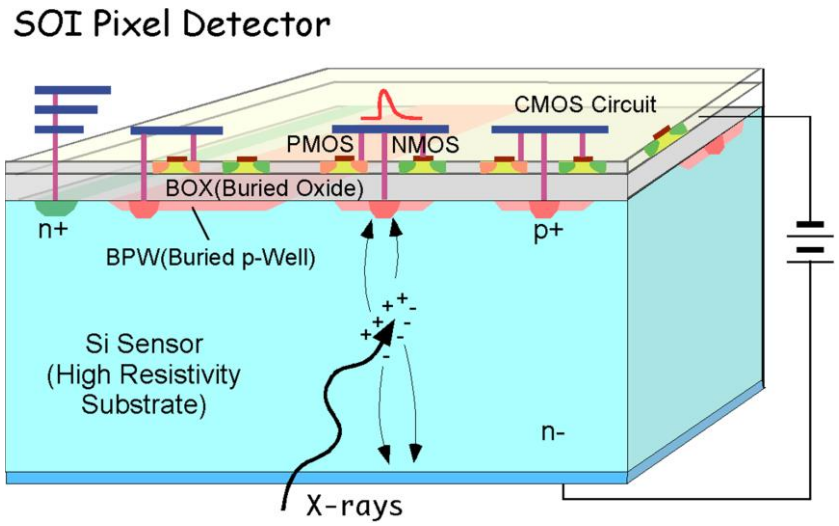

Figure 1.10 Cross-section of the SOI monolithic pixel device [48].

detector) and CNTPIX (CouNting-Type PIXel detector) series [48] by KEK (High Energy Accelerator Research Organization), the LDRD-SOI (Laboratory Directed Research and Development-SOI) [49] and SOImager [50] series mainly by LBNL (Lawrence Berkeley National Laboratory) and INFN (Instituto Nazionale di Fisica Nucleare) and the MAMBO (Monolithic Active pixel Matrix with Binary cOunters) series [51] by FNAL (Fermi National Accelerator Laboratory). In particular, the SOImager-2 chip, fabricated in 2010, contains a matrix of 256 x 256 pixels arrayed on a 13.75 µm pitch. The in-pixel analog readout electronics employs a reset transistor, a source follower and a transmission gate for row selection. The pixels are read out through four parallel arrays of 64 columns each in a rolling shutter mode with 1-1.5 kframes/s (656 µs integration time). This chip has been successfully tested in a beam-test at CERN with 300 GeV pions, showing a detection efficiency of 99% and an intrinsic single point resolution around 1 µm. The SOI technology is immune to SEEs (Single Event Effects) given the reduced thickness of the transistor layer, but not to TID (Total Ionizing Dose) due to the presence of the BOX layer. The tolerance of the SOI technology to total dose effects has been measured to be 1 kGy.

1.3.2.8 3D

In microelectronics, the 3D-IC (3D-Integrated Circuit, i.e. a vertically integrated circuit) technology concept refers to the stacking of multiple thin logic dies (named tiers) equipped with deep metal vias (named TSVs as Through-Silicon-Vias) to form a monolithic device. The potential of this technology lies in the fact that it allows to split the sensor, readout electronics and digital blocks into different layers in order to overcome some of the intrinsic limitations of the tracker detector candidates, while still preserving the fabrication with standard CMOS

processes. At the same time, it also allows to achieve higher densities of integration without having to use nanometer technologies, which complicate the design of analog circuits and suffer from high technologic deviations. Thus, for instance, due to the utilization of n-well diodes as a charge collection device, MAPS may take advantage of the 3D-IC alternative to go beyond the prohibition of pMOS transistors inside the sensing area [52], which severely limits the choice of the readout electronics circuitry. Moreover, there exist groups working with the traditional HEP hybrid pixel approach in 3D (ATLAS effort for 3D integration) with the goal of reducing the pixel size while keeping the 130 nm feature size. Nevertheless, the 3D-IC option can also be used as a solution to increase the fill-factor of GAPD detectors [53], which rarely exceeds the 10% when fabricated in conventional 2D technologies. Although the 3D-IC technologies are being pursued in many different forms, they can be classified into two main categories depending on the nature of the interconnection process between tiers. Essentially, 3D-ICs can be manufactured by independently fabricating the 2D logic dies corresponding to the different tiers in separate wafers, then aligning and interconnecting them through TSVs. However, TSVs may be an integral part of the foundry process, being formed before or right after the FEOL (Front-End-Of-Line) processing, or may be added as the last step after wafer bonding in the areas being free of active circuits. The first approach is called via-first and the second one via-last [54].

The VIP (Vertically Integrated Pixel) chip, the first readout chip fabricated in a 3D-IC approach inside the HEP community, was conceived as a demonstration of 3D-IC technologies aimed at ILC. The first version of this chip (named VIP1) was produced in a 3-tier 180 nm FD-SOI process at MIT-LL (Massachusetts Institute of Technology-Lincoln Laboratory) [55]. The design was submitted for fabrication in October 2006. However the first set of dies was not delivered until November 2007, which reflects the complexity of the 3D endeavor undertaken by a non-commercial VLSI line. The VIP1 prototype features 20 μm x 20 μm pixels, which are laid out in an array of 64 x 64 elements. In-pixel electronics to perform analog and digital operations are distributed between the three tiers, so that the critical analog functions consisting of integration, discrimination and correlated double sampling are on the top tier (closest to the detector), and the digital readout with zero suppression is on the bottom tier (farthest from the detector). The intermediate layer is used for implementing the time-stamping circuitry. In the present technology, TSVs are added in a via-last process. Moreover, stacked TSVs from the bottom tier to the top one are allowed. Bonding from the intermediate tier to the bottom one is done face-to-face, while from the top tier to the intermediate one is done face-to-back. Although a very low yield and some problems related to flaws in the processing of individual tiers were found amongst the fabricated devices, the tests performed on the VIP1 chip showed a correct functional operation of the structure. All the interconnections between the circuit layers worked, which was considered as a major success.

In spite of the MIT-LL efforts to produce 3D-IC devices, a 3D-IC Consortium led by FNAL was formed in 2008 to explore various issues associated with vertical integration [22]. This consortium promotes MPW runs in the Global Foundries (previously Chartered Semiconductor)/Tezzaron 3D process, which typically consists of two logic dies fabricated in the Global Foundries 130 nm technology and vertically integrated by Tezzaron. Global Foundries uses a via-first approach to add 6 μm deep TSVs to a standard 130 nm CMOS technology. The TSVs are then used to interconnect the logic circuitry to the backside I/O pad cells of the top tier. Tezzaron performs the 3D stacking using face-to-face wafer-to-wafer bonding through the top copper metal layer of the technology, thus allowing the connection of relaying signals between tiers. Although the designs for the first MPW run in the Global Foundries/Tezzaron 3D process organized by the 3D-IC Consortium were initially completed in May 2009, they were not accepted for fabrication until March 2010 due to numerous problems related with the utilization of different versions of the design kit provided by Tezzaron, misinterpretation of the design rules or shifting requirements of Global Foundries [56]. Moreover, the transition from Chartered Semiconductor to Global Foundries also slowed the wafer fabrication process. Last but not least, the first lot of wafers was misaligned for 3D bonding and 2D performance could be tested only after delivery in November 2010. The tests of these devices at several laboratories confirm a good correspondence to simulations and show a similar behavior between chips with and without TSVs. The first 3D wafer was delivered in November 2011 and tests are ongoing. However, due to the mentioned technical difficulties, more time and funding will be required for this 3D-IC technology to reach maturity. More details on the Global Foundries/Tezzaron 3D process will be given in Chapter 5.

1.4 Detector systems in other particle colliders

The TOTEM (TOTal Elastic and diffractive cross-section Measurement) experiment is one of the seven experiments that are currently underway at CERN [57]. It is aimed at the study of the forward region to focus on physics complementary to the general purpose experiments. In particular, it is dedicated to the measurement of the total proton-proton cross-section and to the study of the elastic scattering and diffractive processes at the LHC. The diffractive processes are investigated partly in collaboration with CMS, with whom TOTEM shares IP 5.

To that end, the TOTEM experiment must be able to detect particles moving at very small angles with respect to the beam. The experimental apparatus designed for this task is composed of three subdetectors: two tracking telescopes, T1 and T2, with two arms each and a system of four detector stations that are called Roman Pots. The three subdetectors are placed symmetrically on both sides of IP 5 and the CMS experiment. The T1 and T2 telescopes are

placed at ±9 m and ±13.5 m respectively from the IP. They are aimed at the detection and partial reconstruction of inelastic events produced at the polar angles between a few mrad and ~100 mrad [58]. The inelastic rate is necessary for the determination of the total proton-proton cross-section. In contrast, the Roman Pot stations are located at ±147 m and ±220 m from the IP to detect mostly elastically and diffractively scattered protons (the so-called leading protons) produced at very small polar angles down to a few μrads [59]. Moreover, the experiment also comprises special beam optics to optimize proton detection in terms of acceptance and resolution. A schematic drawing of the TOTEM experiment is depicted in Fig. 1.11.

The detectors of the tracking telescopes are of gaseous nature. In particular, each arm of the T1 telescope is composed of five planes of trapezoidal CSCs (Cathode Strip Chambers), with six chambers per plane covering a region of 60º in azimuthal angle. The CSC chambers provide the three coordinates of each particle track within a plane with a spatial resolution of ~1 mm. The T2 telescope is made of GEM (Gas Electron Multiplier) chambers. Each arm is made of two sets of ten aligned detector planes with almost semicircular shape. The GEM chambers provide two-dimensional information of the track position covering an azimuthal angle of 192º.

The Roman Pots are special beam pipe insertions which allow setting the detectors very close to the beam without interfering with the primary vacuum of the machine. Each Roman Pot station is made of two units separated by a distance of about 5 m to achieve higher trigger efficiency. In turn, each unit is equipped with three Roman Pot detectors (making a total of 24 individual pots installed at the LHC), two of them approaching the outgoing beam vertically and the other one horizontally. The elastic protons will pass mainly through the vertical pots, while the diffractive protons, with a small fraction of momentum lost, will be in the region covered by the horizontal pot. Although the Roman Pots have already been successfully used at other colliders since 1971, the challenging constraints of the LHC, such as the thin high-intensity beam, the ultra-high vacuum or the required physics performance of TOTEM which demands active detectors at 1 mm from the beam center, have enforced the development of new technologies for these detectors. A main issue has been the welding technology employed for the thin window that separates the vacua of the machine and the Roman Pot, still minimizing the distance of the detector from the beam. As result of this development, a thickness and a planarity of less than 150 μm and 20 μm respectively have been achieved for the thin windows produced. Each Roman Pot detector is equipped with a stack of ten planes of novel silicon strips, with the sensors approaching the thin window to a few hundreds of microns. The single-sided silicon microstrip detectors have been fabricated with planar technology, with the special characteristic of reducing the insensitive area at the edge facing the beam to only ~50 μm and thus maximize the acceptance of scattered protons at microradian angles. Five of the planes have their strips oriented at an angle of +45º, while the other five are oriented at -45º. The

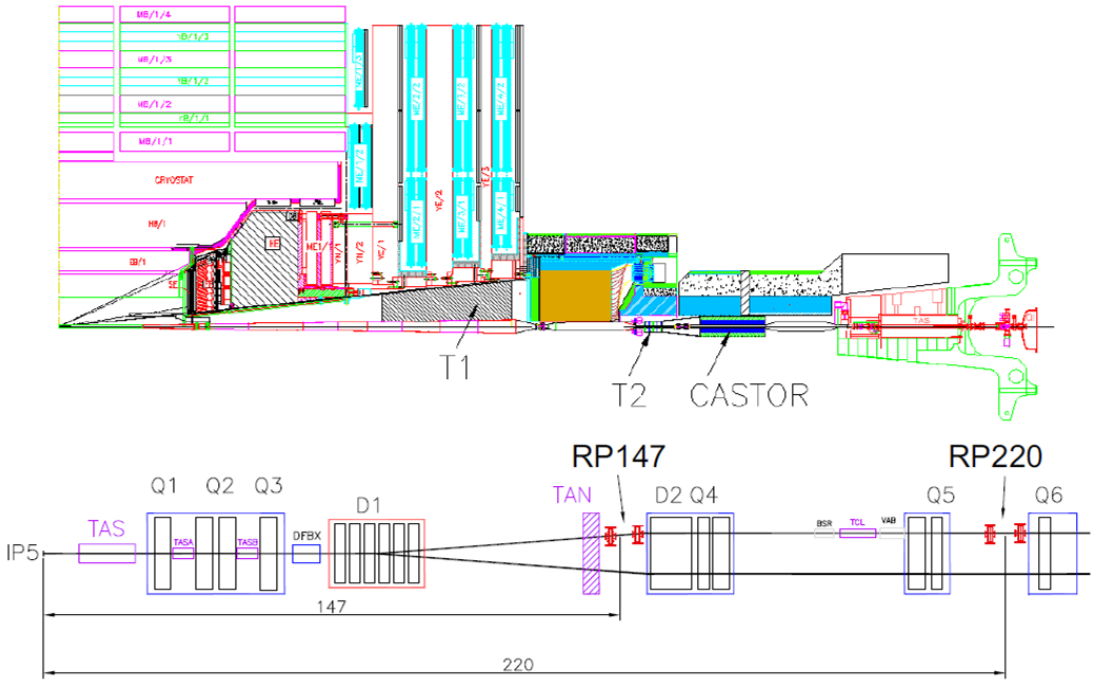

Figure 1.11 The TOTEM forward trackers T1 and T2 embedded in the CMS detector together with the planned CMS forward calorimeter CASTOR (top). The LHC beam line on one side of interaction point IP5 and the TOTEM Roman Pots at distances of about 147 m (RP147) and 220 m (RP220) (bottom) [61].

planes are placed so that the strip directions alternate between consecutive planes. This topology allows for a single hit resolution of ~20 μm. Each plane has 512 strips with 66 μm pitch processed on very high resistivity n-type silicon wafers with 300 μm thickness. The read out of all the TOTEM subsystems is based on the custom-developed digital VFAT (Very Forward Atlas and Totem) chip [60], which is in a 0.25 μm CMOS technology. A schematic drawing of a Roman Pot unit and station is shown in Fig. 1.12.

Given the bunched structure of the beams, at the LHC ~25 collisions occur within a time range of 170 ps every 25 ns. Because of the large number of interactions within one bunch, combinatorial background is a serious problem at full intensity. Nevertheless, the situation can be improved with proton timing, since the time difference between two protons determines the position of the interaction along the beam. The required time resolution for an acceptable reduction of the combinatorial diffractive background at a luminosity of $1 \cdot 10^{34}$ $cm^{-2}s^{-1}$ is 10 ps. The requirements on detectors aimed at Roman Pots can be summarized as follows:

- A single point resolution of 30 μm
- A dead space at the detector edge of 50 μm

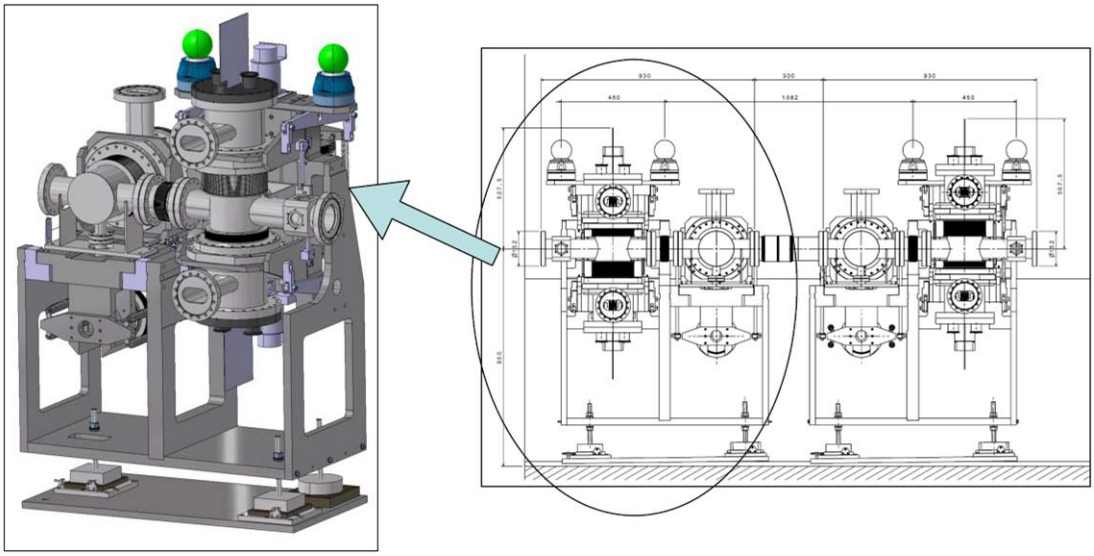

Figure 1.12 The Roman Pot unit (right) and the Roman Pot station (left) [65].

• A relative position accuracy between opposite detectors (i.e. partially overlapping detectors) of 10 μm

• A time resolution of 10 ps

• An occupancy below 1%

• Radiation tolerance up to 100 Gy and $5 \cdot 10^{13}$ p/cm^2 per year

• Readout and trigger capability with the DAQ (Data AcQuisition) of the experiment

• EMI immunity

• An affordable cost

Although the TOTEM experiment has been successfully taking data since the beginning of 2010, considerations to equip some Roman Pots partly with another type of silicon detectors are being made. Technologies proposed so far are planar 3D detectors [62], i.e. devices with a conventional planar microstrip interior and active edges, and GAPDs [63]. In particular, the TOTEM experiment is looking at GAPDs as one possibility to try to reach a time resolution of 10 ps in the measurement of forward protons. Time resolutions of 10 ps or less have been reported with GAPD detectors that include TDCs (Time-to-Digital Converters) in their on-chip readout electronics [64]. Moreover, the TOTEM experiment could also benefit from other of the outstanding capabilities of GAPD detectors. To start with, the requirement on the dead space at the detector edge can be easily accomplished by not placing any pads at the side of the chip that is closest to the beam. In addition, a single point resolution of 30 μm or even less is achievable by controlling the sensor size. Small sensor sizes also help to keep the occupancy at low levels.

Finally, as it will be demonstrated in this thesis, GAPD detectors can be operated in a trigger mode showing excellent performance. Nevertheless, the requirement on radiation tolerance should be further investigated.

1.5 Other applications

Apart from HEP experiments, there exists a wide range of applications that require the measurement of radiation, mainly optical signals in the visible and near infrared spectrum, and therefore could benefit from the extraordinary capabilities of GAPDs. Target applications are as diverse as biomedical imaging [66-68], Raman and near infrared spectroscopy [69, 70], 3D cameras [71], distance ranging [72] and space [47]. Until recently, PMTs (PhotoMultiplier Tubes) and CCDs have been the sensors of choice in most of these fields, however they are bulky and expensive. With the progress of the CMOS technology, MAPS (also known as CMOS sensors) have emerged as a solid alternative. Actually, MAPS outperform CCDs in terms of speed, noise and cost. Beyond that, SiPMs (Silicon Photomultipliers) appear as very promising devices for the detection of optical signals as weak as single photon events. Like GAPDs, SiPMs present outstanding capabilities regarding the sensitivity, internal gain and timing response. However, their spatial resolution is low. GAPDs add high resolution to all the pluses offered by SiPMs.

Some applications of particular interest that could benefit from GAPDs are AFI (AutoFluorescence Imaging), SPECT (Single-Photon Emission Computed Tomography) and CT (Computed Tomography) systems. AFI is a technique that exploits the autofluorescence phenomenon, i.e. the light emitted naturally by some molecules, to diagnose certain health diseases such as cancerous tumors. The performance of this technique can be described as follows. After excitation by a short wavelength light source, the fluorescent molecules or fluorophores emit light at another wavelength, typically longer. The intensity of the emitted light is fixed by the fluorophore concentration, and in turn this varies depending on the health status of the biological tissue. AFI systems use the variation in the autofluorescence intensity as a way to distinguish between healthy and unhealthy tissues.

The emission of light from any sample, occurring from electronically excited states due to the absorption of photons, is a form of luminescence known as photoluminescence. This is a statistical process that usually follows an exponential decay. The average time between absorption and emission of light (or excitation and relaxation of the excited states) is defined as lifetime. Moreover, the photoluminescence can be divided into two categories, phosphorescence and fluorescence. The prior involves a transition that is forbidden by the laws of quantum

mechanics. The probability of the forbidden transition occurring is low, the emission rate slow and the phosphorescence lifetime relatively long (in the order of milliseconds to seconds). In contrast, the transition responsible for the latter is allowed, resulting in a significantly shorter relaxation time in the order of a few nanoseconds. However, because some of the original energy is dissipated due to the loss of vibrational energy when electrons go from an excited state to the ground state, the emitted photons have lower energy (longer wavelength) than those absorbed. This phenomenon, known as Stokes shift, appears to be a very interesting feature that is exploited by AFI systems.

In contrast to other techniques based on the fluorescence phenomena, such as FLIM (Fluorescence Lifetime Imaging Microscopy), the autofluorescence does not require the introduction of fluorescently-labeled probes into the biological samples under investigation. This situation is advantageous in terms of avoiding toxicity as well as unwanted background signals, which can be originated by the probes and violate the integrity of the obtained results. For these reasons, AFI is gaining great interest as a newly emerging technique, since it can provide information about biological tissues without having to add any external agents.

A typical AFI set-up uses a light excitation source in combination with a narrow bandpass filter, a long-pass filter with an appropriate cut-off wavelength and a detector system. The filters are used to discriminate the autofluorescence from the illumination wavelength and also to minimize the unwanted autofluorescence from other molecules than those of interest. Two possible configurations for the measurement of the autofluorescence are depicted in Fig. 1.13. The main contributors to the autofluorescence phenomenon in human tissues, specifically from the gastrointestinal tract, are intercellular small molecules, such as flavins and vitamins, and extracellular matrices, such as collagen or elastin. In particular, flavin, which presents the most substantial and measurable autofluorescence intensity, has an optimal excitation wavelength of 450 nm and a peak autofluorescence emission of 520 nm.

AFI may have a direct application in endoscopic capsules aimed to diagnose and treat many diseases of the gastrointestinal tract. Endoscopic capsules are non-invasive devices that are being developed to improve the conventional endoscopic instruments, which are not only discomfortable and painful for the patient but also involve some risk of infection and damage to internal organs [67, 73]. The endoscopic capsule requires compact and low power electronics. This, together with the need for very sensitive light detectors imposed by the weakness of the autofluorescence emission, makes GAPDs ideal candidates for the present application.

Regarding tomographic techniques, monolithic GAPDs have been proposed to replace PMTs and SiPMs in PET scanners just recently [68]. However, they could also be used in SPECT and CT systems. Like PET, SPECT and CT are nuclear medicine imaging techniques

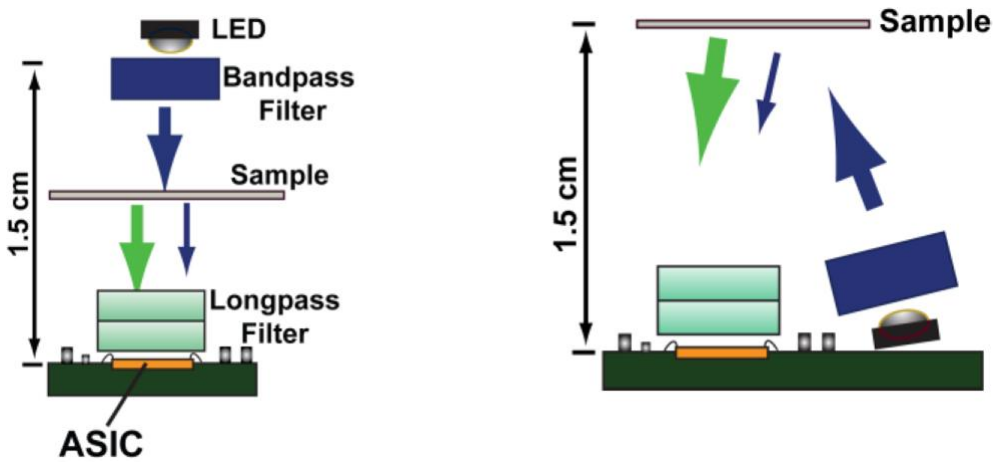

Figure 1.13 Autofluorescence measurement setup. The biological sample is positioned in between the light source and the detector (left). The light source and the detector face the sample (right). In both cases the blue arrow represents the illumination light and the green arrow the fluorescence [67].

that use gamma rays (PET and SPECT) or X-rays (CT) to generate a 3D image of a patient as a diagnostic tool of cancerous tumors, amongst other diseases. PET and SPECT techniques employ radioactive tracer material, a chemical compound (typically glucose or an amino acid) in which one or more atoms have been replaced by a radioisotope. The radioactive decay of the radioisotope results in the emission of gamma radiation of a few hundred keV. Once introduced to the body, organs and tissues process the radioactive tracer as part of their normal metabolic function. However, cancerous cells have a much higher metabolic rate than other cells and thus collect a greater concentration of tracer, which results in a higher emission of gamma radiation. Both the place of origin and concentration of the emitted gamma radiation are detected by the scanner. Nevertheless, PET and SPECT systems use tracers of different nature, which determine the topology of the emitted gamma radiation. The tracer used in PET emits positrons that annihilate with electrons after travelling a short distance (~1 mm) within the body, which causes two 511 keV photons being emitted at almost 180º to each other. PET scanners detect these two photons coincident in time and hence it is possible to localize their source along a straight line of coincidence. In contrast, the tracer used in SPECT emits gamma photons above 100 keV that can be measured directly. As a consequence, PET scanners provide higher resolution images than SPECT, at the expenses of a significative higher cost, partly because SPECT scanners can work with radioisotopes more easily obtainable. Apart from that, CT imaging is based on the absorption of X-rays of less than 140 keV as they pass through the different parts of the body. Depending on the amount of absorbed X-rays, a different amount of radiation will pass through and exit the body. When compared to traditional 2D medical radiography, CT scans provide several advantages in terms of high contrast resolution and rotation of the generated 3D images in different planes for a better diagnostic task. Another

possibility goes through the integration of CT into PET or SPECT within a single system, which has recently emerged as a brilliant imaging technique capable to provide extremely fine 3D localization of high uptake tissues. A schematic diagram of a PET scanner is depicted in Fig. 1.14.

Although SPECT imaging is particularly aimed at the detection of cancerous tumors, this technique can also be used to screen the function of the heart during the different stages of the cardiac cycle, provided that the electrocardiogram of the patient guides the acquisition of images. Thus, given that cardiac SPECT is triggered, this imaging technique is known as gated-SPECT. The tracer injected is taken up by cardiac tissues in rough proportion to myocardial perfusion (i.e. the flow of blood to the heart muscle). Therefore, areas of decreased uptake represent areas of relative or absolute ischemia (i.e. a decrease in the blood supply caused by obstruction of the blood vessels). Gated-SPECT imaging allows the simultaneous assessment of myocardial perfusion and left ventricular function. When combined with a cardiac stress test, heart conditions such as coronary artery disease and other heart abnormalities can be evaluated with this technique.

The imaging techniques mentioned are performed by using a gamma (PET and SPECT) or an X-ray (CT) source and a detector rotating around the patient to acquire multiple 2D images

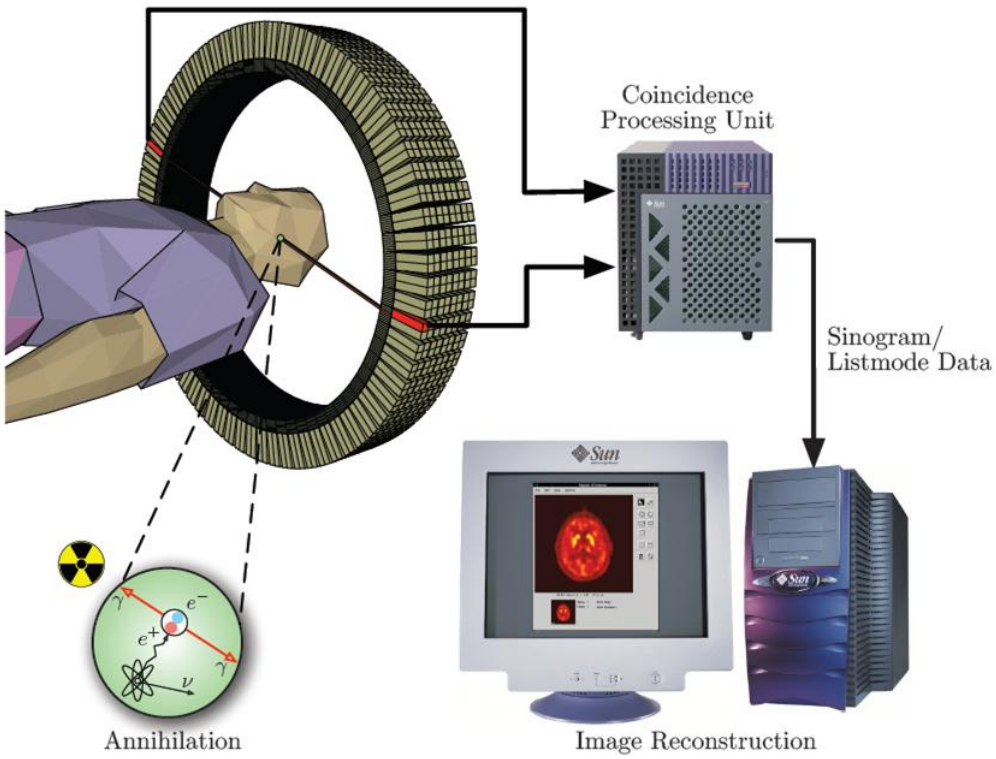

Figure 1.14 Schematic diagram showing the different processing steps of PET, from the annihilation process through registering the photons at the scanner ring until the final image reconstruction [75].

from different angles. A computer is then used to apply a reconstruction algorithm to the multiple projections, which yields a 3D image. This 3D image can be manipulated to obtain body sections in any orientation, which can be used to localize areas of abnormal tracer uptake in the case of PET and SPECT scans. The detector typically consists of one or more scintillators optically coupled to an array of PMTs or SiPMs. One of the scintillators most commonly used is the LYSO (cerium doped Lutetium-Yttrium OrthoSilicate) crystal, which has an emission spectrum that nominally peaks at 430 nm when it is excited by gamma photons or X-rays [74]. To detect the scintillator output, most scanners use PMTs or SiPMs. However, these detectors could be replaced by GAPDs to obtain a better performance in terms of contrast and spatial resolution. To achieve such a target, GAPD detectors must have sensitivity to the violet-blue range of the spectrum, minimum noise, high fill-factor, trigger capability (gated-SPECT), radiation tolerance, EMI immunity and an affordable cost. Moreover, GAPD detectors aimed at PET systems must include readout electronics capable to tag at very high rates the incoming signal with a timing label. In other words, PET detectors require a readout circuit with a TDC.

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Chapter 2

Geiger-mode avalanche photodiodes in CMOS technologies

This chapter reviews the most important aspects of the GAPD technology. The first section explains in great detail the principle of operation of avalanche photodiodes, both in linear and Geiger modes. The most important figures of merit, regarding the different sources that contribute to the pattern noise of the sensor, probability to trigger an avalanche, photon detection probability and timing resolution, are outlined in the second section. Next, the state-of-the-art of the GAPD technology is described. Both custom and CMOS manufacturing processes of GAPDs are commented. The evolution of the sensor noise per area as a function of the technology node of CMOS technologies is also summarized in this section. Finally, the last section is an introduction to the readout circuits that are required by the sensor. The different modes of operation of the sensor, mainly the free-running and the time-gated regime, are also presented in this last section.

APD devices are sensitive to impinging radiation in the form of high energtic particles and photons, but output signals can appear also as a consequence of the intrinsic noise generated by the sensor. Another possibility is to inject charge by electrical means. Since in this thesis the GAPD technology is explored mainly for particle tracking purposes, but light applications are also investigated in a complementary way, impinging radiation refers to high energy particles and photons from now on.

2.1 Principle of operation

A p-n junction reversely biased above its breakdown voltage (V_{BD}) and equipped with quenching and recharge circuits constitutes essentially a GAPD. When photons or ionized particles are absorbed by the junction, an avalanche current pulse may be triggered. The quenching circuit stops the avalanche current to prevent the destruction of the device, while the recharge circuit prepares the device for the following ignition. The avalanche current can be easily detected by the readout electronics. Before examining in detail the operation of GAPDs, some basic notions about p-n junctions will be reviewed here.

A p-n junction is created when a p-doped semiconductor and an n-doped semiconductor are

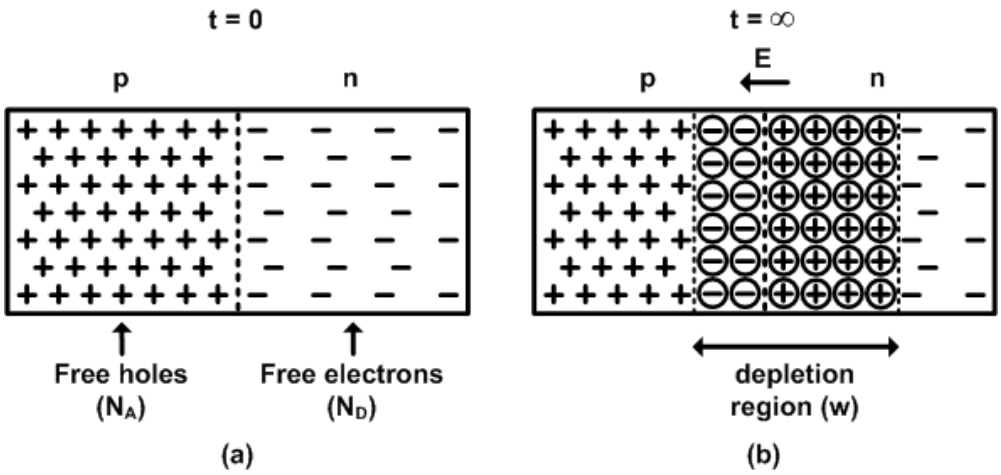

Figure 2.1 Creation of a p-n junction (a) and apparition of the depletion region (b).

brought into contact (Fig. 2.1). Both semiconductors are doped with a certain type and concentration of impurities to provide free charge carriers in the material. Thus, the p-doped semiconductor contains holes (acceptors) as impurities intentionally introduced into the silicon crystal lattice at a given density N_A. In contrast, the n-doped semiconductor contains electrons (donors) at a density N_D. Moreover, in the p-doped semiconductor the concentration of holes is higher than the concentration of electrons. This is also true vice versa for the n-doped semiconductor. It is said that in the p-doped region the holes are the majority charge carriers and the electrons the minority charge carriers, and vice versa for the n-doped region. Due to the carrier concentration gradient, the excess holes in the p-region diffuse to the n-region, while the excess electrons in the n-region diffuse to the p-region. As a result, an excess negative charge is created in the p-region and a positive charge is created in the n-region of the junction (Fig. 2.2-a). This in turn induces an electrical field over the junction (Fig. 2.2-b), which generates a reverse drift current in contraposition to the diffusion flow. Thus, the direction of transport by drift is always from minority side to majority side, i.e. electrons drift from the p-region to the n-region and holes drift in the opposite direction. As a result, the electrical field quickly sweeps any free charge carriers out of the junction, creating a region nearly empty of free charge carriers which is called the space charge region or depletion region [1].

A p-n junction with no external bias is in thermal equilibrium between diffusion and drift, which results in a zero total current over the junction. The electric potential difference across the depletion region in thermal equilibrium is known as the built-in potential of the p-n junction (Fig. 2.2-c). It can be expressed as

$$V_{bi} = \frac{k_B \cdot T}{q} \cdot \ln \frac{N_A \cdot N_D}{n_i^2} \tag{2.1}$$

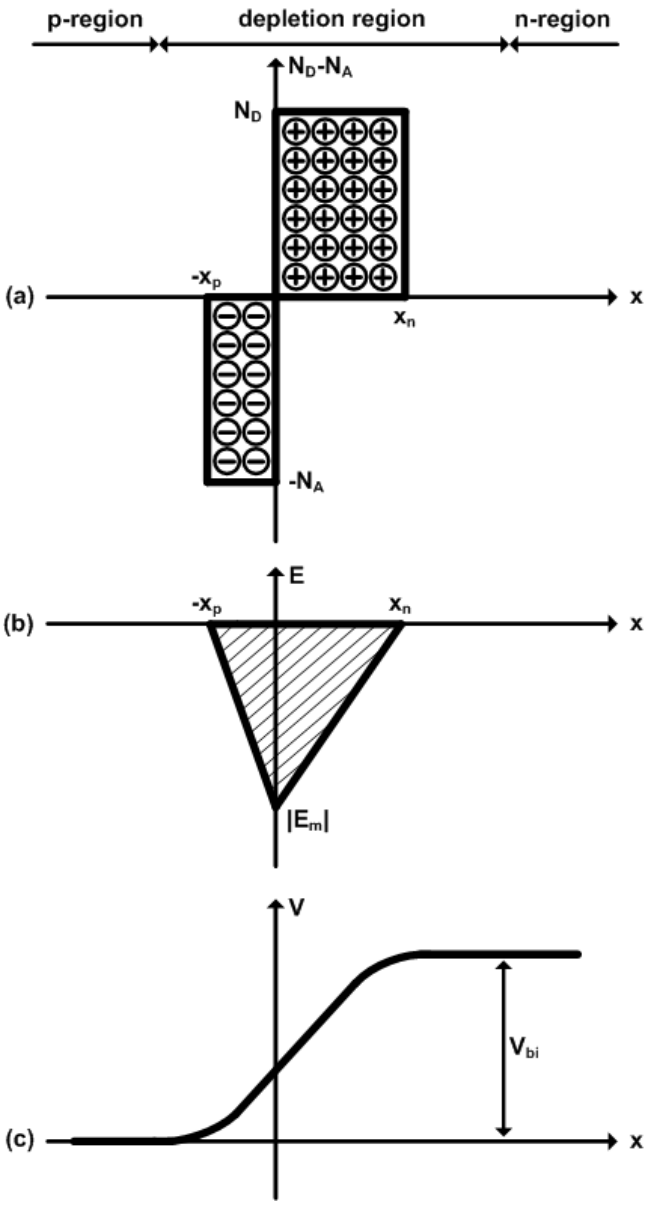

Figure 2.2 Abrupt p-n junction in thermal equilibrium: impurity distribution (a), electric field distribution (b) and potential variation with distance (c).

where k_B is the Boltzmann constant ($1.380 \cdot 10^{-23}$ J/K), T the absolute temperature of the junction, q the charge of the electron ($-1.602 \cdot 10^{-19}$ C) and n_i the intrinsic carrier concentration of the semiconductor (silicon in this case). Moreover, assuming an abrupt junction in thermal equilibrium, the spatial extend of the depletion region in the n-type semiconductor (x_n) and in the p-type semiconductor (x_p) can be derived from the density of donors and acceptors. This results in the equation

$$N_A \cdot x_p = N_D \cdot x_n \tag{2.2}$$

which indicates that the side with the lower concentration will have the longer extension of the depletion region. Considering that the transition from the p-region to the n-region is set at x=0, the electrical field (E) and the potential difference (V) in the depleted p-region are given by [2]

$$E(x) = -\frac{q \cdot N_A}{\varepsilon_S}\left(x + x_p\right) \tag{2.3}$$

$$V(x) = \frac{q \cdot N_A}{2\varepsilon_S}\left(x + x_p\right)^2 \tag{2.4}$$

and in the depleted n-region are given by

$$E(x) = -\frac{q \cdot N_D}{\varepsilon_S}\left(x_n - x\right) \tag{2.5}$$

$$V(x) = \frac{q \cdot N_A}{2\varepsilon_S} x_p^2 + \frac{q \cdot N_D}{2\varepsilon_S}\left(x_n - \frac{x}{2}\right)x \cdot \tag{2.6}$$

Here ε_S is the permitivity in silicon ($1.035 \cdot 10^{-12}$ F/cm). In this approximation, the electrical field is zero outside the depletion region. From x_n and x_p, it grows linearly towards the center of the junction, where it reaches its maximum value [1], expressed by

$$\left|E_m\right| = \frac{q \cdot N_A \cdot x_p}{\varepsilon_S} = \frac{q \cdot N_D \cdot x_n}{\varepsilon_S} = \sqrt{\frac{2q}{\varepsilon_S} \cdot \frac{N_A \cdot N_D}{N_A + N_D} \cdot V_{bi}} \cdot \tag{2.7}$$

The total width of the depletion region (W) is given by

$$W = \sqrt{\frac{2\varepsilon_S}{q} \cdot \frac{N_A + N_D}{N_A \cdot N_D} \cdot V_{bi}} \cdot \tag{2.8}$$

A depletion capacitance (also referred as the diode capacitance) can be assigned to the depletion region as in Eq. 2.9, where A is the junction area

$$C_D = \frac{\varepsilon_S}{W} \cdot A \cdot \tag{2.9}$$

If an external bias is applied to the p-n junction, the previous equations are still valid to describe the behavior of the diode, with the only exception of having to replace V_{bi} by $V_{bi} - V$ in Eq. 2.7 and Eq. 2.8 [1]. Depending on the value of the applied voltage, the junction will operate in one of these three main regions: forward, reverse and breakdown (Fig. 2.3). If a positive bias voltage larger than the built-in potential is applied (forward region), an intensity current given by the Shockley ideal diode equation

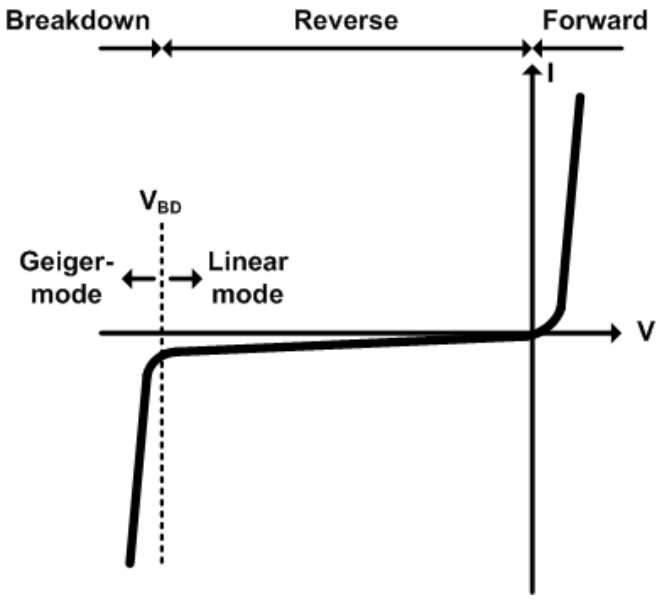

Figure 2.3 I-V characteristic of a p-n junction. The value of the applied voltage determines the working region of the device: forward, reverse and breakdown.

$$I_f = I_0 \cdot \left(\exp\left(qV/nk_BT\right) - 1\right) \tag{2.10}$$

will flow through the terminals of the junction. In Eq. 2.10, I_0 is the reverse saturation current, V the forward voltage applied across the junction and n the ideality factor (typically between 1 and 2). In this case, the voltage applied supplies free electrons and holes with the extra energy they require to cross the junction as the width of the depletion region of the p-n junction is decreased. In contrast, if a negative bias voltage is applied (reverse region), very little current will flow. Here, the electric field of the junction and the width of the depletion region will grow with the applied voltage, thus causing the drift velocity and kinetic energy of free charge carriers injected into the depletion region to increase. When the reverse bias becomes very large (breakdown region), the electric field in the depletion region is so strong that it can accelerate free charge carriers up to a point at which they gain enough energy to break a covalent bond when colliding with lattice atoms, thus generating a new electron-hole pair in a process that is called impact ionization [2]. Both the original and secondary carriers will be accelerated by the electric field and possibly contribute to the generation of more electron-hole pairs, which leads to a chain of impact ionizations. As a result of this effect, commonly known as avalanche multiplication, a detectable current pulse is generated. This detectable pulse is also referred to as Geiger current or Geiger pulse.

The breakdown region can be further subdivided into the linear and Geiger-mode regions. Diodes operated in the linear region are called linear APDs (Avalanche Photodiodes), whereas

Geiger-mode diodes are referred to as GAPDs. In the linear region, where the diode is biased slightly below the breakdown voltage, the electrical field is strong enough to cause significant ionization through free electrons, but not through free holes. This is a consequence of the higher ionization coefficients of electrons in comparison with holes, which results in a range of reverse bias where electrons gain enough energy for impact ionization but holes do not. Moreover, the impact ionization process is not self-sustained and therefore the gain of the device is proportional to the impinging radiation flux. This moderate gain, which in addition is severely affected by background noise, makes linear APDs unsuitable for the detection of single photons [3]. Instead, linear APDs can be used to detect clusters of photons and to determine their energy. In contrast, in the Geiger-mode region the diode is biased beyond the breakdown voltage, achieving an electric field of the order of 10^6 V/cm at the depletion region. By doing so, both electrons and holes can contribute to the generation of new electron-hole pairs. Since the diode is biased well above the breakdown voltage, the avalanche process of charge carrier generation is self-sustained, resulting in the rapid discharge of the diode depletion capacitance and a virtually infinite internal gain of 10^5-10^6. In this configuration, the GAPD produces the same signal regardless of the number of primary electron-hole pairs, i.e. it is a binary device and the proportionality to the impinging radiation flux is lost. The charge generated in an avalanche is given by [3]

$$A \propto Q = C_D \cdot \left(V - V_{BD}\right) = C_D \cdot V_{OV} \tag{2.11}$$

where A is the gain, Q the generated charge and V_{OV} the reverse bias overvoltage above V_{BD}. In particular, the avalanche can be triggered by a single photon or a MIP (Minimum Ionizing Particle). However, it should be noted that the mere generation of an electron-hole pair by an absorbed photon or MIP is not a sufficient condition to create an avalanche. The probability for an electron or hole from a generated electron-hole pair to trigger an avalanche (called avalanche breakdown probability) depends on the position in the depletion region [4]. Due to the higher ionization coefficient of electrons, the probability that an electron initiates an avalanche is always higher in silicon. Further details about the avalanche breakdown probability will be given in the next section.

On the other hand, once the avalanche has been triggered, the detector is blind for the detection of subsequent impinging radiation flux since the avalanche is self-sustained. For this reason, it is necessary to operate the GAPD with a suitable circuit that stops the avalanche and restores the initial bias condition. A detailed explanation about quenching and recharge circuits is given in section 2.4.

2.2 Figures of merit

This section outlines the performance parameters that typically characterize GAPDs. These parameters are then discussed in the context of device characterization in Chapter 3 and Chapter 4.

2.2.1 Dark count rate

In GAPDs, any free carrier located at the depletion region of the p-n junction can trigger an avalanche breakdown. In practice, an avalanche multiplication can be started by a primary carrier not induced by absorbed radiation. Uncorrelated (i.e. not related to previous avalanche events) avalanche multiplication events not related to absorbed radiation are known as dark counts. The frequency at which dark counts are generated is known as DCR (Dark Count Rate) and it is measured in counts per second or Hz. The main mechanisms that contribute to the generation of dark carriers in the depletion region are the thermal generation and band-to-band tunneling. Fig. 2.4 shows the energy and band diagram of the sources of noise counts in GAPDs.

Charge current generation in a semiconductor involves the transfer of electrons from the valence band to the conduction band (i.e. the break up of a covalent bond to form a free electron and a free hole). This process is known as electron-hole pair generation. In the case of silicon, the bandgap between the upper part of the valence band and the lower part of the conduction band is large (1.12 eV at room temperature), which makes very unlikely the direct transfer of an electron. To assist the process of electron-hole pair generation, silicon is doped with impurities. These impurities, also called defects or traps, act as intermediate states between the valence and the conduction bands. Thermal generation of carriers can occur whenever the thermal equilibrium condition of the semiconductor is disturbed. Due to the presence of traps, the rate of free carrier generation in darkness is significantly increased. The thermal carrier generation process in semiconductor devices is well explained by the SRH (Shockley-Read-Hall) theory.

At very high electric fields, the thermal generation of charge carriers is combined with band-to-band tunneling. This effect lies in the probability for an electron located at the maximum energy of the valence band to move to the minimum energy of the conduction band. Moreover, the tunneling probability can be greatly increased by the presence of impurities, which reduce the required energy to cross the bandgap. The typical electrical fields at which tunneling becomes a significant noise source start from 10^6 V/cm. Such electric fields are better achieved with advanced CMOS technologies, where the concentration of impurities is also higher and therefore the width of the depletion region narrower.

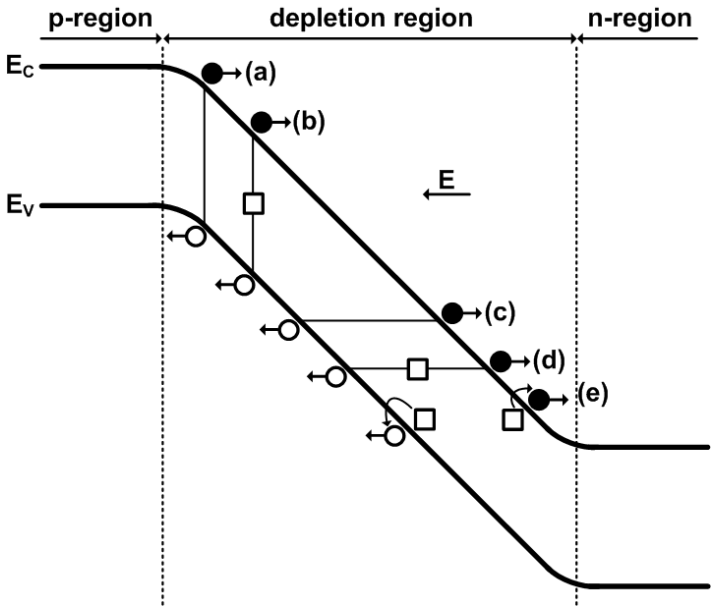

Figure 2.4 Sources of noise counts in GAPDs: thermal generation (a), trap-assisted thermal generation (b), band-to-band tunneling (c), trap-assisted tunneling (d) and afterpulsing (e). A white circle represents an electron, a black circle a hole, and a square a trap.

The DCR caused by thermal generation in the depletion region is dependent on the fabrication process, as it is influenced by the trap concentration, and directly proportional to the GAPD surface. It also depends on the reverse bias overvoltage due to the increase of the avalanche breakdown probability and enlargement of the depletion region. Obviously, it is a function of the working temperature (it is roughly divided by two each 10 ºC decrease). In contrast, band-to-band tunneling is extremely dependent on the reverse bias overvoltage and the doping profile of the device.

In GAPDs, the intensity of the Geiger current does not provide any information about the intensity of the impinging radiation. The Geiger current has the same amplitude regardless of whether it has been triggered by a single or multiple photons or particles. Intensity information is then obtained by counting the pulses generated during a certain period of time or by measuring the mean arrival time between successive pulses. It is therefore very important to characterize the DCR, since this parameter limits the detection of weak optical signals. In addition, it can be subtracted from each pixel to obtain the quantity of detected signal. Solutions based on cooling are commonly used to reduce the DCR.

2.2.2 Afterpulsing

The afterpulsing phenomenon is a source of correlated noise of GAPDs. When an avalanche breakdown is triggered in a GAPD, due to either a noise count or a signal event, a large number

of charge carriers flow through the depletion region. Some of these carriers may be captured by trapping centers for a finite time. If they are released after the sensor has recovered its avalanche multiplication capability, they may trigger a new avalanche breakdown and induce a noise count that is called afterpulse. The afterpulsing probability, that is the probability to trigger an afterpulse some time after a signal event or a noise count, depends on the number of deep-level trapping centers and the quantity of charge carriers travelling through the multiplication region during the avalanche. Deep-level trapping centers, i.e. energy levels created in the middle of the bandgap, typically have lifetimes that are longer than the dead time (i.e. the time required to stop the avalanche and recharge the sensor so as to fully recover the multiplication capability) of the GAPD. Consequently, the released charge carriers are susceptible to trigger a new avalanche breakdown not due to impinging radiation. The energy and band diagram corresponding to an afterpulse is also sketched in Fig. 2.4.

The afterpulsing probability can be limited by decreasing the quantity of charge carriers travelling through the depletion region during an avalanche. This can be achieved by reducing the parasitic capacitance seen by the sensitive node of the GAPD or forcing the premature extinction of the avalanche through active quenching circuits. Reducing the density of trapping centers is not an option at hand, since this parameter is dependent on the fabrication process and therefore out of reach by designers. On the other hand, the afterpulsing probability can be also limited by artificially increasing the dead time of the GAPD until the sensor has released all the trapped charges. This can be achieved by means of a hold-off circuit or by time-gating the sensor. Further details will be given in section 2.4.1.

2.2.3 Crosstalk

Crosstalk is a second source of correlated noise that is present in arrays of GAPDs. It is the phenomenon by which the avalanche breakdown in one pixel can trigger a secondary breakdown in a neighboring pixel. Depending on the mechanism of generation of crosstalks, one can distinguish between electrical and optical crosstalk.

As stated before, a large number of charge carriers flow through the GAPD during an avalanche. The generated electrons and holes start to drift immediately due to the high electric field of the depletion region. However, this charge generation occurs in a very limited volume, which produces a huge carrier concentration that diffuses in all directions much more strongly than drifts. In the particular case of a junction formed by a p^+ diffusion on top of an n-well, the majority of the generated holes will recombine with electrons after reaching the n-well side of the depletion region. Nevertheless, because the diffusion is so strong and only if the GAPDs are

not isolated from each other by placing them in different n-wells, some of the generated holes can diffuse through the n-well, reach a neighboring GAPD and eventually trigger a new avalanche breakdown. Electrical crosstalk can be prevented by placing the GAPDs in different wells. However, this solution reduces significantly the fill-factor of GAPD arrays.

Optical crosstalk occurs when a GAPD in avalanche breakdown emits photons because of the electroluminescence and these photons are detected by nearby GAPDs. Since the electroluminescence phenomenon is related to the current intensity that flows through the GAPD during avalanche breakdown, the optical crosstalk can be reduced by limiting the Geiger current. Moreover, surrounding each pixel with a deep thin trench filled with polysilicon is another solution used at present time to reduce the optical crosstalk [5].

2.2.4 High energy particle detection

In the experiments that will be performed at future linear colliders, very high energy particles of several GeV are expected to be observed. It is known that MIPs generate around 80 primary electron-hole pairs per μm of silicon. The probability for a primary electron-hole pair to trigger an avalanche breakdown is given by the avalanche breakdown probability $P_{trigger}(x)$

$$P_{trigger}(x) = P_e(x) + [1 - P_e(x)] \cdot P_h(x) \tag{2.12}$$

where $P_e(x)$ is the probability for a primary electron to trigger an avalanche breakdown and $P_h(x)$ is the analogous for a primary hole. $P_{trigger}(x)$ is the sum of two contributions: the probability for the primary electron to induce an avalanche breakdown and the probability for the primary hole to trigger an avalanche if the electron does not succeed. Electrons have in silicon a higher probability to trigger avalanches with respect to holes, and their difference increases with increasing fields. Moreover, $P_{trigger}(x)$ depends on the position where the primary electron-hole pairs are generated. The probabilities $P_e(x)$ and $P_h(x)$ can be expressed with the relations derived by Oldham [6]

$$\frac{d}{dx} P_e(x) = (1 - P_e) \cdot \alpha_e \cdot P_{trigger} \tag{2.13}$$

$$\frac{d}{dx} P_h(x) = -(1 - P_h) \cdot \alpha_h \cdot P_{trigger} \tag{2.14}$$

where α_e and α_h are the ionization coefficients respectively for electrons and holes. The probabilities $P_e(x)$ and $P_h(x)$ can be obtained numerically by solving Eq. 2.13 and Eq. 2.14 with the boundary conditions

$$P_h(x_p) = 0 \tag{2.15}$$

$$P_e(-x_n) = 0. \tag{2.16}$$

The latter equations state that a carrier generated at the limit of the depletion region cannot trigger an avalanche breakdown. The ionization coefficients depend on the electric field, and therefore on the reverse bias overvoltage. As stated in the previous section, the electric field reaches its maximum at the center of the junction, and it decreases to zero at the limits of the depletion region. If an electron-hole pair is generated in the depletion region, both carriers will be immediately separated by the high electric field. In addition, they may impact ionize and start an avalanche breakdown. However, if the electron-hole pair is generated in the undepleted region of the junction, minority carriers (electrons in the p-side, and holes in the n-side) may reach the depletion region by diffusion and trigger an avalanche breakdown.

2.2.5 Photon detection probability

The PDP (Photon Detection Probability) is defined as the probability that an impinging photon of a certain wavelength will trigger an avalanche breakdown. It can be expressed as

$$PDP = QE(\lambda) \cdot P_{trigger} \cdot FF \tag{2.17}$$

where QE(λ) is the quantum efficiency, $P_{trigger}$ the probability that a photogenerated carrier triggers an avalanche breakdown and FF the fill-factor of the device. In turn, QE(λ) is the ratio at which incident photons will produce electron-hole pairs in the active area of the device. It is given by

$$QE(\lambda) = \frac{number\ of\ e^- - h^+\ created\ and\ collected}{number\ of\ incident\ photons}. \tag{2.18}$$

The probability to trigger an avalanche has already been discussed in the previous section. The fill-factor is the ratio between the sensitive area and the total area of the GAPD detector. Several conditions must be accomplished so that an impinging photon generates a Geiger pulse. First, the photon should enter the detector without being reflected at the surface. Then, it has to be absorbed by the sensitive area and generate a primary electron-hole pair. Finally, the photogenerated carriers have to trigger an avalanche breakdown.

The incident photons that succeed in passing the oxide layer and thus penetrating the device are absorbed by the sensitive region or eventually cross the material. The condition for a photon to be absorbed, and hence to create an electron-hole pair, is to provide enough energy for an

electron to move from the valence band to the conduction band. Therefore, the energy of the photon has to be at least equal to the bandgap energy of the semiconductor material (silicon in this case). From the Planck equation

$$E_{ph} = \frac{hc}{\lambda} \tag{2.19}$$

where E_{ph} is the photon energy, h the Planck constant ($4.135 \cdot 10^{-15}$ eV·s), c the speed of light ($3 \cdot 10^{8}$ m/s) and λ the photon wavelength, an expression for the upper cut-off wavelength (λ_c) can be obtained

$$\lambda_c(\mu m) = \frac{1.24}{E_g} \cong 1.1 \mu m \tag{2.20}$$

where 1.24 is the hc product expressed in eV/μm and E_g the bandgap energy of silicon (1.12 eV at room temperature). Incident photons with wavelengths shorter than λ_c become absorbed as they travel in the semiconductor material. The intensity of the incident light, which is proportional to the number of photons, decays exponentially with the depth in the material. The absorption coefficient α(λ) determines how deep into a material the light of a particular wavelength can penetrate before absorption. The absorption coefficient is strongly dependent on the energy of the radiation, as it can be observed in Fig. 2.5. A large α(λ) means that the beam of light is quickly attenuated as it passes through the material, while a small α(λ) means that the medium is relatively transparent to the beam. In practice, this implies that photons with short wavelengths in the UV (UltraViolet) will be absorbed near the sensor surface, and photons having long wavelengths in the IR (InfraRed) can penetrate to a deeper depth. The low end of the wavelength spectrum that can be detected by a GAPD is at the UV region (~350 nm). UV photons with very short wavelengths will be absorbed very near the surface. There, the concentration of lattice defects and impurities is higher since this region is directly exposed during the fabrication process. Therefore, an electron created very close to the surface will recombine and has practically no options to diffuse until the depletion region. More detailed information on this topic can be found in [4].

The photon flux I(x) at a depth z from the surface is given by the absorption exponential law

$$I(x) = I_0 \cdot \exp(-\alpha(\lambda) \cdot x) \tag{2.21}$$

where I_0 is the incident flux entering the material. Then, the probability P(x) for a photon of wavelength λ to generate an electron-hole pair during its travel from the surface to a depth x can then be expressed as

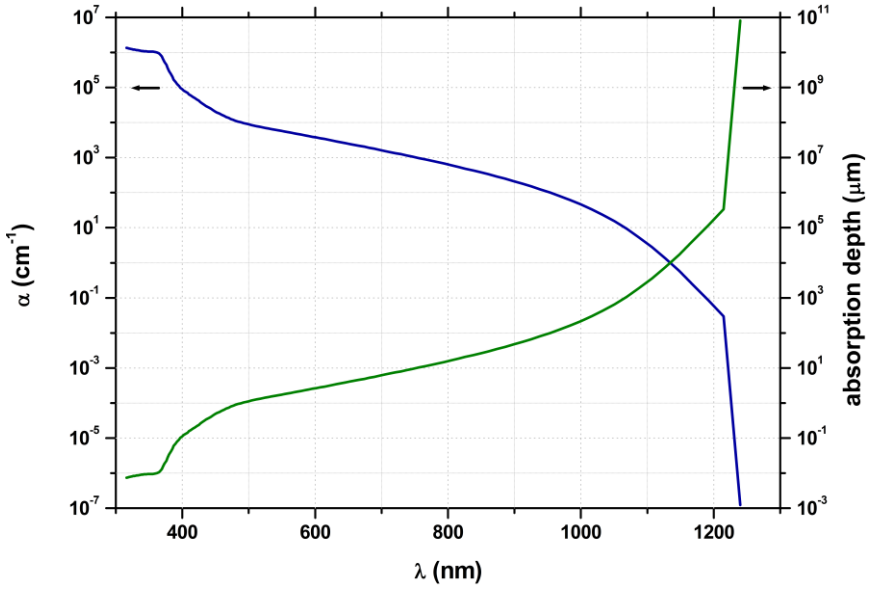

Figure 2.5 Absorption coefficient and absorption depth in silicon as a function of the impinging wavelength.

$$P(x) = 1 - \exp(-\alpha(\lambda) \cdot x). \tag{2.22}$$

To sum up, the PDP can also be written as

$$PDP = T \cdot [1 - \exp(-\alpha(\lambda) \cdot x)] \cdot P_{trigger} \cdot FF \tag{2.23}$$

where T is the transmittance from air to silicon via a silicon dioxide layer. However, in an experimental measurement, the PDP is calculated by subtracting the noise counts of the sensor measured in darkness to the total recorded counts in the presence of an incident photon flux, and dividing this result by the number of incident photons.

$$PDP = \frac{total\ counts\ -\ noise\ counts}{incident\ photons}. \tag{2.24}$$

At any detectable wavelength, the PDP is increased with the reverse bias overvoltage applied to the GAPD, but so does the sensor noise. Although this thesis is aimed to the detection of high energy particles with GAPDs, the PDP of these devices has also been investigated.

2.2.6 Timing resolution

The time interval elapsed between the arrival of impinging radiation at the sensor and the leading edge of the output pulse is defined as timing resolution or timing jitter. In GAPD detectors, the timing resolution depends on the photodiode and the readout electronics. In the

case of the photodiode, it is given by the depth and position across the sensor where the radiation is absorbed, and therefore it suffers statistical fluctuations. Thus, radiation absorbed directly in the depletion region produces electron-hole pairs that are capable to trigger a process of impact ionization almost immediately. In contrast, if radiation is absorbed in the undepleted region of the junction, minority carriers must reach the high electric field region before being able to start an avalanche process. Nevertheless, this contribution to the timing resolution decreases at higher reverse bias polarizations, as the ionization coefficients for electrons and holes are greater. As an approximation, the timing uncertainty related to the generation of the avalanche current can be expected to be in the range of the free carrier transit delay across the junction at saturation velocity, which is approximately 10 ps per μm of depth. In addition, the propagation of the avalanche current laterally through the sensitive area also influences the response time of the photodiode. It is expected that radiation absorbed close to the edge of the junction requires more time to fully discharge the GAPD capacitance than radiation absorbed at the center. Due to the vertical and lateral dependence of the timing uncertainty, GAPDs with narrower and smaller depletion regions typically show better timing resolutions. Finally, the total delay of the readout electronics also limits the timing resolution of the detector. Nevertheless, the utilization of standard CMOS processes to integrate the sensor and the readout electronics on the same substrate allows to achieve improved timing resolutions.

2.3 State-of-the-art

GAPDs can be produced with different methods of fabrication. Depending on the technology process used to manufacture the device, it is possible to discern between custom and CMOS GAPDs. Moreover, the depth of the depletion region determines if custom GAPDs are reach-through or planar. A brief explanation about each of these types of GAPDs is given next.

2.3.1 Custom GAPDs

In general terms, custom GAPDs can be categorized in two different approaches of fabrication: reach-through and planar devices. Reach-through GAPDs are also called thick GAPDs because of the wide depletion region of tens to hundreds of micrometers, which results in excellent detection capabilities. In contrast, planar GAPDs have depletion regions that are from hundreds of nanometers to several micrometers thick, which reduce the detection capabilities, but also the timing jitter and dead time.

In the 1970's, the group around McIntyre introduced the first reach-through GAPDs fabricated on silicon with a custom technology [7]. These diodes generally consist of a p^+-π-p-n^+ structure, where each of the four layers presents a thickness of <1 μm, 20 to 150 μm, ~15 μm and <10 μm, respectively [8]. Early edge breakdown effects are prevented by a p^+ enrichment and by reducing the silicon thickness over it by etching the wafer. The typical operating voltage of such devices is of several hundreds of volts. Therefore, the intrinsic silicon and p-doped layers are completely depleted when operating the Geiger-mode, causing the electric field to extend from the p^+ to the n^+ layers. All the charge carriers injected to the wide depletion region drift towards the high electric field region, the maximum value of which is located at the depleted p-region. There, the injected carriers trigger an avalanche breakdown. As a result of the wide depletion region, the PDP of these devices is extremely high (above 60% for a wavelength range from 400 to 1000 nm), specially to NIR (Near InfraRed) light. The DCR is kept under 1 kHz at room temperature even with large area detectors of several hundred of μm in diameter due to the ultra-clean process employed in the fabrication. As a consequence of the large diameter, these devices can only achieve timing resolutions on the order of 300-800 ps. Moreover, because the fabrication process is based on a proprietary non-planar technology and ultra-high resistivity silicon wafers, reach-through GAPDs present low fabrication yield, high costs and unsuitability for monolithic integration of detectors and readout circuits [9]. Fig. 2.6-a shows a cross-section of a reach-through GAPD with a p^+-π-p-n^+ structure.

Early planar GAPDs were introduced by Haitz in the 1960's [10] and further developed later by Cova [11]. These devices were typically implemented by means of an n^+ diffusion layer placed on top of a p-doped substrate. In this structure, the avalanche region is under the n^+ layer, with typical depths of up to a few micrometers. In addition, a shallow n-well surrounds the junction, thus forming a guard ring to prevent the premature edge breakdown. As a consequence of the proximity of the avalanche region to the surface of the semiconductor, these devices are more sensitive to blue and UV light. Apart from the increase in the timing resolution, planar GAPDs present breakdown voltages of a few tens of volts, which facilitate the integration of the device in CMOS technologies. The structure used by Haitz is depicted in Fig. 2.6-b.

Cova also introduced double epitaxial GAPDs in the late 1980's to improve the main characteristics of these devices. In this approach, epitaxial growth is used to fabricate planar GAPDs on a p-doped layer grown on top of an n-doped substrate [12]. The radiation that enters the device is absorbed in the p-doped epitaxial layer. Then, the generated electron-hole pairs are attracted by a low electric field to the shallow n^+-p junction. A p^+ implant at the center of the device serves as a guard ring. An interesting aspect of this structure is the utilization of a double-epitaxial structure, which allows the realization of two diode junctions. The buried junction between the epitaxial layer and the substrate prevents the electrons photogenerated in

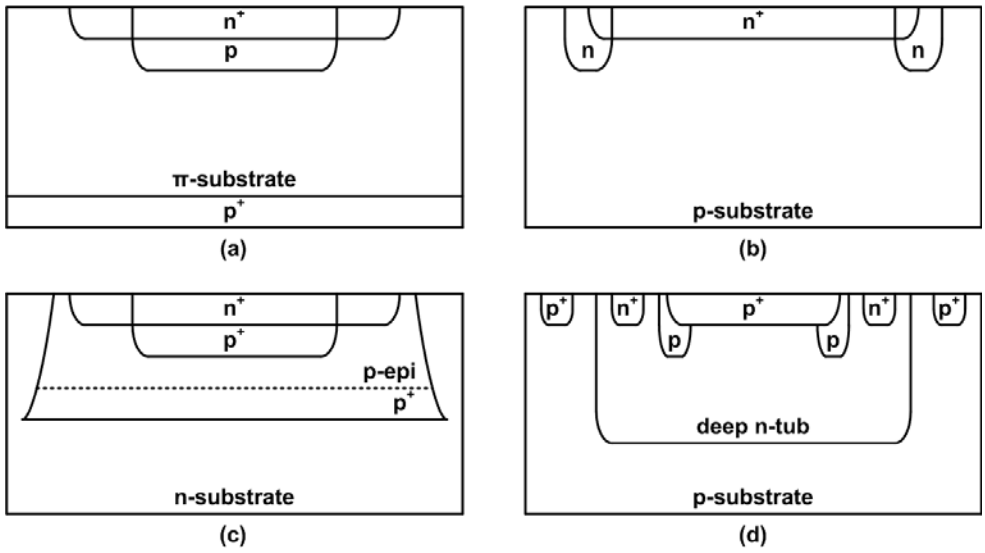

Figure 2.6 Schematic cross-sections of a reach-through GAPD (a), planar GAPD (b), double epitaxial GAPD (c) and CMOS GAPD (d). The cross-section depicted in (d) corresponds to the structure proposed by Rochas in [13]. The cross-sections are not to scale.

the substrate from reaching the avalanche region, thus increasing the timing resolution to 55 ps. A cross-section of a double epitaxial GAPD is shown in Fig. 2.6-c.

2.3.2 CMOS GAPDs

Standard CMOS processes provide reliable and reproducible electronics at low cost. Therefore, GAPDs manufactured with these technologies can take advantage of the ruggedness of the fabrication process as well as the ease to integrate on the same chip the readout electronics together with the sensor. Unfortunately, CMOS processes are focused on the fabrication of transistors rather than optical detectors, which results in severe design constraints. In particular, one of the major challenges is the obtention of a successful mechanism to soften the high electric field at the peripheral edges of the junction and thus avoid the PEB (Premature Edge Breakdown) of the device.

Needless to say, the monolithic integration of GAPDs and readout circuits leads to the improvement of some important performance parameters. To start with, the parasitic capacitance seen by the detector is drastically reduced. As described in section 2.2.2, the afterpulsing probability depends on the density of deep-level traps in the multiplication region and the number of carriers generated during an avalanche, which fill the traps. The trap density depends mainly on the cleanness of the fabrication process and cannot be modified by design. Nevertheless, the number of carriers generated during an avalanche may be reduced by

decreasing the parasitic capacitance introduced by the front-end circuit. Moreover, the reduction of the parasitic capacitance also improves the dynamic response of the sensor.

CMOS GAPDs can be achieved by means of several different configurations of the p-n junction. In addition, to prevent PEB effects as well as to ensure a planar and uniform avalanche region extending underneath the entire active area, guard rings of low doping diffusions are typically employed. Since many modern CMOS processes rely on p-doped substrates, a straightforward GAPD uses the n^+ diffusion layer and the same substrate to generate an n^+-p junction. In this case, a shallow n-well surrounds the junction to form the guard ring. In contrast, if the CMOS process has a deep n-well, a p^+-n junction can be obtained by means of the p^+ diffusion and the deep n-well. In this configuration, a low doped p-well diffusion is used to form the guard ring. The utilization of a deep n-well allows to isolate the GAPD from the substrate noise. Since the substrate and the deep n-well form an additional junction, free carriers in the substrate are prevented from diffusing into the junction. In addition, both the anode and cathode can be biased independently from the substrate. The latter structure was used to monolithically integrate GAPDs with the front-end electronics on a single CMOS die for the first time in 2003 [13]. This was achieved by Rochas using a 0.8 μm high-voltage standard CMOS process by AMS. Fig. 2.6-d shows the cross-section of the GAPD implemented by Rochas. This GAPD structure has been successfully implemented in a several CMOS processes, ranging from the old 0.8 μm node to the more advanced 90 nm node.

Noise performance is a major issue for GAPDs, especially for those GAPDs fabricated in deep submicron CMOS technologies. In these technologies, the presence of noise is more significant due to the higher doping profiles, reduced annealing steps and the presence of the STI (Shallow Trench Isolation). The higher doping profiles increase the effects of tunneling-induced dark counts, while the lack of annealing steps worsens the thermally-generated dark counts and afterpusing effects due to an increased presence of impurities. Moreover, the STI may induce a dramatic increase of the density of deep-level traps and generation centers [14, 15]. This isolation layer is compulsory constructed in the fabrication process of all the technologies at and below the 0.25 μm mark to reinforce the prevention of the punchthrough and latch-up in CMOS circuits. Due to the presence of the STI near the GAPD multiplication region, extremely high DCRs of the MHz order may be induced. These high DCRs are prohibitive in most applications. In an attempt to mitigate the DCR problem, several design techniques at the layout level have been investigated to force the physical separation of the STI from the GAPD avalanche region. Nevertheless, it is said that the progressive scaling down of CMOS technologies, pushed by the need of higher densities of integration and higher speeds, has introduced additional design challenges.

The typical trend of the DCR/area as the technology node decreases is reviewed in the shape of a graph in Fig. 2.7. Thus, GAPDs with a DCR/area per pixel ranging from less than 1 Hz/μm^2 up to several thousands of Hz/μm^2 have been reported for standard CMOS technologies between 0.8 μm and 90 nm [13, 16-37]. In this work, we have chosen the standard HV-AMS 0.35 μm CMOS technology because it provides a good tradeoff between DCR, fill-factor and readout speed. The details of Fig. 2.7 are summarized in Table 2.1.

The low fill-factor, which rarely exceeds the 10% due to the presence of the non-sensitive guard rings, STI-free techniques and readout electronics, is another of the main drawbacks of GAPDs fabricated in standard CMOS technologies. Although a fill-factor as high as possible is desirable in most applications, a 100% fill-factor is not mandatory. However, detector systems aimed to HEP experiments in future linear colliders cannot miss any incoming signal and a 100% fill-factor is then a must. Therefore, it is mandatory to explore novel solutions to maximize the fill-factor of GAPD detectors. The utilization of a common n-well that is shared by some or all the GAPDs of the detector increases the fill-factor up to almost the 70%, as it has been reported recently [40, 41]. Nevertheless, alternative solutions based on 3D-IC technologies achieve a high fill-factor of up to the 92% [42]. Both proposals will be further explained in Chapter 4 and Chapter 5.

2.4 Front-end electronics

As mentioned in section 2.1, GAPD detectors require special circuits to quench the avalanche current and recharge the sensor bias voltage after each ignition. Quenching and recharge circuits, along with any other circuit that may be monolithically integrated in the pixel, are referred as front-end electronics. A review on these circuits is presented next.

2.4.1 Quenching and recharge circuits

Upon Geiger avalanche, the self-sustained current pulse that flows through the p-n junction needs to be stopped in order to avoid self-heating and even burning the device. This operation is performed by the quenching electronics by lowering the reverse bias voltage down to or below V_{BD}, which disables the multiplication capability of the photodiode. Once the avalanche is quenched, the nominal operating voltage of the sensor has to be restored so that the device is sensitive again for upcoming Geiger avalanches. This operation is known as recharge or reset. There exist a variety of avalanche quenching and recharge techniques, partitioned in passive and active methods. They have been nicely reviewed in various articles, such as [43-45].

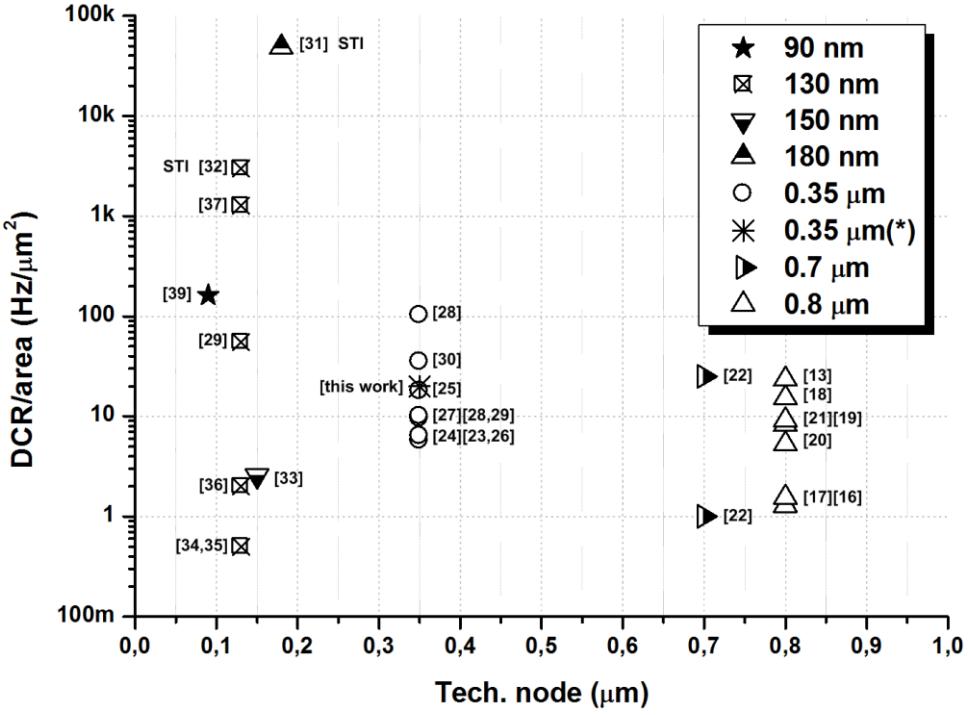

Figure 2.7 DCR/area as a function of the technology node. (*) corresponds to this work.

Tech. node	DCR/area (Hz/μm²)	Sensor area (μm²)	V_{ov} (V)	Architecture	Year	Reference
0.8 μm	1.29	38	2.5	8 x 4	2004	[17]
	1.55	32	2.5	4 x 8	2003	[16]
	5.30	113	5	single pixel	2005	[20]
	8.28	7854	3	64 x 1	2007	[21]
	9.21	38	5	32 x32	2005	[19]
	15.28	19	3	64 x 1	2005	[18]
	23.39	38	5	single pixel	2003	[13]
0.7 μm	1	100	4	single pixel	2007	[22]
	25	400	4	single pixel	2007	[22]
0.35 μm	5.73	78	2.5	4 x 112	2006	[24]
	6.37	38	-	60 x 48	2009	[23]
	6.37	314	5	1 x 32	2008	[26]
	9.55	314	4	single pixel	2008	[27]
	10	400	4	7 x 2	2009	[28]
	10	400	0.5	single pixel	2010	[29]
	18	38	3.3	128 x 128	2008	[25]
	20	2000	1	10 x 43	2013	this work
	35	314	3.3	single pixel	2011	[30]
	102	9800	5	7 x 2	2009	[28]
180 nm	48119	38	7	single pixel	2006	[31]
150 nm	2.55	78	4	single pixel	2011	[33]
130 nm	0.5	50	0.6	single pixel	2009	[34]
	0.5	50	1	32 x 32	2009	[35]
	2	50	1	single pixel	2012	[36]
	55	400	0.5	single pixel	2010	[29]
	1273	78	1.7	single pixel	2007	[37]
	3000	400	0.2	single pixel	2010	[32]
90 nm	161.14	50	0.13	single pixel	2010	[39]

Table 2.1 DCR/area as a function of the technology node. In the case of arrays, the median value has been used when available.

In PQ (Passive Quenching) methods, the p-n junction bias is self-adjusted by a resistive element placed in series with the sensor. The resistive element can be implemented by means of either a simple resistor of a few hundred kΩ [13] or a MOS transistor with the proper W/L ratio and bias [19]. Nevertheless, the MOS transistor option allows to achieve a better pixel miniaturization. In the PQ alternative, after having discharged the depletion capacitance of the p-n junction, the Geiger current charges the parasitic capacitance of the sensing node of the photodiode, which is due to the interconnections to the quenching and readout circuits. The parasitic capacitance as a function of the Geiger current (I_G) can be written as

$$C_P = \frac{\Delta Q}{\Delta V} = \frac{I_G \cdot \Delta t}{\Delta V}. \tag{2.25}$$

From Eq. 2.25, an expression for the increase in voltage of the sensing node can be obtained

$$\Delta V = \frac{I_G \cdot \Delta t}{C_P}. \tag{2.26}$$

After some time, the Geiger current will have injected enough charge to the sensing node so that ΔV will reach V_{OV}. At this moment, the photodiode is no longer biased above the breakdown voltage and therefore the avalanche multiplication is no longer self-sustainable. As a result, the avalanche is quenched. The resistive quenching element (R_Q) together with the sensor resistance (R_D), the depletion capacitance of the sensor (C_D) and the parasitic capacitance (C_P) form an RC circuit that determines the quenching time of the sensor. Provided that $R_Q >> R_D$, the quenching time can be expressed as

$$\tau_Q = (C_D + C_P) \cdot R_D. \tag{2.27}$$

From Eq. 2.27 it can be inferred that large area GAPDs (where the junction capacitance becomes significant) connected to large area components (or a great number of components) will generate long quenching times. Since the charge carriers that are generated in the multiplication region during the quenching time can contribute to the apparition of afterpulses, it is very important to decrease the parasitic capacitance as much as possible.

On the other hand, AQ (Active Quenching) circuits sense the raising edge of the avalanche current or voltage, typically by comparing it to a threshold, and react back on the device by forcing the reverse bias voltage below V_{BD}. A good example that follows the voltage sensing scheme is implemented in [29]. The main goal of AQ circuits is to reduce the quenching time, and therefore minimize the number of carriers generated in the GAPD. Consequently, fast sensing and feedback circuits are required. However, it is rather difficult to implement AQ circuits with response times shorter than the time required to fully discharge the depletion and

parasitic capacitances [46]. For instance, for some of the GAPD pixels implemented in this thesis, which have a sensitive area of 20 μm x 100 μm and a total capacitance C_D+C_P of 556 fF, it is estimated that the full quenching action takes only a few hundred picoseconds. Moreover, AQ circuits tend to increase the parasitic capacitance as a consequence of the higher number of components connected to the sensing node. Therefore, it is very complicated to enhance quenching by active circuits, which often make unnecessary the added complexity and area occupation.

Other different quenching circuits have also been proposed, such as the current-mode quenching circuit [47]. In this circuit, the avalanche current is sensed through a current mirror and used to increase the resistance of, and eventually turn off, a transistor connected in series to the GAPD. This way the current flow is interrupted.

Similarly to quenching, the recharge operation can be accomplished by means of passive or active circuits. In PR (Passive Recharge), the same device used to passively quench the avalanche can be used to bring the sensor to new operating conditions. Consequently, both operations may be performed by means of a single device, a resistor or a MOS transistor. With the passive option, the recharge time (also known as reset time) is given by

$$\tau_R = (C_D + C_P) \cdot R_Q . \tag{2.28}$$

From Eq. 2.27 and Eq. 2.28, it can be inferred that PQ and PR circuits (see in Fig. 2.8-a the schematics diagram of a PQ-PR circuit) present poor control over the quenching and recharge times. In the first place, special consideration has to be taken with the value of the resistance, since high R_Q generate short quenching but long recharge times, and vice versa. Long enough recharge times are necessary to suppress the afterpulsing probability. However, long recharge times also limit the maximum achievable counting rate, which is given by the inverse of the full recharge time. This phenomenon typically leads to an afterpulsing/counting rate trade-off. Secondly, in passive recharge the GAPD bias voltage follows an exponential curve towards the nominal bias, as defined in

$$V(t) = V_{OV} \cdot \exp\left(- \frac{t - t_0}{RC} \right) \tag{2.29}$$

where the RC constant is equal to the product $R_Q \cdot (C_D+C_P)$. Therefore, given that the GAPD is biased above the breakdown voltage during all the recharge transition, it may occur that avalanches are triggered before the GAPD has been recharged to the nominal bias (i.e. in conditions other than desired). For those avalanches triggered during the recharge (the longer the recharge, the higher the probability), the sensor performances in terms of timing response

and detection capability are not only worse than expected, but also variable in time. In spite of these disadvantages, several GAPD detectors based on PQ and PR circuits have been reported to perform successful operation. In [13], for example, a circular GAPD of 6.4 μm in diameter is passively quenched and recharged by a fully integrated 270 kΩ polysilicon resistor, leading to a dead time (i.e. quenching plus recharge time) of 32 ns that is enough to suppress the afterpulsing effects. Based on this result, photon counting rates up to 10 MHz may be measured.

In contrast, AR (Active Recharge) circuits allow full control over the recharge time of the sensor, providing a prompt recovery of the GAPD nominal bias after the avalanche has been quenched (either passively or actively). They are typically implemented by means of a MOS switch, which is operated under a gate command. An interesting feature of AR circuits is that the recharge command can be delayed by means of additional active devices to enable the realization of a hold-off time (see in Fig. 2.8-b the schematics diagram of an AQ-AR circuit). During the hold-off time, the sensor undergoes passive recharge. The reverse overvoltage is kept extremely low on purpose so as to enable the release of the trapped carriers in the multiplication region due to an avalanche, with the consequent mitigation of the afterpulsing effects. When the desired hold-off time has been accomplished, the MOS switch is turned on to rapidly bring the sensor to operating conditions. The typical sensing node waveform of a GAPD is depicted in Fig. 2.9. Typically, AR circuits that allow the utilization of a hold-off time rely on monostable circuits [48, 49] or local oscillators [50]. However, more innovative solutions are often reported in the literature. In [46], active recharge after an adjustable hold-off time is accomplished by means of an active circuit based on a dual-threshold system. This circuit forces the rapid recharge of the sensor only when it senses that the voltage of the sensing node has decreased to a certain extent. The speed at which the voltage of the sensing node drops is controlled by adjusting the gate voltage of a MOS transistor, which in turn is used to passively quench and recharge in a first stage the avalanche. Another alternative proposed in [51] commands the hold-off time by means of an RC circuit included in a feedback circuit from the sensing node to the gate terminal of the quenching/recharge transistor.

2.4.2 Modes of operation

GAPDs can be operated in two different modes, the free-running and the time-gated regimes. In free-running, the detector is always biased above V_{BD} at a fixed voltage. Thus, the GAPD is always ready to trigger an avalanche, induced by either radiation or noise. There are some applications, however, where the signal to be detected originates from a trigger command and therefore the expected signal arrival time can be known in advance. This is the case, for example, of fluorescence lifetime imaging, NIR (Near InfraRed) and Raman spectroscopy, TOF

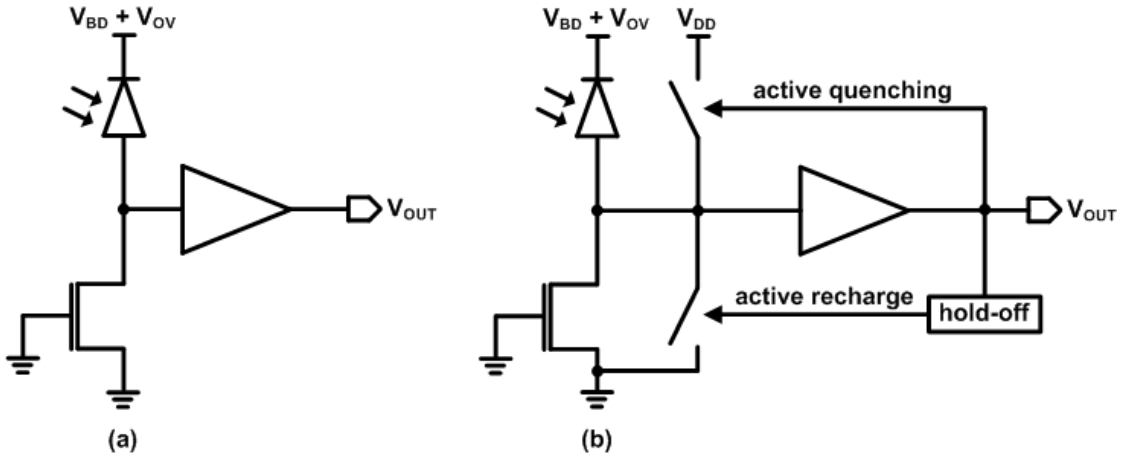

Figure 2.8 Traditional circuits for PQ-PR (a) and AQ-AR (b).

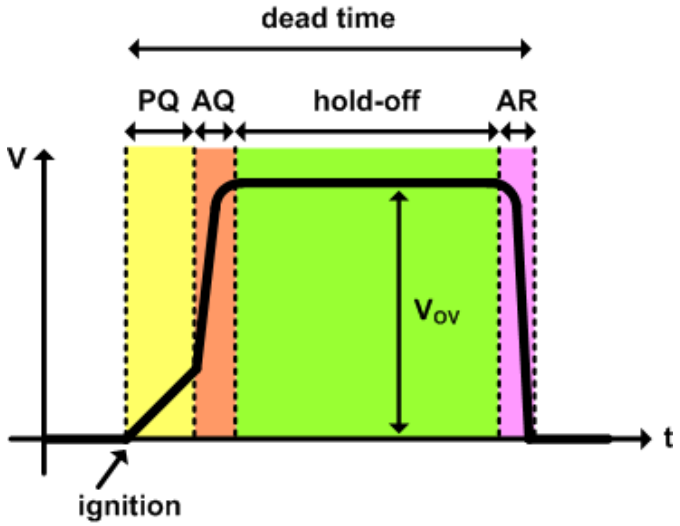

Figure 2.9 Typical GAPD voltage waveform during an avalanche.

(Time-Of-Flight) ranging or some HEP experiments. In these applications, it may be more convenient to operate the GAPD in the time-gated mode, in which the sensor bias is periodically kept below V_{BD} and increased to the desired V_{OV} for a well defined period of time around the expected signal arrival. As a result, the probability to detect the noise counts that interfere with the radiation triggered events is drastically reduced. Needless to say, no signal counts are missed because the expected radiation arrival time is covered by the active periods of the sensor.

The time-gated operation was originally applied in the 1980's [52] and widely exploited right afterwards [53, 54] to mitigate the high noise levels of III-V GAPDs. Therefore, the benefits of this technique in reducing the probability to detect the dark counts and suppressing the afterpulses have already been broadly reported. However, in the last few years there has been a growing interest in time-gated CMOS GAPDs motivated by the huge potential of this technique not only in reducing the detected noise but also in suppressing the unwanted background signal [30, 55]. In fluorescence lifetime imaging, for instance, the laser pulse used

to excite the biological sample to be tested can be so intense so as to completely blind the sensor. In this case, the photodiode can be kept inactive in the presence of the laser pulse and activated immediately afterwards to sense the faint light emitted by the molecules.

Short gated-on pulses can be achieved applying a high-frequency reverse bias voltage or properly activating and deactivating in-pixel MOS switches. In the first case, a high-frequency sinusoidal [56] or square-wave [57] voltage is usually applied to periodically activate and deactivate the sensor. Here, the positive peaks of the high-frequency voltage, which are above V_{BD}, are coincident with the estimated signal arrival. On the other hand, in-pixel time-gating circuitry relies on 1 MOS switch in its simplest form [30]. In this case, the sensor is connected to a fixed reverse bias voltage. By turning on the MOS switch, which is typically connected between V_{DD} and the sensing node of the GAPD, the sensor bias is decreased below V_{BD} and therefore deactivated. However, quenching and recharge circuits, either passive or active, are still needed in both cases. In the case of applying a high-frequency voltage, any Geiger avalanche would be quenched when lowering the reverse bias voltage at the gated-on termination, but the delay between these two processes could damage the device. In the case of in-pixel MOS switches, typically another MOS transistor is employed to quench the avalanches. The same element can be used to recharge the sensor so as to start a new gated-on period. Nevertheless, other in-pixel electronics used to record the Geiger avalanches, such as counters [28, 36] or memory cells [55, 58], can also be time-gated in conjunction with the sensor. The performance of MOS switches, counters and memory cells can be controlled by means of the fast signals generated by an FPGA, being possible to achieve gated-on times as short as 1 ns. A possible implementation of a time-gated GAPD pixel together with the required waveforms is depicted in Fig. 2.10-a (high-frequency reverse bias voltage) and in Fig. 2.10-b (MOS switches).

2.4.3 Readout circuits

The Geiger pulses are typically discriminated by means of in-pixel electronics integrated either with the sensor on the same chip or on a separate readout chip. The first configuration leads to a monolithically integrated pixel detector, while the second one results in an hybrid pixel detector (the term pixel refers to the sensor and readout channel in both approximations). In the hybrid case, the readout chip is attached to the sensor chip by means of bump bonding techniques. In both the monolithical and hybrid configurations, the most typical discriminator is the CMOS inverter [17, 28, 30, 40], although voltage comparators [13, 33, 51] and source follower circuits [59] can also be found in the literature. The CMOS inverter is the preferred choice because of its simplicity and efficiency. Upon Geiger avalanche, if the reverse bias

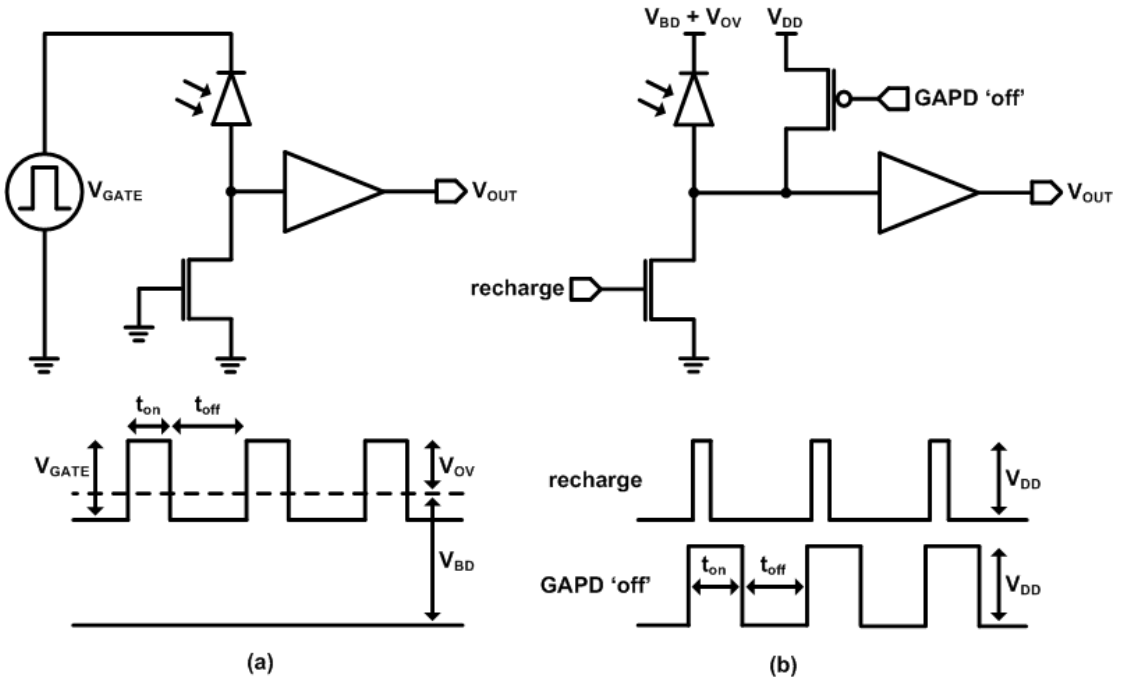

Figure 2.10 Time-gated GAPD and waveforms by means of a high frequency reverse bias voltage (a) and MOS switches (b).

overvoltage of the sensor is higher than the threshold voltage of the inverter, the analogue Geiger voltage is detected and converted into a digital pulse. Nevertheless, if the Geiger pulses are discriminated outside the image sensor, commercially available IC (Integrated Circuit) comparators are used.

Similarly, the detected Geiger pulses can be counted in situ [28, 60] or externally [30]. In the first case, additional electronics must be integrated with the GAPD either in the monolithical or hybrid approach to process the data generated by the sensor. There exist several different possible implementations, being the in-pixel the most common configuration. In this architecture, all the operations are performed and saved locally. The stored value is then read out at a later time. However, if the counting operation is performed off-chip, typically the outputs of the chip are connected to an FPGA which counts the Geiger pulses.

When counters and possibly memory cells are used to process the data generated by the sensor, it is said that the detector performs the photon counting modality. This modality is employed to measure the intensity of optical signals and it can be acquired with long enough integration time-windows. In contrast, applications that rely on TOF methods, such as 3D imagers, use the photon timing modality to measure the photon arrival time. In this modality, TDCs (Time-to-Digital Converters) are typically co-integrated with the sensor [25, 36, 40].

2.4.4 Array architectures

As described in section 2.3, GAPDs can be implemented in either custom or CMOS processes. However, while custom processes may assure excellent detectors thanks to the utilization of dedicated implants available in the fabrication process flow, they do not offer the possibility of integrating large scale electronics. Consequently, the only way to read out matrices with a large number of GAPDs fabricated in a custom technology involves hybrid solutions, which increase the parasitic capacitance of the sensing node. Another disadvantage of custom technologies is the low reliability of the fabrication process, which results in large process variations and high performance variability amongst the different GAPDs within an array. In contrast, CMOS technologies offer not only maturity, cleanliness and reduced fabrication costs, but also the potential of integrating complex electronics together with the sensor on the same chip. Moreover, much smaller pixel sizes can be achieved with monolithic pixel detectors. Since this thesis is aimed to monolithic detectors based on GAPD pixels, from now on only monolithic CMOS GAPDs will be considered.

Early GAPDs were stand-alone devices. Although these devices yielded excellent performance, they were very inefficient in terms of data acquisition. The need for image reconstruction was tedious and led to extremely long acquisition times. Nevertheless, the rapid progress of commercial CMOS technologies has enabled the fabrication of large bidimensional arrays of GAPDs. The first GAPD array monolithically integrated with a standard CMOS technology was reported in 2003 [16]. It consisted of 4 rows per 8 columns of pixels, with a CMOS inverter used as a Geiger discriminator. The array also comprised 4 8-input multiplexers for external selection of the column to be read at the 4 output pads. This GAPD array was read out in random access (row column sequential mode). Other possible architectures to read out GAPD arrays are the event-driven and pipelined based modes. The selection of one readout architecture or another depends on the final implementation of the detector system. A brief review of these architectures is provided next.

In the random access configuration, the pixels are read out sequentially either one by one (Fig. 2.11-a) or by rows or columns (Fig. 2.11-b). This configuration presents a simple implementation, but it leads to low frame rates. Moreover, an enormous number of arriving signal is lost. The first design demonstrating the feasibility of large GAPD arrays comprised a matrix of 32 x 32 pixels that was read out in random access [19]. Each pixel consisted of a GAPD, quenching transistor, CMOS inverter and column access circuitry. The chip also included a 32-channel decoder for row selection, a 32-to-1 multiplexer for column selection and one digital output pad. The main drawback of this design is the fact that only one pixel can be read out at any time while the incoming signal falling outside that pixel is lost.

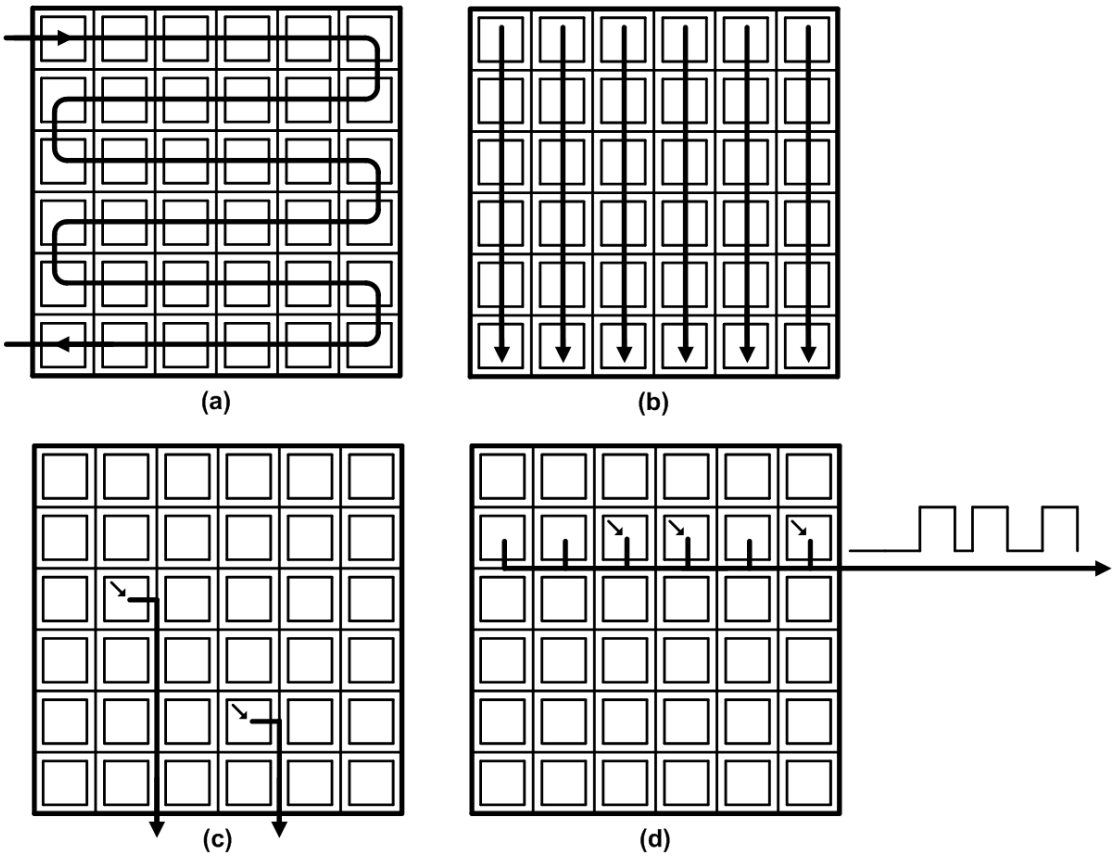

Figure 2.11 Array architecture: random access pixel-by-pixel (a), random access by columns (b), event-driven (c) and pipelined (d).

However, in those detectors aimed to very low intensity applications, the GAPD matrix can be read out in the event-driven approach (Fig. 2.11-c). In this readout mode, each column is transformed into a digital bus, which is accessed by a pixel in an asynchronous fashion every time that an event is generated. The address of the row that contains the triggered pixel is sent to the bottom of the column, where the radiation arrival time is evaluated either on-chip [24] or off-chip [25]. The largest GAPD array implemented so far with an event-driven readout mode consisted of 128 x 128 pixels [25]. Each pixel comprised a GAPD and a total of 7 transistors to perform the quenching and readout operations. The chip also included a bank of 32 TDCs to compute time-interval measurements and a high-speed digital readout circuit. One disadvantage of the event-driven readout architecture is that it introduces large dead times.

Finally, in the latchless pipelined readout each column is used as a timing-preserving delay line (Fig. 2.11-d). Each Geiger pulse is injected into the pipeline at a precise location that corresponds to the physical place where the pixel is situated. The row information is thus encoded in the timing of the pulse arrival at the end of the pipeline. It can be reconstructed by a single TDC at the bottom of the column. A GAPD array operated in the pipelined mode is described in [61]. In this design, each pixel consists of a GAPD, quenching mechanism, CMOS

inverter and electronics for the pipelined readout. Moreover, each pixel also has a gating mechanism that enables firing in a programmable time window to avoid time-domain aliasing.

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Chapter 3

Design and characterization of single pixels and small arrays in a HV-CMOS process

The selection of an appropriate technology is a decision of paramount importance when starting the development of any detector. In the particular case of GAPDs, the technology affects the sensitivity, noise and fill-factor of the device. In this thesis, two different technologies have been explored. On the one hand, the standard HV-AMS 0.35 μm CMOS technology because it provides a good trade-off between DCR and fill-factor. On the other hand, the Tezzaron 3D-IC based on the Global Foundries 130 nm CMOS technology to maximize the fill-factor of the detector.

In this chapter, the design and characterization of several single pixels and small arrays in the standard HV-AMS 0.35 μm CMOS technology (h35b4) will be discussed. All the designs include some elements at the readout circuit level to reduce the intrinsic noise generated by the sensor. The capabilities of both voltage-mode and current-mode readout circuits to operate the sensor at low reverse bias overvoltages, and thus reduce the DCR, have been investigated. Moreover, because at the future tracker detectors the event time is a parameter that can be known in advance, the detectors can be operated in a time-gated mode as an alternative to reduce the detected sensor noise without missing any real signal.

The design and characterization of a large array in the same technology will be introduced in Chapter 4. The design of a GAPD array in the Global Foundries 130 nm/Tezzaron 3D process will be presented in Chapter 5.

3.1 Single pixels with different voltage-mode readout circuits

It is well known that the time-gated operation is advantageous in terms of reducing the detected sensor noise. First, the afterpulsing probability can be completely suppressed at the expenses of leaving a long enough hold-off time between two consecutive measurements. Second, the probability to detect the dark counts can be linearly reduced as the gated-on period of the sensor is shortened. Moreover, it will be demonstrated in this chapter that the electrical crosstalk probability, typical of GAPD sensors that share the well, can be eliminated with short enough gated-on periods.

Apart from that, since the DCR depends on the reverse bias overvoltage of the sensor, low V_{OV} are desired to further reduce the noise. However, low avalanche voltages are not allowed in the HV-AMS 0.35 μm CMOS technology given that the threshold voltage of the nMOS transistors is set at 0.5 V. Three pixels that operate the sensor in the time-gated mode and can discriminate low avalanche voltages by using three different schemes have been explored. The design and characterization of the three pixels is described next.

3.1.1 Design

The generic schematic diagram of the GAPD pixel detectors is shown in Fig. 3.1, together with the electrical model of the sensor. In general terms, each pixel consists of a GAPD, active inhibition and active reset switches to perform the time-gated operation and a readout circuit for the detection of low avalanche voltages. Nevertheless, although the scheme adopted to discriminate the avalanche voltage (named 2G as 2-grounds, LS as level-shifter and TL as track-and-latch) is different in each pixel, the readout circuits share some features. They all include one voltage discriminator, a 1-bit memory cell and one pass-gate to activate the pixel readout. It can be said that the GAPD operates in passive quenching and active recharge. The transistor M_R was included to study the response of the detector for different recharge times, achieved through an externally adjustable V_{bias}, but it is not used in the time-gated operation. It could be removed to minimize the area occupation as well as the charge flowing during an avalanche.

3.1.1.1 Geiger-mode avalanche photodiodes in a 0.35 μm process and mode of operation

The photodiode is based on the structure proposed by Rochas in [1], which was briefly described in Chapter 2. In this structure, the photodiode is implemented by means of a p^+/deep n-tub junction on a p-substrate. The junction is surrounded by a low doped p-tub implantation to achieve a planar and uniform multiplication region, and hence avoid the premature edge breakdown of the device. Moreover, the corners of the sensor are round shaped to avoid electric field peaks. The active area of each sensor is 20 μm (width) x 100 μm (height). This size was chosen so as to satisfy the requirement on the single point resolution. The sensor width of 20 μm is more or less compliant with the demanded size of 17 μm; the radial direction is relaxed to a sensor height of 100 μm to keep the local confusion small at the forward disk of the tracking system (the final emplacement of the GAPD detector). The deep n-tub cathode is biased at a positive $V_{HV}=V_{BD}+V_{OV}$, being V_{BD} the breakdown voltage of the sensor and V_{OV} the reverse bias overvoltage to operate in Geiger-mode. The avalanches are sensed at the p^+ anode (named V_S, as sensing node) due to its lower intrinsic capacitance to ground, which is beneficial in

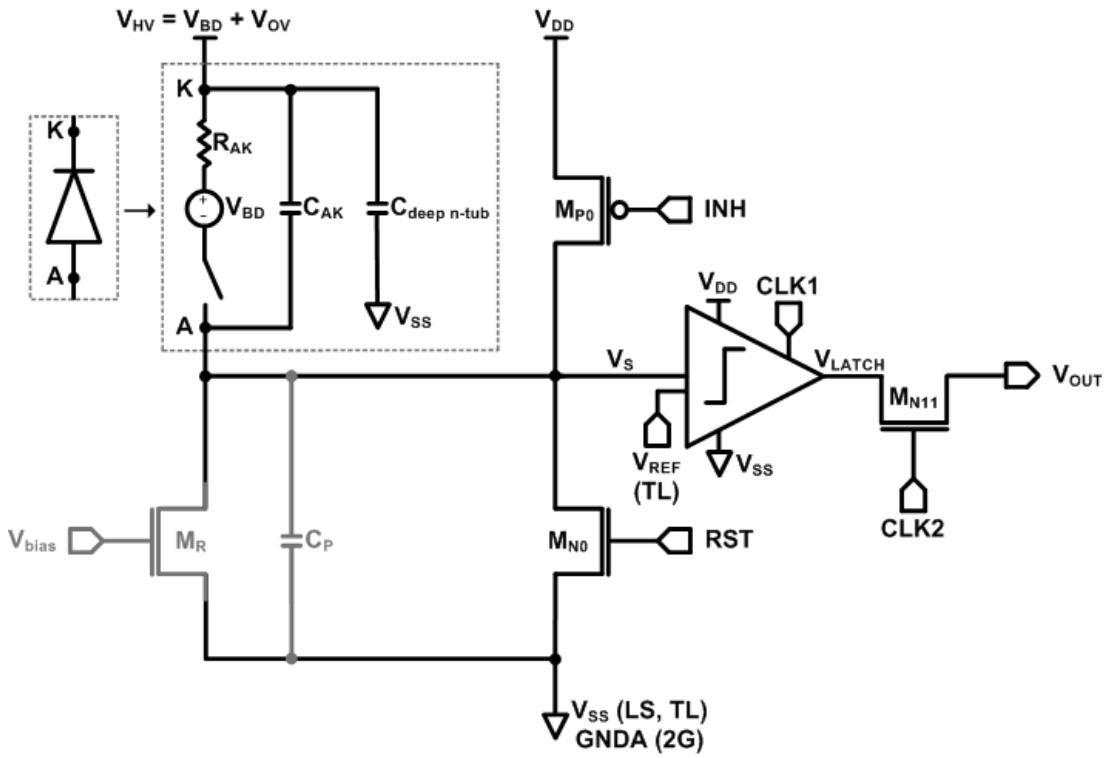

Figure 3.1 Generic schematic diagram of the GAPD pixel detectors. GNDA is the ground node of the sensor in the 2G scheme, whereas V_{SS} is used in the LS and TL schemes. V_{REF} is used in the TL scheme only.

reducing the timing response as well as the afterpulsing probability. The p-substrate is shared with the electronics and therefore connected to ground (V_{SS}). A cross-section of the GAPD device is depicted in Fig. 3.2.

The waveforms to operate the sensor in the time-gated mode together with the response of the device are depicted in Fig. 3.3. The time-gated operation is controlled by means of two external signals (RST and INH) implemented through MOS transistors (M_{N0}-M_{P0}). When the RST signal is set high (M_{N0} is 'on' while M_{P0} is 'off'), the sensor bias is quickly increased up to $V_{BD}+V_{OV}$. Hence, the sensor is recharged and the gated-on period is started. Given that avalanches can still occur while the sensor is in the recharge phase, the RST pulse has to be as short as possible in order to avoid low resistive paths quenching the avalanche. In these pixels, short RST pulses of 2 ns with a recharge transition of less than 1 ns have been used. In contrast, when the INH signal is set low (M_{P0} is 'on' while M_{N0} is 'off'), the polarization of the sensor is reduced to $V_{BD}+V_{OV}-V_{DD}$, with $V_{OV}<V_{DD}$ and V_{DD}=3.3 V in this technology. The sensor is then gated-off and it remains in this state until the next rising of the RST signal. When an avalanche is triggered, the self-sustained current that flows through the junction discharges the sensor capacitance (C_{AK}) and charges the parasitic capacitance (C_P) of the sensing node (V_S in Fig. 3.1). As a result, an analogue voltage pulse is generated in the V_S node in picoseconds. When

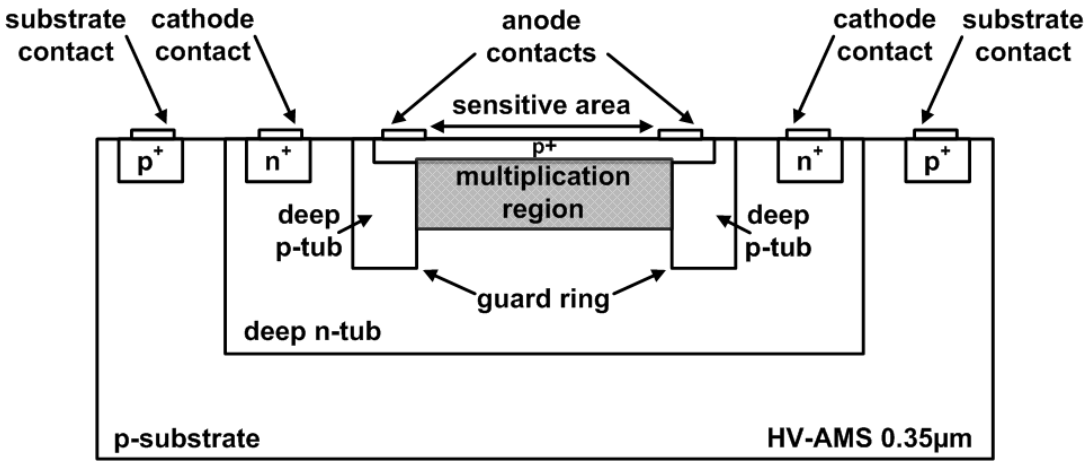

Figure 3.2 Cross-section of the GAPD designed and fabricated with the HV-AMS 0.35 µm CMOS technology. The cross-section is not to scale.

the voltage pulse reaches an amplitude equal to V_{OV}, the polarization of the sensor drops down to V_{BD} and the avalanche quenches. No additional components aimed to quench the avalanches have been included in order to minimize the electronics [2]. The sensing node is connected to the readout electronics, which converts the analogue voltage into a digital pulse. From Eq. 2.8 and Eq. 2.9, the sensor capacitance C_{AK} is calculated to be 540.19 fF at 1 V of overvoltage. The parasitic capacitance C_P is calculated to be between 10 fF and 30 fF for all the pixels proposed.

In all the readout circuits based on the voltage-mode approach, the 1-bit memory cell performs a 2-state operation that is made synchronous with the time-gated operation of the sensor. The first state occurs while the GAPD is gated-on and the memory cell samples the output of the sensor. The duration of the sampling mode is called period of observation or t_{obs}. In contrast, the second state takes place while the sensor is gated-off and the memory cell is latched. The operation of this memory cell is controlled by means of an external signal (CLK1), which has been implemented through a MOS transistor. Because avalanches can still happen during the sensor recharge, the RST and CLK1 signals are set high simultaneously. However, the CLK1 signal is set low one clock pulse before the falling edge of the INH signal so as to avoid storing a false '1'. Moreover, all the pixels use a simple address circuit based on a pass-gate (M_{N11}) activated by an external signal (CLK2) to control the readout of the pixel. When the CLK2 signal is set high, the pixel feeds its corresponding output pad and the readout is completed. A detailed description of each one of the three readout circuits is provided next.

3.1.1.2 2-grounds

In a first approach named 2G (Fig. 3.4-a), a simple and fast CMOS inverter (M_{P1}-M_{N1}) is used as a discriminator to detect the avalanche voltage V_{OV}. To achieve a better immunity to

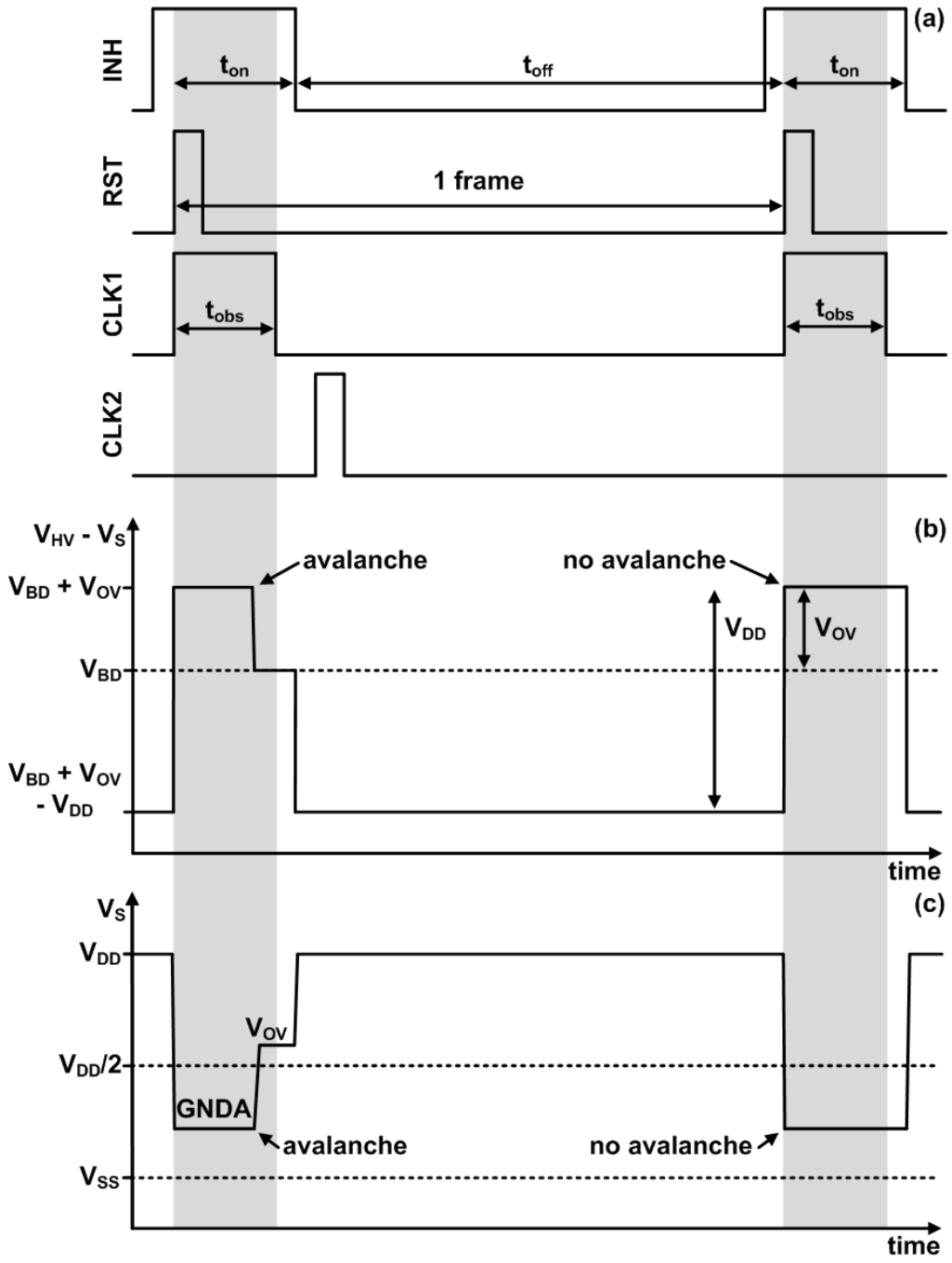

Figure 3.3 Timing diagram of the waveforms to operate the time-gated GAPD pixel detector (a), GAPD bias (b) and response of the sensing node in the 2G scheme (c).

external noise, the inverter is designed to have a threshold voltage of $V_{DD}/2$. Nevertheless, a low V_{OV} below $V_{DD}/2$ is desired to reduce the sensor DCR, as previously stated. As a solution to this problem, a 2-grounds scheme (GNDA for the sensor and V_{SS} for the readout) has been implemented in this strategy. Biasing, for example, GNDA to 1 V (and therefore increasing V_{HV} to V_{BD}+V_{OV}+GNDA), low V_{OV} from 0.65 V can be easily detected and digitized by the CMOS inverter. The output of the inverter (V_{INV}) feeds the 1-bit memory cell based on a dynamic latch (M_{N2}-M_{P2}-M_{N3}), the operation of which is controlled by means of the external signal CLK1

(M_{N2}). The CLK1 signal is set high (M_{N2} is 'on') at the same time that the sensor is activated. When the CLK1 signal is set low at the end of the t_{obs} period, the last value of the V_{INV} node is stored in the V_{LATCH} node ('0' for no avalanche, '1' for avalanche) during the gated-off period.

3.1.1.3 Level-shifter

In a second proposed circuit that makes use of one ground only (V_{SS}, biased at 0 V), low V_{OV} operation is possible thanks to a level-shifter (named LS in Fig. 3.4-b) externally biased by means of an R_{bias} input (M_{P3}-M_{P4}-M_{P5}). The level-shifter rises the voltage at the diode output so that V_{OV} is higher than the threshold voltage of the following CMOS inverter (M_{P6}-M_{N4}), which is also set at $V_{DD}/2$. Like in the two grounds scheme, a dynamic latch (M_{N5}-M_{P7}-M_{N6}) functions as a 1-bit memory cell.

3.1.1.4 Track-and-latch comparator

In the last case, the sensing and storage components have been integrated by means of a sole circuit, a track-and-latch comparator (named TL in Fig. 3.4-c) [3]. This circuit consists of a pMOS controlled source (M_{P8}), a pMOS differential pair (M_{P9}-M_{P10}), two cross-coupled inverters in positive feedback configuration (M_{P11}-M_{N8}, M_{P12}-M_{N9}) and two nMOS transistors (M_{N7}-M_{N10}). Compared with traditional two-stage comparators, in this design there is no need for a pre-amplifier stage, since the avalanche detection is done by the differential pair. In this case, the threshold voltage of the MOS transistors is not a limitation because the input differential pair is implemented with pMOS transistors.

The operation of the track-and-latch comparator can be described as follows. During the so-called track phase, which is coincident with the t_{obs} period, the CLK1 external signal is set high and the transistors M_{P9} and M_{P10} sample the two input nodes. These nodes correspond to the sensing node (V_S) and a reference voltage (V_{REF}). The channel current of the transistors M_{P9} and M_{P10} is modulated in function of the values of V_S and V_{REF}, respectively. However, the nodes V_{out+} and V_{out-} are shorted to ground (V_{SS}) through the transistors M_{N7} and M_{N10}. Consequently, the charge injected by the transistors M_{P9} and M_{P10} remains accumulated at their drain nodes. In contrast, during the latch phase, the CLK1 signal is set low, the transistors M_{N7} and M_{N10} are turned 'off' and they no longer connect V_{out+} and V_{out-} to ground. If there has been an avalanche, the charge accumulated at the drain node of the transistor M_{P10} is higher than that of the transistor M_{P9}. Thus, the metastable voltage generated at the V_{out+} node will be higher than that at the V_{out-} node and the transistor M_{N8} will drive more current than the transistor M_{N9}. Consequently, the

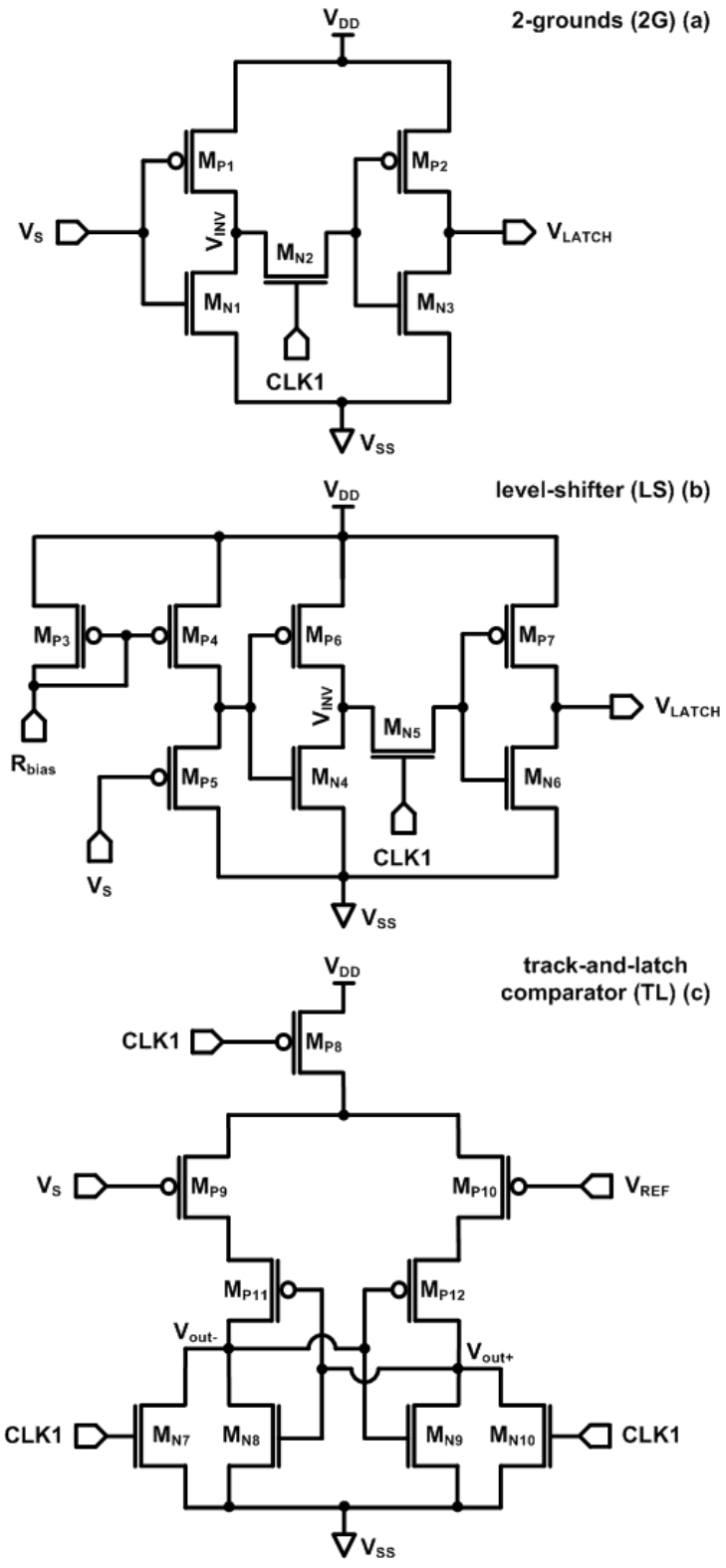

Figure 3.4 Schematic diagram of the voltage-mode readout schemes: 2-grounds (a), level- shifter (b) and track-and-latch comparator (c). In (c), the V_{out+} and $V_{out\_}$ nodes are connected to the output buffer, whose output node is V_{latch}.

V_{out+} node will store a logic '1', whereas the V_{out-} node will store a logic '0' due to the positive feedback. The opposite values are generated if no avalanche has been detected [4]. The V_{out+} and

V_{out-} nodes are connected to an output buffer to achieve a more robust circuit.

Nevertheless, the design of the track-and-latch comparator deserves special attention. Since the operation mode of the circuit is based on the channel current difference that flows through M_{P9} and M_{P10}, the (W/L) ratios of these transistors have to be optimized so that the cross-coupled inverters enter the saturation mode for a small difference between V_S and V_{REF}. For instance, if the (W/L) ratios of M_{P9} and M_{P10} are too large, the latch circuit will not be able to manage the generated currents and the comparator will always be stuck at the same state [5].

3.1.2 Characterization

The chip containing the pixel detectors described in this section was submitted for fabrication through a MPW run organized by Europractice on 26th April 2010. A micrograph of the pixel detectors fabricated with the standard HV-AMS 0.35 μm CMOS technology is presented in Fig. 3.5. The main target of fabricating these pixels was to study the efficiency of the proposed methods (i.e. time-gated operation and low V_{OV}) in terms of noise reduction. In first approximation, the afterpulsing probability and the DCR were extensively characterized. Pixels from different sample chips were also tested to analyze chip-to-chip variations. Finally, the features of the different readout circuits were compared.

To start with, the current-voltage curve of the sensor was characterized to obtain the breakdown voltage. This experiment was conducted with a test GAPD accessible to the sensing node that was included in the same chip. A 4-wire method implemented by means of a Keithley 2611A source directly connected to the terminals of the sensor was used to apply a reverse bias voltage while measuring the current generated by the GAPD. Well below V_{BD}, the current that flows through the GAPD is in the nA range. However, as the breakdown region is reached, the current increases sharply up to the tenth part of the mA. This experiment revealed that at room temperature V_{BD} of the GAPD is set at 18.72 V with light and at 18.94 V in darkness, as it can be observed in Fig. 3.6.

To characterize the afterpulsing probability and the DCR, the fabricated chip was mounted on a printed circuit board and powered with an Agilent E3631A voltage source. A control board based on an ALTERA Stratix II FPGA was used to generate the control signals (RST, INH, CLK1 and CLK2) that are necessary to operate and read out the pixels. The FPGA was also used to count off-chip the number of pulses generated by the detectors and to manage the communication with a computer via a USB. The computer controlled the experimental set-up with the support of a dedicated software. The sensor characterization was done with a programmable total measuring time (t_m) that depends on the t_{obs} period and the number of times

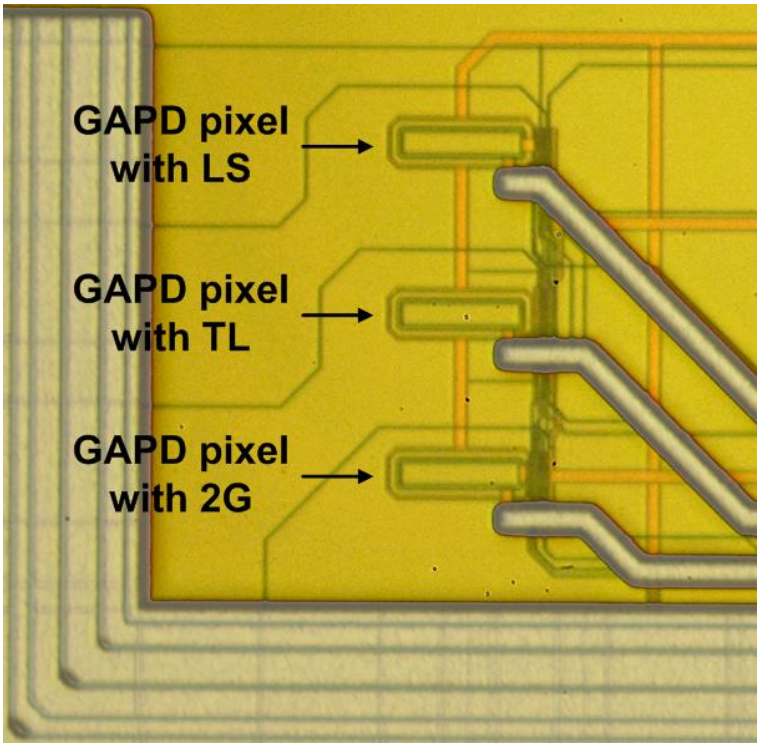

Figure 3.5 Micrograph of the fabricated voltage-mode pixel detectors.

that t_{obs} is repeated. In this particular characterization, different t_{obs} periods that range from 10 ns to 1280 ns were analyzed. The number of repetitions (n_{rep}) was set at 10^5 times to obtain significant statistics. For each t_{obs}, the total measuring time is given by

$$t_m = t_{obs} \cdot n_{rep} . \tag{3.1}$$

The NCR (Noise Count Rate) of the detector, a parameter that includes dark counts and afterpulses (and also crosstalks in the case of arrays), can be obtained from the expression

$$NCR = \frac{noise\ counts}{t_m} \tag{3.2}$$

where the number of noise counts is given directly by the FPGA. As it will be demonstrated, one of the advantages of time-gating the GAPD is that it is possible to completely suppress the afterpulsing probability by leaving long enough gated-off periods. Therefore, the DCR of the sensor can be measured separately from the afterpulses. The DCR can be obtained from the expression

$$DCR = \frac{dark\ counts}{t_m} . \tag{3.3}$$

The experimental analysis was repeated for different V_{OV} of 0.5 V, 1 V and 1.5 V.

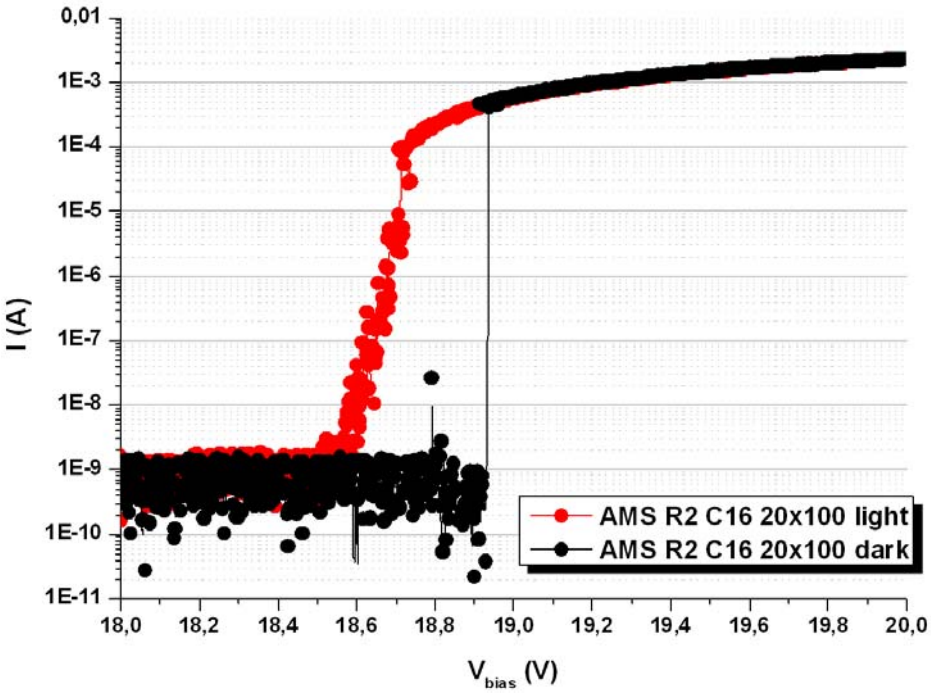

Figure 3.6 I-V curve of the Geiger-mode with and without light.

The afterpulsing probability was tested by leaving different gated-off periods for a fixed t_{obs} of 10 ns. This measurement was done with the 2-grounds pixel detector from sample chip number 1 in darkness and at room temperature. Two different experimental methods were employed. In the first case, the infinite permanence option of a MSO7104A Agilent oscilloscope was used to obtain a qualitative result. In the second case, the NCR for each measured t_{off} was provided directly by the FPGA.

The oscilloscope images with time/voltage information extracted from the analysis with the infinite permanence option are shown in Fig. 3.7. In these figures, the trigger of the oscilloscope was activated by edge, and thus the noise counts originate from the same instant of time. The reverse bias overvoltage applied to the pixel detector was 1 V. In Fig. 3.7-a the gated-off period of the sensor is 80 ns, whereas in Fig. 3.7-b it is 300 ns. Because the detector is in darkness, the first pulse (in blue) in both images corresponds to a dark count. In Fig. 3.7-a, there is a clear presence of several secondary pulses after the primary pulse. The secondary pulses correspond to afterpulses. In contrast, in Fig. 3.7-b the primary pulse is free of secondary pulses, i.e. afterpulses. In Fig. 3.7-a, the pulses that are far beyond the primary and secondary pulses correspond to new dark counts. New dark counts are not observed in Fig. 3.7-b given the shorter number of repetitions (because of the longer t_{off}) that are represented in this image.

The data obtained from the analysis with the FPGA is shown in Fig. 3.8, where the NCR has been obtained from Eq. 3.2. Here, different reverse bias overvoltages of 0.5 V, 1 V and 1.5 V were used. For all the V_{OV} measured, the NCR presents a constant value for long enough t_{off}

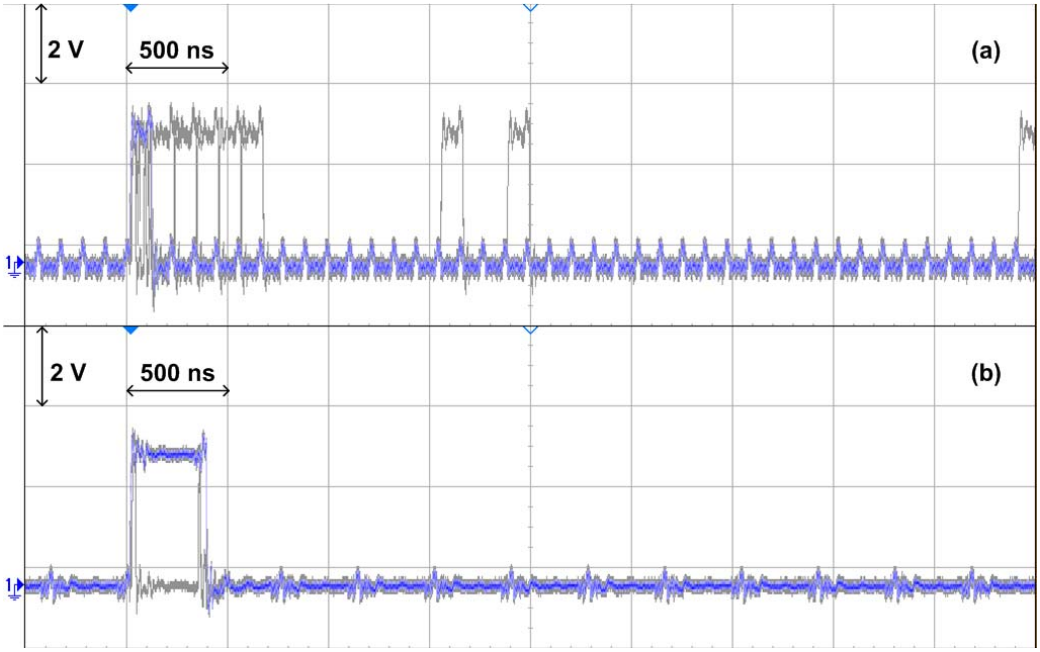

Figure 3.7 Presence of afterpulses with a t_{off} of 80 ns (a) and elimination of afterpulses with a t_{off} of 300 ns (b). Measured with the infinite permanence option of the oscilloscope.

durations, as it can be observed in Fig. 3.8. In contrast, for t_{off} periods starting around 500 ns, the NCR increases as t_{off} is reduced. This is a clear sign of afterpulsing. It indicates that the trapped carriers have not been completely released during the gated-off time and therefore contribute to the GAPD ignitions. For instance, a t_{off} of 500 ns yields an afterpulsing probability lower than 1% for all the V_{OV} measured. However, for a t_{off} of 50 ns this probability rises up to 30%, 52% and 69% when V_{OV} is 0.5 V, 1 V and 1.5 V, respectively. The increase of the afterpulsing probability with V_{OV} is due to the increase of the avalanche breakdown probability with higher overvoltages.

After that, the DCR of the three pixel detectors (2G, LS and TL) was measured with a fixed t_{off} of 500 ns and different t_{obs} that range from 10 ns to 1280 ns. Chip-to-chip variations were also investigated by testing pixel detectors from two different sample chips. Again, these measurements were done in darkness and at room temperature. The results plotted in Fig. 3.9 show that the DCR is constant despite the value of t_{obs}, as it should be. Moreover, the DCR is lower as V_{OV} is decreased (see 2G pixel detector from chip 1 at 0.5 V, 1 V and 1.5 V of V_{OV}). In the same figure, it can also be observed that for a fixed V_{OV} there exist large variations amongst the DCR of different pixels, either from the same sample chip (2G, LS and TL pixel detectors from chip 1 at 0.5 V of V_{OV}) or a different one (2G pixel detector from chips 1 and 5 at 0.5 V of V_{OV}). Because these variations are so large, they cannot be related to the readout circuit. Instead, they are a consequence of the extreme sensitivity of GAPDs to punctual defects in the crystal lattice of silicon [6].

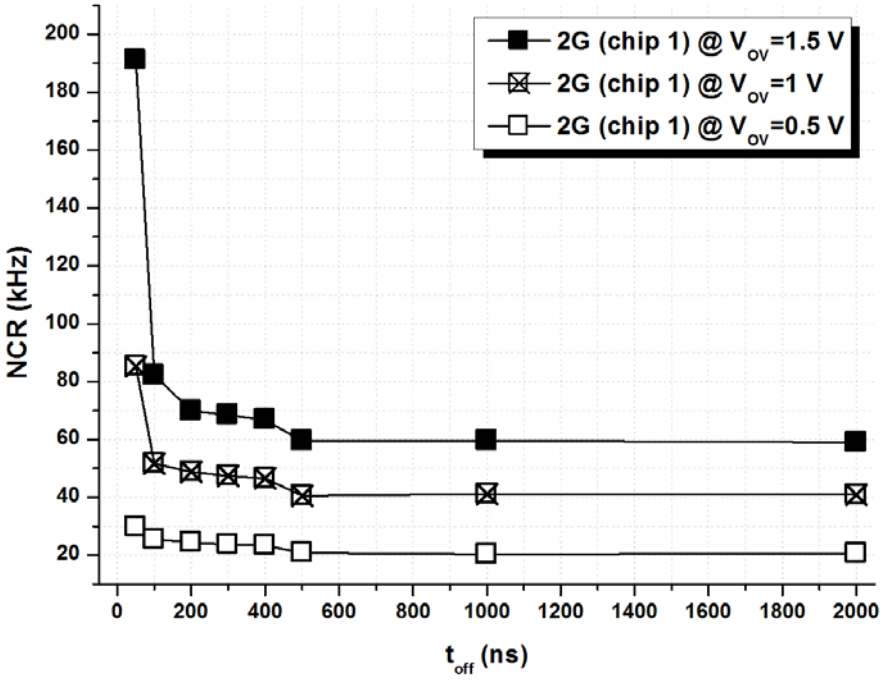

Figure 3.8 Presence of afterpulses for different t_{off} and V_{OV}.

The DCR of approximately 40 kHz at 1 V is high when compared to the literature, where typically lower DCRs obtained with smaller GAPDs are reported. Although the DCR increases with the sensor area, large GAPDs were chosen in this work to meet the required geometry for the detector and also increase the fill-factor. Then, as a solution to the high DCR, the detector is operated in a time-gated mode, where the probability to detect one dark count within a given frame (i.e. n_{rep}=1) is reduced linearly as t_{obs} is shortened. The DCP (Dark Count Probability), the parameter that accounts for this phenomenon, can be expressed as

$$DCP = DCR \cdot t_{obs}. \tag{3.4}$$

Thus, with a DCR of 40 kHz, the DCP can be reduced from 10^{-2} to 10^{-4} when the sensor t_{obs} is shortened from 1280 ns to 10 ns. This situation can be advantageous for triggered imaging systems, such as tracker detectors, where the expected signal time of arrival can be known in advance and therefore the detector can be operated in a time-gated mode without losing any useful input signal. As it will be demonstrated in Chapter 4, the utilization of this technique results in an extension of the DR (Dynamic Range) [7] and the resolution of the recorded images [8].

All the proposed readout circuits have demonstrated their capability of working with low V_{OV}, which as shown reduces the DCR. However, each circuit has its own advantages and limitations. The 2-grounds scheme, for instance, uses two ground voltages. The bulk node of the transistor M_{N0} (RST) is connected to GNDA and not to V_{SS}, which induces the apparition of the substrate effect. Triple well transistors were discarded due to their high area occupation. In

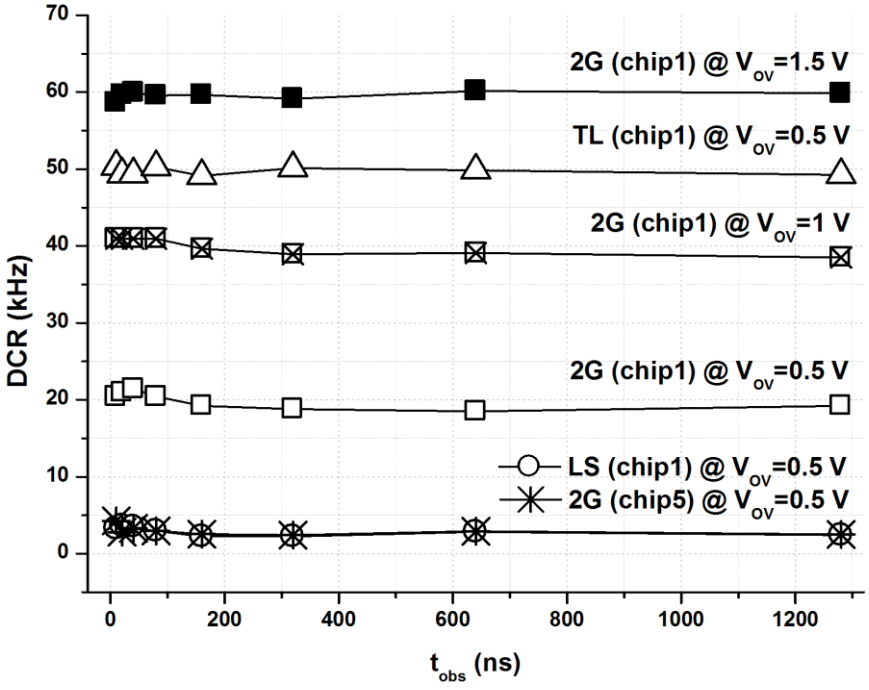

Figure 3.9 DCR of the different GAPD pixels for different t_{obs} and V_{OV}.

contrast, the level-shifter and the track-and-latch comparator use one ground only, but they need a higher number of transistors. Moreover, both circuits require one additional input, the external bias for the level-shifter and the reference voltage for the track-and-latch comparator. Nevertheless, the track-and-latch comparator offers the advantages of integrating the sensing and storage components within the same circuit and a higher readout speed when compared to the other proposed readout circuits. We can conclude that there is no circuit whose performance is exceptionally better than the other ones.

When referred to time-gated pixels with low overvoltage operation, two trade-offs may come up for discussion. On the one hand, long gated-off periods may reduce the maximum admissible radiation counting rate. However, the proposed GAPD pixels are aimed to triggered detectors and the gated-on periods of the sensor can be made coincident with the expected signal time of arrival. On the other hand, the utilization of low overvoltages can certainly help to reduce the DCR. However, the detecting capabilities of the sensor are not severely reduced, as it could be expected. A reverse bias overvoltage of 1 V has been demonstrated to be good enough to detect the impinging radiation [9].

3.2 Single pixel with a current-mode readout circuit

The most part of the readout circuits that can be found in the literature are based on the voltage-mode approach, i.e. they sense the voltage drop or increase that results from the

triggering of an avalanche. However, it is also possible to use a readout circuit based on the current-mode approach, which takes advantage of the GAPD current flow being the electrical parameter modified upon an avalanche [10]. Based on this topology, a GAPD pixel has been designed and characterized.

3.2.1 Design

A schematic diagram of the GAPD pixel with the current-mode readout circuit is depicted in Fig. 3.10. The pixel consists of a GAPD, an active reset switch to recharge the sensor and a readout circuit that is sensitive to the avalanche current. The photodiode has a sensitive area of 20 μm (width) x 100 μm (height). It is based on the same structure described in section 3.1.1.1, and therefore it will not be further commented. The readout circuit copies the current generated by the sensor while providing isolation between the sensor and the detection electronics (an inverter in this case). This circuit allows to sense avalanches at very low reverse overvoltages, which has a beneficial impact on the range of light intensity that can be detected by the sensor (i.e. the dynamic range). The principle of operation of the readout circuit is explained in detail in the following lines.

Prior to any new observation, the RST signal is momentarily set high (M_{N0} and M_{N3} are 'on') so as to respectively recharge the sensor to its operating bias and pre-charge the V_{PRE} node. Because M_{N3} is an nMOS transistor, the V_{PRE} node will never be pre-charged to 3.3 V, but to 2.7 V to speed up the avalanche detection process. In quiescence conditions, V_S is set to ground, the transistors M_{N1} and M_{N4} are in the cut-off region, and V_{PRE} is set to 2.7 V. As a consequence, the output of the pixel is low, i.e. a logical '0'. To bias M_{N2} and M_{N5}, one would expect transistor M_{N2} to be arranged as a resistance, like in a cascode current mirror. However, the current that flows from M_{N1} to M_{N2} is so low, that if the resistance topology was used for M_{N2}, the transistors M_{N2} and M_{N5} would never be switched on. Instead, an analogue signal V_N (typically set at 2.7 V) is used to bias M_{N2} and M_{N3}. When an avalanche is triggered, the current that flows through the sensor rapidly turns on M_{N1} and M_{N4} (i.e. the current that flows through the sensor is copied), which are in a current mirror configuration. As a result, the V_{PRE} node is discharged. This situation is detected by the chain of inverters that act as buffers and the output voltage swiftly switches to a logical '1'. Like in the voltage-mode readout circuits, no additional components aimed to quench the avalanches have been included in this design. The avalanche auto-quenches when the voltage of the V_S node reaches the reverse bias overvoltage (i.e. V_{OV}). A timing diagram of a 3-frames measurement is depicted in Fig. 3.11.

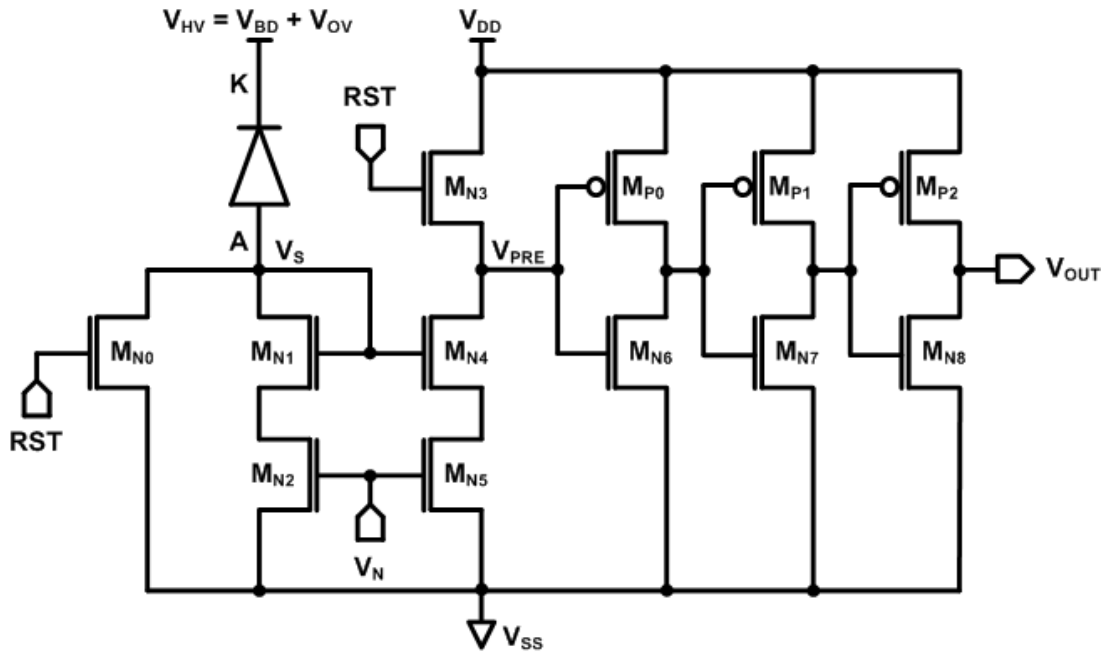

Figure 3.10 Schematic diagram of the current-mode readout circuit.

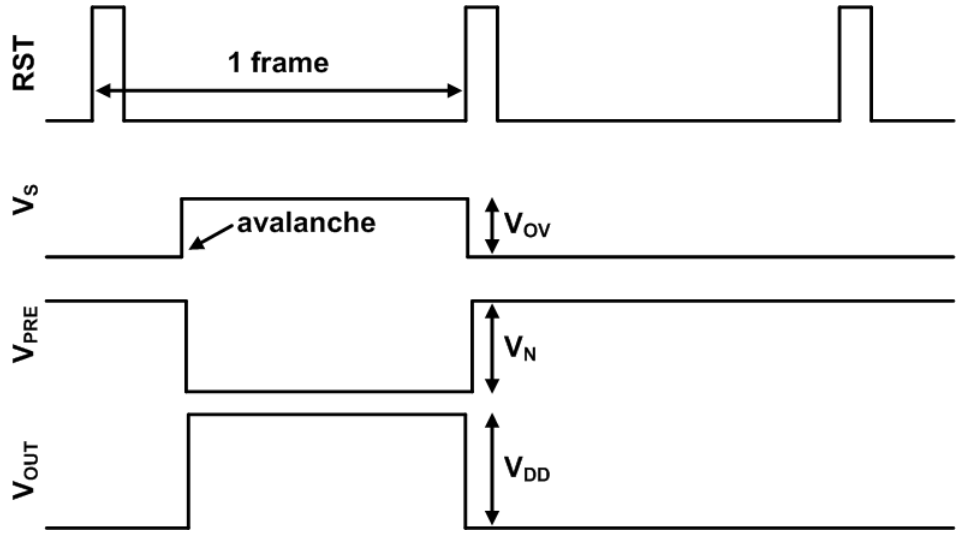

Figure 3.11 Timing diagram of a 3-frames measurement using typical configuration parameters.

3.2.2 Characterization

A micrograph of the current-mode pixel detector fabricated with the standard HV-AMS 0.35 µm CMOS technology is presented in Fig. 3.12. This pixel was submitted for fabrication in the same run as the voltage-mode pixels. The set-up used for the characterization of the current-mode pixel is also the same as that one used for the voltage-mode pixels.

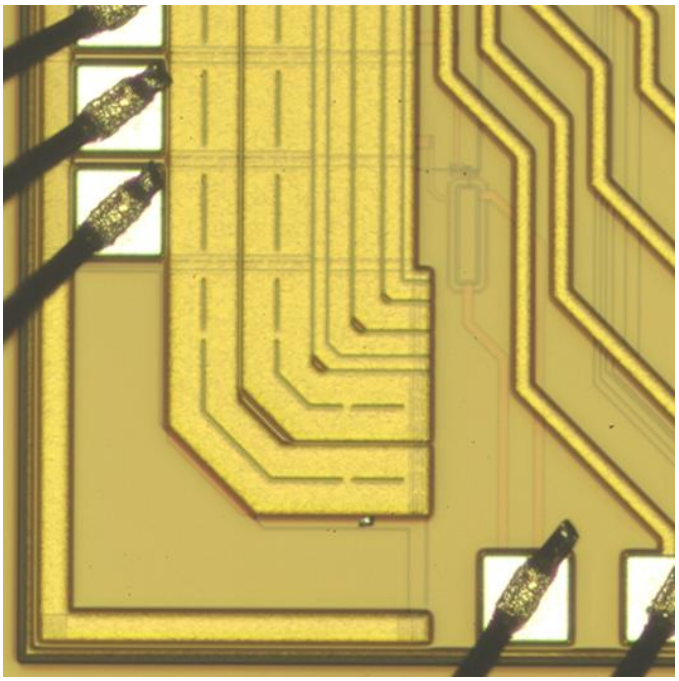

Figure 3.12 Micrograph of the fabricated current-mode pixel detector.

Because the current generated by the GAPD during an avalanche is macroscopic regardless of V_{OV}, the current-mode pixel can detect signal at very low overvoltages of a few mV and therefore with an extremely reduced sensor noise. To investigate this feature, the optical response of the pixel to a variable intensity of a 645 nm light was tested. A red LED was placed 0.5 cm above the GAPD and powered by an HP 3245A universal source. The current flowing through the light emitter was measured by means of an HP 3458A multimeter. The chip, together with the FPGA and the red LED, was placed inside a metallic box to protect the circuit from electromagnetic interferences and uncontrolled light sources.

The response to light of the current-mode pixel was tested for several reverse bias voltages (i.e. V_{HV}) ranging from 18.6 V to 20 V, in steps of 10 mV. For each V_{HV}, the detector was illuminated with different light intensities comprised between 10 μA and 5 mA and its response was observed 10^5 times. A counter with a maximum capacity of 10^5 counts was arranged in the FPGA to count the generated pulses. The experimental data are plotted in Fig. 3.13, where the number of counts has been depicted as a function of V_{HV} in the dark and also for different LED intensities (I_{LED} in Fig. 3.13). From this figure, several observations can be made. To start with, the minimum V_{HV} to detect the pulses generated by the sensor decreases with higher light intensities. Thus, the minimum V_{HV} to observe counts in darkness is 18.97 V, whereas for an I_{LED} of 5 mA the minimum V_{HV} is 18.80 V. This result is in good agreement with the measured I-V curve of the sensor (see Fig. 3.6). Second, in light conditions, the measured counts increase sharply for a short V_{HV} range of less than 200 mV between 18.80 V and 19.90 V. Because the increase of the measured counts is so sharp, they cannot be induced by the sensor noise, but to

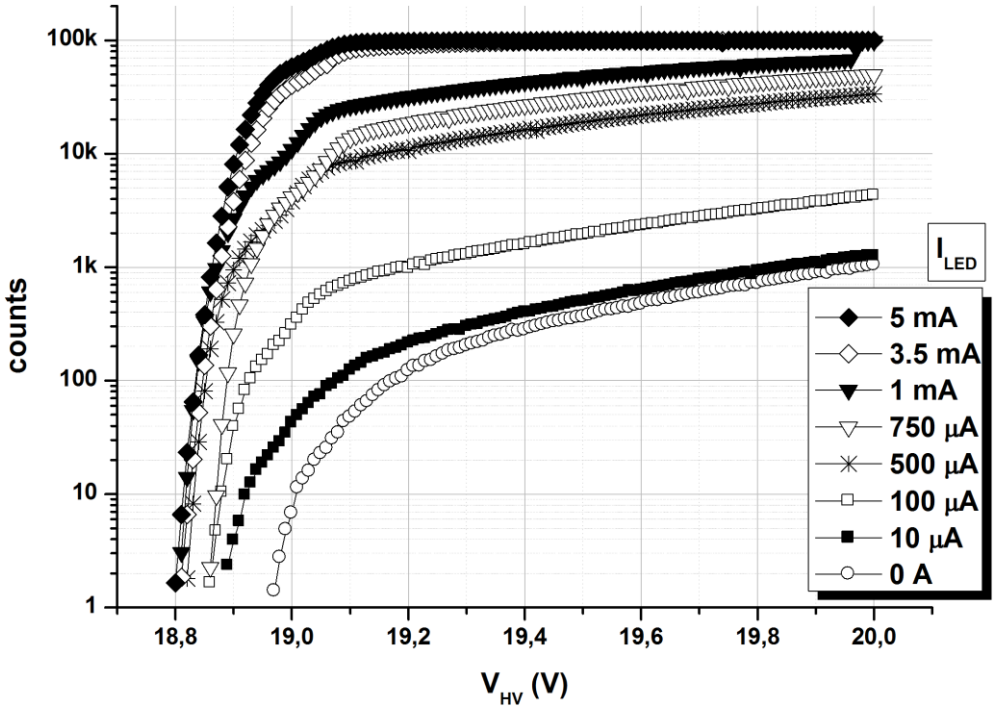

Figure 3.13 Measured counts as a function of V_{HV} for different light intensities.

the detected signal. Therefore, signal counts can be appreciated with low reverse bias overvoltages starting at some ten mV above V_{BD}, which is measured to be around 18.72 V with light. Moreover, at low V_{HV} below 19 V and for the measured I_{LED}, the detector never saturates (i.e. the generated counts are less than the maximum capacity of the counter). As a consequence, it is possible to observe a wider range of signal intensities. It is concluded that the current-mode pixel is useful especially in the detection of faint signal at low reverse bias voltages.

3.3 Array of 3 x 3 pixels

This detector consists of an array of 3 rows per 3 columns of GAPD pixels. Each pixel combines a GAPD, active inhibition and active reset switches to perform the time-gated operation and a readout circuit based on the level-shifter, as described in section 3.1. A schematic block diagram of the 3 x 3 GAPD array together with the testing board used in the experimental set-up is depicted in Fig. 3.14.

3.3.1 Design

With the purpose of increasing the fill-factor of the matrix, all the GAPDs of rows 0 and 1 and all the GAPDs of row 2 share a common deep n-tub, thus generating two macro-pixels of 6 and 3 GAPDS, respectively. Nevertheless, the introduction of the p-tub implantation (see Fig.

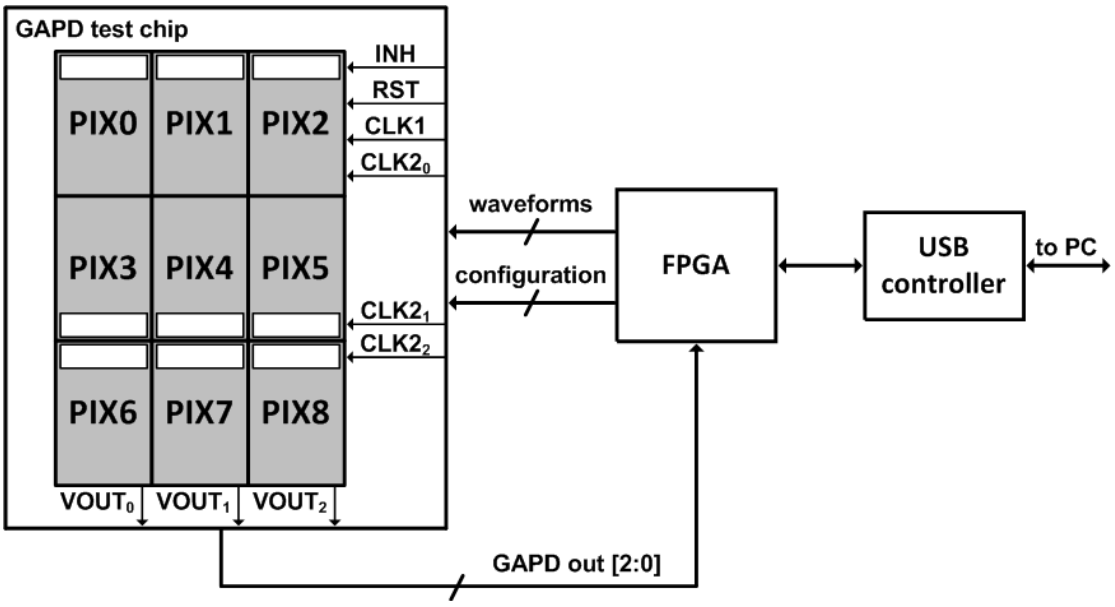

Figure 3.14 Schematic block diagram of the 3 x 3 GAPD array together with the testing board.

3.2) generates a minimum separation between two neighboring GAPDs of 1.7 µm (width). The in-pixel readout electronics are placed on top of each pixel (or at the bottom in case of row 1). As a result, the detector features a pixel pitch of 22.9 µm (width) and 105.6 µm (height, including the readout electronics), and an optical fill-factor of 54.4%.

The three rows of the GAPD array are sequentially read out row by row during the gated-off periods of the sensor. Thereby, the three columns of each row are read out in parallel, requiring only three output pads. The pass-gate M_{N14} is controlled by means of the external signal $CLK2_m$, with m=[0, 2]. When the $CLK2_m$ signal is set high, the corresponding row of the detector is activated, thus feeding the three output column lines that are directly connected to the three output pads. Multiplexers or selection decoders are not used in this configuration. Despite the small number of pixels, the presented array is a demonstrator of a larger bidimensional camera.

3.3.2 Characterization

The 3 x 3 GAPD pixel detector was fabricated together with the single pixels described in the previous sections. A micrograph of the fabricated prototype can be seen in Fig. 3.15. The DCR of this detector was characterized in darkness with the same test set-up described in the previous section. The noise counts generated with different t_{obs} that range from 10 ns to 1280 ns were analyzed for different V_{OV} of 0.5 V, 1 V and 1.5 V. The number of repetitions was set at $4 \cdot 10^5$.

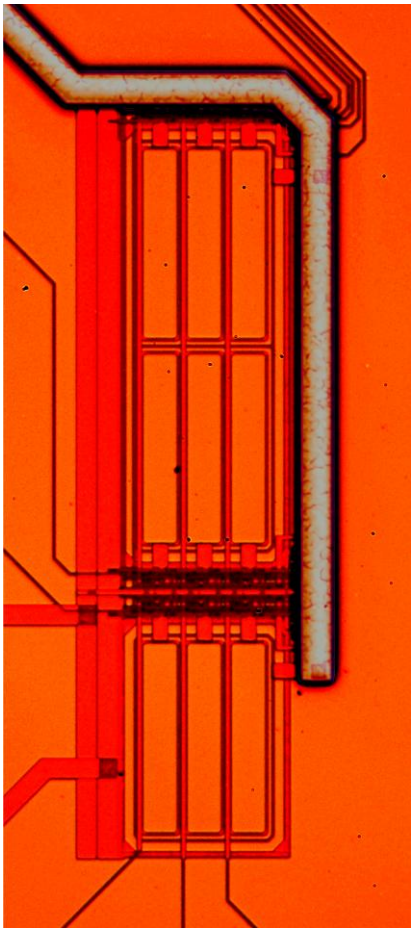

Figure 3.15 Micrograph of the fabricated 3 x 3 GAPD array.

Fig. 3.16 plots the generated noise counts as a function of the t_{obs} period for the specified number of repetitions. As expected, the dark counts are reduced for a lower V_{OV} (see PIX0 at 0.5 V, 1 V and 1.5 V of V_{OV}). Moreover, the dark counts are linearly decreased with shorter t_{obs}, as it can be inferred from Eq. 3.3. It can also be observed that noise discrepancies amongst the pixels of the array are large (more than a factor 20 between the most and the less noisy ones), as it usually happens in GAPD arrays.

3.4 Array of 1 x 5 pixels

This detector consists of a linear array of 5 GAPD pixels. Each pixel combines a GAPD, active inhibition and active reset switches to perform the time-gated operation and a readout circuit based on the 2-grounds scheme, as described in section 3.1. However, this array was produced during a MPW run that took place after the one mentioned above (specifically, on 26th April 2011), and therefore the transistor M_R (see Fig. 3.1) was eliminated. All the GAPDs share a common deep n-tub, generating a macro-pixel of 5 GAPDs. Like in the case of the 3 x 3 GAPD array, the introduction of the p-tub implantation generates a minimum separation

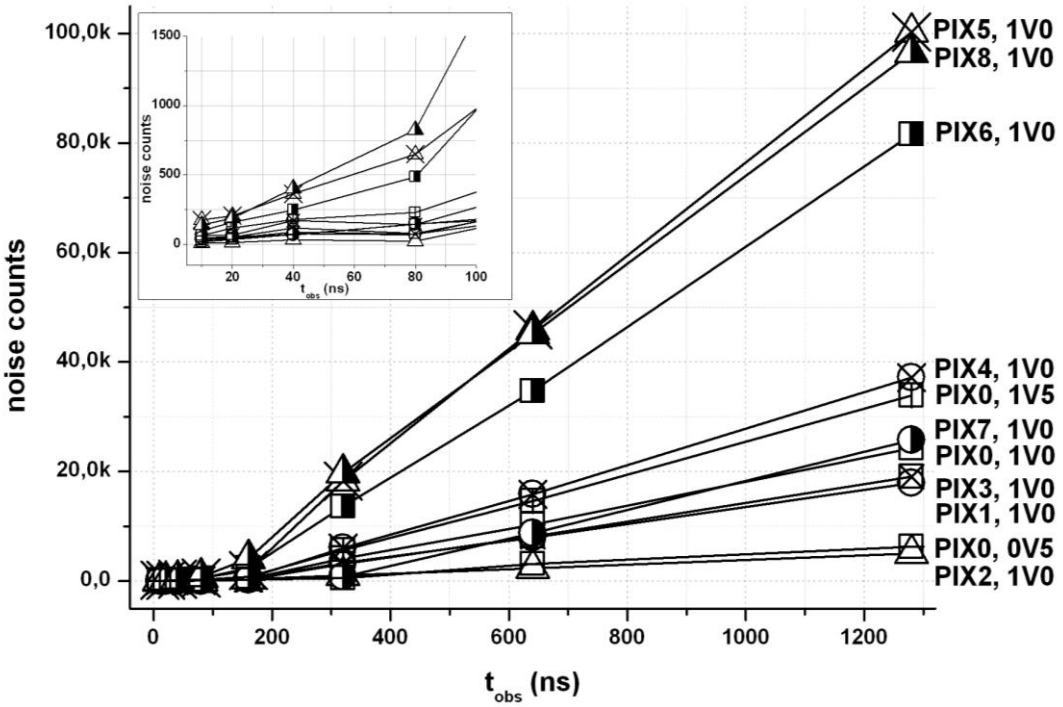

Figure 3.16 Noise counts of the different pixels of the array for different t_{obs} and V_{OV}.

between two neighboring GAPDs of 1.7 μm (width). A cross-section of the GAPD macro-pixel is depicted in Fig. 3.17. The in-pixel readout electronics are placed on top of each pixel. This array was used to characterize the electrical crosstalk effects as a function of the gated-on period in a time-gated array of GAPDs.

3.4.1 Crosstalk in time-gated GAPD arrays that share the well

When an avalanche is triggered in a GAPD, a large quantity of electrons and holes is generated in the multiplication region. These charge carriers are accelerated by the high electric field of the depletion region (10^6 V/cm), but they also diffuse in all directions even more intensely given the limited volume where the charge carrier generation takes place. In particular, drift-diffusion simulation of the sensor structure by ISE-TCAD indicates that more than $1 \cdot 10^{13}$ holes/cm^3 reach the neutral n-zone 1 ns after the avalanche itself. In this region, the holes are minority and they start to recombine at a rate given by their lifetime. However, the diffusion is still so strong that it dominates the holes movement in such a way that some of them can reach the neighboring active region (placed in the same well), drift towards its p^+-region and trigger a new avalanche breakdown ascribable to electrical crosstalk.

From the theoretical point of view, the holes diffusion along the neutral n-region involves high concentrations that question the analogy with the material transfer in a solution or heat

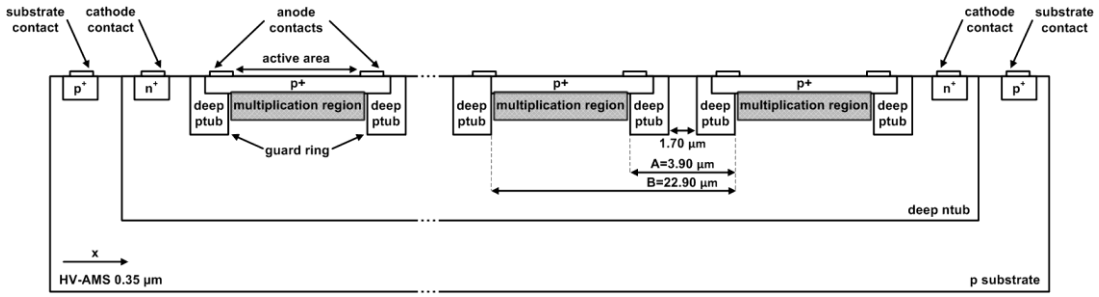

Figure 3.17 Cross-section of the GAPD macro-pixel designed and fabricated with the HV-AMS 0.35 µm CMOS technology. The cross-section is not to scale.

transfer by conduction, which is the basis of the Fick's theory. However, as a first approximation to the problem, the transfer of particles per unit area in a one-dimensional flow can be described by the Fick's first law

$$J = -D\frac{\partial C(x,t)}{\partial x} \tag{3.5}$$

where J is the particle flow per unit time and unit area, D the diffusion coefficient and C the particle concentration, which depends on the position (x) and the time (t). The combination of the previous law with the law of the conservation of the matter

$$\frac{\partial C(x,t)}{\partial t} = -\frac{\partial J(x,t)}{\partial x} \tag{3.6}$$

gives the known Fick's second law for diffusion

$$\frac{\partial C(x,t)}{\partial t} = \frac{\partial}{\partial x}\left[D\frac{\partial C(x,t)}{\partial x} \right]. \tag{3.7}$$

The resolution of this equation needs careful description of the initial and boundary conditions. In our study we will neglect diffusion through the depletion region. We will consider the initial conditions x=t=0 when carriers reach the neutral n-region. A large quantity of particles appear suddenly in the depletion limit, with a fixed amount of holes S per unit area, before they diffuse. Mathematically, this initial holes distribution corresponds to the delta function. Consequently, in this approximation, the initial and contour conditions can be written as

$$C(x,0) = S\delta(x) \tag{3.8}$$

$$\int_0^\infty C(x,t)dx = S \tag{3.9}$$

$$C(x,\infty) = 0\,. \tag{3.10}$$

The solution of the Fick's second law with these conditions is the Gaussian

$$C(x,t) = \frac{S}{\sqrt{\pi D t}} \exp\left(-\frac{x^2}{4Dt}\right). \tag{3.11}$$

The value of S can be estimated as the product of the holes concentration arriving to the neutral n-zone ($1\cdot10^{13}$ holes/cm^3) and the depth of the depletion zone (2 μm), which yields S=$2\cdot10^9$ holes/cm^2. Taking this into account, the distance that a given holes concentration travels in time can be estimated. Thus, after t=164 ps, the C=$1\cdot10^5$ holes/cm^3 concentration that can be considered as necessary to assure an avalanche has travelled 3.90 μm, which is the distance between two neighboring active regions (A in Fig. 3.17). Similarly, after 6.23 ns this concentration has travelled 22.90 μm, i.e. it has crossed an entire pixel and reached the next active area (B in Fig. 3.17). According to this description, electrical crosstalks should be produced between 164 ps and 6.23 ns after the ignition of the avalanche. These results match well with the drift-diffusion simulations by ISE-TCAD. Fig. 3.18 shows two frames of the evolution of the holes distribution across two neighboring GAPDs after the ignition of an avalanche in the middle of the left sensor. Fig 3.18-a represents the moment in which the generated holes concentration is maximum (400 ps after the ignition). Fig 3.18-b shows the highest holes concentration reaching the neighboring pixel (6 ns after the ignition). The values of the parameters for the ISE-TCAD simulation are based on the FEOL (Front-End Of Line/transistor formation) process of the HV-AMS 0.35 μm technology. Apart from that, some photons may be released due to electroluminescence during an avalanche. These photons may be absorbed by neighboring pixels, where they may trigger an avalanche caused by optical crosstalk. However, optical crosstalk is negligible in monolithic GAPD arrays given the relatively small number of carriers involved in an avalanche in comparison to hybrid devices [11].

3.4.2 Characterization

According to the theoretical description provided above, it seems feasible to eliminate or at least reduce the electrical crosstalk between GAPD pixels allocated in the same well by inhibiting the sensors a short enough time just after the triggering of an avalanche. This theory was validated by means of two different experiments. On the one side, a first characterization was obtained by means of a dual-beam FIB-SEM (Focused Ion Beam-Scanning Electron Microscopy) machine, which was used to focus an electron beam with a nanometer spot on one

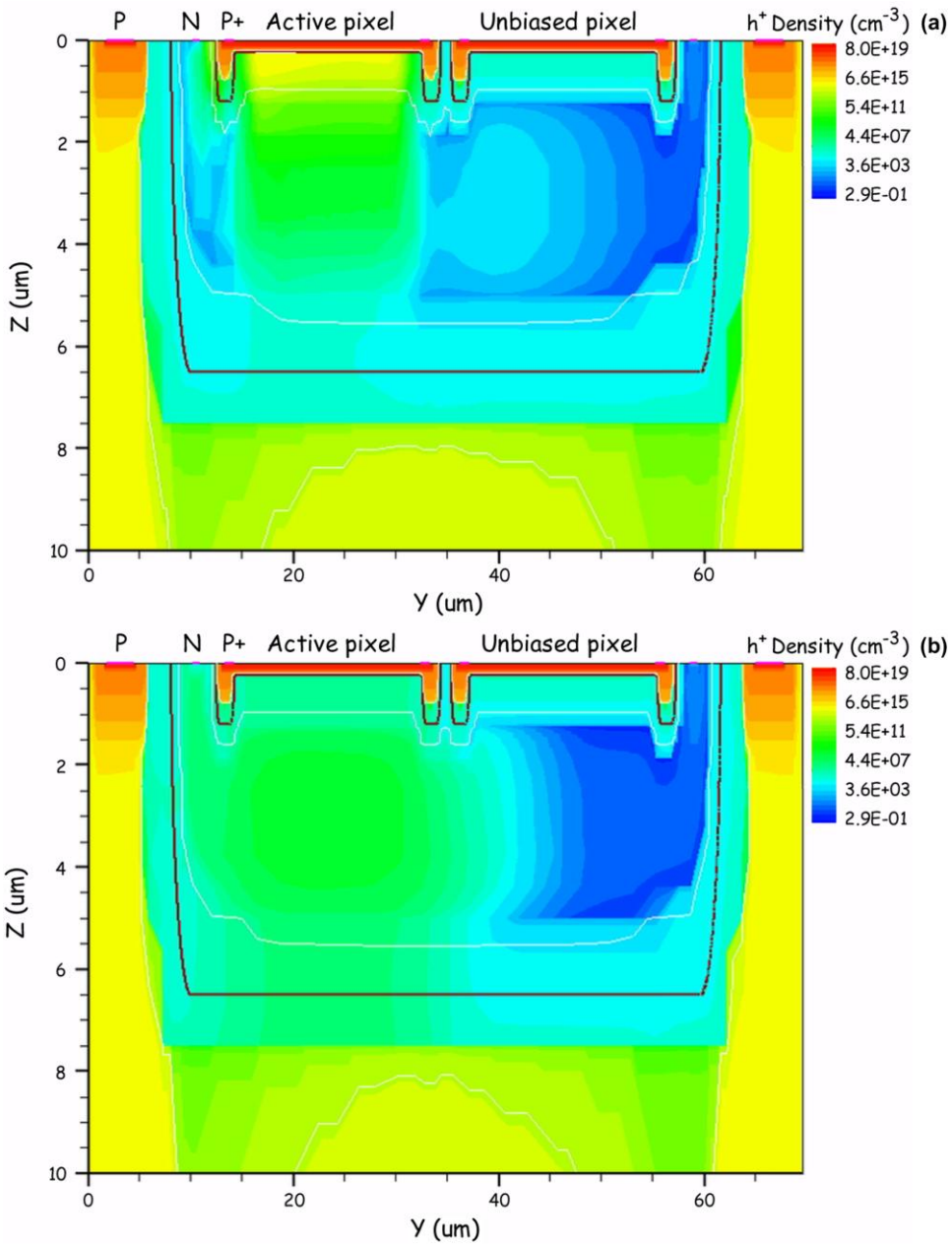

Figure 3.18 ISE-TCAD drift-diffusion simulation of the holes distribution across two sensors of the GAPD array 400 ps (a) and 6 ns (b) after after an avalanche is triggered in the middle of the left sensor.

pixel of the GAPD array. However, the progressive oxide charging during the realization of the experiment prevented the complete characterization of the device. On the other side, a much more detailed characterization was achieved when only the pattern noise generated by the sensor in the dark was accounted to quantify the electrical crosstalk. Good agreement is found between the behavior observed in the sensor through both experiments. The experimental set-ups used and the results obtained are described in the following lines.

In the first experiment, a FEI DualBeam Strata 235 FIB-SEM machine was used to generate a controlled electron beam. The advantage of this apparatus is that it can generate spots with nanometer size, which can be focused on one GAPD pixel of several μm with great accuracy [12]. After being produced, the beam was collimated, accelerated up to 1 keV and focused to a spot diameter of 1 nm on one pixel at one of the edges of the GAPD array. The chip containing the 1 x 5 GAPD array used for the characterization was mounted onto a PCB, which was stacked to a terasIC DE0-Nano development board based on an ALTERA Cyclone IV FPGA. The FPGA was used to generate the fast control signals that are required for the detector operation, count the number of pulses generated and manage the communication with a computer via a USB, as done in the characterization of the previous circuits. The whole detector system formed by the PCB with the chip and the FPGA were kept in the vacuum chamber of the FIB-SEM machine during the measurements, while the control and display system was outside the machine. The set-up used in this experiment is shown in Fig. 3.19.

During the measurement, the detector was biased at 2 V of overvoltage. To characterize the maximum value of the electrical crosstalk, the gated-on period was set at a long value of 100 ns. To get rid of afterpulses and relax the data acquisition system, the gated-off period was set also at a long value of 1 μs. The number of repetitions was $1 \cdot 10^6$ so as to obtain reliable results. Before the electron beam was turned on, the pattern noise of the array was measured to be 364 counts, $71.54 \cdot 10^3$ counts, 539 counts, $5.40 \cdot 10^3$ counts and $4.21 \cdot 10^3$ counts for pixels from 0 to 4, respectively, after $1 \cdot 10^6$ repetitions in the dark. Thus, the measured pattern noise includes dark counts and electrical crosstalks. During irradiation, pixel 4 received the electron beam. It generated a net signal (i.e. the total counts generated in the presence of the beam minus the pattern noise) of 6702 counts. In pixel 3, the first neighbor, a spread of 147 counts was recorded. This value corresponds to the 2.2% of the signal counts generated by pixel 0. Negligible spreads were recorded in the other pixels. This experiment suggests that the maximum electrical crosstalk of the GAPD array is 2.2% in the first neighbor and negligible in the remaining pixels.

Due to the difficulties related to this experimental set-up, further measurements at shorter gated-on periods were not successfully achieved with this measuring technique. The electron beam progressively charges the oxide layers that are present above the silicon surface of the chip until saturation. It is known that this phenomenon affects the breakdown voltage of GAPDs [13]. To validate and complement the preliminary results, a second experiment accounting only the noise counts generated by the sensor in the dark was performed. A set of measurements for different gated-on periods that range from 37 ns to 3.7 ns were carried out in darkness at 1 V of overvoltage. The minimum gated-on period is set by the control system and cannot be further reduced. To quantify the electrical crosstalk probability, a photodiode with a high DCR in a

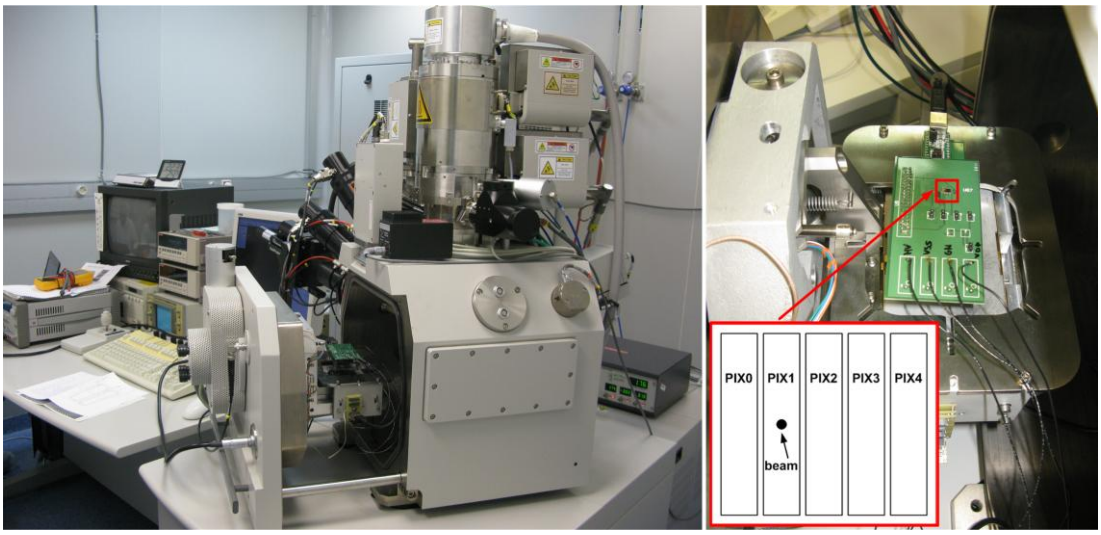

Figure 3.19 Experimental set-up for the characterization of the electrical crosstalk in GAPD arrays using a dual-beam FIB-SEM machine.

relatively quiet environment was selected from the GAPD array [14]. This photodiode, which can generate electrical crosstalk to its primary and secondary neighbors, is considered to be the emitter. A pulse coincidence between the emitter and one or more of its primary and secondary neighbors within the same active period indicates either a random coincidence of two dark counts or an electrical crosstalk between these diodes. The percentage of pulse coincidences (calculated as *counts receiver·100/counts emitter*) is shown in Fig. 3.20, which shows that the electrical crosstalk can be suppressed with short t_{obs} of a few nanoseconds. The numerical pixel emissions for the emitter and its neighbors are plotted in Fig. 3.21.

The electrical crosstalk probability at long gated-on periods is measured to be 2.6%, which matches the result obtained with the FIB-SEM set-up. As the gated-on period is shortened, the crosstalk probability is kept constant until 7 ns. At this gated-on period the electrical crosstalk starts to decrease. With a t_{obs} of 3.7 ns, the percentage of pulse coincidences between the pixel emitter and its primary neighbors is around 0.23%. These measured results match well with the ISE-TCAD simulations. The measurement also indicates that crosstalk counts generated in secondary neighbors have a maximum probability around 0.25% starting from t_{obs}=7 ns. This result is not reasonable, given the time needed by the charge concentration to travel to the first and second neighbors. It is estimated that this is the percentage that corresponds to the error associated to the measurement. The detected coincidences between the emitter and its neighbors as a function of the gated-on period are summarized in Table 3.1. It can be inferred from this table that the expected dark counts during the measurement time does not have a significant negative influence on the measurement of the crosstalk with this technique.

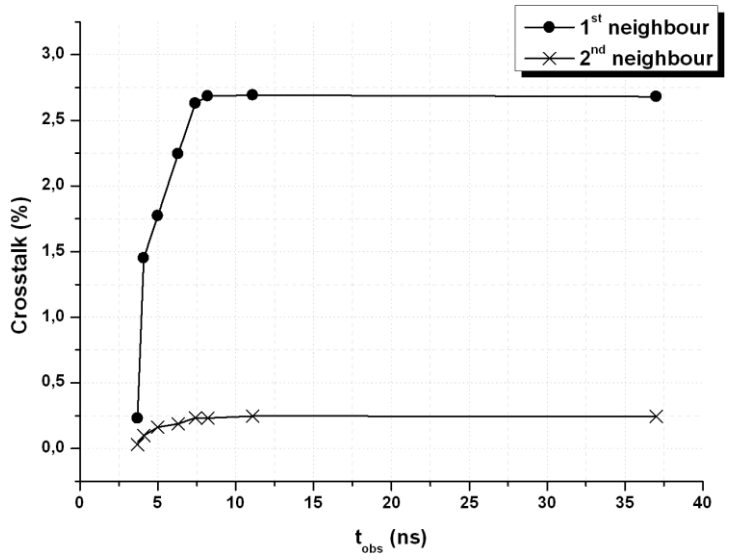

Figure 3.20 Percentage of crosstalks as a function of t_{obs} at 1 V of overvoltage.

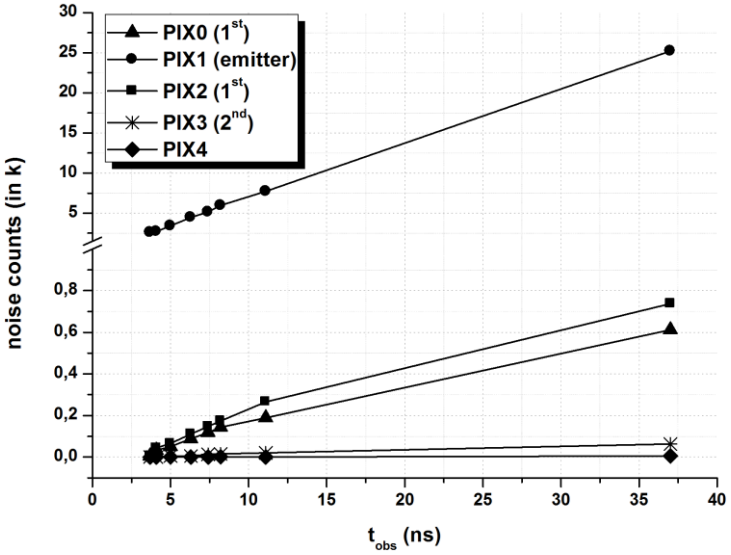

Figure 3.21 Pixel emissions as a function of t_{obs} for the emitter (PIX1) and its neighbors.

3.5 Discussion

Without a doubt, the most demanding requirement for all the candidate technologies aimed at particle tracking at future linear colliders is to comply with the demanded occupancy, which is usually induced in the most part by the beam related backgrounds. In the case of ILC, 0.004 background hits/cm^2/BX (4th layer of the forward tracker detector) [15] are foreseen, while this number is as high as 0.87 background hits/cm^2/BX [16] in the case of CLIC. Considering a sensitive area of 20 μm x 100 μm per pixel together with the 2820 or 312 bunch crossings per train at ILC and CLIC respectively, a total of $8 \cdot 10^{-8}$ background hits/GAPD/BX ($2.26 \cdot 10^{-4}$

t_{obs} (ns)	$t_m=t_{obs}\cdot coin$ (µs)	PIX0 (2.28 kHz)	PIX1 (42.84 kHz)	PIX2 (3.33 kHz)	PIX3 (32.55 kHz)	PIX4 (25.57 kHz)
3.7	9.6	6 (0.23%) 0.02 n.c.	2618	6 (0.23%) 0.03 n.c.	0 (0%) 0 .31 n.c.	0
4.1	11.1	33 (1.22%) 0.02 n.c.	2712	44 (1.62%) 0.04 n.c.	1 (0.03%) 0.36 n.c.	0
5	17.0	51 (1.50%) 0.03 n.c.	3407	66 (1.93%) 0.05 n.c.	5 (0.15%) 0.55 n.c.	0
6.3	28.1	88 (1.97%) 0.06 n.c.	4463	111 (2.49%) 0.09 n.c.	6 (0.13%) 0.91 n.c.	1
7.4	38.0	119 (2.33%) 0.09 n.c.	5136	148 (2.88%) 0.13 n.c.	13 (0.25%) 1.23 n.c.	1
8.2	48.9	144 (2.40%) 0.11 n.c.	5974	174 (2.92%) 0.16 n.c.	15 (0.25%) 1.59 n.c.	2
11.1	85.8	189 (2.45%) 0.19 n.c.	7732	266 (2.93%) 0.28 n.c.	20 (0.25%) 2.79 n.c.	1
37	932	612 (2.43%) 2.12 n.c.	25201	738 (2.91%) 3.10 n.c.	63 (0.25%) 30.3 n.c.	5

Table 3.1 Detected coincidences between the emitter (PIX1) and its neighbors as a function of the gated-on period. The values in column PIX1 correspond to the pulses generated by the emitter during a certain measuring time, while the values of other columns correspond to the detected pulse coincidences between the emitter and each neighbor, the percentage of crosstalk (in brackets) and the expected noise pulses according to the DCR of the pixel and the measuring time. The DCR of each pixel is in brackets in the first row of the table. The measuring time is given by the gated-on period and the pulses generated by the emitter.

background hits/GAPD/train) at ILC and $1.74\cdot10^{-5}$ background hits/GAPD/BX ($5.43\cdot10^{-3}$ background hits/GAPD/train) at CLIC are expected.

However, in GAPD detectors the occupancy is dominated by the high frequencies of the sensor pattern noise rather than the beam related backgrounds. A GAPD detector operated in free-running at 1 V of V_{OV}, and thus with an average NCR of 85 kHz (see Fig. 3.8), will generate 80.78 noise counts/GAPD/train at ILC. This value is extremely higher than the expected background hits (more than 5 orders of magnitude) and therefore is unacceptable. In this chapter, the capabilities of the time-gated operation in terms of reducing the detected sensor noise have been investigated. It has been demonstrated that it is possible to eliminate the afterpulsing probability with a long enough gated-off period. Moreover, the DCP can be reduced as the gated-on period is shortened. At ILC, where the bunch-spacing is long enough to pulse the detector and also extract the content of each pixel after each bunch crossing, it is possible to lessen the DCR to 45 kHz with a gated-off period around 300 ns at 1 V of V_{OV} (see Fig. 3.8). Then, with a gated-on period of 10 ns the DCP can be suppressed down to $4.50\cdot10^{-4}$ noise counts/GAPD/BX. If a shorter gated-on period of 1 ns can be used, it should be also possible to suppress the electrical crosstalk effects. Considering that the crosstalks represent the 2.6% of the noise generated in GAPD sensors arranged in arrays, the average DCR of 45 kHz

can be reduced to 43.83 kHz. In this case, $4.38 \cdot 10^{-5}$ noise counts/GAPD/BX, with a difference of 3 orders of magnitude with respect to the beam related backgrounds, are to be expected.

Given the challenging bunch-spacing of 0.5 ns planned for CLIC, at this particle collider it is not possible to operate the GAPD detector in the time-gated mode nor extract the generated information during the inter-bunches. Therefore, the detector has to be operated in the free-running mode and read out during the inter-train period, which yields $1.33 \cdot 10^{-2}$ noise counts/GAPD/train (1 order of magnitude higher than the beam related backgrounds).

Anyhow, the noise counts generated by the sensor are still much higher than the induced background hits at both particle colliders, even if the detector is operated in the time-gated mode. It is therefore necessary to explore other solutions, such as cooling, that could be applied in conjunction with the time-gated operation. The benefits obtained with the reduction of the working temperature will be presented in the following chapter. Nevertheless, the possibility of using a logic AND between the output values of two or more overlapped pixels from two or more different layers as a solution to decrease the DCP is also considered. Also in the following chapter, a complete analysis of the fulfillment of the ILC and CLIC requirements by GAPD detectors will be detailed.

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Chapter 4

Design and characterization of large arrays in a HV-CMOS process

A very important breakthrough in the development of a new sensor technology aimed to particle tracking is accomplished by characterizing the performance of the proposed technology to a series of beam-tests experiments. In a beam-test, the response of a prototype detector to high energy particles is characterized. If not satisfactory, the results of the beam-test may invalidate the proposed sensor technology as a suitable candidate for tracking detector systems.

This chapter reports the design and characterization of a prototype GAPD array monolithically integrated in a conventional 0.35 μm HV-CMOS process (h35b4). The design includes a readout circuit based on the voltage-mode approach to operate the sensor at low overvoltages and reduce the DCR. Moreover, the detector can be operated in the time-gated regime to reduce the probability of detecting the sensor noise around a certain time slot. A number of experiments have been conducted on the detector to show that the proposed techniques are advantageous in improving not only the occupancy of the detector, but also the dynamic range, contrast and spatial resolution. It is also demonstrated that further improvements can be achieved with the reduction of the working temperature. Finally, the suitability of the detector for particle detection is shown with the results of a beam-test campaign conducted at CERN-SPS (European Organization for Nuclear Research-Super Proton Synchrotron).

4.1 Design of a time-gated array of 10 x 43 pixels

A first prototype of a time-gated GAPD pixel array has been designed and fabricated as a proof of concept of such sensors in high energy particle detectors. Therefore, techniques to mitigate the radiation effects and on-chip data processing are not included at the moment. The detector consists of an array of GAPD pixels which are arranged in 10 rows per 43 columns. In total, it has a sensitive area of 1 mm x 1 mm, which was chosen to increase the probability to observe events during the beam-test of the detector. Each photodiode has a sensitive area of 20 μm (width) x 100 μm (height) to meet the geometry required for the tracking detector system. It is based on the same structure and mode of operation described in section 3.1.1.1, and therefore this will not be further commented. The in-pixel readout circuit is placed on top of each pixel,

between two consecutive rows of sensors (see Fig. 4.1). With the purpose of maximizing the fill-factor of the array, all the GAPDs within a row share a common deep n-tub, generating a macro-pixel of 43 GAPDs (see Fig. 3.17). However, the introduction of the deep p-tub implantation to avoid the premature edge breakdown generates a minimum separation between two neighboring GAPDs of 1.7 μm (horizontal direction). As a result, the detector features a pixel pitch of 22.9 μm (width) x 138.1 μm (height, including the readout circuit), and an optical fill-factor of 67%. Although this value is superior to the usual GAPD fill-factors, it must be further incremented to fulfill the requirements that future linear colliders put on tracking detector systems. Apart from that, because the GAPDs that belong to the same macro-pixel share the deep n-tub layer, the electrical crosstalk probability is nonzero. Nevertheless, this probability can be minimized with short enough gated-on periods, as demonstrated in the previous chapter.

A schematic diagram of the pixel is shown in Fig. 4.2, together with the delay introduced by each element. Each pixel is comprised of a GAPD, inhibition (M_{P0}) and active reset (M_{N0}) switches to perform the time-gated operation and a readout circuit based on the 2-grounds scheme described in section 3.1.1.2. Amongst all the readout circuits explained in the previous chapter and that were developed prior to the design of the 10 x 43 GAPD array, the one based on the 2-grounds scheme was chosen for implementation in a larger detector because of its reduced number of transistors. Thus, the readout circuit of the 10 x 43 GAPD array comprises a CMOS inverter (M_{P1}-M_{N1}), a 1-bit memory register (M_{N2}-M_{P2}-M_{N3}) and a pass-gate (M_{N4}) to read the array sequentially. With respect to the first version of this circuit, the transistor M_R (see Fig. 3.1) was eliminated to save area and reduce the parasitic capacitance of the V_S node. The area occupation of the transistors M_{P0} and M_{N0} was reduced as well. Like in the previous chip, the sensor capacitance C_{AK} is calculated to be 540.19 fF at 1 V of overvoltage. The value of C_P, the parasitic capacitance associated to the sensing node, can be expressed as

$$C_P = C_{D,MP0} + C_{D,MN0} + C_{G,MP1} + C_{G,MN1} \tag{4.1}$$

where $C_{D,MP0}$ and $C_{D,MN0}$ correspond respectively to the drain capacitances of transistors M_{P0} and M_{N0}, and $C_{G,MP1}$ and $C_{G,MN1}$ correspond to the gate capacitances of transistors M_{P1} and M_{N1}. The parasitic capacitance C_P is calculated to be 15.75 fF [1].

In order to control the outward data flow, a simple address circuit based on a pass-gate (M_{N4}) placed between the dynamic latch and the output column line is used to sequentially read the ten rows of the GAPD array during the gated-off intervals. The pass-gate M_{N4} is controlled by means of the external signal $CLK2_m$, with m=[1, 10]. When the $CLK2_m$ signal is set high, the transistor M_{N4} of row m is switched on and the dynamic latch feeds its corresponding output

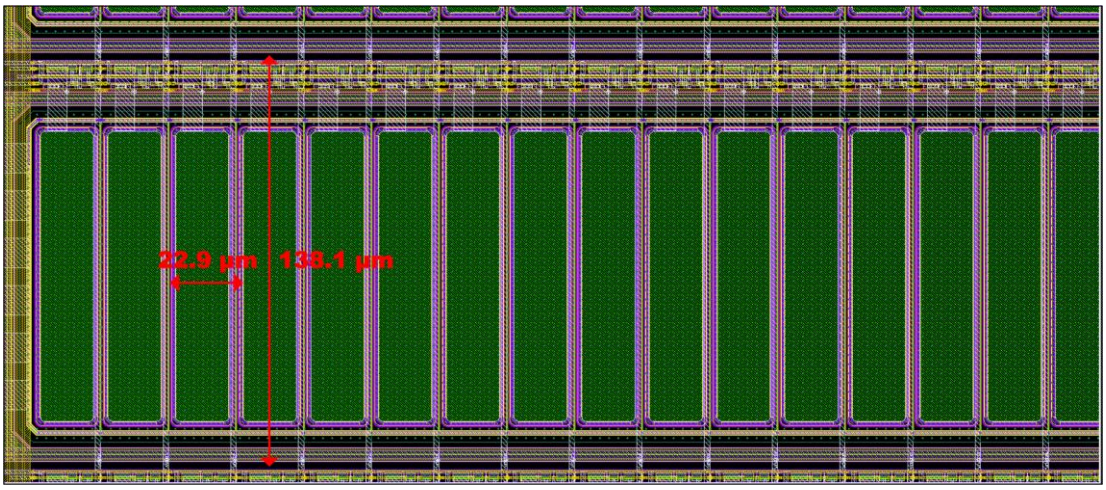

Figure 4.1 Row of GAPDs with their corresponding readout circuits.

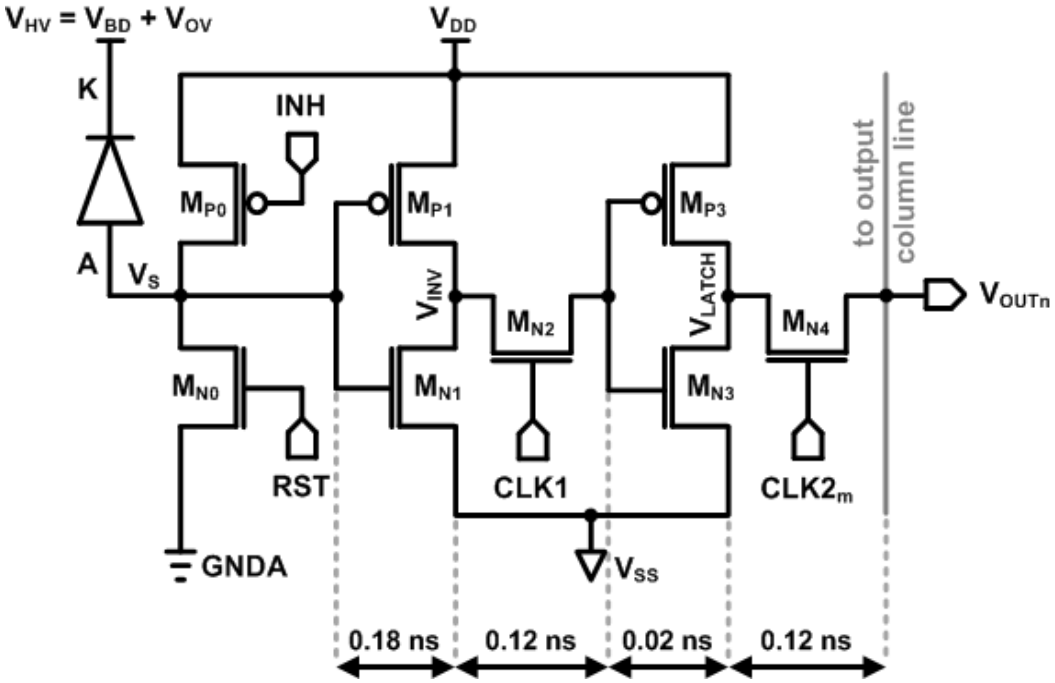

Figure 4.2 Schematic diagram of the time-gated digital pixel in the HV-AMS 0.35 µm CMOS technology. V_{OUTn} is connected to the output column line n.

column line n, with n=[1, 43]. The output column line is directly connected to the output buffer and output pad. Multiplexers or selection decoders are not used and hence this readout configuration requires 43 output pads plus 13 pads for the control signals (RST, INH, CLK1 and the ten CLK2). After an avalanche has been triggered (rising time around a few hundred picoseconds), it takes 0.32 ns to digitize and store the generated signal in node V_{LATCH}, i.e. delay introduced by the inverter M_{P1}-M_{N1} (0.18 ns), the pass-gate M_{N2} (0.12 ns) and the inverter M_{P2}-M_{N3} (0.02 ns). Then, when transistor M_{N4} is turned on, the signal reaches the exterior of the chip in 1.33 ns, i.e. delay introduced by the pas-gate M_{N4} (0.12 ns), the output buffer (0.26 ns) and the output pad (0.95 ns). As a result, each pixel can be read in 1.65 ns.

4.2 Characterization

The chip containing the 10 x 43 GAPD pixel detector was submitted for fabrication through a MPW run organized by Europractice on 26th April 2011. A micrograph of the complete chip fabricated with the HV-AMS 0.35 µm standard CMOS technology is shown in Fig. 4.3. The central area of the chip corresponds to the 10 x 43 GAPD array. In addition, the chip also contains a test sensor with access to the sensing node (lower left side in Fig. 4.3) to characterize the current-voltage curve of the sensor. A test pixel with the same readout circuit as that used by the pixels of the array was integrated in the chip (central left side in Fig. 4.3) to study the performance of the pixel without the influence of neighboring pixels.

The performance of the GAPD pixel detector was characterized by means of an Agilent E3631A voltage source and a terasIC DE0-Nano development board based on an ALTERA Cyclone IV FPGA. The FPGA was used to generate the control signals, count off-chip the number of pulses generated by the pixels and manage the communication with a computer via an FTDI chip and a USB. Real time images were obtained with the support of a dedicated software. The characterization of the detector was done with a programmable total measuring

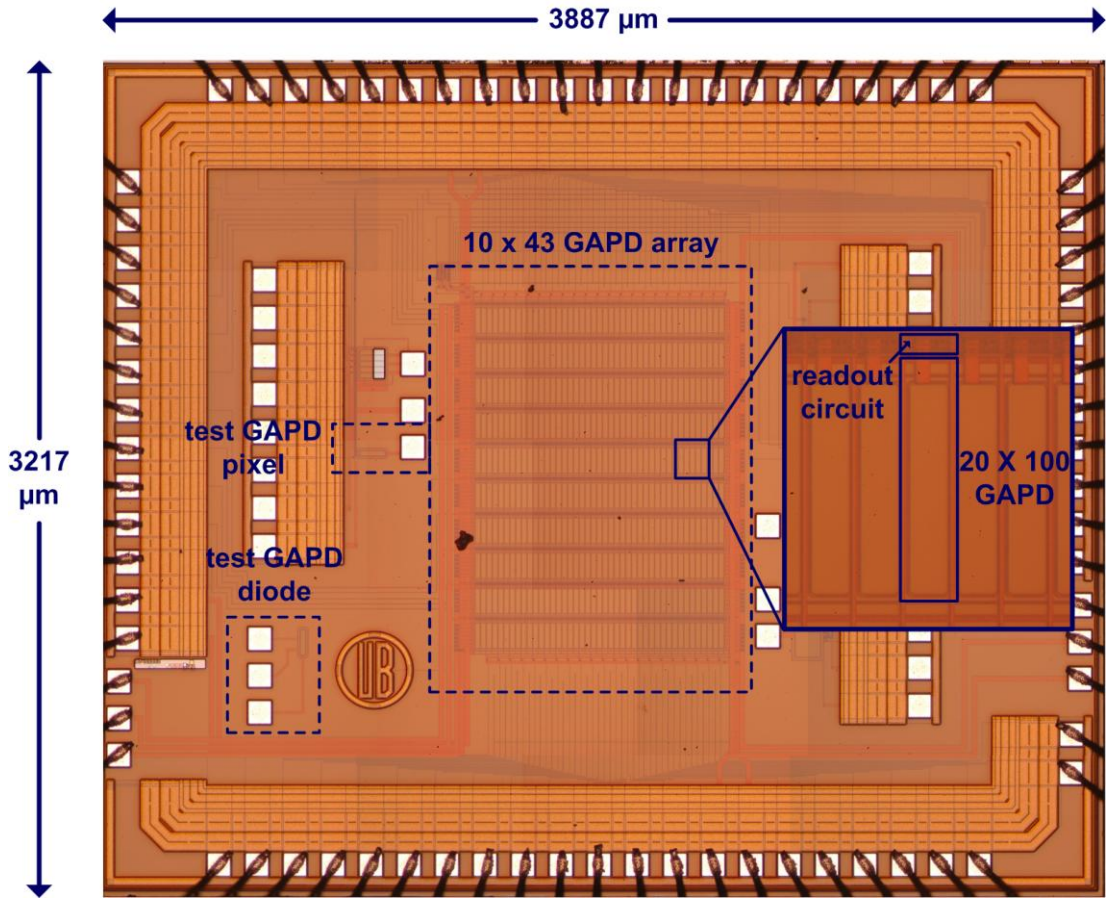

Figure 4.3 Micrograph of the fabricated chip with the 10 x 43 GAPD array.

time that depends on the period of observation and the number of repetitions.

4.2.1 I-V curve

As in the previous run, the current-voltage curve of the test GAPD was characterized with a 4-wire method to obtain the breakdown voltage. At room temperature in the dark, V_{BD} and I_{GAPD} are respectively set at 18.90 V and 0.4 mA, as it can be observed in Fig. 4.4.

4.2.2 Afterpulsing

The afterpulsing probability of the test pixel was measured in darkness as a function of the gated-off period. Fig. 4.5 shows the NCR (defined in Eq. 3.2) data extracted from the analysis, which was obtained using a fixed t_{obs} of 12 ns and different V_{OV} of 1 V, 1.5 V and 2 V. The NCR presents a constant value for long t_{off} durations regardless of V_{OV}. On the contrary, for short t_{off} durations starting around 200 ns, the NCR increases as t_{off} is reduced. For instance, a t_{off} of 200 ns yields an afterpulsing probability lower than 1% for all the V_{OV} measured. However, for a t_{off} of 50 ns this probability raises up to 11%, 17% and 22% when V_{OV} is 1 V, 1.5 V and 2 V, respectively.

4.2.3 Dark count rate

The DCR (defined in Eq. 3.3) of the 10 x 43 GAPD array was measured also in darkness with the sensor t_{obs} and t_{off} set at 1274 ns and 1 µs, respectively. Although t_{off} periods around 200 ns should be enough to eliminate the afterpulsing probability, t_{off} intervals of 1 µs were chosen so as not to stress the data acquisition system. Fig. 4.6 shows the cumulative plot of the DCR for two different overvoltages of 1 V and 2 V at room temperature. Cumulative plots typically describe the probability at which a certain value of the magnitude being analyzed will be find in a given population. The plot of Fig. 4.6 indicates the cumulative percent of pixels of the array that are less than or equal to a certain frequency. The median DCR of the array (i.e. the value that corresponds to a cumulative percent of the 50%) is respectively 40 kHz and 95.3 kHz at 1 V and 2 V of overvoltage. In contrast, the mean DCR is respectively 67 kHz and 139 kHz at 1 V and 2 V of overvoltage. The literature typically reports lower DCRs obtained with smaller GAPDs. It is well known that the DCR increases with the sensor area. However, large sensor areas were chosen in this work to meet the requirements of the next generation of particle colliders. In Fig. 4.6 it can also observed that the variation of the DCR across the array is almost

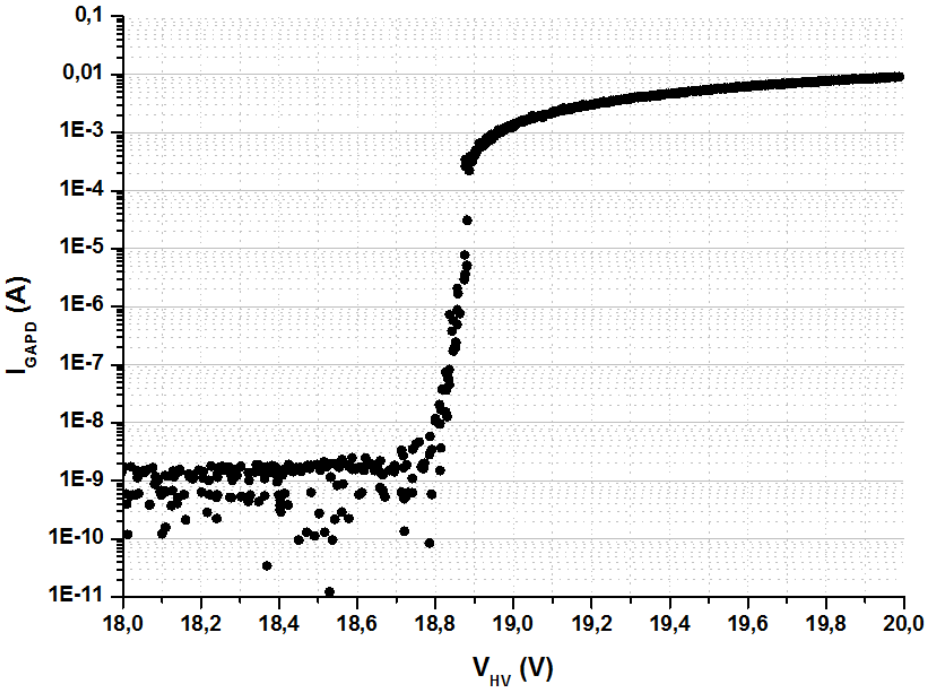

Figure 4.4 I-V curve of the Geiger-mode in the dark.

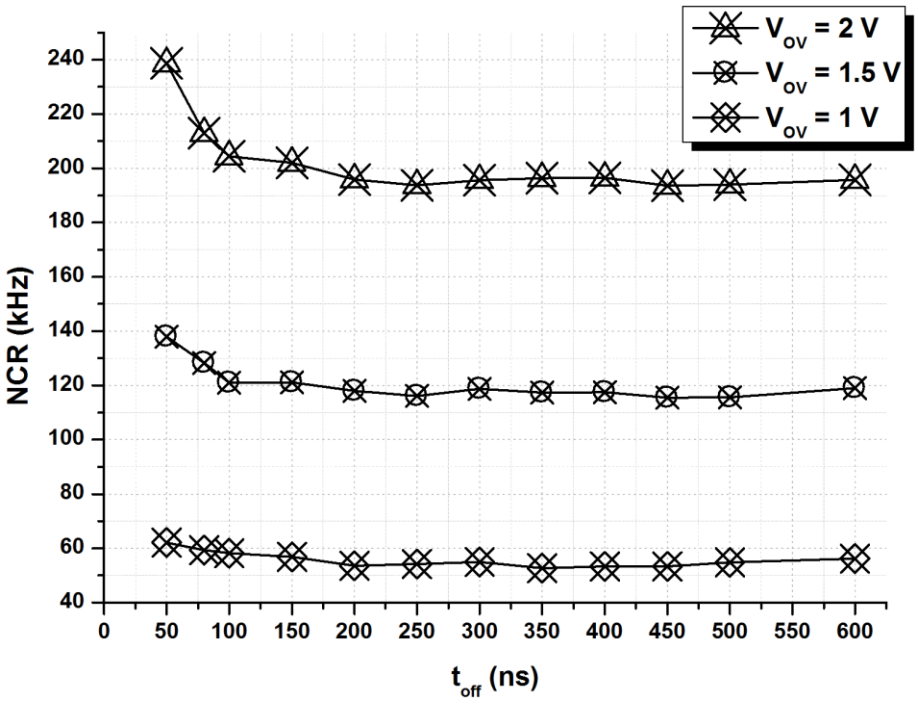

Figure 4.5 Noise count rate for different t_{off} and V_{OV}.

of 2 orders of magnitude. However, similar phenomena have been reported in [2, 3]. In particular, in [3] a DCR variation of 4 orders of magnitude is registered. This phenomenon is due to the extreme dependence of the DCR to defects in the crystal lattice of silicon.

As a solution to the high DCR, the detector is operated in a time-gated regime, where the probability of a certain pixel detecting a dark count within a given frame (i.e. DCP) lessens

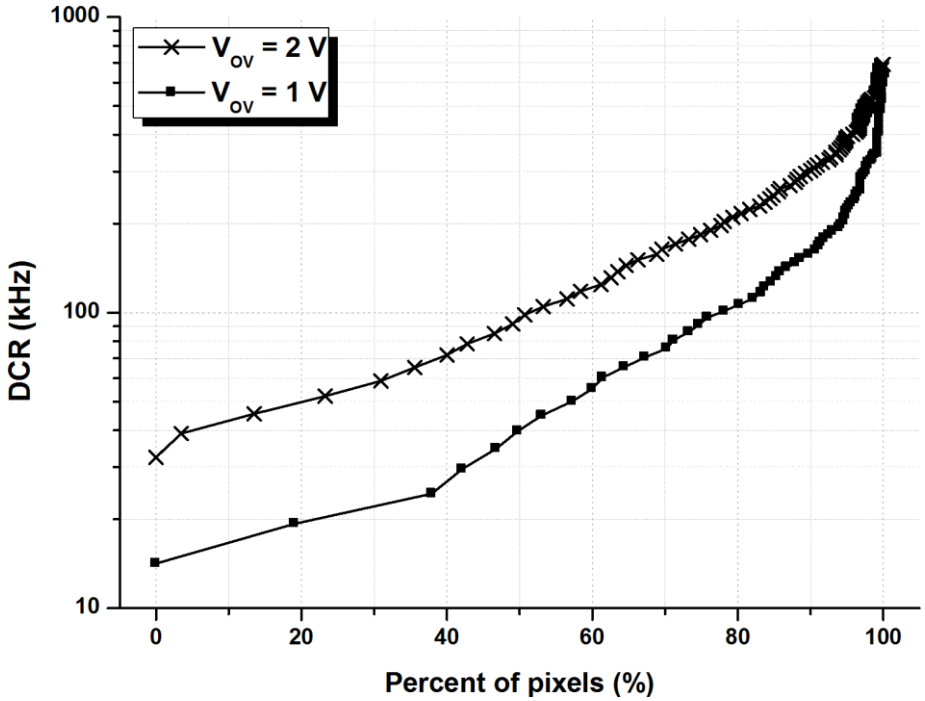

Figure 4.6 Cumulative plot of the DCR distribution across the GAPD array at 1 V and 2 V of overvoltage.

linearly as t_{obs} is shortened [4-6]. Thus, with a mean DCR of 67 kHz at 1 V of overvoltage, the DCP per pixel can be reduced from $8 \cdot 10^{-2}$ to $2 \cdot 10^{-4}$ when the sensor t_{obs} is shortened from 1274 ns to 4 ns. This situation is advantageous for imaging systems aimed to sense ionizing radiation with a predictable time of arrival, where it is possible to operate the detector in a time-gated mode to reduce the DCP without losing any useful input signal. Some of the benefits gained are an increase of the SNR, an extension of the DR and the improvement of the contrast and spatial resolution of the detector, as it will be shown next.

4.2.4 Photon detection probability

The spectral response of the GAPD array was tested using a UV-VIS spectrophotometer (SPECORD 250) and a calibrated reference detector. The measured PDP (Photon Detection Probability) as a function of the photon wavelength within the range 400-1000 nm is depicted in Fig. 4.7. The plotted data correspond to the average value of all pixels of the array. The PDP is larger than 10% between 500 nm and 710 nm with a V_{OV} of 2 V. Acceptable values around 4% have been achieved for the same wavelengths with a V_{OV} of 1 V. The peak is reached at about 610 nm, with values of 13.2% and 5.5% for the two measured V_{OV}. This performance is below expectations [6, 7] due to the reduced optical transparency introduced by the polymide

passivation layer of the technology process, as reported in [8]. The polymide coating could be prevented to improve these results.

4.2.5 Dynamic range

The input DR is the ratio between the maximum and minimum input signal. In this case, the lower limit (I_{th}) corresponds to the minimum light intensity from which signal counts above the background noise can be detected, i.e. at the level where the SNR is approximately unity. In contrast, the upper limit (I_{sat}) is given by the intensity that causes the saturation of the readout electronics. In a time-gated detector, I_{sat} is not given by the dead time of the sensor (set at 1 μs in this case), but by the maximum capacity of the counter. The DR can be expressed in base-2 logarithmic value by

$$DR = \log_2 \left(I_{sat} / I_{th} \right). \tag{4.2}$$

In many optical applications, the DR plays a very important part in the extraction of information of the physical process under investigation. In imaging applications, for instance, a wide DR results in a better differentiation in color and light, i.e. better contrast, between the parts of the generated image.

To obtain the DR of a time-gated GAPD array, the response to a variable optical intensity of

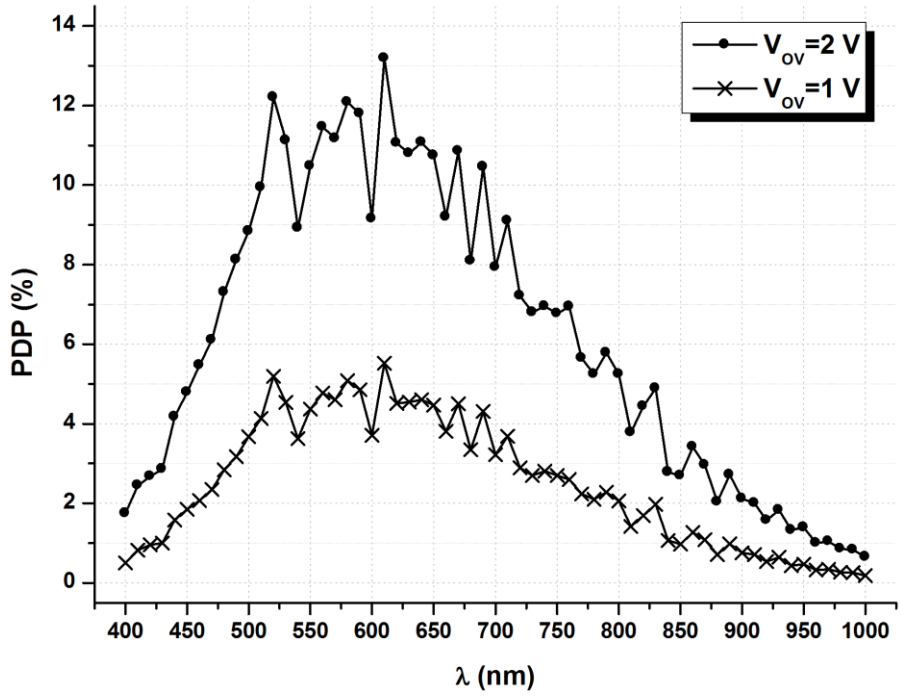

Figure 4.7 Average PDP measured at 1 V and 2 V of overvoltage.

a pulsed light source, typically a laser, should be tested. However, it is not possible to control the optical intensity of a laser. Other light sources, such as LEDs, allow controlling the optical intensity, but their slow switching times around 0.5 µs makes them useless for triggered measurements in the nanosecond range. In this work, a 880 nm LED [10] was used to indirectly estimate the DR of the time-gated GAPD array under pulsed light conditions within the sensor t_{obs}.

Fig. 4.8 illustrates the optical response of the GAPD array as a function of the current intensity of the 880 nm LED for two different t_{obs} of 1274 ns (*) and 14 ns (●). A LED active period of 14 ns within the sensor t_{obs} is assumed, being the pulse rate 0.44 MHz (0.99 MHz) and the duty cycle 0.61% (1.38%) for the 1274 ns (14 ns) t_{obs}. For each LED intensity, the detector response was observed as many times as the maximum capacity of the counter ($n_{rep}=10^7$ times) at a fixed V_{OV} of 1 V. The plotted data correspond to the average value of all the pixels of the array. As shown in Fig. 4.8, the detected noise counts are lower with the shorter t_{obs}. Moreover, the noise counts for both t_{obs} are in good agreement with the average DCR discussed before. Due to a lower noise background achieved with the shorter t_{obs}, weaker light intensities can be detected. As a consequence, the DR is extended from 9.21 to 12.84 bits (40%), which results in a better differentiation in luminance (i.e. a better contrast).

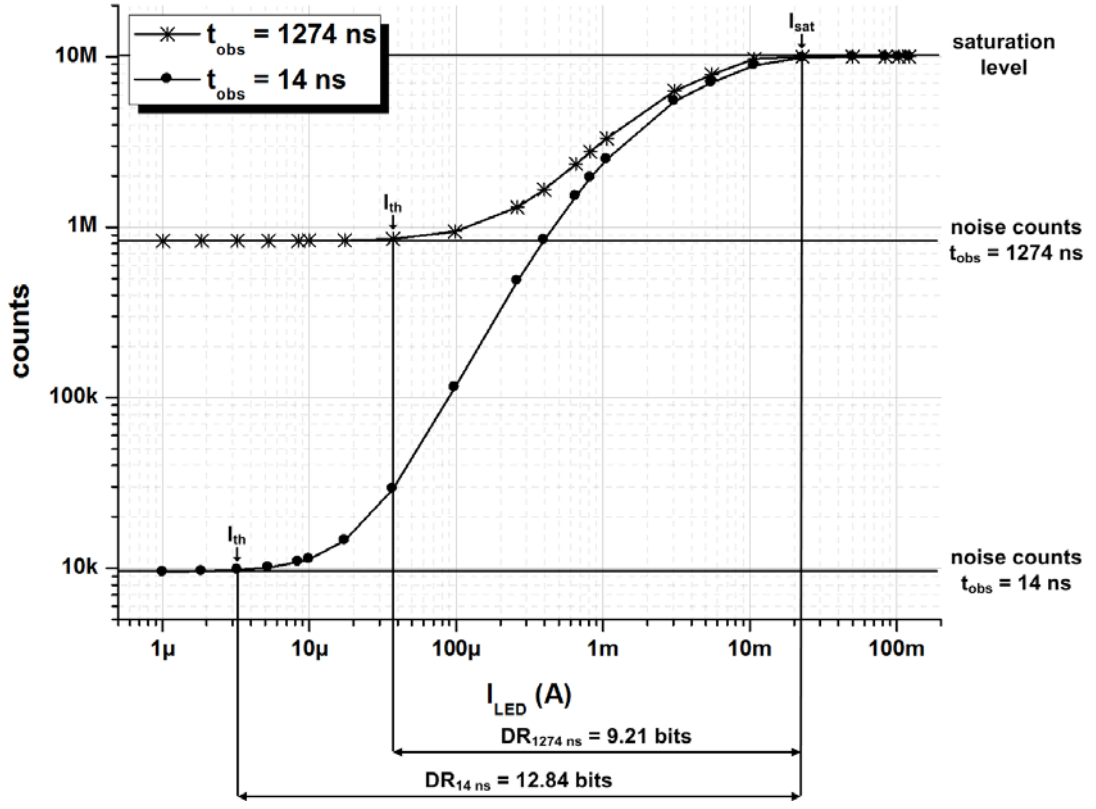

Figure 4.8 Optical response and dynamic range of the GAPD array to a variable optical intensity of a 880 nm pulsed light source using two different sensor t_{obs} of 1274 ns and 14 ns at a fixed V_{OV} of 1 V.

4.2.6 2D imaging

To show that short gated-on periods are advantageous to avoid the blinding of GAPD detectors as well as to increase the resolution, a triggered imaging system was assembled with the developed sensor. 2D images were obtained with the set-up shown in Fig. 4.9, where a pulsed laser was used as the light source. The array was coupled with a standard lens and a target object was placed in front of the array-lens system at a suitable distance. The target object was aligned with the array-lens system with a micropositioner. A pulsed 850 nm VCSEL (Vertical Cavity Surface-Emitting Laser) array [11] with an active window of 22 ns within the sensor t_{obs} was used to illuminate the target object. For the t_{obs} investigated, the pulse rate of the laser ranged from 0.44 MHz (t_{VCSEL}=22 ns, t_{obs}=1274 ns, t_{off}=1 μs, duty cycle 0.97%) to 0.97 MHz (t_{VCSEL}=22 ns, t_{obs}=34 ns, t_{off}=1 μs, duty cycle 2.13%). A second lens was used to spread the laser beam. A fast nFET placed between the VCSEL cathode and ground was used to switch the laser. The gate node of the nFET was connected to the FPGA, which periodically turned on and off the transistor and therefore the laser.

Fig. 4.10 shows the resulting images taken with different t_{obs} that range from 1274 ns to 34 ns. Each image is the sum of 10^7 frames. The high number of noise counts detected with longer t_{obs} masks the reproduction of the object. Given an average DCR of 67 kHz at 1 V of overvoltage, the 0.085 noise counts per frame that are detected with a t_{obs} of 1274 ns fill the 8.5% of the counter capacity. However, this parameter can be reduced to 0.23% with a sensor t_{obs} of 34 ns. This yields an improvement of the SNR and the spatial resolution of the recorded image, as it can be seen in Fig. 4.10.

4.2.7 Thermal effects

The thermal effects on some figures of merit of the GAPD detector, mainly the DCR, afterpulsing and PDP, were studied in the temperature range between -20 ºC and 60 ºC with a climatic chamber. It is well known that V_{BD} falls with the temperature because of the thermal dependence of the e^--h^+ ionization coefficients [12, 13]. Therefore, to characterize the thermal dependence of the sensor at a fixed V_{OV}, the thermal effect on V_{BD} was measured before. This experiment was conducted with the test GAPD accessible to the sensing node that was included in the chip. The data obtained by means of a 4-wire method indicates a linear decrease of V_{BD} with the temperature with a coefficient of ~20 mV/ºC, as shown in Fig. 4.11. The breakdown voltage at 0 ºC is measured to be 18.41 V.

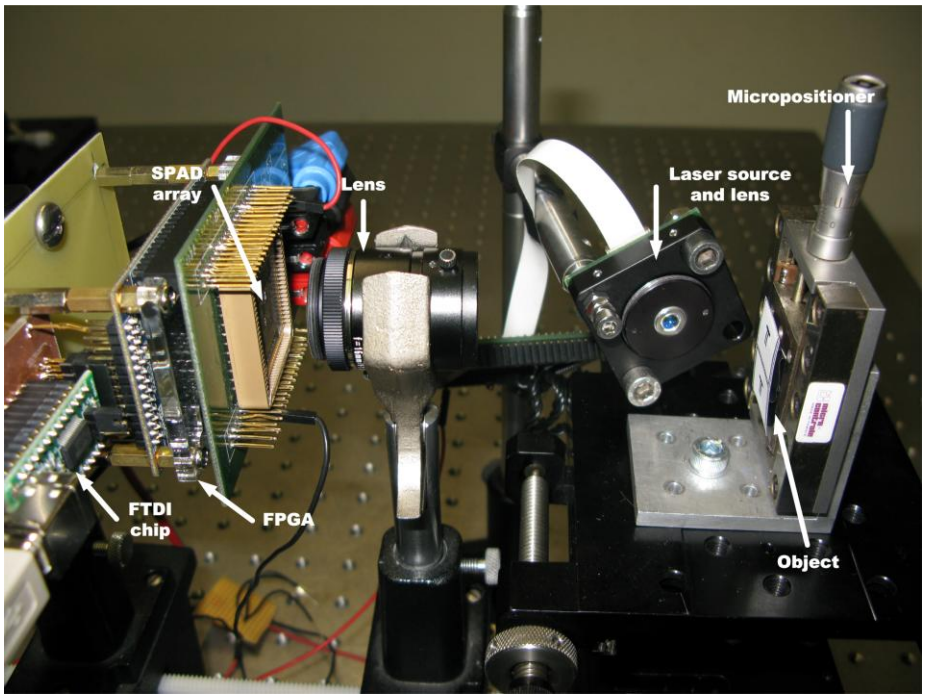

Figure 4.9 2D imaging set-up.

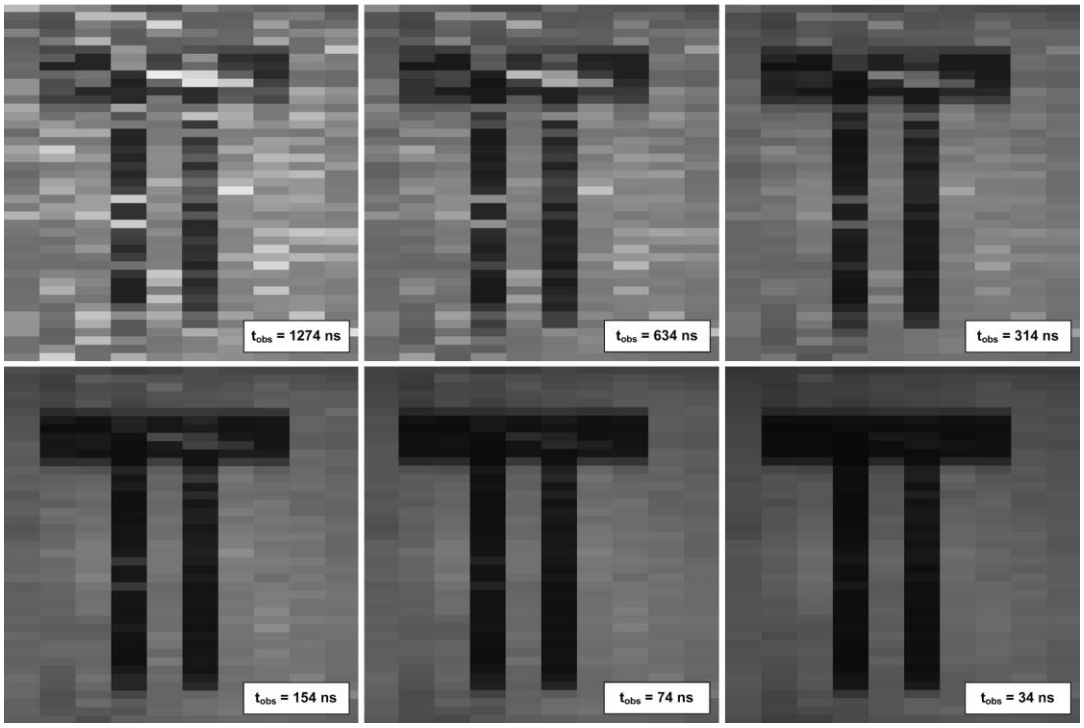

Figure 4.10 Image of a model at various t_{obs}. The model was illuminated by a pulsed laser light with an active window of 22 ns within the t_{obs}.

The thermal dependence of the DCR finds its explanation in the temperature dependent SRH (Shockley-Read-Hall) generation, including trap assisted tunneling, and band-to-band tunneling. Above room temperature, where the SRH generation dominates the band-to-band tunneling, the expected behavior of the DCR as a function of the temperature is an exponential dependence

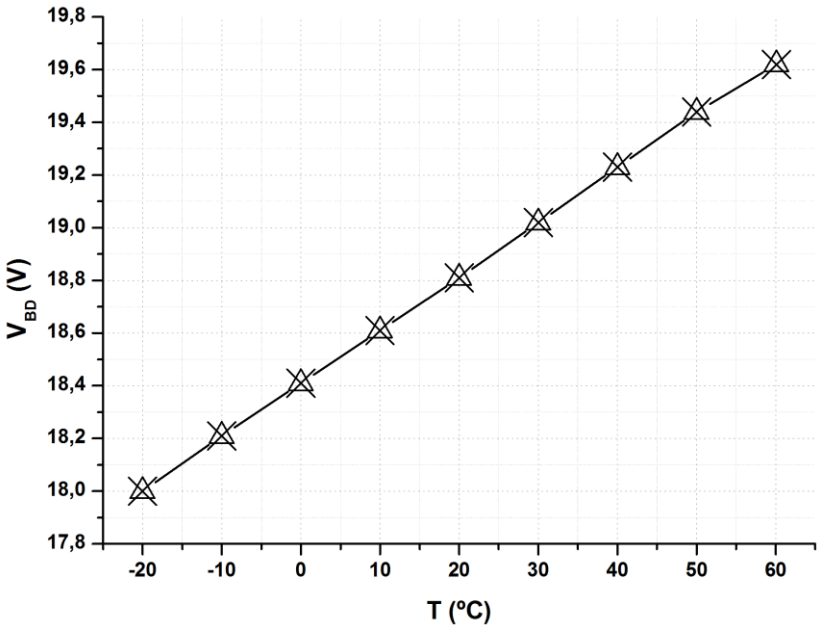

Figure 4.11 Measured breakdown voltage as a function of the temperature.

[14]. In this region, the DCR is roughly divided by two every 10 ºC. At low temperatures, in contrast, band-to-band tunneling becomes the dominant mechanism. Since this phenomenon is very weakly dependent on the temperature, the DCR is only slightly decreased. The corner temperature at which the SRH generation and the band-to-band tunneling have the same weight is around 10 ºC. Apart from that, the afterpulsing probability tends to rise below 0 ºC as the trapping lifetimes become longer.

For the 10 x 43 GAPD array, the NCR was measured in the dark within the temperature range between -20 ºC and 60 ºC at two different V_{OV} of 1 V and 2 V. The NCR is the noise generated by the sensor when this is operated in continuous mode or free-running. Therefore, the NCR includes dark counts, afterpulses and crosstalks. To operate the present GAPD detector in continuous mode, the INH control signal was not used during the measurements. The total measuring time was 14 ms for each of the points analyzed. Fig. 4.12 and Fig. 4.13 show a spatial map and the cumulative plot, respectively, of the NCR across all the pixels of the array. For a V_{OV} of 1 V, the mean NCR ranges from 132 kHz at -20 ºC to 630 kHz at 60 ºC. A noticeable increase is observed in the measurements at 2 V, where the mean NCR ranges from 636 kHz at -20 ºC to 1.66 MHz at 60 ºC. In Fig. 4.13, it can be appreciated that a slight percentage of the pixels (between 1 and 2%) exhibit a NCR which is well above the average value of the array. Thus, for instance, at 1 V of overvoltage, 2% of the pixels present a NCR of 2 MHz or higher. This percentage corresponds to the so-called hot pixels. The hot pixels of the GAPD detector reported here have been omitted in the spatial map plotted in Fig. 4.12 (only for the highest temperature), so that details in the behavior of the vast majority of the pixels can be easily

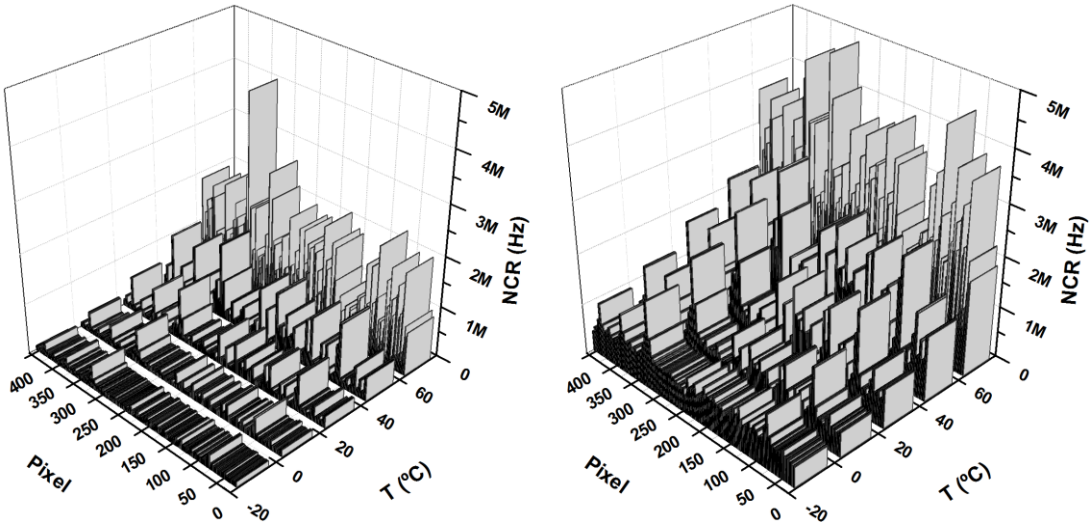

Figure 4.12 NCR across the detector within a temperature range between -20 ºC and 60 ºC at 1 V (left) and 2 V (right) of V_{OV}.

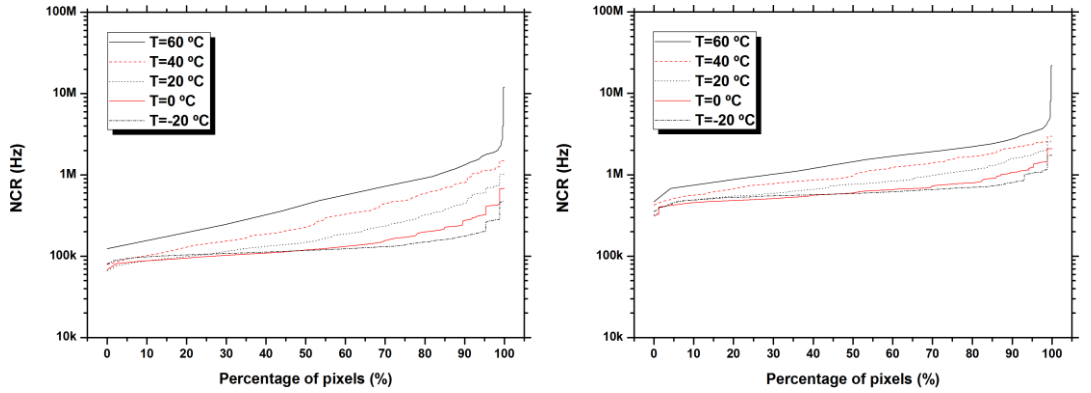

Figure 4.13 NCR cumulative plot across the detector within a temperature range between -20 ºC and 60 ºC at 1 V (left) and 2 V (right) of V_{OV}.

appreciated. Apart from that, the slope of the cumulative plots is softer at lower temperatures, which indicates that for a given number of bins the percentage of pixels sharing the same NCR margins is higher as the temperature is decreased. This is a consequence of the reduction of the difference between the maximum and minimum NCR over the pixels at low temperatures. The standard deviation of the NCR across the array is also reduced with the temperature (see Fig. 4.14), which indicates that the NCR of the different pixels tends to be closer to the mean value as the temperature is lowered. Moreover, also in Fig. 4.13 it can be seen that at and below 0 ºC, the minimum values of the detector NCR surpass those recorded at some higher temperatures. This is a symptom of the thermal effects of the afterpulsing.

The high NCR of the detector even at low temperatures makes it unsuited for particle detection. Nevertheless, the time-gated operation with a long enough gated-off period allows to get rid of the afterpulses. As a consequence, the noise rate of the detector (i.e. the DCR) can be

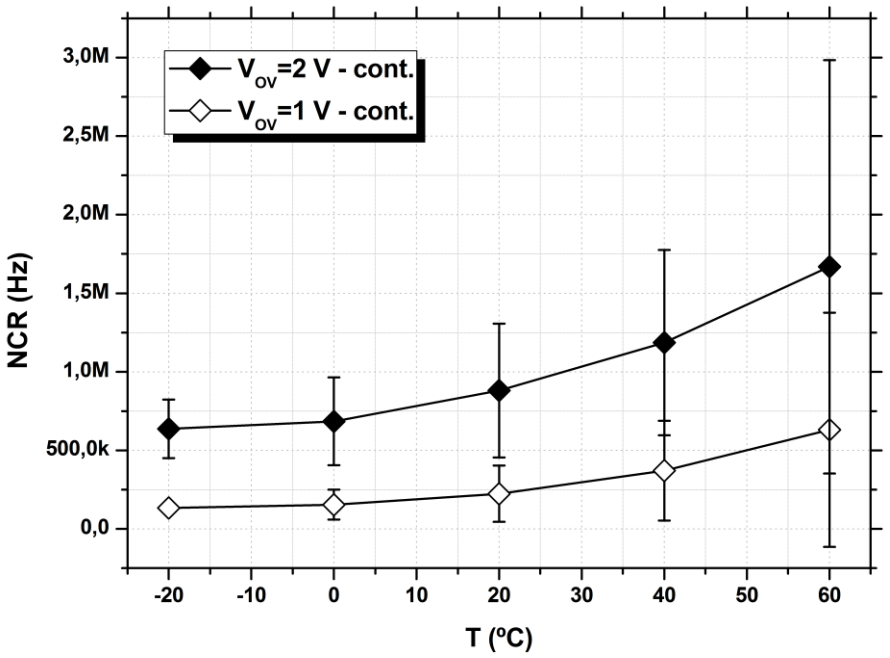

Figure 4.14 NCR dependence on the temperature with the standard deviation at 1 V and 2 V of V_{OV}.

reduced in almost two orders of magnitude throughout the measured temperature range. The DCR was measured also in the dark within the temperature range between -20 ºC and 60 ºC at two different V_{OV} of 1 V and 2 V. During the measurement, the gated-on and gated-off periods were set at 14 ns and 1 µs, respectively. The number of repetitions was $1 \cdot 10^6$ times and therefore the total measuring time was also 14 ms for each of the points analyzed. Fig. 4.15 shows a comparison between the mean NCR and mean DCR across all the pixels, obtained in the continuous and time-gated modes respectively, as a function of the temperature. When the detector is operated in the time-gated mode, the mean DCR at a reverse bias overvoltage of 1 V ranges from 9.8 kHz at -20 ºC to 350 kHz at 60 ºC. In contrast, these figures are increased to 23.9 kHz and 819 kHz, respectively, when a reverse bias overvoltage of 2 V is used. These numbers indicate a remarkable decrease in the sensor noise when this is operated in the time-gated mode to suppress the afterpulses. Moreover, the values obtained for the DCR show a reduction by a factor of 2 every 10 ºC, which matches well with the theory. In contrast, the NCR shows a weak dependence on the temperature, especially below 0 ºC. The change in the slope of the NCR at temperatures exceeding 0 ºC suggests that thermally generated carriers are the main contributors to the NCR at high temperatures, while afterpulses dominate at lower temperatures. The results obtained with the time-gated operation are fairly good values for GAPDs of this size fabricated in a conventional CMOS technology. When scaled to DCR/µm^2, they are in good agreement with other GAPDs fabricated with the same technology, as for example [15]. The thermal dependence of the crosstalk has not been investigated in this work. However, a decrease of this noise source with the temperature can be foreseen. At low temperatures, the DCR is low. Moreover, the e^--h^+

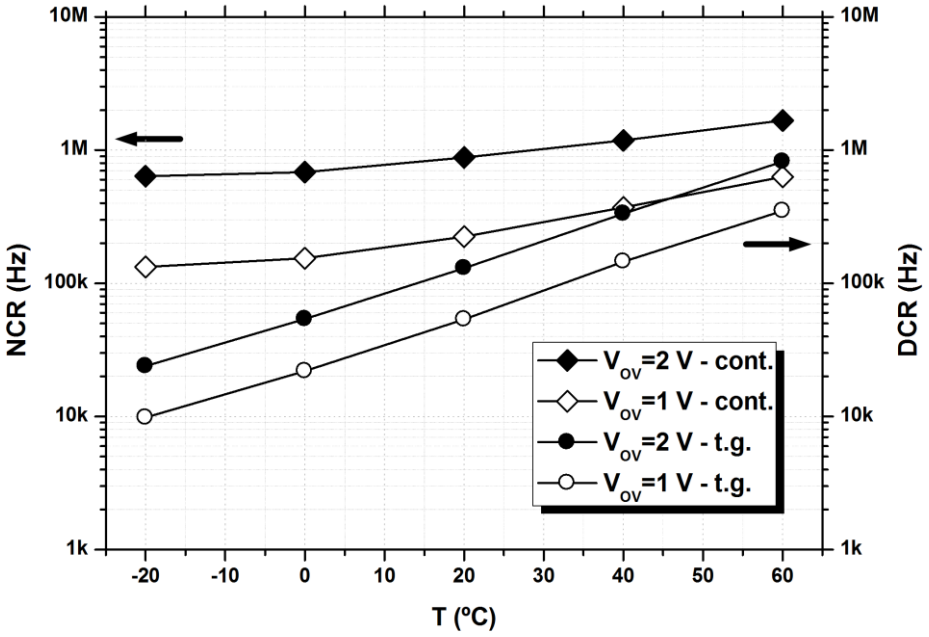

Figure 4.15 NCR (in continuous mode) and DCR (in time-gated mode) as a function of the temperature at 1 V and 2 V of V_{OV}.

ionization coefficients also loose some efficiency at low temperatures. Therefore, the number of crosstalks should decrease with the temperature.

The measured DCR can be analyzed into more detail to extract some parameters of the technology, such as the activation energy or E_a, and check if they match the theory. The SRH contribution to the DCR can be expressed through the well known equation

$$DCR \cong T^{1.5} \cdot \exp\left(-E_g / 2k_B T\right) \tag{4.3}$$

where T is the absolute temperature, E_g the bandgap energy and k_B the Boltzmann constant. Because of the exponential factor, it is generally useful to plot the natural logarithm of the measured DCR as a function of $1/k_BT$, i.e. to plot the DCR variation versus the temperature in an Arrhenius plot. The resulting slope of this plot provides an activation energy for the change in the DCR with the temperature. At those temperatures in which the thermal generation of carriers dominates the DCR, E_a should be close to $E_g/2$ (0.56 eV in the case of silicon). In contrast, when tunneling is the prevailing mechanism, a much smaller E_a as a sign of a much weaker temperature dependence is to be expected. In the case of the 10 x 43 GAPD detector, the experimental results match well with the theory. Hence, activation energies of 0.413 eV and 0.398 eV were extracted from the Arrhenius plot between 60 ºC and 10 ºC at 1 V and 2 V of V_{OV}, respectively (see Fig. 4.16). Alternatively, the extracted activation energies drop to 0.134 eV and 0.155 eV between 10 ºC and -20 ºC.

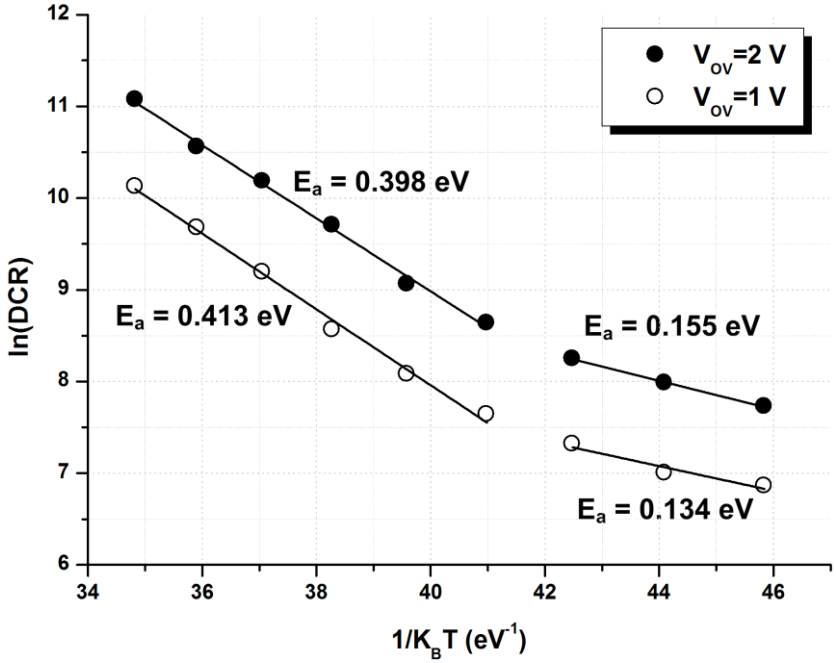

Figure 4.16 Arrhenius plot of the DCR and extracted activation energies.

Considering the results obtained for the NCR, if the GAPD detector is operated in the continuous mode 1 noise count is expected each 1.5 μs at 1 V of overvoltage and 60 ºC of temperature (NCR=630 kHz). In this regime, the reduction of the working temperature does not significantly reduce the noise problem, given that at -20 ºC 1 noise count will still be generated each 7.5 μs (NCR=132 kHz). This means that, even reducing the working temperature, 125 noise counts/GAPD/train or 0.1 noise counts/GAPD/train would be generated at ILC and CLIC, respectively. Given the long bunch-spacing of 337 ns at ILC, at this particle collider the GAPD detector can be operated in the time-gated mode to eliminate the afterpulsing probability and extract the content of the pixels after each BX. Although the characterization of the GAPD detector as a function of the temperature was performed with a gated-off period of 1 μs, which is not compatible with the synchronous operation between the GAPD detector and the bunch train structure at ILC, this long gated-off period is a limitation of the data acquisition system and not of the detector itself. The detector can be read out during a gated-off period of less than 300 ns. In the final prototype, a data acquisition system that allows to fully exploit the capabilities of the GAPD detector should be used. Thus, the values for the expected noise have been calculated assuming this hypothesis. The DCP is $\sim 3 \cdot 10^{-3}$ noise counts/GAPD/BX with a gated-on period of 10 ns at 1 V of overvoltage and 60 ºC of temperature (DCR=350 kHz). When the detector is operated at -20 ºC, this figure can be reduced to $\sim 10^{-4}$ false counts/GAPD/BX if the same gated-on period is applied or even to $\sim 10^{-5}$ false counts/GAPD/BX with a gated-on period of 1 ns (DCR=9.8 kHz). These figures are summarized in Table 4.1.

T (ºC)	NCR/DCR (kHz)	Expected noise counts	
		ILC (2820BX, 337 ns)	**CLIC (312 BX, 0.5 ns)**
60	630 (NCR)	598 n.c./GAPD/train	0.1 n.c./GAPD/train
	350 (DCR)	$3 \cdot 10^{-3}$ n.c./GAPD/BX (t_{obs}=10 ns) $3 \cdot 10^{-4}$ n.c./GAPD/BX (t_{obs}=1 ns)	– –
-20	132 (NCR)	125 n.c./GAPD/train	0.02 n.c./GAPD/train
	9.8 (DCR)	10^{-4} n.c./GAPD/BX (t_{obs}=10 ns) 10^{-5} n.c./GAPD/BX (t_{obs}=1 ns)	– –

Table 4.1 Expected noise counts at ILC and CLIC as a function of the temperature at 1 V of V_{OV}.

As explained in Chapter 2, the PDP depends on the quantum efficiency, the avalanche breakdown probability and the fill-factor of the device (defined in Eq. 2.17). As the temperature is lowered, the impact ionization rate (see Fig. 4.17) and thus the avalanche breakdown probability (see Fig. 4.18) are decreased. Moreover, the electric field across the multiplication region is also reduced. These factors make it more difficult for charge carriers to trigger an avalanche [18], which results in the slow decrease of the PDP over the whole temperature range [19]. Apart from that, the absorption coefficient $\alpha(\lambda)$ is increased with higher temperatures (see Fig. 4.19). As a consequence, the peak wavelength is shifted to lower wavelengths as the temperature decreases [20] (see Fig. 4.20).

The detection capabilities of the 10 x 43 GAPD array as a function of the temperature were tested at a fixed wavelength with different light intensities emitted by a 880 nm LED. The 880 nm LED was placed outside the climatic chamber in order to avoid variations in its behavior due to temperature changes. The emitted light reached the GAPD array through a transparent window. As expected, the decrease of the signal counts generated by the sensors over the measured temperature range is low (<7% in the worst case). The obtained results are plotted in Fig. 4.21.

4.2.8 Radiation effects

The beam-beam interactions generate backgrounds that are potentially problematic for the detector. The main sources of such backgrounds are on the one hand e+e− pairs and photons due to the beamstrahlung process, and on the other hand neutrons created from off energy e+e− pairs and disrupted beam in addition to neutrons created in the beam dumps that are backscattered into the detector [21]. The e+e− pairs impose a requirement on radiation hardness of up to 1 kGy/year at ILC and 200 Gy/year at CLIC. The neutron background is estimated to be

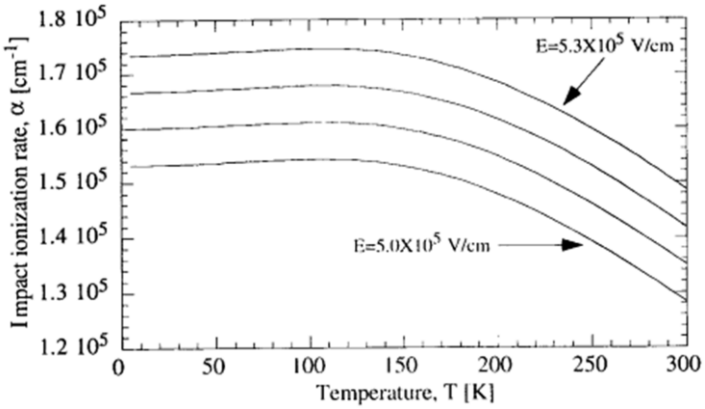

Figure 4.17 Impact ionization rate α as a function of the temperature T_A with the electric field E as a parameter [16].

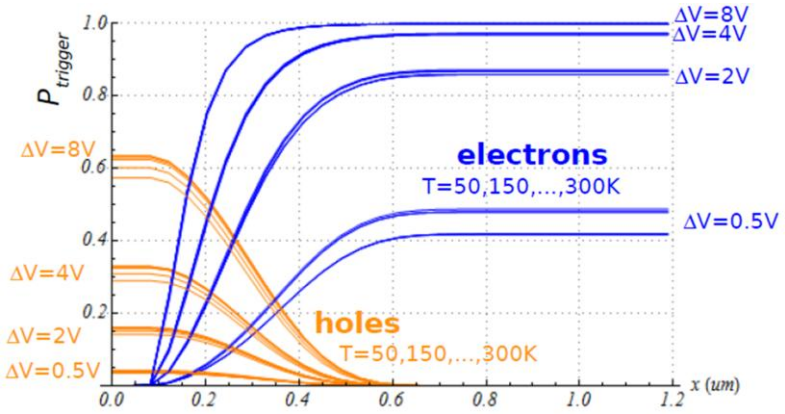

Figure 4.18 Avalanche triggering probability for electrons and holes [17], obtained by using the differential equations method after [18].

at the level of 10^{11} n_{eq}/cm^2/year at ILC and 10^{10} n_{eq}/cm^2/year at CLIC. Detectors at ILC and CLIC are expected to have a useful lifespan between 5 and 10 years.

The way in which radiation interacts with matter depends on the characteristics of both the incident particle and the target material [22]. In semiconductors and insulating materials, electrons and photons are responsible for ionization effects, i.e. they create electron-hole pairs along their path. The number of pairs created is proportional to the quantity of energy deposited in the material, which is expressed through the total absorbed dose or TID (Total Ionizing Dose). This parameter is also called IEL (Ionizing Energy Loss). In contrast, neutrons give origin mainly to nuclear displacement, which generates a neighboring interstitial atom and vacancy before they recombine within a very short time. A major effect of nuclear displacement is the reduction of the minority carriers lifetime in the semiconductor bulk. Moreover, absorbed neutrons can induce the emission of protons, α particles and γ photons. The damage generated by neutrons is usually called NIEL (Non-Ionizing Energy Loss). Protons, which in principle are not expected at the future linear colliders (at least not as primary particles), induce ionization

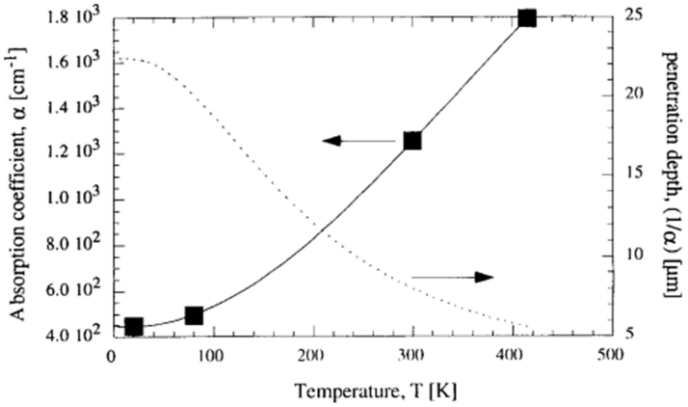

Figure 4.19 Measured absorption coefficient α(■) and fitted α (solid line) versus temperature [16].

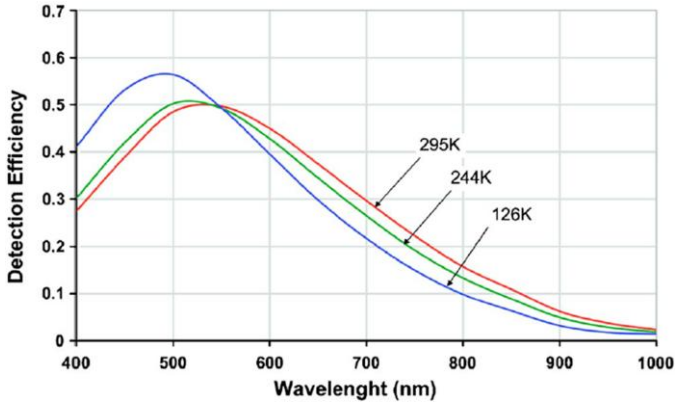

Figure 4.20 Variation of the quantum efficiency for different working temperatures [20].

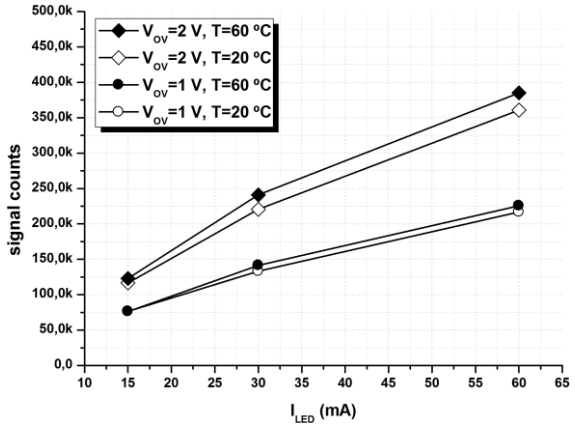

Figure 4.21 Measured signal counts as a function of the LED intensity.

effects and nuclear displacement as well. Ionization effects and nuclear displacement may be caused directly by the incident particle or from secondary phenomena induced by the first. A detailed summary of the type of interaction between radiation and matter and the induced phenomena as a function of the incident particle and its energy is presented in Table 4.2.

GAPD detectors are inherently susceptible to radiation damage. The predominant effects are the increase of the sensor intrinsic noise and the misfunction of the readout electronics.

Concerning the sensor, both IEL and NIEL phenomena increase the DCR and afterpulsing probability since they introduce new recombination-generation trapping centers in the multiplication region and elsewhere. A GAPD detector array that contains radiation tolerant readout circuits and fabricated in the HV-AMS 0.35 μm CMOS process has been irradiated with γ rays and protons, as reported in [23]. According to this reference, the DCR is increased by a factor 3-4 with a γ ray irradiation dose of 10 kGy, which is the expected dose at ILC after 10 years operation. Thus, the DCR of 9.8 kHz, measured at 1 V of V_{OV} and -20 ºC of working temperature, would be risen to 36.45 kHz at the end of the ILC lifespan. In this situation, the DCP would be $\sim 3 \cdot 10^{-4}$ noise counts/GAPD/BX with a gated-on period of 10 ns. At CLIC, in contrast, a softer radiation dose of 2 kGy is foreseen after 10 years operation. The sensor noise would be risen by a factor 2. As a consequence, the NCR of 132 kHz, measured also at 1 V of V_{OV} and -20 ºC of working temperature, would be risen to 234 kHz. This yields 0.04 noise counts/GAPD/train. Irradiation measurements with protons are also reported in [23], but not with neutrons. The measurements indicate a DCR increase by a factor ~45 after a proton irradiation with a fluence of $8.3 \cdot 10^7$ p/cm^2/s (flux of 11 MeV and dose of 40 krad). Although irradiation measurements with neutrons on GAPD detectors fabricated in standard technologies have never been published, the damage induced by neutrons is believed to be similar to that induced by protons, as stated in [24].

The readout electronics, in contrast, is more sensitive to ionization effects than to displacement damage. Because the operation of MOS transistors is based on minority carriers transport near the surface, the influence of neutron irradiation on these devices is almost imperceptible. Ionizing radiation has consequences on the electrical parameters of MOS transistors such as the shift of the threshold voltage, the increase of leakage currents and the decrease of the mobility and the transconductance.

There still exists one last type of damage induced by radiation on integrated circuits, which is called SEE (Single Event Effect). SEEs are caused by highly energy particles, typically neutrons, protons or pions above a certain threshold energy about 20 MeV [25], which traverse the electronics and generate an immediate malfunctioning of one or more transistors. The generated errors, which can influence the entire circuit, can be reversible (called soft errors) or non-reversible (called hard errors). SEUs (Single Event Upsets), the most common apparition of soft SEEs, are induced by the impact of incoming particles, such as heavy ions, and the subsequent deposit of charge on a critical node of sequential or combinatory circuitry. As a consequence, a bit-error is generated (i.e. the logic state of the cell is flipped from a logical ‘1’ to a logical ‘0’ or vice versa) until the cell is overwritten. For each device there is a minimum charge quantity, called critical charge, which is able to generate a SEU. In contrast, SEL (Single Event Latch-up), the most important hard SEE, is the radiation-induced latch-up of CMOS

Particle	Energy (eV)	Radiation-matter interaction	Phenomena
Electrons	–	Coulomb interaction	Ionization
	–		Atomic excitation
	–	Scattering with the nuclei	Nuclei's displacement
	–	e− decelerated in the material	Emission of X-rays
Photons	–	Photoelectric effect	Emission of photons
	≤ 1.024 M	Compton effect	Emission of γ rays
	–	Absorbance	Ionization
Neutrons*	< 1 (slow)	Nuclear reaction	Emission of protons, α particles and γ photons
	< 1 (slow) > 100 k (fast)	Elastic collision	Nuclei's displacement
	Very high energies	Inelastic collision	Nuclei's displacement and emission of γ rays
Protons	–	Coulomb interaction	Ionization
	< 100 k		Atomic excitation
	–	Collisions with the nuclei	Nuclei's excitation
	1-100 M		Nuclei's displacement
	> 10 M	Nuclear reaction	Emission of protons, α particles and γ photons

Table 4.2 Radiation-matter interaction and induced phenomena as a function of the incident particle and its energy. * Neutrons are divided into slow (< 1 eV) and intermediate and fast (> 100 keV).

circuitry. It occurs when an ionizing particle strikes the substrate of a CMOS circuit causing a low impedance path between power and ground within the device, thus allowing for a sudden current flow which can be destructive if not interrupted promptly.

The tolerance to radiation of GAPD sensors stands as it is and it cannot be improved at the design level. In contrast, standard CMOS circuits can sustain high doses of radiation if certain measures are adopted. To start with, the natural trend in device scaling of standard CMOS technologies improves their tolerance to ionizing radiation. State-of-the-art standard CMOS technologies present such a reduced gate oxide thickness that the threshold voltage shift and the degradation of the mobility and the transconductance become negligible even after doses of several hundreds of Gy. Moreover, leakage currents, SEUs and SEL can be mitigated by introducing some special techniques at the circuit and layout levels. Leakage currents, present in nMOS transistors only, can be mitigated by implementing nMOS ELTs (Enclosed Layout Transistors), in which the parasitic path that connects the drain and source diffusions is eliminated [22, 23, 26, 27]. Leakage currents between n^+ implantations from different components can be prevented by using p^+ guard rings to separate them. SEU tolerant circuits can be obtained by using special circuit architectures to restore data when flipped by an ion hit,

such as those that are provided with an appropriate feedback, implement techniques for the detection and correction of errors or use TMR (Triple Modular Redundancy). SEL phenomena can be minimized with the extensive use of n^+ and p^+ guard rings around pMOS and nMOS transistors. However, the solutions to improve the radiation tolerance of CMOS circuits present some drawbacks that may be critical in the present application, such as the larger area consumption. ELT transistors are also characterized by slower switching times, as well as limitations and difficulties in the choice and modelization of the W/L ratio.

Although irradiation facilities with ^{60}Co gamma photon and neutron radiation, such as the TRIGA-Mark-III reactor of Ljubljana [28], were considered for an irradiation campaign, the GAPD detector presented here has not been irradiated. Nevertheless, an increase of the DCR and afterpulsing probability is to be expected after irradiation, as mentioned above. Apart from that, because the GAPD detector is a first prototype, it is not optimized for performance. Thus, techniques to mitigate the radiation effects on readout circuits, such as nMOS ELTs, special readout circuits to avoid SEUs or additional guard rings, were not introduced in the design so as to minimize the risk of circuit failure and maximize the sensitive area of the detector. The feasibility to investigate the detector performance at a beam-test was prioritized over other features. However, the techniques mentioned should be definitely introduced in the design of a second prototype, which should be irradiated to have first hand information about the behavior of the detector in a harsh radiation environment such as ILC and CLIC. Several devices should be irradiated using different steps with incremental dose, until reaching the levels expected at the future linear colliders. Moreover, since the degradation of the circuits depends on the bias conditions during irradiation, some of the devices should have all the terminals short-circuited to ground and some others should be biased as in usual operation. Annealing effects should also be investigated.

4.2.9 Power consumption

In CMOS integrated circuits, the power consumption is mainly caused by static and dynamic power components. The static power consumption is the current that flows through the circuit when this one is holding a value, i.e. not switching. It is determined by the formula

$$P_S = I_S \cdot V_{DD}, \tag{4.4}$$

where I_S is the total current that flows through the circuit and V_{DD} the supply voltage. It is composed by all the undesired currents in the circuit due to non-idealities, such as reverse biased p-n junctions or subthreshold leakages. Typically, CMOS technologies do not present

any static power consumption, although this component becomes significant with the scaling of the technology node. The dynamic power consumption occurs every time there is a change of logic state, i.e. from '0' to '1' or vice versa. In this case, the consumption is caused by the power required to charge or discharge the load capacitance. It can be expressed as

$$P_D = C_L \cdot V_{DD}^2 \cdot f \tag{4.5}$$

where C_L is the load capacitance, V_{DD} the supply voltage and f the frequency of operation. As it can be inferred from Eq. 4.5, the dynamic power consumption increases as the frequency of operation does. This component is responsible for the main contribution to the power dissipation in CMOS circuits.

The power consumption of the 10 x 43 GAPD detector was measured by reading directly at the voltage source the current that flows through the entire detector. When the detector was unbiased (i.e. V_{HV}=GNDA=V_{DD}=V_{SS}=0 V), the power consumption was measured to be null, as it should be in a technology without leakage dissipation such as HV-AMS 0.35 μm. Moreover, when the detector was biased at a positive voltage below V_{BD} (i.e. V_{HV}<V_{BD}+1.1 V, GNDA=1.1 V, V_{DD}=3.3 V, V_{SS}=0 V), the power consumption was measured to be null as well, which indicates that GAPDs do not present any leakage dissipation either. Thus, it can be concluded that the detector has no static power consumption. In contrast, when the detector was biased at a certain V_{OV} above V_{BD} (i.e. V_{HV}>V_{BD}+1.1 V, GNDA=1.1 V, V_{DD}=3.3 V, V_{SS}=0 V), the power consumption was measured to be nonzero due to the state transitions of the circuit. This power consumption, i.e. the dynamic dissipation, is caused by the in-pixel readout circuits and mostly by the output pads of the chip, as it will be demonstrated in the following lines.

The dynamic power consumption and the DCR of the GAPD detector were measured in the dark with 5 different chips. The DCR was measured because it is an indicator of the frequency of operation of the circuit. During the measurements, the GAPD arrays were operated with fixed gated-on and gated-off periods of 4 ns and 1 μs, respectively. The number of repetitions was $100 \cdot 10^6$ times and therefore the total measuring time was 0.4 s. To obtain several data pairs of power consumption versus DCR, different reverse bias overvoltages that range from 0.8 V to 2.4 V in steps of 0.2 V were used. The dynamic power consumption as a function of the average DCR across all the pixels of the 5 chips is plotted in Fig. 4.22. It can be observed in this figure that the dynamic dissipation increases from 123 mW to 183 mW as the DCR does. Nevertheless, at very high DCRs, the power consumption decreases to 154 mW. This is a consequence of the way in which the detector is read out, as it will be explained next.

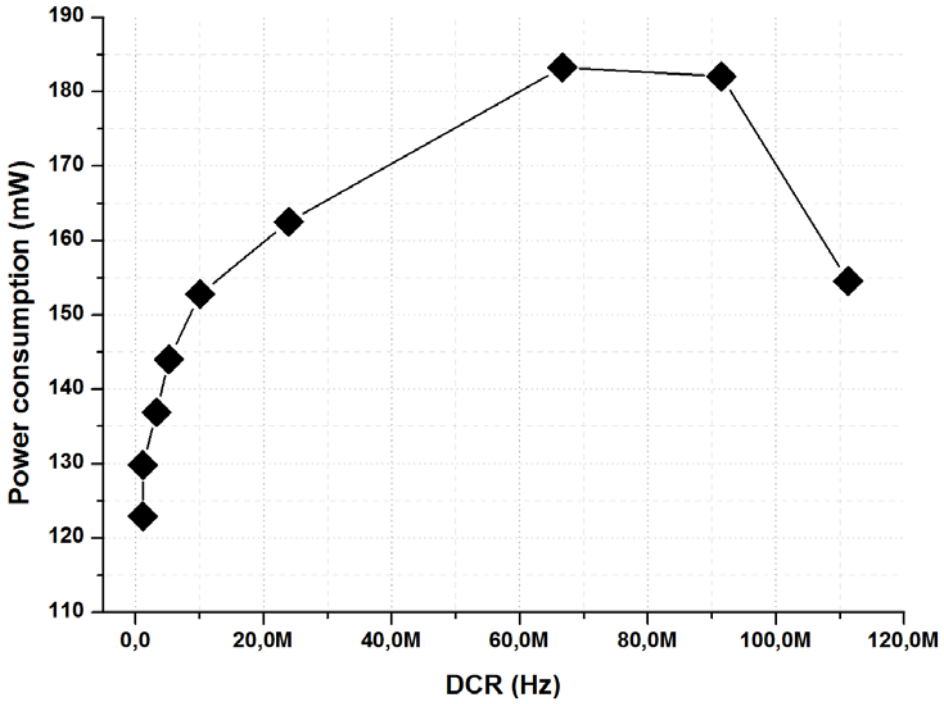

Figure 4.22 Measured power consumption as a function of the DCR.

The present GAPD detector is read out sequentially by rows, without resetting the output column line between the readout of two consecutive rows. Thus, if one pixel of a certain row and column has the same output value (e.g. pixel from row 4 and column 21, with '1' as output value) as the pixel from the same column of the previous row (e.g. pixel from row 3 and column 21, with '1' as output value), the output pad does not switch its state. Therefore, the readout of this particular pixel does not present any dynamic dissipation at the pad level. Qualitatively speaking, when few pixels are fired, such as in the case of event detection with a faint input signal, only a few pixels give a logical '1' as an answer and the switching frequency of the output pads is low. Consequently, the dynamic power consumption is low too. With an increasing number of activated pixels, the switching frequency of the output pads also increases and so does the dynamic dissipation. But if most of the pixels are activated, as it happens in the case of a very intense input signal, the large majority of the pixels give a logical '1' as an answer and the switching frequency of the output pads is low again. As a result, the dynamic dissipation decreases.

The measured dynamic consumption of the present GAPD detector can be expressed as

$$P_{D,measured} \cong DCR \cdot t_{obs} \cdot n_{rep} \cdot 430 \cdot \left(P_{D,circuit} + P_{D,pad}\right) \tag{4.6}$$

where $DCR \cdot t_{obs} \cdot n_{rep} \cdot 430$ is approximately the number of transitions at a certain reverse bias overvoltage, $P_{D,circuit}$ the dynamic consumption per readout circuit and $P_{D,pad}$ the dynamic consumption per output pad. From Eq. 4.6, and knowing the number of transitions and the

dynamic consumption per output pad, it it possible to deduce the dynamic consumption per readout circuit. However, Eq. 4.6 is only true for those reverse bias overvoltages where the number of noise counts matches the number of transitions at the output pads. At low reverse bias overvoltages, there may be more transitions than noise counts (e.g. if the output value of one pixel is '1' and the output value of the next pixel is '0'). In contrast, at high reverse bias overvoltages, the number of transitions tends much lower than the number of noise counts, as most of the pixels are fired. At a reverse bias overvoltage of 1.2 V, the number of noise counts is believed to match quite well the number of noise counts. Thus, according to the measured data, the dynamic consumption and the number of transitions at 1.2 V are 0.137 mW and $4.52 \cdot 10^8$, respectively. The dynamic consumption per output pad is 295 μW/MHz, according to the information supplied by the foundry [29]. In these conditions, Eq. 4.6 yields a dynamic consumption per readout circuit of 8 μW/MHz. This value is in fairly good agreement with the simulated dynamic dissipation of the readout circuits, which is 10 μW/MHz. Moreover, in the same conditions, the total dynamic dissipation of the output pads is 133 mW (97% of the total), while the readout circuits contribute with only 4 mW (3% of the total).

As just shown, the power consumption of the present GAPD detector is high, which may limit the suitability of integrating a larger array of 32 x 32 or 64 x 64 or even more pixels. Nevertheless, the most part of the dissipation is caused by the output pads. This contribution could be severely decreased by using an LVDS (Low-Voltage Differential Signaling) pad, which would ensure large arrays with reasonable power consumptions.

4.3 High energy particle detection

Although the extraordinary capabilities of GAPDs in photon detection are widely known [30], the performance of these sensors in particle detection has been investigated here for the first time under the framework of the project FPA2010-21549-C04-01 funded by the Spanish National Program for Particle Physics. At current time, three beam-tests have already been performed. The first two beam-tests were at the SPS area of CERN between June and October 2012. The particle beam used for the characterization consisted in 120 GeV pions. The third and last beam-test took place in July 2013. Because of the long shutdown of CERN, planned between the early 2013 and 2015, the third beam-test took place at DESY. In this case, a 6 GeV electron beam was used. The set-up for the beam-test of the GAPD technology, together with the results obtained, is described next.

A schematic diagram of the set-up for the GAPD beam-test is depicted in Fig. 4.23. The set-up is comprised of one DUT (Design Under Test), a reference system consisting of one

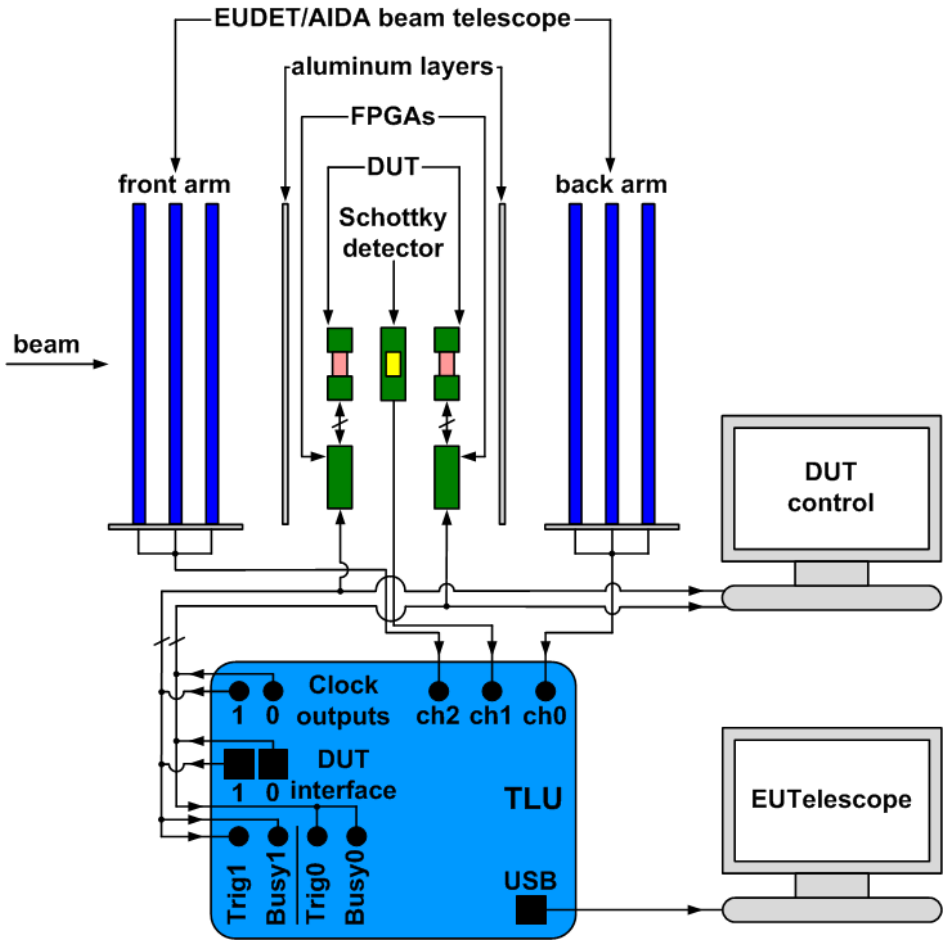

Figure 4.23 Schematic diagram with the DUTs and the satellite electronics for the test beam. The different elements are not to scale.

Schottky detector and an EUDET/AIDA beam telescope, and a TLU (Trigger Logic Unit) which is used to distribute the trigger signal. The scope of this experiment is to test whether the GAPD technology detects high energy particles and, if so, determine the efficiency of the technology and study the different areas of sensitivity of the sensor. Moreover, in an attempt to test the efficiency of the GAPD technology in particle tracking, the DUT is comprised of two GAPD detector arrays. This arrangement also allows to discriminate the signal from the sensor noise by particle sampling at the two layers. Each GAPD detector array is allocated in a PCB and controlled by an ALTERA Cyclone IV FPGA-based control board. The Schottky detector is allocated in a third PCB. The PCBs with the two GAPD detector arrays and the Schottky detector are in a metallic box (also referred to as the mechanics), which is used to fix and align the devices (see Fig. 4.24). The mechanics also serves to protect the sensors from uncontrolled light sources.

A schematic diagram of the GAPD array board together with the FPGA control board is shown in Fig. 4.25. A picture of the fabricated devices is presented in Fig. 4.26. In an attempt to reduce the multiscattering in the particle path, no packages are used and the naked die is wire

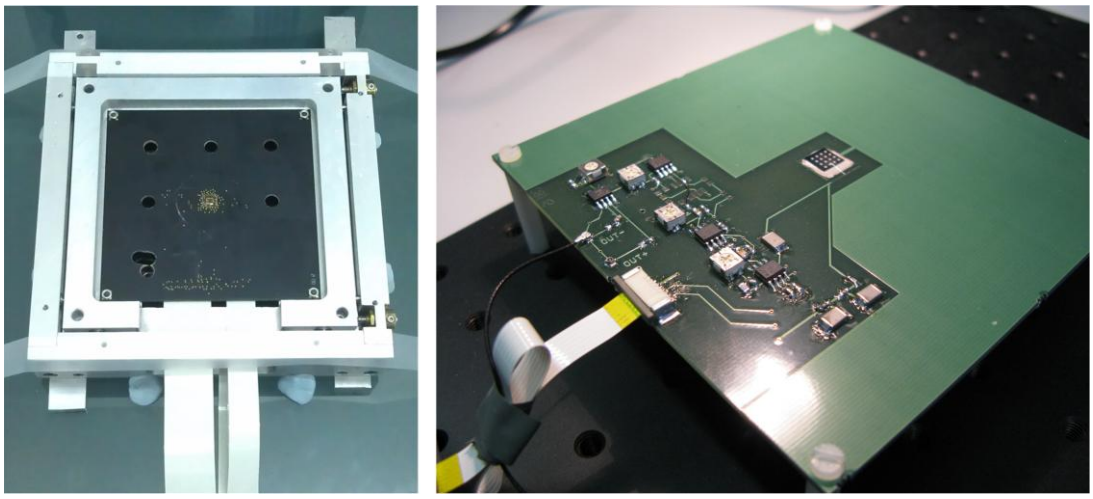

Figure 4.24 Mechanics (left) and Schottky detector (right). The top layer of the mechanics corresponds to the first PCB with its GAPD array.

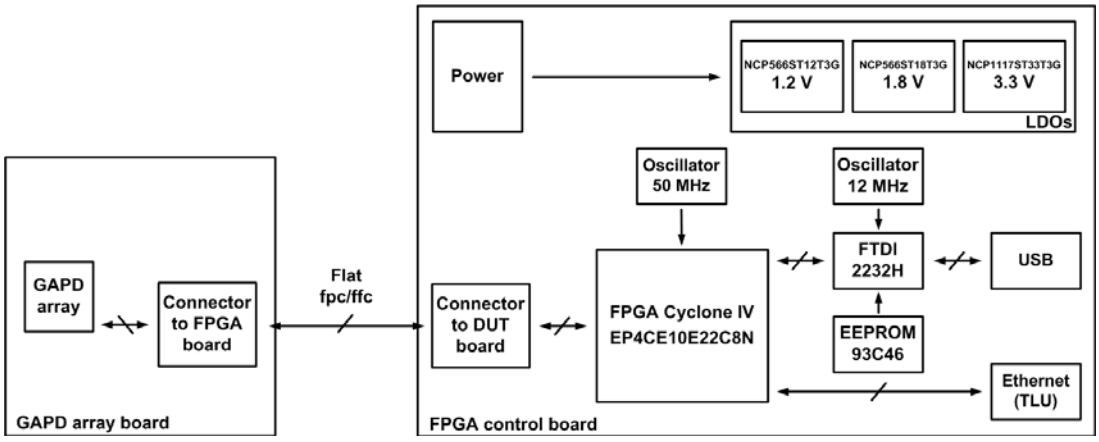

Figure 4.25 Schematic diagram of the GAPD array (left) with the FPGA control board (right).

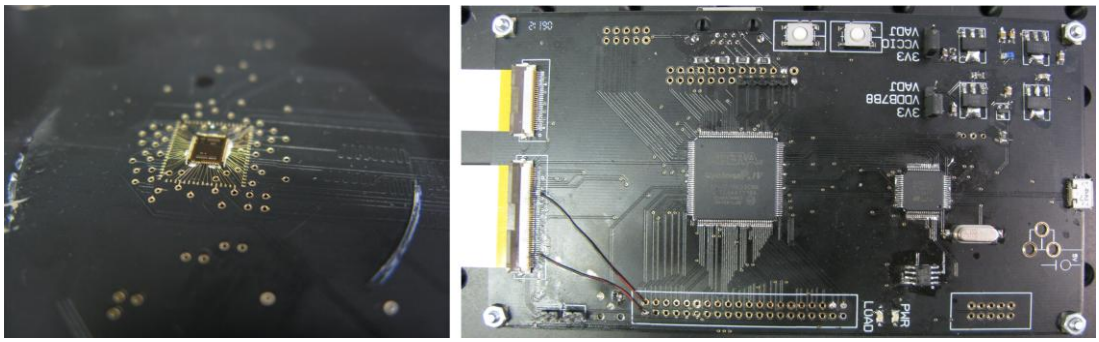

Figure 4.26 Photo of the GAPD array (left) with the FPGA control board (right).

bonded directly to the board. The board is then perforated under the chip. Moreover, the die of the GAPD detector is thinned down to 250 µm. The FPGA control board comprises an ALTERA Cyclone IV FPGA, an FTDI chip for data transmission, an EEPROM memory, a USB connector for communication with a computer and an Ethernet connector for communication with the TLU. A power system with different voltage regulators is used to power the

components of the board. Two oscillators that generate clock signals at 12 MHz and 50 MHz are used by the FTDI chip and the FPGA, respectively. The data transmission between the GAPD array board and the FPGA control board is done through a flat fpc/ffc cable. The FPGAs are used to generate the control signals of the detector (RST, INH, CLK1 and $CLK2_m$, where m is the index that identifies the rows of the matrix) and also to count the number of pulses generated by the sensor. Because the GAPD detector is operated in a time-gated mode, and therefore the sensors are not always active, an appropriate duty cycle given by the ratio between the gated-on period and the sum of the gated-on and gated-off periods and programmed by the FPGA is chosen so as to facilitate the observation of particle counts without seriously increasing the fake hit probability. The generated pulses are stored in an internal FIFO of the FPGA which has a programmable capacity. The number of frames to be stored by the FIFO is selected depending on the delay between the real event and the trigger signal distributed by the TLU (see Fig. 4.27 for a schematic temporal diagram). Moreover, the FPGAs also handle the TLU control signals. In this set-up configuration, a minimum gated-off period of 1.75 μs was necessary to read and store each frame, although it was later reduced to 700 ns. A minimum delay of 27.3 ± 3 ns is set by the transmission wires. One single FPGA could be used to control both GAPD arrays, but a solution based on two FPGAs has been chosen in this work. The FPGAs are not aligned with the GAPD arrays.

To characterize the performance of the GAPD technology during the beam-test, it is also necessary to determine with a reference system the tracks of the high energy particles with great accuracy. The resolution of the reference system has to be higher than the expected intrinsic resolution of the DUT. This is usually achieved with beam telescopes, which are placed in the beam-test together with the DUT. Thus, it is possible to measure the tracks of the particles and study the response of the DUT at the same time. In this work, an upgrade of the EUDET/AIDA beam telescope with six reference planes subdivided into two arms is used for this purpose. The telescope has a sensitive area of 5 x 5 cm^2 and a spatial resolution around 4.5 μm per plane. The mechanics that contains the DUT and the Schottky detector is allocated between the two arms of the telescope. The mechanics is 100 μm thick on each side. Remote-controlled stages help to spatially align the telescope with the DUT. Nevertheless, the sensitive area of the telescope is much higher than that of the DUT. As a consequence, another element is needed to discriminate between the hits that occur in the overlapped DUT-telescope area from those ones that occur outside this region. In this work, a Schottky detector [31] of 1 mm in diameter and 300 μm thick is used. The Schottky detector is arranged in a PCB of 1.6 mm thick and placed between the two dies in the mechanics.

A TLU [32] is used as interface between the EUDET/AIDA telescope, the GAPD detectors and the data acquisition system. The TLU is operated under the trigger data handshake, in which

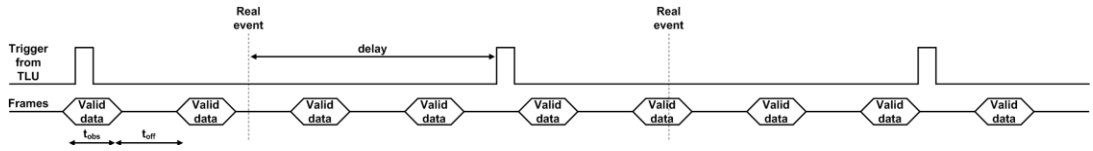

Figure 4.27 Schematic temporal diagram of the procedure used to save the data that corresponds to real events.

data is transferred from the TLU to the FPGAs on each trigger. The TLU receives trigger signals from both the front and back arms of the telescope (1 signal per arm) as well as the Schottky detector. The output nodes of these devices are connected to three different input channels of the TLU, which are then fed into an AND logic gate. Upon trigger coincidence between both arms of the telescope and the Schottky detector (i.e. the output of the AND logic gate is set to '1'), the TLU asserts the TRIGGER output signal. In response, the FPGAs force the TLU BUSY input signal to '1'. In reception of the BUSY signal going high, the TLU de-asserts the TRIGGER signal and the FPGAs send 16 TRIGGER-CLOCK pulses. The pulses are counted by the TRIGGER line, whose pin has been switched to the output of a shift register holding the trigger number. Within the 16 TRIGGER-CLOCK pulses, the TLU sends the 16 bits of the time-stamp to the FPGAs. The time-stamp together with the current content of the FIFOs is transferred to a computer via an FTDI chip and a USB cable. Simultaneously, the six frames that correspond to the six arms of the telescope for the same time-stamp are stored in a second computer. This second computer is equipped with EUtelescope [33], the software of the EUDET/AIDA beam telescope. In the last place, when the writing data is complete, the BUSY signal is set low and the system is ready for triggers again.

The software EUtelescope reconstructs the particle trace through the six planes of the telescope with an intrinsic resolution between 2 and 3 μm. The interpolation of this trace should allow to determine through which pixel of the DUT, or even through which specific area of a certain pixel, the particle has passed. However, the different materials of the beam-test set-up can introduce scattering phenomenon that deviate the particle path. As a consequence, the interpolation of a particular trace is affected by a certain degree of uncertainty. This uncertainty limits the reconstruction of the particle trace through the DUT. In the worst case, when there is a particle entrance but not an exit, it becomes impossible to determine which pixel of the DUT has been hit.

In order to determine in advance the expected extent of the multiscattering phenomenon, which can hinder or impede the reconstruction of the traces if not minimized, it is mandatory to simulate the passage of particles through the materials of the beam-test set-up. However, the complete response of a given semiconductor to an energy electron beam is difficult to predict because of the many physical effects that can occur (probabilistic domain). Nevertheless, the

Geant4 (for Geometry And Tracking) software [34, 35], developed at CERN, can be used to predict all these interactions. Both the semiconductor geometry and thickness are key input parameters for Geant4. The amount of electron-hole pairs produced by incident electrons can be obtained using Monte Carlo simulations over the whole electron energy range. In this work, two set-ups have been studied. In the first case, the set-up analyzed includes all the different materials that can introduce scattering in the particle path. These materials are two aluminum layers of 100 μm thick each (in grey in Fig. 4.28-a), two GAPD detectors of 250 μm thick each (in orange in Fig. 4.28-a), one Schottky detector of 300 μm thick (in yellow in Fig. 4.28-a) and three PCBs of 1.6 mm thick each (in green in Fig. 4.28-a). The two aluminum layers correspond to the front and back sides of the mechanics. The three PCBs correspond to the two GAPD detectors and the Schottky detector. The distance between each one of these elements is taken to be 1 cm. The blue layer of Fig. 4.28-a corresponds to the first plane of the back arm of the beam telescope. Different distances of 2 cm and 10 cm between the back side of the box and the first plane of the back arm of the telescope have been simulated. In addition, to study the effects of the PCB and point out the importance of reducing the area of this material to the minimum, a second beam-test set-up, in which the PCBs have been removed, has also been characterized. The second beam-test set-up is depicted in Fig. 4.28-b.

The particles are launched from the front side of the beam-test set-up. For the analysis with Geant4, it has been considered that they are launched from a distance equal to the separation between the last plane of the front arm of the beam telescope and the front aluminum layer, which is either 2 or 10 cm in these simulations. The particles are launched with perpendicular momentum with reference to the aluminum layer. The particle sources are a 6 GeV electron beam at DESY and a 120 GeV pion beam at CERN.

The standard deviations of the hit distribution in the EUDET/AIDA beam telescope obtained with the simulations for the two proposed set-ups are presented in Table 4.3. As expected, the deviation of the particle track increases with the distance between the inner plane of the telescope and the aluminum layer. It also increases with the presence of more materials in the set-up. An intrinsic resolution of 9.37 μm can be achieved at DESY beam-test with the simplified set-up (Fig. 4.28-b) and a telescope-aluminum layer separation of 2 cm. If the complete set-up is used (Fig. 4.28-b), the maximum achievable resolution is reduced down to 17.69 μm. In addition, if the distance between the telescope-aluminum layers increases up to 10 cm, the maximum resolution is 26.02 μm for the simplified set-up and 50.01 μm for the complete one. These results outline the importance of reducing to the minimum the amount of materials used in the test set-up. Moreover, it is also clear that the telescope should be as near as possible to the aluminum box. However, given that the pixel width is 20 μm, it should be still possible to distinguish detection at pixel level. In contrast, at CERN beam-test with a telescope-

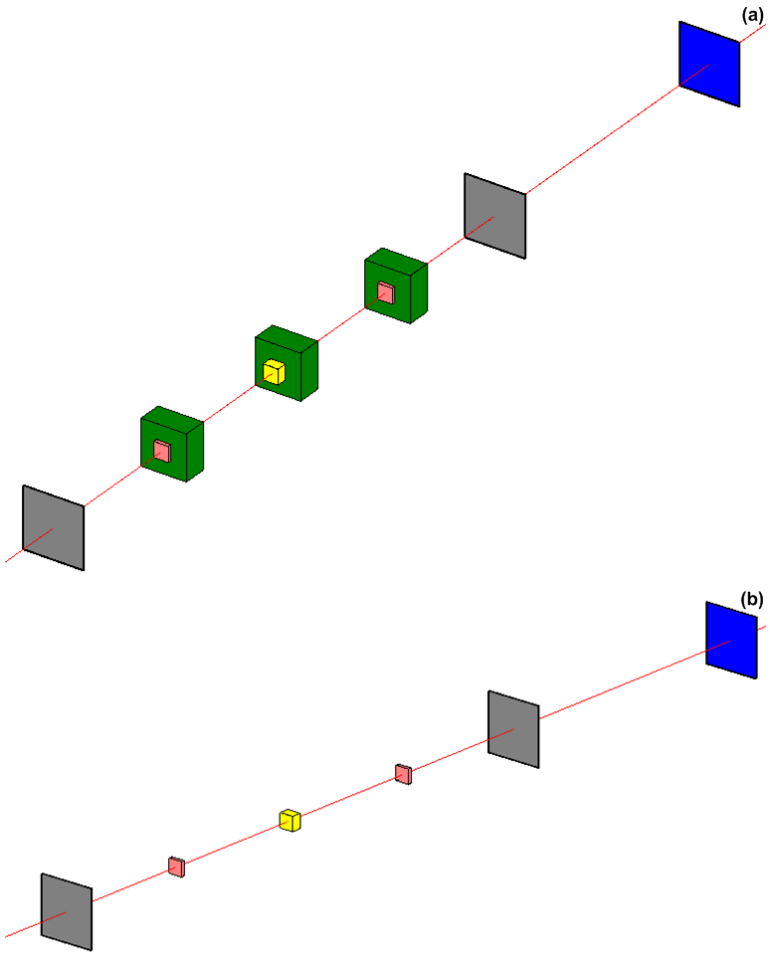

Figure 4.28 Schematic diagram of the set-up materials used in the Geant4 analysis, with complete (a) and simplified (b) versions [36].

Source	Electrons (6GeV)		Pions (120GeV)	
Distance (in cm)	2	10	2	10
Scattering (in μm, corresponding to set-up 4.28-a)	17.69	50.01	0.86	2.48
Scattering (in μm, corresponding to set-up 4.28-b)	9.37	26.02	0.45	1.23

Table 4.3 Expected standard deviations of the hit distribution at DESY and CERN beam-tests.

aluminum layer distance of 2 cm the deviation is under 1 μm for both studied set-ups. When the telescope-aluminum layer separation is increased up to 10 cm, the particle deviation is 1.23 μm and 2.48 μm for the simplified and complete set-ups, respectively.

The beam-tests at CERN allowed to check and improve the performance of the set-up proposed, as well as to verify that GAPD sensors can detect MIPs. The set-up used at the CERN beam-test is shown in Fig. 4.29. Due to technical problems during the beam-tests, it was not possible to obtain high statistics or measure the detection efficiency. Nevertheless, it was still possible to demonstrate that the GAPD technology can sense MIPs with a short gated-on period of 30 ns and low overvoltage of 1.2 V. Fig. 4.30 shows the correlation between the GAPD

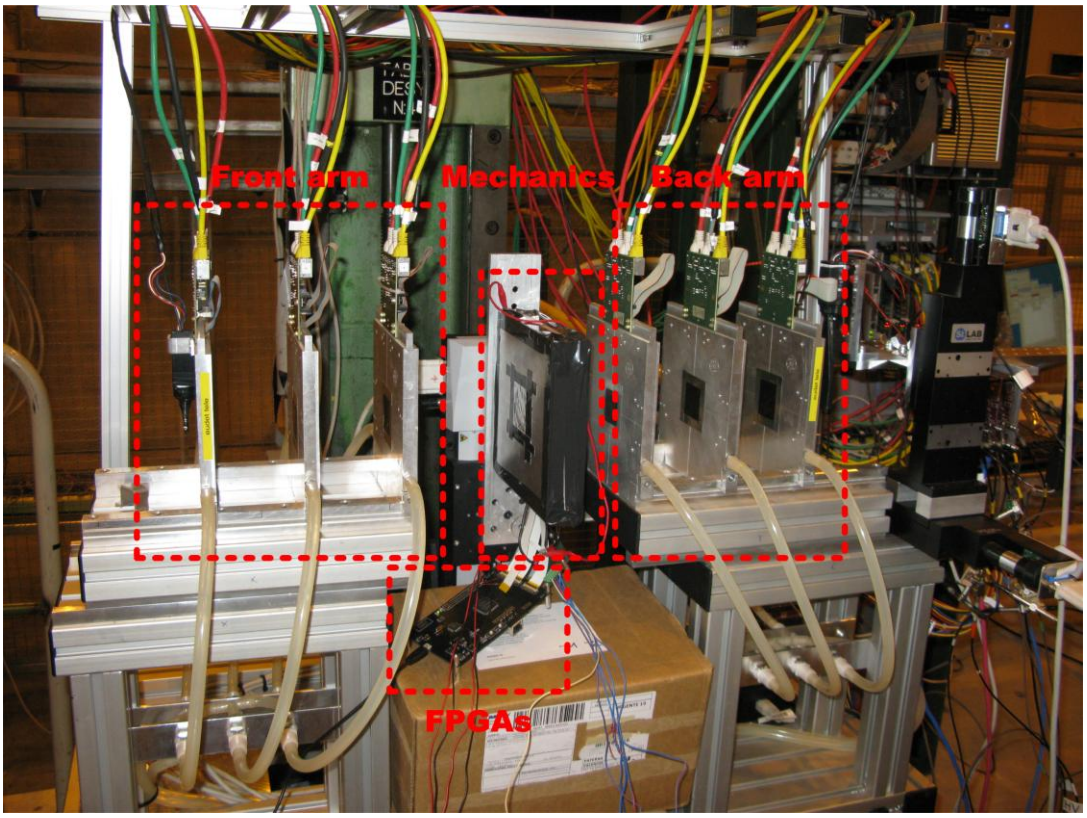

Figure 4.29 Set-up used at the CERN beam-test.

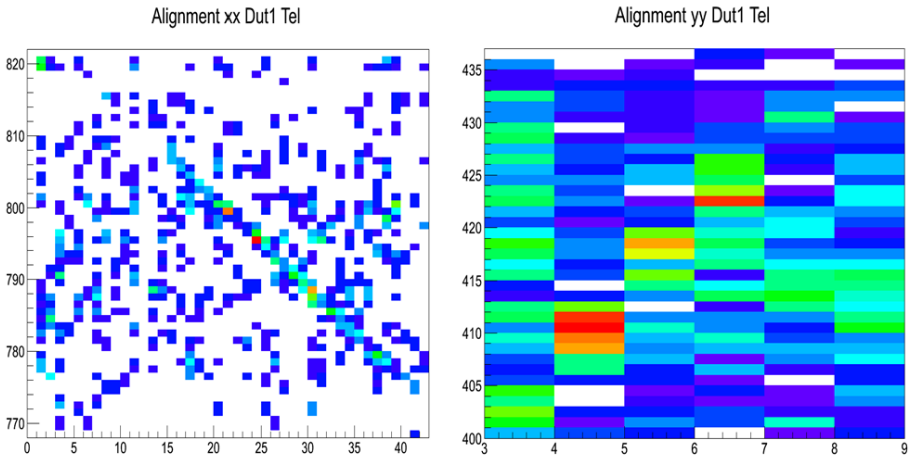

Figure 4.30 Correlation between the GAPD detector array and the EUDET/AIDA beam telescope.

detector array and the EUDET/AIDA beam telescope [37]. Further beam-tests are planned, but they are outside this work.

4.4 Discussion

In this chapter, the design and characterization of a prototype GAPD detector aimed mainly at particle tracking at future linear colliders has been analyzed. The suitability of this or any

other sensor technology for the mentioned application field is given by the capability to fulfill the highly demanding requirements of ILC and CLIC on detector systems. However, the GAPD detector presented here is a proof of concept prototype and therefore it is not optimized for performance. In the following lines, the extent of fulfillment of ILC and CLIC requirements by the prototype GAPD detector is reviewed. Solutions are also provided where the current device fails to meet the specifications.

To achieve an accurate particle track reconstruction, a maximum 17 μm pixel size is required. Nevertheless, at the forward disk of the tracking system (the final emplacement of the GAPD detector), the radial direction of the pixel can be relaxed to 100 μm. Thus, a sensitive area of 20 μm x 100 μm per pixel was chosen for the present design. The 20 μm x 100 μm sensitive area of the pixels, together with a reduced readout circuit that comprises 8 transistors only and the fact that all the GAPDs within a row share the same deep n-tub, yields a 67% fill-factor. Although this value is much higher than the typical fill-factors of GAPD arrays in conventional 2D technologies, it is still far from the 100% fill-factor demanded on future tracker detectors. Nevertheless, this parameter can be highly increased to values close to 100% with the utilization of 3D technologies, as it will be shown in the next chapter. In spite of having proved that the present GAPD array can sense MIPs, further studies on this topic are necessary to characterize the spatial resolution.

To reduce the uncertainty in the reconstruction of the traces, the multiple scattering on the quantity of material being crossed by the particles has to be minimized. This sets a maximum detector thickness of 300 μm, according to the SiD proposal. Europractice typically produces chips with a thickness of 700 μm, but it also offers the possibility to thin the backside of the dies down to 250 μm without any additional costs, as it was done with the prototype presented in this chapter. The thinning does not have any negative consequences on the performance of the detector.

Regarding the timing resolution, GAPD detectors are the only sensor technology proposed so far that is capable to provide single bunch crossing precision without using time-stamping techniques. Although GAPD sensors are characterized by rise times of a few hundred picoseconds, the timing resolution of the detector is also determined by the readout electronics. The pixels of the present GAPD detector array, built in a relatively old technology process, require 1.65 ns to be read out. Thus, the present detector could be used at ILC as it is, but the prototype is not suited for CLIC. The mere utilization of a deep submicron technology process, where propagation delays are significantly reduced, would still not solve the problem, as the CLIC bunch-spacing of 0.5 ns is too short to allow for a complete readout of a large detector within this time slot. Alternatively, the detector could be read out by using time slicing,

provided that it complies with the required occupancy. A more efficient solution goes through the implementation of TDCs, which can tag with a timing label each sensor ignition.

In order not to affect pattern recognition, the occupancy including beam-induced background hits must be below 1%. Regarding this specification, ILC and CLIC typically impose different performance features on detector technologies, since these two colliders are characterized by different background levels and different bunch train time structures. On the one side, a background level of 0.004 hits/cm^2/BX (4th layer of the forward tracker detector) and trains with 2820 bunch crossings that take place each 337 ns are foreseen at ILC. On the other side, these parameters will be much more challenging at CLIC, where a background level of 0.87 hits/cm^2/BX and trains with 312 bunch crossings that are 0.5 ns apart are expected. Thus, considering a GAPD pixel with a sensitive area of 20 μm x 100 μm, $8 \cdot 10^{-8}$ background hits/GAPD/BX and $5.43 \cdot 10^{-3}$ background hits/GAPD/train are expected at ILC and CLIC, respectively. However, in the case of GAPD detectors the noise counts generated by the sensor dominate the occupancy. In the previous chapter, the importance of operating the detector in the time-gated mode to reduce the probability to detect the noise pulses and thus the occupancy was already stated. Nevertheless, the need to further improve the results obtained was also pointed out. The experimental characterization of the 10 x 43 GAPD array has shown that a deeper reduction of the DCP is possible by cooling the working temperature to -20 ºC. The small decrease of the avalanche breakdown probability as the temperature is lowered should not affect the detection of MIPs, which generate around 80 primary electron-hole pairs per μm as they pass through silicon. Thus, $1 \cdot 10^{-5}$ noise counts/GAPD/BX are induced at ILC under the conditions of 1 V of V_{OV}, 1 ns gated-on period, 300 ns gated-off period and -20 ºC. In contrast, at CLIC $2 \cdot 10^{-2}$ noise counts/GAPD/train are generated at 1 V of V_{OV}, continuous mode of operation and -20 ºC. The difference between the beam related backgrounds and the noise counts is still between 3 (ILC) and 1 (CLIC) orders of magnitude, which may threaten the utilization of GAPD detectors at future linear particle colliders. To keep the noise counts below the beam related backgrounds, the logic AND between the output values of two or more overlapped pixels from two or more different layers could be done. With a 2-input logic AND, $1 \cdot 10^{-10}$ noise counts/GAPD/BX and $4 \cdot 10^{-4}$ noise counts/GAPD/train would be induced at ILC and CLIC, respectively. These DCPs are below the expected beam related backgrounds at both colliders, and therefore acceptable.

To ensure the proper performance of the detector over its useful lifespan, a certain extent of radiation tolerance is required. Thus, tolerance to a TID and NIEL of 1 kGy/year and 10^{11} n_{eq}/cm^2/year is required at ILC, and of 200 Gy/year and 10^{10} n_{eq}/cm^2/year at CLIC. GAPD detectors are not exempt of radiation damage, being the increase of the sensor intrinsic noise and the misfunction of the readout electronics the predominant effects. Although the present

GAPD array was not irradiated, according to [23] a DCR increase by a factor 3-4 is expected after an irradiation dose of 10 kGy, which is the cumulative radiation foreseen at ILC after 10 years of operation. Regarding the consequences of NIELs, the only results published so far report a DCR increase by a factor ~45 after a proton irradiation with a fluence of $8.3 \cdot 10^7$ p/cm^2/s, which is 4-5 orders of magnitude higher than the fluences foreseen at ILC and CLIC. The increase of the DCR as a consequence of IELs will result in an aggravation of the DCP to $4 \cdot 10^{-5}$ noise counts/GAPD/BX at ILC and $8 \cdot 10^{-2}$ noise counts/GAPD/train at CLIC after 10 years of operation. The effects of NIELs should be lower than those of IELs at both colliders. Nevertheless, the present GAPD detector should be submitted to an irradiation campaign to obtain more concluding results on this topic. Concerning the readout electronics, mechanisms to mitigate the effects of SEEs were not included in the present design so as to minimize the risks of failure, but they should be incorporated in a future version.

To minimize the material budget of the cooling system, the power consumption of the detector should be as low as a few mW/cm^2. However, due to the output pads of the present chip, the power consumption of the GAPD array is high. This issue could be solved by using an LVDS pad. Finally, immunity to EMIs is ensured by the nature of GAPDs and an affordable cost is guaranteed by the possibility to build the detector in a conventional CMOS technology.

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Chapter 5

Further improvements for GAPD technologies

Amongst other severe specifications, a 100% fill-factor is demanded by future linear colliders on detector systems [1]. In the particular case of GAPDs, the presence of non-sensitive areas due to the guard ring to prevent the premature edge breakdown and the monolithically integrated readout circuit to improve the detector response induce low fill-factors which rarely exceed the 10% [2-6]. Additionally, in those technologies that are below the 0.25 μm feature, the masks that the designers introduce in the layout to block the STI, and thus avoid a dramatic increase of the DCR, worsen the situation. In this thesis, 3D-ICs are explored as a solution to overcome the fill-factor limitation of standard GAPDs. In this chapter, the maximum fill-factor achievable by a GAPD pixel detector in the Global Foundries 130 nm/Tezzaron 3D process is analyzed. The study shows that fill-factors between the 66% and 96% can be obtained with different array architectures and a time-gating readout circuit of minimum area. The design of a time-gated GAPD pixel detector in the Global Foundries 130 nm/Tezzaron 3D process and aimed to particle tracking at future linear colliders is also described here.

Additionally, the possibility to improve the performance of the GAPD technology in light detection applications has also been investigated in this thesis. On the one hand, the time-gated operation is proposed as an effective technique to extend the sensitivity of dSiPMs (digital Silicon PhotoMultipliers), detectors that are also based on GAPD pixels and widely used in the imaging field. On the other hand, several correction techniques are investigated to minimize the effects of the non-uniformities that are inherent to GAPD arrays. The experiments realized and the results obtained are broadly discussed in this chapter.

5.1 3D vertical integration with the Global Foundries 130 nm/Tezzaron 3D process

The 3D GAPD detector described in this chapter is in a 130 nm low power CMOS process fabricated by Global Foundries and vertically integrated by Tezzaron, available in MPW runs organized by CMP, MOSIS and CMC Microsystems. 3D-ICs manufactured in the Global Foundries 130 nm/Tezzaron 3D process typically consist of two layers of logic dies fabricated by Global Foundries and two or (if possible) three layers of memories supplied by Tezzaron. However, it is also possible to build a two-layer stack with no memories attached (no-DRAM option), which is the case with this work.

In this option, the 3D-ICs are manufactured by independently fabricating the 2D logic dies corresponding to the two different tiers on separate wafers. Then, the two wafers are stacked face-to-face, bonded together, thinned and finally diced [7]. During the stacking process, the top of the WTOP wafer is flipped onto the top of the WBOTTOM wafer in a right-to-left orientation. Hence, the two logic dies are bonded face-to-face (i.e. wafer-to-wafer). The bonding process is done by means of the Tezzaron's Cu-to-Cu thermocompression. The connection between tiers for relaying signals is made through Metal 6, which is the highest metal of the technology process. This 3D process also uses via-first TSVs (filled with tungsten) for connection between the logic circuitry and the I/O bond pads, which are placed on the back of the WTOP tier. TSVs are also used to control thinning. As a consequence, it is necessary to maintain a minimum TSV density throughout both tiers, which forces the utilization of dummy TSVs. The recommended TSV pitch is 100 μm. TSVs are arranged in a hexagonal shape with a width (edge-to-edge) of 1.2 μm and covered with Metal 1. After bonding, the WTOP wafer is thinned down to about 12 μm until the bottom ends of the TSVs are exposed. Being the WBOTTOM wafer backlapped to about 750 μm, the total thickness of the two-layer logic stack is nominally 765 μm. The WBOTTOM wafer can also be thinned, however this incurs additional costs. Back metal for bonding pads is applied to the thinned WTOP wafer. When all this processing is done, the wafer stack is diced. A schematic diagram of a finished device is shown in Fig. 5.1.

5.1.2 Geiger-mode avalanche photodiodes in a 130 nm process

The low fill-factor of GAPD detectors is due to two aspects of the design of the pixel, which are the non-sensitive areas of the sensor and the readout electronics. The non-sensitive areas of the sensor include the guard ring surrounding the p-n junction as well as the masks used to block the STI. In a conventional CMOS process, the diode geometry creates a higher electric field at the edges, which leads to premature edge breakdown. To avoid this unwanted effect, the junction of the diode is surrounded by a guard ring with a lower doping profile, as explained in previous chapters. However, the guard ring usually is non-sensitive. In addition, for those technologies below the 0.25 μm node, as it is the case of the process supplied by Global Foundries, a SiO_2 STI is compulsorily constructed in the fabrication process to prevent punch-through and latch-up. Punch-through is the existence of a parasitic current path located below the gate which shorts the drain and source terminals of CMOS transistors. Latch-up is the inadvertent creation of a low impedance path between the high and the low power supply terminals of CMOS circuits. Both phenomena increase the power consumption and therefore they must be avoided. Nevertheless, the presence of the STI near the GAPD multiplication

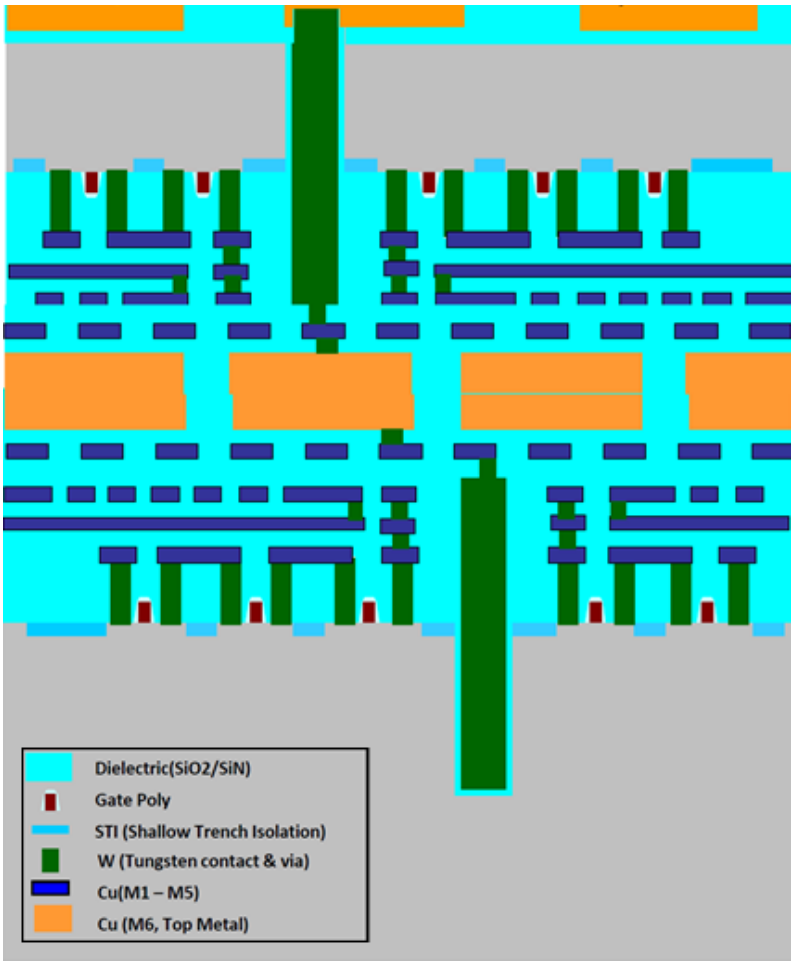

Figure 5.1 WTOP and WBOTTOM tiers in a finished device [12].

region may induce extremely high levels of noise at frequencies above several MHz [8]. Fortunately, there exist several design techniques at the layout level to force the physical separation of the STI interface from the GAPD multiplication region and obtain a beneficial impact on the noise, but at the expense of reducing the fill-factor [9-11]. The readout electronics is also monolithically integrated with the sensor on the same die to improve the dynamic response. Despite of using a readout circuit based on a simple voltage inverter and a memory cell, and thus with a small number of transistors, the area occupied by the transistors is still too large when compared to the sensor area. As a result, the non-sensitive area of the pixel chip is quite large compared with the sensitive area.

5.1.3 Array design

The proposed 3D GAPD detector consists of an array of 48 x 48 pixels. As shown in Fig. 5.2 and similarly to other GAPD pixels already described in this thesis, each pixel is comprised of a GAPD, active inhibition (M_{P0}) and active reset (M_{N0}) switches to perform the time-gated

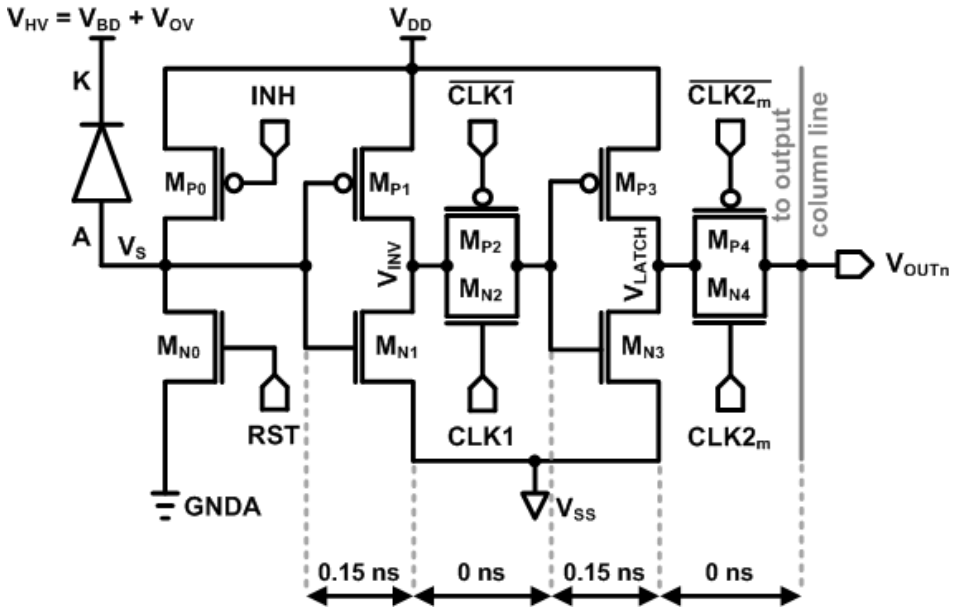

Figure 5.2 Schematic diagram of the time-gated digital pixel in the Global Foundries 130 nm CMOS technology. V_{OUTn} is connected to the output column line n.

operation, and a readout circuit based on a voltage discriminator (M_{P1}-M_{N1}), a 1-bit memory register (M_{P2}-M_{N2}-M_{P3}-M_{N3}) and a transmission-gate (M_{P4}-M_{N4}). The number of transistors per pixel is the lowest possible for a time-gated GAPD detector and the size of the transistors is the minimum allowed by the technology.

5.1.3.1 Sensor and mode of operation

In this 130 nm technology process, the sensor diode is implemented by means of a p^+ anode within an n-well cathode. As usual, the junction is surrounded by a low doped p-well guard ring to achieve a planar multiplication region and hence avoid the premature edge breakdown. Moreover, a buried n-type isolation layer or deep n-well, available in this technology, is used to achieve full isolation of the p-well guard ring from the p-substrate. This layer is also used to prevent the punch-trough of the p-well to the p-substrate. The n-well cathode is biased at a positive V_{BD}+V_{OV} to operate in Geiger-mode. The avalanches are sensed at the p^+ anode. The electronics is located within the p-substrate, which is connected to ground (V_{SS}).

The Global Foundries 130 nm technology requires the utilization of the STI. This isolation layer is etched in all regions not covered by a heavy implant or polysilicon to make sure that it surrounds all the p^+ and n^+ implantations for an isolation improvement. In order to avoid contact between the STI and the multiplication region of the GAPD, and thereby have an acceptable DCR, a polysilicon gate (polysilicon, oxide, diffusion and p^+ layers) is drawn around the p^+ anode. A GAPD cross-section is shown in Fig. 5.3. The polysilicon gate is biased at the same

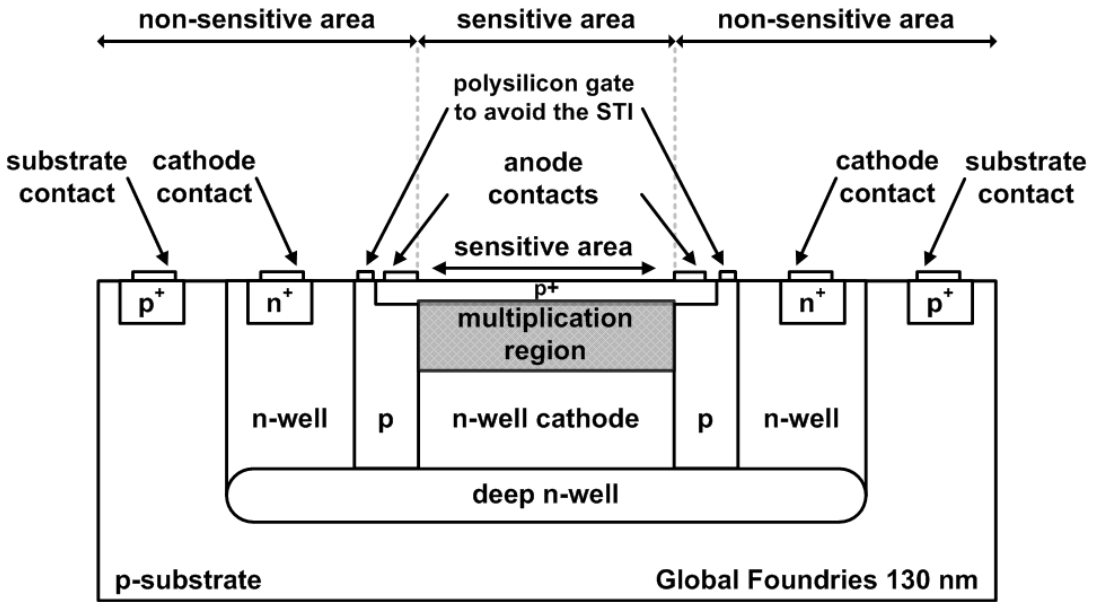

Figure 5.3 Cross-section of the GAPD designed with the Global Foundries 130 nm CMOS technology. The cross-section is not to scale.

potential as the p^+ layer [9]. The separation between two neighboring GAPDs is filled with n-well, which is short-circuited to the n-well cathode through the deep n-well layer. Ohmic contacts for bias to $V_{BD}+V_{OV}$ are placed on top of the n-well separation to ensure a robust cathode biasing throughout all the pixels of the array. The introduction of the p-well guard ring, together with the polysilicon for an STI-free GAPD and the cathode ohmic contacts, generates a minimum separation between two neighboring GAPDs of 2.24 μm.

The sensor time-gating is controlled by means of two external signals (RST and INH) implemented through MOS transistors (M_{N0}-M_{P0}), as previously described in this thesis. The supply voltage V_{DD} is 1.2 V in this technology.

5.1.3.2 Readout circuit

The readout circuit is based on the 2-grounds scheme with a dynamic latch that has been explained in previous chapters. In this case, the CMOS inverter used to detect and digitize the Geiger pulses was designed to have a threshold voltage of $V_{DD}/2$ and a propagation delay of 150 ps. However, the typical pass-gates controlled by the CLK1 and CLK2 control signals have been substituted by transmission-gates. A voltage pulse propagated through a minimum area nMOS pass-gate suffers from a voltage drop of around 0.6 V. Given that V_{DD} is 1.2 V in this technology, a logic '1' generated by the CMOS inverter that senses the Geiger pulses (M_{P1}-M_{N1}) is seen as a logic '0' by the CMOS inverter of the dynamic latch (M_{P3}-M_{N3}, which also has a

threshold voltage of $V_{DD}/2$). This problem was solved by using a transmission-gate, which ensures the correct transmission of logic '0' and '1'.

5.1.3.3 Array architecture

Prior to the final layout of the 48 x 48 GAPD array, the maximum achievable fill-factor with the Global Foundries 130 nm/Tezzaron 3D process and the readout electronics proposed before was investigated with several array architectures (drawn in Fig. 5.4). A first scheme implements the sensors in one tier and the readout electronics in the other one (Fig. 5.4-a). With a sensor area of 18 µm x 18 µm, a fill-factor of 66% is achieved with this configuration. The other structures studied benefit from the two-layer vertical stacking to overlap the non-sensitive areas of one tier with the sensitive areas of the other tier. In addition, different sensor areas were used to maximize the overlap between tiers. Thus, the second approach is based on clusters of four pixels and two sensor areas of 18 µm x 18 µm and 30 µm x 30 µm. Three 18 µm x 18 µm sensors together with the readout electronics of the four sensors are placed in one tier, whereas the 30 µm x 30 µm GAPD is strategically placed in the other tier to overlap the readout electronics and most of the non-sensitive areas of the 18 µm x 18 µm sensors (Fig. 5.4-b). This approach generates a 92% fill-factor. A similar idea is implemented in the structure depicted in Fig. 5.4-c, however clusters of five pixels are used here. A 96% fill-factor is achieved in this structure with two sensor areas of 8 µm x 8 µm and 20 µm x 30 µm, however the solution is bizarre and risky. As reported in [8], GAPD devices fabricated in conventional 130 nm technologies and with large areas starting around 40 µm x 40 µm do not experience the avalanche breakdown phenomenon. Therefore, the smaller the sensor, the more guarantees that it will work properly. The last strategy explored is shown in Fig. 5.4-d. It uses clusters of four pixels and both tiers have sensors and readout electronics. The sensor areas are 18 µm x 15 µm and 23 µm x 20 µm. An 85% fill-factor is achieved in this case.

Out of the four array architectures proposed, the structures represented in Fig. 5.4-a and Fig. 5.4-b were selected to be implemented in the final layout and study their performance. The first structure was chosen for its simplicity and the second one because it provides the maximum fill-factor with the lowest risks. Thus, the 48 x 48 GAPD array is composed of two sub-arrays of 48 x 24 pixels each. The GAPDs of the first array plus the 18 µm x 18 µm GAPDs and the readout electronics of the second array are placed in the WTOP tier. In contrast, the readout electronics of the first array plus the 30 µm x 30 µm GAPDs of the second array are implemented in the WBOTTOM tier. Hence, there is interconnection between tiers from the node V_S to the readout circuits in both sub-arrays. The sensors were distributed in the two tiers bearing in mind to place the maximum possible number of sensors in the WTOP tier, which is 12 µm thick. The TSVs

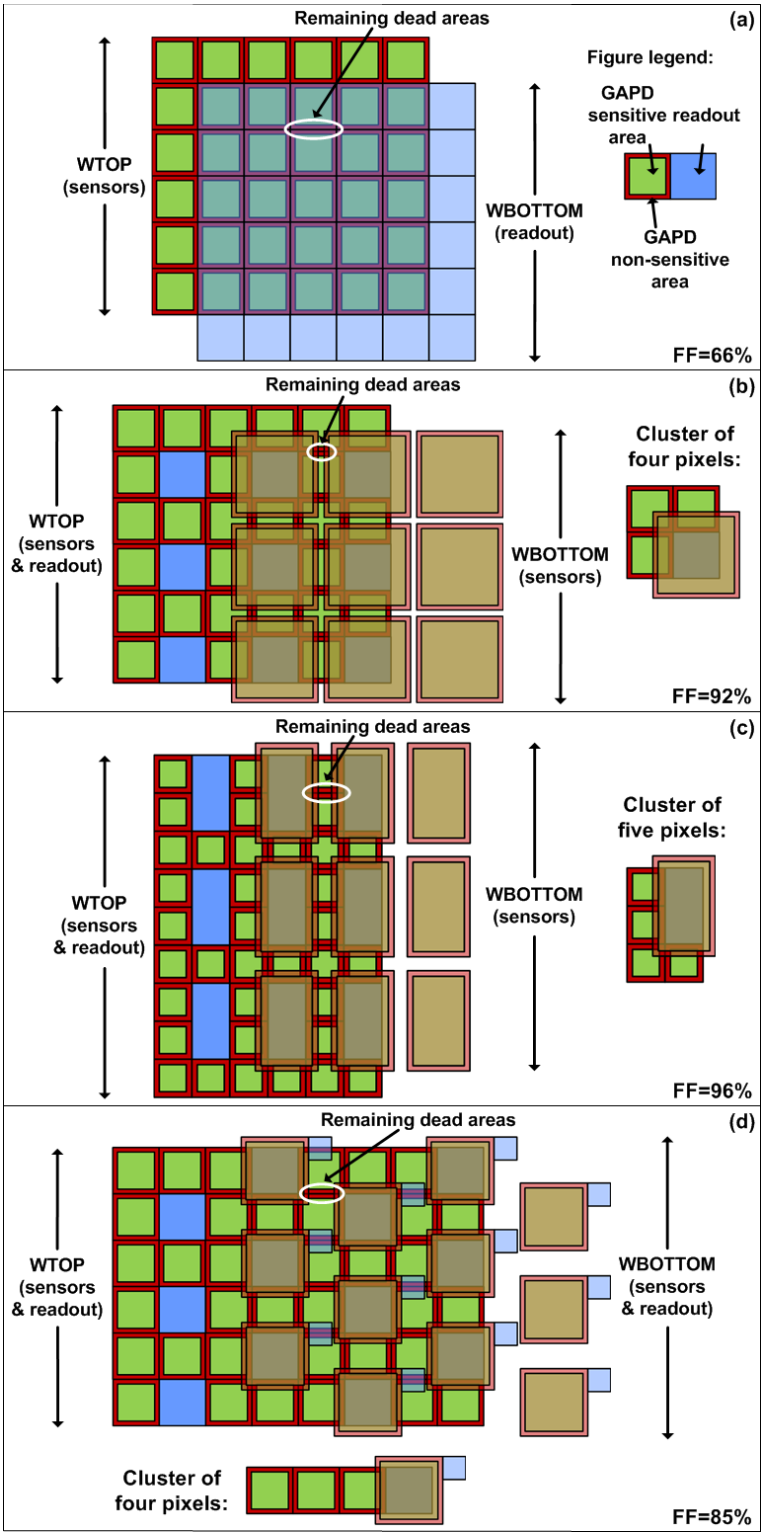

Figure 5.4 Analysis of the achievable fill-factor with several array architectures of GAPDs and considering the technology design rules of the Global Foundries 130 nm/Tezzaron 3D process. The sensors and readout electronics are not to scale.

are located together with the readout circuits when possible. In those regions were sensors only are present, the TSVs are placed in between two sensors while maintaining the minimum

recommended pitch.

The 48 x 48 GAPD detector is sequentially read out by rows during the gated-off periods, following the same scheme already presented in previous chapters. In this design, however, only one pad is implemented to distribute the CLK2 external signal to the different rows of the array in order to save area. To reach the 48 rows one after the other, a decoder with 48 output lines and a SEL (as SELect) signal is also included in the chip. As the chip is equipped with only 6 output pads, 6 8-bit shift-registers are placed between the output column lines and the output pads. To extract the information generated by the sensors, a readout protocol is used. Thus, when a particular row (m) is activated by its corresponding $CLK2_m$ signal and the contents of the 6 shift-registers have been updated with the new information, a WrEn (Write Enable) signal generated by the chip is set high. In response, when the FPGA used to count off-chip the Geiger pulses senses that the WrEn signal is high, an EnOut (Enable Output) signal generated by the FPGA is set high. Then, the 6 shift-registers are emptied in 8 pulses of their clock, which is set at 1 GHz at full speed. To ensure the rapid response of the array, a CMOS buffer is placed between the input pads of the control signals RST, INH and CLK1, or each output of the decoder in the case of the $CLK2_m$, and each row of the matrix. CMOS buffers have also been placed between each output line and the inputs of the shift-registers. The detector can be read out in less than 400 ns. A functional diagram of the chip is depicted in Fig. 5.5. The waveforms for the pixel operation together with the readout protocol described here are depicted in Fig. 5.6.

Although the design of the detector is finished (see Fig. 5.7 for the final layout of the chip), it has not been submitted for fabrication due to the continuous delays in the MPW runs of the Global Foundries 130 nm/Tezzaron 3D technology. Nevertheless, the GAPD pixel detector designed in a 3D process demonstrates that the typical low fill-factor of GAPD detectors can be increased up to values close to 100%, as demanded by future linear colliders on detector systems.

5.2 Time-gated operation as an effective method to extend the sensitivity of dSiPM

SiPM detectors, also known as MPPCs (Multi-Pixel Photon Counters), consist of an array of GAPD sensors that are generally connected in parallel on a common silicon substrate and passively quenched through a monolithic resistor. The connection between the pixels, considering that one pixel is composed of one GAPD and its corresponding quenching resistor, is made on one side by the low resistivity substrate and on the other side by a metal layer. Due to their GAPD based nature, the principle of operation of SiPMs is therefore the avalanche multiplication process. Accordingly, the main features of these devices comprise single-photon

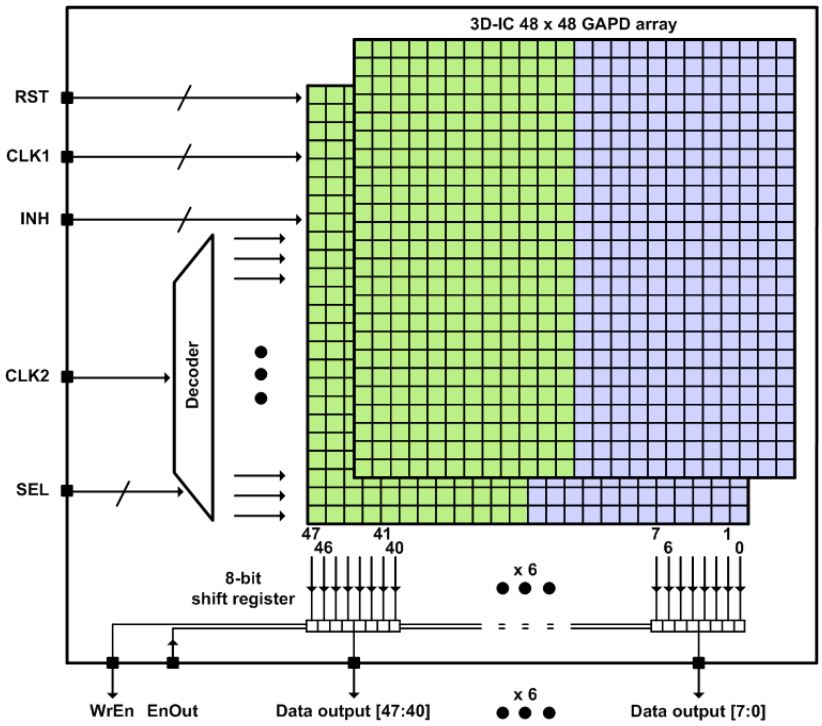

Figure 5.5 Functional diagram of the detector readout.

sensitivity, fast timing response and virtually infinite gain, but also a high pattern noise given by dark counts, afterpulses and crosstalks. However, in contrast to GAPD detectors, in a conventional SiPM the sensing nodes (i.e. the anodes) of all the pixels are connected together and thus the output signal is the sum of the individual currents of the fired cells. Therefore, although the pixels of SiPMs operate digitally as a binary device, traditional SiPMs are analogue detectors.

In spite of SiPMs being a relatively young technology that was not invented until 1997 [13], these devices have undergone a fast development in the last few years. They are currently produced by different manufacturers, such as Hamamatsu, Philips and the Semiconductor Laboratory of the MPI (Max-Planck-Institute), amongst others. Due to their notable advantages, they have become the real solid-state alternative to the more standard PMTs, which require supply voltages that are around 200 V, in addition to being sensitive to magnetic fields and also highly priced.

Regarding the extraction of the information generated by the sensor, some SiPM detectors under development are just tested by means of a fast waveform digitizer. Nevertheless, to better exploit their advantages, these devices need to be read out via a multi-channel ASIC. At present time, there exist a few readout ASICs, mostly for applications in HEP experiments [14] and medical imaging [15], that are well established amongst the SiPM community. They allow to measure the energy generated by the sensor or the energy and the time as well, either providing an analogue or a digital output signal. A summary of these chips can be found in [16].

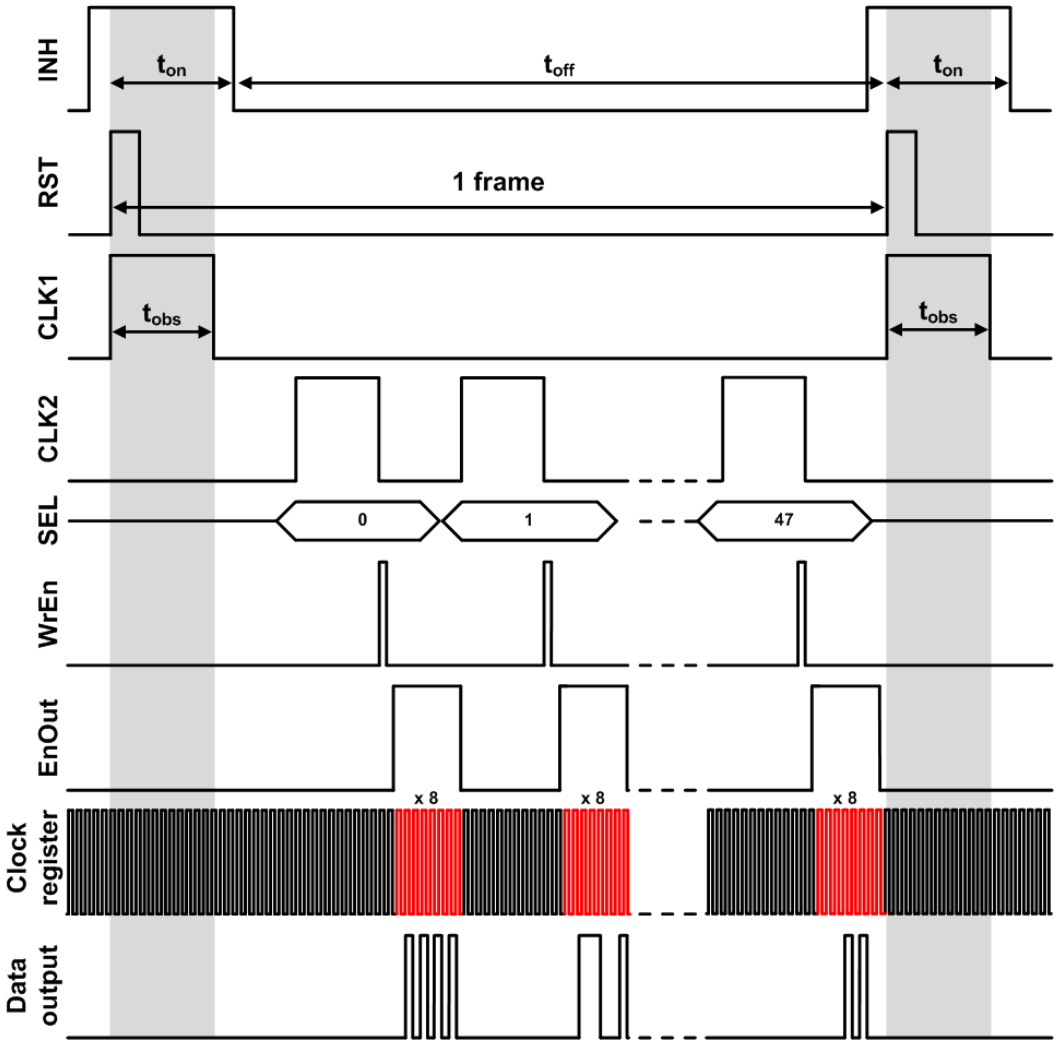

Figure 5.6 Waveforms to operate and read out the time-gated GAPD detector.

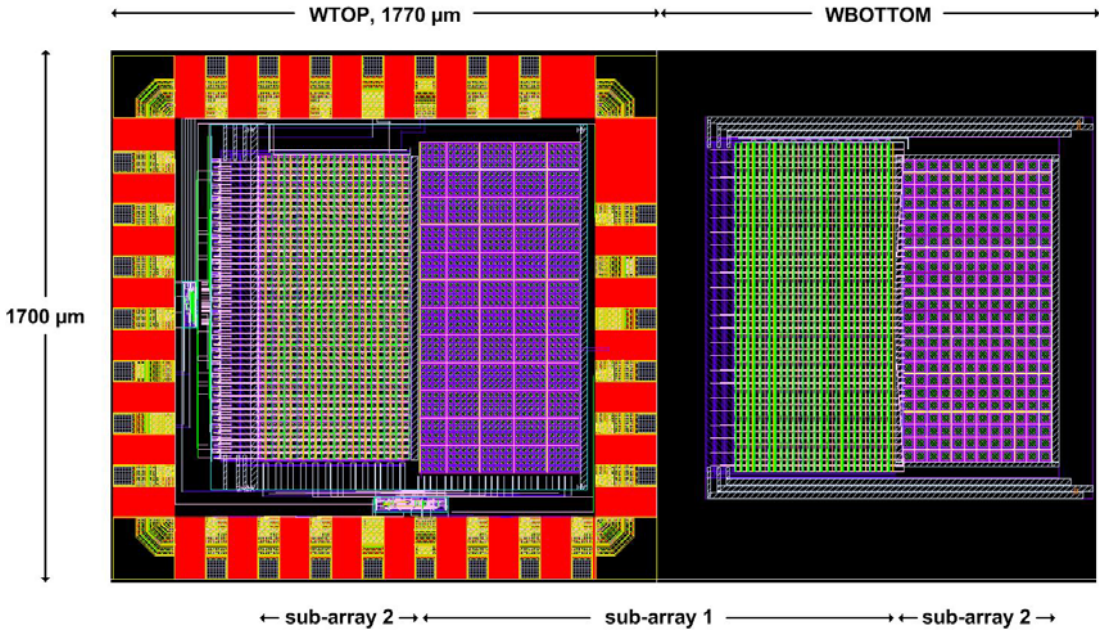

Figure 5.7 Layout of the two GAPD sub-arrays designed with the Global Foundries 130 nm/Tezzaron 3D process.

However, most current SiPM detectors do not take full advantage of the excellent intrinsic properties of GAPDs. On the one side, since the output signal is generated by all the fired pixels of the array, the pattern noise can be of several hundred kHz even at cooled temperatures, which prevents single photon detection. On the other side, the generated signal is deteriorated by the relatively large parasitic capacitances between the sensing device and the readout chip, and active quenching circuits are required to reduce the afterpulsing effects. Moreover, the generated signal can also be easily affected by electronic noise. The digital SiPM, or simply dSiPM, developed by Philips overcomes this issue by equipping each GAPD with a monolithic readout circuit [17, 18], so that each pixel can be read out individually. The readout circuit used by Philips contains a voltage discriminator to sense the voltage drop at the GAPD anode upon avalanche, active quenching and recharge circuits to improve the recovery time in addition to a 1-bit memory for the selective inhibit of GAPD pixels with an abnormally high DCR. Each pixel (i.e. the GAPD and its corresponding readout circuit) is connected to a TDC via a configurable and balanced trigger network. A separate synchronous bus is used to connect each pixel to the counters that determine the number of avalanches sensed. Thus, the output for each pixel consists of data packets containing the number of avalanches with its corresponding time-stamp. The detector is fabricated in a 180 nm modified CMOS technology by NXP. The presented topology allows to achieve a fill-factor between 50 and 78%, depending on the version of the prototype. The basic structure of analogue and digital SiPMs is depicted in Fig. 5.8.

In analogue and digital SiPMs, the intensity of the impinging signal is obtained by counting the number of fired cells during a certain integration time. Those pixels with an unusually high DCR are fired by noise phenomena most of the time and therefore they prevent the detection of extremely weak intensities. Moreover, other pixels with a significant pattern noise are gradually fired as the integration time is increased, thus increasing the threshold of events from which signal counts above noise counts can be observed. To solve this problem, Philips switches off the GAPDs with a DCR well above the average value. Thus, a better SNR and production yield can be achieved when compared to conventional SiPMs. According to Philips, only 5 to 10% of the diodes of their arrays with several thousand pixels show an abnormally high DCR due to defects. However, switching off these diodes is equivalent to the corresponding loss of fill-factor. Consequently, the probability to detect events is reduced. Moreover, the dynamic range, which is limited by the number of pixels composing the detector, is also decreased. This situation is not particularly delicate in photon applications, where the 30-40% PDP of the dSiPMs by Philips still outperform many PMTs, but it is an issue in HEP applications where having a 100% fill-factor is fundamental. Nevertheless, the situation can also be improved by means of the time-gated operation, which does not involve a loss of sensitive area. The

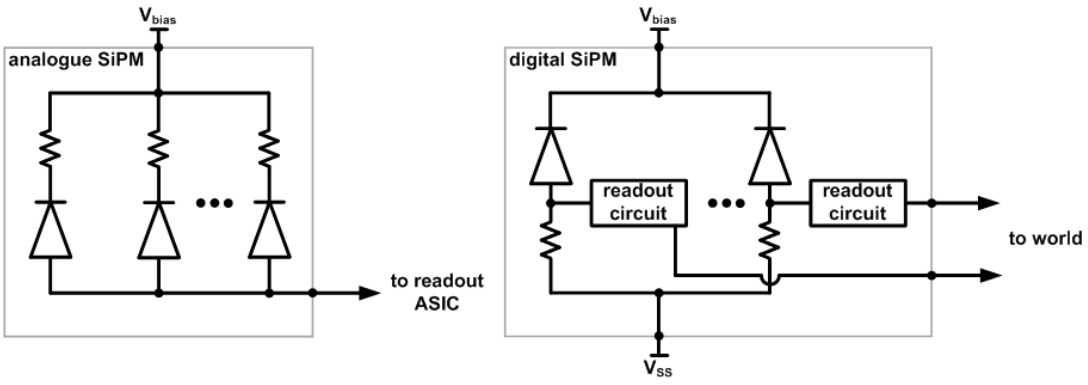

Figure 5.8 Schematic diagram of the basic topology of analogue (left) and digital (right) SiPMs. In digital SiPMs the quenching resistor can also be replaced by a transistor.

reduction of the gated-on period of the sensor allows to decrease the probability of pixels being fired by noise, while the signal detection capabilities remain intact and the dynamic range is extended.

The GAPD array introduced in Chapter 4, which can also be regarded as a time-gated dSiPM (referred to as time-gated dSiPM from now on in this section), has been used to test this feature. The time-gated dSiPM was operated with different gated-on periods that range from 200 ns to 3.2 μs, a gated-off period of 1 μs and a reverse bias overvoltage of 1 V. The number of repetitions was set at $1 \cdot 10^5$ for each of the measurement points. This characterization was done with the set-up described in section 4.2. Moreover, to show the improvements achieved with the time-gated operation in the detection of light, a pulsed 850 nm VCSEL array [19] with an active window of 100 ns within the gated-on period of the sensor was used to illuminate the time-gated dSiPM. With this experiment, we expected to see that shorter gated-on periods generate a lower number of pixels fired by the noise and, as a consequence, the minimum irradiance needed to sense signal is reduced and the dynamic range is increased while the fill-factor achieved by design is kept constant. A schematic representation of the number of pixels fired by the noise and the expected results can be found in Fig. 5.9 and Fig. 5.10, respectively.

To start with, the number of pixels fired by the noise as a function of the gated-on period was investigated. For this purpose, the noise counts recorded in the dark after $t_{obs} \cdot n_{rep}$ seconds were averaged over all the repetitions (i.e. noise $counts_{pix0}$ + noise $counts_{pix1}$ +…+ noise $counts_{pix430}/n_{rep}$). Thus, if all the pixels are always silent the result is 0, while if all the pixels are always fired the result is 430 (i.e. the total number of pixels of the array). The resulting values plotted in Fig. 5.11 show a linear increment, starting from 5.5 fired pixels at a gated-on period of 200 ns to 75.5 fired pixels at a gated-on period of 3.2 μs (approximately 5 pixels more every new 200 ns). These results match well with the expected DCP of the time-gated dSiPM for each gated-on period. With a mean DCR of 25.2 MHz, generated by the time-gated dSiPM of 430

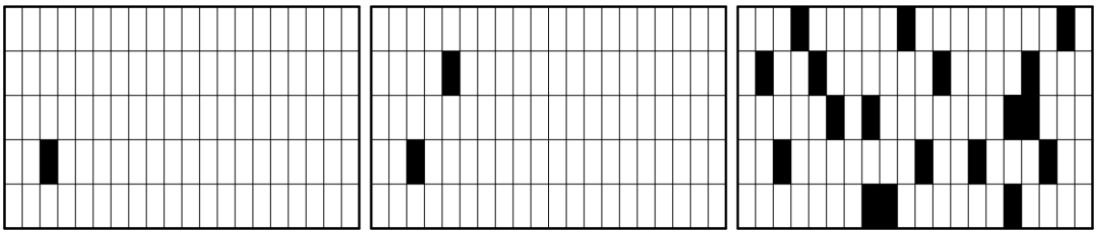

Figure 5.9 Schematic representation of the expected pixels fired by the noise at t_{obs1} (left), t_{obs2} (middle) and t_{obs3} (right), with $t_{obs1}<t_{obs2}<t_{obs3}$.

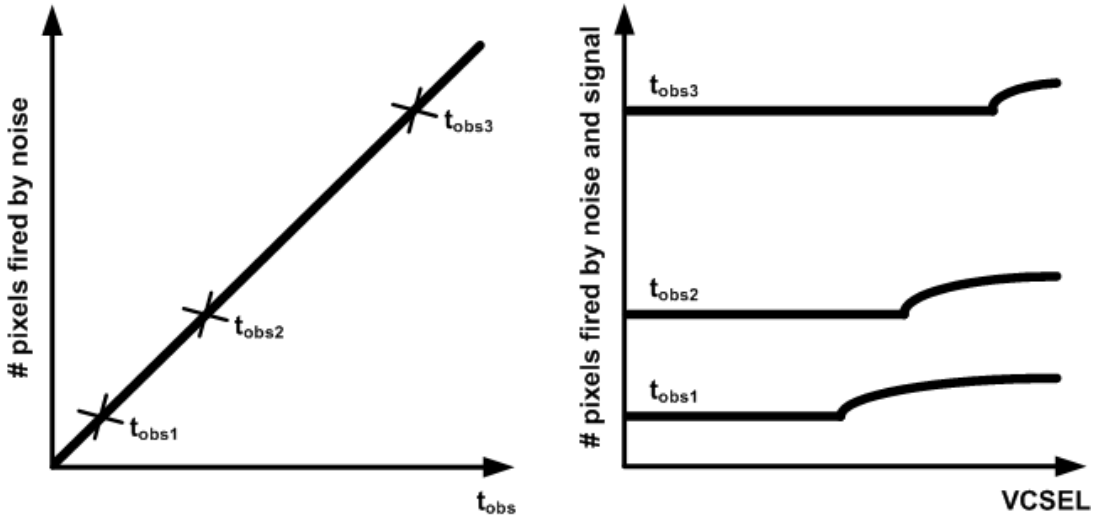

Figure 5.10 Schematic representation of the expected results to be found with time-gated dSiPMs applied to light detection applications.

pixels and measured at room temperature, the expected DCP is 5.2 pixels fired at 200 ns, 10.4 pixels fired at 400 ns and so on until 76.5 pixels fired at 3.2 µs.

After that, the time-gated dSiPM was illuminated with the pulsed VCSEL array. In this experiment, the pulse rate of the laser ranged from 0.24 MHz (t_{VCSEL}=100 ns, t_{obs}=3.2 µs, t_{off}=1 µs, duty cycle 2.38%) to 0.83 MHz (t_{VCSEL}=100 ns, t_{obs}=200 ns, t_{off}=1 µs, duty cycle 8.33%). The minimum irradiance from which pixels fired by signal can be observed was analyzed. The results plotted in Fig. 5.12 indicate a power dependence between V_{th}, the voltage used to bias the VCSEL array from which events can be discerned from noise, and the gated-on period. The shape of this curve is a consequence of the voltage-current curve of the VCSEL array, which also presents a power dependence. The increase of the threshold voltage as the gated-on period does is a consequence of the higher irradiance needed to generate signal above noise as the number of pixels fired by the noise is increased with the gated-on period. This result is consistent with what we expected. In the last place, the number of pixels triggered as a function of the irradiance was investigated for the different gated-on periods 200 ns, 800 ns and 3.2 µs. The measured values averaged over all the repetitions are plotted in Fig. 5.13. The flat regions of the curves correspond to those irradiances below V_{th}, i.e. the pixels are fired by noise

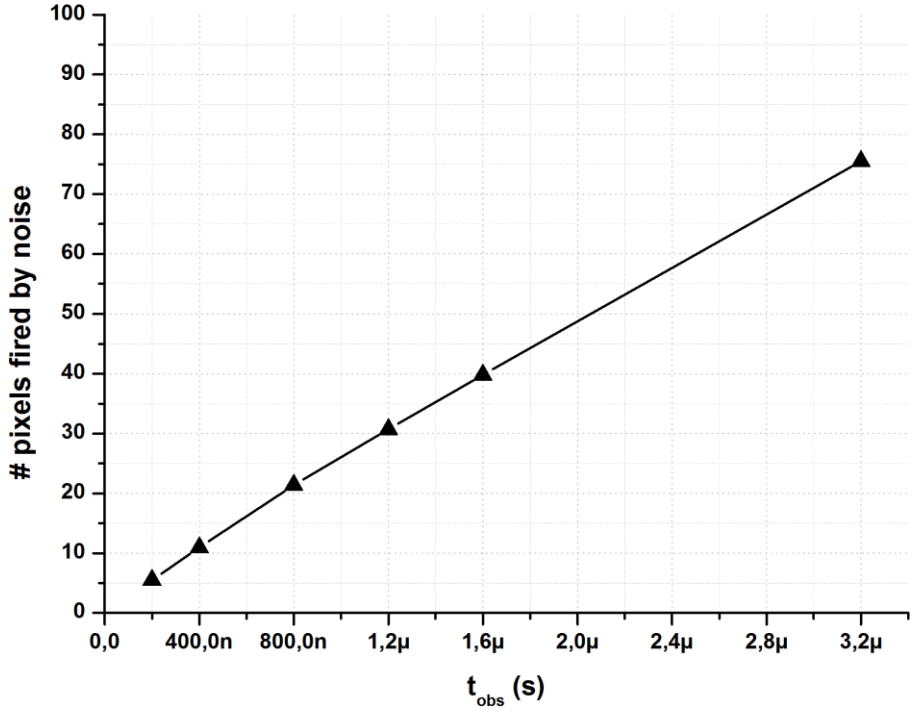

Figure 5.11 Number of pixels of the dSiPM fired by the intrinsic noise as a function of the gated-on period.

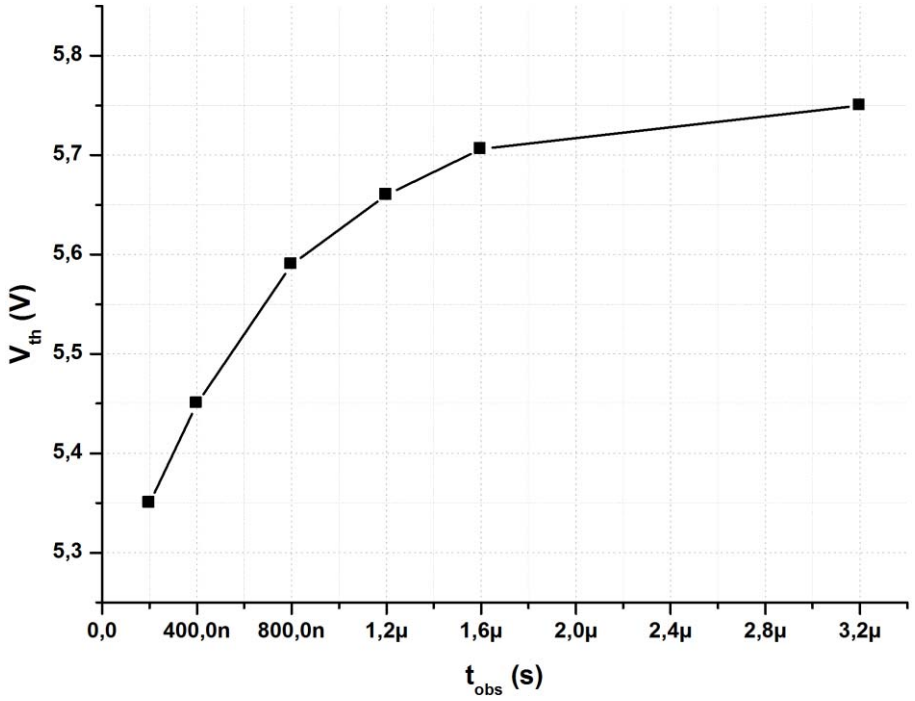

Figure 5.12 Threshold voltage from which pixels fired by signal can be observed as a function of the gated-on period.

phenomenon only. For all the gated-on periods investigated, the number of pixels fired by the noise is in good agreement with the values plotted in Fig. 5.11. Moreover, as the threshold irradiance is surpassed (see Fig. 5.14 for zoomed plot), a few pixels are fired by the impinging

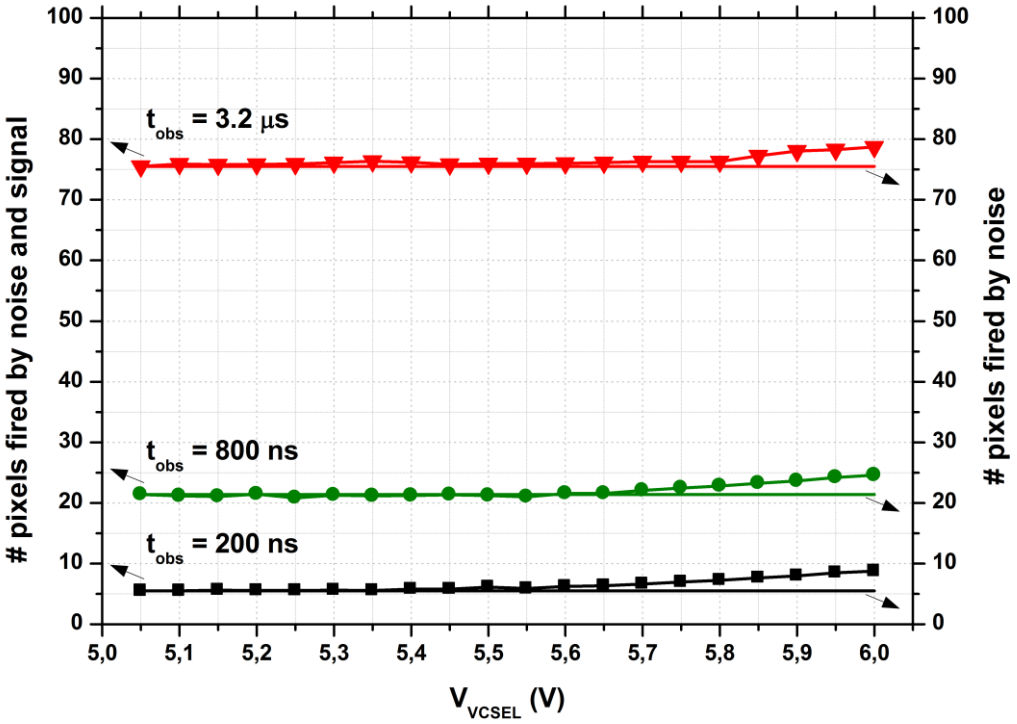

Figure 5.13 Pixels fired by noise and signal as a function of the bias of the VCSEL light source and for different gated-on periods.

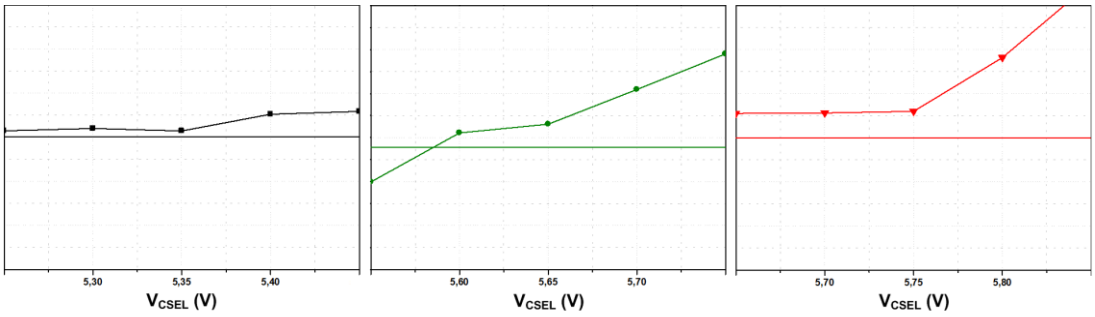

Figure 5.14 Zoom of the regions where the number of pixels fired starts to increase for the different gated-on periods investigated (200 ns is on the left, 800 ns is in the middle and 3.2 µs is on the right).

light. Thus, for a gated-on period of 200 ns, an increase in the number of pixels fired is sensed from 5.35 V (i.e. the voltage used to bias the VCSEL array). For the gated-on periods of 800 ns and 3.2 µs, the increase is sensed from 5.6 V and 5.75 V, respectively. These values match well with the data plotted in Fig. 5.12. It can also be observed in Fig.5.13 that the number of pixels fired by the impinging light for the different gated-on periods and the same voltage used to bias the VCSEL array is approximately the same once V_{th} has been surpassed. When the VCSEL array is biased at 6 V, i.e. at the maximum bias allowed the this laser, around 3 pixels are fired by the light with all the gated-on periods measured. However, the number of pixels being fired is low given the reduced PDP of the time-gated dSiPM at the the wavelength of the laser. It can be concluded that short gated-on periods of some nanoseconds longer than the width of the

expected impinging signal allow to observe weaker intensities without diminishing the fill-factor, the sensitivity nor the dynamic range of the detector.

5.3 Improvement of the dynamic range in vision systems based on GAPDs

A GAPD camera aimed at vision systems is composed of a moderate or large number of pixels. However, due to the doping profile fluctuations and lattice defects that are unavoidably introduced during the fabrication process [20], serious DCR and PDP variations may appear amongst the pixels of a single array. Moreover, the response of the pixels over the input irradiance range is non-linear. These DCR and PDP non-uniformities, together with the non-linear response of the pixels, reduce the output dynamic range of the camera and thus become relevant to the quality of the reproduced images. Nevertheless, it is also possible to minimize their impact through correction techniques, as it will be demonstrated in this section.

To depict a digital image, vision systems scale the range between the minimum and maximum pixel values, which are respectively generated by the weakest and strongest measurable light intensities, to a certain number of bins, each of which has the same exact increment. Each bin is then assigned to one representation level or color. The number of representation levels determines the number of bits or contrast of the generated image. However, because of the non-uniformities, the number of representation levels that in principle are available for quantization may be severely reduced. As a result, the number of bits or contrast are badly damaged.

This phenomenon is schematically illustrated in Fig. 5.15, where the minimum (in pink) and maximum (in blue) number of counts respectively generated by the less (pix_{min}) and most (pix_{max}) active pixels of a GAPD array are depicted as a function of the irradiance. Both the number of counts and the irradiance are split into 16 representation levels (i.e. 4 bits of contrast). However, given the DCR and PDP variations amongst the pixels, the quantity of counts generated by both pixels under the same irradiance is different. In fact, the differences may be so large, that the counts generated at a particular irradiance may belong to different representation levels (count levels 7 and 12 at irradiance level 9, as an example in Fig. 5.15). When the maximum number of counts at one level is higher than the minimum number of counts at the following level, there exists an overlapped area where it is impossible to establish an univocal relation between irradiation levels and count levels. As a result of these overlapped areas, which are determined by the deviation of the pixel counts across the array, representation levels are lost with respect to the original ones. The contrast of the generated image is also worsened.

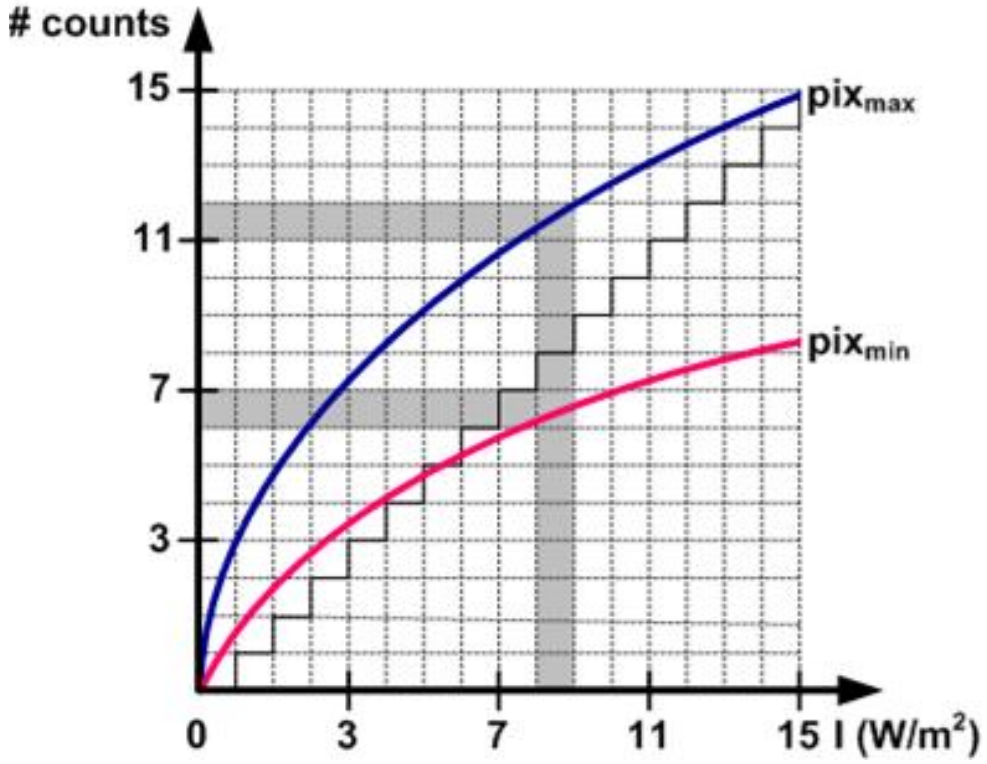

Figure 5.15 Schematic plot of the the minimum (in pink) and maximum (in blue) number of counts generated by the less (pix_{min}) and most (pix_{max}) active pixels of a GAPD array.

This issue can be minimized with NUC (Non-Uniformity Correction) techniques, which are based on either calibration or scene algorithms. The first type of algorithm equalizes the response of the pixels to the irradiance by means of an equation, while the second involves motion compensation or temporal accumulation and thus is more complex. Although NUC techniques are widely applied in the imaging field, especially in infrared and magnetic resonance imaging, their potential in GAPD cameras remains almost unexplored. So far, only one dSiPM detector with a LUT (Look Up Table) per pixel to correct the number of detected photons at sensor saturation has been reported [17]. In this work, NUC techniques based on calibration algorithms to improve the quality of GAPD imagers have been investigated.

A schematic diagram of the optical set-up used to measure the noise and sensitivity non-uniformities across the 10 x 43 GAPD array introduced in Chapter 4 is depicted in Fig. 5.16. It is based on an aspherical lens (model 352150 by Thorlabs) and an illumination ring consisting of 9 white LEDs (model SMLP12WBC7W by Rohm Semiconductor). Gated-on and gated-off periods of 10 ns and 1 µs were used, respectively, for these measurements. The number of repetitions was $10 \cdot 10^6$ times and therefore the total measuring time was 100 ms for each of the points analyzed. The reverse bias overvoltage was set at 1 V. The counts for each individual pixel as a function of the power consumption of the illumination ring, which is proportional to

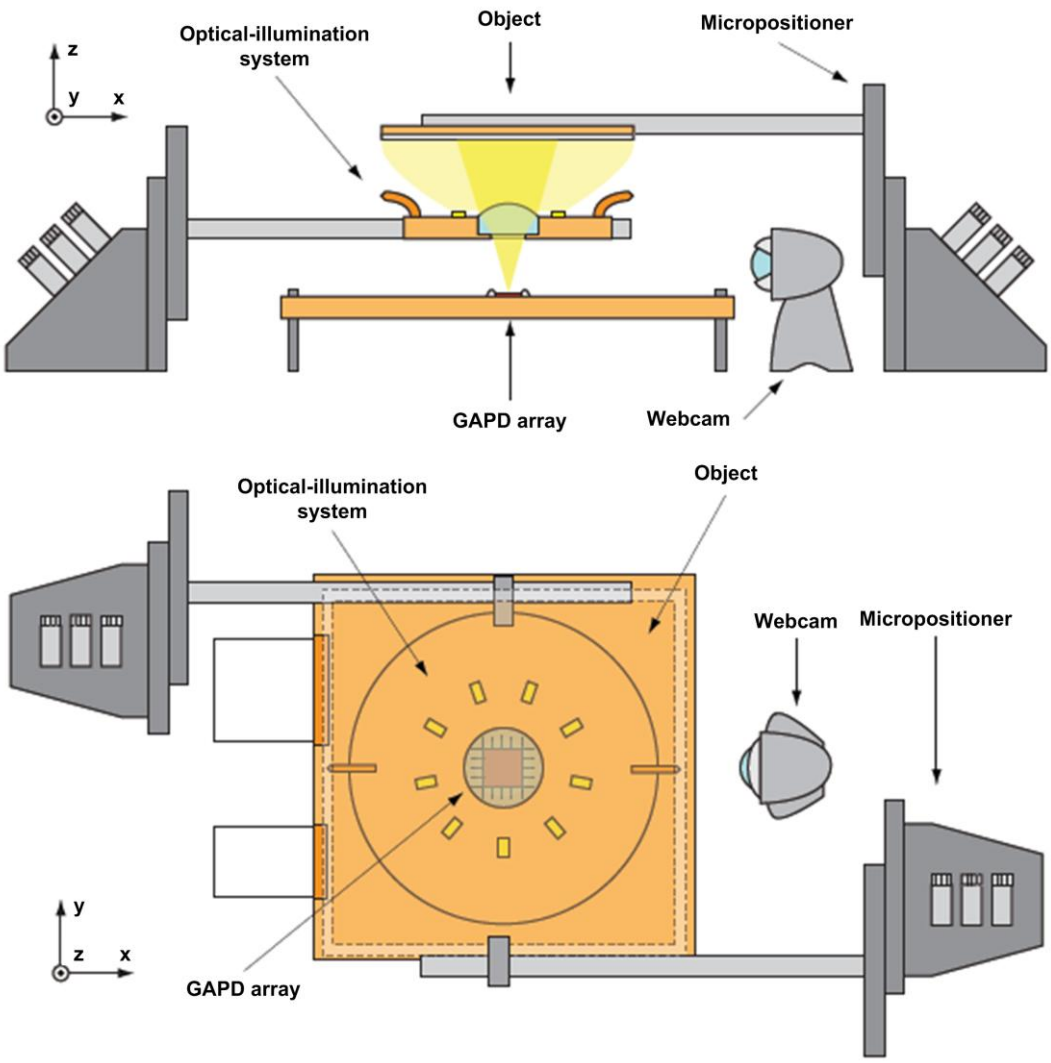

Figure 5.16 Schematic diagram of the set-up used for the measurement of the non-uniformities. Front (up) and top (down) views [21].

the irradiance, are shown in Fig. 5.17. It can be observed that the general trend of the pixel counts is to increase with the irradiance, from darkness until the saturation of the optical system. However, the response of each pixel is different, showing a high deviation across the array that is around 6% of the mean value and results in the reduction of the representation levels that can be used to depict an image. This behavior justifies the application of a correction technique. Nevertheless, because of the high deviation, the correction method cannot be applied with equality to all the pixels, which forces the utilization of a pixel-by-pixel calibration.

As a first solution, a calibration algorithm that makes use of one linear equation per pixel to equalize the response of all the pixels to a certain curve was applied to reduce the deviation. In this particular calibration algorithm, the response of all the pixels was equalized to the average pixel counts over the measured irradiance range. To start with, the effect of the DCR variation was eliminated by subtracting to each pixel the noise counts measured in the dark to the counts

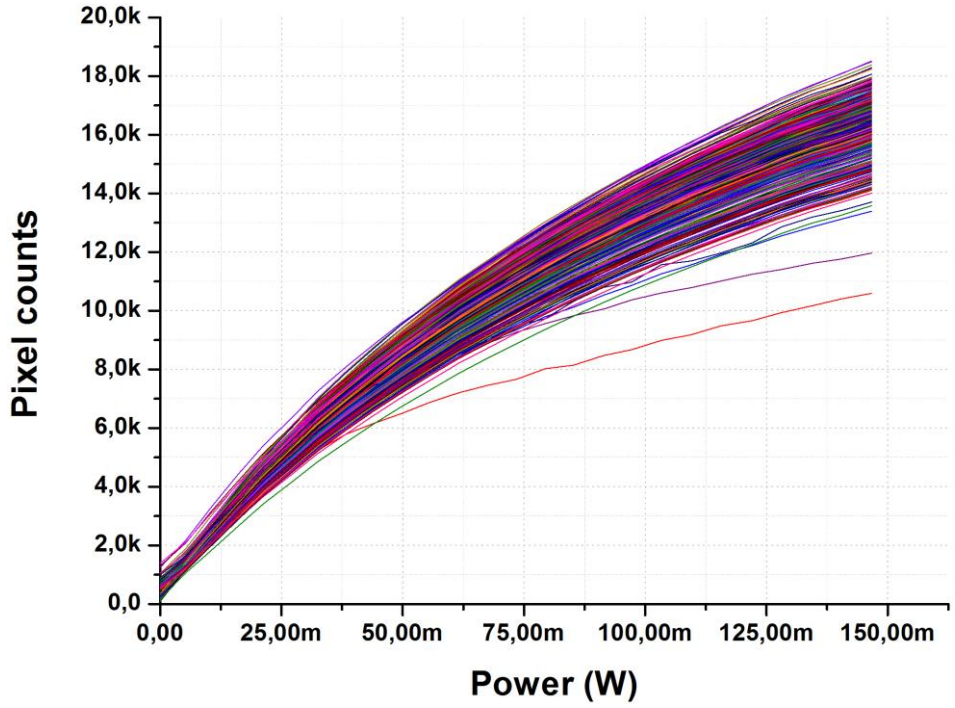

Figure 5.17 Pixel counts as a function of the power consumption of the illumination ring [21].

measured at each irradiance. Then, to eliminate the effect of the PDP variation, for each pixel the resulting value from subtracting the noise counts to the counts measured at each irradiance was multiplied by a correcting factor. The correcting factor shifts the response of each pixel to the average curve. However, given the high deviation, each pixel has its own correcting factor. The 430 correcting factors were calculated at the maximum irradiance (i.e. at the saturation of the optical system) and applied over the measured irradiance range. Spatial maps of the noise counts of all the pixels across the array, counts measured at the maximum irradiance and counts after the subtraction of the noise counts to the counts measured at the maximum irradiance are depicted in Fig. 5.18, Fig. 5.19-left and Fig. 5.19-right, respectively. The spatial map of the resultant counts across the array at the maximum irradiance after having applied to each pixel its correction factor is shown in Fig. 5.20-left. It can be observed that the pixel counts are exactly the same for each pixel (15.98 kcounts). Moreover, this value is equal to the average pixel counts across the array at the same irradiance. However, it is not possible to recover the average value by applying the same correction factors to the other measured irradiances. Fig. 5.20-right plots the spatial map of the pixel counts at the half irradiance after having subtracted the noise counts and applied the correcting factors calculated at the maximum irradiance. In this figure, the corrected pixel counts are different from the average value (10.65 kcounts) and not exactly the same for each pixel. This is a consequence of using a calibration algorithm based on linear equations. Fig. 5.21 shows the curves for all the pixels over the measured irradiance range after the correction. It can be appreciated that the deviation is significantly reduced when compared to the original data (from 6% to 1% of the mean value). As a result, the representation levels and

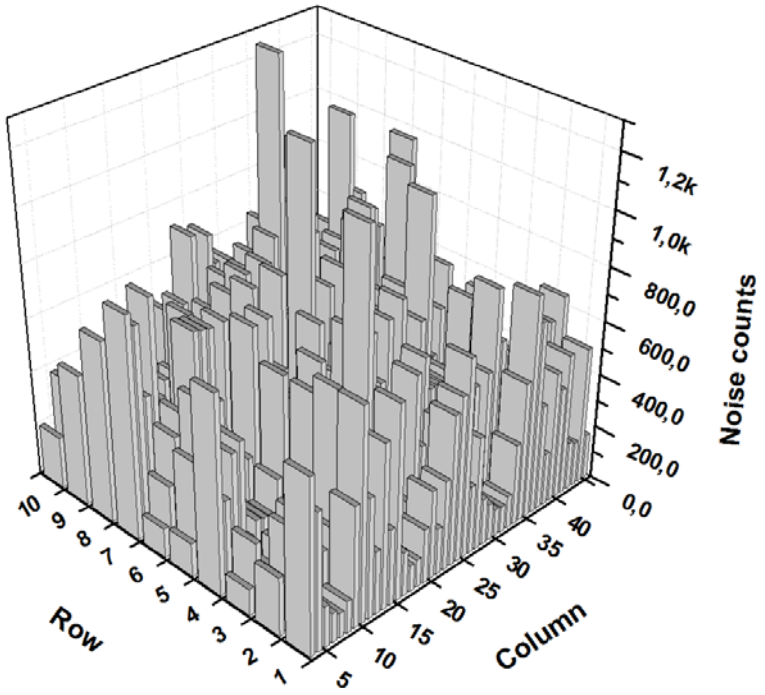

Figure 5.18 Noise counts across the array measured at 1 V of overvoltage.

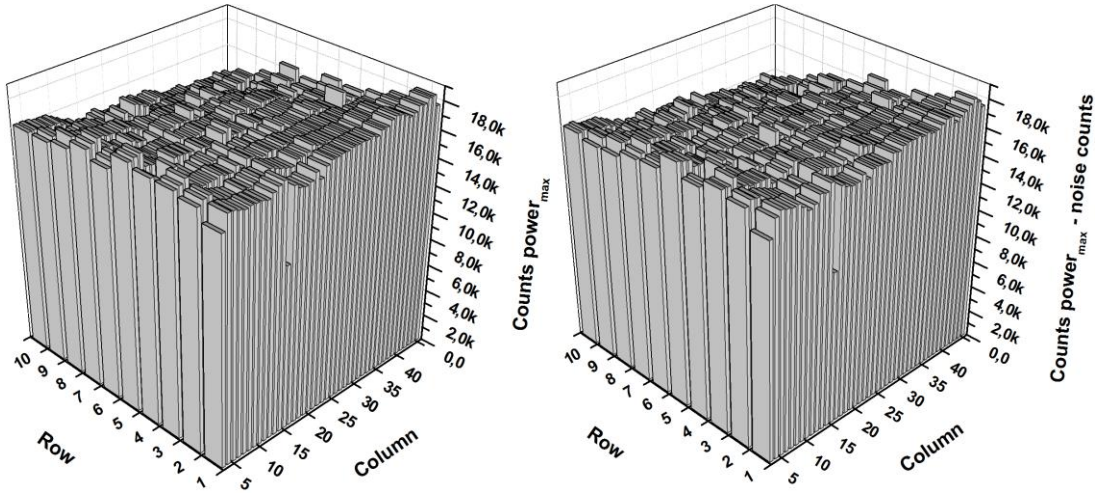

Figure 5.19 Measured counts at the maximum irradiance (left) and measured counts at the maximum irradiance minus the noise counts (right).

thus the number of bits are increased. The original 3.8 bits of the measured data are expanded to 6.9 bits after the correction. Nevertheless, more accurate results could be obtained by means of a calibration algorithm that uses non-linear equations.

As a next step, the capabilities of a calibration algorithm that uses B-splines to equalize the response of all the pixels were investigated. For each pixel, up to four pairs of measured pixel counts versus power consumption were used to generate 256 interpolated pairs equally distributed between the minimum and maximum measurable irradiances (i.e. 256 representation levels). Two of the four pairs of data were obtained in the dark and almost saturation of the

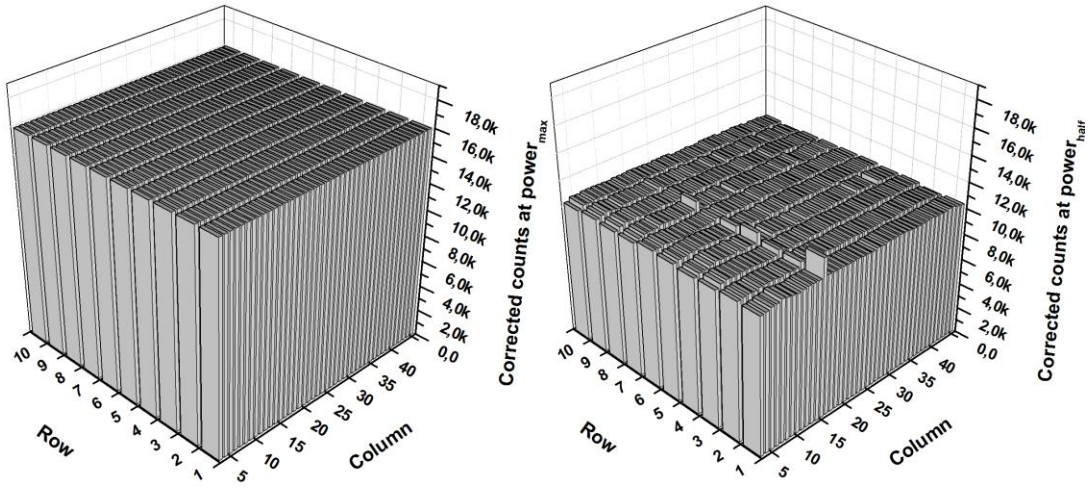

Figure 5.20 Corrected counts at the maximum (left) and half (right) irradiances.

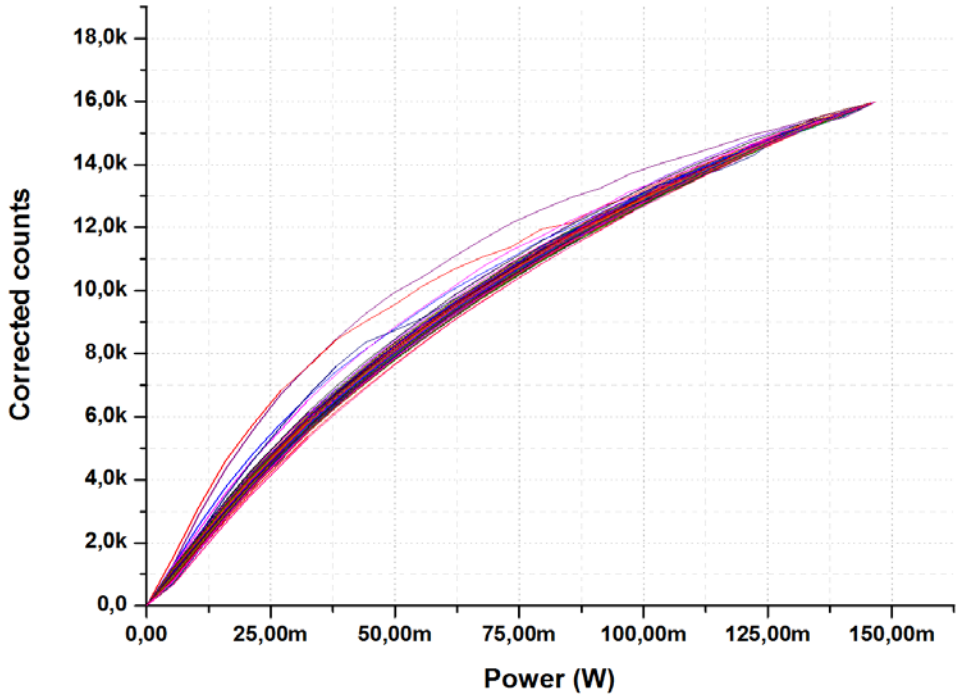

Figure 5.21 Corrected counts over the entire measured irradiance range.

optical system. The other two were distributed in between the irradiance range. It was observed that the higher the number of data points, the higher the accuracy of the adjustment. Then, the lowest pixel value was assigned to level 0 (the darkest black), the following pixel value to level 1, and so on until the highest value was assigned to level 255 (the brightest white). The generated values for each pixel were saved in a LUT that was used to reproduce digital images. Fig. 5.22 shows images obtained with a white background at different irradiances and corrected by means of the linear and non-linear calibration algorithms investigated in this work. It can be appreciated that the images corrected by means of the LUT based algorithm present uniformity.

The same algorithms were used to correct the array non-uniformities in the representation of an object. It can be observed in Fig. 5.23 that the contrast and quality of the generated images are highly increased after the correction with the LUT based algorithm.

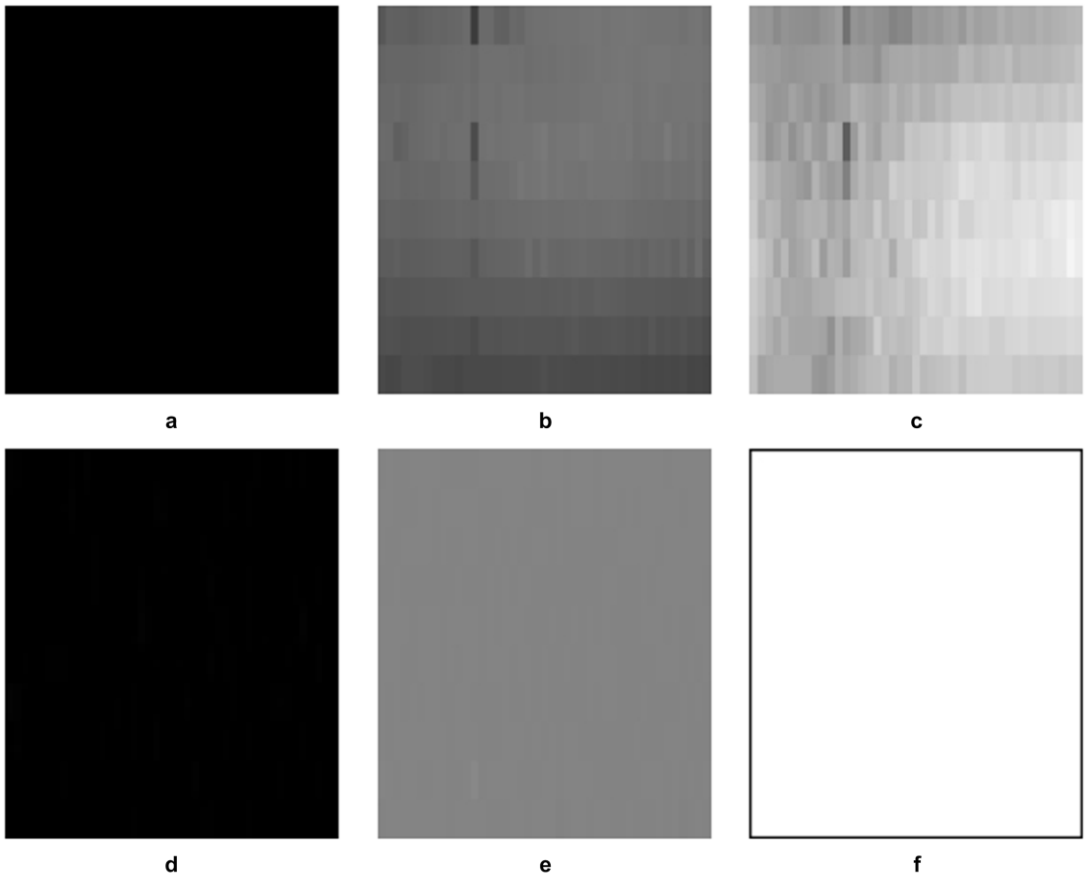

Figure 5.22 Images obtained after correction with the linear algorithm (a, b and c) and the non-linear algorithm (d, e and f). Frames a and d correspond to darkness, b and e to a medium gray, and c and f to white [21].

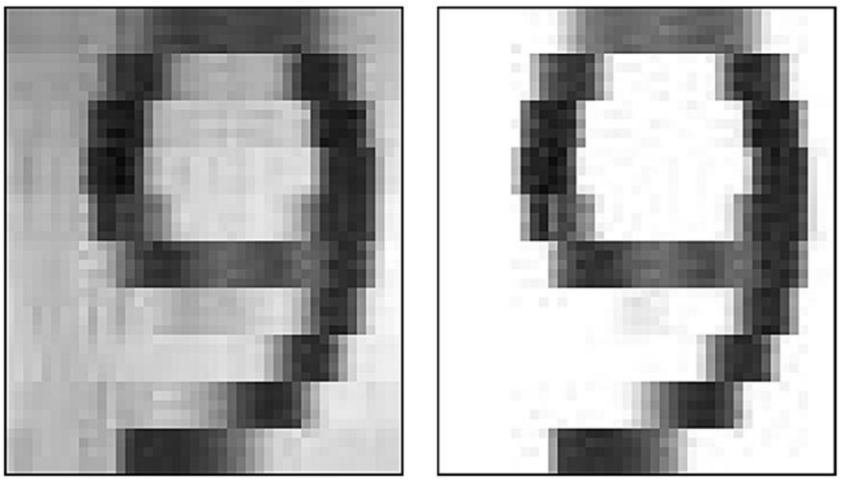

Figure 5.23 Representation of an object after correction with the linear algorithm (left) and the non-linear algorithm (right) [21].

5.4 Discussion

In this chapter, several techniques to improve the performance of the GAPD technology in HEP experiments and light detection applications have been presented and discussed. To start with, a 3D GAPD pixel detector has been designed with the Global Foundries 130 nm/Tezzaron 3D process, which allows the vertical stacking of two layers and therefore improves the fill-factor of the detector. Several array architectures were studied to determine the maximum achievable fill-factor with the proposed technology process and a time-gated readout circuit of minimum area. The final design consists of a 48 x 48 GAPD pixel array, which is composed of two sub-arrays of 48 x 24 pixels each. The first sub-array, where the sensor and the readout electronics are split into the two layers, presents a 66% fill-factor. In contrast, in the second sub-array the sensors are implemented in both tiers to overlap as much as possible the non-sensitive areas due to the sensors and the readout electronics. In this case, a 92% fill-factor is achieved. Therefore, it has been proved that the typical low fill-factor of GAPD detectors can be increased up to values close to 100% with 3D technologies, as required by future linear colliders.

Regarding light detection applications, it has been shown that the time-gated operation is also an effective method to extend the sensitivity of dSiPMs. It has been demonstrated that short gated-on periods generate a low number of pixels being fired by the noise. Therefore the minimum irradiance needed to detect signal above the noise is reduced. As a result, the dynamic range of the detector is extended while the fill-factor achieved by design is preserved. Finally, techniques to increase the contrast of vision systems based on GAPD cameras by minimizing the non-uniformities of the sensor have also been investigated. Pixel-by-pixel calibration algorithms based on both linear and non-linear methods have been used to reduce the typical high deviation of the response of GAPD arrays. As a consequence of the application of these techniques, the representation levels that are available to depict an image, and by extension the contrast, are increased. Nevertheless, due to the non-linear response of GAPD pixels with the irradiance, the best results are achieved with non-linear methods.

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Conclusion

To fully exploit the physics potential of the future particle colliders ILC and CLIC, and thus complement the discoveries made at LHC, detector systems with unprecedented performance are needed. In the case of the tracker detector, the required specifications comprise a single point resolution better than 5 μm, a low material budget of 0.3% X_0 per layer, a fast readout, a reduced occupancy below 1% and radiation tolerance. Among others, one proposed sensor technology for the tracker detector is the GAPD approach. Within the scope of this thesis, a prototype GAPD pixel detector aimed mostly at particle tracking at future linear colliders has been developed, including the design of several prototype chips and the complete characterization of the sensor. The design and the results of the characterization of the prototypes have been thoroughly discussed in this thesis.

The development of a tracker detector capable to meet all the specifications demanded by ILC and CLIC is a defiant field. In the case of GAPD detectors, the two most ambitious aspects make reference to the occupancy and the fill-factor. Despite the single bunch crossing resolution of GAPDs, the high frequency of the pattern noise generated by the sensor increases the occupancy to unacceptable values. In an attempt to minimize this problem, the operation of the detector in the time-gated mode and at low reverse bias overvoltages was conceived as a possible solution. To fully explore the potential of the proposed techniques, two prototype chips were designed and fabricated in the HV-AMS 0.35 μm standard CMOS technology. The first chip, containing several GAPD pixels and small arrays with a sensitive area of 20 μm x 100 μm per pixel and different readout circuits, allowed us to prove that it is possible to suppress the afterpulsing probability with gated-off periods of around 300 ns and reduce the DCP with short gated-on periods in the nanosecond time scale while still preserving to PDP to acceptable levels. Moreover, it was also discovered that gated-on periods of around 3 ns and shorter prevent the apparition of electronic crosstalks, which are present in our devices as a consequence of the common deep n-tub amongst the sensors of the same row as a strategy to increase the fill-factor. Thus, the expected DCP at 1 V of V_{OV} is 10^{-5} noise counts/GAPD/BX at ILC and 10^{-2} noise counts/GAPD/train at CLIC, where the short bunch-spacing of 0.5 ns makes it impossible to operate the present detector in the time-gated mode nor extract the content of the pixels after each bunch crossing. Nevertheless, the expected values of the DCP are, respectively, 5 and 3 orders of magnitude higher than the beam induced backgrounds at both particle colliders and therefore unaffordable.

The second chip, containing a 10 x 43 GAPD pixel array also operated in the time-gated mode, was especially designed to prove the particle detection efficiency of the sensor. To

facilitate the observation of events at a beam-test, the array presents a total sensitive area of 1 mm x 1 mm. It exhibits an unusual fill-factor of 67% as a result of the large sensor area of 20 μm x 100 μm, the reduced number of transistors of the readout circuit and the common deep n-tub amongst the sensors of the same row. Given its proof of concept nature, techniques to mitigate the radiation effects nor on-chip data processing were not included in the prototype. Instead, the information generated by the detector is processed off-chip, after being read out sequentially row by row. Although the detector exhibits a high average DCR of 67 kHz at 1 V of V_{OV} and room temperature, the expected noise counts can be sharply reduced with the time-gated operation and the decrease of the working temperature. Thus, with a gated-on period of 1 ns at a temperature of -20º C, the DCP can be reduced to $1 \cdot 10^{-5}$ noise counts per pixel and frame. If the detector is read out after each bunch crossing and radiation damage is not accounted, $1 \cdot 10^{-5}$ noise counts/GAPD/BX is the expected DCP at ILC. However, due to the short bunch-spacing of 0.5 ns foreseen at CLIC, and the consequent inability to operate the present array in the time-gated mode, $2 \cdot 10^{-2}$ noise counts/GAPD/train are foreseen at CLIC. These values, which are still higher than the beam related backgrounds, could be further reduced by doing the logic AND between the output values of two overlapped pixels from two different layers. In that case, $1 \cdot 10^{-10}$ noise counts/GAPD/BX and $4 \cdot 10^{-4}$ noise counts/GAPD/train would be induced at ILC and CLIC, respectively. Thus, the DCP would be lowered below the expected beam related backgrounds. The results of the beam-tests conducted at CERN-SPS with a gated-on period of 30 ns and a V_{OV} of 1.2 V confirm that the GAPD technology can sense MIPs. Moreover, given the spectral response of the GAPD array within the range 400-1000 nm, the detector is also suited for photon detection applications. A number of complementary experiments conducted on the detector have shown that the time-gated operation also allows to extend the input DR in more than 3 bits, and improve the contrast and spatial resolution of the generated images.

To address the requirement on a 100% fill-factor, the potential of 3D technologies, which allow the vertical stacking of two layers of logic dies, was explored. In particular, the maximum achievable fill-factor by a GAPD pixel array in the Global Foundries 130 nm/Tezzaron 3D process was analyzed with several array architectures and a time-gating readout circuit of minimum area. The study shows that the maximum fill-factor is achieved when the two-layer vertical stack is used to overlap the non-sensitive areas of one layer with the sensitive areas of the other one, and vice versa. Moreover, different sensor areas can be used to further increase the fill-factor. A 3D detector composed of two sub-arrays of 48 x 24 pixels each and with 66% and 92% fill-factors was completely designed. However, it has not been submitted for fabrication given the continuous delays in the MPW runs of the Global Foundries 130 nm/Tezzaron 3D technology. In spite of that, the GAPD pixel detector designed in the

mentioned 3D process demonstrates that the fill-factor of GAPDs can be increased up to values close to 100%, as demanded by future linear colliders on tracker detectors.

Although the performance of the prototypes developed is encouraging, further studies concerning radiation effects and the sensor efficiency in the detection of high energy particles are needed. In addition, a prototype in a 3D technology with small pixels that comply with the required single point resolution, and includes techniques to mitigate radiation effects on the readout electronics, as well as TDCs to tag the incoming signal with a timing label and on-chip processing should be designed and tested.

Resum

Aquesta tesi presenta el desenvolupament d'un detector de píxels de GAPDs (Geiger-mode Avalanche PhotoDiodes) dedicat principalment a rastrejar partícules en futurs col·lisionadors lineals. Els GAPDs ofereixen unes qualitats extraordinàries per satisfer els requisits extremadament exigents d'ILC (International Linear Collider) i CLIC (Compact LInear Collider), els dos projectes per la propera generació de col·lisionadors que s'han proposat fins a dia d'avui. Entre aquestes qualitats es troben una sensibilitat extremadament elevada, un guany virtualment infinit i una resposta molt ràpida, a part de la compatibilitat amb les tecnologies CMOS estàndard. En concret, els detectors de GAPDs fan possible la conversió directa d'un esdeveniment generat per una sola partícula en un senyal CMOS digital amb un temps inferior al nanosegon. Com a resultat d'aquest fet, els GAPDs poden ser llegits després de cada bunch crossing, una qualitat única que cap dels seus competidors pot oferir en el moment actual. Malgrat tots aquests avantatges, els detectors de GAPDs pateixen dos grans problemes. D'una banda, existeixen fenòmens de soroll inherents al sensor, els quals indueixen polsos de soroll que no poden ser distingits d'esdeveniments reals generats per partícules i que a més empitjoren l'ocupació del detector a nivells inacceptables. D'altra banda, el fill-factor (és a dir, l'àrea sensible respecte l'àrea total) és molt baix i redueix l'eficiència detectora. En aquesta tesi s'han investigat solucions als dos problemes comentats i que a més compleixen amb les especificacions altament severes dels futurs col·lisionadors lineals.

1. Futurs col·lisionadors lineals de leptons i altres aplicacions potencials

La física d'altes energies és la branca de la ciència que estudia els components elementals de la matèria i les interaccions entre ells. L'existència d'aquests components i les seves interaccions es descriu en models teòrics, els quals són provats mitjançant experiments que es porten a terme en col·lisionadors de partícules. Als col·lisionadors, els acceleradors impulsen feixos de partícules a energies de l'ordre dels GeV abans de fer-los col·lisionar entre ells. Els resultats d'aquestes col·lisions són enregistrats pels detectors. Actualment, existeixen dos tipus d'acceleradors d'altes energies. D'una banda, els sincrotrons, on les partícules accelerades segueixen un anell circular de radi constant. D'altra banda, els acceleradors lineals, on les partícules presenten un moviment lineal. En ambdós casos, els feixos de partícules accelerats es fan col·lisionar a la regió del detector.

A dia d'avui, l'accelerador de partícules més potent del món es l'LHC (Large Hadron Collider), que es troba al CERN (European Organization for Nuclear Research) a prop de Ginebra (Suïssa). En aquesta màquina, s'acceleren dos feixos d'hadrons que circulen en direccions oposades en un anell de 27 km de longitud situat sota terra. Es preveu que quan s'hagi assolit la màxima energia, els feixos d'hadrons accelerats arribaran als 7 TeV cadascun a una lluminositat nominal (nombre de partícules per unitat d'àrea i per unitat de temps) d'$1 \cdot 10^{34}$ $cm^{-2}s^{-1}$. Entre altres descobriments, els experiments duts a terme a l'LHC han permès confirmar l'existència d'una nova partícula el 2012. La nova partícula és presumiblement el bosó de Higgs, l'últim element del model estàndard de la física de partícules que restava per observar. Tanmateix, calen nous experiments per poder assegurar aquest fet amb certesa, així com estudiar amb detall les propietats d'aquesta partícula. Tot i l'extraordinària capacitat de l'LHC, la precisió d'aquesta màquina està intrínsecament limitada, ja que en col·lisionar hadrons contra hadrons resulta impossible determinar amb exactitud l'energia inicial de cadascun dels feixos.

Per tal de resoldre aquest problema, la comunitat científica ja ha començat a treballar en l'era post-LHC. Hi ha un consens mundial que estarà caracteritzada per col·lisionadors de leptons, on les col·lisions entre electrons i positrons permetran realitzar mesures de precisió i per tant examinar profundament la nova partícula. No obstant, construir un col·lisionador circular de leptons no és una opció. Quan una partícula s'accelera en una trajectòria circular, pateix pèrdues d'energia en forma de radiació electromagnètica (també anomenades radiació de sincrotró). La radiació de sincrotró és inversament proporcional a la quarta potència de la massa de les partícules i al radi de curvatura de l'accelerador. Com que l'electró és una partícula lleugera, acceleradors circulars de leptons de només uns centenars de GeV patirien unes pèrdues de radiació de sincrotró tan grans, que farien falta compensacions energètiques inviables per poder assolir l'energia nominal. Incrementar el radi de l'anell tampoc és una opció a causa dels elevats costos econòmics que se'n derivarien. Per tots aquests motius, la comunitat científica ha decidit que el proper gran col·lisionador, encarregat de complementar i ampliar els descobriments sorgits de l'LHC, serà un col·lisionador lineal de leptons. A més, també s'ha acordat que l'energia nominal d'aquest proper col·lisionador es trobarà en l'escala dels TeV. Fins a dia d'avui, s'han proposat dos projectes alternatius que podrien complir els requisits demanats als futurs col·lisionadors lineals. Són els anomenats ILC i CLIC.

En un col·lisionador lineal, les partícules són accelerades seguint trajectòries rectes i oposades en cadascun dels dos acceleradors lineals o linacs, fins que assoleixen l'energia nominal i col·lisionen a la regió del detector. Les partícules s'agrupen en els anomenats feixos de partícules i cada col·lisió es coneix amb el nom de bunch crossing o BX. Diversos BXs separats per un espai temporal curt formen un tren de BXs. La lluminositat requerida pels experiments només es pot assolir mitjançant la freqüència de repetició adequada dels BXs,

nombre de BXs en un tren, nombre de partícules en cadascun dels dos BXs, secció del feix al punt de la col·lisió i interacció mútua entre els feixos. La interacció mútua entre els feixos és conseqüència del signe de càrrega oposat que presenten les partícules dels dos feixos. Aquesta atracció provoca una desviació en la trajectòria de les partícules, cosa que indueix la irradiació de fotons. Els fotons deguts a aquest fenomen, conegut com a procés beamstrahlung, no estan relacionats amb partícules generades durant les col·lisions i per tant són considerats soroll de fons. El soroll de fons pot induir ocupacions elevades i per tant s'ha de procurar minimitzar-ne les conseqüències mitjançant estratègies de lectura adequades o píxels d'àrea petita. La Taula R.1 presenta un resum de les propietats principals del feix als col·lisionadors ILC i CLIC.

Els objectius de la física a ILC i CLIC imposen requisits molt exigents al detector. Aquestes qüestions han estat abordades en dues propostes diferents, les validades ILD (International Linear Detector) i SiD (Silicon Detector), les quals estan basades en una estructura comuna però tecnologies complementàries. Ambdues propostes presenten un detector format per diversos subsistemes de strips i píxels de silici amb forma de barril i disc que envolten el feix de partícules. Aquestes subsistemes són essencialment el detector de vèrtexs, el detector de traces, el calorímetre i el detector de muons. La Taula R.2 detalla els diferents subsistemes d'ILD i SiD, així com la tecnologia de cadascun d'ells. Tot i que els detectors proposats a ILD i SiD van ser originalment ideats per ILC, CLIC ha adoptat les mateixes propostes ja que també necessita un detector adequat per un col·lisionador que treballa a l'escala dels TeV.

Els requisits que demanen ILD i SiD al sistema detector es poden resumir com:

• Resolució espacial millor que 5 μm, o el que és el mateix, píxel de mida no superior a 17 μm

• Gruix inferior a 0.15% (ILD) o 0.30% (SiD) X_0 per capa, on X_0 és la longitud de radiació, per minimitzar la dispersió de Coulomb múltiple

• Alta granularitat per a una bona separació de les partícules

• Resolució temporal que permeti distingir un sol BX

• Ocupació inferior a l'1%, incloent el soroll de fons

• Tolerància a la radiació

• Consum promig inferior a uns quants mW/cm^2

• Immunitat a fenòmens EMI (ElectroMagnetic Interference)

• Un cost raonable

Paràmetres del feix	ILC	CLIC
Energia del centre de masses	500GeV (1TeV)	500GeV (3TeV)
Lluminositat ($\cdot 10^{34}cm^{-2}s^{-1}$)	1.49 (2.70)	2.3 (5.9)
Repetició del tren (Hz)	5	50
Bunches/tren	2820	354 (312)
Separació entre bunches (ns)	337	0.5
Partícules/bunch ($\cdot 10^{9}$)	7.5	6.8 (3.72)
Mida horitzontal del feix (nm)	640	200 (40)
Mida vertical del feix (nm)	5.7	2.26 (1)

Taula R.1 Comparació entre els col·lisionadors ILC i CLIC.

Proposta ILD		Proposta SiD	
Subsistema	**Tecnologia**	**Subsistema**	**Tecnologia**
Detector de vèrtexs	Píxels de silici	**Detector de vèrtexs**	Píxels de silici
	- 3 barrils de doble capa		- 5 barrils - 4 discs forward - 4 discs backward - 3 discs
SIT	Strips de silici	**Detector de traces**	Strips de silici
	- 2 capes		
SET	Strips de silici		- 5 barrils - 4 discs
	- 2 capes		
TPC	Lectura MPGD		
ECAL	Absorbent de W	**ECAL**	Píxels de silici-W
HCAL	Absorbent de Fe	**HCAL**	RPC-acer
Bobina	Camp de 35 T	**Solenoide**	SC de 5 Tesla
Muó	Capes centellejadores	**Retorn de flux (sistema de muons)**	Centellejador-acer

Taula R.2 Tecnologies dels diferents subsistemes del detector segons les propostes ILD i SiD. SIT correspon a Silicon Internal Tracker, SET a Silicon External Tracker, TPC a Time Projection Chamber, ECAL a Electromagnetic CALorimeter, HCAL a Hadron CALorimeter, MPGD a Micro-Pattern Gas amplification Detectors, RPC a Resistive Plate Chamber i SC a SemiConductor.

Donat l'extremisme d'aquests requisits, actualment no hi ha cap tecnologia disponible al mercat que els satisfaci tots. Aquest fet ha motivat el desenvolupament de nous sistemes detectors de forma paral·lela a l'accelerador. Els detectors que concentren la major part de la recerca es basen en tecnologies de píxels CMOS, ja sigui monolítiques, híbrides o 3D. Els principals dispositius sensors són els anomenats DEPFET (DEPleted Field Effect Transistors), MAPS (Monolithic Active Pixel Sensors) i FPCCD (Fine Pixel Charge Coupled Devices). Tecnologies alternatives són els Chronopixels, Timepix i GAPDs. Una altra possibilitat passar

per explorar noves tecnologies emergents, com poden ser les tecnologies SOI (Silicon-On-Insulator) i 3D. Les principals característiques dels detectors proposats es resumeixen a la Taula R.3. En aquesta tesi es presenta el desenvolupament d'un detector de píxels de GAPDs, l'aplicació principal del qual és rastrejar partícules a ILC i CLIC.

A part dels experiments de física d'altes energies en futurs col·lisionadors lineals, existeix un ampli espectre d'aplicacions que requereixen mesurar radiació i que per tant podrien beneficiar-se de les propietats extraordinàries dels GAPDs. D'una banda, hi ha els experiments en altres col·lisionadors de partícules, com per exemple el TOTEM (TOTal Elastic and diffractive cross-section Measurement). Aquest experiment del CERN, que actualment es troba en fase de realització, està dedicat a estudiar amb gran detall l'estructura dels protons i les interaccions dels protons a altes energies. Tot i que està prenent dades de manera satisfactòria des del 2010, s'està estudiant la possibilitat d'equipar parcialment algun dels detectors amb tecnologies 3D planars o GAPDs. Els GAPDs són especialment interessants per aquest experiment, donat que ofereixen la possibilitat d'aconseguir una resolució temporal de 10 ps durant les mesures. D'altra banda, hi ha el camp de la detecció de senyals òptics en el visible i infraroig proper. En aquest cas, les aplicacions d'interès són tan diverses com la generació d'imatges biomèdiques, l'espectroscòpia Raman i d'infraroig proper, càmeres 3D, mesura de distàncies i l'espai. Algunes aplicacions d'especial interès que podrien beneficiar-se dels GAPDs són aquelles que utilitzen les tècniques AFI (AutoFluorescence Imaging), SPECT (Single-Photon Emission Computed Tomography) i CT (Computed Tomography).

2. Fotodíodes d'allau operats en el mode Geiger

Una junció p-n inversament polaritzada per sobre de la seva tensió de ruptura (V_{BD}) i equipada amb circuits de quenching i recàrrega constitueix essencialment un GAPD. Quan la junció p-n absorbeix fotons o partícules ionitzades, es pot disparar un procés de multiplicació de portadors de càrrega, també anomenat allau, que deriva en un pols de corrent macroscòpic. Donat que el fotodíode està polaritzat per sobre de V_{BD}, el procés de generació de càrrega per allau és auto-sostingut. Com a conseqüència, els GAPDs tenen un guany intern virtualment infinit de 10^5-10^6 independentment del nombre inicial de portadors de càrrega. Concretament, una allau pot ser disparada per un sol fotó o MIP (Minimum Ionizing Particle). No obstant, la mera absorció d'un fotó o d'un MIP no és suficient per generar una allau, sinó que aquest fet està condicionat per una probabilitat que depèn de la posició a la zona de càrrega espacial on s'absorbeix la radiació. Per tal d'evitar que l'allau generada destrueixi el dispositiu, el circuit de quenching atura l'allau disminuint la polarització del sensor fins a o per sota de V_{BD}. O el que és el mateix, el circuit de quenching força la generació al node sensible del GAPD d'un voltatge

Detector	DEPFET	MAPS	FPCCD	Chrono.	Timepix	GAPD	SOI
Re. espacial (μm)	~1	~3	–	~3	2.3	~5	~1
Gruix (μm)	50	50	50	50 - 100	300	250	70
Gran. (μm x μm)	20 x 20	18.4 x 18.4	5 x 5	10 x 10	55 x 55	20 x 100	13.75 x 13.75
Re. temporal	integració	integració	integració	stamping	stamping	cada bunch	integració
Tolerància a radiació	10 kGy	10 kGy 10^{13} n_{eq}/cm^2	10^{12} e^-/cm^2	–	4 Mgy	–	1 kGy
Consum	5 W	250 mW/cm^2	16 mW/ch	–	886 mW/cm^2	–	–
Fill-factor (%)	100	100	100	100	87	67	100

Taula R.3 Característiques principals dels detectors proposats pels futurs col·lisionadors lineals.

d'amplitud igual o superior a la tensió per sobre de V_{BD} a la que està polaritzat el sensor. Per rehabilitar el sensor per futures deteccions, el circuit de recàrrega restaura la polarització del sensor. El pols de corrent generat pot ser fàcilment detectat per l'electrònica de lectura.

Quan la junció està polaritzada just per sota de V_{BD}, es diu que opera en el mode lineal. En aquest mode, el procés de generació de càrrega per allau no és auto-sostingut i per tant el guany del dispositiu és proporcional al flux de radiació incident. Aquest guany moderat, que a més es veu seriosament afectat per soroll de fons, fa que els APDs (Avalanche PhotoDiodes) lineals no siguin adequats per detectar fotons individuals o MIPs. És per aquest motiu que el detector de fotodíodes desenvolupat en aquesta tesi opera en el mode Geiger i no en el mode lineal.

El rendiment dels GAPDs normalment es caracteritza mitjançant una sèrie de figures de mèrit, com són el DCR (Dark Count Rate), afterpulsing, crosstalk, sensibilitat a partícules altament energètiques, PDP (Photon Detection Probability) i resolució temporal. El DCR, afterpulsing i crosstalk són fenòmens de soroll inherents al sensor, els quals generen allaus que no estan relacionades amb l'absorció de senyal extern. La detecció de partícules altament energètiques i PDP tenen a veure amb les capacitats de disparar allaus i de detecció del dispositiu, mentre que la resolució temporal fa referència a l'interval de temps transcorregut entre l'arribada del senyal extern i la generació del flanc de pujada del senyal de sortida. Donat que en aquesta tesi es dóna especial rellevància a la reducció del soroll per augmentar l'eficiència del sensor, el DCR, l'afterpulsing i el crosstalk seran explicats amb més detall tot seguit.

El DCR ve donat per aquelles allaus no relacionades amb l'absorció de senyal extern ni correlacionades amb allaus anteriors. Els mecanismes principals que contribueixen a la generació del DCR són els portadors tèrmics i l'efecte túnel. El DCR causat per portadors tèrmics depèn del procés de fabricació, la superfície del GAPD, la tensió per sobre de V_{BD} a la

qual es polaritza el sensor per operar en mode Geiger i la temperatura de treball. En canvi, l'efecte túnel és extremadament dependent de la tensió per sobre de V_{BD} a la qual es polaritza el sensor i del perfil de dopatge del dispositiu. El DCR es defineix com nombre d'allaus per segon i per tant té unitats de freqüència o Hz. Aquest paràmetre limita la detecció de senyals òptics d'intensitat baixa. Per tant, és molt important tenir-lo ben caracteritzat.

L'afterpulsing és un tipus de soroll correlacionat típic dels GAPDs. Quan es dispara una allau en un GAPD, ja sigui a causa d'un fenomen de soroll o d'un senyal extern, es genera un gran nombre de portadors de càrrega que circulen a través de la zona de càrrega espacial. Alguns d'aquests portadors poden quedar atrapats en centres de captura durant un temps finit. Si els portadors atrapats són alliberats després que el detector hagi recuperat la seva capacitat multiplicadora, poden generar una nova allau i induir un fenomen de soroll que s'anomena afterpulse. La probabilitat d'afterpulsing depèn del nombre de centres de captura i de la quantitat de portadors de càrrega que circulen per la regió de multiplicació durant una allau. Donat que reduir del nombre de centres de captura no és una opció, la probabilitat d'afterpulsing només es pot reduir limitant el nombre de portadors. Això es pot aconseguir disminuint la capacitat paràsita associada al node sensible del GAPD o bé forçant l'extinció prematura de l'allau mitjançant circuits de quenching actius. Una altra opció passa per incrementar artificialment el temps mort del GAPD (temps que transcorre des que es produeix l'allau fins que el sensor recupera la seva polarització d'operació) fins que el sensor hagi alliberat totes les càrregues atrapades.

El crosstalk és un segon tipus de soroll correlacionat que es troba en matrius de GAPDs, és a dir, diversos píxels de GAPDs agrupats formant un sol detector. Aquest fenomen ocorre sempre que una allau generada en un píxel dispara una allau secundària en un píxel veí. Segons el mecanisme de generació de crosstalk, es pot distingir entre crosstalk elèctric i òptic. En aquelles matrius on els GAPDs comparteixen el mateix pou, alguns dels portadors generats en una allau poden difondre a través del pou, arribar a un GAPD veí i eventualment disparar una nova allau. Aquest fenomen correspon a un crosstalk elèctric. Es pot eliminar col·locant els GAPDs en pous diferents, però a costa de reduir el fill-factor del detector. En canvi, el crosstalk òptic té lloc quan els fotons que emet un GAPD en allau com a conseqüència de l'electroluminescència són detectats per GAPDs propers. El crosstalk òptic pot ser reduït limitant el corrent que circula per un GAPD durant una allau o bé rodejant cada píxel mitjançant un fossat profund farcit de polisilici.

Pel que fa al procés de fabricació, els GAPDs poden ser produïts mitjançant tecnologies a mida o bé mitjançant tecnologies CMOS. Els GAPDs desenvolupats en aquesta tesi es troben en tecnologies CMOS estàndard per tal de treure profit dels avantatges que aquestes ofereixen, com

són processos de fabricació robusts a baix cost i la possibilitat d'integrar en un mateix xip el sensor juntament amb l'electrònica de lectura. Aquesta última característica permet reduir la capacitat paràsita del node sensible del detector, cosa que al mateix temps disminueix el nombre de portadors generats durant una allau i per tant fenòmens de soroll com l'afterpulsing o el crosstalk. A més, la resposta dinàmica del sensor també en resulta beneficiada. Com a contrapartida, donat que els processos CMOS se centren en la fabricació de transistors en lloc de detectors òptics, el disseny dels GAPDs es veu afectat per certes limitacions. Concretament, un dels aspectes més dificultosos és l'obtenció d'un mecanisme eficient que permeti suavitzar el camp elèctric a les vores de la junció, per aconseguir així una regió de multiplicació uniforme i evitar la ruptura prematura del dispositiu. Aquest problema se sol solucionar mitjançant anells de guarda amb un perfil de dopatge baix, però a costa de disminuir el fill-factor del detector. Un altre aspecte negatiu dels GAPDs fabricats amb tecnologies CMOS és l'elevada presència de fenòmens de soroll, sobretot en aquelles tecnologies submicròniques.

Els circuits de quenching i recàrrega, necessaris per aturar l'allau i restaurar la polarització del sensor, poden ser implementats mitjançant diverses configuracions actives o passives. Els circuits de quenching passius típicament estan formats per una resistència o un transistor en sèrie amb el sensor, mentre que els circuits de quenching actius requereixen una electrònica més complexa capaç de detectar ràpidament el corrent generat pel GAPD i actuar sobre ell. Els circuits de quenching actius minimitzen el temps de quenching, i per tant també el nombre de portadors generats pel GAPD durant una allau, però són difícils d'implementar i ocupen més àrea. Pel que fa als circuits de recàrrega, en l'opció passiva el mateix element de quenching pot ser utilitzat per polaritzar de nou el sensor per sobre de V_{BD}. En canvi, en l'opció activa habitualment s'implementa un transistor MOS que és activat de forma convenient. Una característica interessant dels circuits de recàrrega actius és que permeten retardar la recàrrega del sensor de manera intencionada per tal de buidar-lo de portadors de càrrega i així mitigar els efectes de l'afterpulsing. Aquest temps de retard intencionat s'anomena temps de hold-off. A la Fig. R.1 es mostren els esquemes típics d'un circuit de lectura amb quenching i recàrrega passives i d'un circuit de lectura amb quenching i recàrrega actives.

Segons el mode d'operació, es distingeix entre GAPD en free-running o en time-gated. En el mode free-running, el detector està sempre polaritzat per sobre V_{BD} a una tensió fixada. D'aquesta manera, el GAPD està sempre preparat per disparar una allau, ja sigui induïda per un esdeveniment real o per un fenomen de soroll. Hi ha algunes aplicacions, però, on es pot conèixer el temps d'arribada del senyal que es vol detectar amb anterioritat a la seva generació, com és el cas dels experiments de física d'altes energies. En aquests casos, pot ser més convenient operar el GAPD en el mode time-gated, en el qual la polarització del sensor disminueix per sota de V_{BD} i incrementa per sobre de V_{BD} de forma periòdica. Fent coincidir els

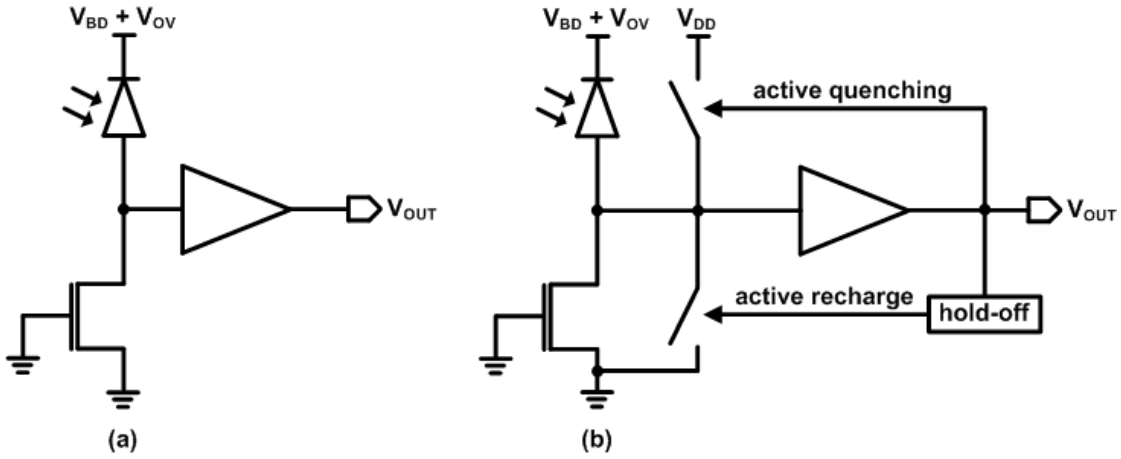

Figura R.1 Esquema típic d'un circuit de lectura amb quenching i recàrrega passives (a) i d'un circuit de lectura amb quenching i recàrrega actives (b).

períodes actius del sensor amb el moment d'arribada del senyal, es pot reduir considerablement la probabilitat de detectar els fenòmens de soroll sense tenir pèrdues d'informació. La polarització periòdica del sensor es pot aconseguir mitjançant diverses tècniques, com per exemple aplicant una tensió tipus quadrada o sinusoïdal d'alta freqüència o bé activant i desactivant convenientment transistors MOS que es troben al circuit de lectura. Esquemes típics per operar el GAPD en el mode time-gated es mostren a la Fig. R.2.

Els polsos de corrent generats en un GAPD com a conseqüència d'una allau solen ser detectats mitjançant l'electrònica que es troba als circuits de lectura. Els circuits de lectura poden trobar-se juntament amb el sensor en el mateix xip o bé en un xip a part. En el primer cas es diu que es té un detector de píxels monolíticament integrat, mentre que en el segon cas es té un detector de píxels híbrid. En ambdós casos, els circuits de lectura inclouen forçosament un discriminador d'allaus, essent l'inversor CMOS l'opció més utilitzada, tot i que comparadors de voltatge i circuits tipus source follower també són habituals. A més, els circuits de lectura poden integrar altres components, com per exemple comptadors, TDCs (Time-to-Digital Converters) o memòries. Una altra opció per comptar els polsos generats pel detector és utilitzar un comptador extern, per exemple en una FPGA. Les matrius de GAPDs poden llegir-se mitjançant diverses estratègies, essent l'accés aleatori, aleatori per files o columnes, per interrupcions i pipelined les més populars.

3. Disseny i caracterització de píxels aïllats i petites matrius en un procés HV-CMOS

L'elecció d'una tecnologia apropiada és una decisió d'extrema importància en el moment d'iniciar el desenvolupament d'un nou detector. En el cas particular dels GAPDs, la tecnologia afecta la sensibilitat, el soroll i el fill-factor del dispositiu. En aquesta tesi, s'han investigat dues

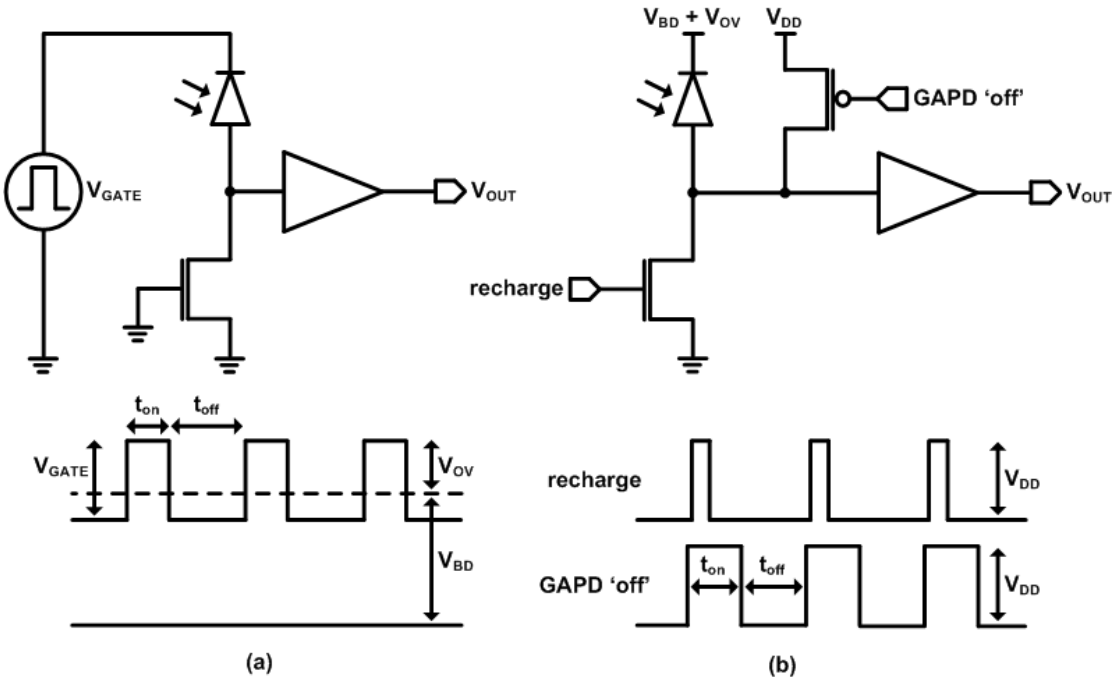

Figura R.2 Esquema típic i formes d'ona per operar el GAPD en el mode time-gated mitjançant un voltatge d'alta freqüència (a) i transistors MOS (b).

tecnologies. D'una banda, la tecnologia CMOS estàndard HV-AMS 0.35 µm perquè proporciona un bon compromís entre el DCR i el soroll. D'altra banda, la tecnologia CMOS estàndard Global Foundries 130 nm integrada en 3D per Tezzaron per maximitzar el fill-factor del detector. En aquesta secció, es presenta el disseny i els principals resultats aconseguits mitjançant píxels aïllats i petites matrius en la tecnologia CMOS estàndard HV-AMS 0.35 µm.

Tots els detectors de píxels basats en GAPDs que s'introdueixen en aquesta secció estan formats per un sensor amb una àrea sensible de 20 µm (amplada) x 100 µm (alçada) i un circuit de lectura monolíticament integrat. El disseny del sensor està basat en l'estructura proposada per Rochas. L'àrea del sensor va ser escollida per satisfer el requisit de resolució espacial demanat pels futurs col·lisionadors. Així, l'amplada del sensor de 20 µm compleix aproximadament amb l'amplada requerida de 17 µm, mentre que la direcció radial del sensor s'ha relaxat a 100 µm per tal de minimitzar la confusió local al disc del detector. Pel que fa als circuits de lectura, tots inclouen alguna estratègia que permet reduir el soroll generat pel sensor. En aquest sentit s'han explorat circuits de lectura que permeten operar el sensor a baixes polaritzacions per reduir el DCR, tant amb discriminadors d'allaus en mode voltatge com en mode corrent. A més, donat que als futurs detectors de partícules l'instant de l'esdeveniment és un paràmetre que pot ser conegut amb antelació, els detectors poden ser operats en el mode time-gated com una alternativa per reduir el soroll detectat sense perdre senyal real.

A la Fig. R.3 es mostra l'esquema genèric del píxel amb el circuit de lectura en mode voltatge, juntament amb l'esquema elèctric del sensor. Respecte al circuit de lectura, a la mateixa figura es poden observar els transistors actius per operar el sensor en el mode time-gated (és a dir, transistors per resetejar (M_{N0}) i inhibir (M_{P0}) el sensor en el moment adequat), el el discriminador en mode voltatge i una porta de pas que en ser activada permet extreure el contingut del píxel (M_{N11}). El discriminador en mode voltatge pot mostrejar la sortida del fotodíode o bé guardar l'últim valor observat. El mostreig té lloc durant els períodes actius del sensor (anomenats t_{obs}), mentre que el valor es guarda durant els períodes no actius (anomenats t_{off}). L'extracció del contingut del píxel es produeix durant els períodes no actius. El reset, la inhibició i el mostreig del sensor, així com l'extracció del contingut del píxel, estan controlades pels senyals externs RST, INH, CLK1 i CLK2, respectivament (veure Fig. R.4 per les formes d'ona juntament amb la resposta del detector). El càtode del fotodíode està polaritzat a un voltatge positiu $V_{HV}=V_{BD}+V_{OV}$, on V_{OV} és la polarització per operar el mode Geiger. Les allaus són detectades a l'ànode, el qual és anomenat V_S. L'electrònica es polaritza entre V_{DD} i V_{SS}, essent 3.3 V la diferència entre aquestes dues tensions en aquesta tecnologia. Cal notar que el píxel no inclou elements addicionals pel quenching de les allaus, sinó que aquestes s'apaguen quan el corrent generat pel GAPD ha induït a l'ànode un voltatge igual a V_{OV}. El transistor M_R es va incloure per estudiar la resposta del detector per diferents temps de recàrrega, però no s'utilitza en el mode time-gated. C_P és la capacitat paràsita associada al node sensible, amb un valor d'entre 10 fF i 30 fF segons el circuit de lectura, mentre que la capacitat del díode és de 540.19 fF a 1 V de V_{OV}.

Pel que fa als discriminadors en mode voltatge, s'han dissenyat i caracteritzat 3 circuits amb topologies diferents. Tot els circuits inclouen un discriminador que permet detectar el voltatge que es genera al node sensible del GAPD en produir-se una allau i una cel·la de memòria d'1 bit. No obstant, l'estratègia integrada a cada circuit per poder detectar voltatges baixos és diferent. Així, en el primer cas el discriminador és un inversor CMOS amb una tensió llindar fixada per disseny a $V_{DD}/2$, el qual presenta una massa diferent a la del GAPD per poder detectar voltatges baixos. Una altra estratègia provada que utilitza només una massa inclou un level-shifter, el qual incrementa el voltatge generat a la sortida del fotodíode perquè pugui ser detectat per un inversor CMOS amb una tensió llindar també a $V_{DD}/2$. Aquest circuit requereix una entrada addicional per la seva pròpia polarització i ocupa més àrea. En l'últim cas, s'ha optat per integrar el discriminador i la cel·la de memòria d'1 bit en un sol circuit anomenat comparador track-and-latch. Aquest circuit també requereix una entrada addicional per la tensió de referència.

La caracterització experimental d'aquests píxels ha permès comprovar l'eficiència dels mètodes proposats per reduir el soroll del sensor. Per la caracterització, el xip fabricat amb els

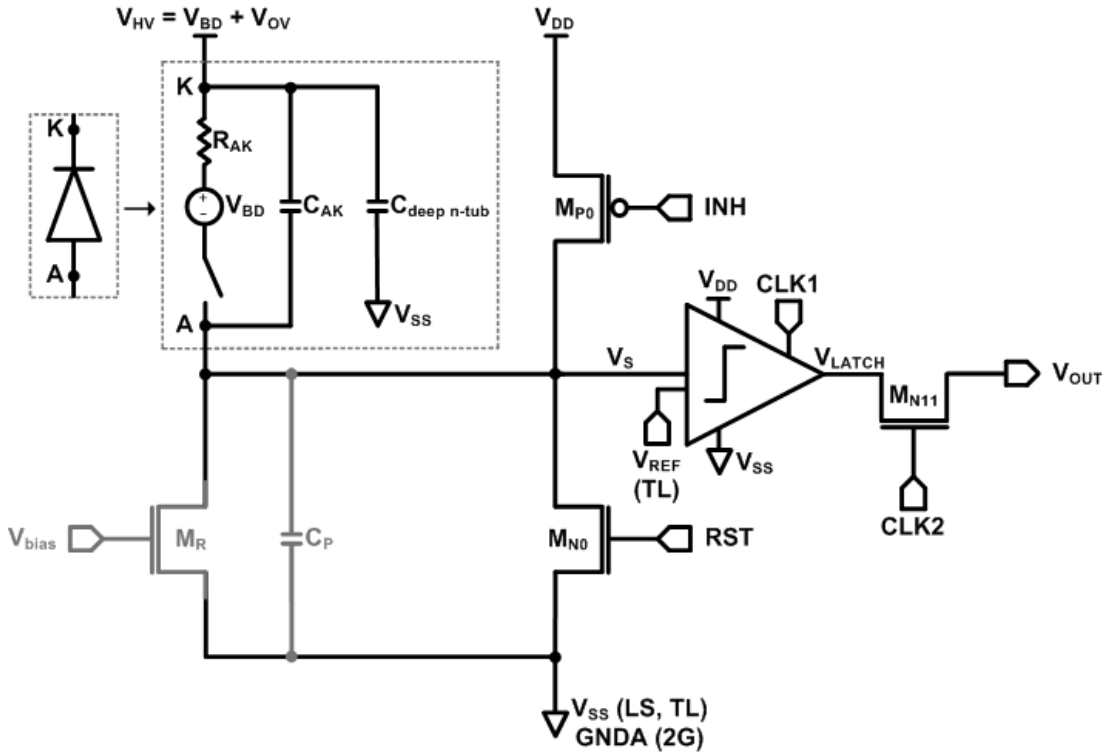

Figura R.3 Esquema genèric del píxel de GAPDs. GNDA és el node de massa del sensor en la topologia de les dues masses (2G), mentre que V_{SS} és utilitzat en les topologies del level-shifter (LS) i del comparador track-and-latch (TL). V_{REF} és utilitzat només en la topologia TL.

píxels s'ha col·locat en una PCB i s'ha polaritzat amb una font de voltatge. Per generar els senyals de control dels píxels (RST, INH, CLK1 i CLK2), s'ha utilitzat una placa de control basada en un FPGA Stratix II d'ALTERA. La placa de control també s'ha utilitzat per comptar off-chip el nombre de polsos generats pels detectors i gestionar la comunicació amb un ordinador a través d'un port USB. L'ordinador controla el muntatge experimental amb el suport d'un programari dedicat. La caracterització del sensor s'ha realitzat amb un temps total de mesura programable (t_m) que depèn del període t_{obs} i del nombre de vegades que aquest és repetit (n_{rep}). S'han utilitzat diferents t_{obs} des de 10 ns fins a 1280 ns i diferents V_{OV} de 0.5 V, 1 V i 1.5 V.

La caracterització experimental del soroll del sensor en funció del t_{off} ha revelat que és possible suprimir completament la probabilitat d'afterpulsing a costa de deixar un t_{off} mínim de 300 ns entre dues mesures consecutives, independentment del valor de V_{OV}. També s'ha observat que la probabilitat de detectar polsos deguts al DCR pot ser linealment reduïda a mesura que el t_{obs} del sensor és escurçat. El concepte que engloba la probabilitat de detectar una allau deguda a DCR en un t_{obs} donat s'anomena DCP (Dark Count Probability). S'obté a partir de $DCR \cdot t_{obs}$ quan $n_{rep}=1$. Així, un DCR de 40 kHz, mesurat a 1 V de V_{OV}, dóna una DCP d'aproximadament 10^{-4} polsos falsos quan el sensor és operat amb un t_{obs} de 10 ns. Tots els

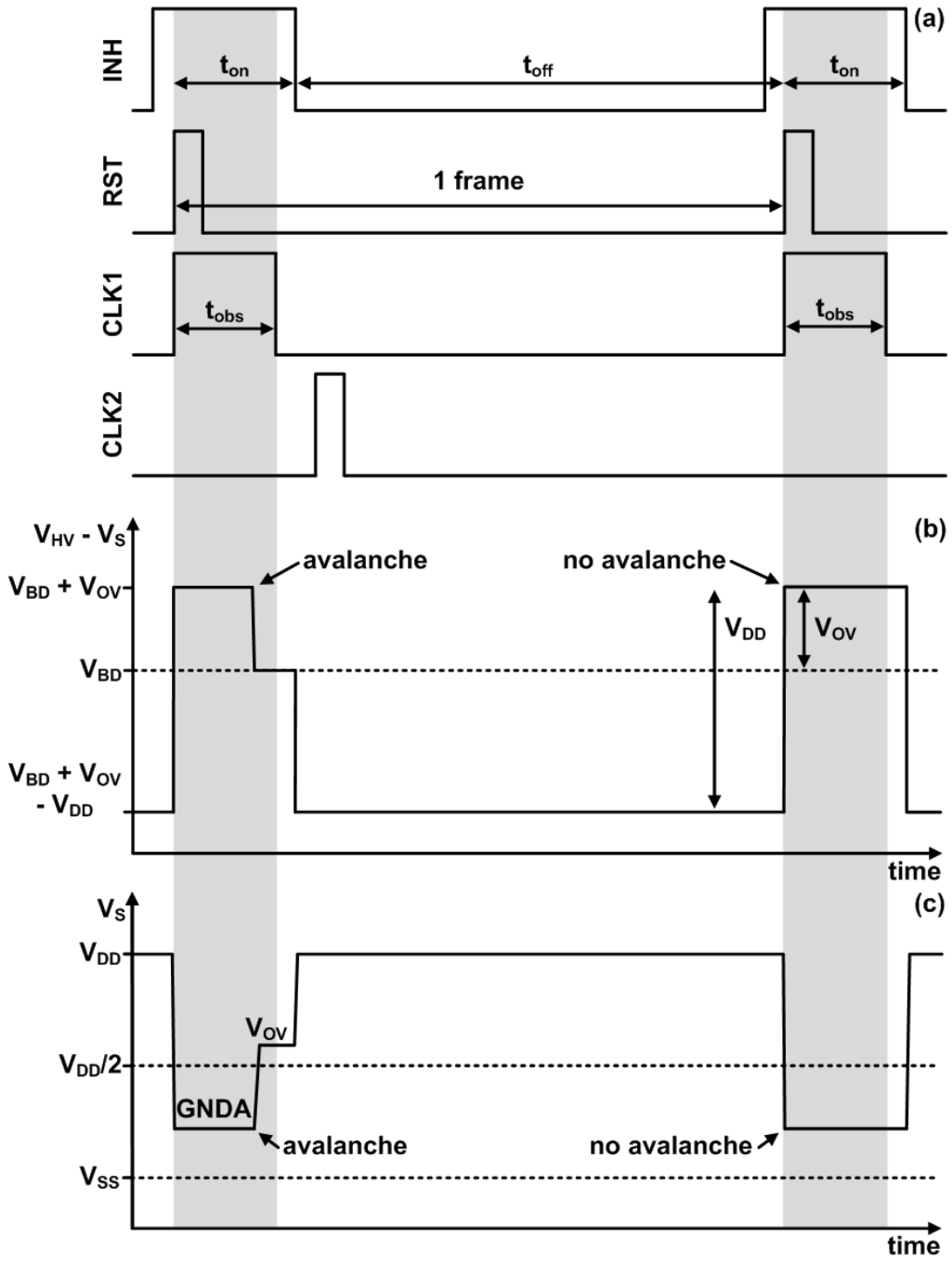

Figura R.4 Diagrama temporal amb les formes d'ona per operar el detector de GAPDs en el mode time-gated (a), polarització del GAPD (b) i resposta del node sensible en la topologia 2G (c).

circuits estudiats han demostrat tenir capacitat per operar el sensor a V_{OV} baixos i en el mode time-gated per reduir el soroll detectat, tal com es volia demostrar.

S'ha caracteritzat la probabilitat de crosstalk en funció del t_{obs} en una matriu de GAPDs operada en el mode time-gated. Per aquest propòsit s'ha utilitzat un detector de GAPDs format per 5 píxels organitzats en una fila, on els sensors comparteixen el mateix pou per tal d'incrementar el fill-factor. Aquest detector inclou un circuit de lectura en mode voltatge,

concretament el circuit de dues masses. Mitjançant la caracterització experimental del detector, s'ha observat que és possible eliminar el crosstalk elèctric entre GAPDs que comparteixen el mateix pou gràcies a la inhibició dels sensors a partir d'un temps suficientment curt just després d'haver-se disparat una allau. Els resultats s'han obtingut mitjançant dos experiments diferents. D'una banda, s'ha utilitzat una màquina FIB-SEM (Focused Ion Beam-Scanning Electron Microscopy) de doble feix per enfocar un feix d'electrons amb un spot nanomètric en un dels sensors de la matriu. No obstant, observar una resposta clara als sensors veïns mitjançant aquest experiment és difícil com a conseqüència de la càrrega progressiva de l'òxid. S'han pogut obtenir només resultats parcials. D'altra banda, la utilització del patró de soroll generat per un sensor de la matriu per quantificar el crosstalk als sensors veïns ha permès una caracterització molt més detallada. Malgrat tot, s'ha trobat una bona concordança entre les dues mesures, i també amb la teoria i les simulacions realitzades mitjançant ISE-TCAD. Els resultats indiquen que t_{obs} grans de 37 ns generen una probabilitat de crosstalk del 2.6 % al primer veí i del 0.25 % al segon veí. Aquest valor es manté constant a mesura que es redueix el t_{obs}, fins que a 7 ns el percentatge comença a disminuir. Per un t_{obs} de 3.7 ns, la probabilitat de crosstalk és del 0.23 %. A banda d'això, el crosstalk òptic és negligible donat el nombre reduït de portadors de càrrega que es genera a cada allau gràcies a la integració monolítica del sensor amb el circuit de lectura.

4. Disseny i caracterització de grans matrius en un procés HV-CMOS

Un punt molt important en el desenvolupament d'una nova tecnologia orientada a rastrejar partícules té lloc quan es caracteritza el comportament de l'esmentada tecnologia en una sèrie de beam-tests. En un beam-test, s'analitza la resposta del detector prototip a partícules altament energètiques. Si els resultats no són satisfactoris, el beam-test pot invalidar la tecnologia proposada com una tecnologia apta per rastrejar partícules.

S'ha dissenyat i fabricat un primer prototip d'una matriu de píxels de GAPDs com a prova de concepte de l'esmentada tecnologia en detectors de partícules altament energètiques. Per tant, no s'han inclòs tècniques per mitigar els efectes de la radiació present als col·lisionadors ni tampoc electrònica per processar en el mateix xip la informació generada. La matriu té una àrea sensible total d'1 mm x 1 mm, la qual va ser escollida per incrementar la probabilitat d'observar esdeveniments durant el beam-test del detector, i els píxels s'organitzen en 10 files per 43 columnes. L'àrea, l'estructura i el mode d'operació dels fotodíodes són els mateixos que els descrits a la secció anterior. Els píxels integren el circuit de lectura en mode voltatge amb la topologia de les dues masses, juntament amb l'electrònica per operar el mode time-gated. El circuit de lectura està col·locat a la part superior de cada píxel, entre dues files consecutives de sensors (veure Fig. R.5). Amb el propòsit de maximitzar el fill-factor de la matriu, tots els

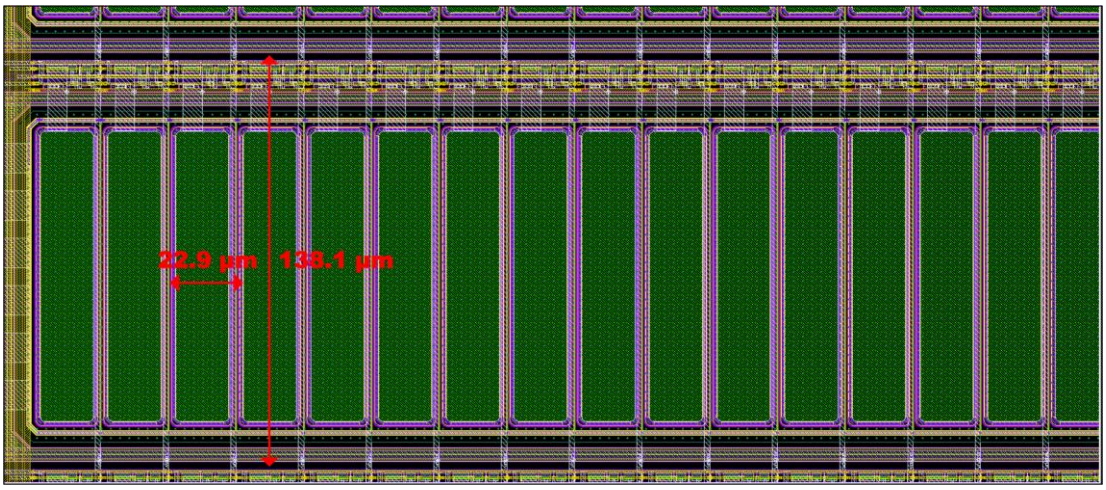

Figura R.5 Fila de GAPDs amb els seus corresponents circuits de lectura.

GAPDs d'una mateixa fila comparteixen el mateix pou, generant així un macropíxel de 43 GAPDs. No obstant, la introducció de l'anell de guarda per evitar la ruptura prematura del dispositiu genera una separació mínima entre dos GAPDs veïns d'1.7 µm en la direcció horitzontal. Com a conseqüència, el detector presenta un pitch (mida total del píxel) de 22.9 µm (amplada) x 138.1 µm (alçada, incloent el circuit de lectura), i un fill-factor del 67%. Tot i que aquest valor és superior als fill-factors habituals, encara ha de ser augmentat per satisfer els requisits que els futurs col·lisionadors lineals demanen als sistemes detectors.

L'esquema del píxel es mostra a la Fig. R.6, juntament amb el retard introduït per cada element. Cada píxel està format per un GAPD, transistors actius per inhibir (M_{P0}) i resetejar (M_{N0}) el sensor segons el mode d'operació time-gated i un circuit de lectura en mode voltatge amb la topologia de les dues masses. D'entre tots els circuits de lectura dissenyats i caracteritzats amb anterioritat, el circuit amb la topologia de les dues masses s'ha escollit per ser implementat en un detector amb un nombre considerable de píxels perquè és el que presenta una menor ocupació d'àrea. Així, el circuit de lectura de la matriu de 10 x 43 píxels comprèn un inversor CMOS (M_{P1}-M_{N1}), una cel·la de memòria d'1 bit (M_{N2}-M_{P2}-M_{N3}) i una porta de pas (M_{N4}). Els senyals de control RST, INH i CLK1 són comuns pera tots els píxels de la matriu, mentre el senyal CLK2 és compartit només pels píxels d'una mateixa fila. El transistor M_R, present en la primera versió del circuit, ha estat eliminat per reduir l'àrea i la capacitat paràsita del node V_S. La capacitat paràsita associada a aquest node té un valor de 15.75 fF, mentre que la capacitat del fotodíode és de 540.19 fF a 1 V de V_{OV}. La matriu es llegeix seqüencialment per files. Per aquest propòsit, els píxels d'una mateixa columna estan directament connectats a un únic buffer de sortida, el qual alimenta un pad de sortida. Per tant, aquesta configuració requereix 43 pads de sortida, més 13 pads d'entrada pels senyals de control (RST, INH, CLK1 i deu CLK2). Es necessita un total d'1.65 ns per llegir un píxel després d'haver-se disparat una allau (1.33 ns de retard degut al píxel, 0.26 ns degut al buffer i 0.95 ns degut al pad).

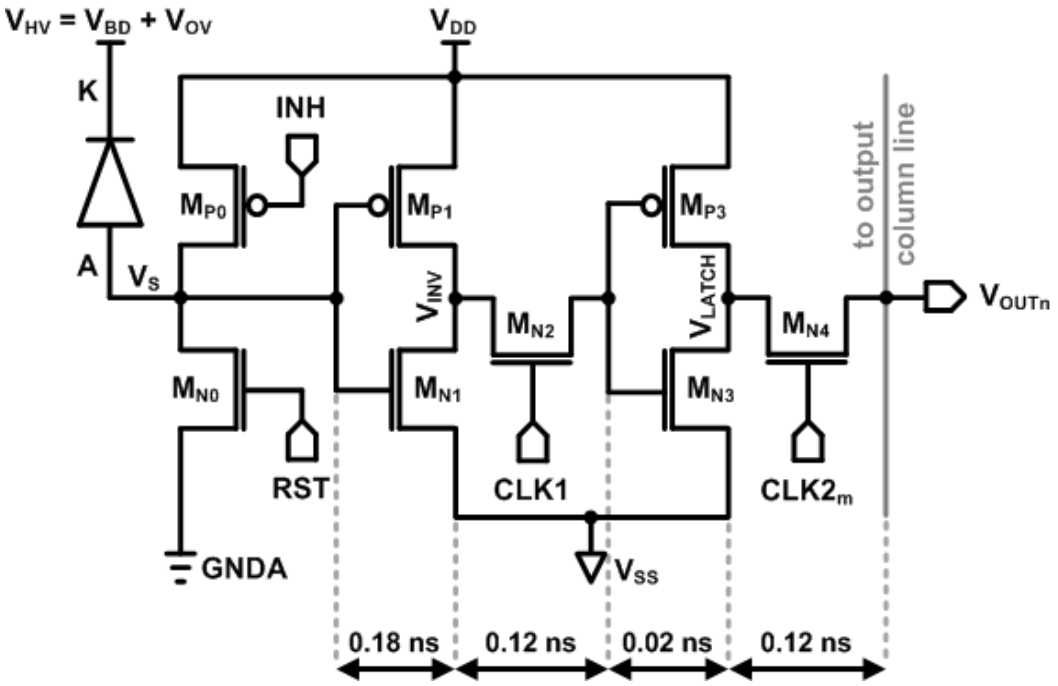

Figura R.6 Esquema del píxel time-gated amb sortida digital en la tecnologia CMOS estàndard HV-AMS 0.35 µm. V_{OUTn} està connectat a la columna de sortida n.

La caracterització del detector s'ha realitzat mitjançant una placa de desenvolupament DE0-Nano basada en una FPGA Cyclone IV d'ALTERA, la qual s'ha utilitzat per generar els senyals de control dels píxels, comptar el nombre de polsos generats i gestionar la comunicació amb un ordinador mitjançant un xip FTDI i un USB. D'aquest detector, s'ha caracteritzat l'afterpulsing, el DCR, la PDP, el rang dinàmic, la capacitat de generar imatges bidimensionals, i els efectes que tenen els canvis de temperatura en el soroll i la sensibilitat del sensor. Els resultats obtinguts demostren que l'operació time-gated és eficient en termes de reducció de soroll també en matrius amb un nombre considerable de píxels. A més, la reducció de soroll permet millorar el valor de certs paràmetres com el rang dinàmic, la resolució espacial i el contrast.

Així, s'ha observat que es pot eliminar la presència d'afterpulses amb un t_{off} mínim d'aproximadament 200 ns entre dues mesures consecutives, independentment del valor de V_{OV}. També s'ha detectat que la mitjana del DCR per tots els píxels de la matriu és de 67 kHz a 1 V de V_{OV} i temperatura ambient. A causa de l'àrea elevada del sensor, que va ser escollida per satisfer els requisits imposats pels futurs col·lisionadors lineals, el DCR mesurat és superior a altres valors que poden trobar-se a la literatura. No obstant, la DCP per píxel pot ser reduïda a aproximadament 10^{-4} polsos falsos quan el sensor és operat amb un t_{obs} de 4 ns. Aquesta situació resulta en l'increment del rang dinàmic d'entrada del sensor, el qual passa de 9.21 a 12.84 bits en reduir el t_{obs} de 1274 ns a 14 ns, i per tant també en un millor contrast. Els avantatges proporcionats pel mode d'operació time-gated també s'han apreciat en la generació d'imatges

bidimensionals. Per aquest propòsit, la matriu de GAPDs ha estat acoblada a una lent estàndard. El sistema matriu-lent s'ha col·locat a la distància adequada al davant d'un objecte. L'objecte s'ha il·luminat amb un làser polsat, els períodes d'emissió del qual tenen un valor constant de 22 ns i ocorren durant la part inicial del t_{obs} del sensor. Les imatges generades per la matriu de GAPDs amb diferents t_{obs} des de 1274 ns fins 34 ns es mostren a la Fig. R.7. La reducció del soroll detectat amb t_{obs} curts permet reproduir l'objecte amb un millor contrast. A banda d'això, la caracterització tèrmica del detector mostra que és possible reduir el DCR a 9.8 kHz quan es disminueix la temperatura de treball a -20 ºC. També s'ha mesurat el consum de potència, el qual és degut exclusivament al comportament dinàmic dels circuits de lectura (10 μW/MHz) i en major mesura dels pads de sortida (295 μW/MHz). La contribució dels pads de sortida podria ser reduïda mitjançant un pad LVDS (Low-Voltage Differential Signaling).

S'ha investigat la resposta de la matriu de GAPDs en la detecció de partícules altament energètiques en una sèrie de beam-tests, els quals han tingut lloc al CERN i a DESY. Pels dos beam-tests que s'han realitzat al CERN s'han utilitzat pions de 120 GeV, mentre que el beam-test a DESY s'ha fet amb electrons de 6 GeV. El muntatge experimental consta de dos xips amb una matriu de GAPDs cadascun, un sistema de referència format per detector Schottky i un telescopi EUDET/AIDA, i una TLU (Trigger Logic Unit) per distribuir el senyal de trigger. El muntatge experimental durant la realització del beam-test al CERN es mostra a la Fig. R.8. Cada xip està col·locat en una PCB i està connectat a una placa de control basada en una FPGA

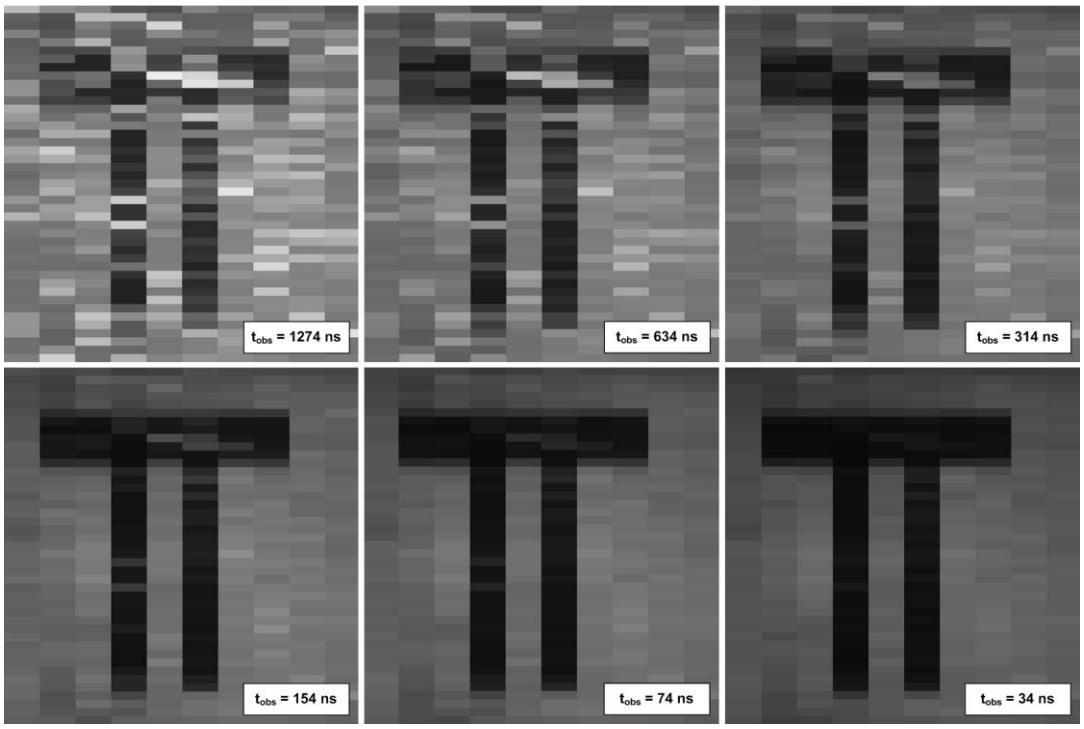

Figura R.7 Imatge d'un model amb diversos t_{obs}. El model és ser il·luminat amb un làser polsat, el qual presenta un període actiu de 22 ns dins del t_{obs} del sensor.

Cyclone IV d'ALTERA. El detector Schottky es troba en una tercera PCB. Les PCBs amb les matrius de GAPDs i el detector Schottky es troben a l'interior d'una caixa metàl·lica, la qual serveix per alinear els dispositius i protegir els sensors de fonts de llum no controlades. La caixa metàl·lica es troba entre els dos braços, amb 3 plans sensors cadascun, del telescopi EUDET/AIDA. Per tal de reduir la dispersió en la trajectòria de les partícules, els xips amb les matrius de GAPDs s'han aprimat fins a 250 μm. A més, cada xip està connectat directament a la seva PCB sense l'encapsulat, i la PCB està foradada a la regió de sota el detector. El programari EUtelescope reconstrueix les traces de les partícules a través a través dels 6 braços del telescopi. La interpolació de les traces permet determinar a través de quin píxel de la matriu han passat les partícules. Els beam-tests al CERN han permès comprovar i millorar el rendiment del muntatge proposat, així com verificar per primera vegada que els GAPDs poden detectar MIPs. A causa de problemes tècnics durant els beam-tests no va ser possible obtenir un elevat nombre d'estadística o mesurar l'eficiència detectora d'aquesta tecnologia. La correlació entre la matriu de GAPDs i el telescopi EUDET/AIDA es mostra a la Fig. R.9.

La caracterització detallada de la matriu de GAPDs ha permès quantificar el grau de compliment dels requisits demanats pels futurs col·lisionadors lineals als sistemes detectors. En el cas de l'ocupació, tant ILC com CLIC demanen que sigui inferior a l'1% incloent el soroll de fons. A ILC, els 0.004 hits/cm^2/BX de soroll de fons, els 2820 BXs per tren i els 337 ns de separació entre BX i BX indueixen $8 \cdot 10^{-8}$ hits de fons/GAPD/BX tenint en compte l'àrea sensible de 20 μm x 100 μm per píxel i la possibilitat de llegir el detector després de cada BX. A CLIC, en canvi, es tenen 0.87 hits/cm^2/GAPD, 312 BXs per tren i 0.5 ns de separació entre BX i BX, els quals generen $5.43 \cdot 10^{-3}$ hits de fons/GAPD/tren. A CLIC, donada la separació de 0.5 ns entre BX i BX, resulta impossible aplicar el mode d'operació time-gated o llegir el detector entre BX i BX. Per aquest motiu, els càlculs es presenten respecte la durada d'un tren sencer. Tanmateix, en el cas dels detectors de GAPDs el patró de soroll generat pel sensor domina l'ocupació. Per tal de minimitzar aquest problema, la matriu proposada en aquesta tesi funciona en el mode time-gated. A més, la reducció de la temperatura de treball permet obtenir uns millors resultats. Així, es calcula que a ILC es tindran $1 \cdot 10^{-5}$ polsos de soroll/GAPD/BX sota les condicions d'1 V de V_{OV}, 1 ns de t_{obs}, 300 ns de t_{off} i -20 ºC de temperatura. En canvi, a CLIC es tindran $2 \cdot 10^{-2}$ polsos de soroll/GAPD/tren a 1 V de V_{OV}, mode d'operació free-running i -20 ºC de temperatura. La diferència entre els hits de fons i els comptes de soroll és d'entre 3 (ILC) i 1 (CLIC) ordre de magnitud, cosa que pot amenaçar la utilització dels detectors de GAPDs en futurs col·lisionadors de partícules. Per mantenir els comptes de soroll per sota dels hits de fons, es pot realitzar una AND lògica de dos o més píxels solapats en diferent nivells del detector. En aquest cas, s'induirien $1 \cdot 10^{-10}$ polsos de soroll/GAPD/BX i $4 \cdot 10^{-4}$ polsos de soroll/GAPD/tren a ILC i CLIC, respectivament, i així la DCP seria inferior als hits de fons en

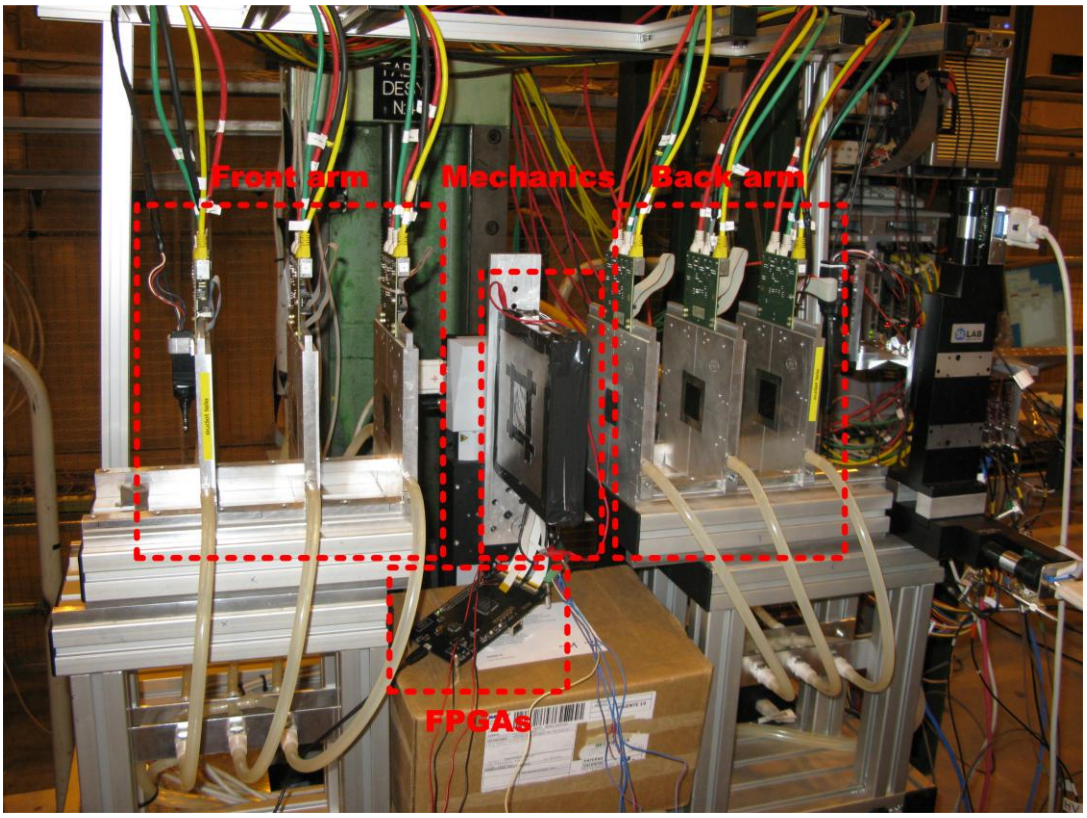

Figura R.8 Muntatge utilitzat al beam-test del CERN.

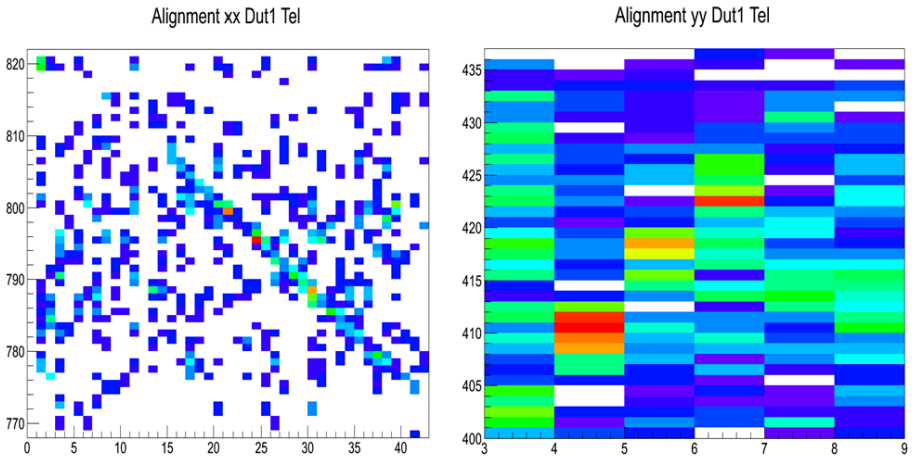

Figura R.9 Correlació entre la matriu de GAPDs i el telescopi EUDET/AIDA.

ambdós col·lisionadors. Els efectes de la radiació sobre la matriu de GAPDs no s'han investigat, però es creu que suposarien un increment del DCR d'entre un factor 3 i 4 a ILC i d'un factor 2 a CLIC després de 10 anys d'operació. Aquest agreujament del DCR no representa un agreujament significatiu de la DCP respecte els hits de fons. Tanmateix, caldria sotmetre la matriu de GAPDs a una campanya d'irradiació per tenir resultats de primera mà.

5. Més millores per les tecnologies GAPD

Entre altres especificacions molt severes, un fill-factor del 100% és demanat pels futurs col·lisionadors lineals als sistemes detectors. En el cas particular dels GAPDs, la presència d'àrees no sensibles com a conseqüència de l'anell de guarda per evitar la ruptura prematura del fotodíode, juntament amb els circuits electrònics monolíticament integrats per millorar la resposta del detector, indueixen fill-factors baixos que rarament excedeixen el 10%. A més, en aquelles tecnologies amb un node tecnològic inferior a 0.25 μm, les màscares que els dissenyadors introdueixen al layout per bloquejar el STI (Shallow Trench Isolation), i evitar així un increment dràstic del DCR, empitjoren la situació. En aquesta tesi, les tecnologies 3D s'han explorat com una solució per superar la limitació del fill-factor en detectors de GAPDs. Concretament, s'ha analitzat quin és el màxim fill-factor que es pot aconseguir en una matriu de GAPDs en la tecnologia CMOS estàndard Global Foundries 130 nm integrada en 3D per Tezzaron. A més, també s'ha dissenyat una matriu de GAPDs amb l'esmentada tecnologia.

L'anàlisi realitzat mostra que és possible aconseguir fill-factors d'entre el 66% i el 96% amb diferents arquitectures de matriu i un circuit de lectura d'àrea mínima (veure Fig. R.10). El circuit de lectura està basat en la topologia de les dues masses i inclou electrònica per operar el sensor en el mode time-gated. El disseny final està format per una matriu de 48 x 48 píxels de GAPDs, la qual s'ha dividit en dues submatrius de 48 x 24 píxels de GAPDs amb una arquitectura diferent cadascuna. De totes les estructures estudiades, s'han escollit per la implementació final les dues que presenten una major simplicitat i per tant un menor risc. Així, la primera submatriu implementa sensors de 18 μm x 18 μm en una capa i els circuits de lectura a l'altra, obtenint d'aquesta manera un fill-factor del 66% (Fig. R.10-a). La segona submatriu es beneficia de la integració 3D per solapar les àrees no sensibles d'una capa amb les àrees sensibles de l'altra. A més, també utilitza dues àrees sensibles diferents per maximitzar tant com sigui possible el solapament entre capes. Està basada en una estructura de quatre píxels. Tres sensors amb una àrea de 18 μm x 18 μm juntament amb els circuits de lectura dels quatre píxels es troben en una capa. El quart sensor, el qual presenta una àrea de 30 μm x 30 μm, està col·locat estratègicament a l'altra capa per solapar els circuits de lectura i la major part de l'àrea no sensible dels sensors de 18 μm x 18 μm. Aquesta estructura genera un fill-factor del 92% (Fig. R.10-b). Les TSVs (Through-Silicon-Vias), necessàries en aquesta tecnologia per connectar els circuits electrònics amb els pads d'entrada i sortida així com per controlar el procés de fabricació del xip, s'han col·locat als circuits de lectura quan ha estat possible o bé entre dos sensors. La matriu de 48 x 48 píxels es llegeix seqüencialment per files durant els períodes t_{off}, de manera semblant al procediment descrit anteriorment per la matriu de 10 x 43 píxels. Tot i que s'ha completat el disseny de la matriu, aquesta no s'ha fabricat com a

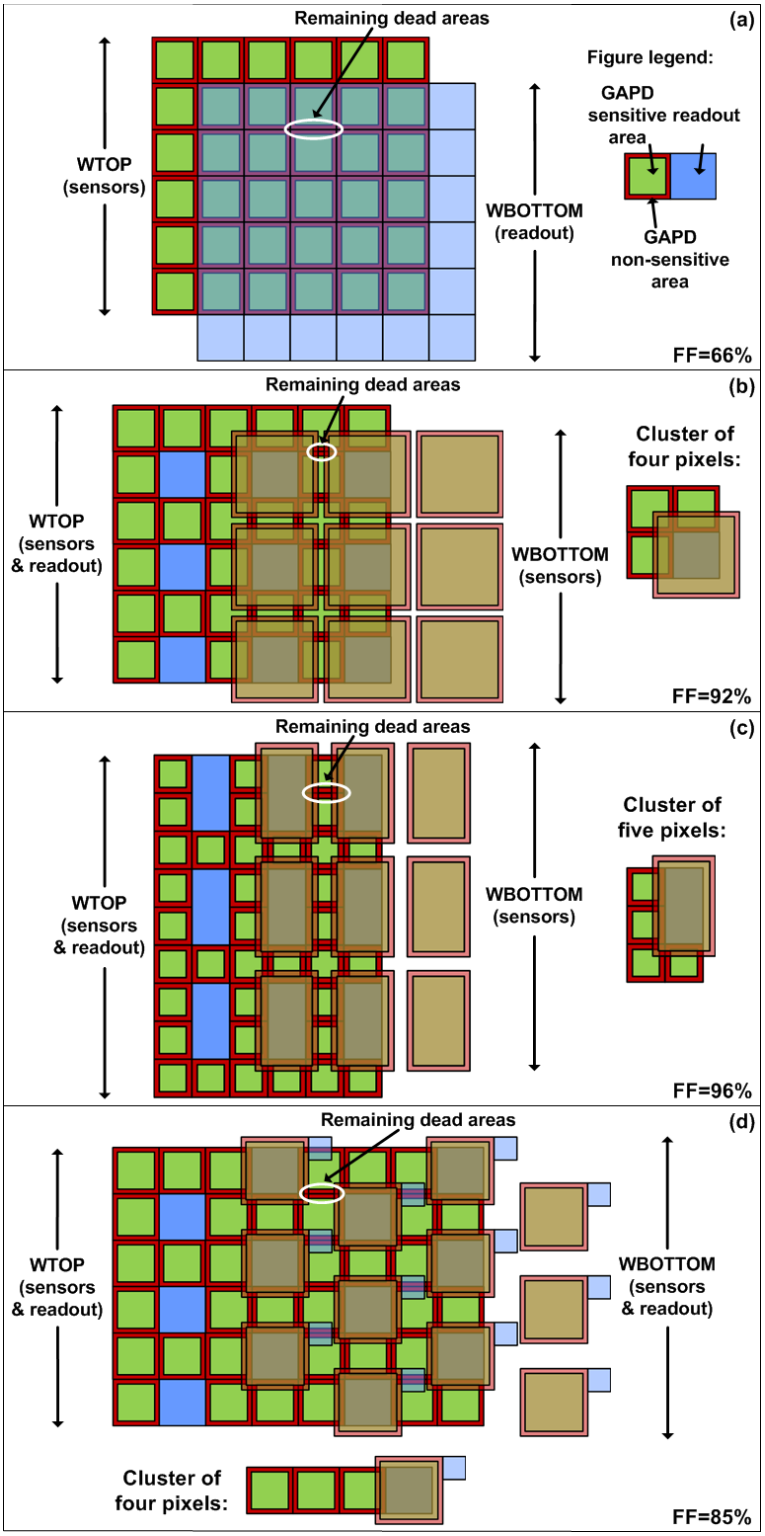

Figura R.10 Anàlisi del fill-factor assolible amb diferents arquitectures de matriu i considerant les normes de disseny de la tecnologia Global Foundries 130 nm/Tezzaron 3D. Els sensors i els circuits de lectura no estan a escala.

conseqüència dels retards continus en les dates d'inici del procés de fabricació propis de les tecnologies 3D.

A més, també s'ha investigat la possibilitat de millorar el rendiment de la tecnologia GAPD en aplicacions dedicades a la detecció de llum. D'una banda, s'ha proposat l'operació time-gated per ampliar el rang de sensibilitat dels dSiPMs (digital Silicon PhotoMultipliers), detectors de píxels que també estan basats en GAPDs i són àmpliament utilitzats en el camp de la generació d'imatges. Els experiments realitzats han permès observar que períodes t_{obs} curts generen un nombre reduït de píxels disparats per fenòmens de soroll i per tant la mínima irradiació necessària per detectar senyal es redueix. Així, dSiPMs actius només durant un interval de temps de l'ordre dels nanosegons poden detectar intensitats molt dèbils, cosa que amplia el rang dinàmic del detector mentre es manté el fill-factor aconseguit per disseny. D'altra banda, s'han estudiat diverses tècniques de correcció que permeten minimitzar els efectes de les no-uniformitats que típicament són presents en matrius de GAPDs, amb la finalitat d'incrementar el contrast dels sistemes de visió basats en aquesta tecnologia. S'han utilitzat algorismes de calibració píxel a píxel basats en mètodes lineals i no-lineals per tal de suprimir al màxim l'elevada desviació que habitualment s'observa en la resposta de les matrius de GAPDs. Com a conseqüència de l'aplicació d'aquestes tècniques, els nivells de representació que estan disponibles per representar una imatge, i per extensió el contrast, augmenten. No obstant, a causa de la resposta no-lineal dels GAPDs amb la irradiància, els millors resultats s'aconsegueixen amb els mètodes no-lineals. Aquests últims dos experiments aquí descrits s'han realitzat amb la matriu de 10 x 43 píxels.

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2. E. Vilella, O. Alonso, A. Montiel, A. Vilà, and A. Diéguez, "A low-noise time-gated single-photon detector in a HV-CMOS technology for triggered imaging", *Sens. Actuators A: Phys.*, vol. 201, pp. 342-351, 2013.

3. E. Vilella, O. Alonso, and A. Diéguez, "3D integration of Geiger-mode avalanche photodiodes aimed to very high fill-factor pixels for future linear colliders", *Nucl. Instr. Methods Phys. Res. Sect. A*, in press, 2013.

4. E. Vilella, and A. Diéguez, "Readout schemes for low noise single-photon avalanche diodes fabricated in conventional HV-CMOS technologies", *Microelectron. J.*, in press, 2013.

5. E. Vilella, O. Alonso, J. Trenado, A. Vilà, R. Casanova, M. Vos, L. Garrido, and A. Diéguez, "A test beam setup for the characterization of the Geiger-mode avalanche photodiode technology for particle tracking", *Nucl. Instr. Methods Phys. Res. Sect. A*, vol. 694, pp. 199-204, 2012.

6. E. Vilella, and A. Diéguez, "A gated single-photon avalanche diode array fabricated in a conventional CMOS process for triggered applications", *Sens. Actuators A: Phys.*, vol. 186, pp. 163-168, 2012.

7. E. Vilella, A. Comerma, O. Alonso, D. Gascon, and A. Diéguez, "Gated Geiger mode avalanche photodiode pixels with integrated readout electronics for low noise photon detection", *Nucl. Instr. Methods Phys. Res. Sect. A*, vol. 695, pp. 218-221, 2011.

8. E. Vilella, and A. Diéguez, "Avoiding sensor blindness in Geiger mode avalanche photodiode arrays fabricated in a conventional CMOS process", *J. Instrum.*, vol. 6, C12005, 2011.

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